REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2; PER IPC-6011.
   PCB SHALL BE MANUFACTURED USING I-SPEED OR EQUIVALENT.
2. MATERIALS:
   1. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101D/126. (MIN.TG 180)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED, THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
7. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. ALL VIA HOLES SHALL BE FILLED AND CAP PLATED AS PER TYPE VII REQUIREMENT. ONLY SOLDERMASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE BLUE.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 200M [0.00079"],.
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLAIN TO IPC6012, CLASS 2.
8. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO,UL FILE NUMBER, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
9. TEST REQUIREMENTS:
   1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
10. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
11. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
12. FINISHED PCB THICKNESS SHALL BE 0.065" +/-10%.
13. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.0032".
14. ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
15. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IN INTERNAL LAYERS.
16. FOR DETAILED STACKUP REFER "PROC112_STACKUP.pdf"
17. ENSURE THAT UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON PCB SILKSCREEN.

F1 BACKDRILLING TO BE DONE FROM L04 TO L12.

BACKDRILL: BOTTOM to L4-GND

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
-	7.99	+3.0/-3.0	PLATED	16

NOTES:
- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- VENDOR IS REQUIRED TO SELECT TOOLING FOR OVERDRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER.

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
F1 -	7.99	+3.0/-3.0	PLATED	16
-	8.0	+3.0/-4.0	PLATED	3524
•	16.0	+3.0/-3.0	PLATED	14
•	24.0	+3.0/-3.0	PLATED	20
•	28.0	+3.0/-3.0	PLATED	51
•	32.0	+3.0/-3.0	PLATED	22
•	36.0	+3.0/-3.0	PLATED	10
•	40.0	+3.0/-3.0	PLATED	9
•	40.0	+3.0/-3.0	PLATED	3
•	44.0	+2.0/-2.0	PLATED	25
•	44.0	+3.0/-3.0	PLATED	40
■	66.0	+3.0/-3.0	PLATED	2
■	90.0	+3.0/-3.0	PLATED	4
◍	118.0	+3.0/-3.0	PLATED	2
•	32.0	+3.0/-3.0	NON-PLATED	2
•	40.0	+3.0/-3.0	NON-PLATED	2
•	44.0	+2.0/-2.0	NON-PLATED	2
•	62.0	+2.0/-2.0	NON-PLATED	2
◍	108.0	+3.0/-3.0	NON-PLATED	9
◍	126.0	+3.0/-3.0	NON-PLATED	2
▬	48.0x22.0	+3.0/-3.0	PLATED	2
▬	48.0x24.0	+3.0/-3.0	PLATED	4
▬	62.0x24.0	+3.0/-3.0	PLATED	2
▬	66.0x32.0	+3.0/-3.0	PLATED	2
▬	68.0x34.0	+3.0/-3.0	PLATED	2
▬	82.0x24.0	+3.0/-3.0	PLATED	2
▬	86.0x32.0	+3.0/-3.0	PLATED	2

DETAIL-A(V-GROOVE DETAILS)
SCALE:NTS

IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	EDGE COUPLED MICROSTRIP	L1/L12	4.18	6.32	100	L2/L11
02	EDGE COUPLED MICROSTRIP	L1/L12	5.10	5.4	90	L2/L11
03	EDGE COUPLED MICROSTRIP	L1/L12	6.0	5.5	85	L2/L11
04	EDGE COUPLED MICROSTRIP	L1	6.56	4.94	80	L2
05	EDGE COUPLED MICROSTRIP	L1/L12	7.2	8.3	120	L3/L10
06	MICROSTRIP	L1	9.9	-	38	L2
07	MICROSTRIP	L1/L12	10.4	-	40	L2/L11
08	MICROSTRIP	L1/L12	6.5	-	50	L2/L11
09	EDGE COUPLED STRIPLINE	L3, L8,L10	4.07	7.93	100	L2/L4,L7/L9, L9/L11
10.	EDGE COUPLED STRIPLINE	L3, L8,L10	4.82	6.18	90	L2/L4,L7/L9, L9/L11
11.	EDGE COUPLED STRIPLINE	L8,L10	5.35	6.15	85	L7/L9,L9/L11
12.	EDGE COUPLED STRIPLINE	L3,L5	5.93	6.07	80	L2/L4,L4/L6
13.	EDGE COUPLED STRIPLINE	L10	6.4	5.6	76	L9/L11
14.	STRIPLINE	L3,L5, L8,L10	4	-	50	L2/L4,L4/L6, L7/L9,L9/L11
15.	STRIPLINE	L6	5.0	-	50	L5/L7
16.	STRIPLINE	L10	6.8	-	38	L9/L11
17.	STRIPLINE	L3,L5, L8,L10	6.25	-	40	L2/L4,L4/L6, L7/L9,L9/L11
18.						

LAYER STACKUP

LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS [INCHES]
PRIMARY SIDE SILKSCREEN			
PRIMARY SIDE SOLDERMASK			
L01 — PRIMARY SIDE	1.45oz.		0.0037
L02 — GROUND-PLANE-1	1oz.		0.0035
L03 — INNER-SIGNAL-1	0.5oz.		0.0043
L04 — GROUND-PLANE-2	1oz.		0.0035
L05 — INNER-SIGNAL-2	0.5oz.		0.0042
L06 — POWER-PLANE-1	1oz.		0.010
L07 — POWER-PLANE-2	1oz.		0.0043
L08 — INNER-SIGNAL-3	0.5oz.		0.0035
L09 — GROUND-PLANE-3	1oz.		0.0043
L10 — INNER-SIGNAL-4	0.5oz.		0.0035
L11 — GROUND-PLANE-4	1oz.		0.0043
L12 — SECONDARY SIDE	1.45oz.		0.0037
SECONDARY SIDE SOLDERMASK			
SECONDARY SIDE SILKSCREEN			

SIGNATURES		DATE
LAYOUT BY	UD	160822
REVIEWED BY	ZA	160822
APPROVED BY	AMB	160822

TEXAS INSTRUMENTS | PROC112

TDA4VM EDGE AI KIT

SIZE D | Rev B | SCALE: NONE | SHEET 1 OF 19