

J7AEP SOM - Dual Leo2.0 + HCPS Hera2.0 PDN-0A

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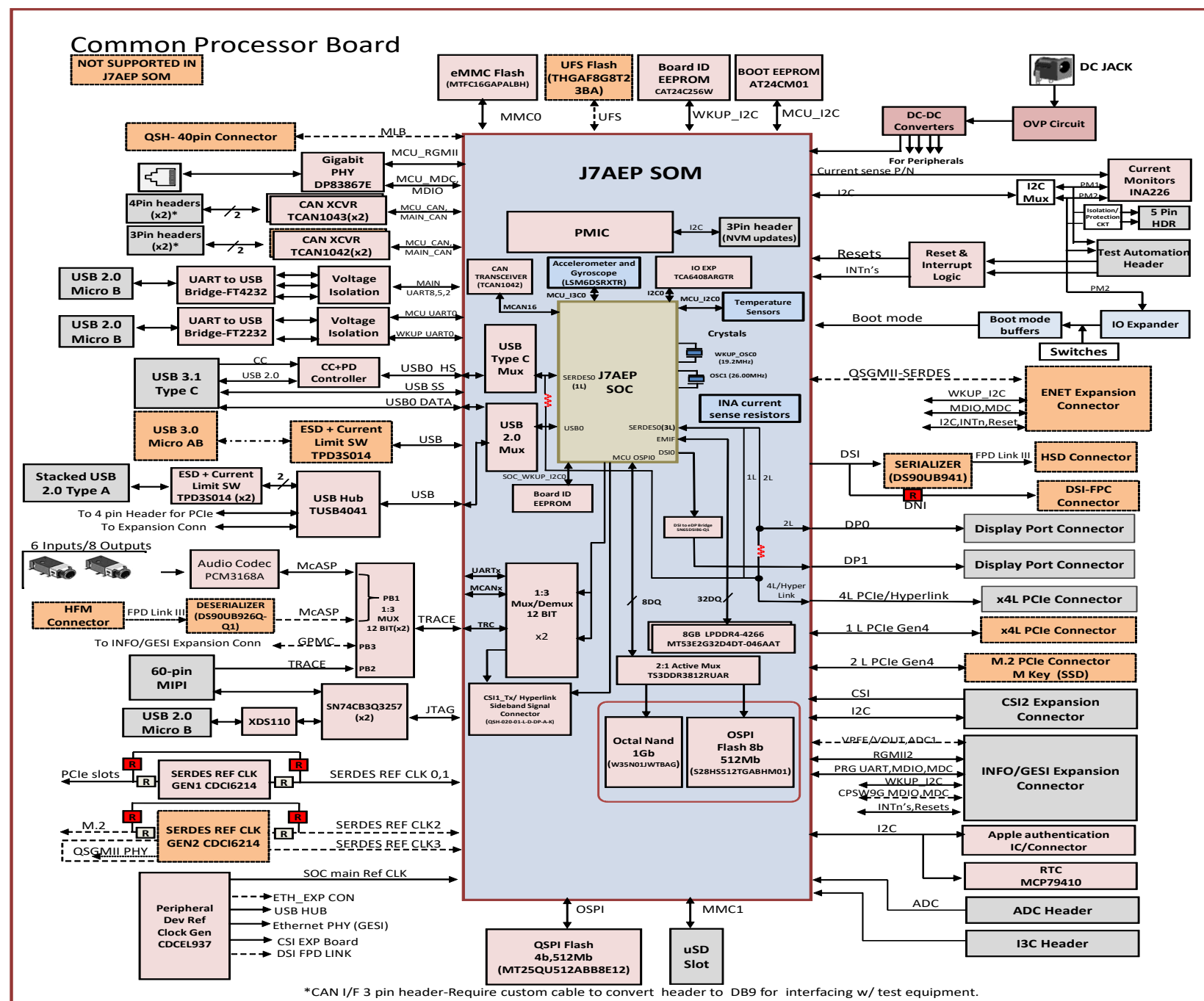
REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	01 JUNE 2021	Added Test Point for MCU_ONAND_CLK, ADC_EXT_TRIGGER0	Mistral Design Team		
	04 JUNE 2021	Following Caps are deleted as per TI comment VDDAR_CORE_0V85: C954, C954, C955 VDDAR_CPU_0V85: C2226, C2227, C2228 VDD_MCU_0V85: C425 VDD_CPU_AV5: C420, C403, C416 VDDAR_MCU_0V85: C967, C968, C970	Mistral Design Team		
	15 June 2021	Updated SoC symbol as follows: 1. Added "Symbol: v1.1 (date)" parameter to text for tracking symbol only changes. 2. Moved GPIO0_11 & GPIO0_12 from "MCU RGMIIT" (sub-symbol "K", pg17) to "General IO" (sub-symbol "M", pg16) to align GPIO's with similar interfaces with output buffers ref to VDDSHV2. 3. Optimized "DDR#_CSN#_Channel#" ball groups (pgs 11 & 12) within SoC symbol to match SDRAM symbol groups to reduce possiblity of net connection errors. Example ball group changes: From: To: DDR0_CSN0_0 (Ch A) DDR0_CSN0_0 (Ch A) DDR0_CSN0_1 (Ch B) DDR0_CSN1_0 (Ch A) DDR0_CSN1_0 (Ch A) DDR0_CSN0_1 (Ch B) DDR0_CSN1_1 (Ch B) DDR0_CSN1_1 (Ch B) Fixed DDR0 (pg11) SCH net connections on "DDR0_CSN#_Ch#" to correct SoC & SDRAM alignment.			
	16 June 2021	Removed the PBs SW2004 & SW2003 and updated the CAN_WKUP logic	Mistral Design Team		
	19 June 2021	Updated for TI review comments LEOA_FB_B3 Resistor divider values updated (Vdiv set to 1.5V) Renamed the VDD_MCUWK_0V85_REG to VDD_MCUWK_0V8_REG Hyperlink Sideband signal pinouts updated and added VSYS_IO_3V3	Mistral Design Team		
	21 June 2021	Updated for TI review comments 3T Caps added to input power of PMICs, Resistor Mux option removed for VIO_VIN	Mistral Design Team		
	23 June 2021	Removed the Vdividers from the PMIC Voltage monitor pins Updated the power supply of MOD2000 to VSYS_MCU_GPIORET_3V3 from VDD_MCU_GPIORET_3V3 Removed the resistor R21 and connected VCCA_3V3 directly to VIO_VIN pin of PMIC-A,B & C	Mistral Design Team		
	24 June 2021	Added SMD TPs for the unused Voltage mointor pins	Mistral Design Team		
	29 June 2021	Added 0E resistor b/w Gnd & U13-9	Mistral Design Team		
	29 June 2021	Updated the PU supply of I2C1_SCL_MUX/I2C1_SDA_MUX to VSYS_IO_3V3	Mistral Design Team		
	01 July 2021	Updated for TI review Comments Made PMIC B OSC32KCAP pin as NC Pull Up added to external EXT_I2C_Sxx Signals	Mistral Design Team		
	06 July 2021	UART5_TXD and RXD swapped Moved DDR0 de-embedding circuit to DDR1	Mistral Design Team		
	08 July 2021	SI_DDR_0&1_CA5 Signal Coupon Components removed, J2000 connector Pin 26 and 28 are made as NC	Mistral Design Team		
	12 July 2021	PCB back annotated SCH Updated	Mistral Design Team		
	14 July 2021	R294,R269,R365,R368 and R144 are made as DNI	Mistral Design Team		
	15 July 2021	SPI5_CS0 signal moved from J21.B17 to J21.F13.	Mistral Design Team		
	26 July 2021	500E resistors R238,R47,R48,R53,R265 are replaced with 499E, R150 is made as DNI	Mistral Design Team		
E1A	25 Aug 2021	SoC Symbol Updated: IO BANK LABEL in Block A and C is updated	Mistral Design Team		
E1B	13 OCT 2021	C491 and C476 is replaced by 10uF having MFR PART# GRT155C80E106ME13D Part L4, L8, L9 and L10 Inductors are replaced by 0.47uH Inductor	Mistral Design Team		
E1C	14 OCT 2021	R358 is Mounted and R359 is DNI'd	Mistral Design Team		
E1D	07 DEC 2021	Instruction given to fix power issue in U40(VCCA<=VCCB) is shown in page no 28 R357 and R367 DNI'd Heat sink with MFR_PART# 374424B00035G is added	Mistral Design Team		
E2	18 Nov 2021	Supply to the Pull Up resistor of I2C1_, I2C3_, I2C4_, I2C5 Instances: R274, R273, R257, R252,R275, R99, R307, R303, R269, R268 resistors pulled to VSYS_IO_3V3 Supply to the WKUP_I2C0 pull up resistors R160, R158 changed to VSYS_MCUIO_3V3 PMIC Wake-up logic changed at page 33 x2(C562, C563) 1uF is added to VDA_DLL_0V8 rail C491 and C476 is replaced with 10uF, 0805 package capacitor in VDA_DLL_0V8 rail Change in SoC Pin names: PMIC_WAKE0 to PMIC_WAKE0n VMON6_IR_VEXT1P8 to VMON_IR_VEXT0P8 Chabnge in schematic net names: H_PMIC_WAKE1 is changed to H_PMIC_WAKE1n H_PMIC_WAKE0 is changed to H_PMIC_WAKE0n MON6_IR_VEXT1V8 to MON6_IR_VEXT0V8 WAKE_FULL_ACTIVE to WAKE_FULL_ACTIVEn	Mistral Design Team		
	25 Nov 2021	PDN Diagram updated to PDN v1.3 NVMFS4C05NT1G is replaced with alternate part CSD16413Q5A Leo PMIC Part is replaced with production part numbers TPS65941421RWERQ1 and TPS65941120RWERQ1 for U17 and U5 respectively.			

REVISION HISTORY CONT'D

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	17 Dec 2021	R392 pulled to VSYS_IO_1V8 0E added between Gnd and Test pin2 of eDP Bridge PCB Revision changed to E2 External oscillator added to DSI to eDP bridge	Mistral Design Team	TI	
E3	24 Mar 2022	U51 MUX added to Audio I2C3 signals U52 Buffer added to DP0_HPDP signal Pull up option provided for I2C3(R402,R403)	Mistral Design Team	TI	
E4	02 sep 2022	Bulk capacitors were added to VDD_CPU_AVS rail Replaced 4x 0.47uF, 10V, 0402 caps (C108 - 111) with 1x new 100uF, 4V, 1210 Replaced 4x 22uF, 10V, 1206 caps (C123, 122, 66 & 77) with 4x new 100uF, 4V, 1210 (PN: GCM32ED70G107MEC4), Replaced C128&C131 with new 100uF, 4V, 1210 Cap Added 5x new 100uF, 4V, 1210 Correct TI SoC MFR# part used i,e XJ721S2GAALZ	Mistral Design Team	TI	
	13 Sep 2022	Replaced FL10 and FL11 with BLM21SP111BH1D(4A @ 125C, Zpk = 110ohm @ 100MHz) to reduce the IR Drop<1% target Replaced 4x 22uF, 10V, 1206 caps (C139, 81, 71 & 125) with 4x new 100uF, 4V, 1210 (PN: GCM32ED70G107MEC4) Removed top-side 3-T caps C133, 142 or 149 & placed 2x new 100uF, 1210 4V Cap DDR rail capacitor with MFR# C0402C103K5RACTU Capacitor is replaced with Murata GRM series capacitos i,e GRM155R71H103KA88D	Mistral Design Team	TI	
	15 Nov 2022	Replaced 6x 100uF, +/-20%, X7T, 4V, 1210 (PN: GCM32ED70G107MEC4) with 47uF, +/-20%, X7T, 4V, 1206 (PN:GCM31CD70G476ME02)at following 6x cap Ref Des: C66, 77, 108, 122, 123 & 131 DNI the following 3x cap Ref Des: C128, 571 & 572 Replaced 6x 100uF, +/-20%, X7T, 4V, 1210 (PN: GCM32ED70G107MEC4) with 47uF, +/-20%, X7T, 4V, 1206 (PN: GCM31CD70G476ME02) at following 6x cap Ref Des: C71, 81, 125, 133, 139 & 142 Replaced 11x 47uF, +/-20%, X7R, 6.3V, 1210 (PN: GCM32ER70J476ME19K) with 47uF, +/-20%, X7T, 4V, 1206 (PN: GCM31CD70G476ME02) at following 8x cap Ref Des: C90, 315, 62, 302, 93, 314, 65, 277, 276, 308, 309 & 301 Replaced 2x 100uF, +/-20%, X7T, 4V, 1210 (PN: GCM32ED70G107MEC4) with 47uF, +/-20%, X7T, 4V, 1206 (PN: GCM31CD70G476ME02)at following 2x cap Ref Des: C573 & 574 Replace 4x 47uF, +/-20%, X7R, 6.3V, 1210 (PN: GCM32ER70J476ME19K) with 100uF, +/-20%, X7T, 4V, 1210 (PN: GCM32ED70G107MEC4 at following 4x cap Ref Des: C28, 27, 69 & 70 Hera PMIC updated to rev 2.0	Mistral Design Team	TI	
	05 Jan 2023	Sch title updated to "J7AEP SOM - Dual Leo2.0 + HCPS Hera2.0 PDN-0A" Part description updated for U5- PMIC B, U17 PMIC-A & U2 PMIC-C	Mistral Design Team	TI	
	30 Mar 2023	R1 R2 R3 R4 R5 R6(50E_1%) is replaced by 49.9E_1% resistor Revieued the schematic for latest vE4 ECN v1.1, schematic is in align with vE4 ECN v1.1.	Mistral Design Team	TI	

SoM SYSTEM BLOCK DIAGRAM



PDN

TDA4AL/VL/VE Dual Leo2.0 + Hera1.0 Interim PDN-0A

(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TP56594**1120**RWERQ1 (Ti PN ID = **1**, MP Buck Rails = **1**, PG2.0 NVM ID = **20**)
 Leo PMIC-B, PN TP56594**1421**RWERQ1 (Ti PN ID = **1**, MP Buck Rails = **4**, PG2.0 NVM ID = **21**)
 Hera PMIC-C, PN LP8764**11A5**RQKRQ1 (MP Buck Rails = **1**, Ti PN ID = **1**, **PG1.0** NVM ID = **A5**)

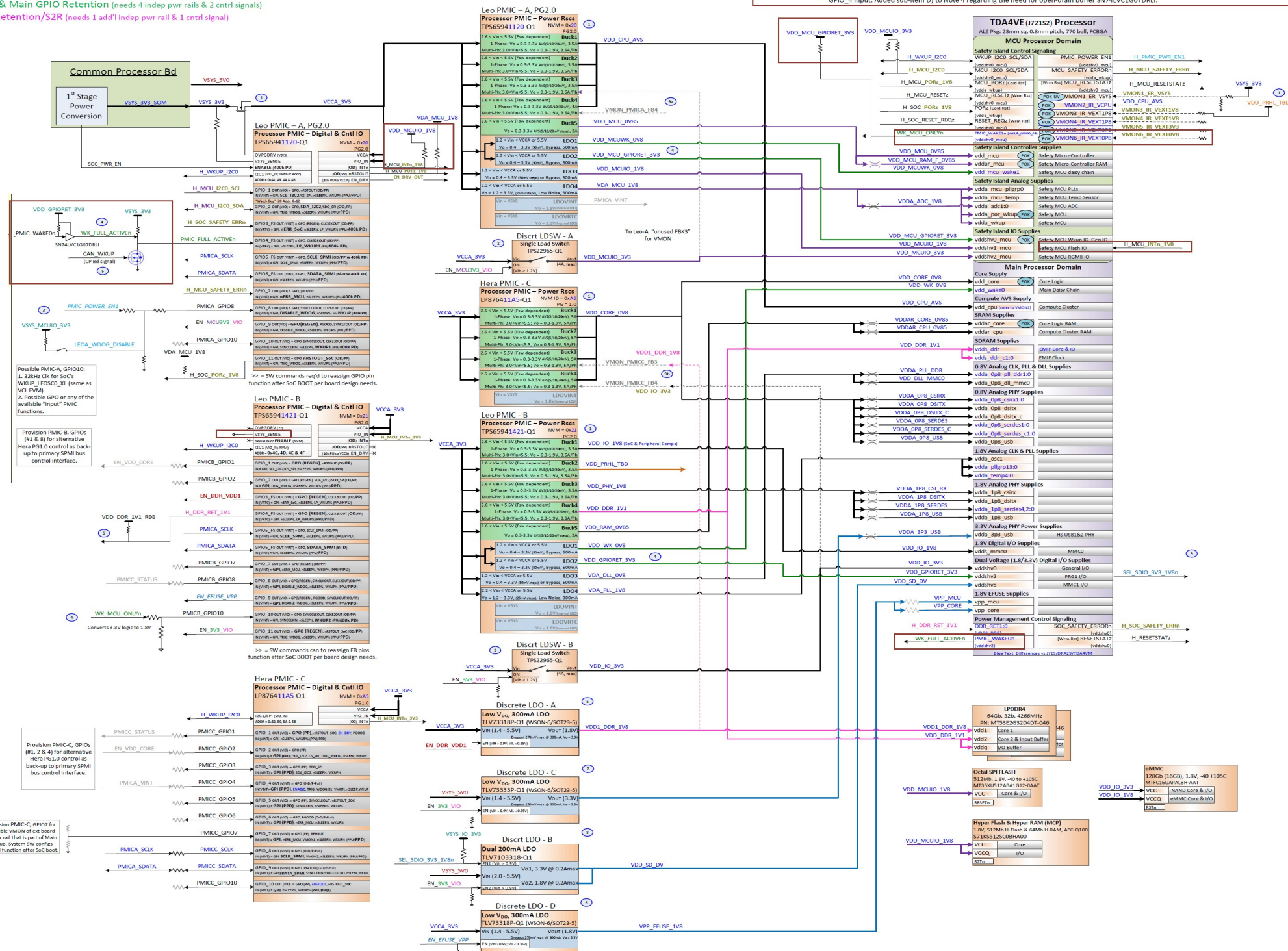
Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ isolated Main & **MCU power rails**
3. 2x SDRAMs: 32Gb, 4-Die, 32b, 4266MT/s, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:


- a. MCU Island/Only with Dual VIO (needs 4 indep pwr rails & 1 cntrl signal)
- b. MCU & Main GPIO Retention (needs 4 indep pwr rails & 2 cntrl signals)
- c. DDR Retention/S2R (needs 1 add'l indep pwr rail & 1 cntrl signal)

7. End Product Options:

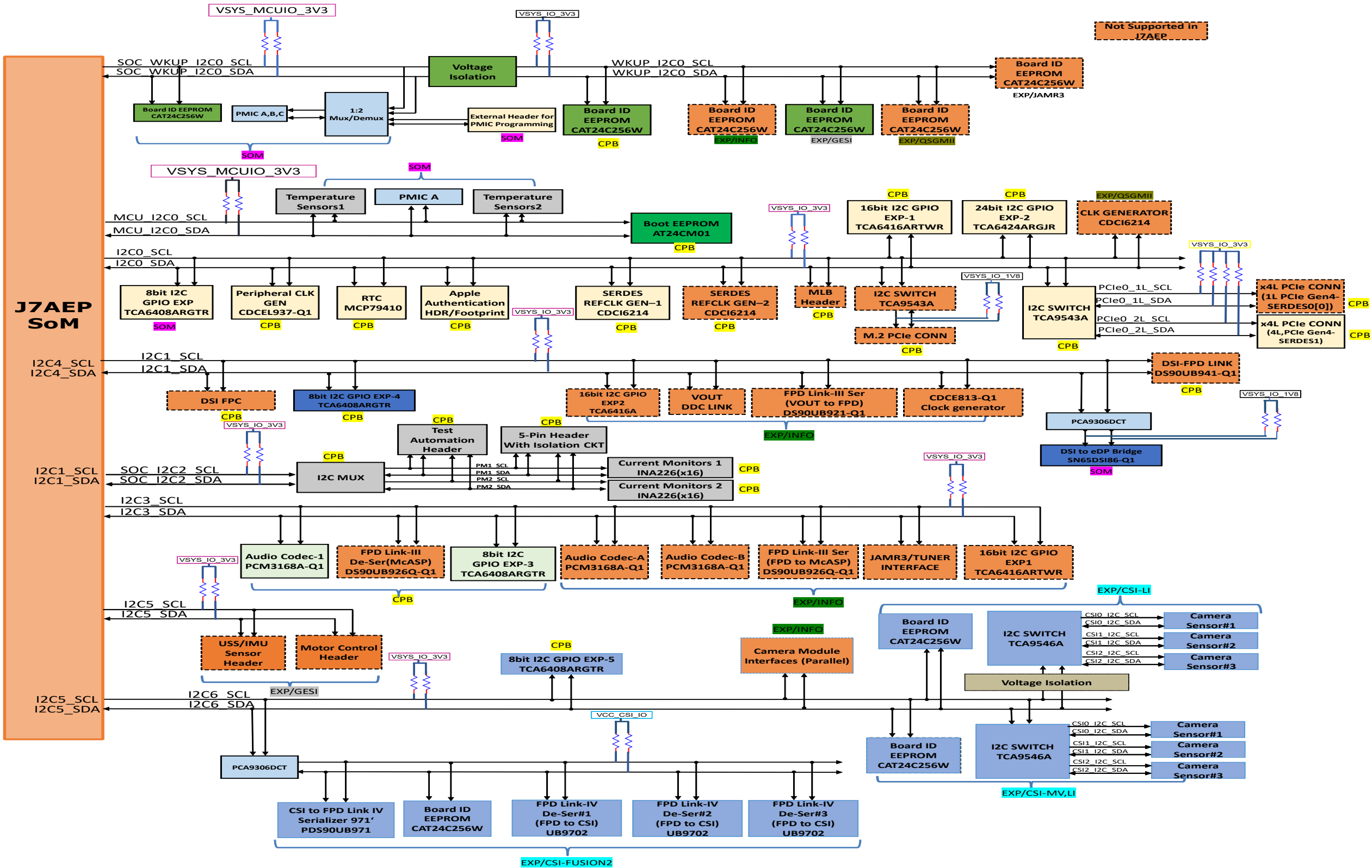
- a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs $V_{in} = 5V$)
- b. Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs $V_{in} = 5V$)
- c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)



V0.8	6/15/2021	<ol style="list-style-type: none"> 1. All 3x PMIC GPIO to function NVN defaults captured in block diagram per NVN settings review 2. Added "Italicized names" to legend for ID of PMIC GPIO functions, rails & signals that must be SW configured following SCo standard boot-up 3. Connecting EN_EFUSE_VPP control signal from PMIC to sense GPIOs if added are limited.
V0.9	6/16/2021	<ol style="list-style-type: none"> 4. Provision unused SCo VMON inputs for VDD_PRRH_TBD & easy access if add'l rails are desired for testing 1. Added PMIC_WAKE1 signal layout to AEP-SC block diagram since EVM pinmux will select this function for pkg bal K26 & signal name "WKUP_GPIO_49". 2. Added WK_MCU_ONLY & WK_FULL_ACTIVE signaling btw SCo & PMICs
V1.0	7/16/2021	<ol style="list-style-type: none"> 1. Updated PMIC-B block symbol with naming "MCU type 21". 2. Added Wires box and removed engineering review notes
V1.1	8/2/2021	<ol style="list-style-type: none"> 1. Updated I7 SC block symbol with adding "Processor Domain" & "Main Processor Domain" labels, replace prior use of "voltage Domain" by "Supply", remove "(L1V & 0 for LPDDR4X)" text from SDRAM Supplies description & adding PMIC_WAKE1 [default mode=full name].
V1.2	11/17/2021	<ol style="list-style-type: none"> 1. Updated "MCU_IN" net in K pull-up to VDD_MCUIO_V18 supply as an alternate & acceptable power rail that aligns to EVM SCH use of SCo's MCU_OSP1_CSNI/WKUP_GPIO_39 interface I/O that is referenced to VDDSHV1_MCU connected to VDD_MCUIO_V18. 2. Changed PMIC-R's VSENSE_SENSE from a "No Connect" to Gnd per SCH & PMIC review. 3. Updated following signal names to align with BGA name updates to clarify functionality: <ol style="list-style-type: none"> a. PMIC_WAKE1 & PMIC_WAKED by adding "n" suffix to reflect active low & pull-up or RS for open-drain operations. b. VMON6_IR_VEXT1P8 > VMON6_IR_VEXT0P8 to fix BGA name typo. 4. Add discrete FET to invert CAN_WKUP & "wired-AND" active low signal connection to PMIC-A, GPIO4
V1.3	11/15/2021	<ol style="list-style-type: none"> 1. Updated "wired-AND" circuitry to combine PMIC_WAKED & PMIC_WAKE1 to create PMIC_WAKE1_ACTIVE wake-up signal on PMIC-A, GPIO 4 input, added SW-Item C2 to Note 4 regarding the need for open-drain buffer SN74VLC1G07DRL.

Project : J7 EVM		Title PDN				
		Size	PROC118 001 J721S2XSOMG01EVM			Rev
		C				E4
		Date:	Tuesday, March 28, 2023		Sheet	5 of 39

SoM I2C TREE DIAGRAM



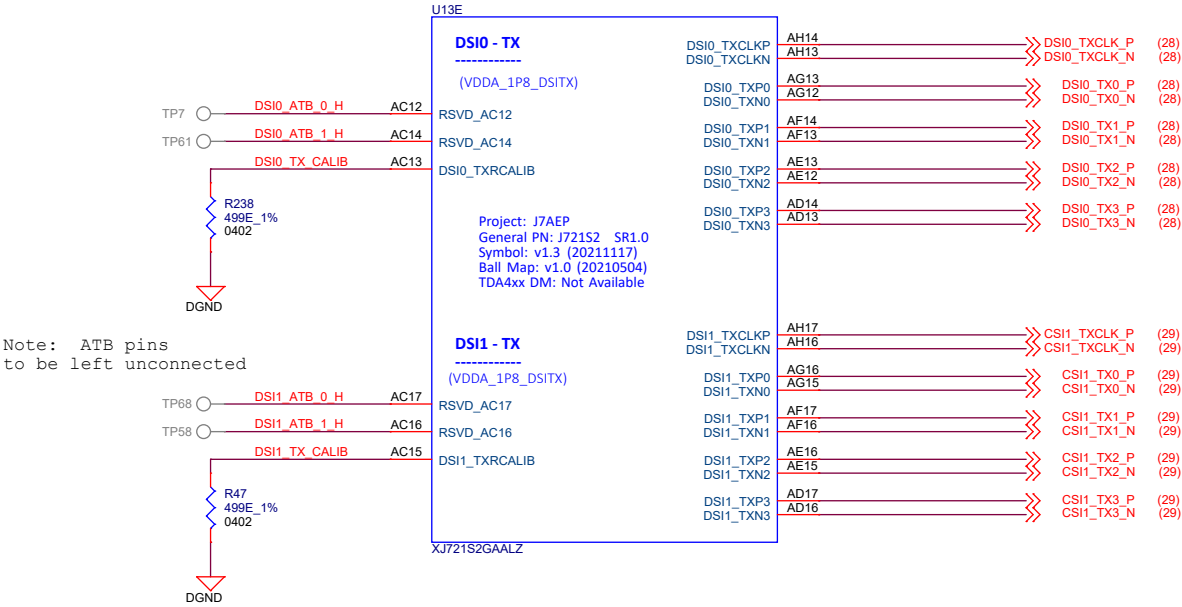
SoM I2C ADDRESS TABLE

Board	Interface name	Part#	Address	J7AEP Port mapping
EVM/SoM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0
EVM/CPB	Board ID EEPROM	CAT24C256W	0x51	
EXP/GESI	Board ID EEPROM	CAT24C256W	0x52	
EVM/SoM	PMICs	PMIC A: TPS659413	PMIC A: 0x48, 0x49, 0x4A & 0x4B	
		PMIC B: TPS659411	PMIC B: 0x4C, 0x4D, 0x4E & 0x4F	MCU_I2C0
		PMIC C: P876411A5RQKRQ1	PMIC C: 0x58, 0x59, 0x5A & 0x5B	
EVM/SoM	Temperature Sensors	TMP100NA/3K	0x48, 0x49	
EVM/SoM	PMIC A	PMIC A: TPS659413	PMIC A: 0x12	
EVM/CPB	Boot EEPROM	AT24CM01	0x50, 0x51	Main I2C0
EVM/SoM	8 bit I2C GPIO Expander	TCA6408ARGTR	0x21	
EVM/CPB	SerDes Clock gen #1 Optional	CDCI6214	Optional	
EVM/CPB	SerDes Clock gen #2	CDCI6214	0x77,0x76	
EVM/CPB	Pheriphal Clock Gen	CDCEL937-Q1	0x6D	
EVM/CPB	16bit I2C GPIO EXPANDER1	TCA6416ARTWR	0x20	
EVM/CPB	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22	Main I2C4
EVM/CPB	8 bit I2C GPIO Expander4	TCA6408ARGTR	0x20	
EVM/SoM	DSI TO eDP BRIDGE	SN65DSI86IPAPQ1	0x2C	
EVM/CPB	DSI FPC Connector	<connector interface>		Main I2C1
EVM/CPB	I2C Switch for Automation header		0x22	
EVM/CPB	Current Monitors and Header		0x40 to 0x4F	
EVM/CPB	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3
EVM/CPB	FPD Link iii Deserializer	DS90UB926Q-Q1	0x2C	
EVM/CPB	AUDIO IF Codec	PCM3168A-Q1	0x44	
EXP/CSI-FUSION2	I2C IO Expander	PCA9536DGKR	0x41	Main I2C5
EXP/CSI-FUSION2	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	0x3D	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x30	
EXP/CSI-FUSION2	CSI to FPD Link IV Serializer 971	UB971	0x18	
EXP/CSI-LI	Board ID EEPROM (Leopard Imaging Adapter)	CAT24C256W	0x52	
EXP/CSI-LI	I2C MUX Camera sensors	TCA9543APWR	0x70	
EXP/CSI-MV	Board ID EEPROM (Machine Vision Application)	CAT24C256W	0x52	
EXP/CSI-MV	Camera Sensor #1	IMX264LQR-C	TBD	
EXP/CSI-MV	Camera Sensor #2	IMX264LQR-C	TBD	
EXP/CSI-MV	I2C MUX Camera sensors	TCA9543APWR	0x70	

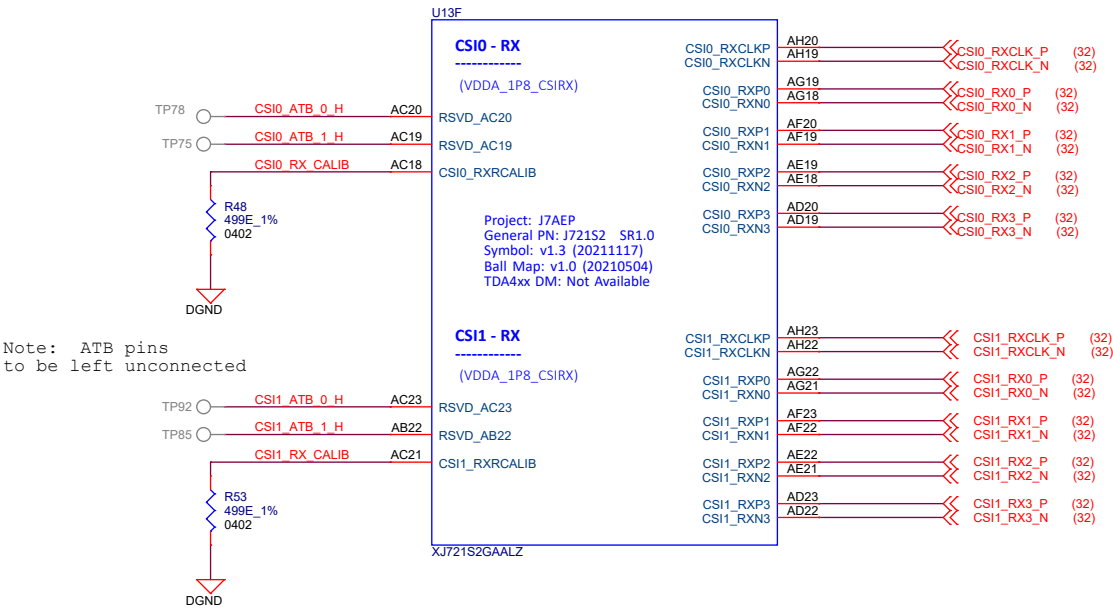
SoC GPIO MAPPING TABLE

J7x SoM - GPIO Mapping Table						
WKUP Domain						
Net name	J7AEP Mapping		Input/Output	Default	State	Remarks
	Package Signal Name	GPIO Number				
MCU_MCAN0_EN	WKUP_GPIO0_0	WKUP_GPIO0_0	Output	BOOTMODE	Active High	MCU CAN0 Enable
BOOT_EEPROM_WP	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	BOOTMODE	Active High	Boot EEPROM Write protect
MCU_CAN1_STB	WKUP_GPIO0_2	WKUP_GPIO0_2	Output	BOOTMODE	Active High	MCU CAN1 Standby
GPIO_MCU_RGMII1_RST#	WKUP_GPIO0_56	WKUP_GPIO0_56	Output	BOOTMODE	Active low	MCU_RGMII1_Reset
SYS_IRQz	WKUP_GPIO0_7	WKUP_GPIO0_7	Input	NA	Active low	Push-button Interrupt, User Defined/Wake S2R ('0>'1' - interrupt pending, '1' - normal operation)
OSPI/ONAND_MUX_SEL	WKUP_GPIO0_6	WKUP_GPIO0_6	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - OCTAL NAND)
PMIC_MCU_INT# / H_MCU_INT#	MCU_OSPI1_CSN1	WKUP_GPIO0_39	Input	PU	Active low	Interrupt from PMIC
OSPI0_INT#/ECC_FAIL	MCU_OSPI0_CSN3	WKUP_GPIO0_30	Output	PU	Active High	OSPI0_ECC_FAIL (Mux option w/ HYPERBUS_CKn), MCU_OSPI0_ECC_FAIL is DNI resistor option.
MCU_RGMII1_INT#	WKUP_GPIO0_3	WKUP_GPIO0_3	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
SYS_MCU_PWRDN	MCU_SPI0_D0	WKUP_GPIO0_55	Output	BOOTMODE	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_CAN0_STBz	MCU_SPI0_D1	WKUP_GPIO0_69	Output	BOOTMODE	Active low	MCU CAN0 Standby
LSM6DSRX_INT	WKUP_GPIO0_57	WKUP_GPIO0_57	Input	BOOTMODE	NA	Interupt from I3C Gyroscope sensor(*LSM6DSRX)
CANIO_RET_WAKE	MCU_SPI0_CS0	WKUP_GPIO0_70	Input	PU	NA	Push-button wake signal
Main Domain						
SOC_EXTINTN	EXTINTN	GPIO0_0	Input	PU	Active low	Push-button Interrupt, User Defined
MAIN_CANIO_RET_WAKE	GPIO0_11	GPIO0_11	Input	PU	NA	Push-button wake signal
C_MCASP10_ACLKR	MCASP0_AXR2	GPIO0_18	Input	PU	Active low	CSI2 IO expander Interrupt.('0' - interrupt pending, '1' - no interrupt) (IOEXP5_INT#)
TRC_DATA11	MCAN0_TX	GPIO0_25	NA	PU	Active low	I2C0 IO expander interrupt. ('0' - interrupt pending, '1' - no interrupt)(I2C0_IOEXP_INT#) Note: GPIO only available from Trace/GPMC Mux
SEL_SDIO_3V3_1V8n	MCAN15_RX	GPIO0_8	Output	PU	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
USBC_DIR	Used for High Speed Mux control		Input	PU	NA	USB Type C Cable Orientation. Type-C plug position 2 (H); Type-C plug position 1 (L)
CSI2_EXP_A_GPIO2	MCAN0_TX	GPIO0_26	I/O	NA	NA	CSI2 Expansion Board Specific. MV - Used for CSI0_XTRIG; LI - Used for CSI0_GPIO0
GPIO_RGMII1_INT#	HYP0_RXPMCLK_MUX	GPIO0_23	Output	PU	Active low	RGMII1_Reset
CSI2_EXP_A_GPIO4	MCAN1_RX	GPIO0_28	I/O	NA	NA	CSI2 Expansion Board Specific. MV - Used for CSI1_XTRIG; LI - Used for CSI1_GPIO0
PM_I2C_SEL	SPI0_CS0	GPIO0_51	Output	PD	NA	CP Board - PM I2C Mux seletion. ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA) GESI - Boosterpack_GPIO1
GPIO Expander						
I2C Instance	Port	Net Name	Input/Output	Default	State	Usage
I2C0 ADDR: 0x21	P00	USB2.0_MUX_SEL	Output	PD	Active High	Signal Mux Control ('0' - USB_C, '1' - USB_Hub)
	P01	CANUART_MUX1_SELO	Output	PU	Active High	Select line for CANUART_MUX1
	P02	CANUART_MUX2_SELO	Output	NA	Active High	Select line for CANUART_MUX2
	P03	CANUART_MUX_SEL1	Output	PU	Active High	Select line shared for both thr CANUART_MUX
	P04	GPIO_RGMII1_RST	Output	PU	Active High	Routed to INFO/GESI expansion connector. GESI - Used for GPIO_PRG0_RGMII_RST; INFO - Not used
	P05	GPIO_eDP_ENABLE	Output	NA	Active High	Used for Enable of DSI to eDP Bridge
	P06	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
	P07	CAN_STB/MCAN2_STB	Output	PU	Active High	Standby signals for CAN Transceivers

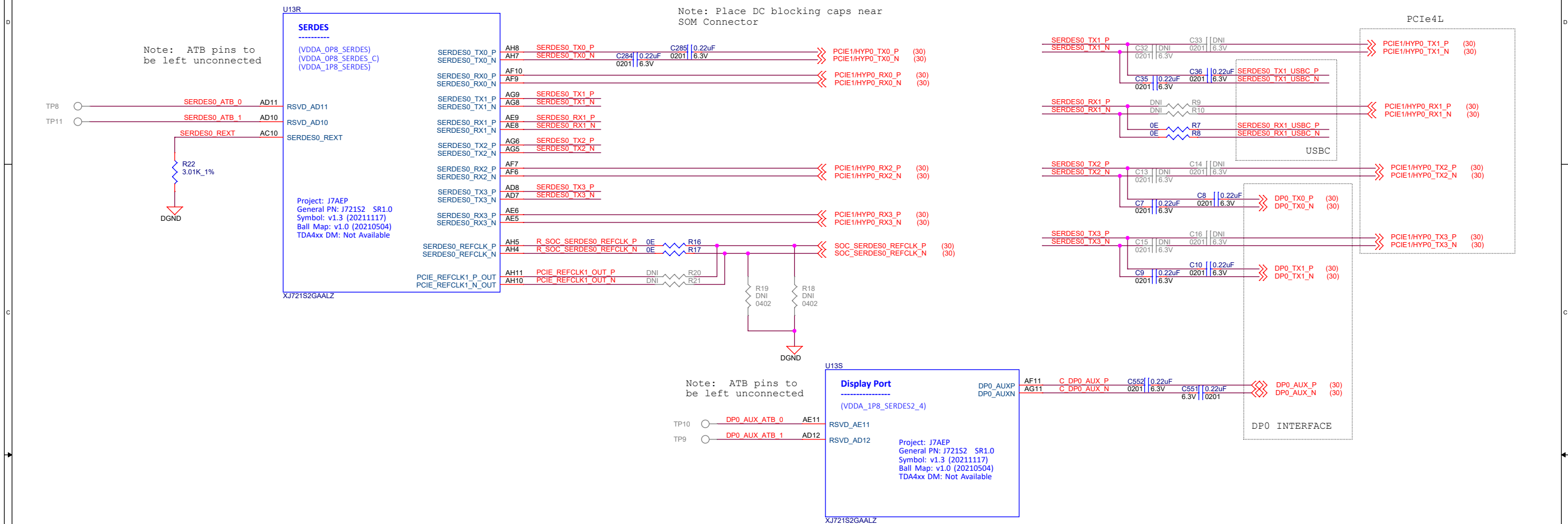
DSI



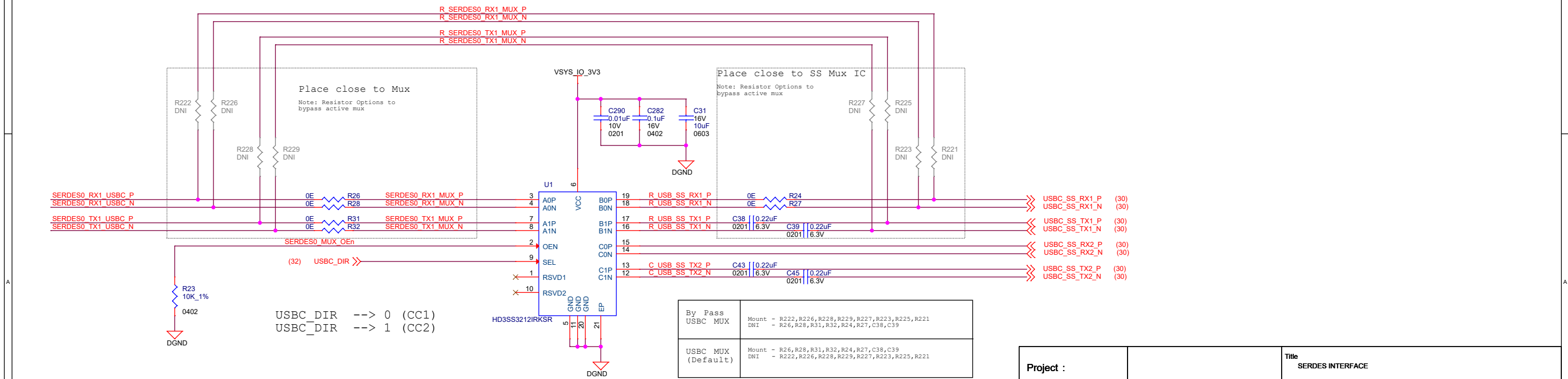
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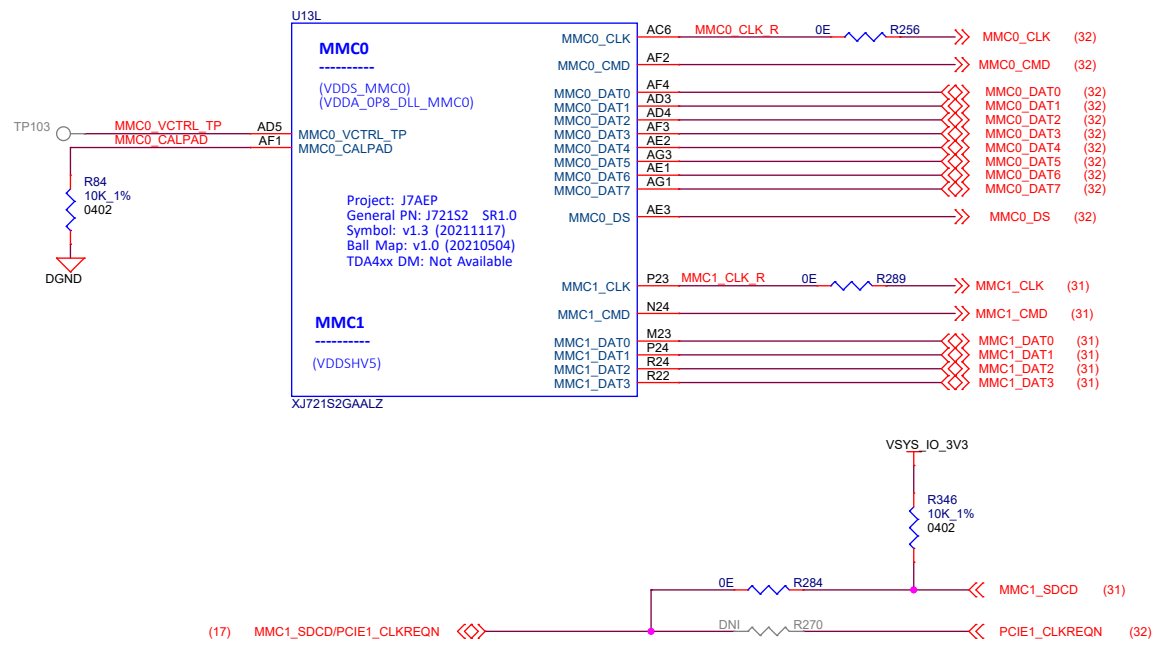
SERDES



USB Type C MUX



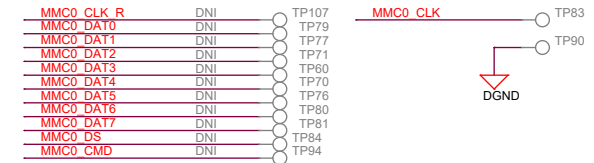
MMC Interface



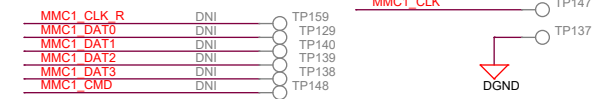
Via Probe Test Points

Place Near SOC

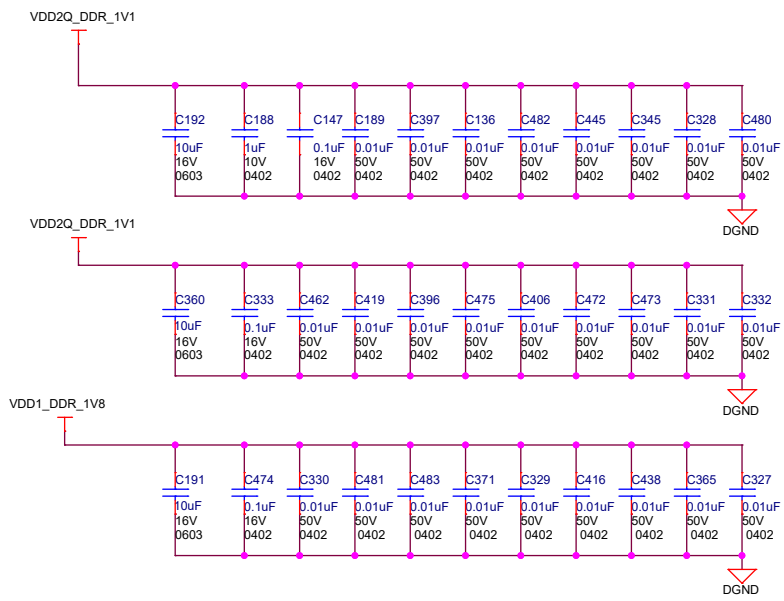
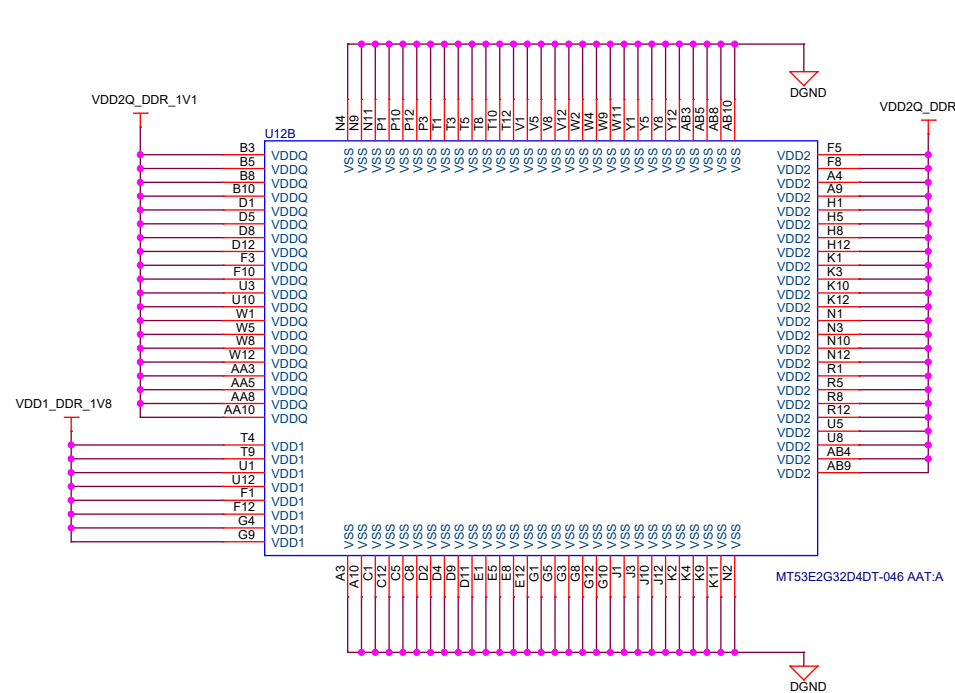
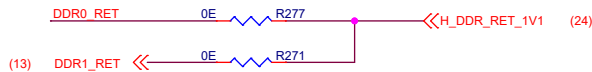
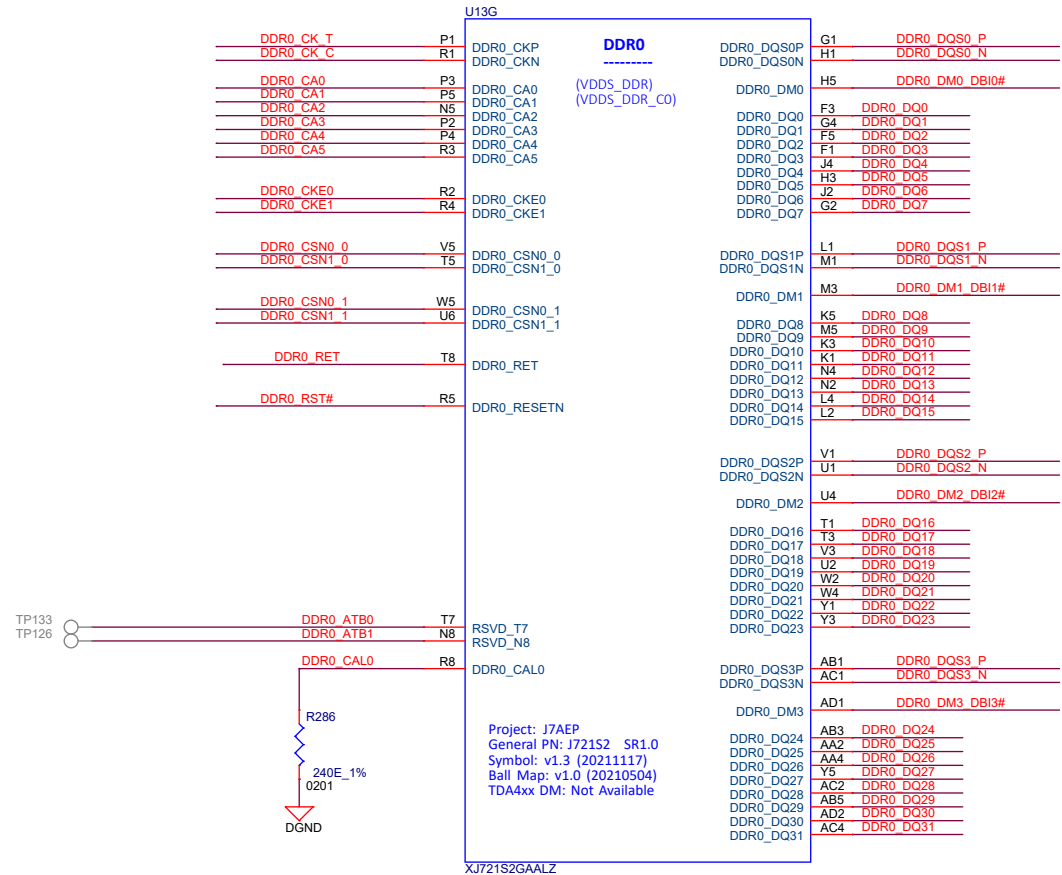
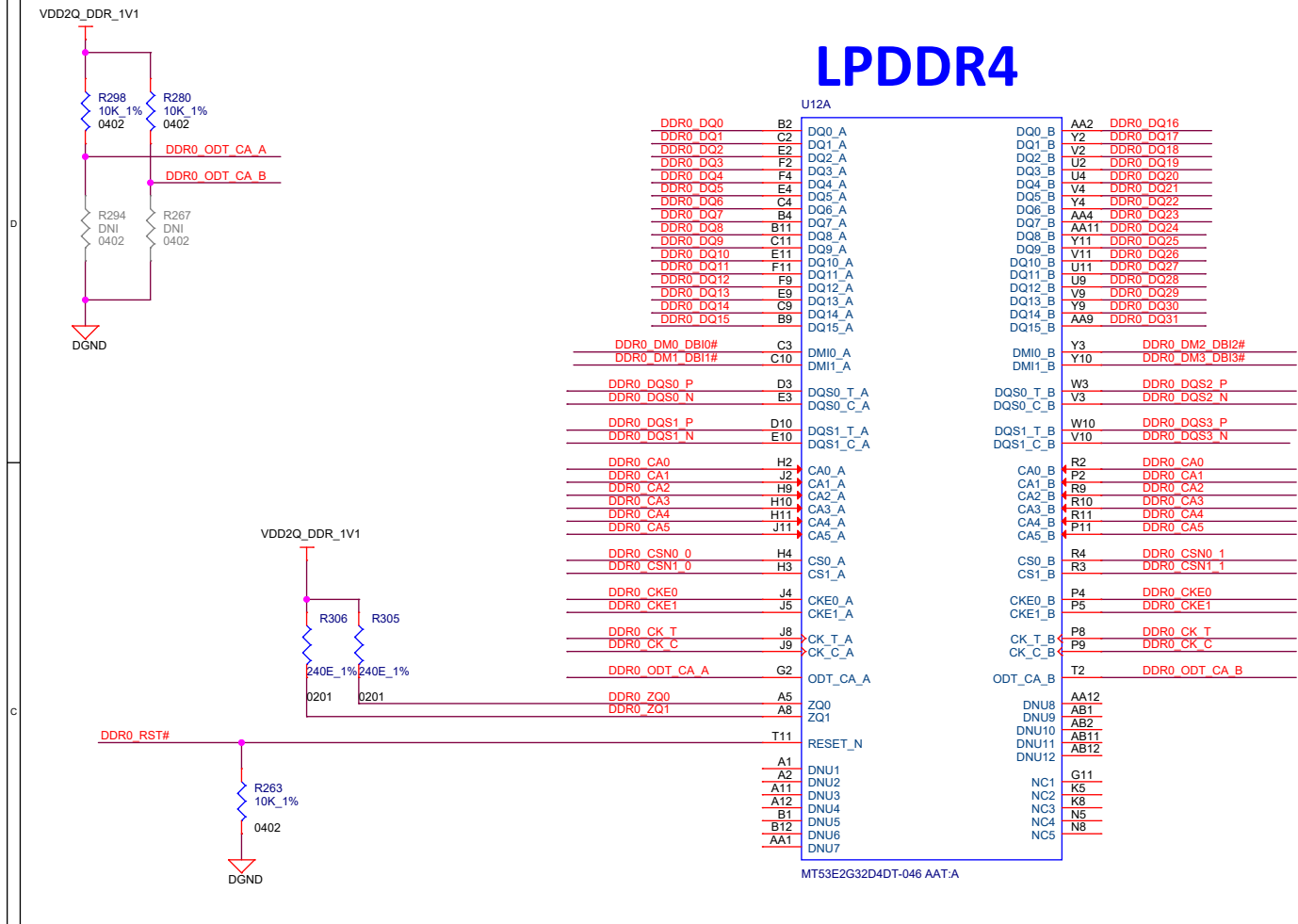
MMC0 :

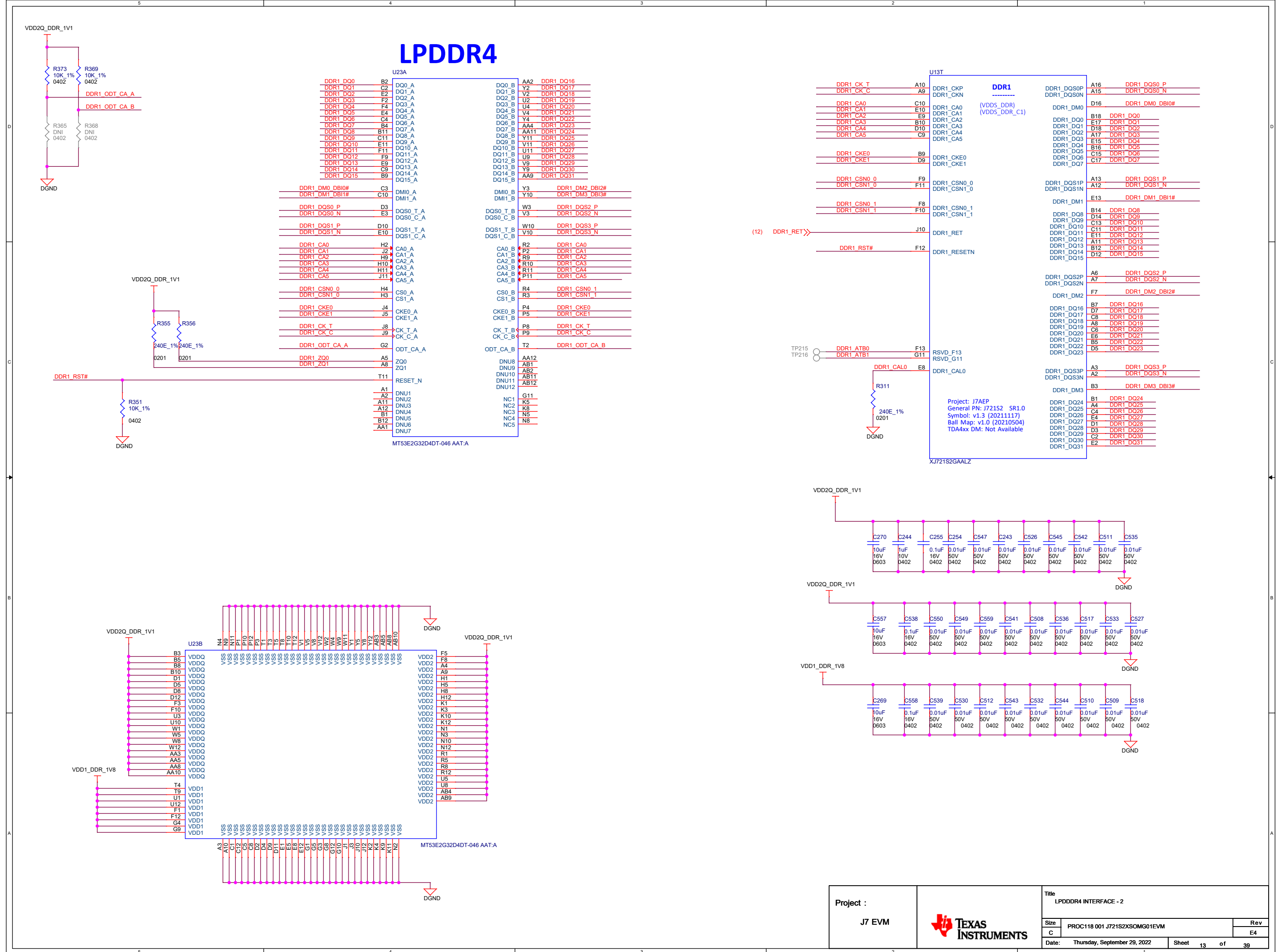


MMC1 :



LPDDR4

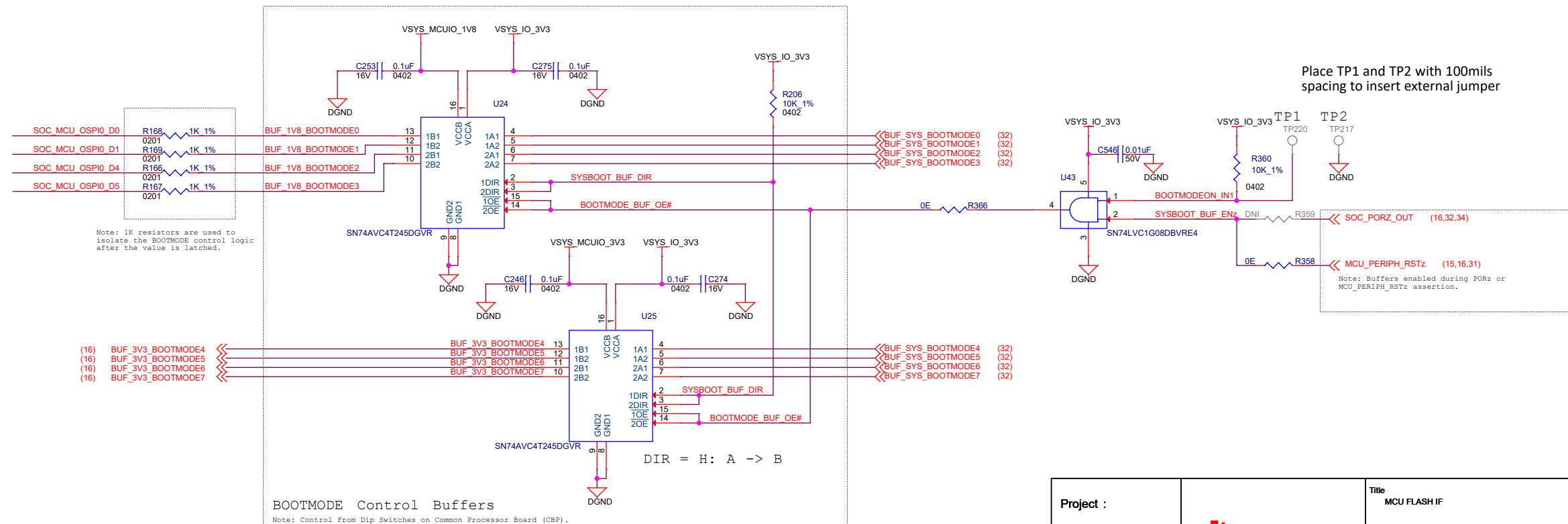
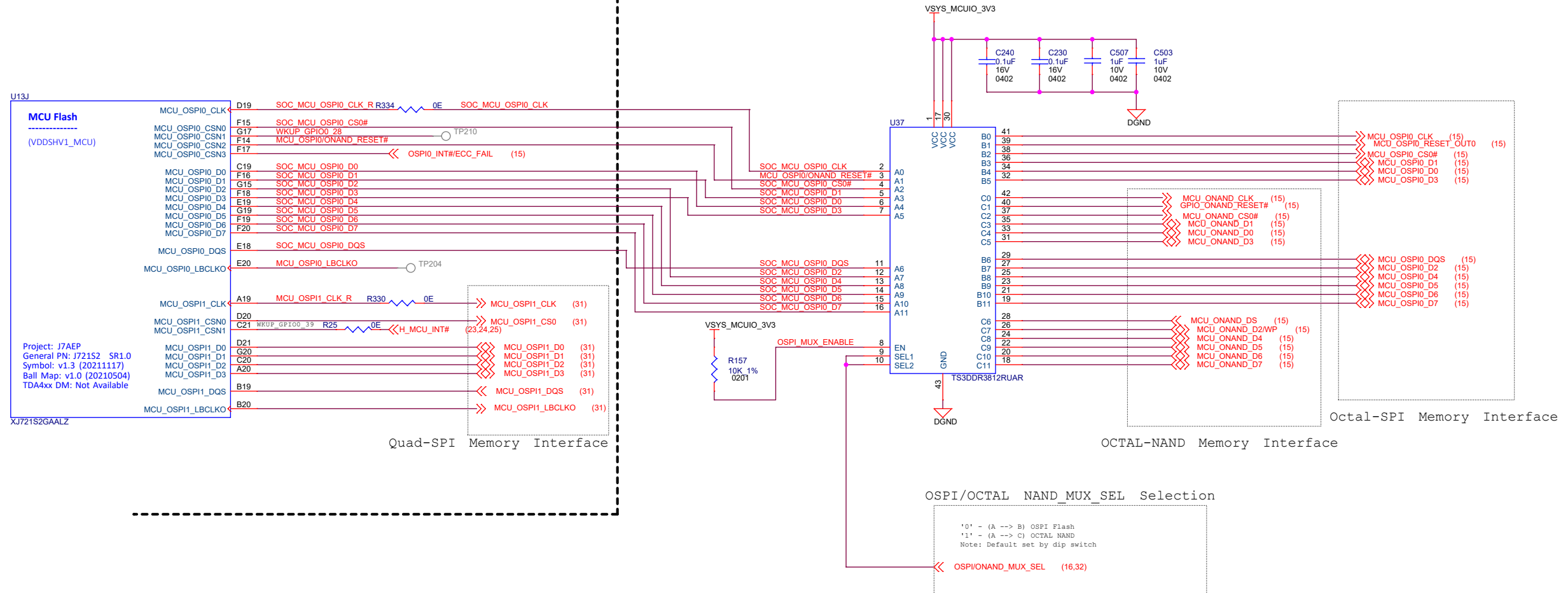




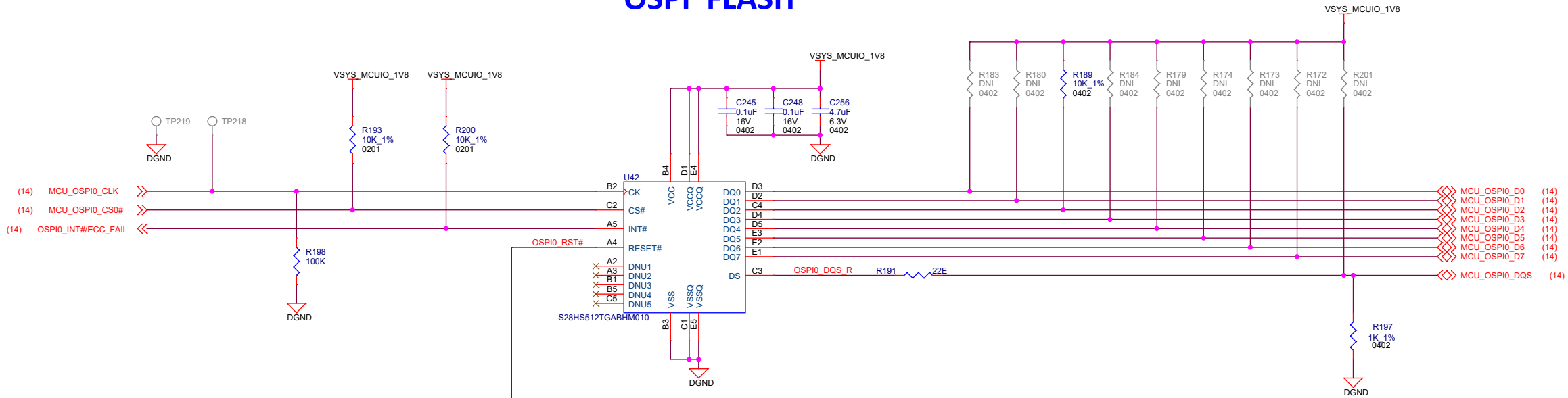
EVM development & evaluation test circuitry (TI EVM Only)

MCU FLASH

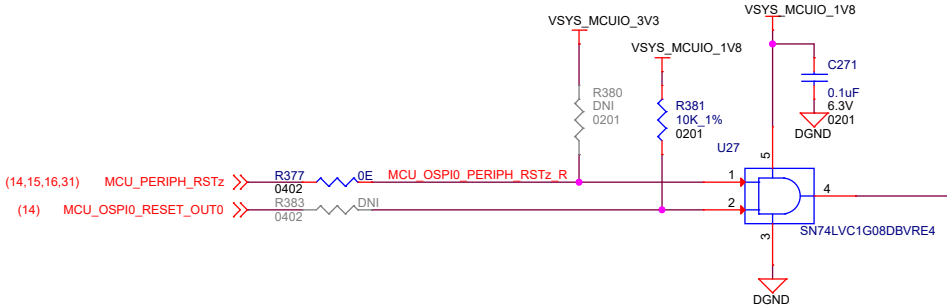
2:1 Mux for OSPI/OCTAL NAND



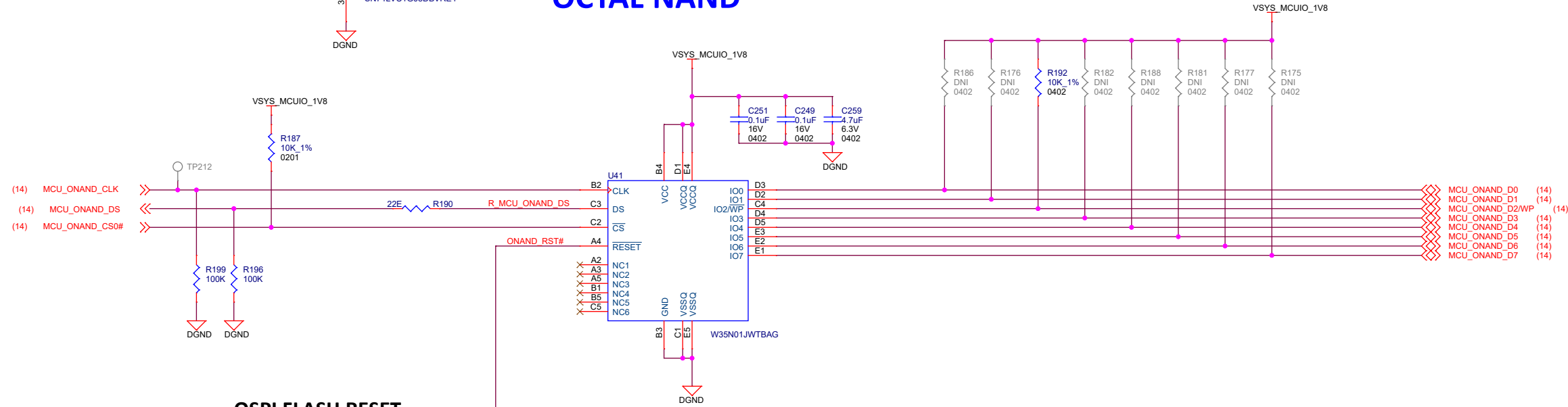
OSPI FLASH



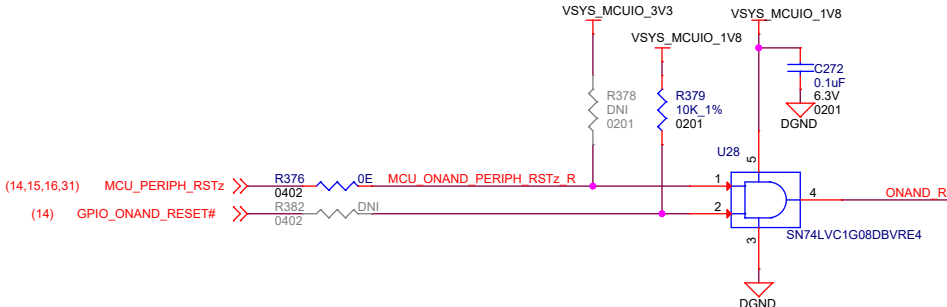
OSPI FLASH RESET



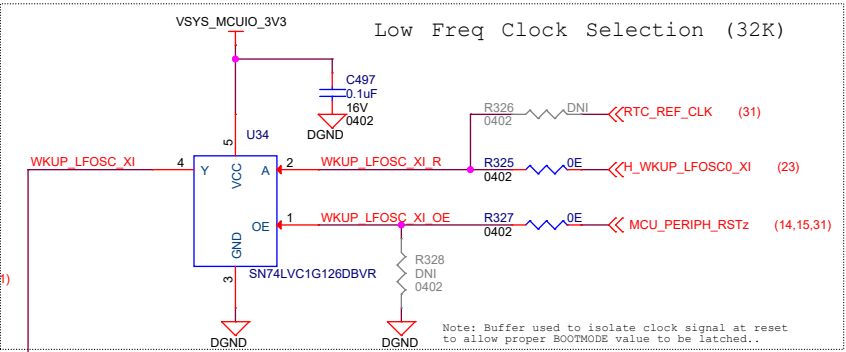
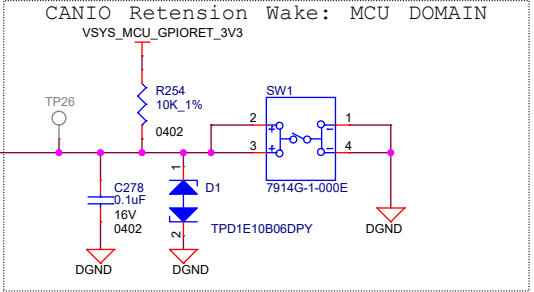
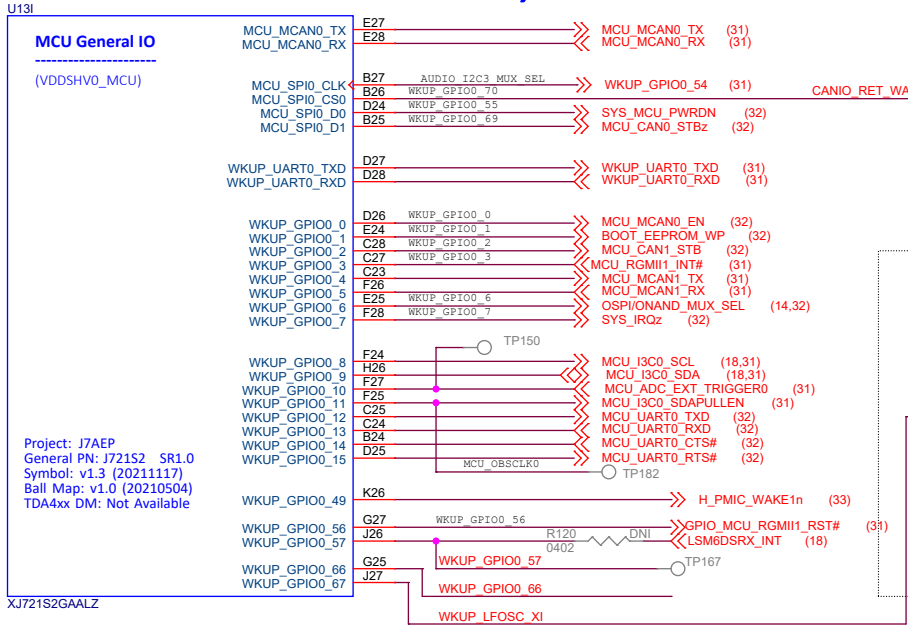
OCTAL NAND



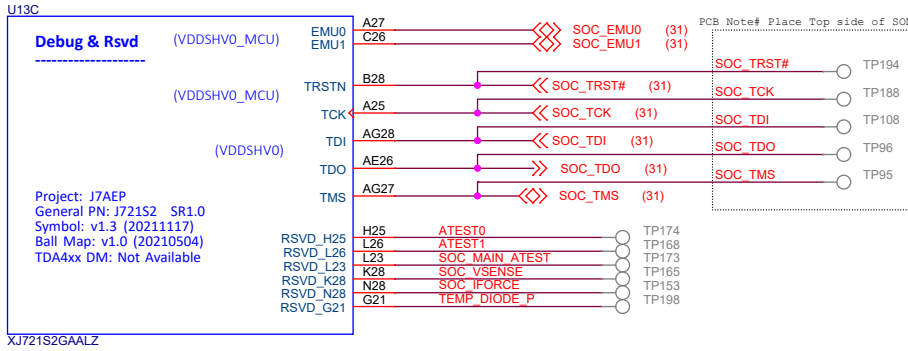
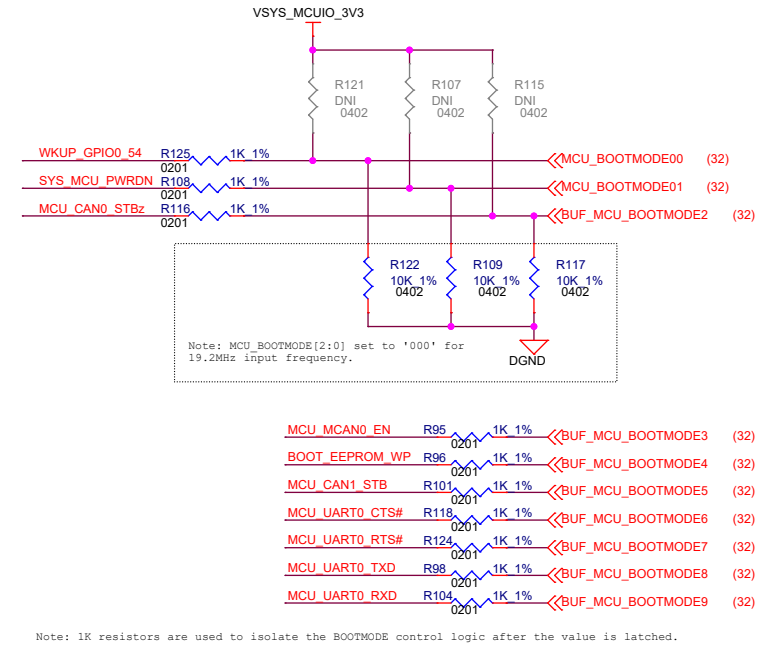
OSPI FLASH RESET



MCU & MAIN GENERAL IO, OSC CLKS

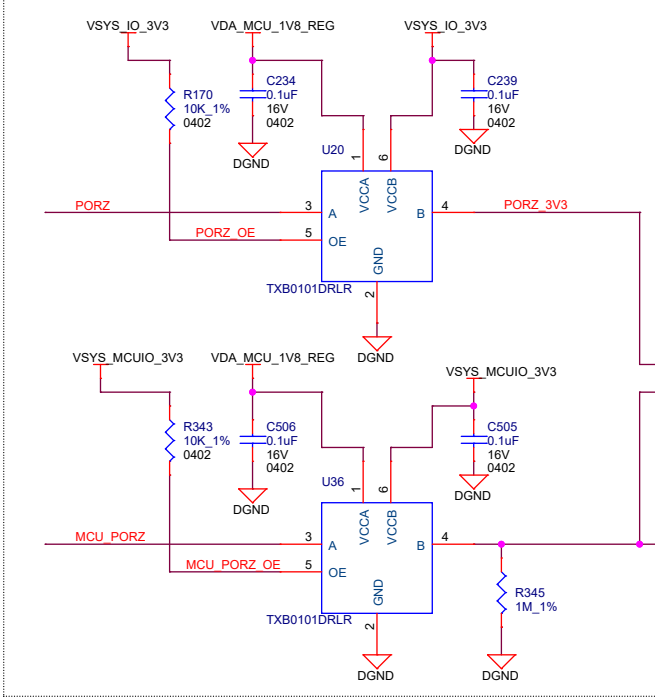


MCU BOOTMODE Control Signals

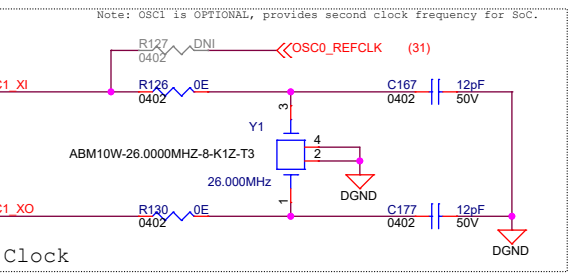
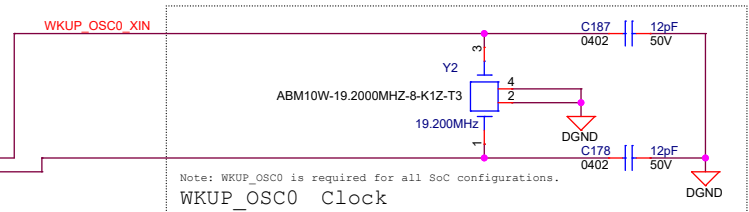
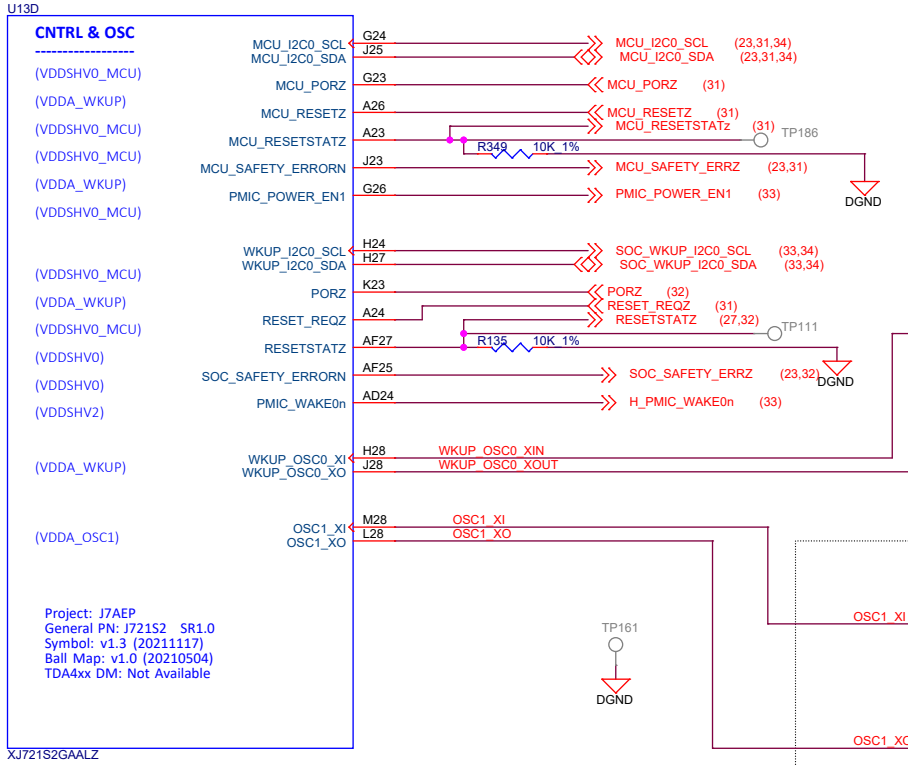
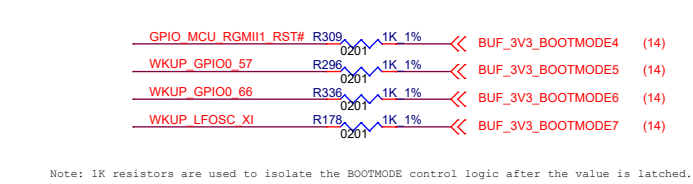


Power-On Reset Buffers

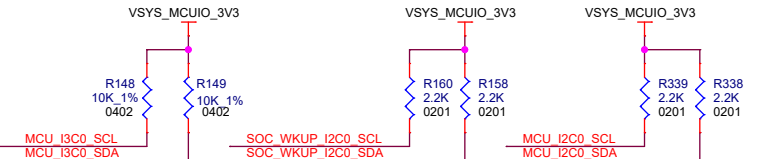
Note: Used to align logic/levels with Common Processor Board (CPB).



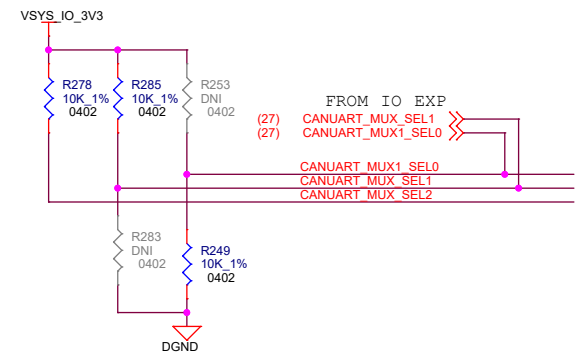
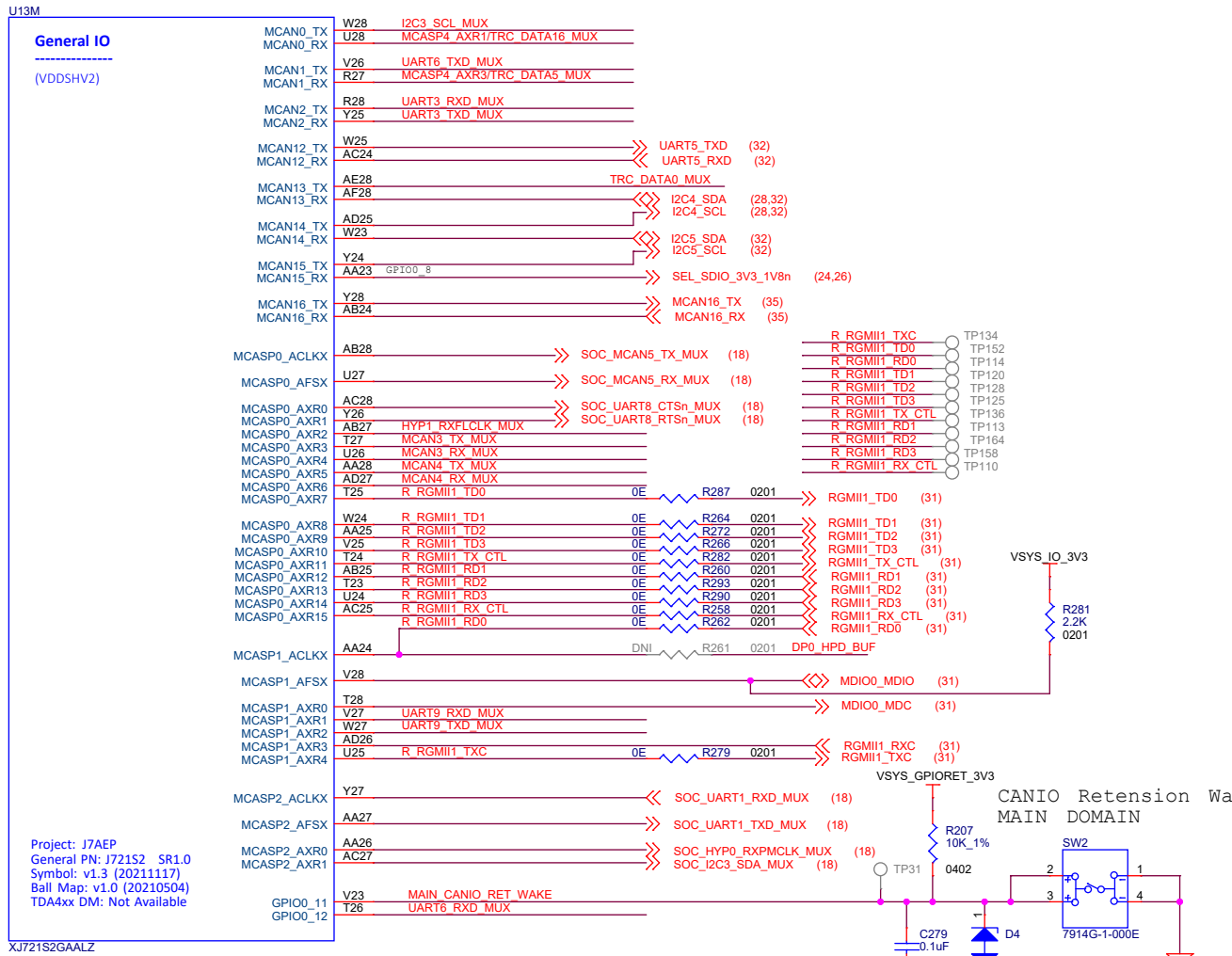
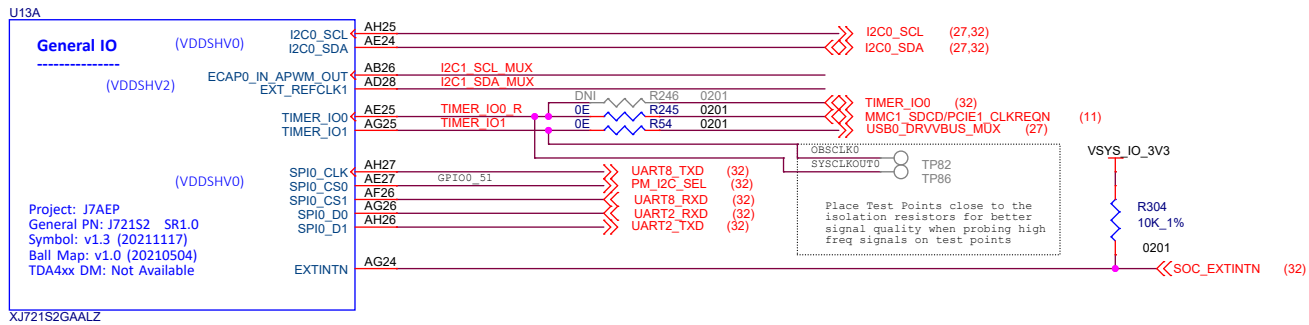
BOOTMODE Control Signals (partial)



MCU I3C/I2C Pull-ups



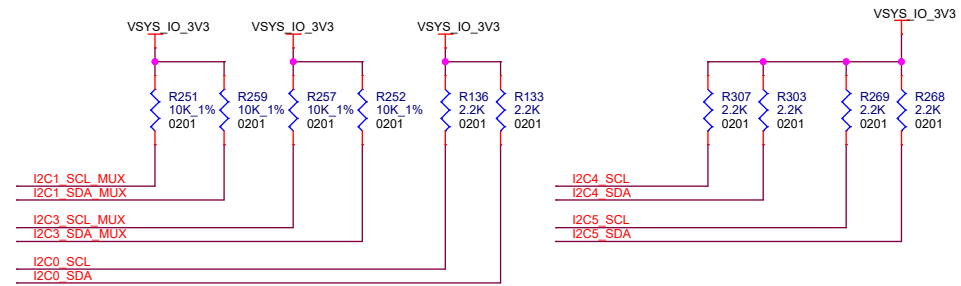
GENERAL IO



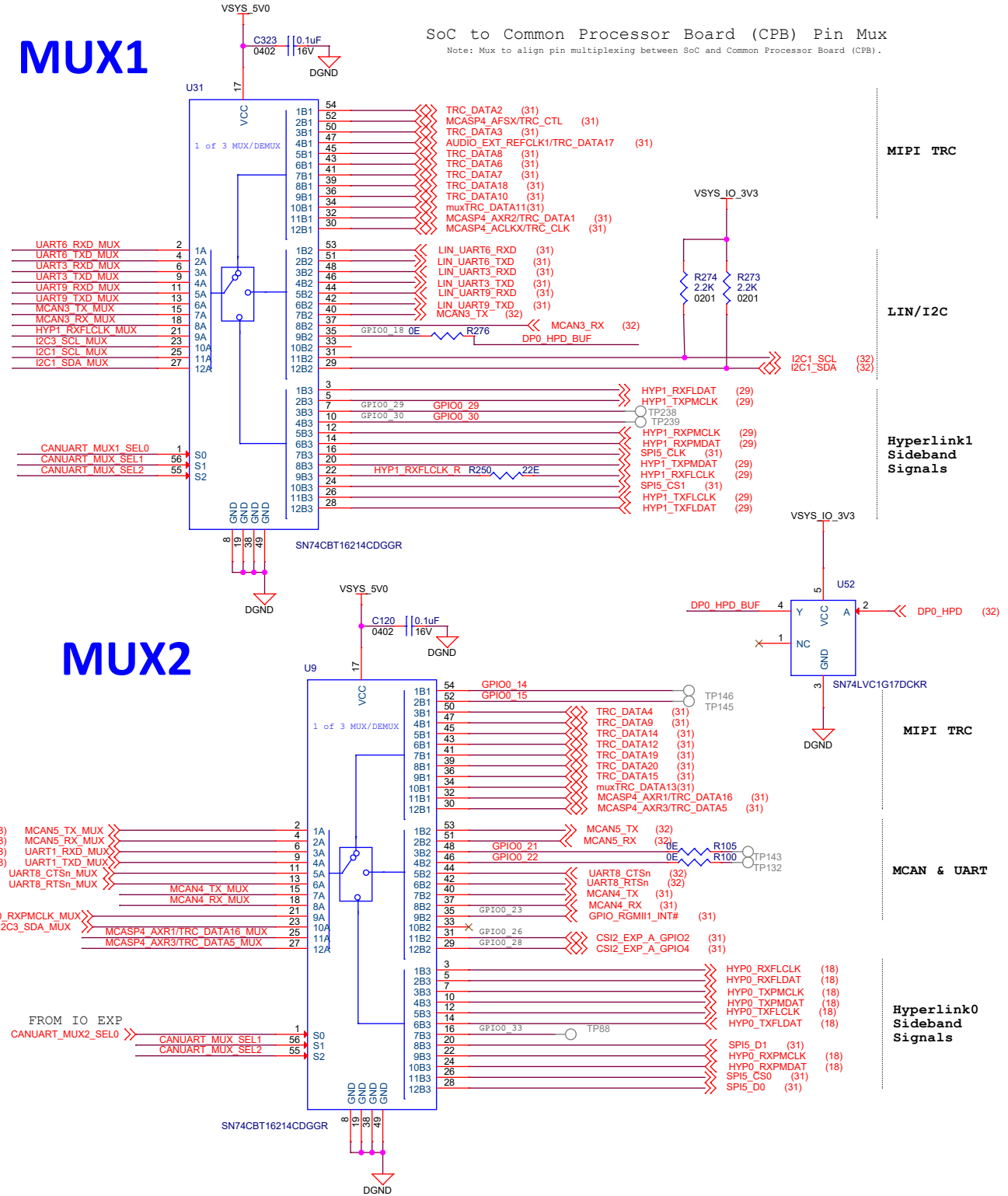
HYPERLINK/TRACE/MCAN/LIN - 1:3 MUX : Truth Table

MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port

(default)



MUX1



Project :

J7 EVM



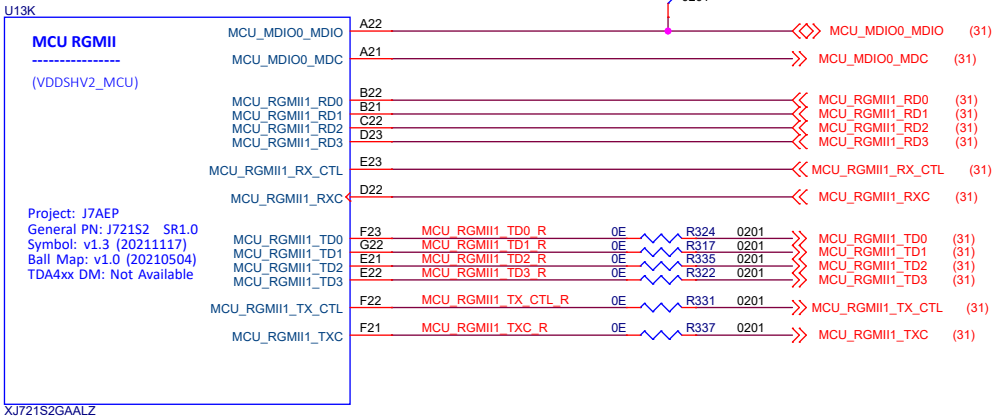
Title	SOC_GENERAL&MCU_GENERAL
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Size	PROC118 001 J721S2XSOMG01EVM
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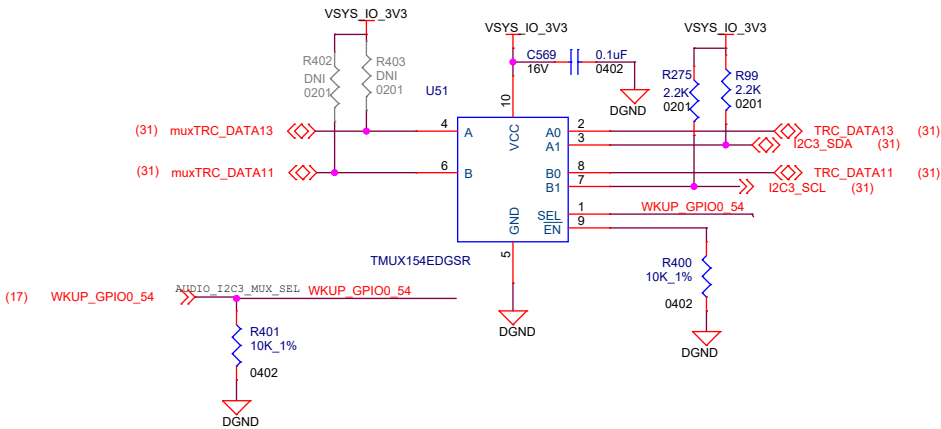
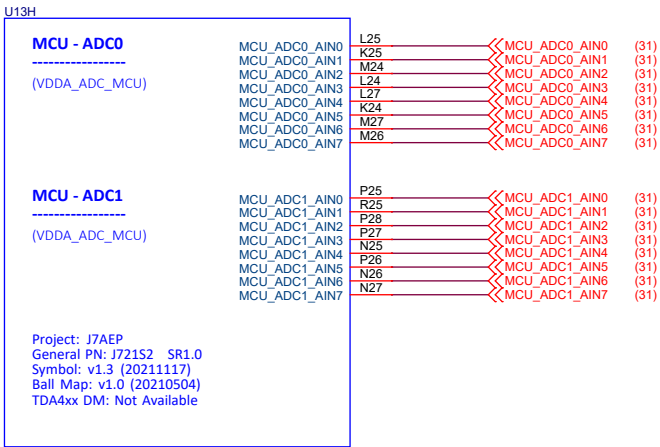
Date: Tuesday, September 06, 2022

Re

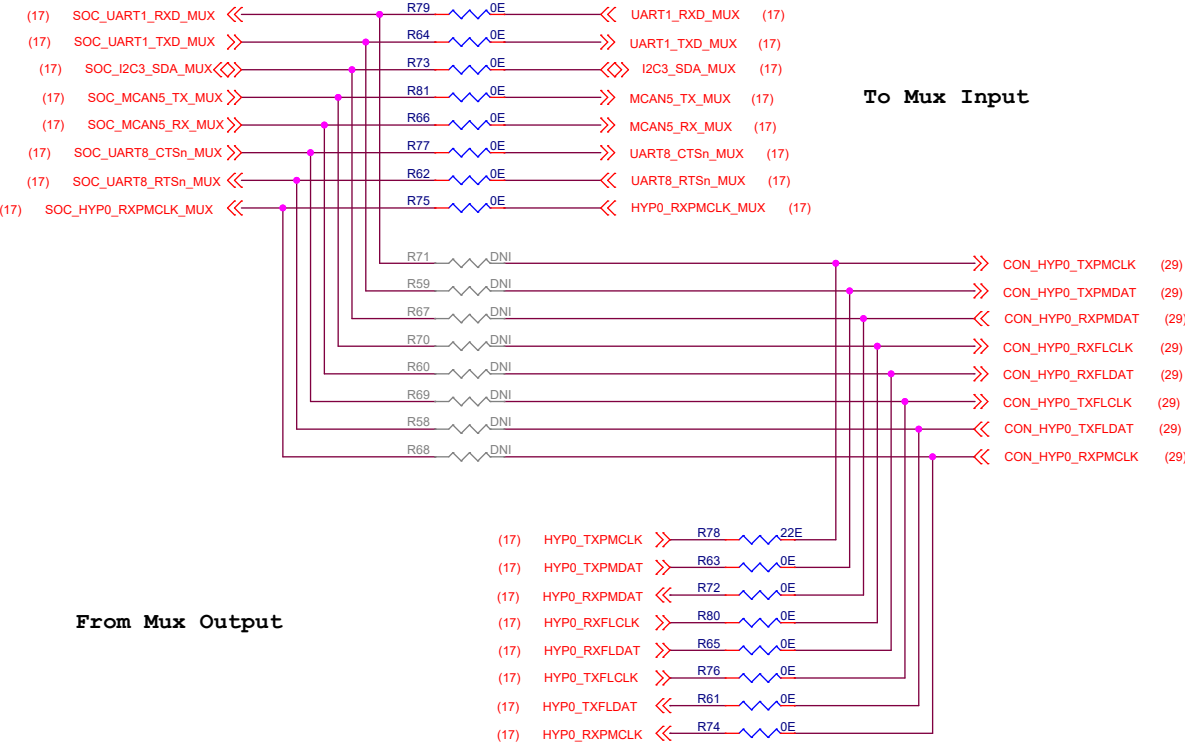
MCU_RGMII



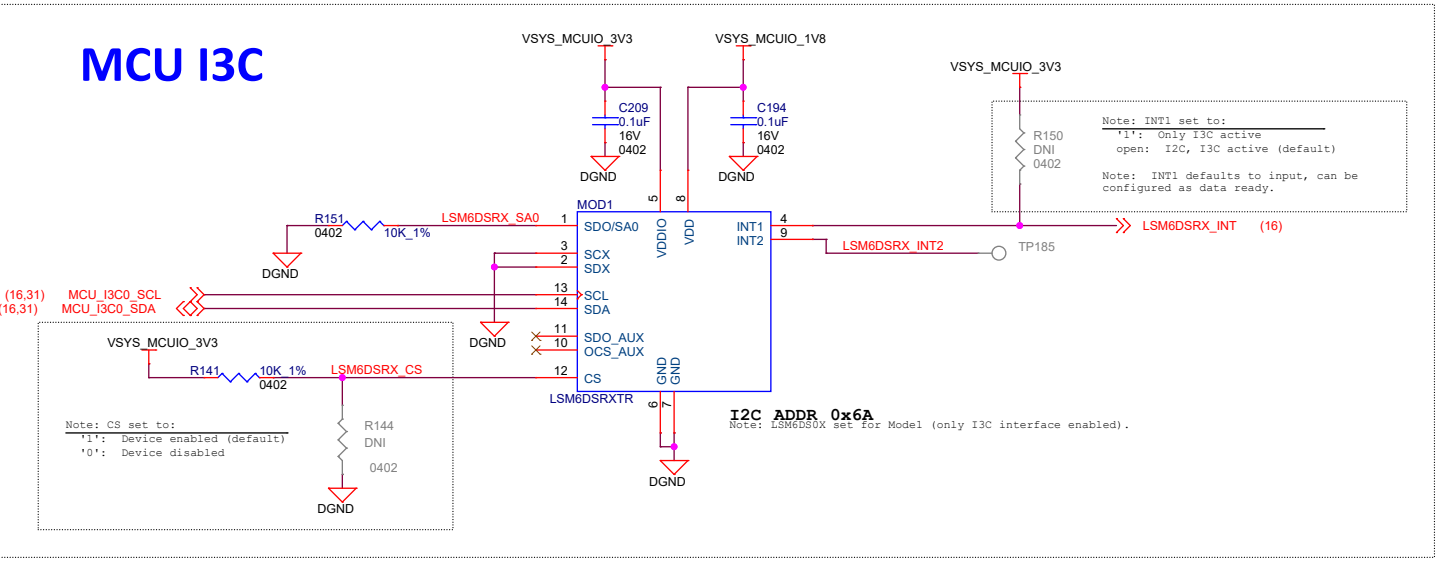
MCU ADCs



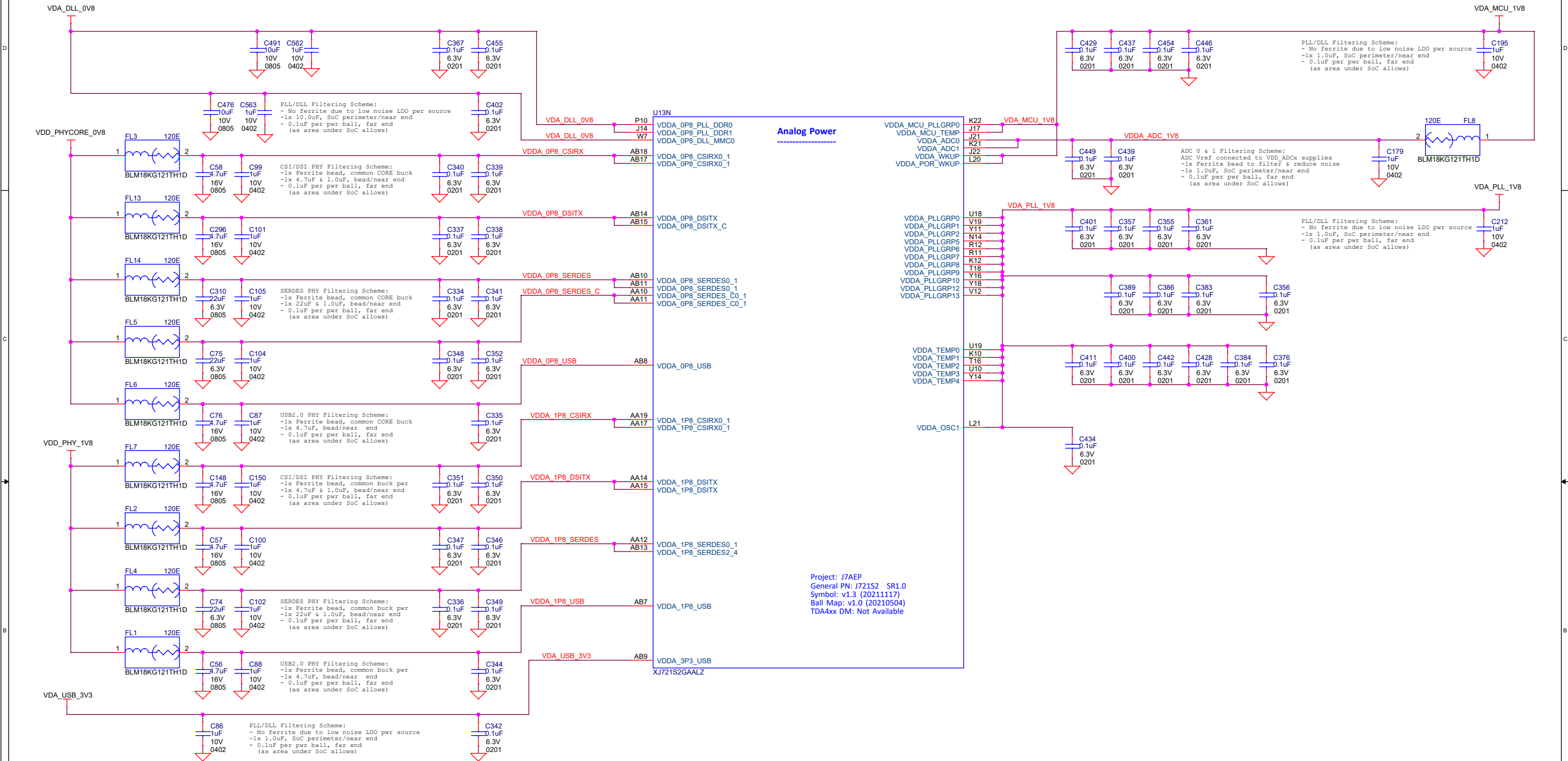
OE#	SEL	FUNCTION
LOW	LOW	AB port = A0B0 port (default)
LOW	HIGH	AB port = A1B1 port
HIGH	Z	DISCONNECT



To Hyperlink Side band Conn



ANALOG POWER 1



Project :

J7 EVM



Title
SOC ANALOG POWER 1

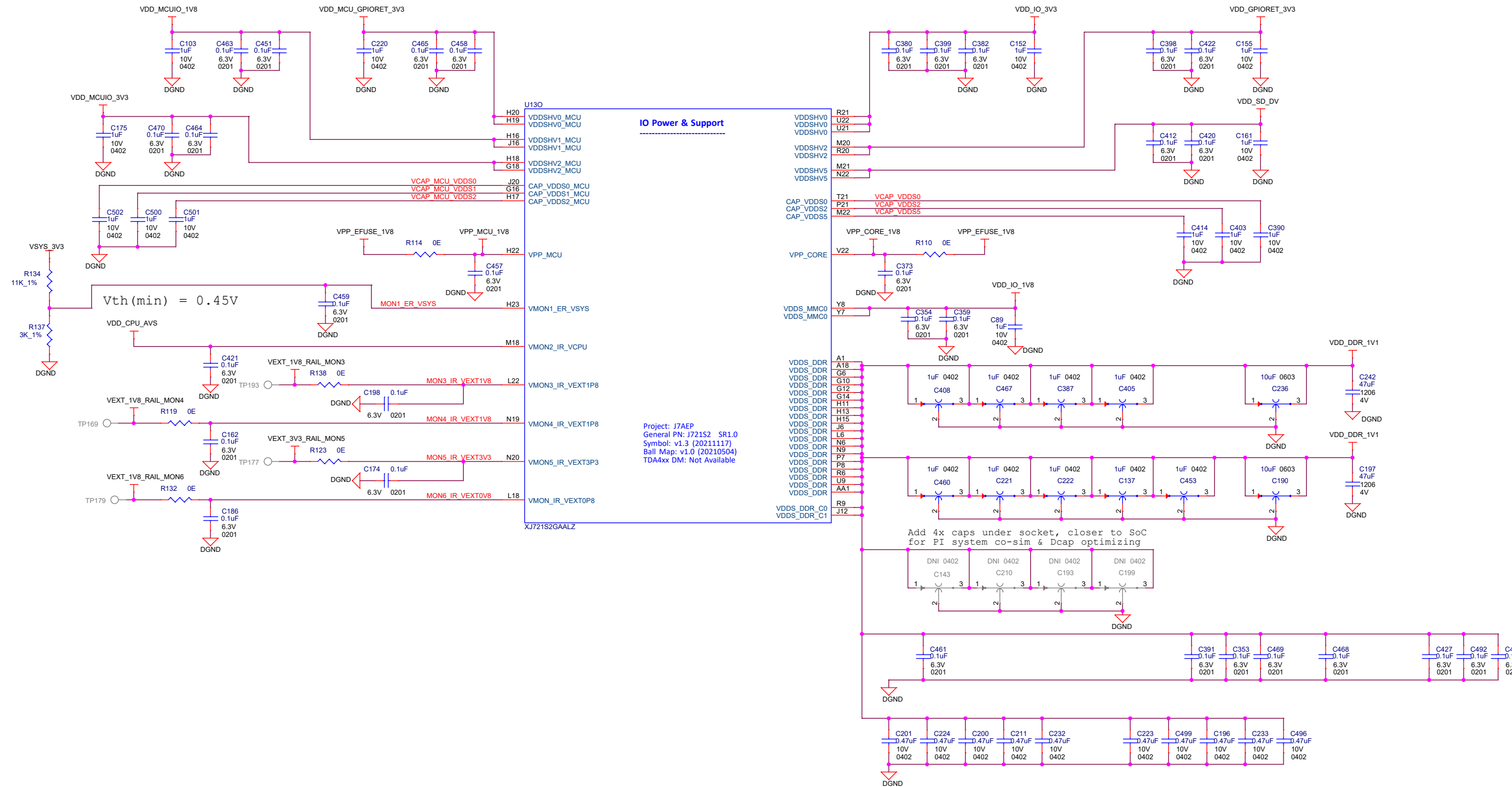
Size
C PROC118 001 J721S2XSOMG01EVM

Date: Tuesday, September 06, 2022

Sheet 19 of 39

Rev
E4

Voltage Monitors & IO POWER 2



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project :

J7 EVM



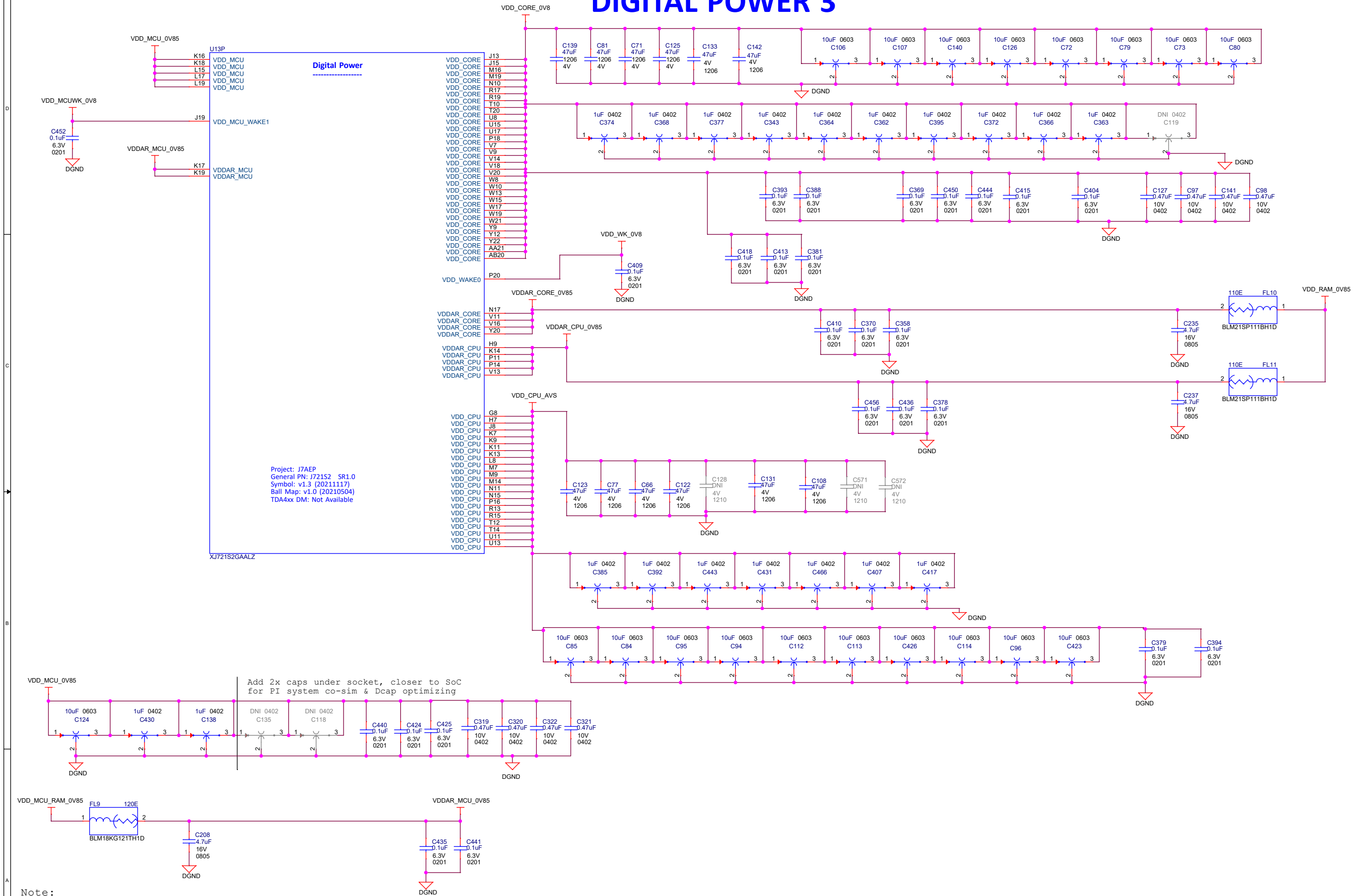
Title	SOC DIGITAL IO & SUPPORT POWER 2
-------	----------------------------------

Size	PROC118.001 I721S2YSOMG01EVM
------	------------------------------

C				E4
Date:	Thursday, September 29, 2022	Sheet	20	of 39

Rev

DIGITAL POWER 3



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project :

J7 EVM



Title	SOC DIGITAL POWER 3
-------	---------------------

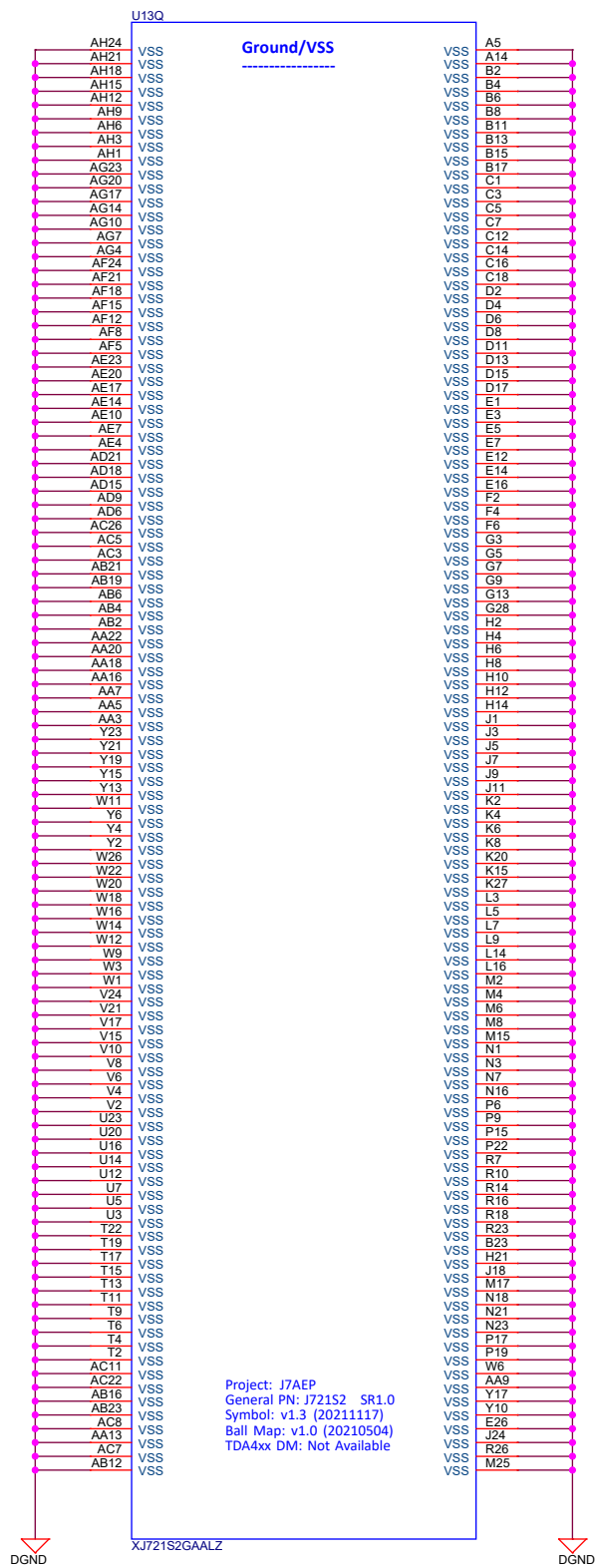
Size	PROC118.001.J721S2XSOMG01EVM
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C	
Date:	Tuesday, March 28, 2023

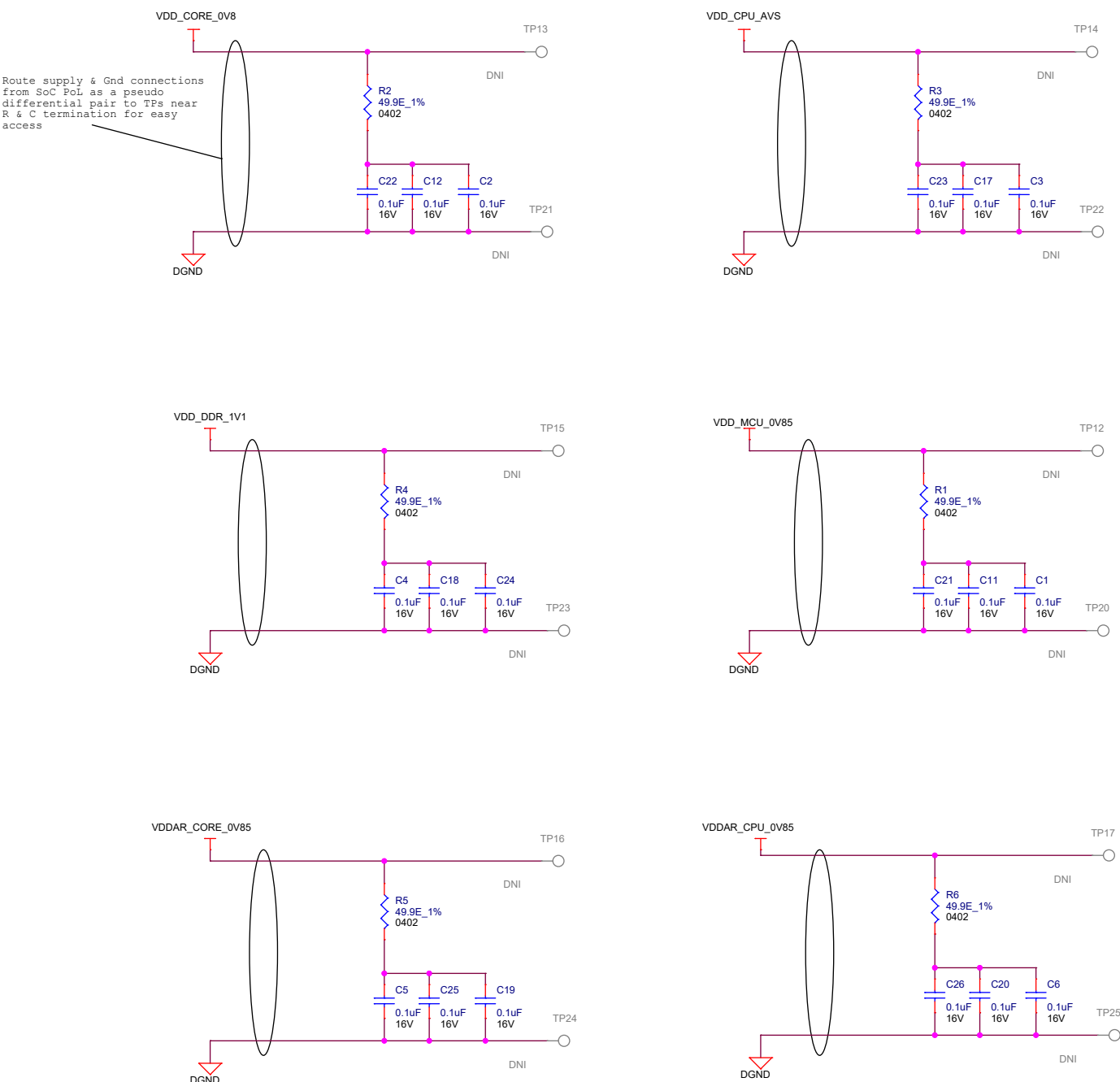
Rev

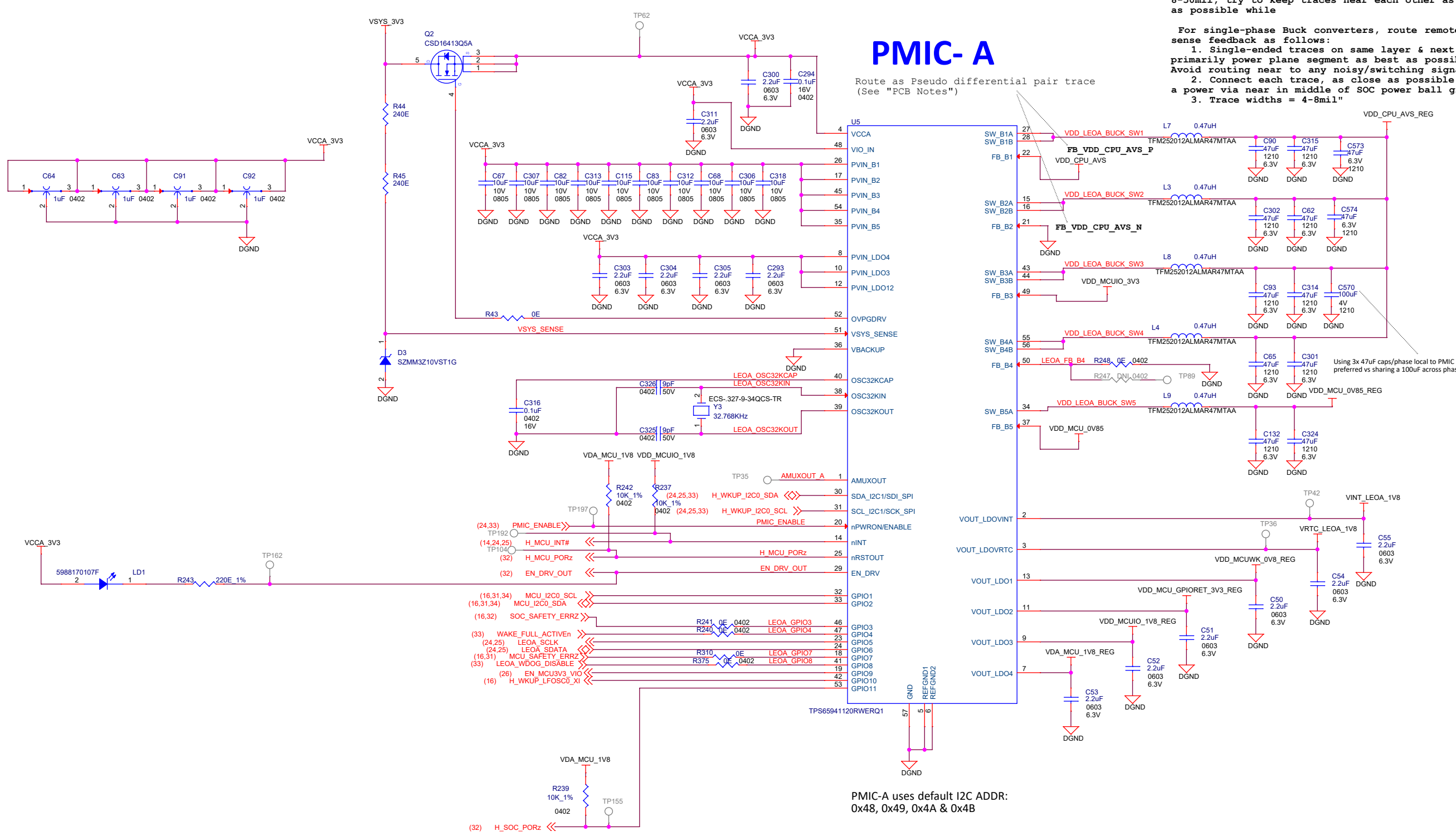
	E4
	39

SOC GROUND



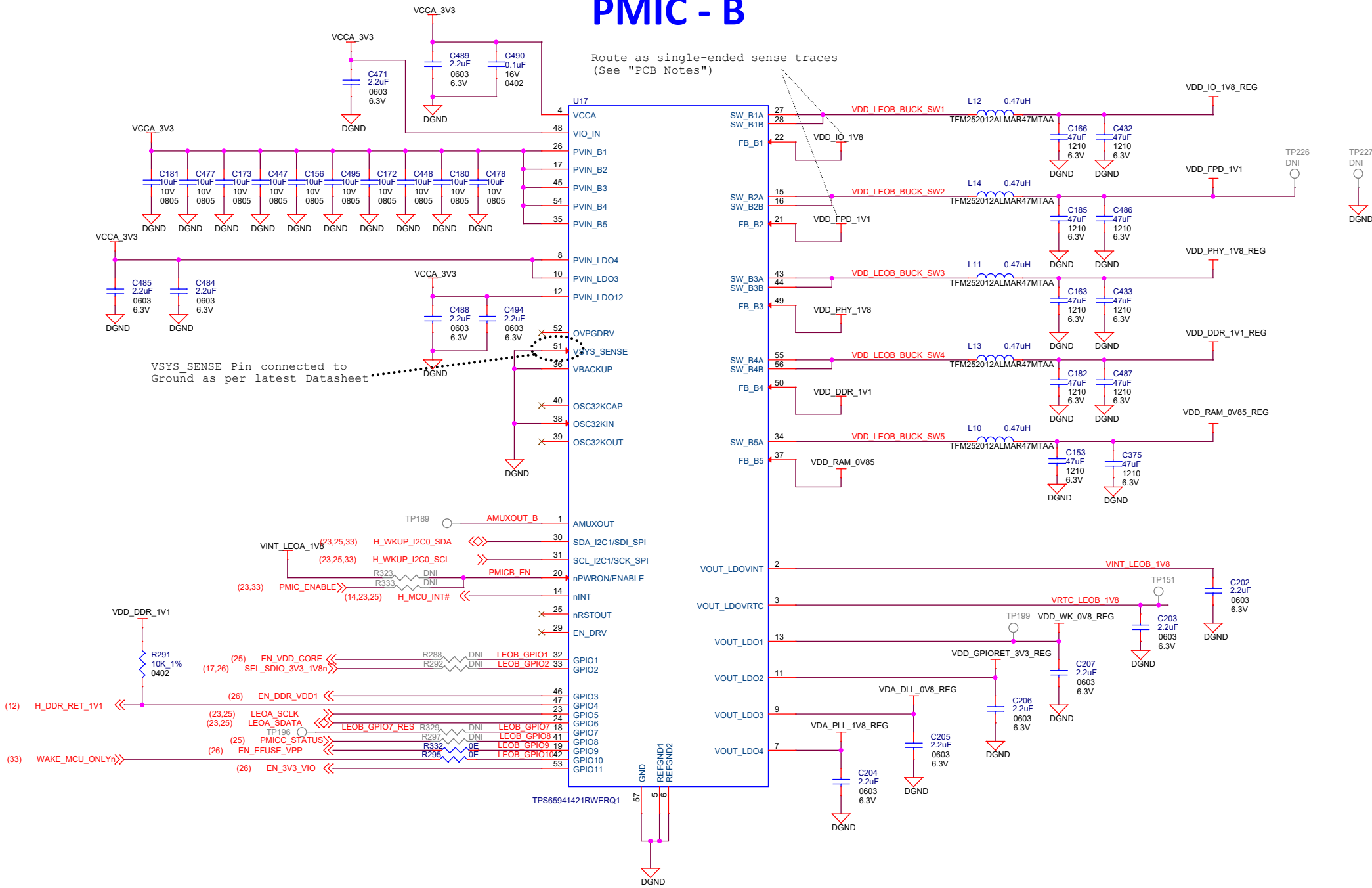
SoC Supply Noise Kelvin Sensing





PMIC - B

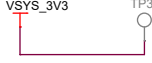
Route as single-ended sense traces
(See "PCB Notes")



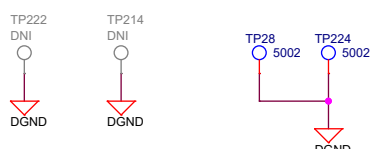
Not used on EVM.
Provisioned to show end product
use of FPD-Link components

PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

Power Test Point

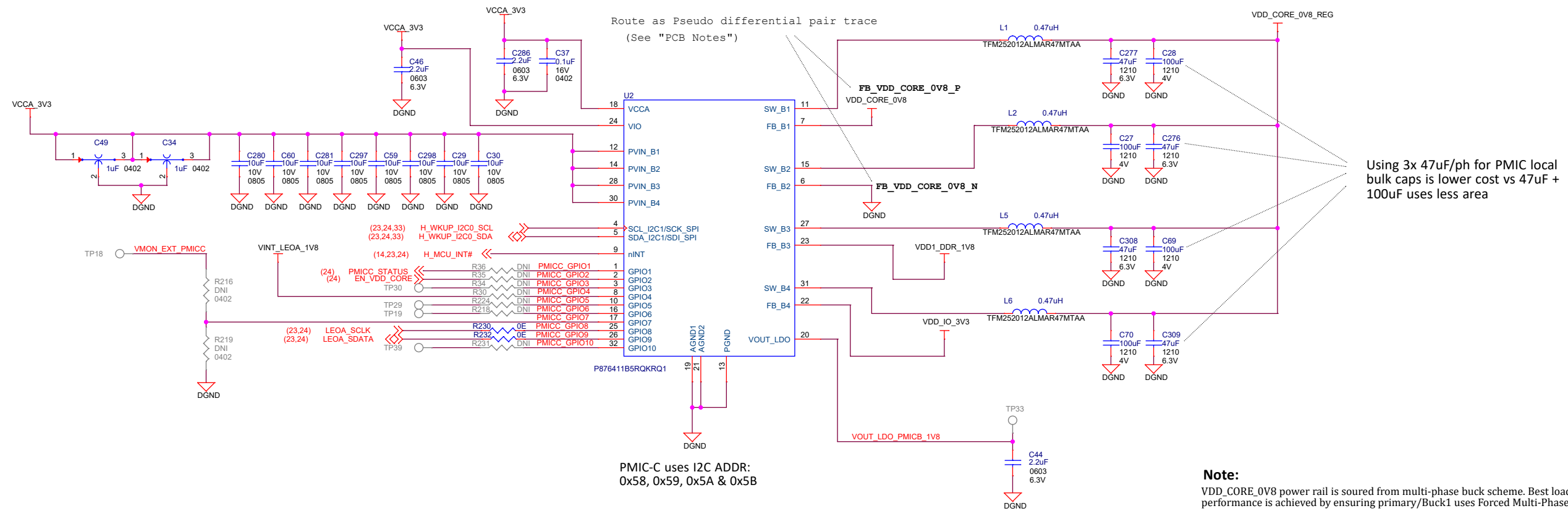


Ground Test Points



Project : J7 EVM		Title POWER SUPPLY 2	
Size C		PROC118 001 J721S2XSOMG01EVM	Rev E4
Date: Thursday, March 30, 2023		Sheet 24 of 39	

High-Current Power Stage (HCPS)



Using 3x 47uF/ph for PMIC local bulk caps is lower cost vs 47uF + 100uF uses less area

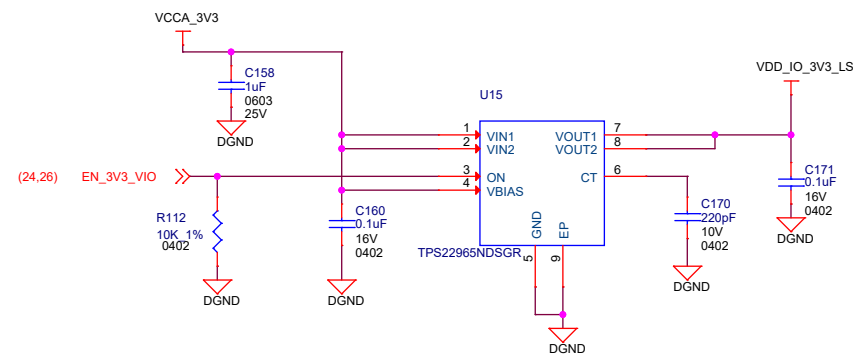
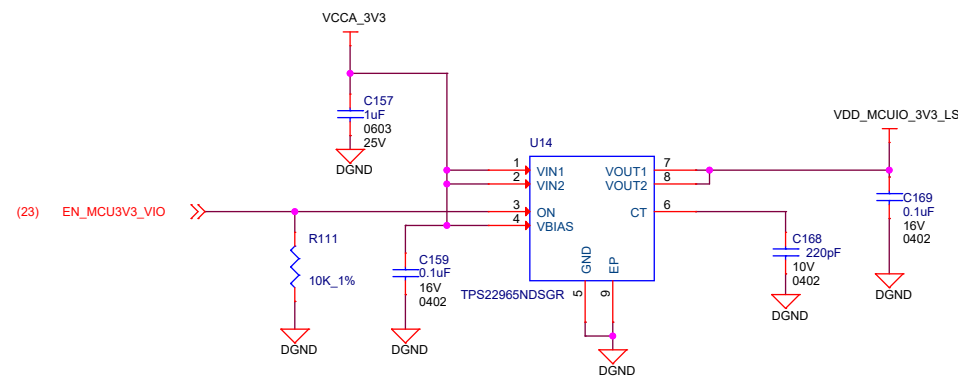
Note:

VDD_CORE_0V8 power rail is sourced from multi-phase buck scheme. Best load step performance is achieved by ensuring primary/Buck1 uses Forced Multi-Phase (FMP) mode.

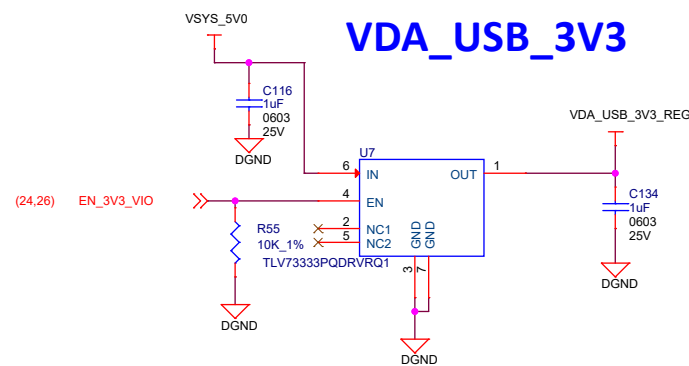
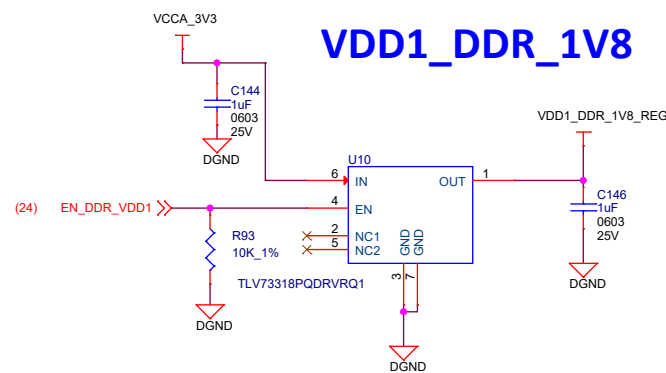
Select FMP mode as follows:

A. VDD_CORE_OV8 supplied from Hera PMIC-C, 4-Ph Bucks 1-4
PMIC Addr: 0x58; BUCK1_CTRL Reg Addr: 0x04; Write Data: 0x37 (FMP)

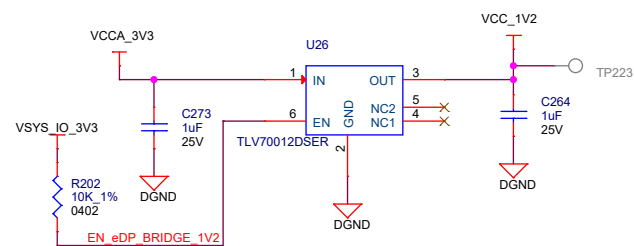
LOAD SWITCHES



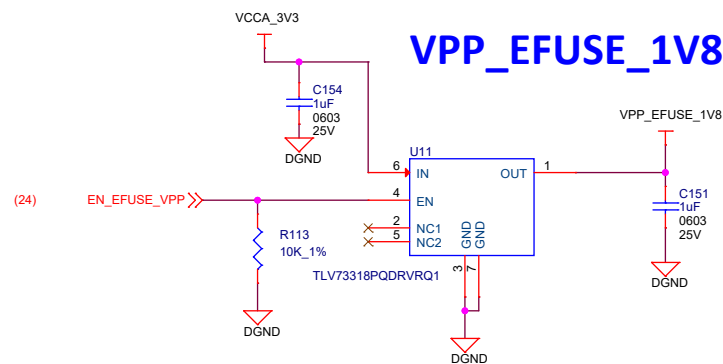
LDOs



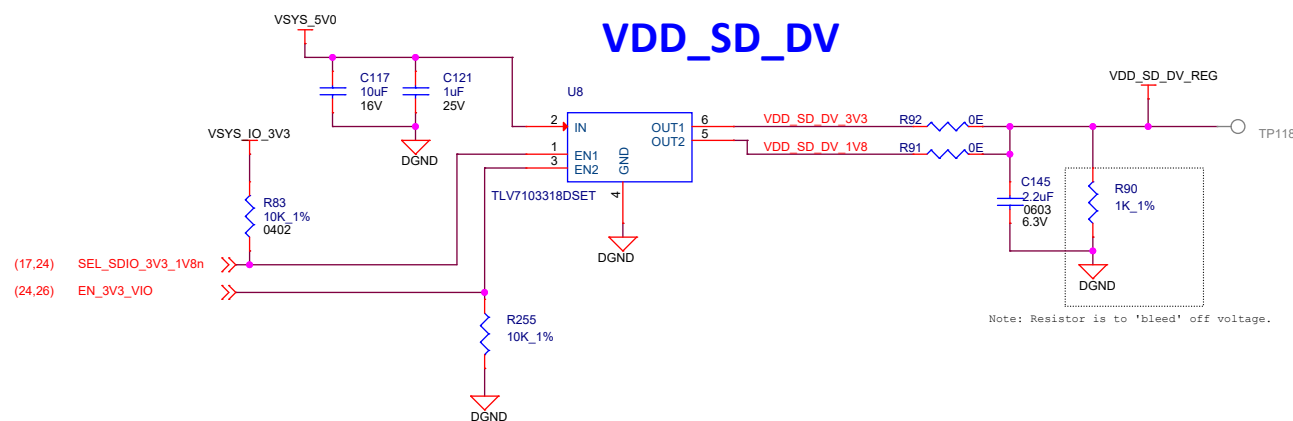
VCC_1V2 - eDP Bridge



VPP_EFUSE_1V8



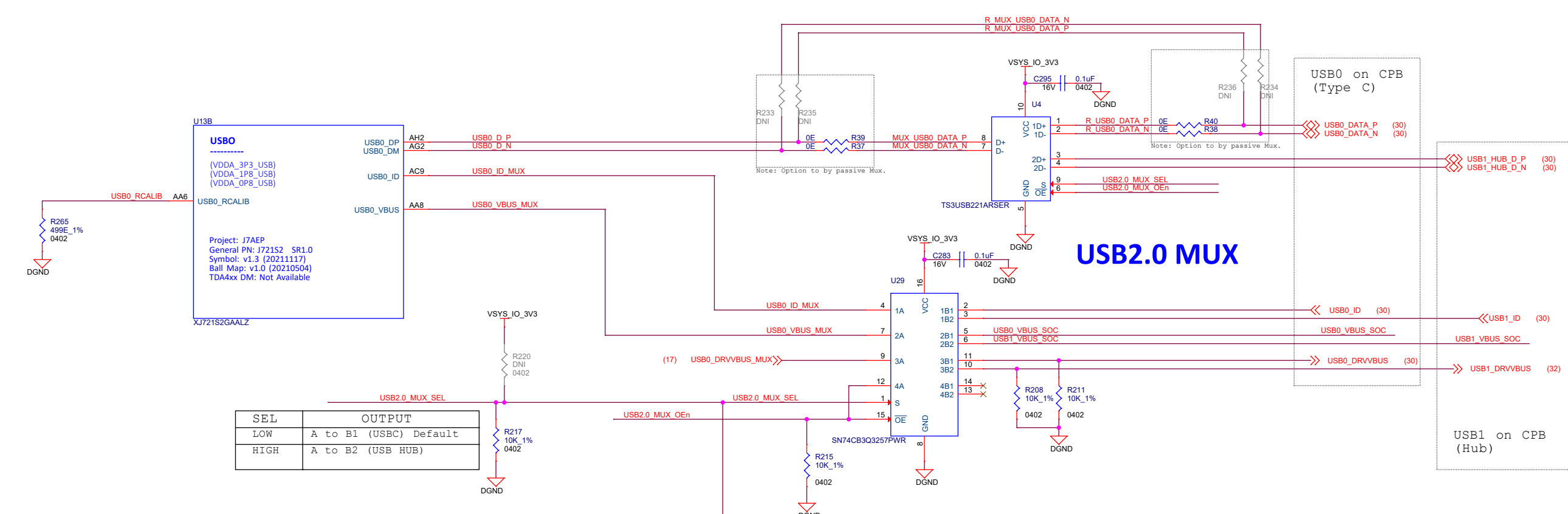
VDD_SD_DV



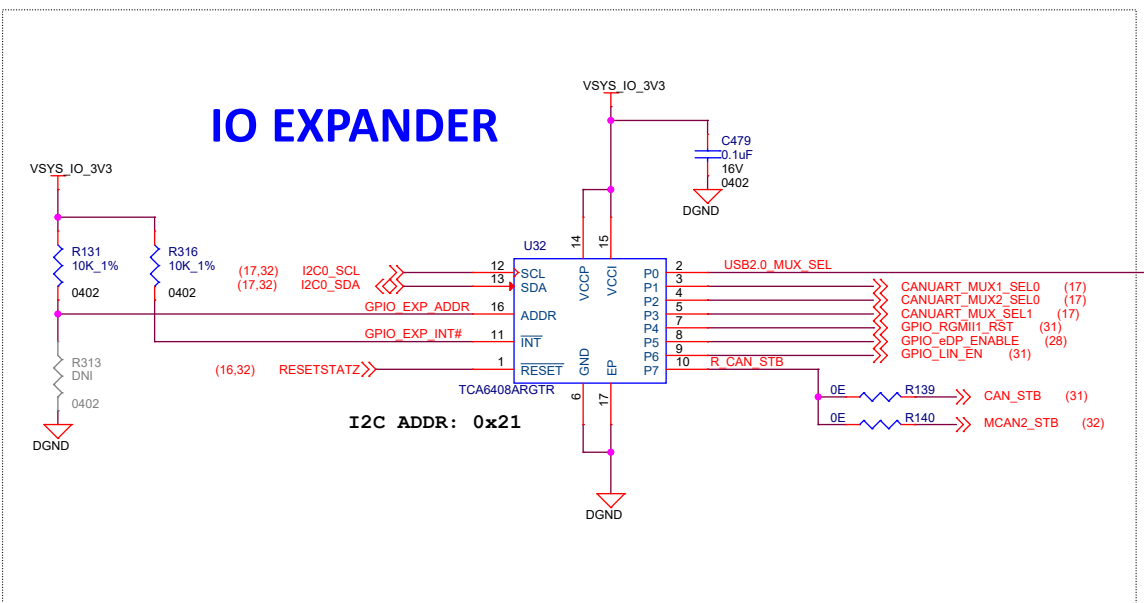
Note: EN EFUSE VPP is used to enable VPP supply. This supply is not enabled by default, and is not part of the standard power up/down sequence. This supply should only be enabled when eFuse programming is being performed on high secure devices. To enable, software will need to configure PMIC's GPIO9 as GPO (output), as NVM defaults to GPI (input)

USB

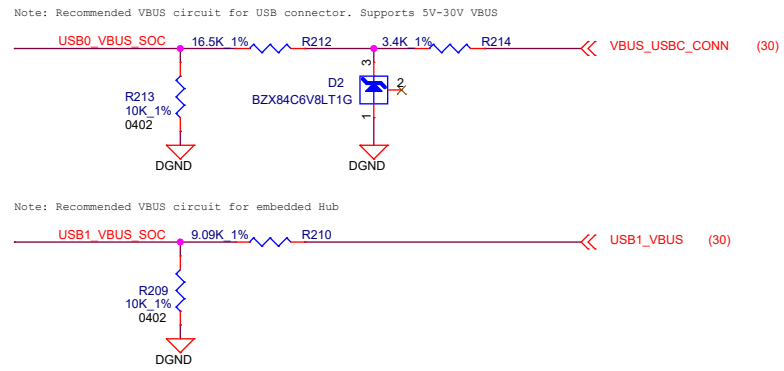
By Pass USB MUX	Mount - R233,R235,R236,R234 DNI - R39,R37,R40,R38
USB MUX (Default)	Mount - R39,R37,R40,R38 DNI - R233,R235,R236,R234



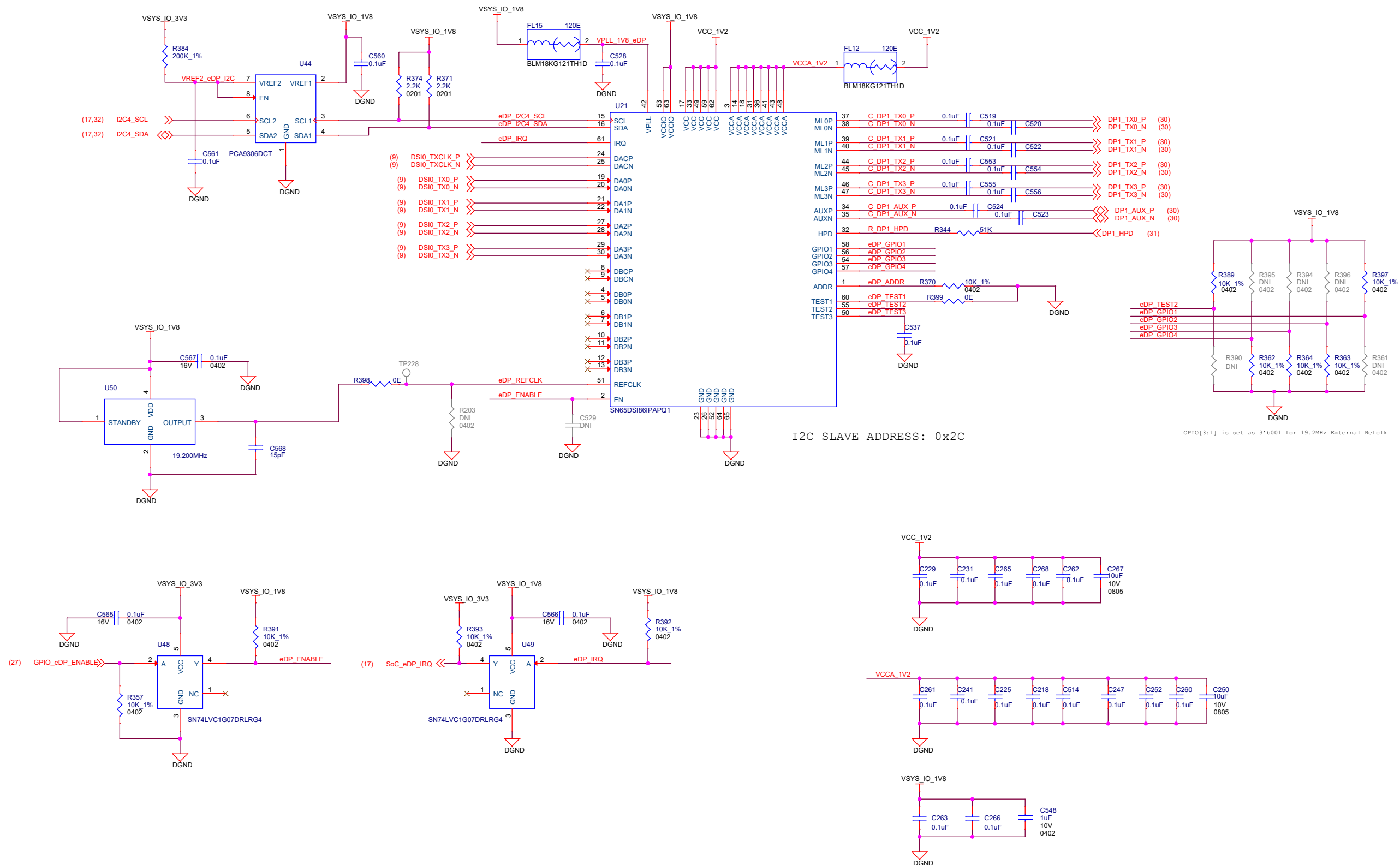
IO EXPANDER



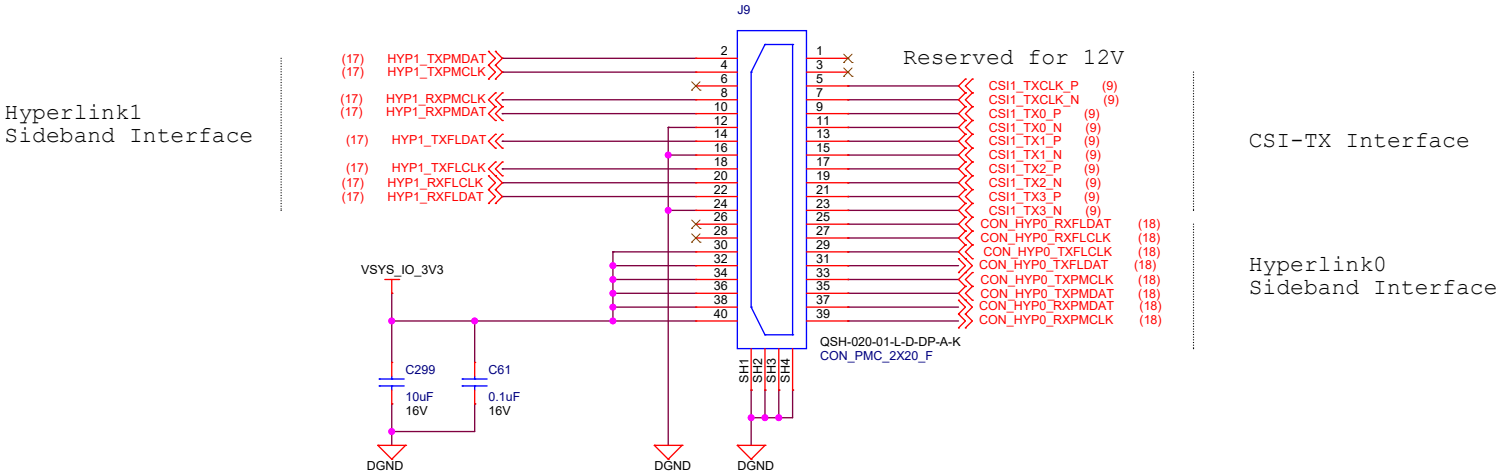
USB VBUS Resistor divider circuit



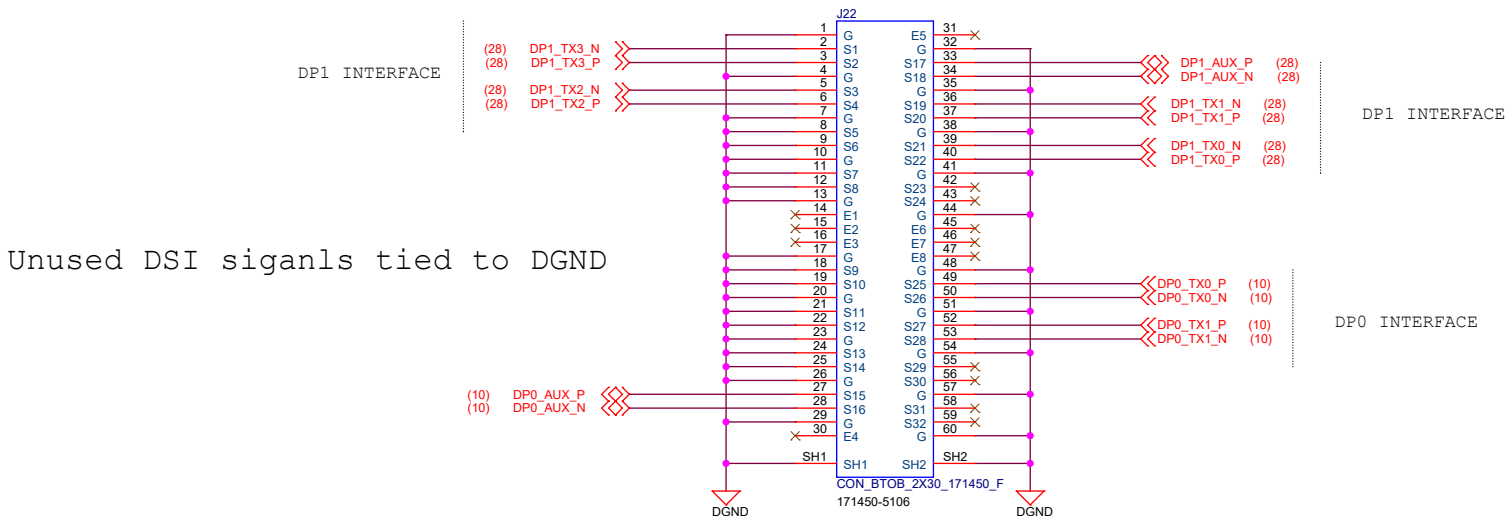
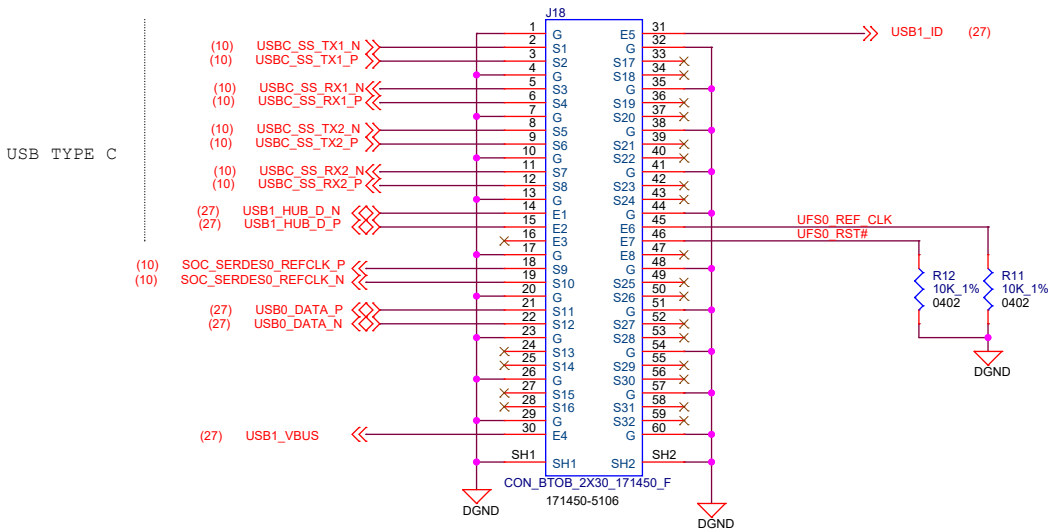
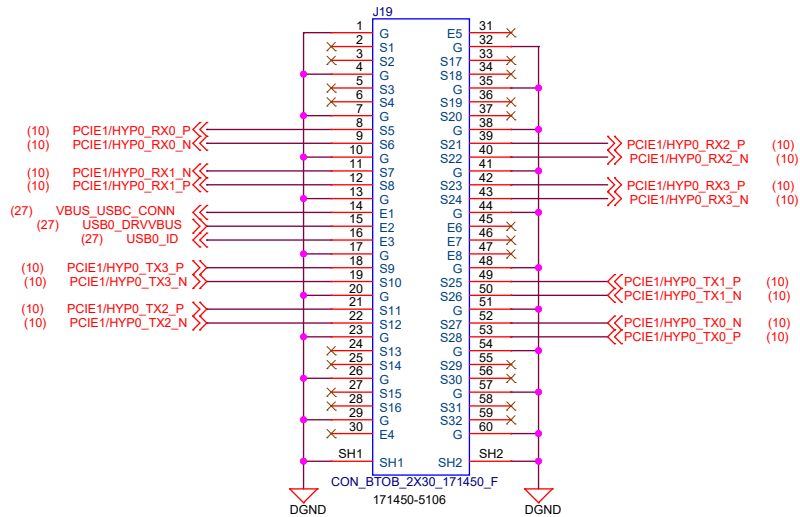
DSI to eDP BRIDGE



HYPERLINK SIDEBAND & CSI-TX CONNECTOR



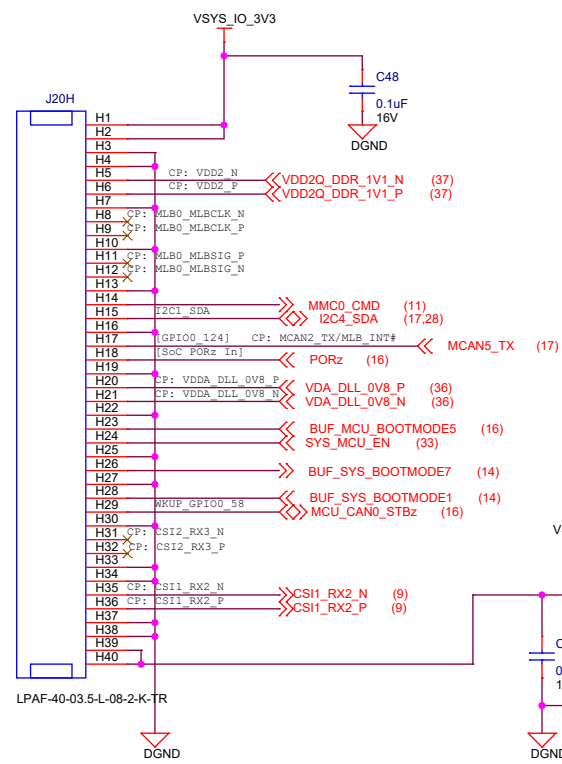
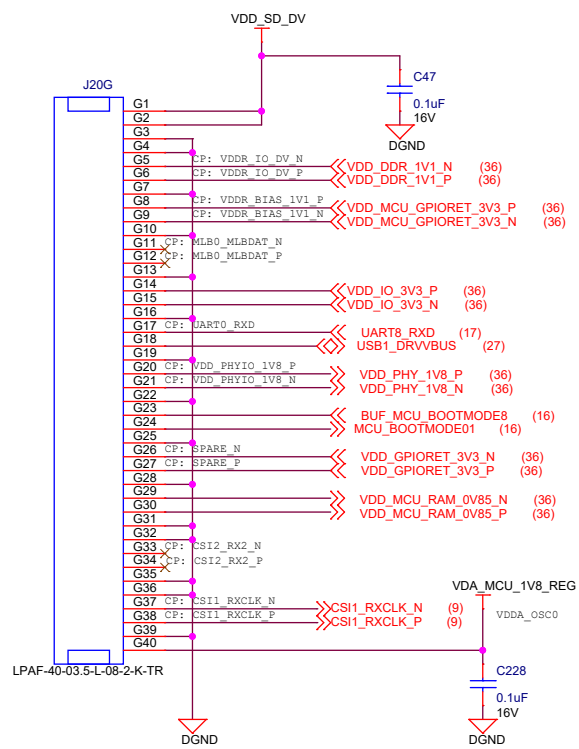
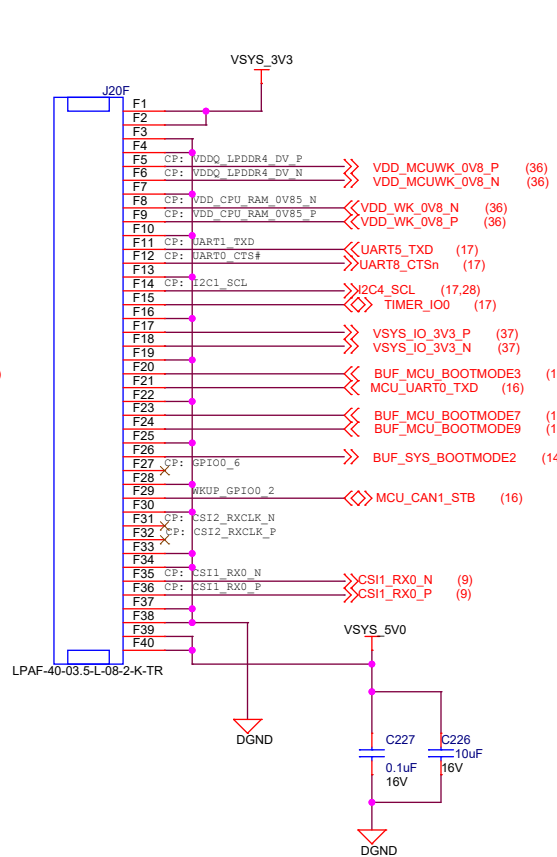
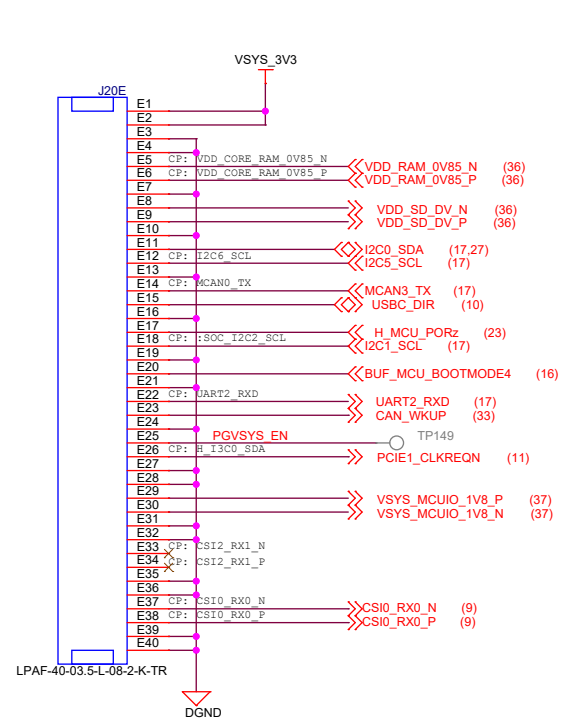
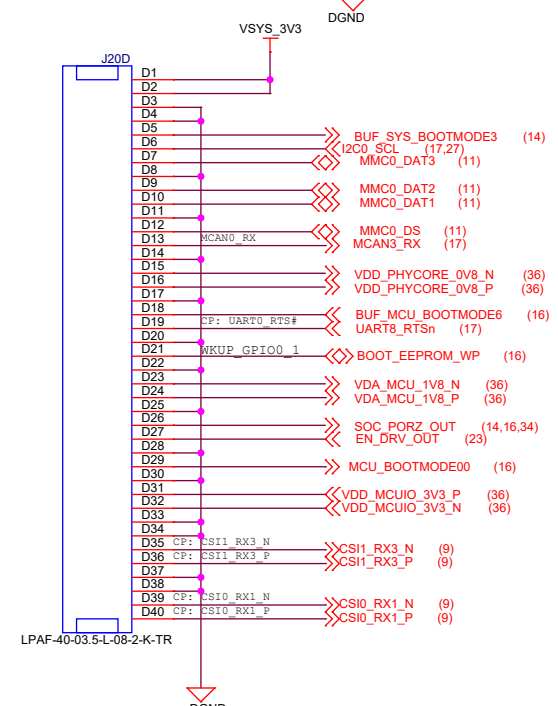
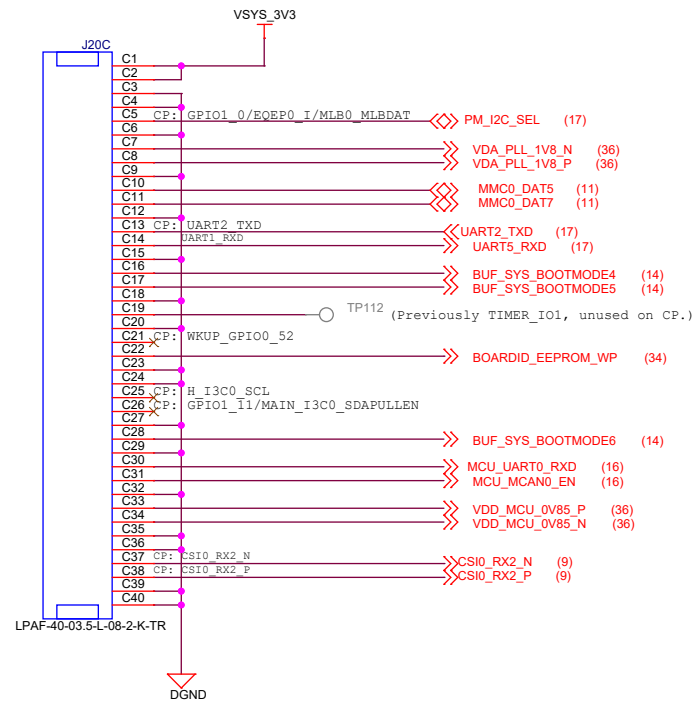
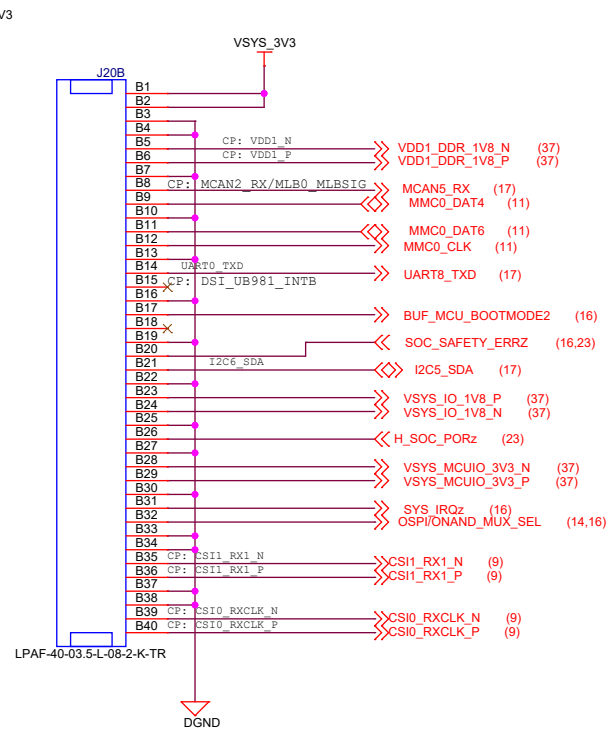
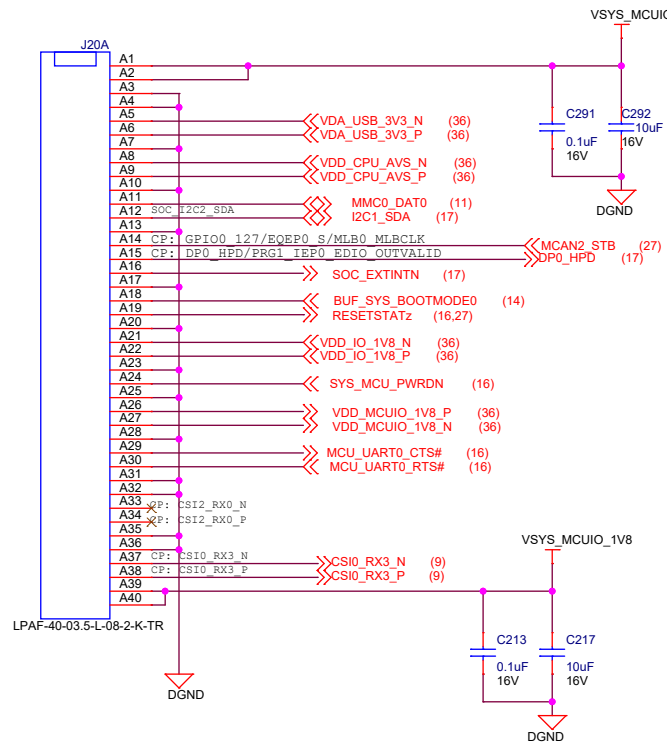
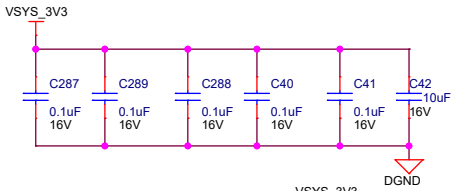
SOM to COMM PROC SERDES CONNECTORS



SOM to COMM PROC PRIMARY CONN #1



SOM to COMM PROC PRIMARY CONN #2

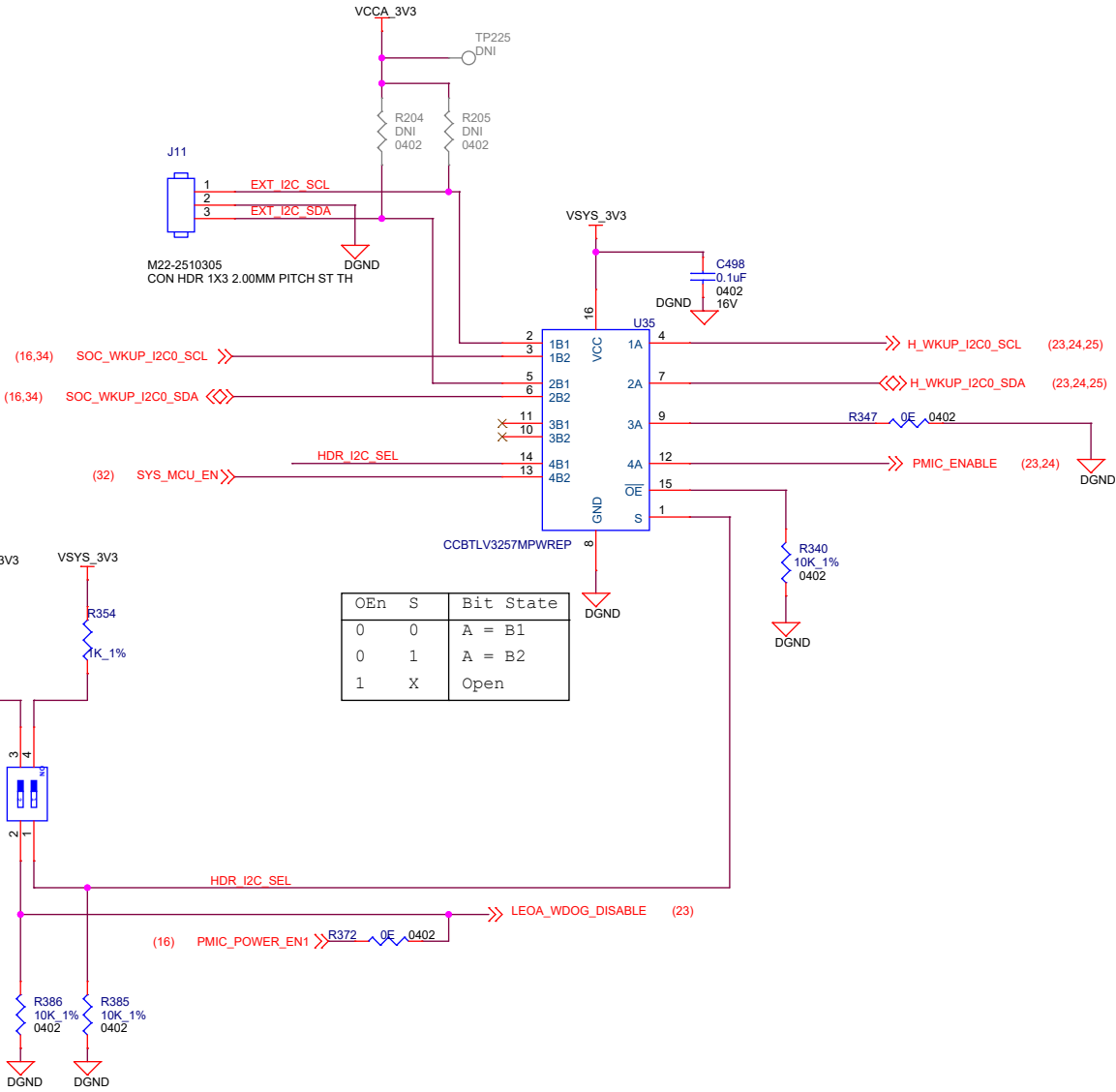


PMIC Support Circuitry

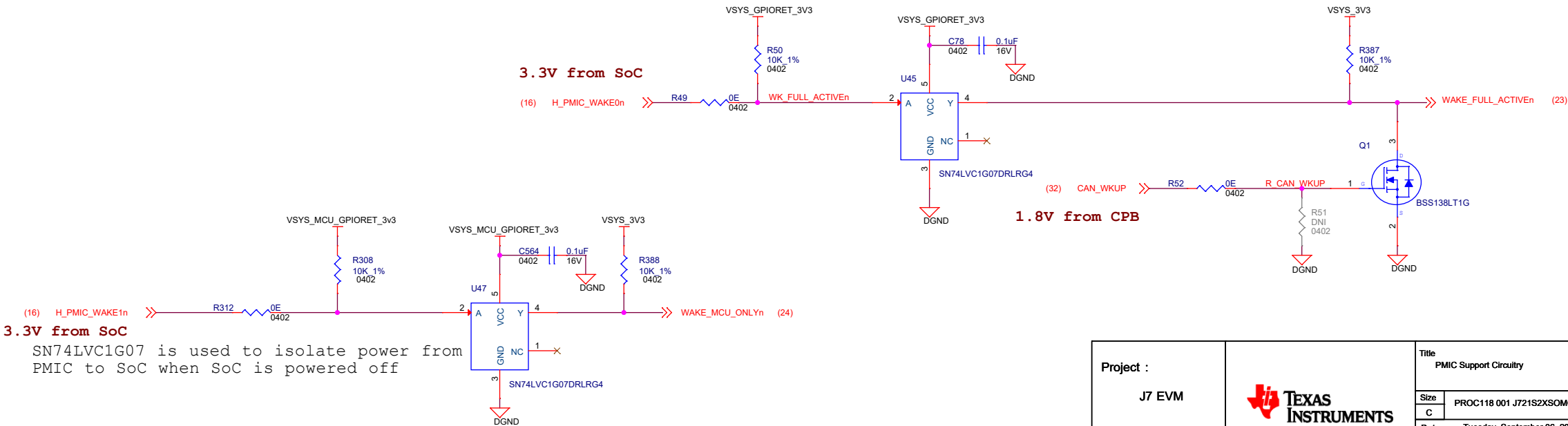
EVM development & evaluation Test circuitry
(TI EVM Only)

(EVM Bd Setting & Leo NVM Default):

SW2	HDR_I2C_SEL	Function
-1 = Closed (High) = Open (Low)	High Low	SoC I2C, PMIC_EN High Ext I2C, PMIC_EN Low
-2 = Closed (High) = Open (Low)	Disable WDOG Timer Enable WDOG Timer	GPIO:Type In In Disable WDOG Enable WDOG



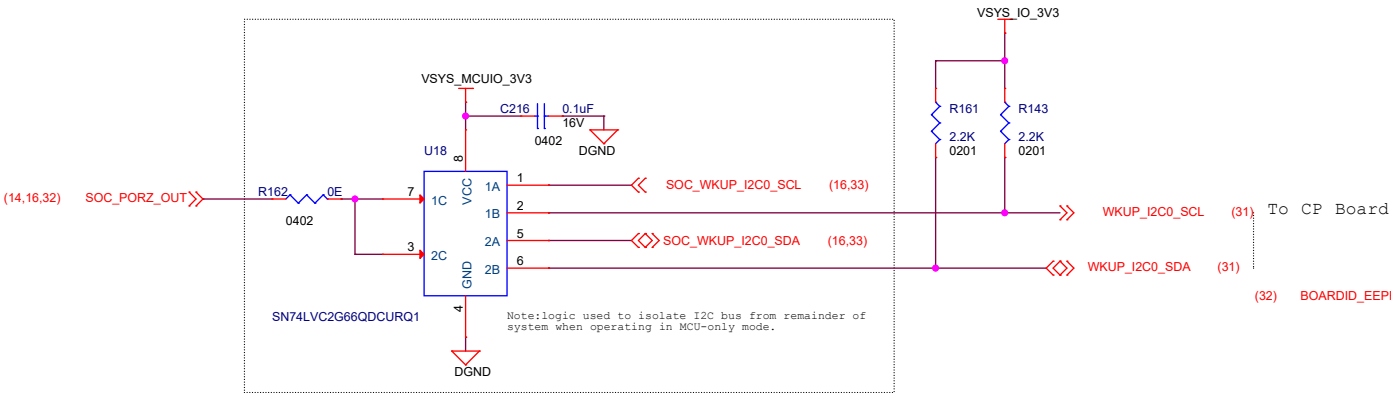
SN74LVC1G07 is used to isolate power from PMIC to SoC when SoC is powered off



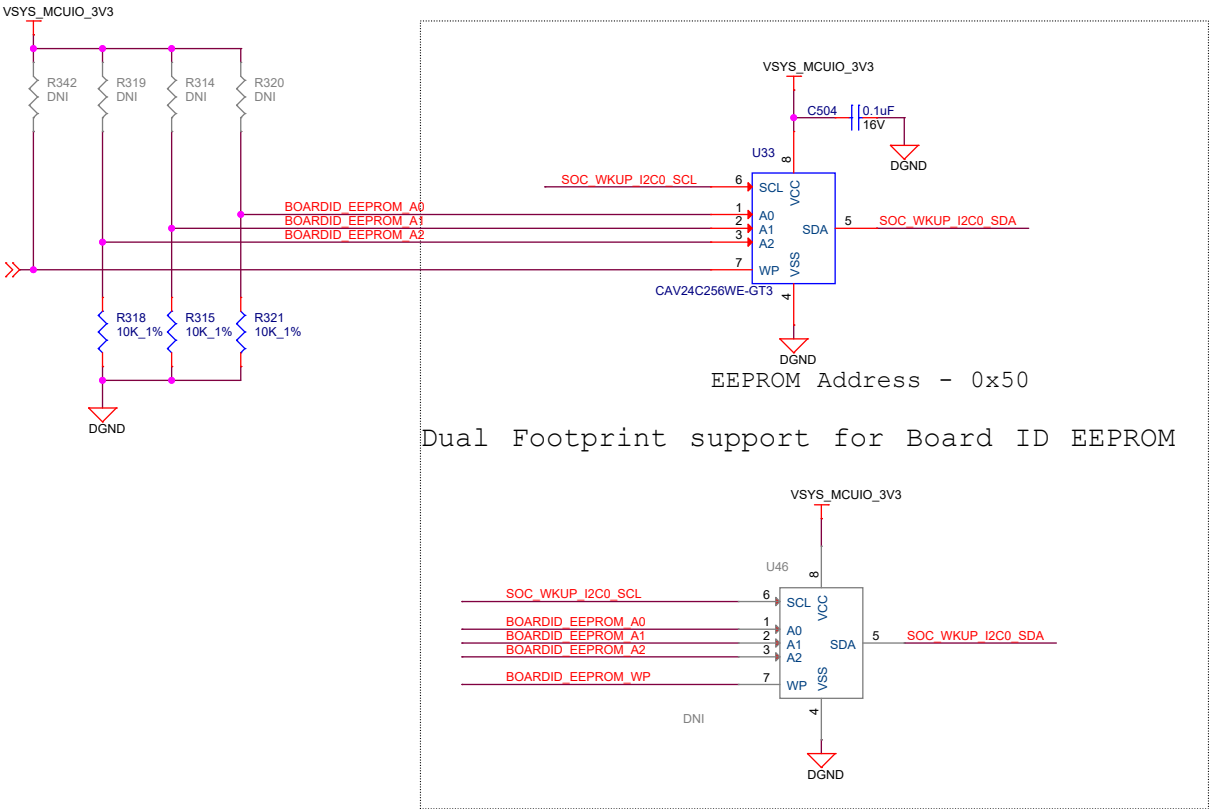
EVM development & evaluation test circuitry

(TI EVM Only)

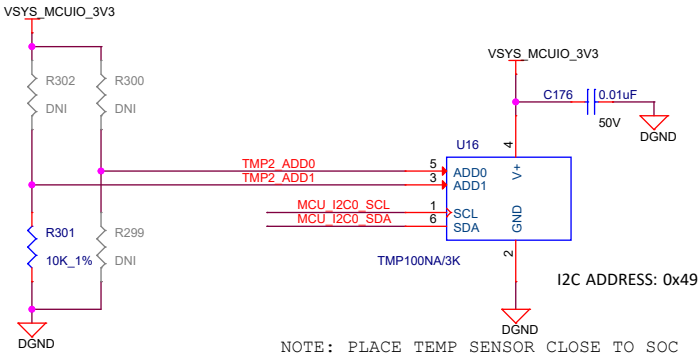
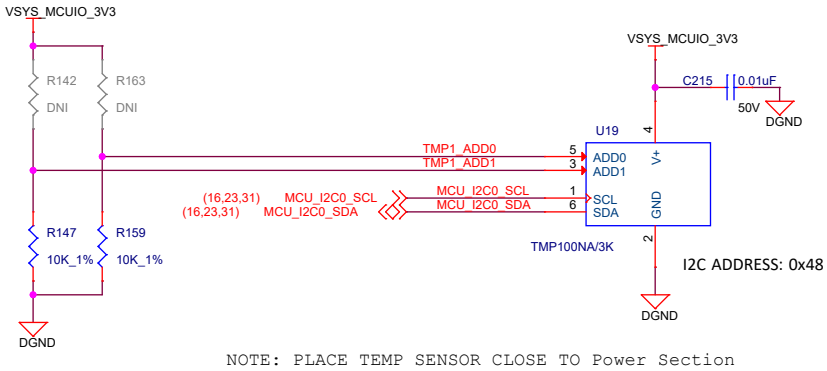
I2C for BOARD ID EEPROMs

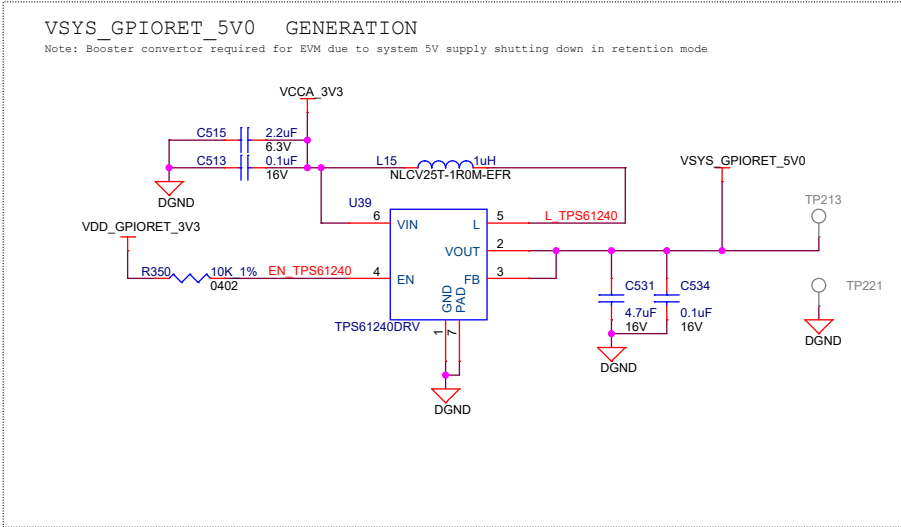


BOARD ID EEPROM (TI EVM Only)

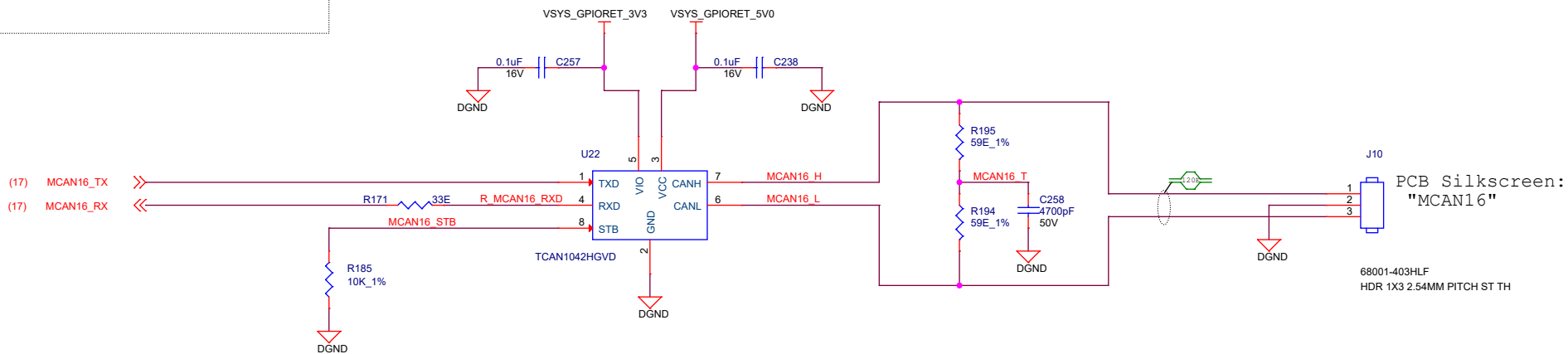


TEMPERATURE SENSORS (TI EVM Only)





CAN TRANSCEIVER

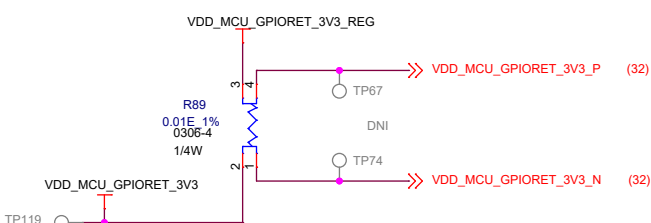
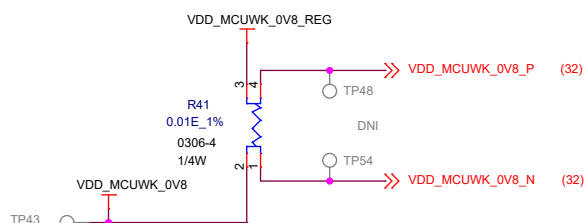
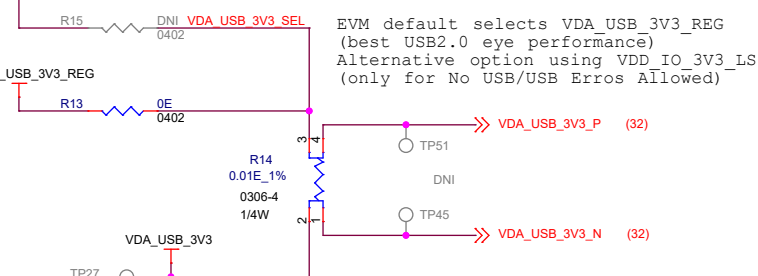
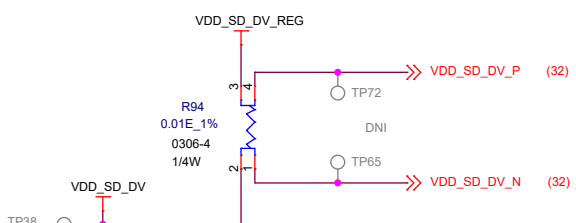
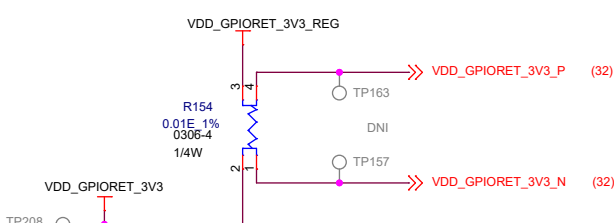
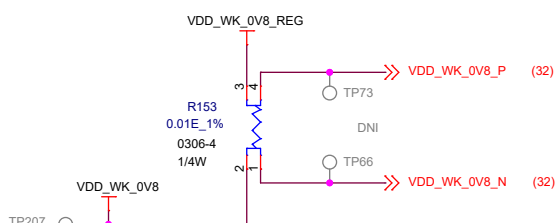
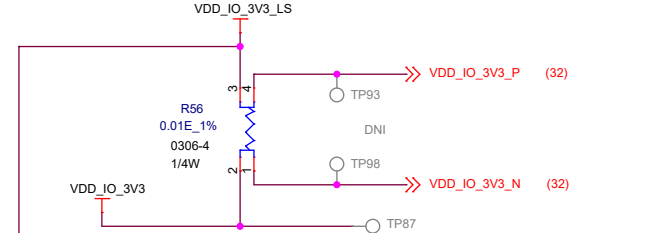
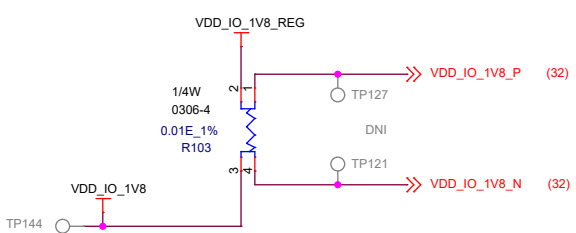
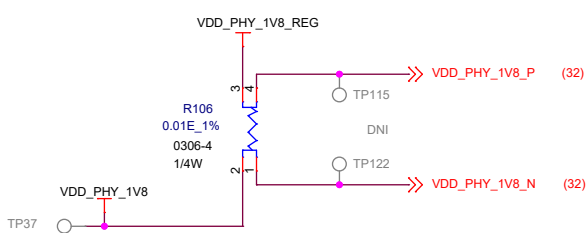
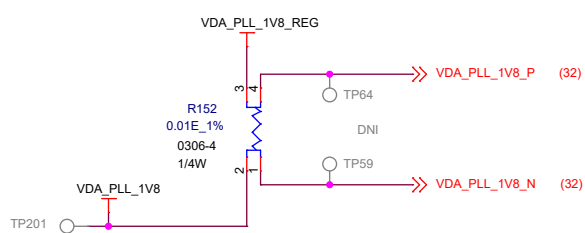
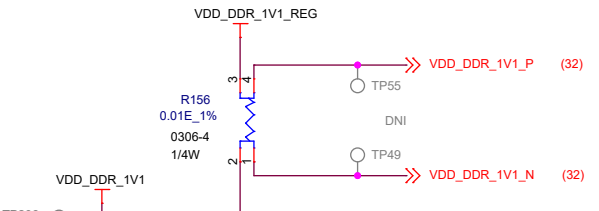
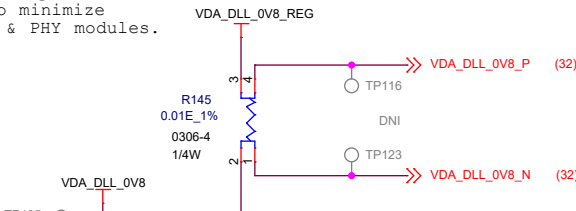
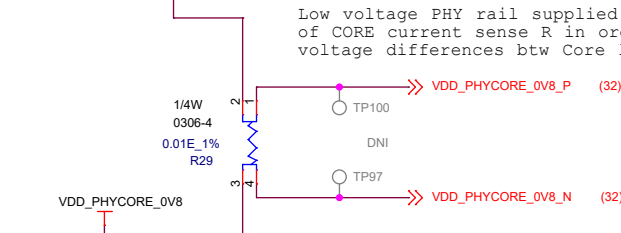
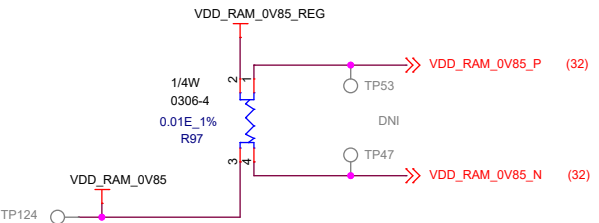
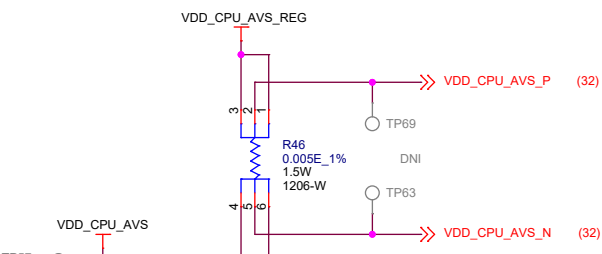
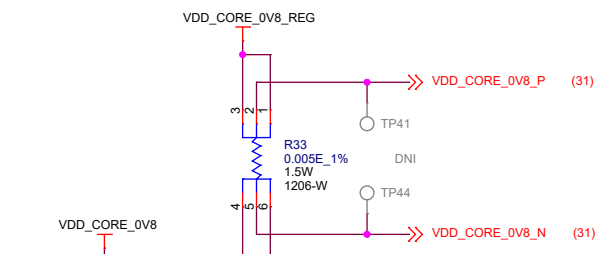
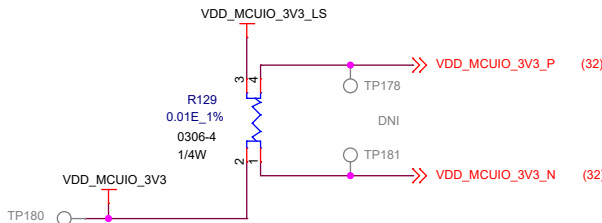
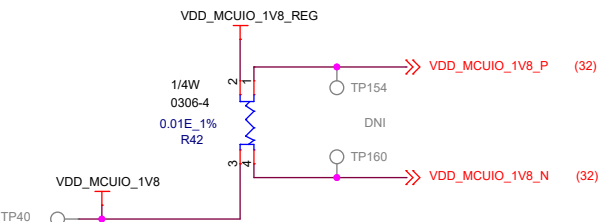
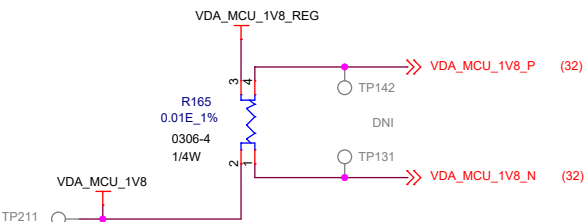
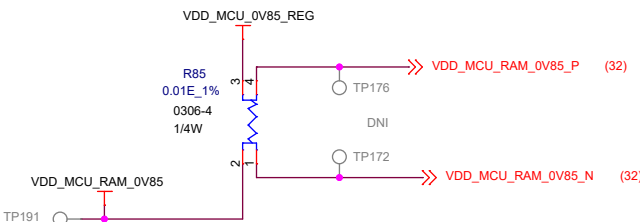
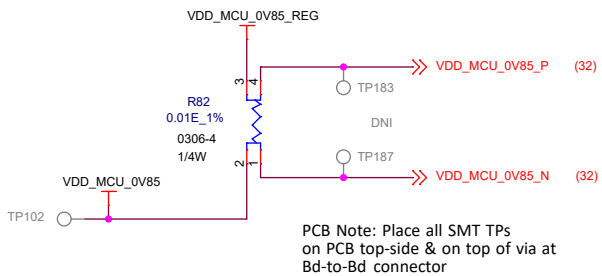


(TI EVM Only)

EVM development & evaluation test circuitry

SOC Current Sense Resistors

(TI EVM Only)

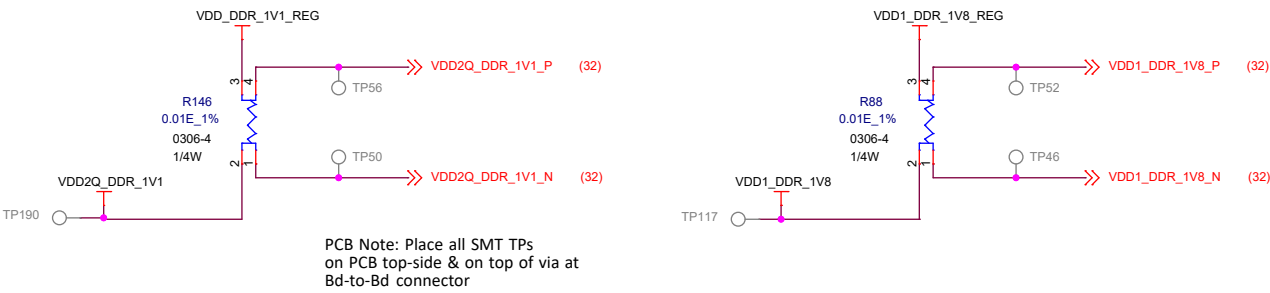


(TI EVM Only)

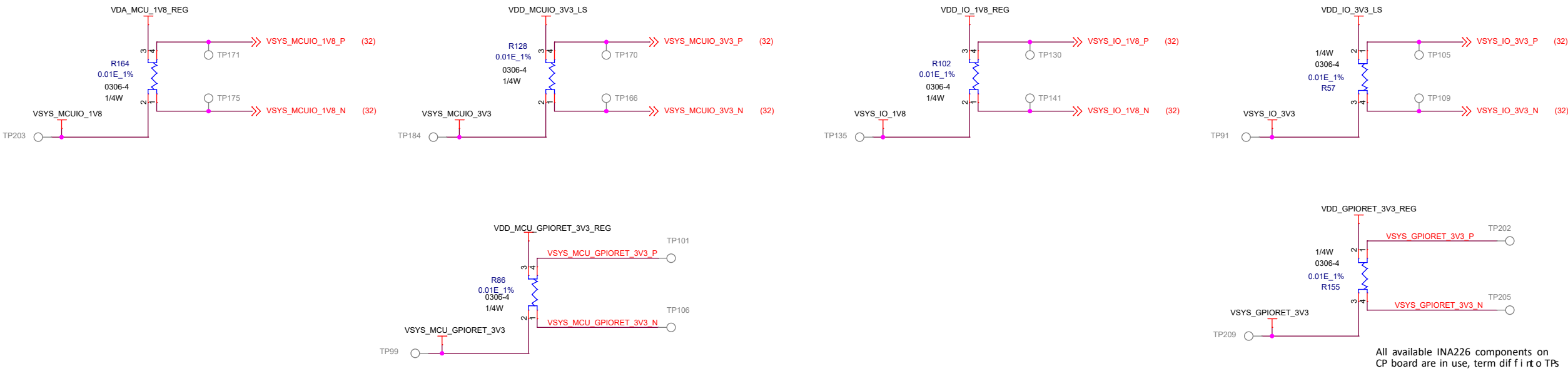
(TI EVM Only)

Project : J7 EVM		Title SOC Current Sense Resistors	
Size C		PROC118 001 J721S2XSOMG01EVM	Rev E4
Date: Tuesday, September 06, 2022		Sheet 36 of 39	

LPDDR4 SDRAM Current Sense Resistors



Peripheral Current Sense Resistors



EVM Development & Evaluation test circuitry

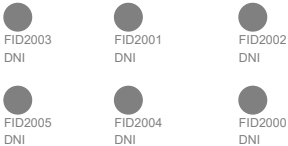
(TI EVM Only)

NOTES, HW & LABELS

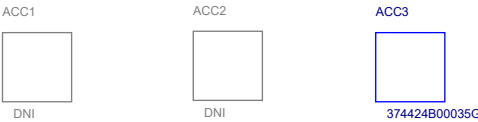
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

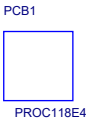
FIDUCIALS



SOCKET, PROCESSOR & HEATSINK AS ACCESSORIES



BARE PCB



LABELS

Board Serial No.



Assembly Revision.



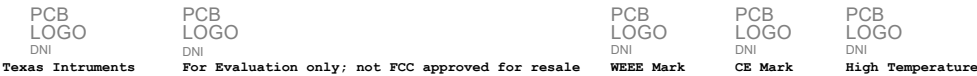
EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J721S2XSOMG01EVM
002:Soldered HS SoC	J721S2XSOMH01EVM
003:Socketed SoC	J721S2XSOMS01EVM

LOGOs



Project :

J7 EVM



Title
EVM NOTES, HW & LABELS

Size
C
PROC118 001 J721S2XSOMG01EVM

Rev

E4

Date: Monday, March 27, 2023

Sheet 38 of 39

SI_SIMULATION_COUPON_BD

Note: Test coupon not part of EVM design, to be used for TI test only

