

J7AEP SOM - DUAL Leo2.0 + HCPS  
(4-Ph Hera1.0 "stand-alone"/GPIO cntlrd)  
Interim PDN-0A for Alpha EVMs ONLY

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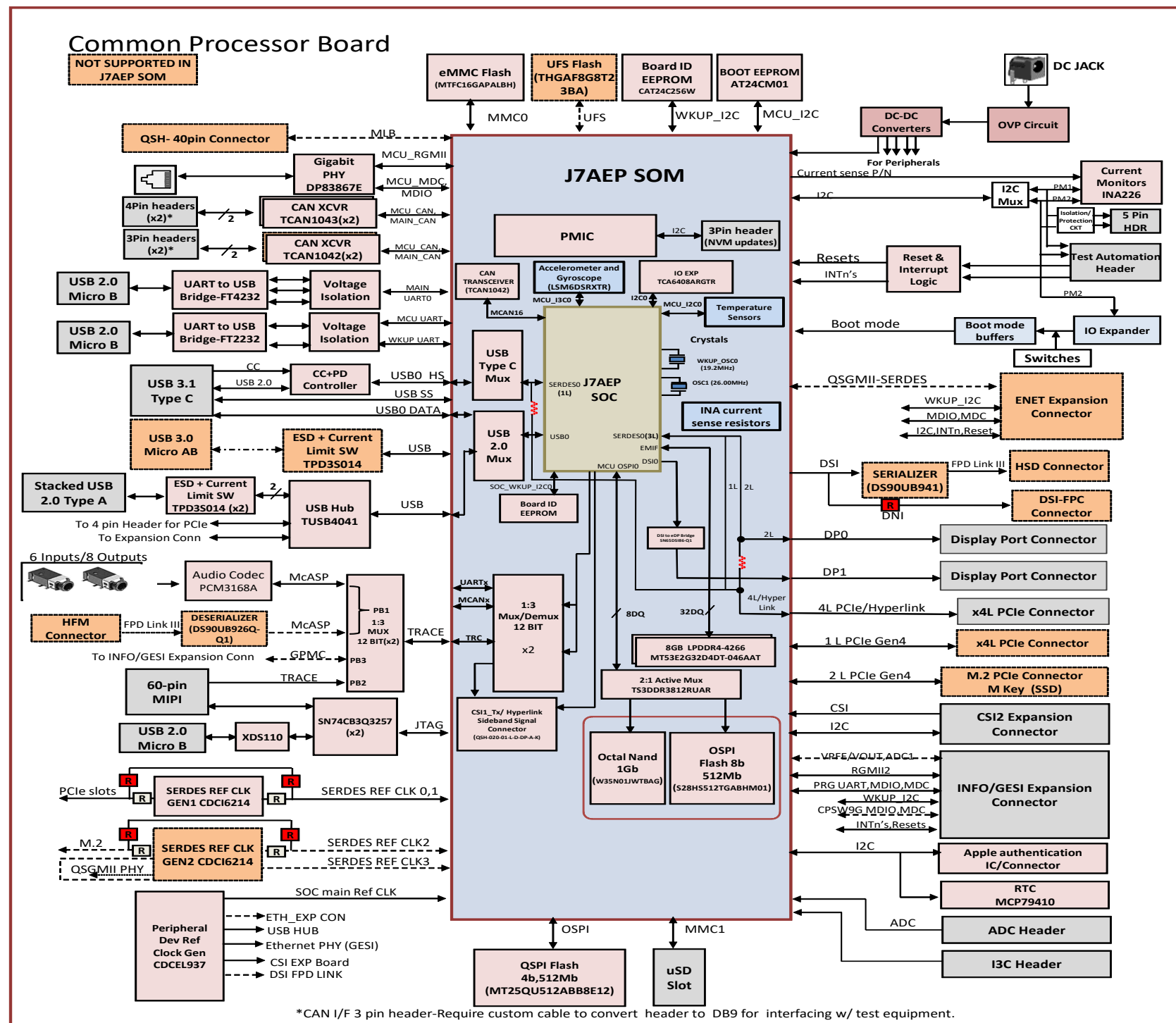
REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	01 JUNE 2021	Added Test Point for MCU_ONAND_CLK, ADC_EXT_TRIGGER0 TP2029,TP2034,TP2028,TP2031,TP2047,TP28,TP22,TP2042 CHANGED FROM 40mil to 30mil Variant Updated	Mistral Design Team		
	02 JUNE 2021	Removed R2316 and Value of R2346, R2329 changed from 0E to 22E Caps and Termination resistor related to Interposer were removed TP36 size changed from 40 mil to 30 mil	Mistral Design Team		
	04 JUNE 2021	Updated for TI's Part-2 review comments Following Caps are deleted as per TI comment VDDAR_CORE_0V85: C954, C954, C955 VDDAR_CPU_0V85: C2226, C2227, C2228 VDD_MCU_0V85: C425 VDD_CPU_AVS: C420, C403, C416 VDDAR_MCU_0V85: C967, C968, C970 TI Review comments updated	Mistral Design Team		
	07 JUNE 2021	V0.7 PDN implemented	Mistral Design Team		
	08 JUNE 2021	Hyperlink Sideband signal bypass resistors optimized	Mistral Design Team		
	09 JUNE 2021	HDR_I2C_SEL connection added to SW2 and removed the 2x1 Header J2006	Mistral Design Team		
	12 JUNE 2021	Integrated Breakout SCH V0P29 (SoC Decap section only, Current Sense Rs not updated)	Mistral Design Team		
	14 JUNE 2021	Implemented TI Review comments	Mistral Design Team		
	15 June 2021	Updated SoC symbol as follows: 1. Added "Symbol: v1.1 (date)" parameter to text for tracking symbol only changes. 2. Moved GPIO0_11 & GPIO0_12 from "MCU RGMII" (sub-symbol "K", pg17) to "General IO" (sub-symbol "M", pg16) to align GPIO's with similar interfaces with output buffers ref to VDDSHV2. 3. Optimized "DDR#_CSN#_Channel#" ball groups (pgs 11 & 12) within SoC symbol to match SDRAM symbol groups to reduce possibility of net connection errors.  Example ball group changes: From: To: DDR0_CSN0_0 (Ch A) DDR0_CSN0_0 (Ch A) DDR0_CSN0_1 (Ch B) DDR0_CSN1_0 (Ch A) DDR0_CSN1_0 (Ch A) DDR0_CSN0_1 (Ch B) DDR0_CSN1_1 (Ch B) DDR0_CSN1_1 (Ch B) Fixed DDR0 (pg11) SCH net connections on "DDR0_CSN#_Ch#" to correct SoC & SDRAM alignment.	TI		
	16 June 2021	Removed the PBs SW2004 & SW2003 and updated the CAN_WKUP logic	Mistral Design Team		
	17 June 2021	Updated for internal review comments	Mistral Design Team	TI	
	18 June 2021	Updated for TI review comments	Mistral Design Team		
	19 June 2021	Updated for TI review comments LEOA_FB_B3 Resistor divider values updated (Vdiv set to 1.5V) Renamed the VDD_MCUWK_0V85_REG to VDD_MCUWK_0V8_REG Hyperlink Sideband signal pinouts updated and added VSYS_IO_3V3	Mistral Design Team		
	21 June 2021	Updated for TI review comments 3T Caps added to input power of PMICs, Resistor Mux option removed for VIO_VIN	Mistral Design Team		
	23 June 2021	Removed the Vdividers from the PMIC Voltage monitor pins Updated the power supply of MOD2000 to VSYS_MCU_GPIORET_3V3 from VDD_MCU_GPIORET_3V3 Removed the resistor R21 and connected VCCA_3V3 directly to VIO_VIN pin of PMIC-A,B & C	Mistral Design Team		
	24 June 2021	Added SMD TPs for the unused Voltage mointor pins	Mistral Design Team		
	29 June 2021	Added 0E resistor b/w Gnd & U13-9	Mistral Design Team		
	29 June 2021	Updated the PU supply of I2C1_SCL_MUX/I2C1_SDA_MUX to VSYS_IO_3V3	Mistral Design Team		
	01 July 2021	Updated for TI review Comments Made PMIC B OSC32KCAP pin as NC Pull Up added to external EXT_I2C_Sxx Signals	Mistral Design Team		
	06 July 2021	UART5_TXD and RXD swapped Moved DDR0 de-embedding circuit to DDR1	Mistral Design Team		
	08 July 2021	SI_DDR_0&1_CA5 Signal Coupon Components removed, J2000 connector Pin 26 and 28 are made as NC	Mistral Design Team		
	12 July 2021	PCB back annotated SCH Updated	Mistral Design Team		
	14 July 2021	R294,R269,R365,R368 and R144 are made as DNI	Mistral Design Team		
	15 July 2021	SPI5_CS0 signal moved from J21.B17 to J21.F13.	Mistral Design Team		
	26 July 2021	500E resistors R238,R47,R48,R53,R265 are replaced with 499E, R150 is made as DNI	Mistral Design Team		
E1A	25 Aug 2021	SoC Symbol Updated: IO BANK LABEL in Block A and C is updated	Mistral Design Team		

REVISION HISTORY CONT'D

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1B	13 OCT 2021	C491 and C476 is replaced by 10uF having MFR PART# GRT155C80E106ME13D Part L4, L8, L9 and L10 Inductors are replaced by 0.47uH Inductor	Mistral Design Team		
E1C	14 OCT 2021	R358 is Mounted and R359 is DNI'd	Mistral Design Team		

## SoM SYSTEM BLOCK DIAGRAM



### (Power Rail & GPIO Mapping Overview)

Will be updated w/ Hera PG2.0 on EVM APL/  
Production release recmd for customer  
designs.

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ isolated Main & MCU power rails (supply FFI)
3. 2x SDRAMs: 32Gb, 4-Die, 32b, 4266MT/s, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:

- a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
- b. Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
- c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)

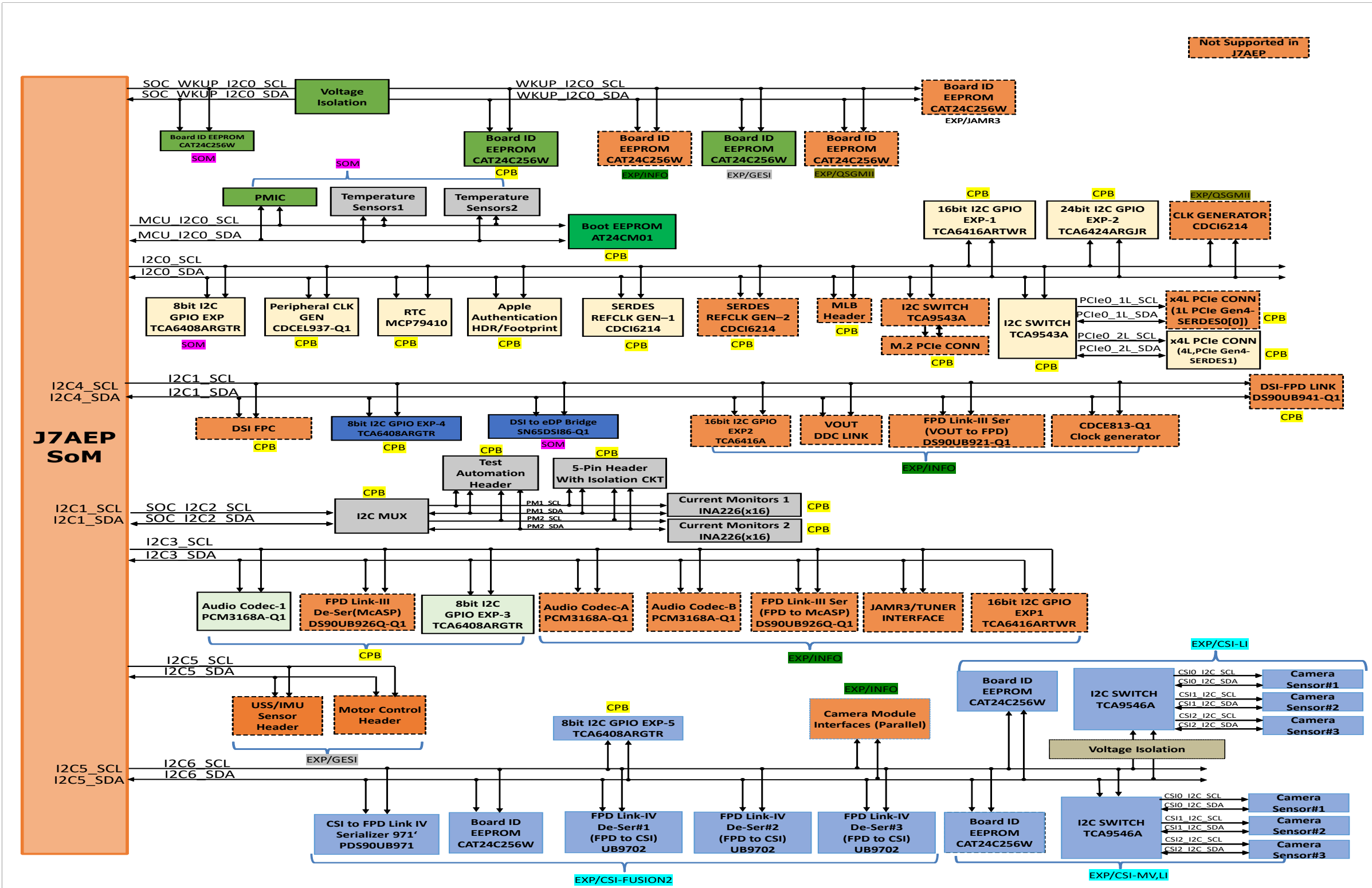
- a. MCU Island/Only with Dual VIO (needs 4 indep pwr rails & 1 cntrl signal)
- b. MCU & Main GPIO Retention (needs 4 indep pwr rails & 2 cntrl signals)
- c. DDR Retention/S2R (needs 1 add'l indep pwr rail & 1 cntrl signal)

V0.1	3/6/2021	Initial capture sts from TDA0M1V-3 Ph3 Dual Leo2.0 FPM-OC v3.16
V0.2	4/1/2021	New mapping for DDR1 LV to use 8-bits, Buckle (64) and 16-bit analog data for lower power 32mhz (FPM-OC) and adding of older 42mhz quad
V0.3	4/9/2021	New mapping for TDA0M1V-3 Ph3 Dual Leo2.0 FPM-OC v3.16, Buckle (64) and 16-bit analog data for lower power 32mhz (FPM-OC) and adding of older 42mhz quad
V0.4	4/9/2021	Replaced 2-Ph Tag with the PGL10 in "stand-alone GPIO" mode of exp for VDD_CORE power resource.
V0.5	4/19/2021	1" Pass power & GPIO mapping complete, ready for PMIC team review. 1. Updated discrete LDO Pto to align with, fixed VDD.
V0.6	5/26/2021	2. Moved EN_EFUSE_VDD control signal to preferred source from SW GPIO 3. Captured new ITAP2/IT2121 block diagram symbol & connected to FPM power rails & signals
V0.7	6/1/2021	1. Updated all PMIC orderable Pto per iPM settings 2. Changed PMIC-B, SW GPIO 3 connected net name from EN_VDD0_V18 to EN_VDD0_V18 to avoid confusion with Open-Drain net names specifying pull-up logic levels per part, "vfy" of pattern.
V0.8	6/1/2021	1. Updated initial PMIC GPIO assignments following NVM 1.0.1.1
V0.9	6/1/2021	2. Changed PMIC-A NVM to supply 0.0V to EN_VDD0_WAEL power rail instead of 0.8V. Silicon team believes op MCU will logic to lower voltage vs MCU core over current. Once verified, then need Rev 5eM could consolidate "GPIF_REF" rails to PMIC-A. This would allow PMIC-B's LDO 1.8 to 2x supply VDDA_VDD3_VDD3_VDD4_VDD5 in block diagram of 2x discrete LDOs.
V1.0	6/15/2021	1. All 3 PMIC GPIO to function NVM defaults captured in block diagram of PMIC settings review 2. Added "realized" name, to tagger for ID of PMIC GPIOs & signals that must be SW configured following SW standard book-up.
V1.1	6/15/2021	3. Connecting EN_EFUSE_VDD control signal from PMIC since SW GPIOs are limited.
V1.2	6/15/2021	4. Provision using SW iMON values for VDD_PHH1_7D to 8x access to add 10k are desired for testing





SoM I2C TREE DIAGRAM



SoM I2C ADDRESS TABLE

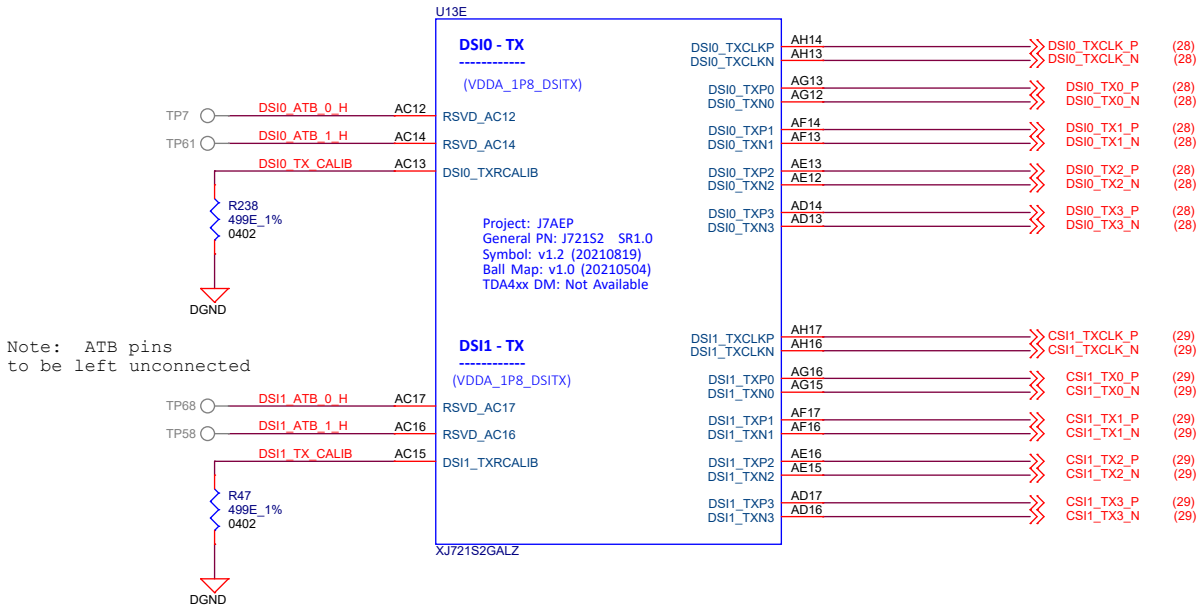
Board	Interface name	Part#	Address	J721E/CPB Port mapping	J7AEP Port mapping
EVM/SoM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0	WKUP_I2C0
EVM/CPB	Board ID EEPROM	CAT24C256W	0x51		
EXP/GESI	Board ID EEPROM	CAT24C256W	0x52		
EVM/SoM	PMICs	PMIC A: TPS659413	PMIC A: 0x48, 0x49, 0x4A & 0x4B		
		PMIC B: TPS659411	PMIC B: 0x4C, 0x4D, 0x4E & 0x4F		
		PMIC C: P876411A5RQKRQ1	PMIC C: 0x58, 0x59, 0x5A & 0x5B		
EVM/SoM	Temperature Sensors	TMP100NA/3K	0x48, 0x49	MCU_I2C0	MCU_I2C0
EVM/CPB	Boot EEPROM	AT24CM01	0x50, 0x51	Main I2C0	Main I2C0
EVM/SoM	8 bit I2C GPIO Expander	TCA6408ARGTR	0x21		
EVM/CPB	SerDes Clock gen #1 Optional	CDCI6214	Optional		
EVM/CPB	SerDes Clock gen #2	CDCI6214	0x77,0x76		
EVM/CPB	Pheriphal Clock Gen	CDCEL937-Q1	0x6D		
EVM/CPB	16bit I2C GPIO EXPANDER1	TCA6416ARTWR	0x20		
EVM/CPB	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22		
EVM/CPB	8 bit I2C GPIO Expander4	TCA6408ARGTR	0x20		
EVM/SoM	DSI TO eDP BRIDGE	SN65DSI86IPAPQ1	0x2C	Main I2C1	Main I2C4
EVM/CPB	DSI FPC Connector	<connector interface>		Main I2C2	Main I2C1
EVM/CPB	I2C Switch for Automation header		0x22		
EVM/CPB	Current Monitors and Header		0x40 to 0x4F		
EVM/CPB	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3	Main I2C3
EVM/CPB	FPD Link iii Deserializer	DS90UB926Q-Q1	0x2C		
EVM/CPB	AUDIO IF Codec	PCM3168A-Q1	0x44		
EXP/CSI-FUSION2	I2C IO Expander	PCA9536DGKR	0x41	Main I2C6	Main I2C5
EXP/CSI-FUSION2	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52		
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	0x3D		
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x30		
EXP/CSI-FUSION2	CSI to FPD Link IV Serializer 971	UB971	0x18		
EXP/CSI-LI	Board ID EEPROM (Leopard Imaging Adapter)	CAT24C256W	0x52		
EXP/CSI-LI	I2C MUX Camera sensors	TCA9543APWR	0x70		
EXP/CSI-MV	Board ID EEPROM (Machine Vision Application)	CAT24C256W	0x52		
EXP/CSI-MV	Camera Sensor #1	IMX264LQR-C	TBD		
EXP/CSI-MV	Camera Sensor #2	IMX264LQR-C	TBD		
EXP/CSI-MV	I2C MUX Camera sensors	TCA9543APWR	0x70		

SoC GPIO MAPPING TABLE

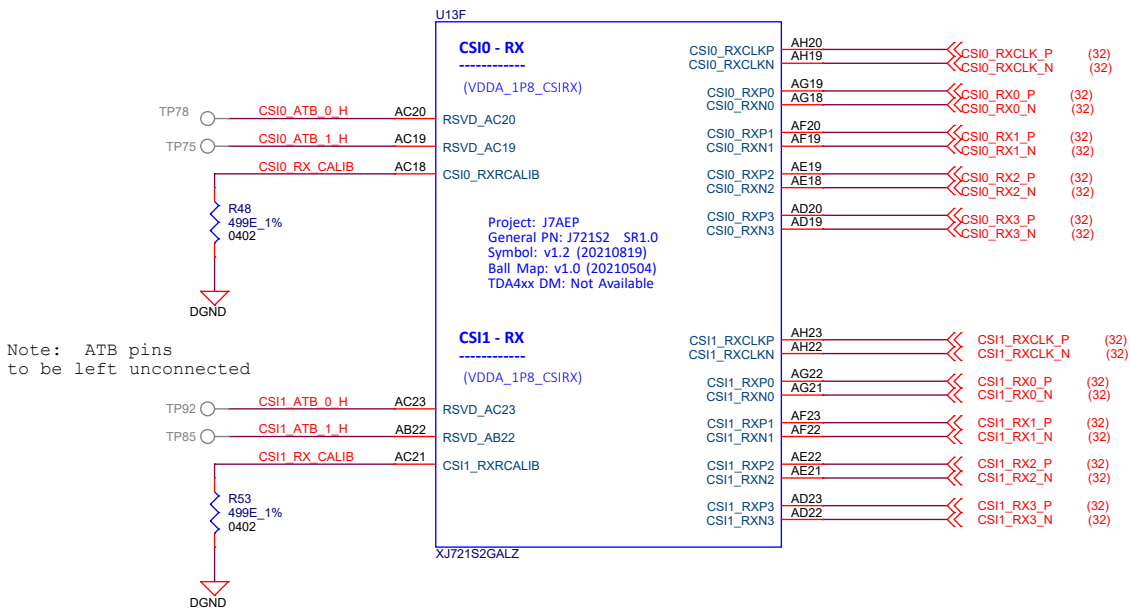
J7x SoM - GPIO Mapping Table						
WKUP Domain						
Net name	J7AEP Mapping		Input/Output	Default	State	Remarks
	Package Signal Name	GPIO Number				
MCU_MCAN0_EN	WKUP_GPIO0_0	WKUP_GPIO0_0	Output	BOOTMODE	Active High	MCU CAN0 Enable
BOOT_EEPROM_WP	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	BOOTMODE	Active High	Boot EEPROM Write protect
MCU_CAN1_STB	WKUP_GPIO0_2	WKUP_GPIO0_2	Output	BOOTMODE	Active High	MCU CAN1 Standby
GPIO_MCU_RGMII1_RST#	WKUP_GPIO0_56	WKUP_GPIO0_56	Output	BOOTMODE	Active low	MCU_RGMII1_Reset
SYS_IRQz	WKUP_GPIO0_7	WKUP_GPIO0_7	Input	NA	Active low	Push-button Interrupt, User Defined/Wake S2R ('0>'1' - interrupt pending, '1' - normal operation)
OSPI/ONAND_MUX_SEL	WKUP_GPIO0_6	WKUP_GPIO0_6	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - OCTAL NAND)
PMIC_MCU_INT# / H_MCU_INT#	MCU_OSPI1_CSN1	WKUP_GPIO0_39	Input	PU	Active low	Interrupt from PMIC
OSPI0_INT#/ECC_FAIL	MCU_OSPI0_CSN3	WKUP_GPIO0_30	Output	PU	Active High	OSPI0_ECC_FAIL (Mux option w/ HYPERBUS_CKn), MCU_OSPI0_ECC_FAIL is DNI resistor option.
MCU_RGMII1_INT#	WKUP_GPIO0_3	WKUP_GPIO0_3	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
SYS_MCU_PWRDN	MCU_SPI0_D0	WKUP_GPIO0_55	Output	BOOTMODE	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_CAN0_STBz	MCU_SPI0_D1	WKUP_GPIO0_69	Output	BOOTMODE	Active low	MCU CAN0 Standby
LSM6DSRX_INT	WKUP_GPIO0_57	WKUP_GPIO0_57	Input	BOOTMODE	NA	Interupt from I3C Gyroscope sensor(*LSM6DSRX)
CANIO_RET_WAKE	MCU_SPI0_CS0	WKUP_GPIO0_70	Input	PU	NA	Push-button wake signal
Main Domain						
SOC_EXTINTN	EXTINTN	GPIO0_0	Input	PU	Active low	Push-button Interrupt, User Defined
MAIN_CANIO_RET_WAKE	GPIO0_11	GPIO0_11	Input	PU	NA	Push-button wake signal
C_MCASP10_ACLKR	MCASP0_AXR2	GPIO0_18	Input	PU	Active low	CSI2 IO expander Interrupt.('0' - interrupt pending, '1' - no interrupt) (IOEXP5_INT#)
TRC_DATA11	MCAN0_TX	GPIO0_25	NA	PU	Active low	I2C0 IO expander interrupt. ('0' - interrupt pending, '1' - no interrupt)(I2C0_IOEXP_INT#) Note: GPIO only available from Trace/GPMC Mux
SEL_SDIO_3V3_1V8n	MCAN15_RX	GPIO0_8	Output	PU	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
USBC_DIR	Used for High Speed Mux control		Input	PU	NA	USB Type C Cable Orientation. Type-C plug position 2 (H); Type-C plug position 1 (L)
CSI2_EXP_A_GPIO2	MCAN0_TX	GPIO0_26	I/O	NA	NA	CSI2 Expansion Board Specific. MV - Used for CSI0_XTRIG; LI - Used for CSI0_GPIO0
GPIO_RGMII1_INT#	HYP0_RXPMCLK_MUX	GPIO0_23	Output	PU	Active low	RGMII1_Reset
CSI2_EXP_A_GPIO4	MCAN1_RX	GPIO0_28	I/O	NA	NA	CSI2 Expansion Board Specific. MV - Used for CSI1_XTRIG; LI - Used for CSI1_GPIO0
PM_I2C_SEL	SPI0_CS0	GPIO0_51	Output	PD	NA	CP Board - PM I2C Mux seletion. ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA) GESI - Boosterpack_GPIO1
GPIO Expander						
I2C Instance	Port	Net Name	Input/Output	Default	State	Usage
I2C0 ADDR: 0x21	P00	USB2.0_MUX_SEL	Output	PD	Active High	Signal Mux Control ('0' - USB, '1' - USB Hub)
	P01	CANUART_MUX1_SELO	Output	PU	Active High	Select line for CANUART_MUX1
	P02	CANUART_MUX2_SELO	Output	NA	Active High	Select line for CANUART_MUX2
	P03	CANUART_MUX_SEL1	Output	PU	Active High	Select line shared for both thr CANUART_MUX
	P04	GPIO_RGMII1_RST	Output	PU	Active High	Routed to INFO/GESI expansion connector. GESI - Used for GPIO_PRG0_RGMII_RST; INFO - Not used
	P05	GPIO_eDP_ENABLE	Output	NA	Active High	Used for Enable of DSI to eDP Bridge
	P06	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
	P07	CAN_STB/MCAN2_STB	Output	PU	Active High	Standby signals for CAN Transceivers



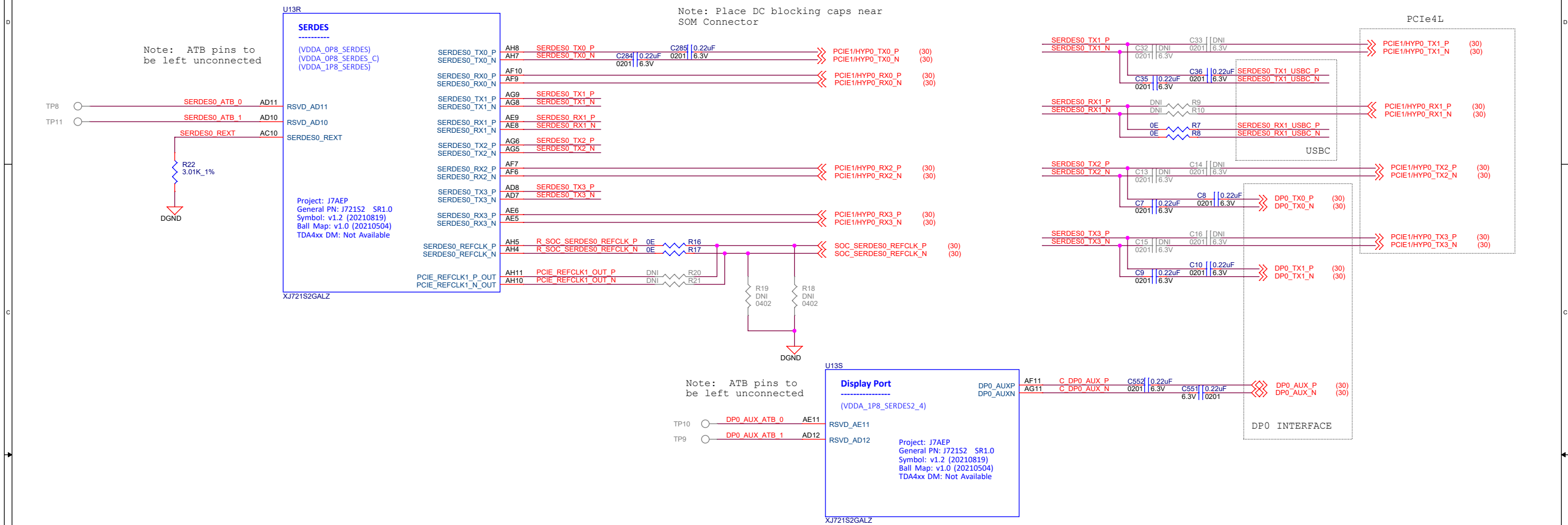
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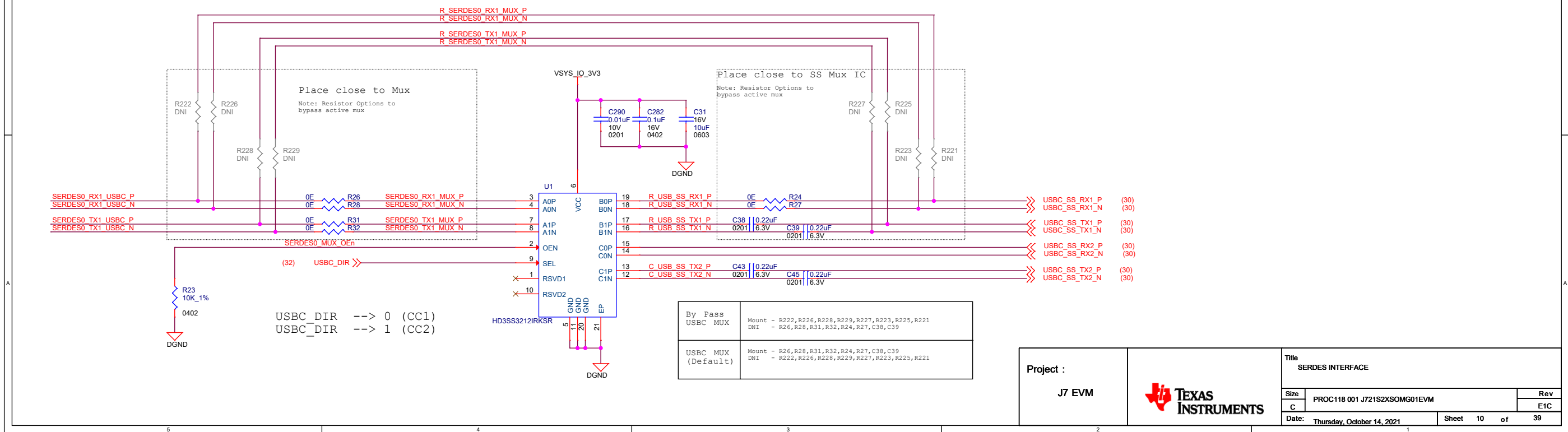
# CSI Interface



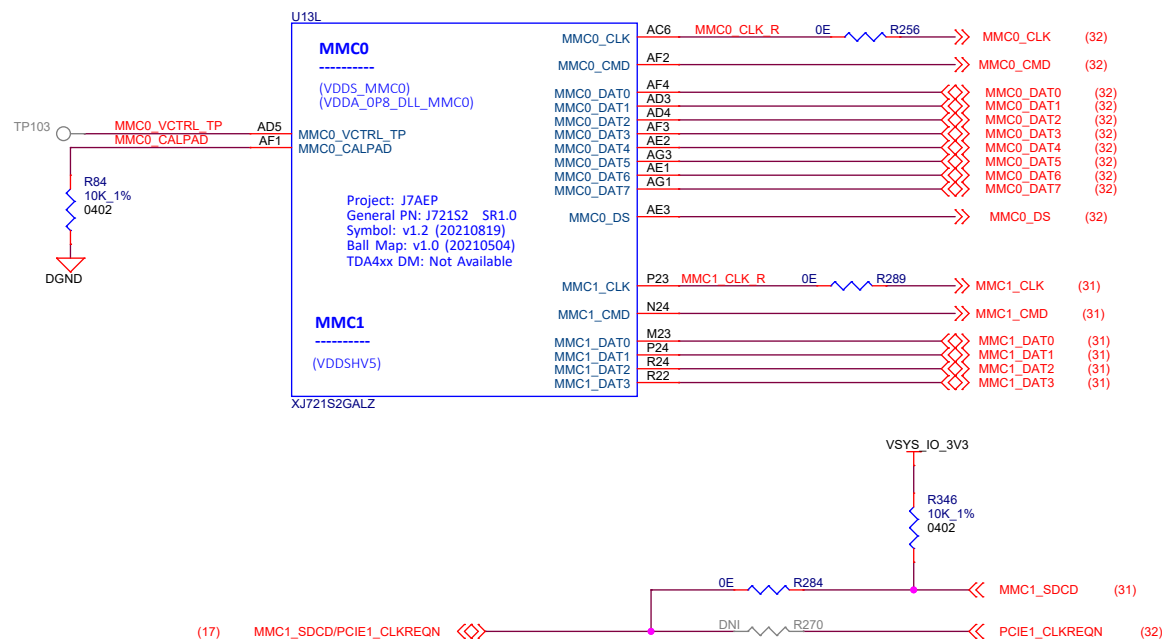
SERDES



USB Type C MUX



# MMC Interface

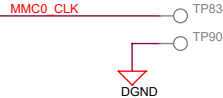


## Via Probe Test Points

Place Near SOC

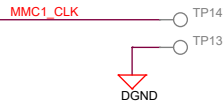
MMC0:

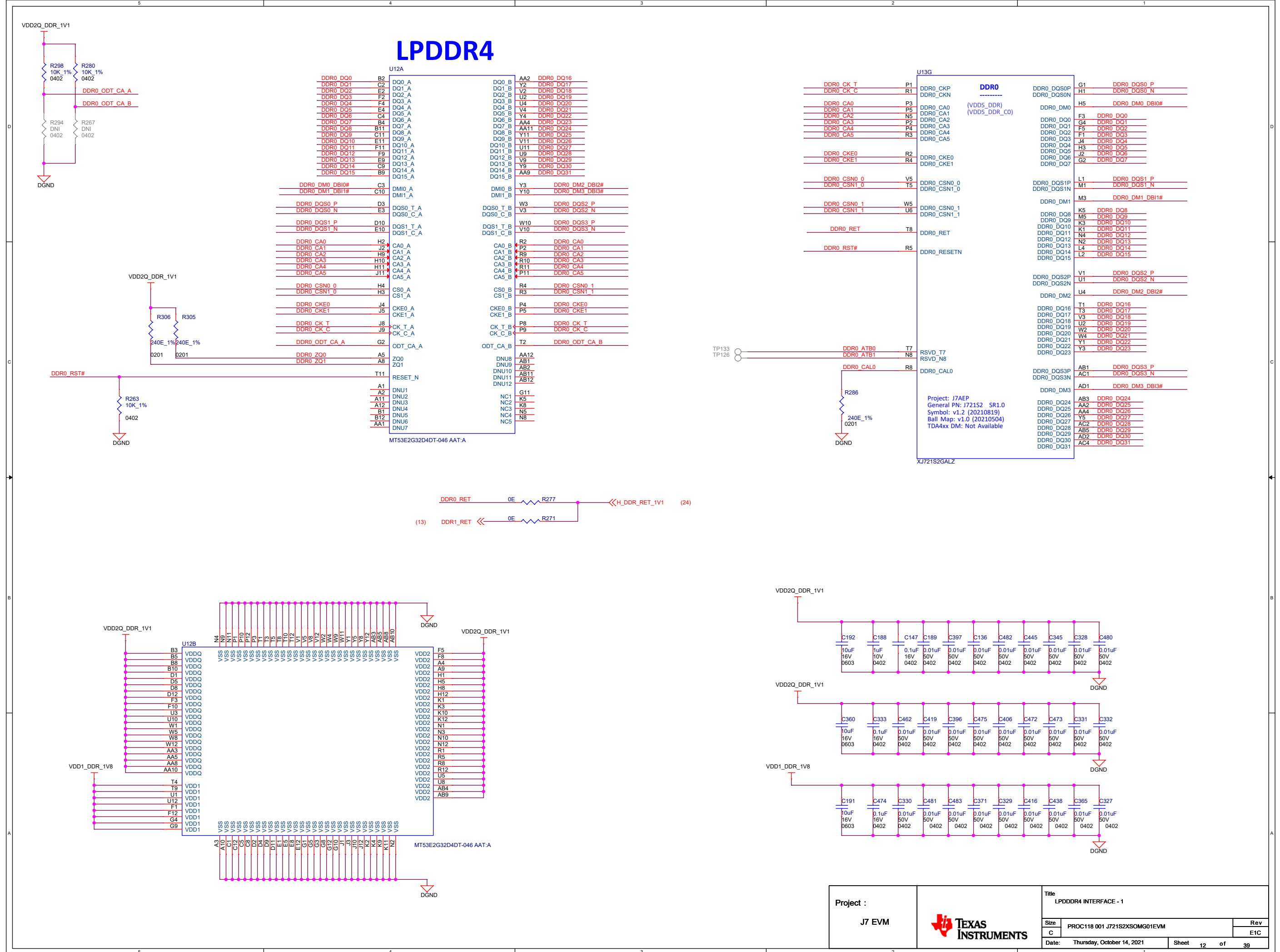
MMC0_CLK_R	DNI	TP107
MMC0_DAT0	DNI	TP79
MMC0_DAT1	DNI	TP77
MMC0_DAT2	DNI	TP71
MMC0_DAT3	DNI	TP60
MMC0_DAT4	DNI	TP70
MMC0_DAT5	DNI	TP76
MMC0_DAT6	DNI	TP80
MMC0_DAT7	DNI	TP81
MMC0_DS	DNI	TP84
MMC0_CMD	DNI	TP94



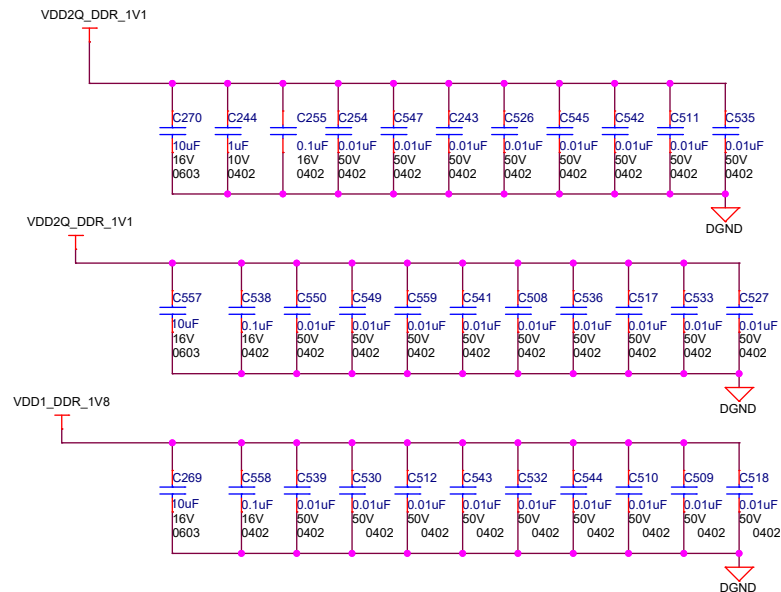
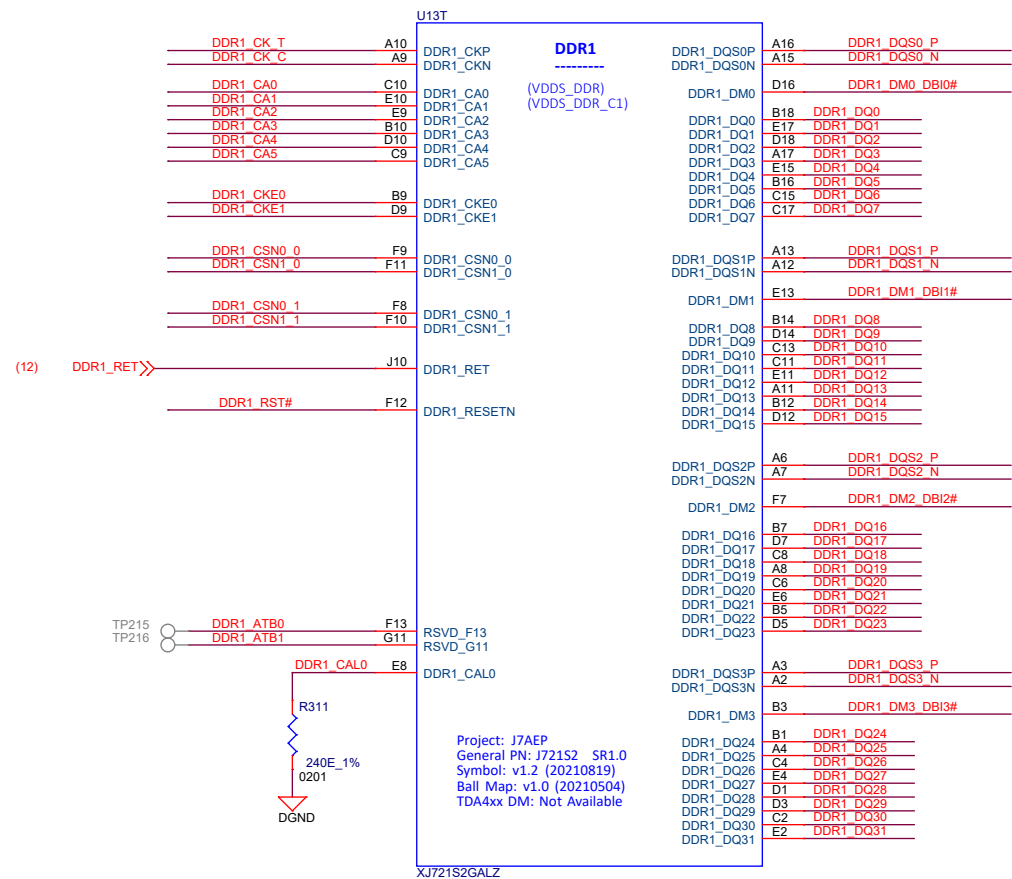
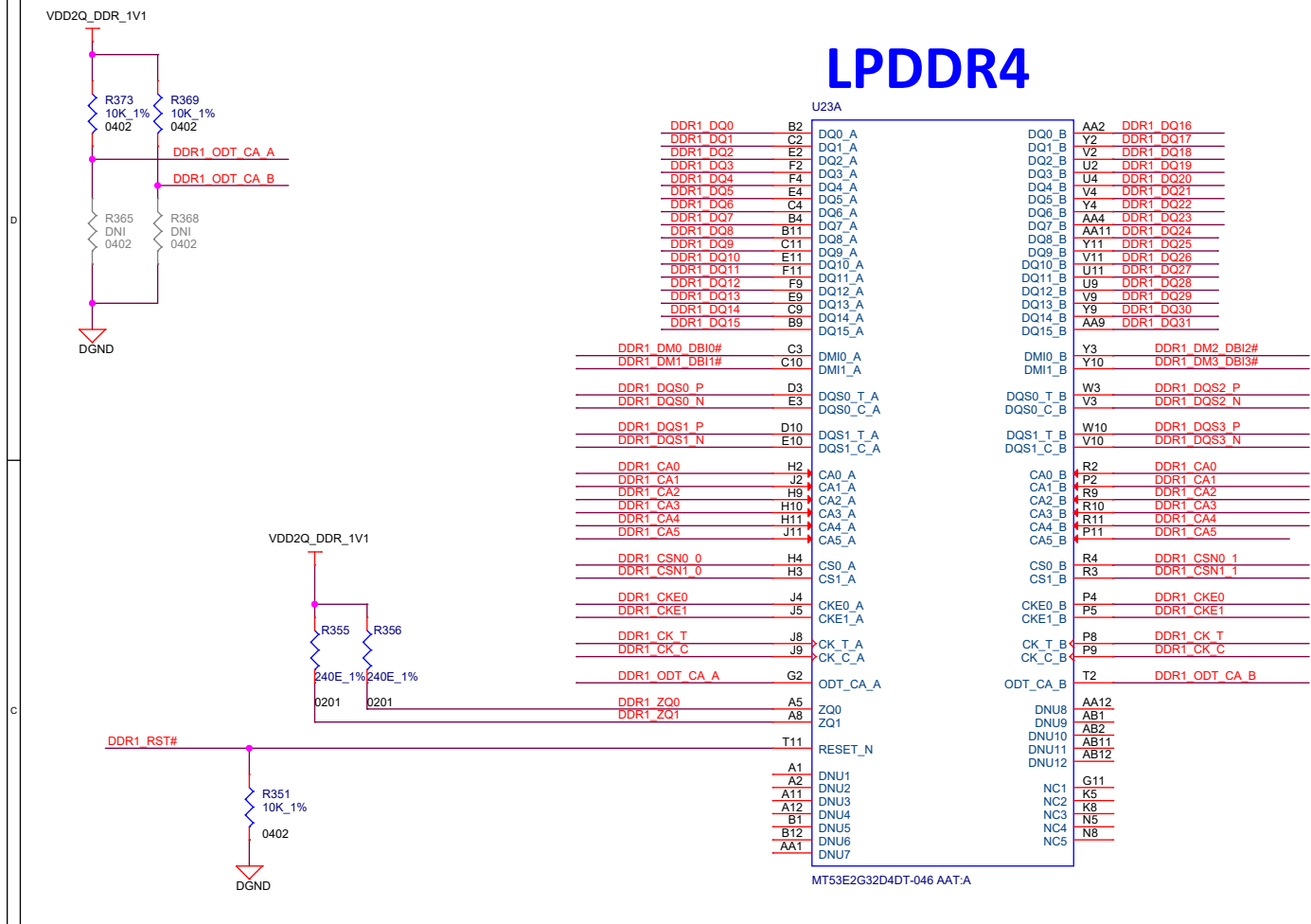
MMC1:

MMC1_CLK_R	DNI	TP169
MMC1_DAT0	DNI	TP129
MMC1_DAT1	DNI	TP140
MMC1_DAT2	DNI	TP139
MMC1_DAT3	DNI	TP138
MMC1_CMD	DNI	TP148





# LPDDR4

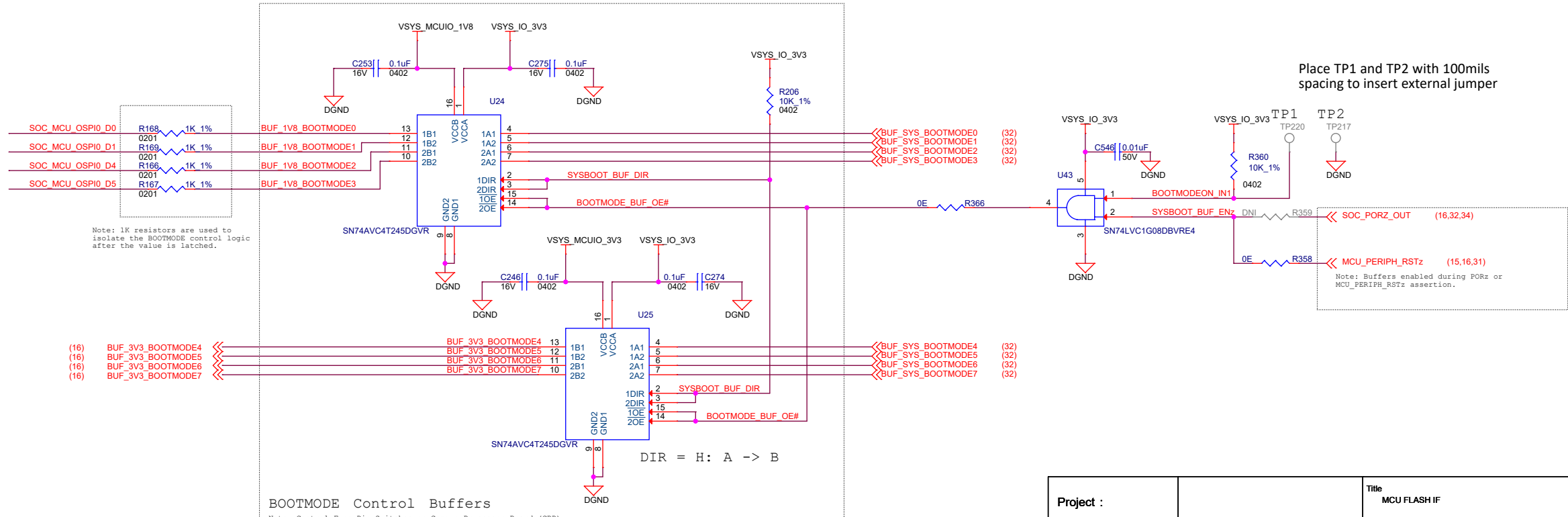
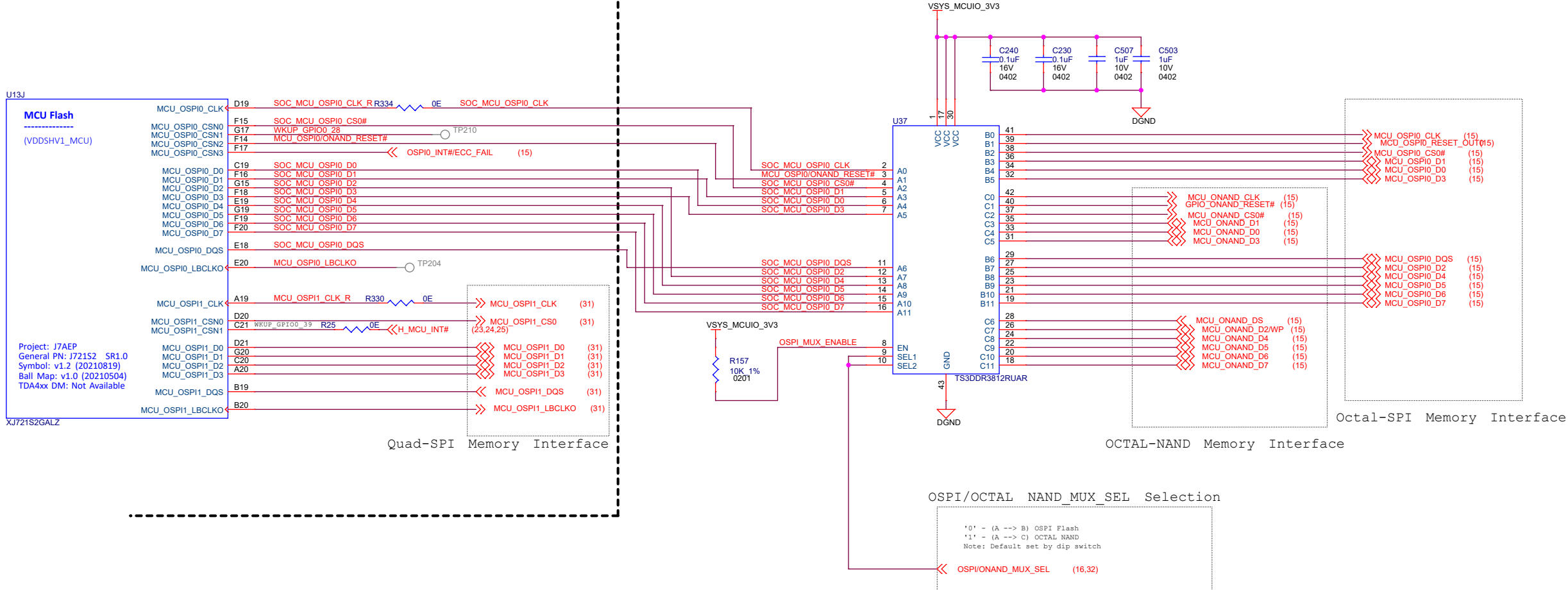




## EVM development & evaluation test circuitry (TI EVM Only)

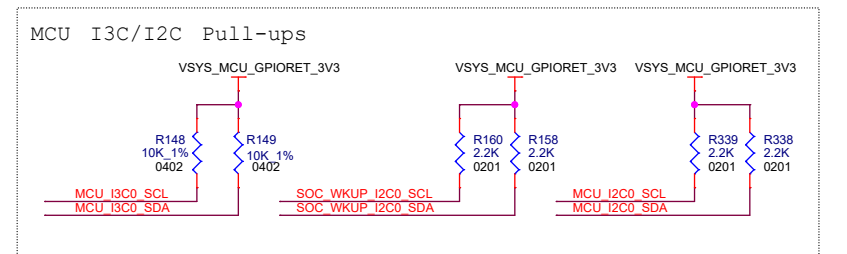
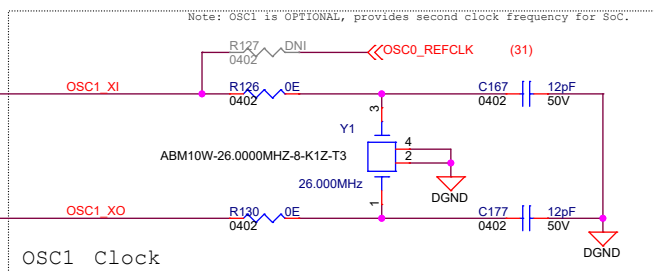
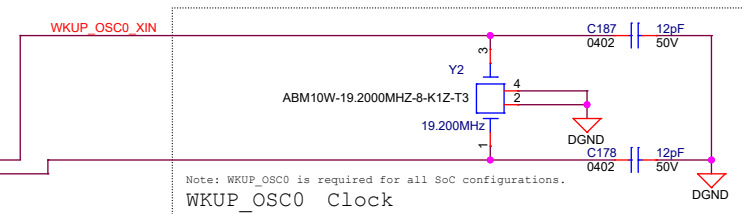
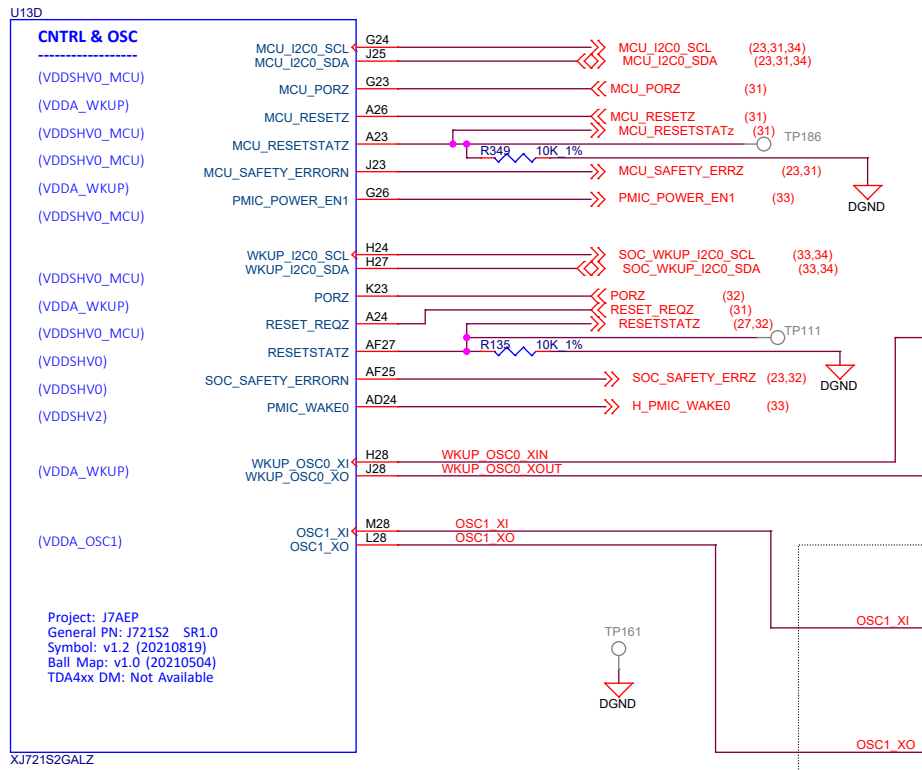
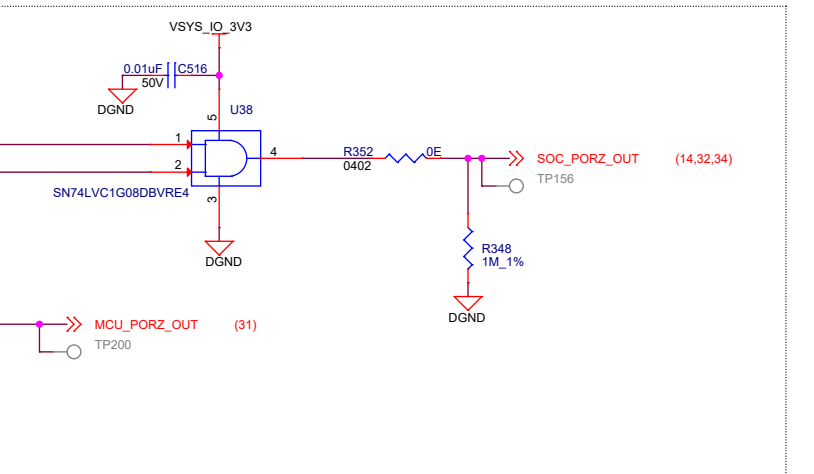
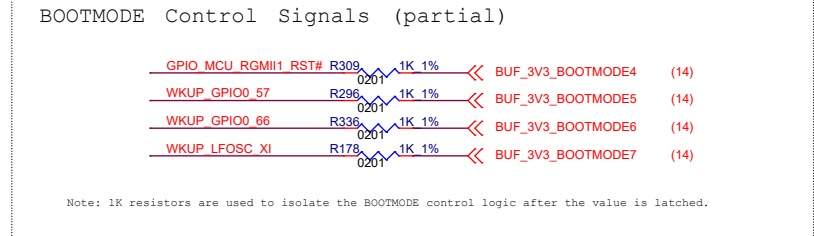
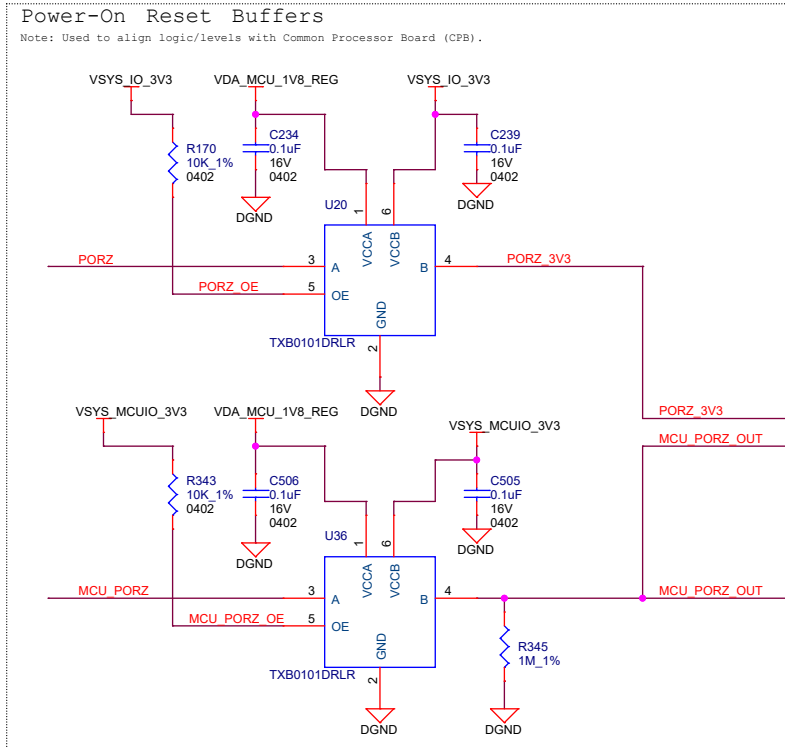
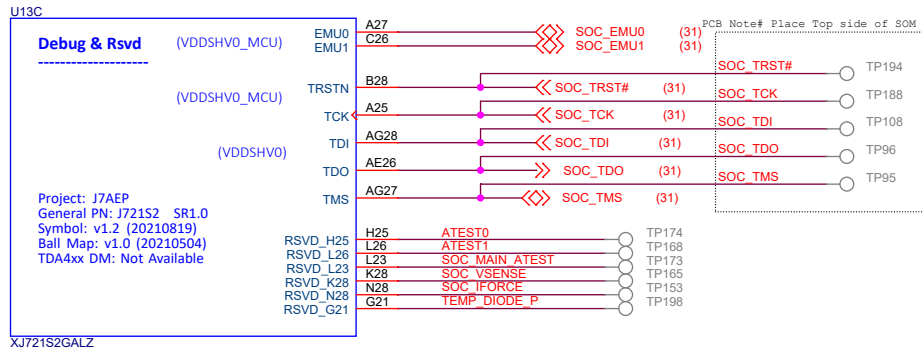
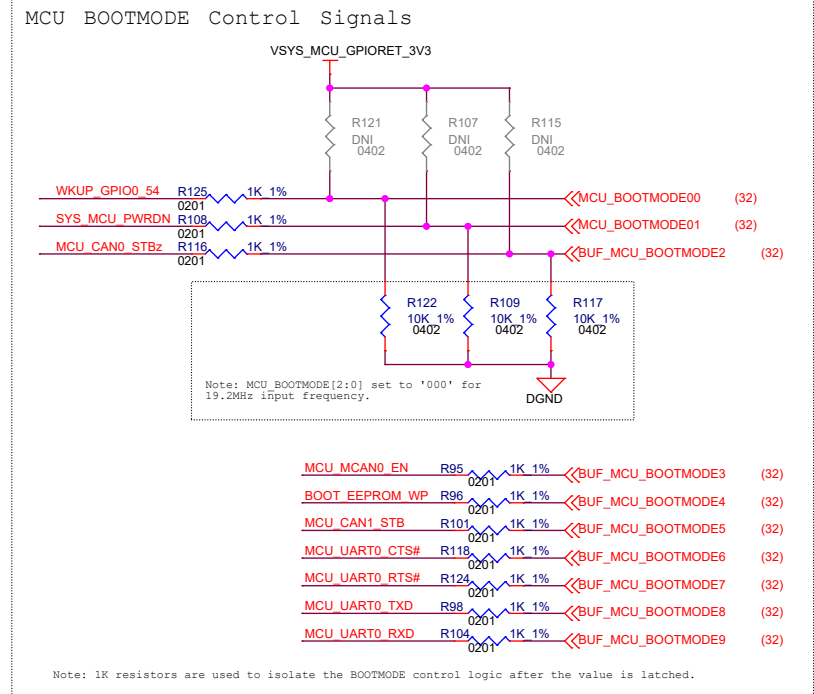
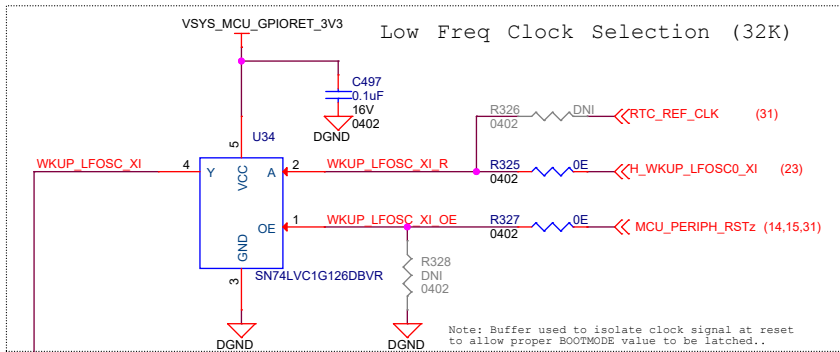
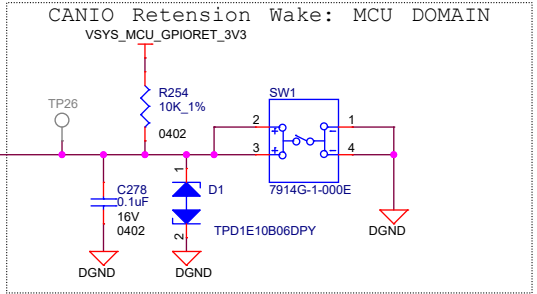
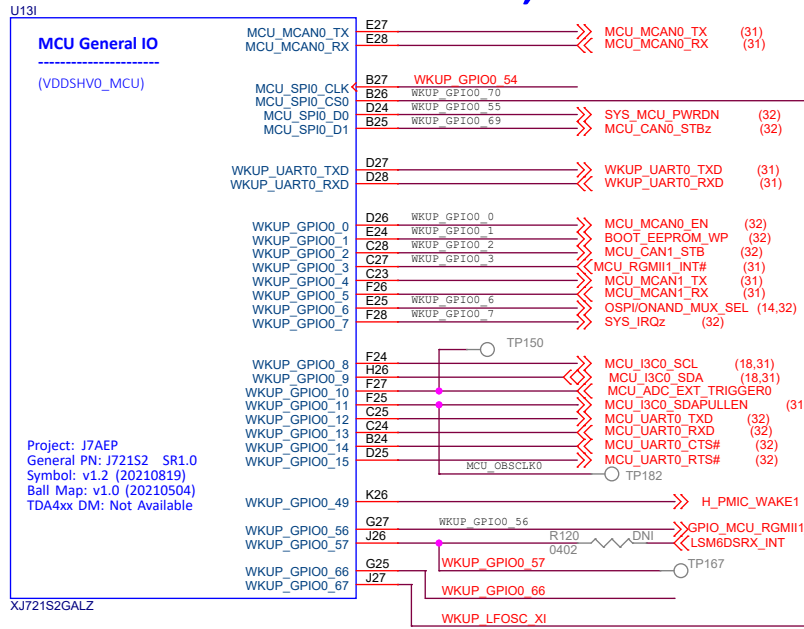
## 2:1 Mux for OSPI/OCTAL NAND

# MCU FLASH

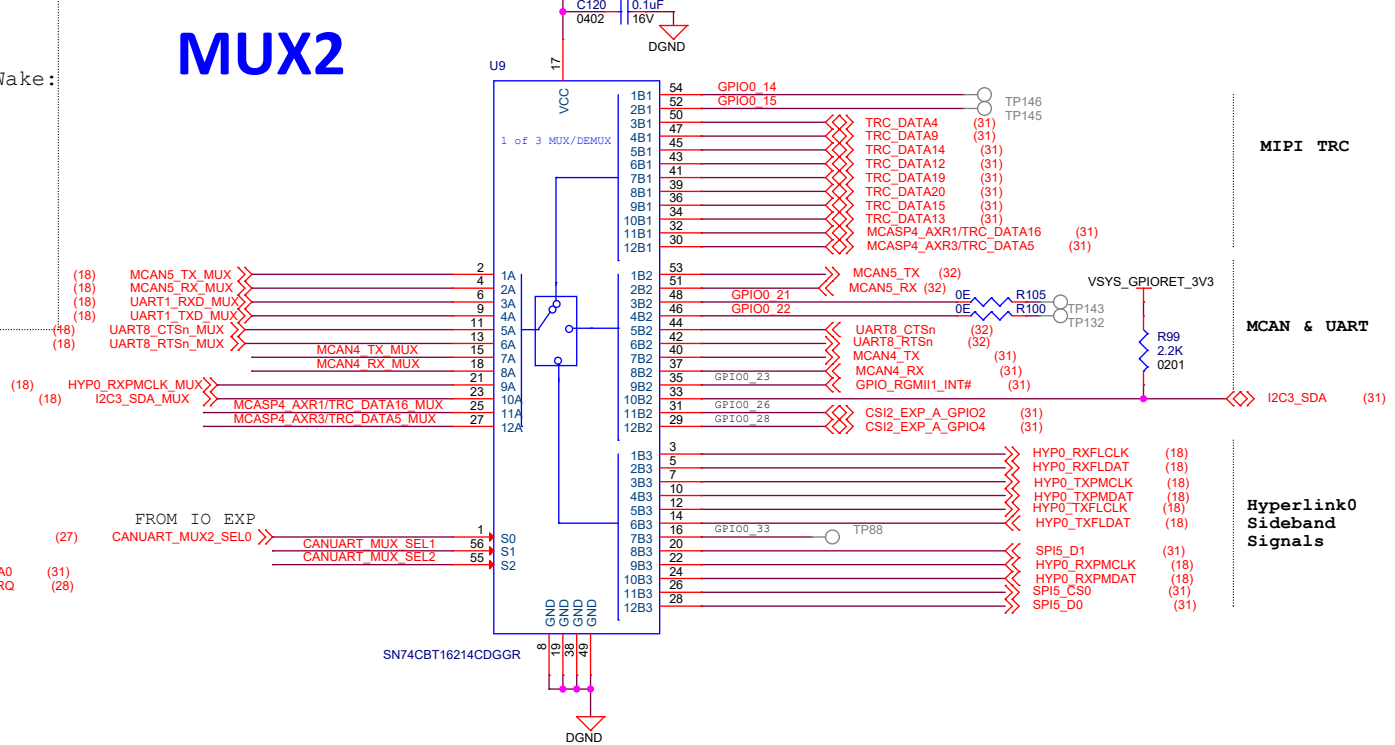
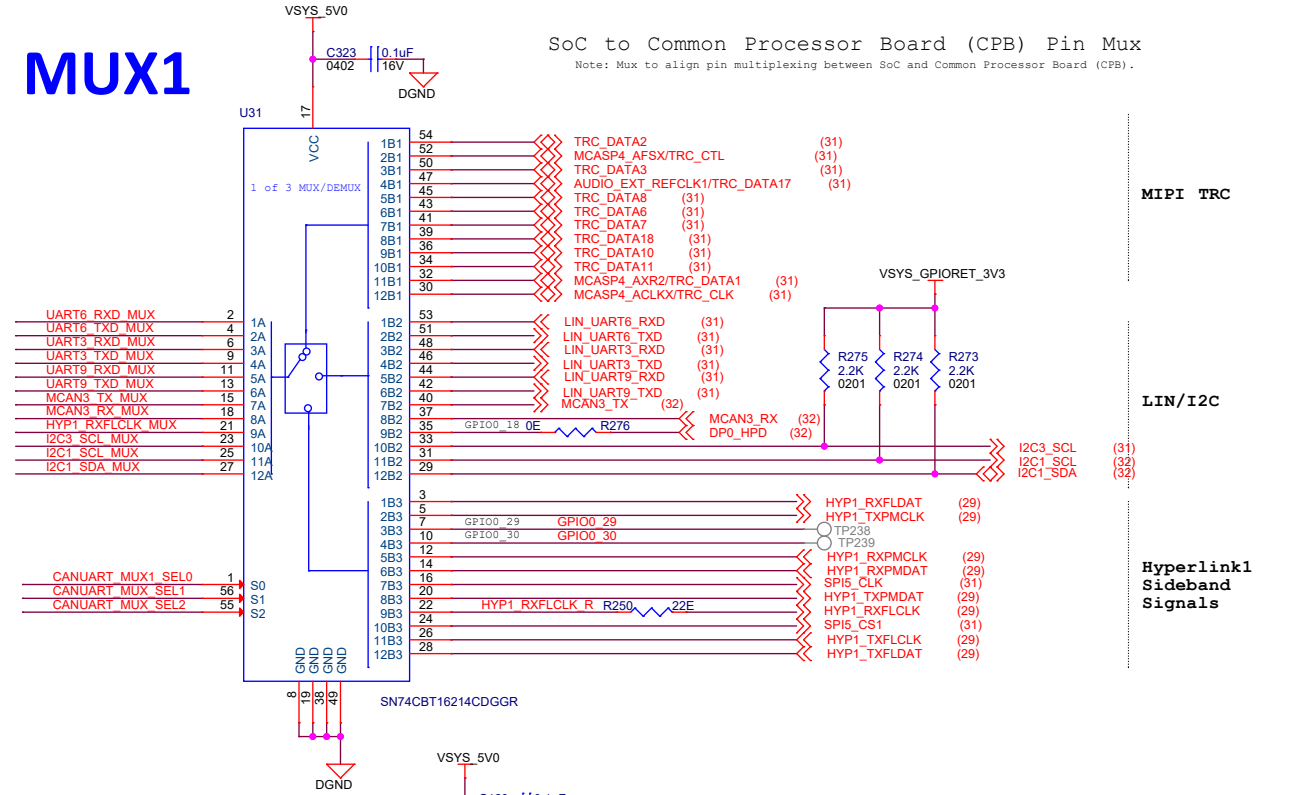
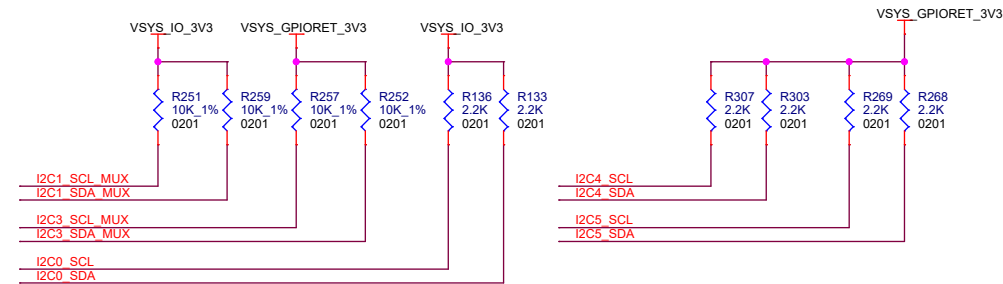
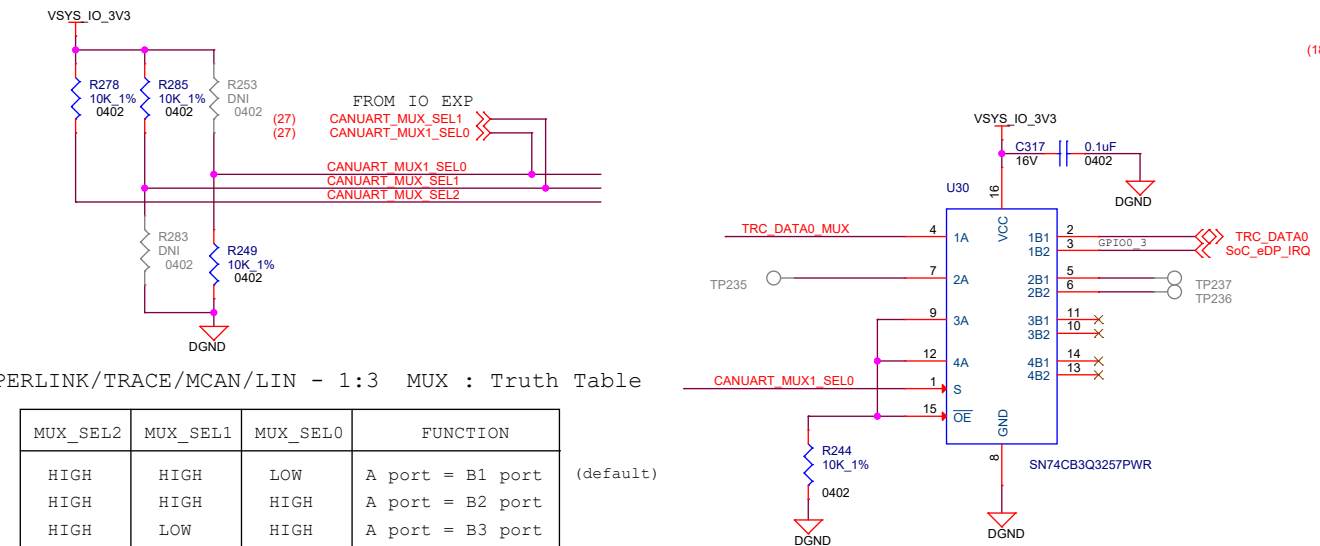
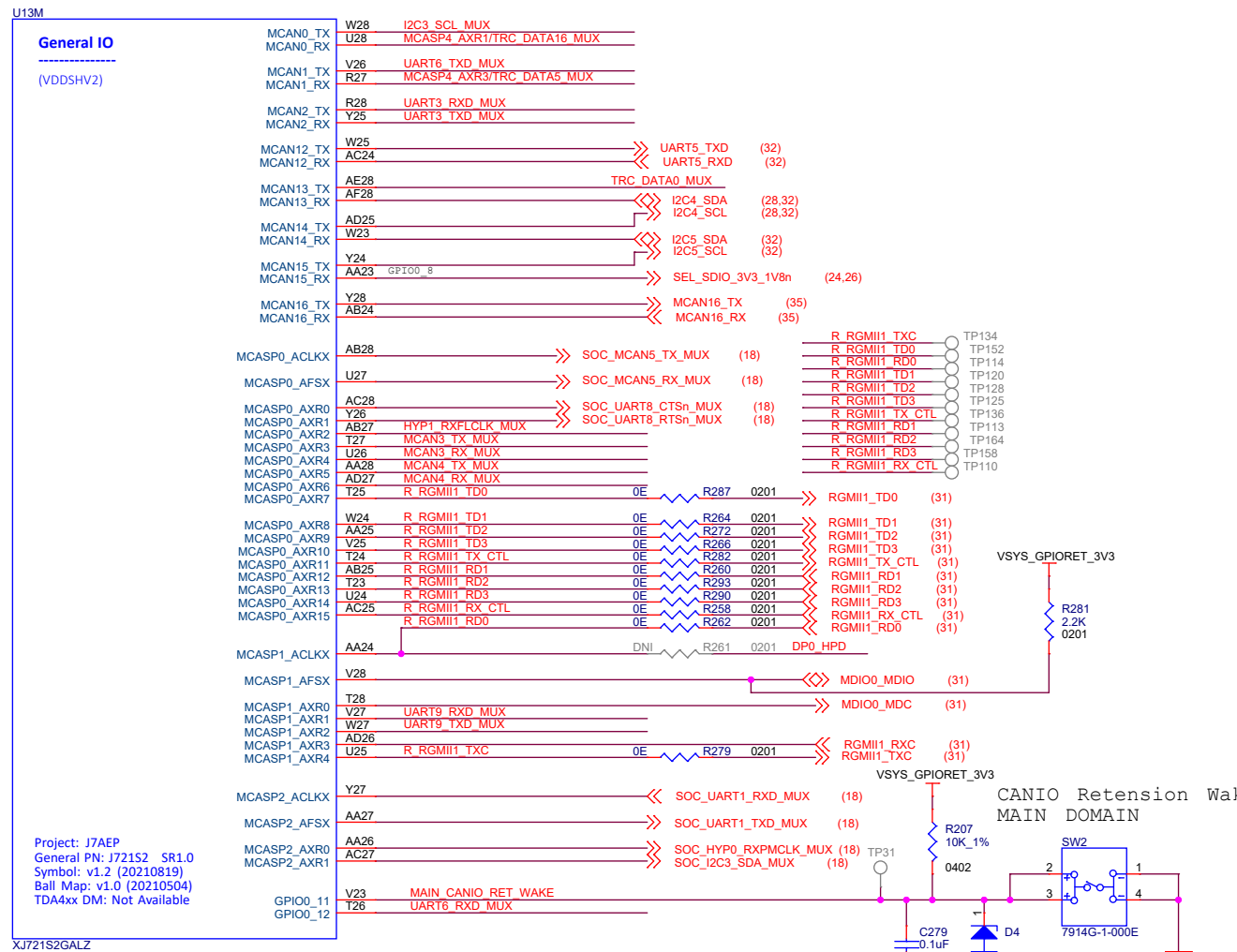
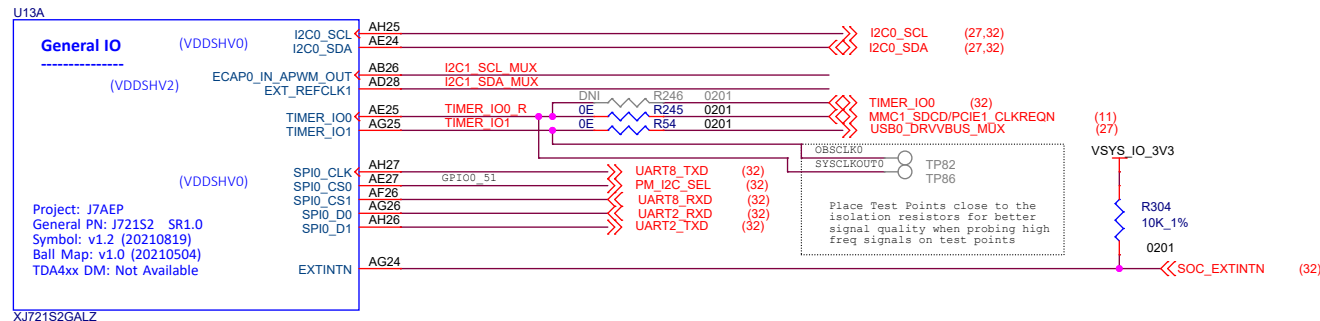




## MCU & MAIN GENERAL IO, OSC CLKS



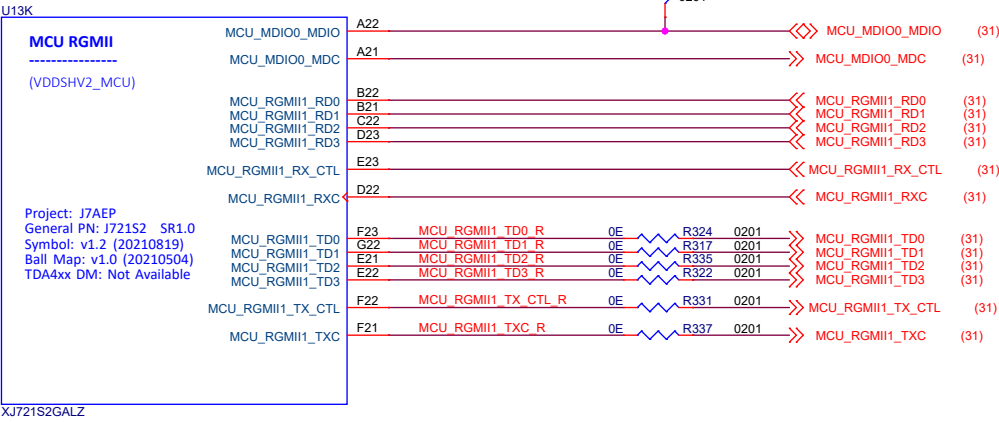
## GENERAL IO



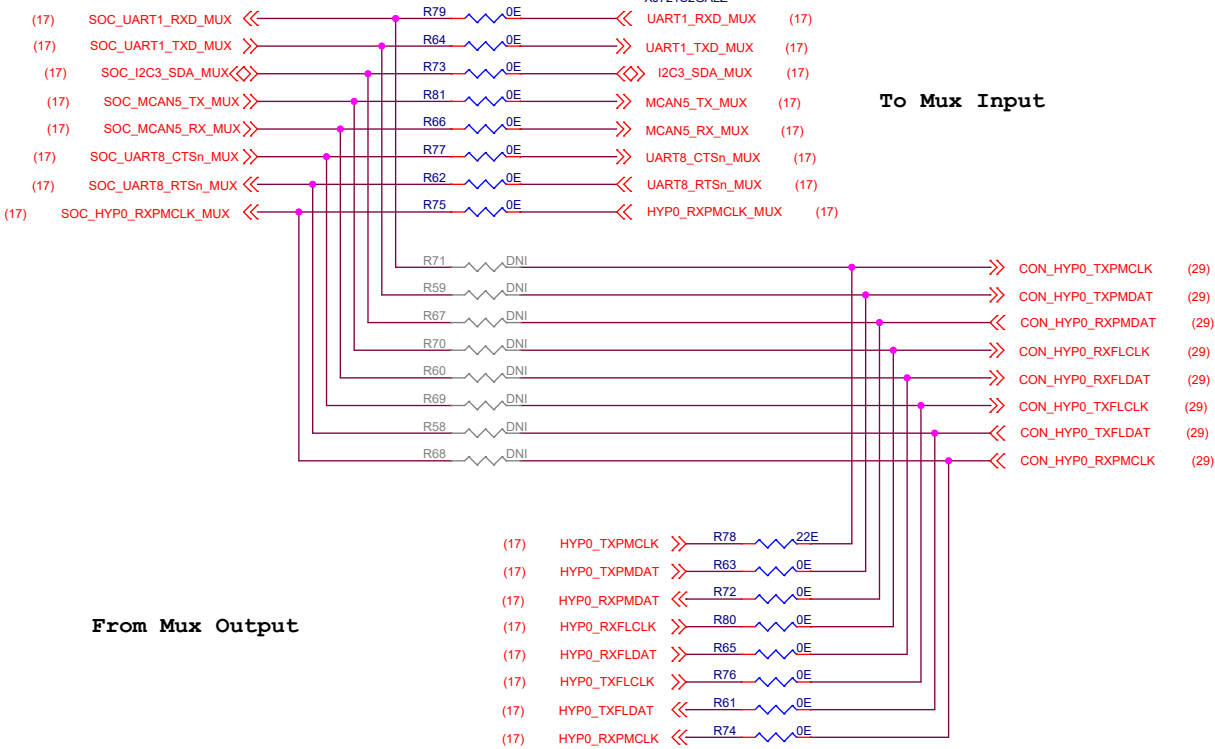
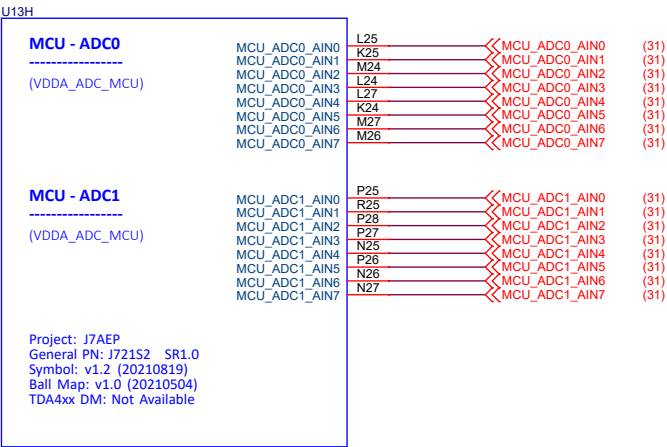
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port

(default)

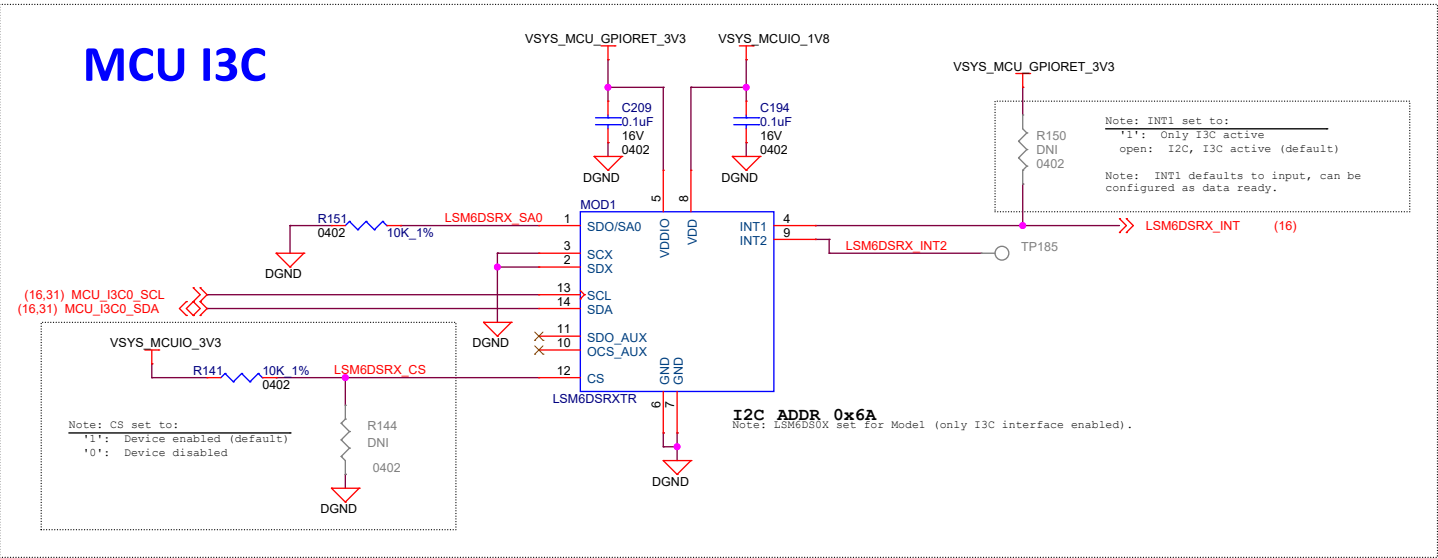
MCU\_RGMII



MCU ADCs

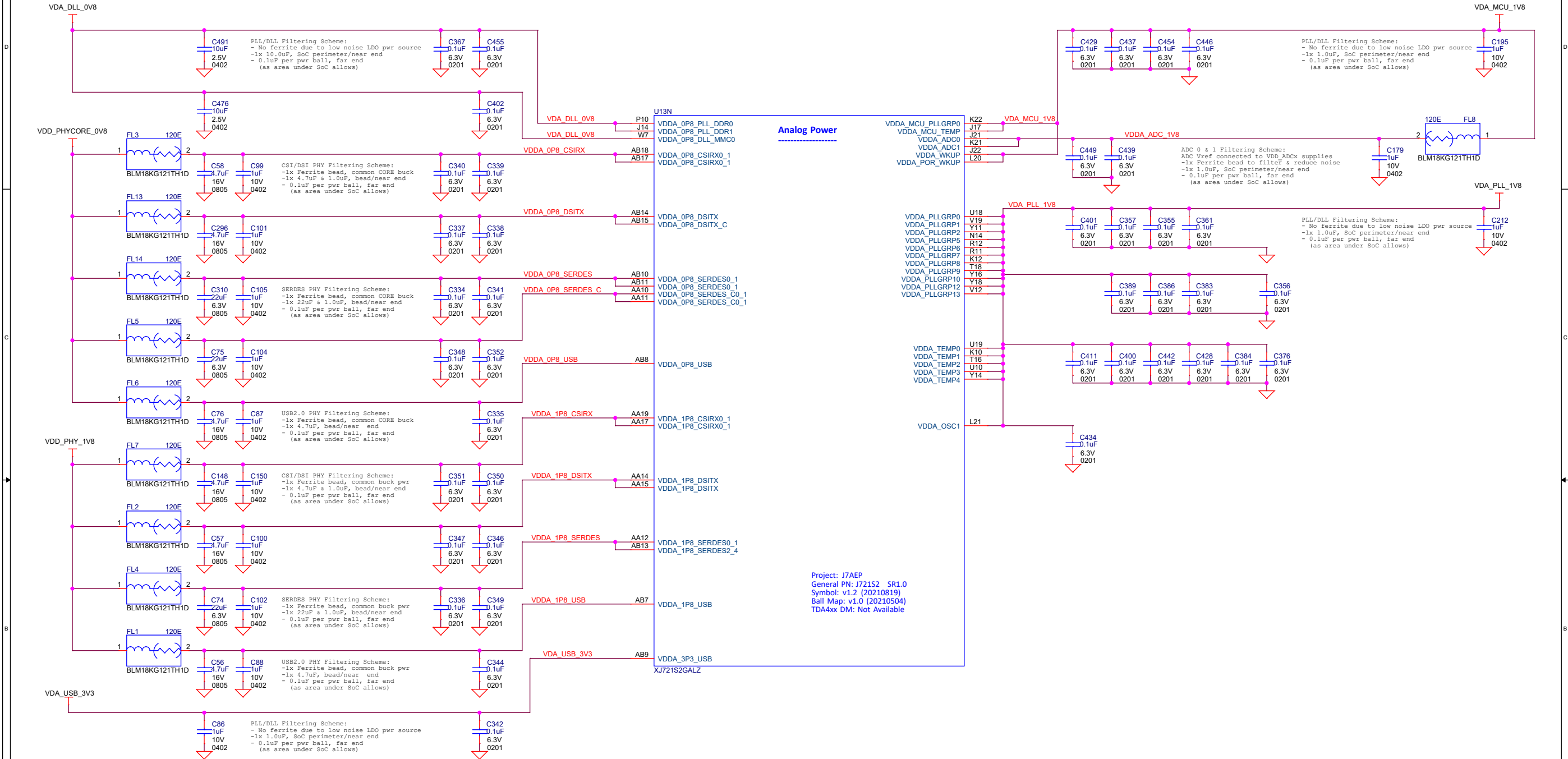


To Hyperlink Side band Conn





ANALOG POWER 1



Project :

J7 EVM



Title  
SOC ANALOG POWER 1

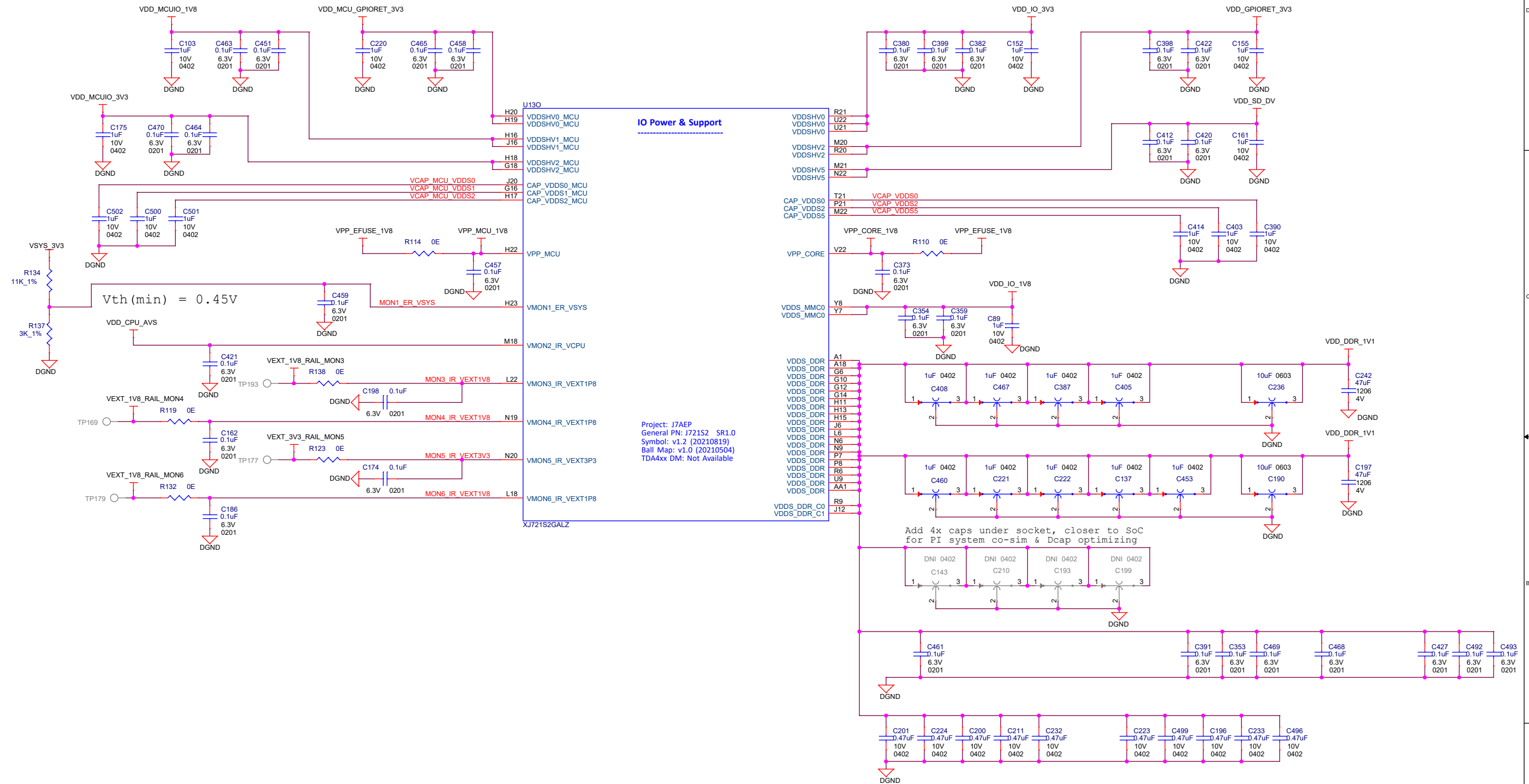
Size  
C PROC118 001 J721S2XSOMG01EVM

Date: Thursday, October 14, 2021

Sheet 19 of 39

Rev  
ETC

## Voltage Monitors & IO POWER 2



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project :

## J7 EVM



**Title**  
**SOC DIGITAL IO & SUPPORT POWER 2**

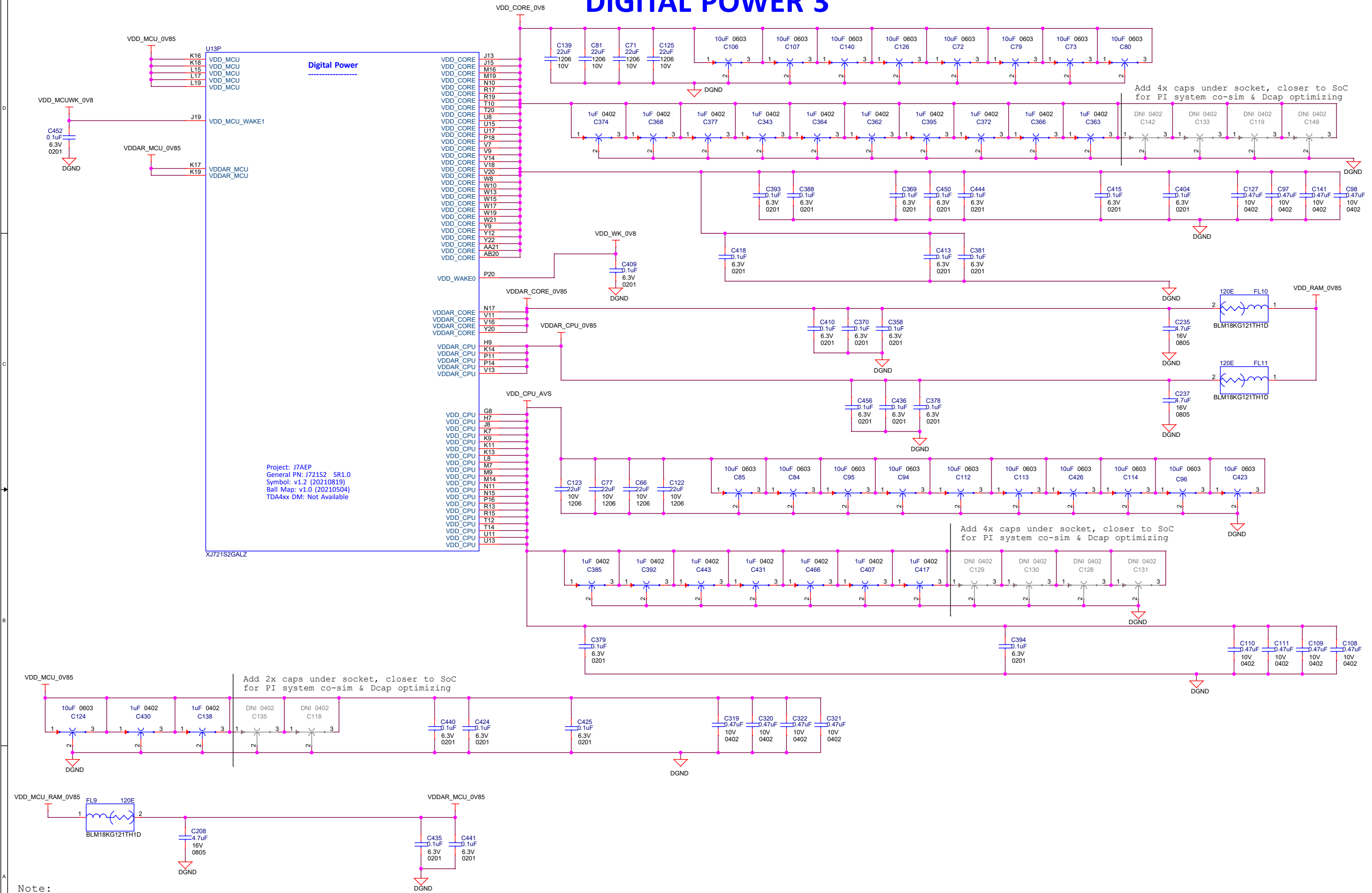
Size	DROC118.001_U72162XSOMC01EVM
------	------------------------------

C	
Date:	

	Rev
--	-----

	E1C
Sheet 1	

# DIGITAL POWER 3



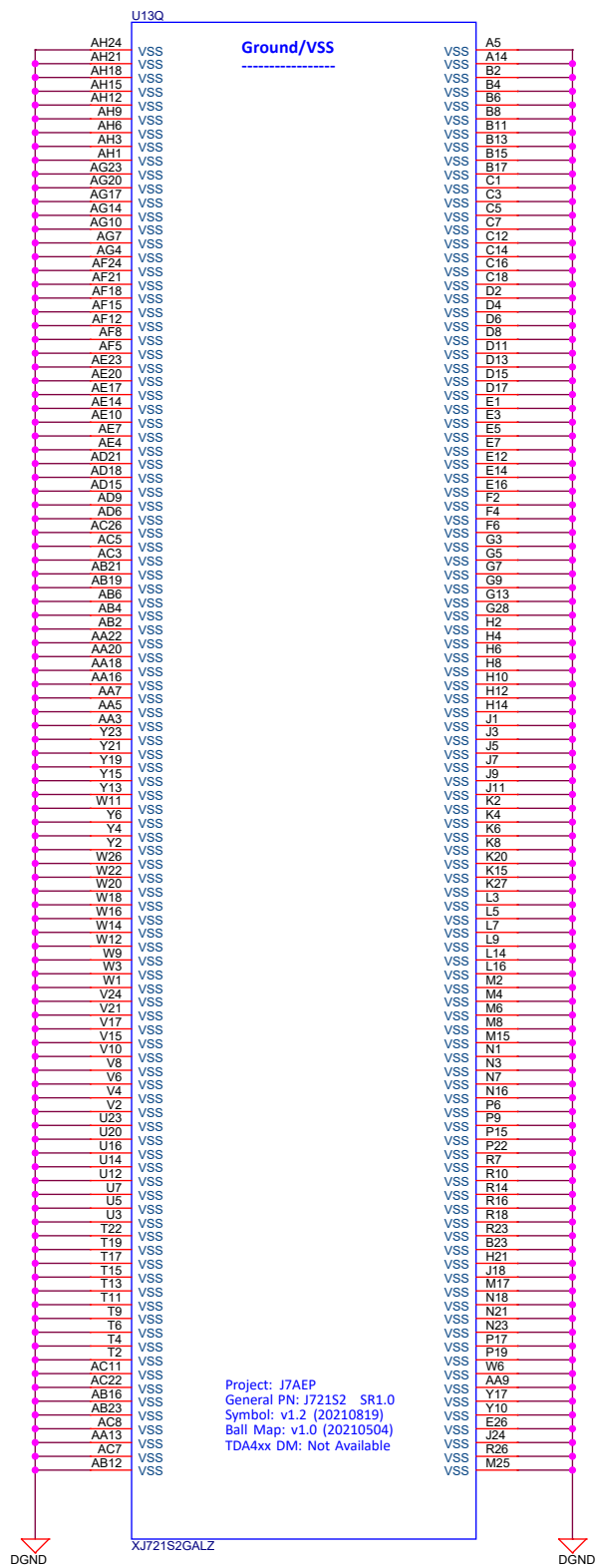
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance ( $Z_t$ ).

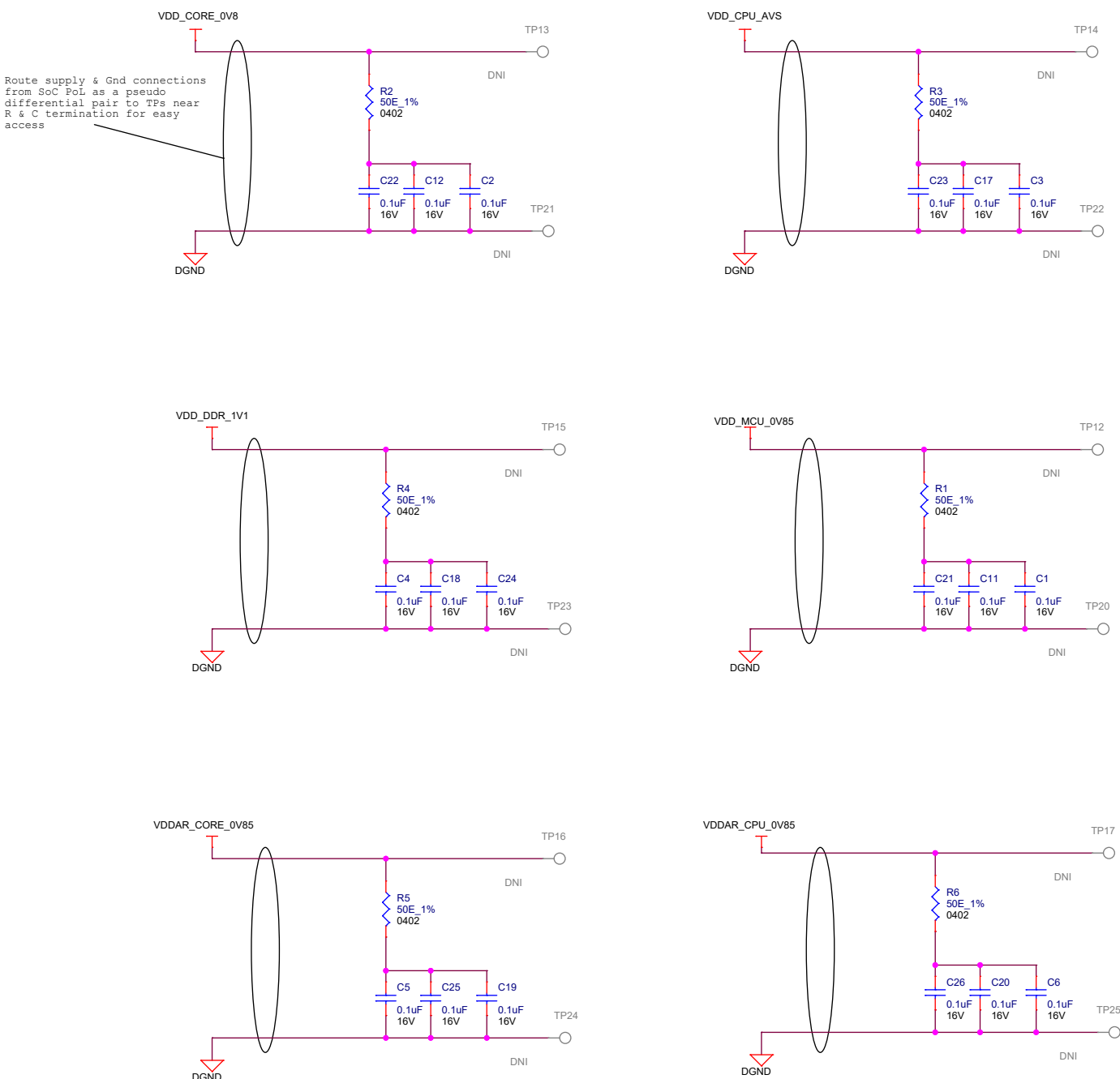
Project :  J7 EVM		Title SOC DIGITAL POWER 3	
		Size C	Rev ETC
		PROC118 001 J721S2XSOMG01EVM	
		Date: Thursday, October 14, 2021	Sheet 21 of 39

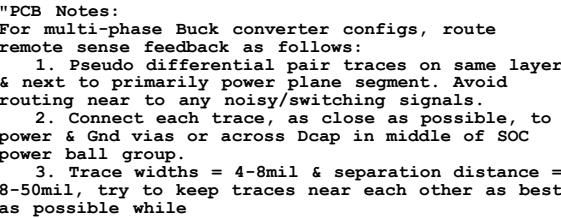
SOC GROUND



Project: J7AEP  
General PN: J721S2 SR1.0  
Symbol: v1.2 (20210819)  
Ball Map: v1.0 (20210504)  
TDA4xx DM: Not Available

SoC Supply Noise Kelvin Sensing






For single-phase Buck converters, route remote sense feedback as follows:

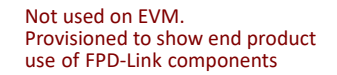
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

Route as Pseudo differential pair trace  
(See "PCB Notes")

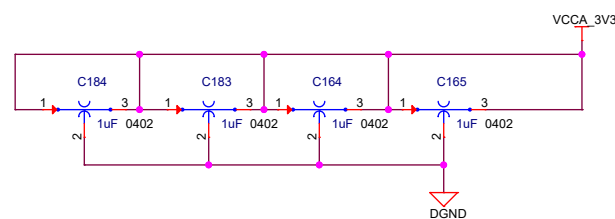
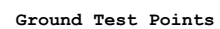
Project :  J7 EVM		Title POWER SUPPLY 1			
		Size	PROC118 001 J721S2XSOMG01EVM		Rev
		C			E1C
		Date:	Thursday, October 14, 2021	Sheet	23 of 39




Route as single-ended sense traces  
(See "PCB Notes")

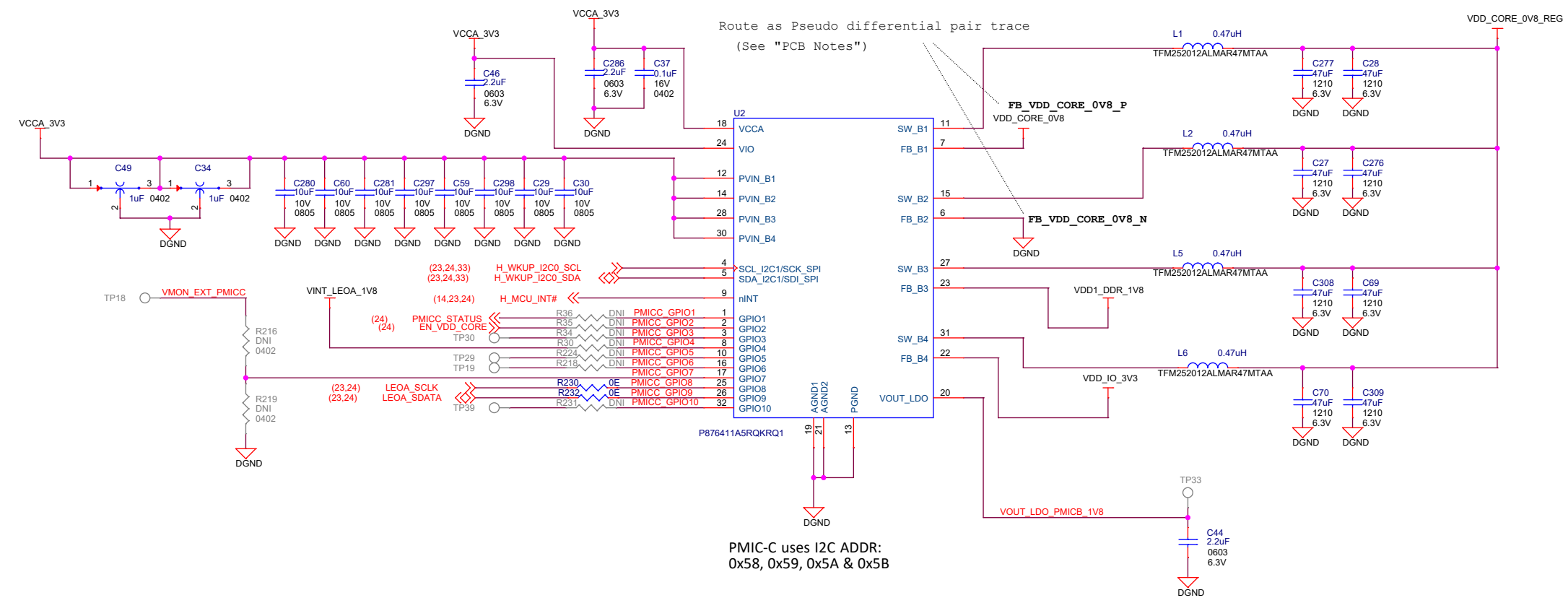


Power Test Point

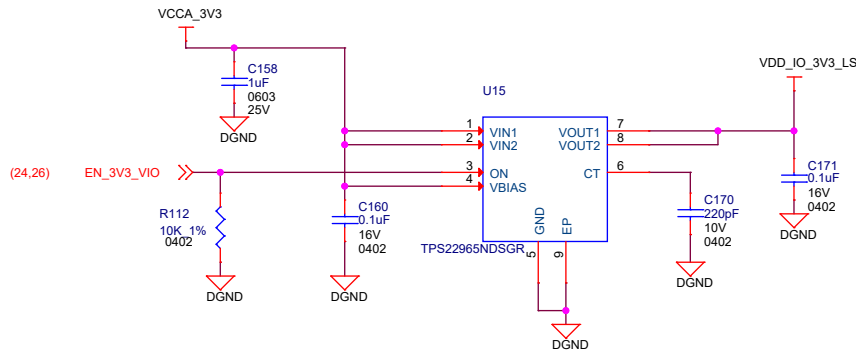
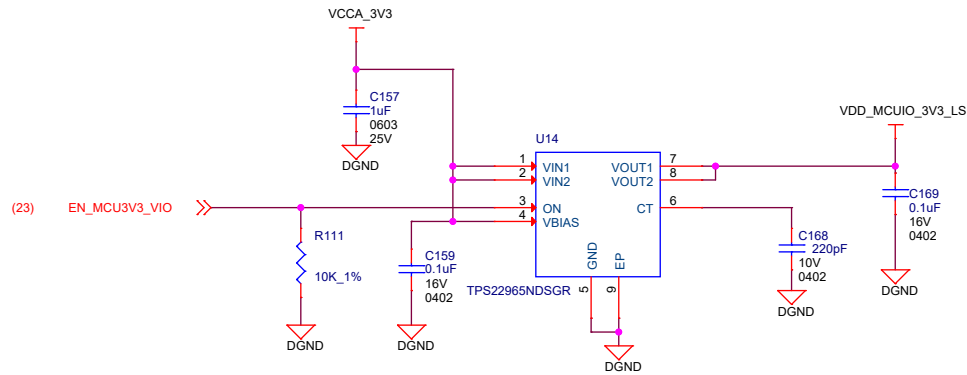


Project :  J7 EVM		Title POWER SUPPLY 2		
		Size	PROC118 001 J721S2XSOMG01EVM	Rev
		C		E1C
		Date: Thursday, October 14, 2021	Sheet 24 of 39	

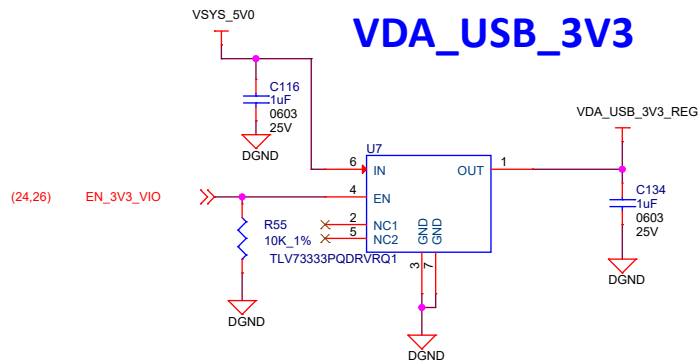
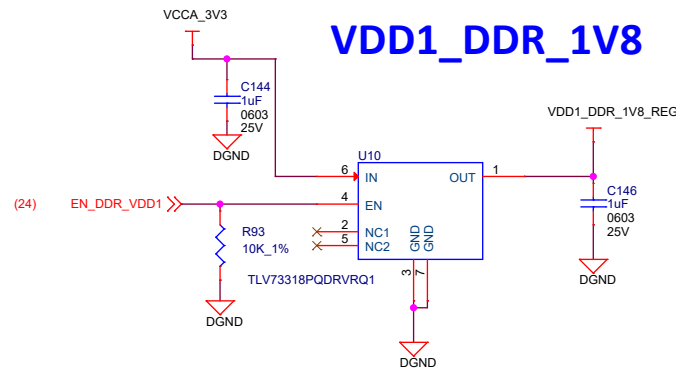
High-Current Power Stage (HCPS)



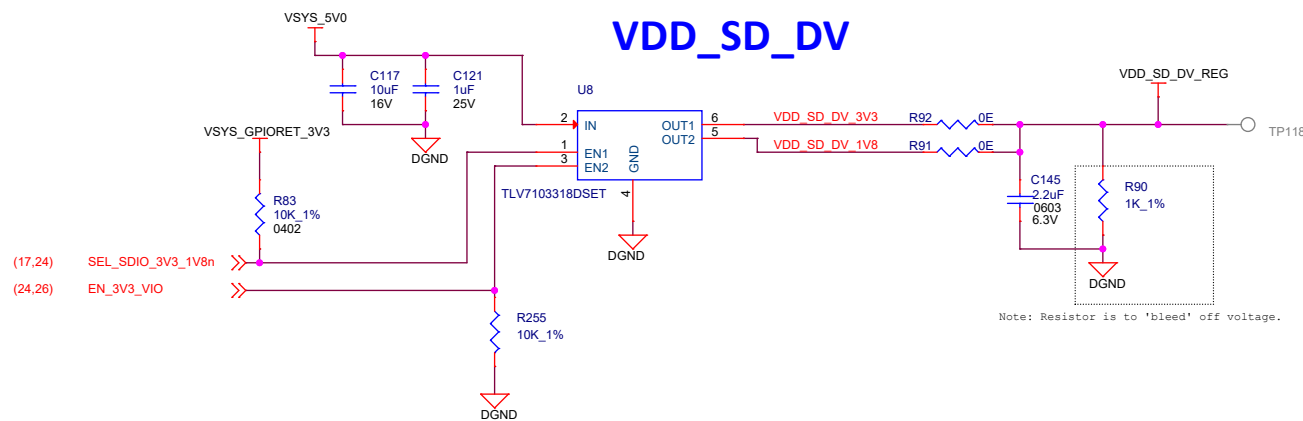
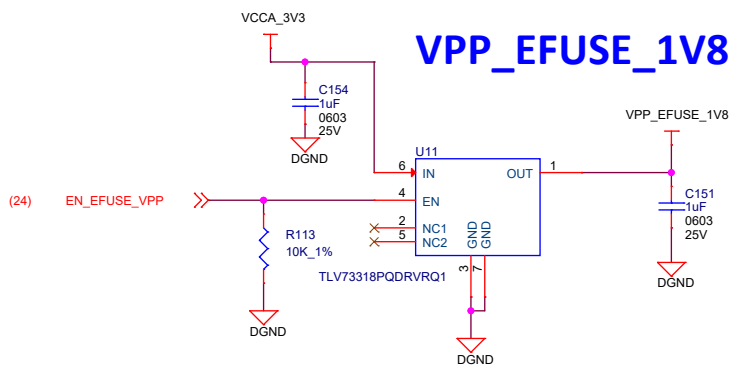
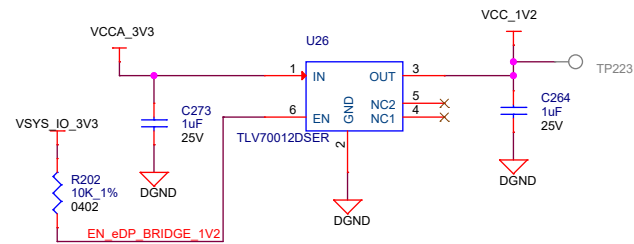
# LOAD SWITCHES



# LDOs

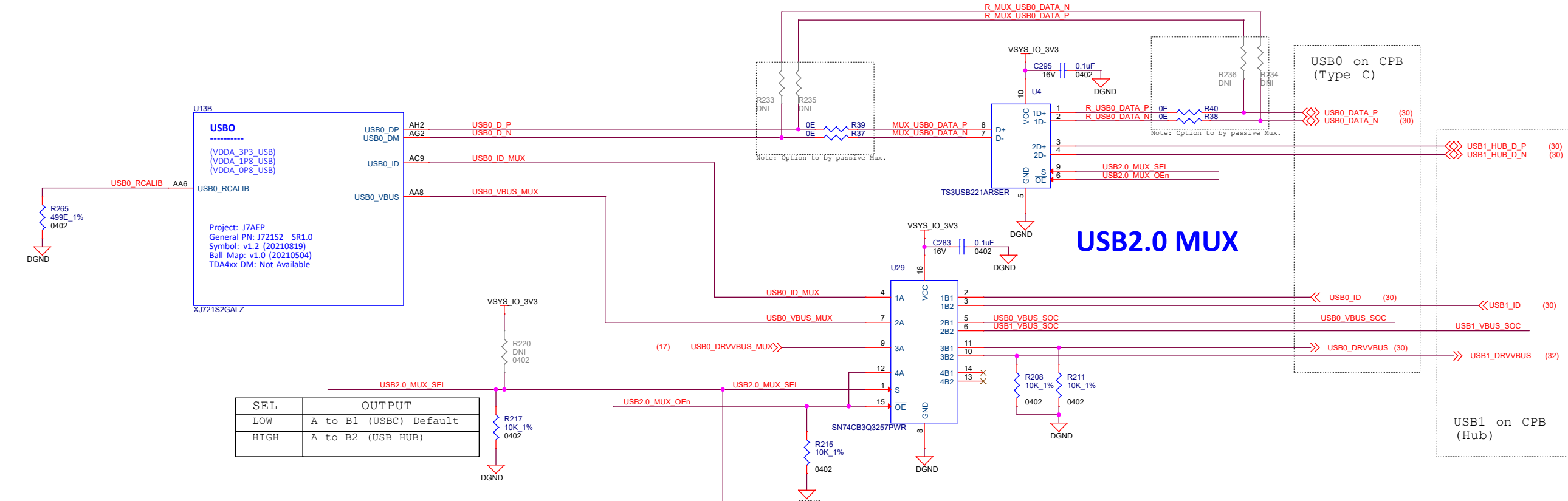


# VCC\_1V2 - eDP Bridge

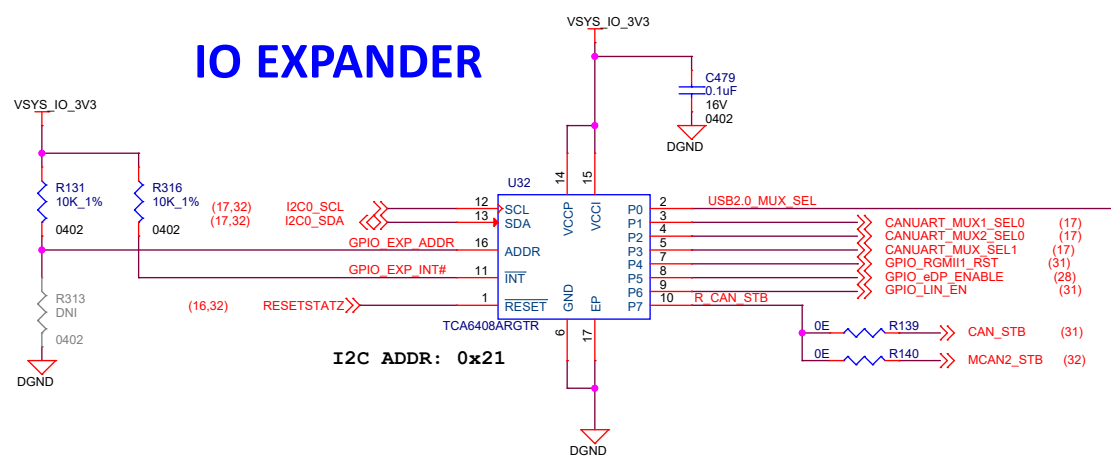


USB

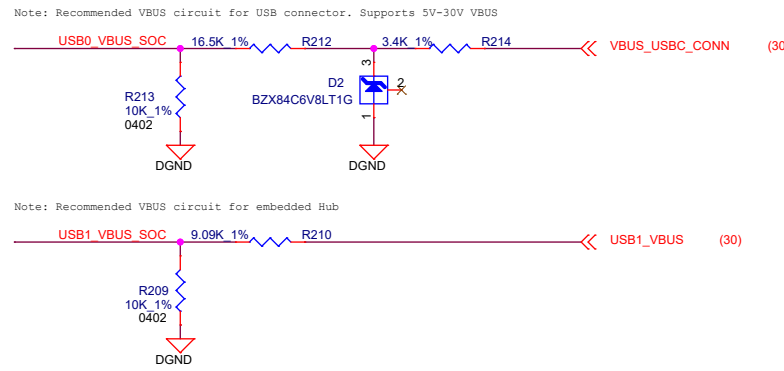
By Pass USB MUX	Mount - R233,R235,R236,R234 DNI - R39,R37,R40,R38
USB MUX (Default)	Mount - R39,R37,R40,R38 DNI - R233,R235,R236,R234



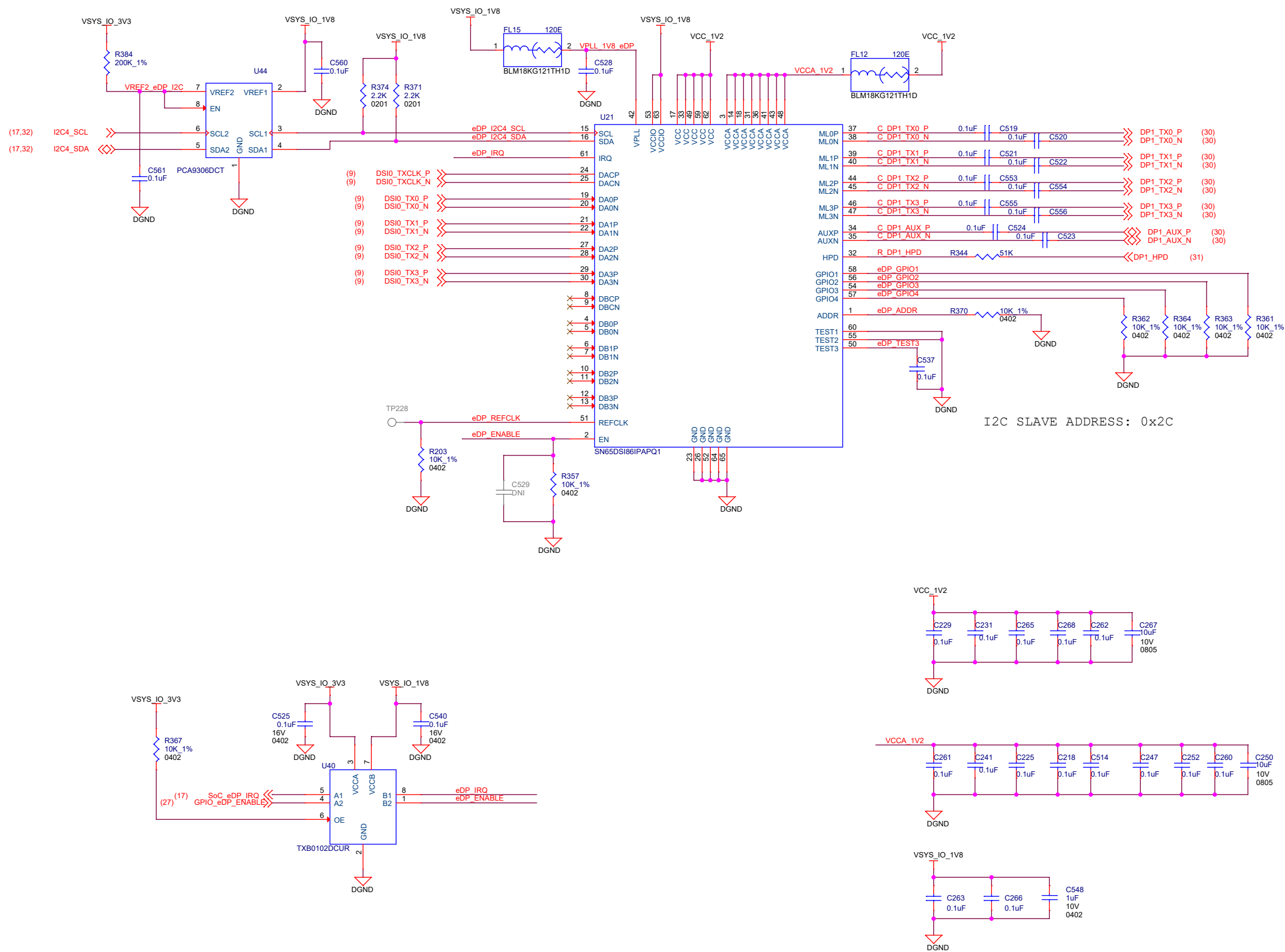
IO EXPANDER



USB VBUS Resistor divider circuit

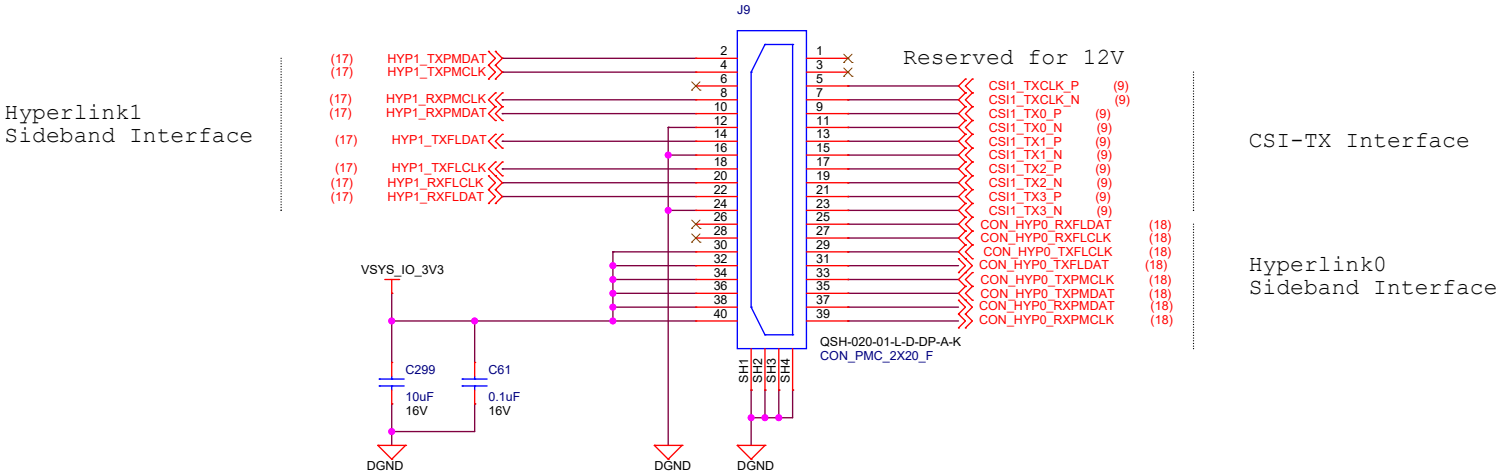


DSI to eDP BRIDGE

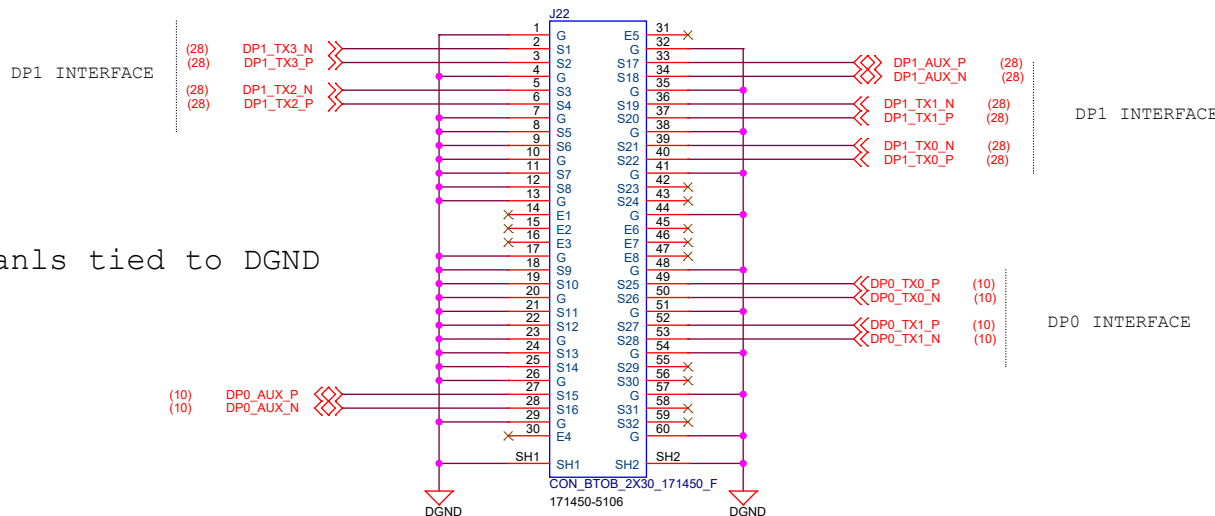
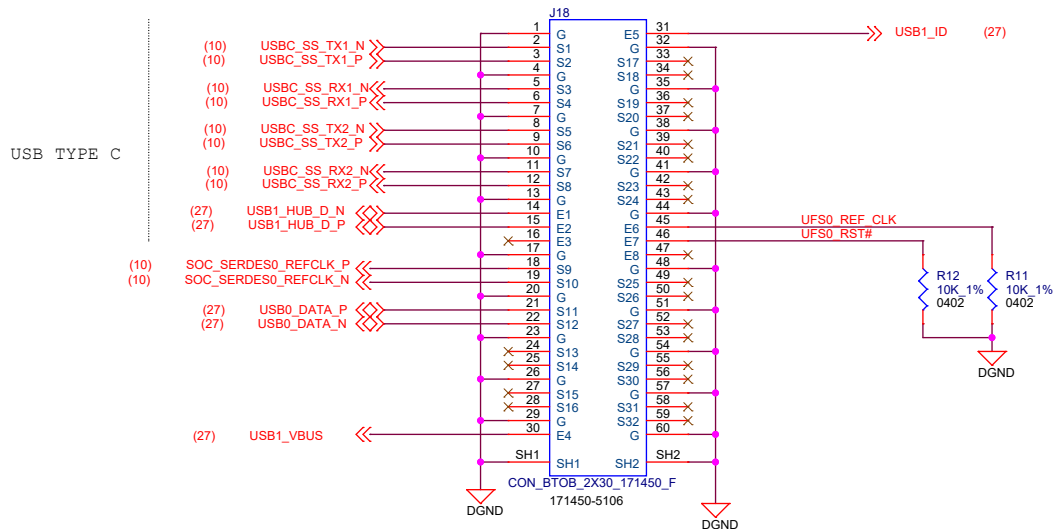
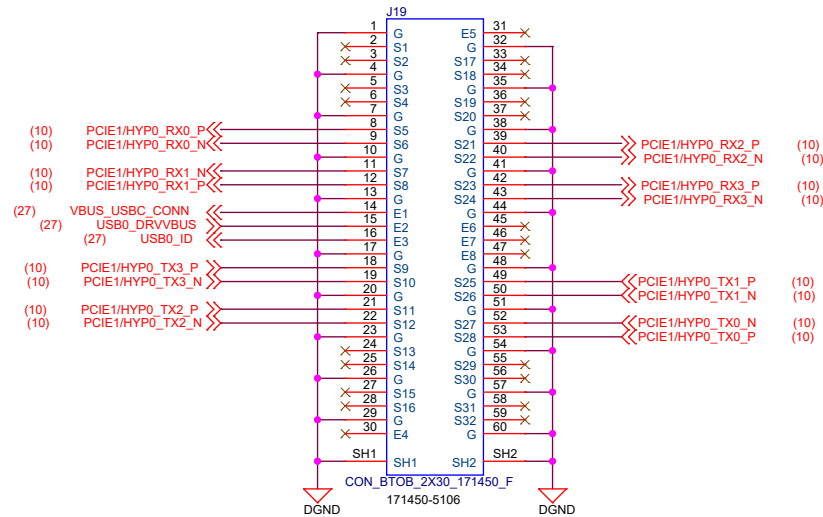




HYPERLINK SIDEBAND & CSI-TX CONNECTOR

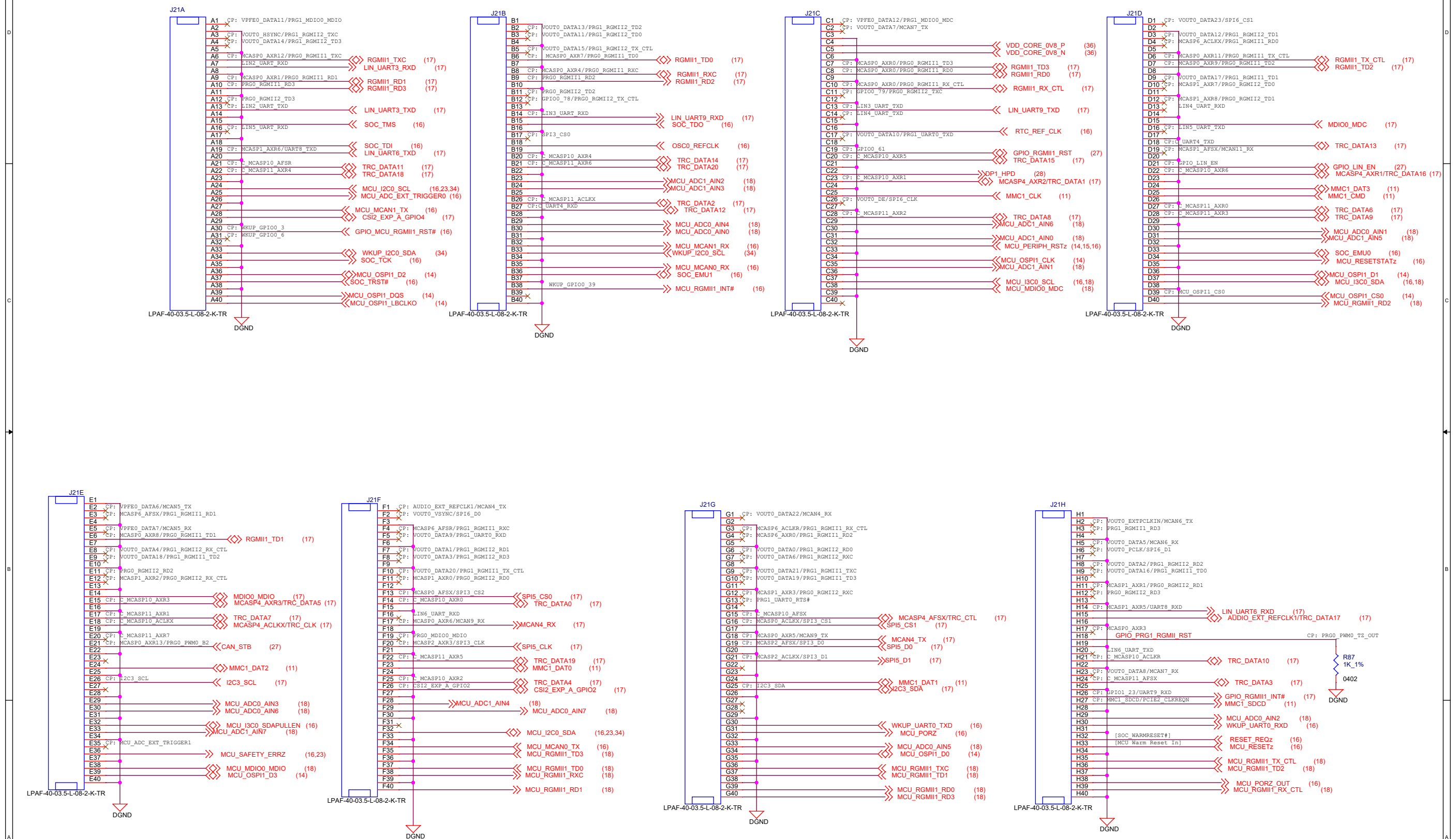


# SOM to COMM PROC SERDES CONNECTORS

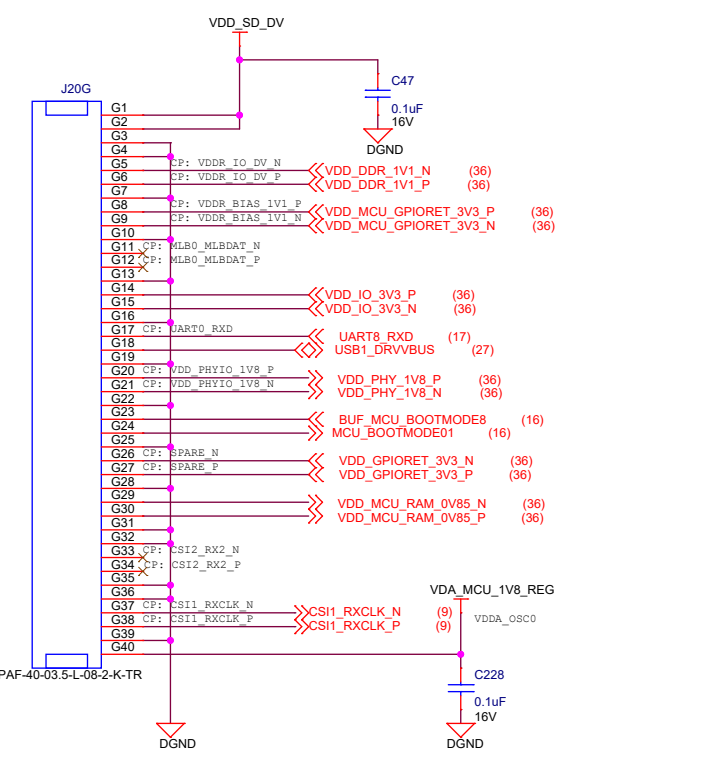
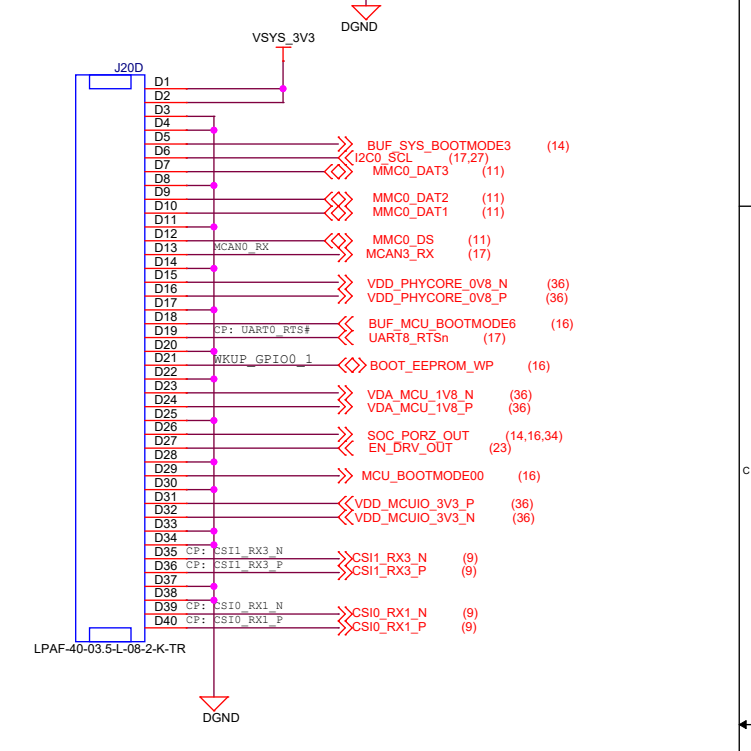
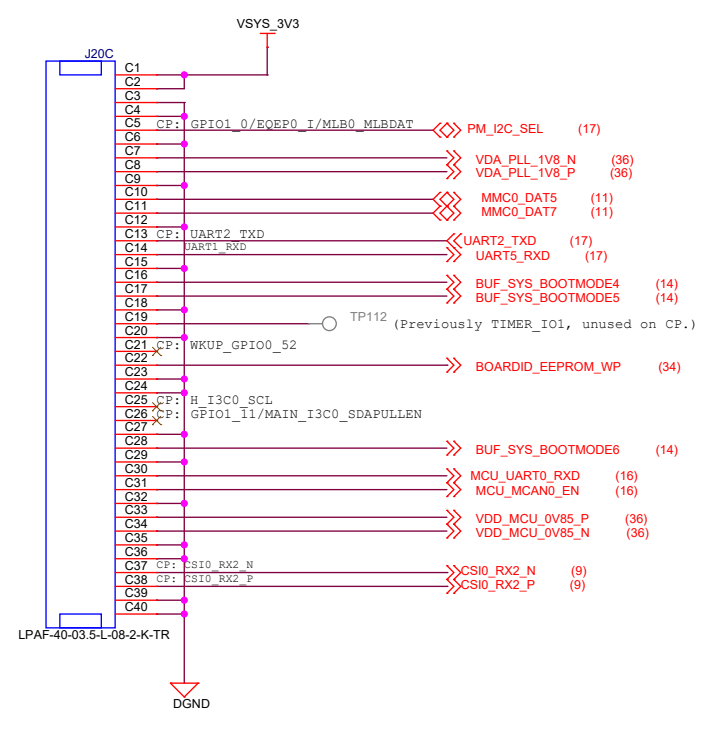
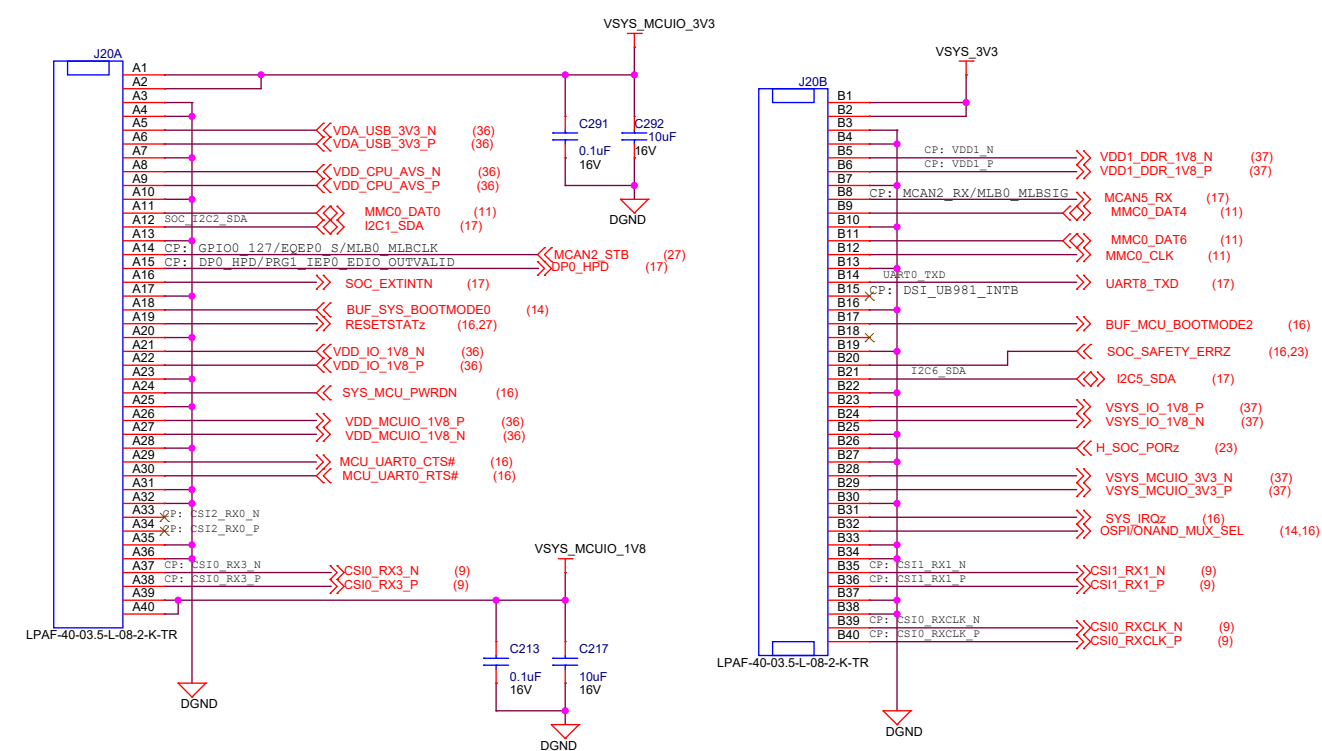
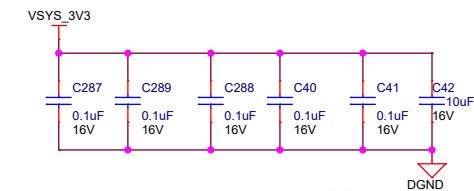


Unused DSI siganls tied to DGND

# SOM to COMM PROC PRIMARY CONN #1

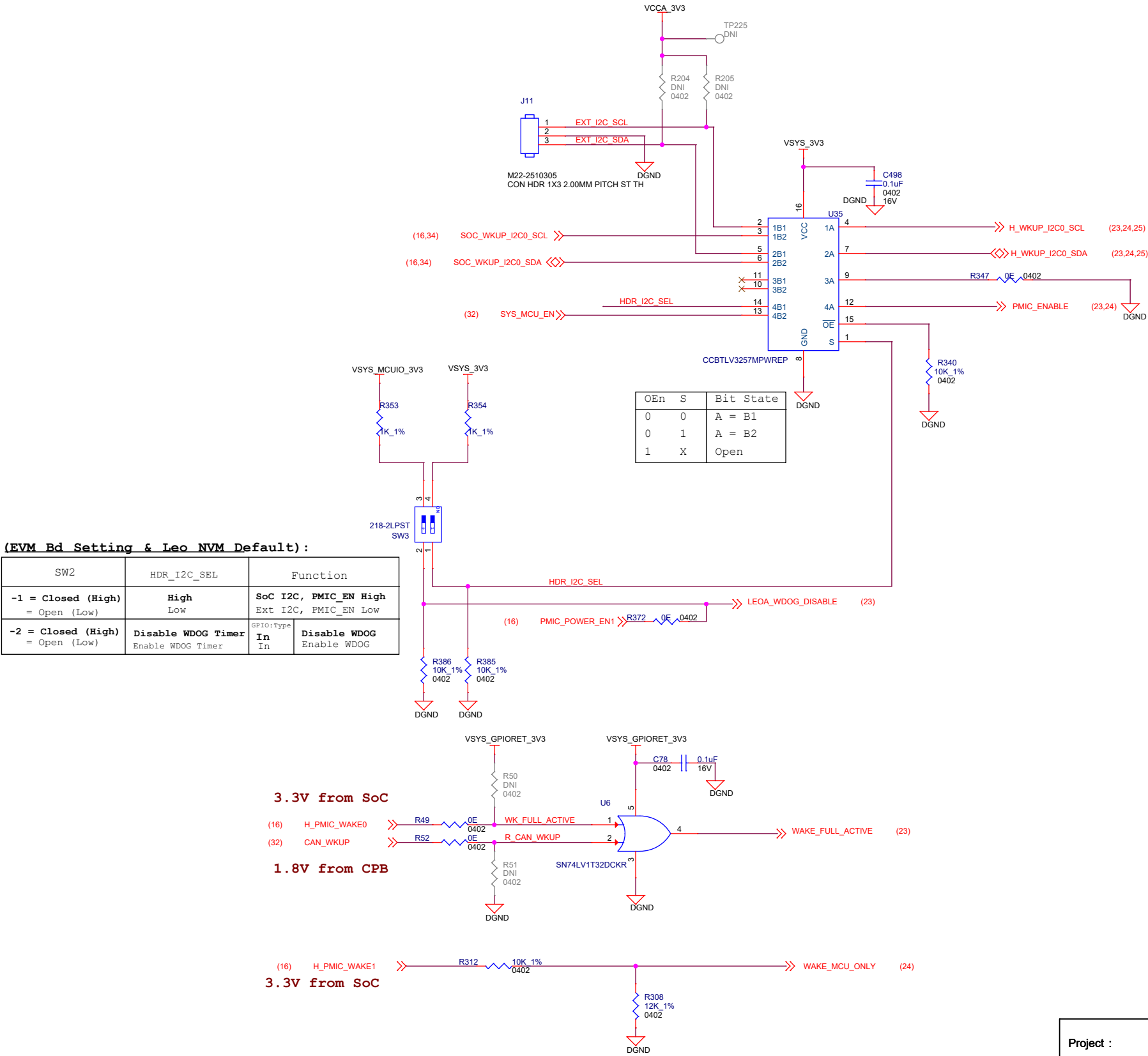


# SOM to COMM PROC PRIMARY CONN #2



PMIC Support Circuitry

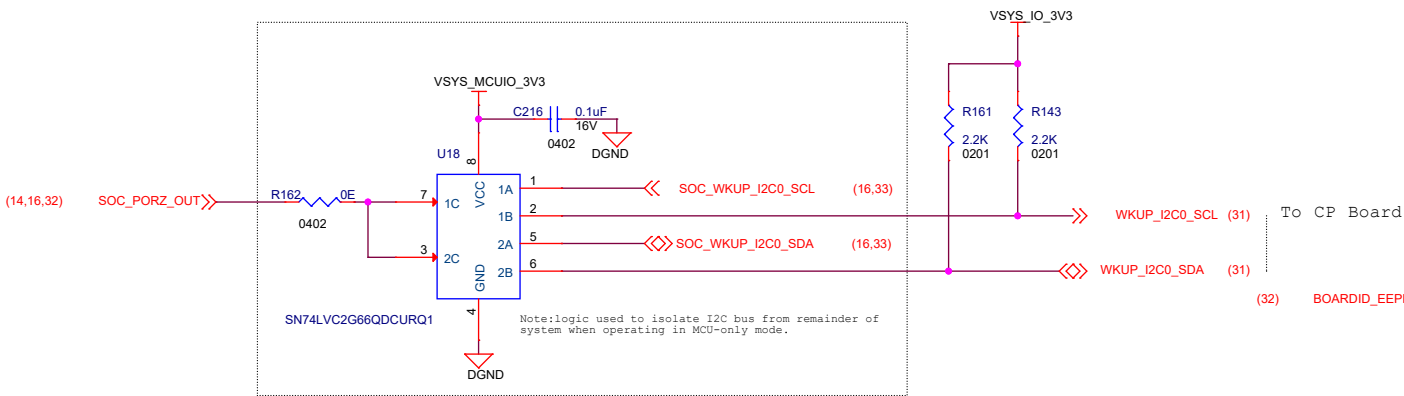
EVM development & evaluation Test circuitry  
(TI EVM Only)



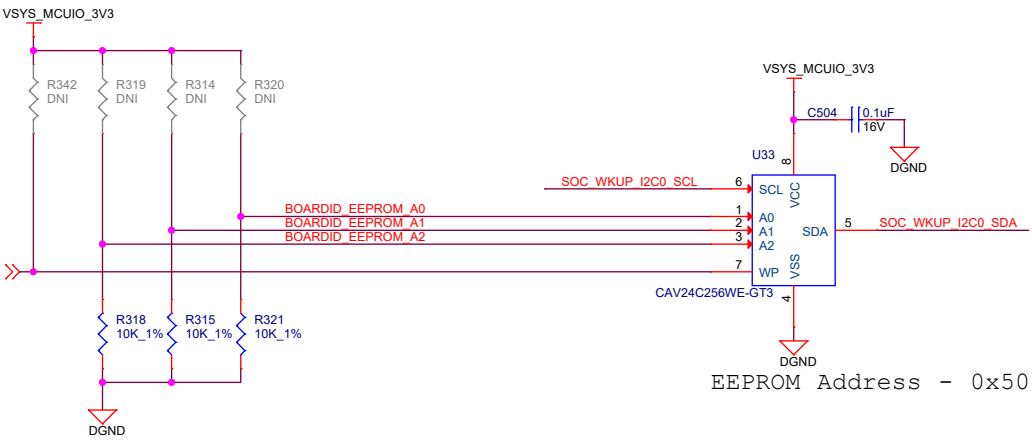
EVM development & evaluation test circuitry

(TI EVM Only)

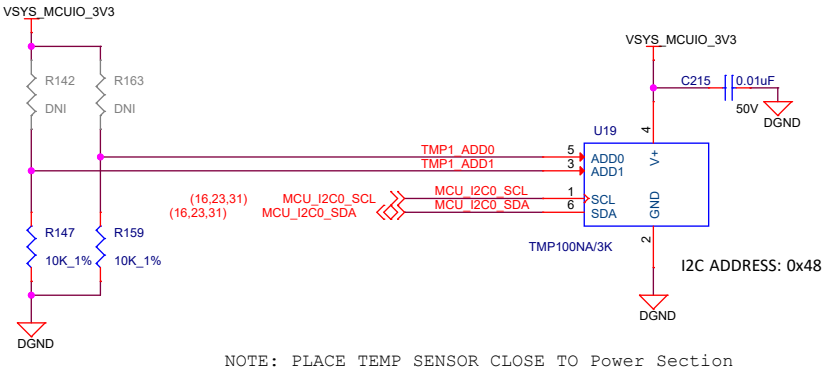
I2C for BOARD ID EEPROMs



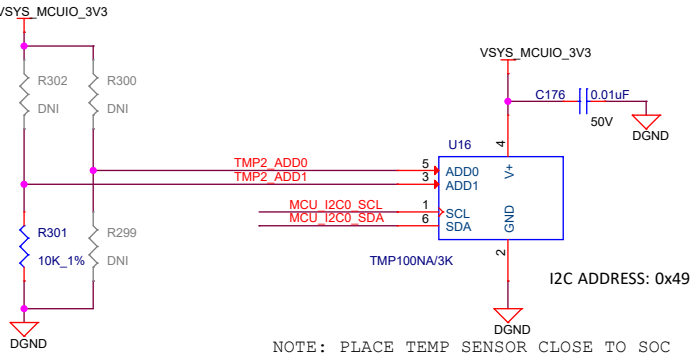
BOARD ID EEPROM (TI EVM Only)



TEMPERATURE SENSORS (TI EVM Only)

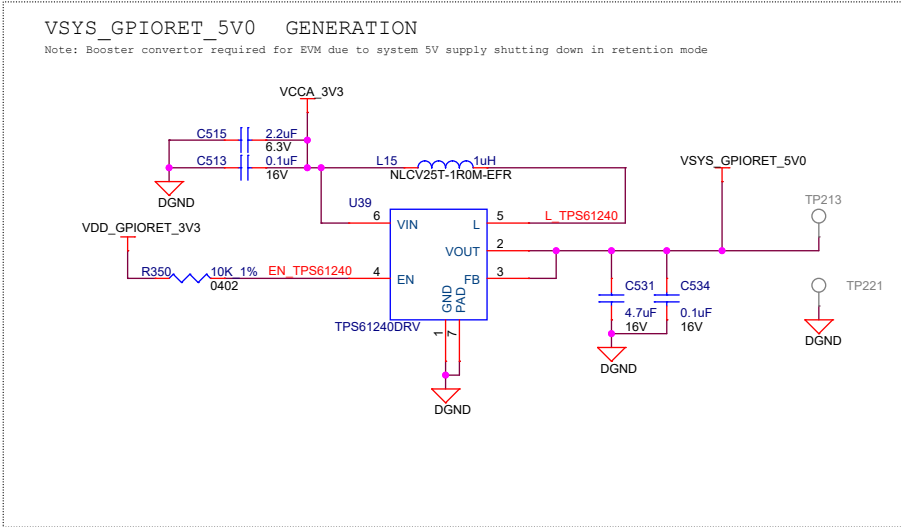


NOTE: PLACE TEMP SENSOR CLOSE TO Power Section

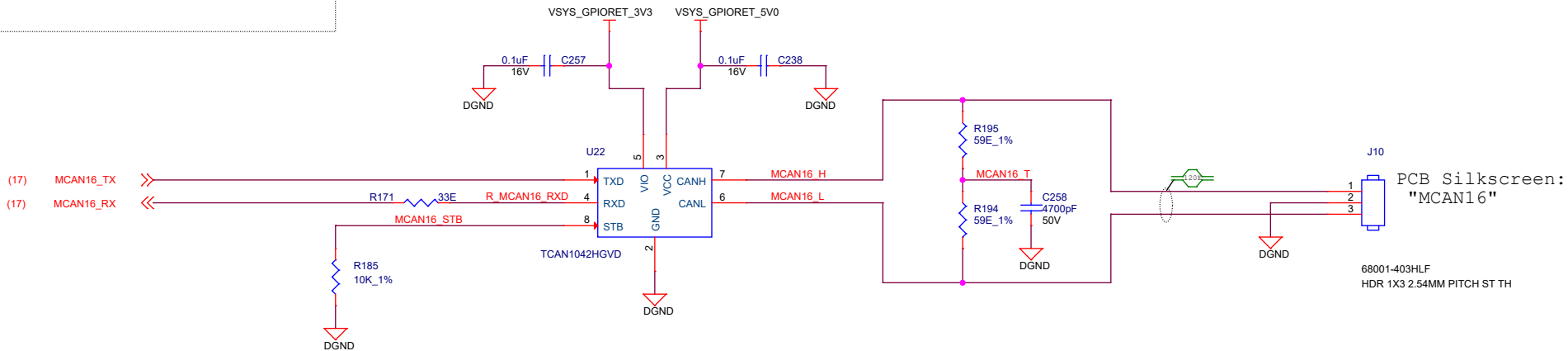


NOTE: PLACE TEMP SENSOR CLOSE TO SOC





# CAN TRANSCEIVER

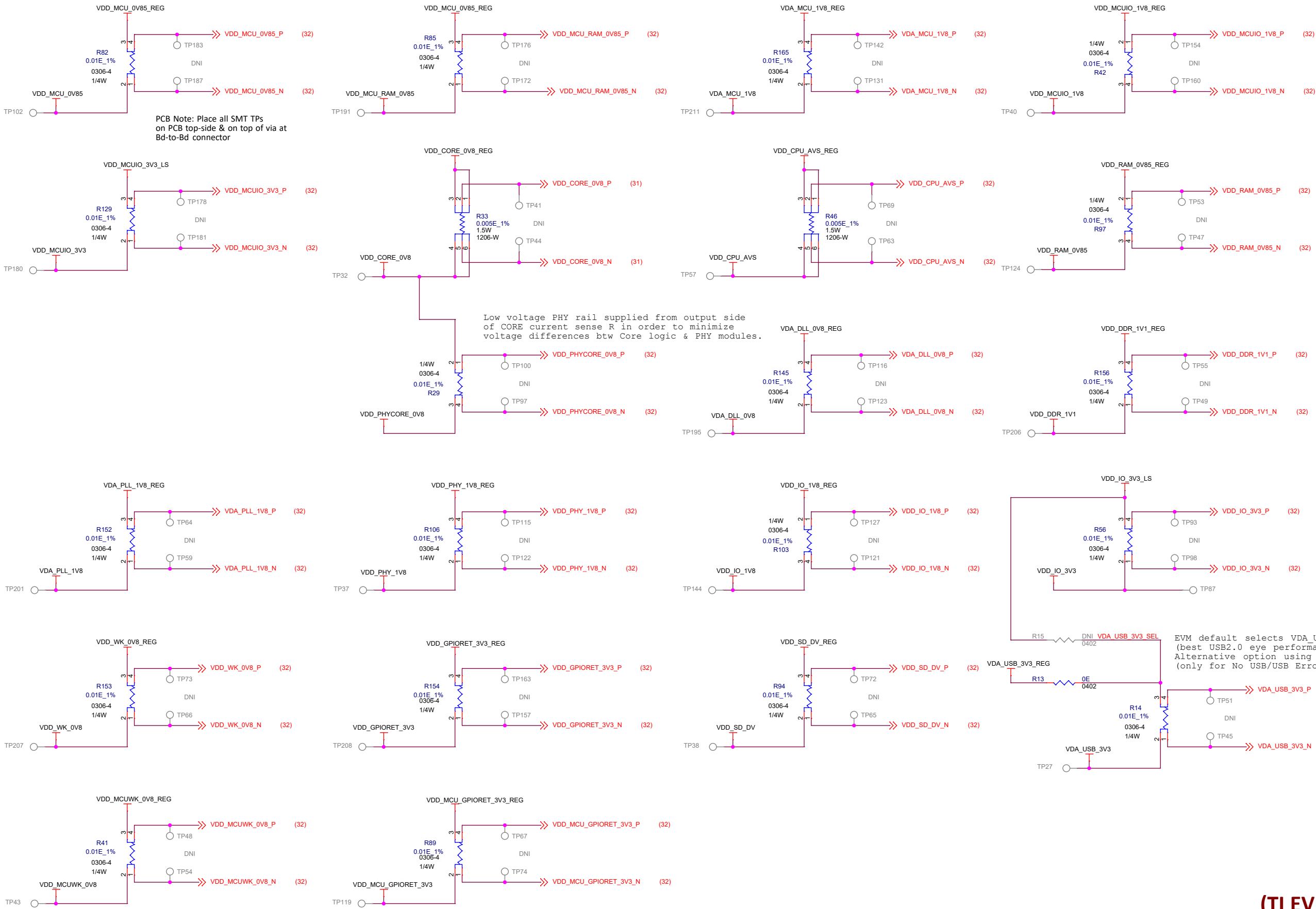


(TI EVM Only)

# EVM development & evaluation test circuitry

## SOC Current Sense Resistors

(TI EVM Only)

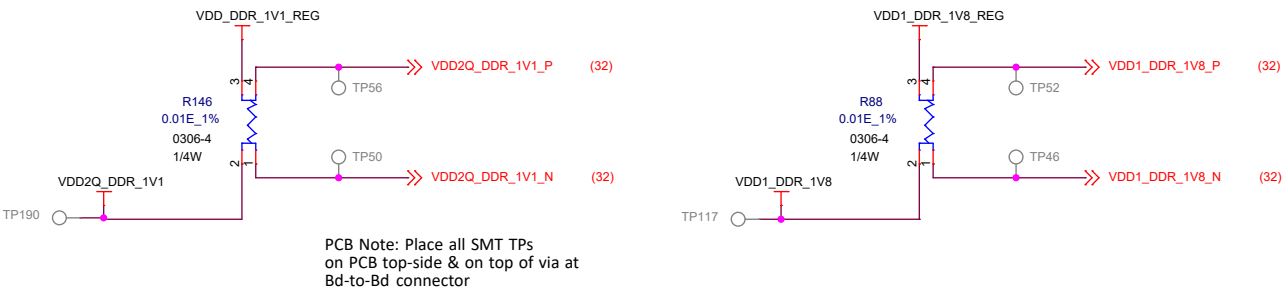


(TI EVM Only)

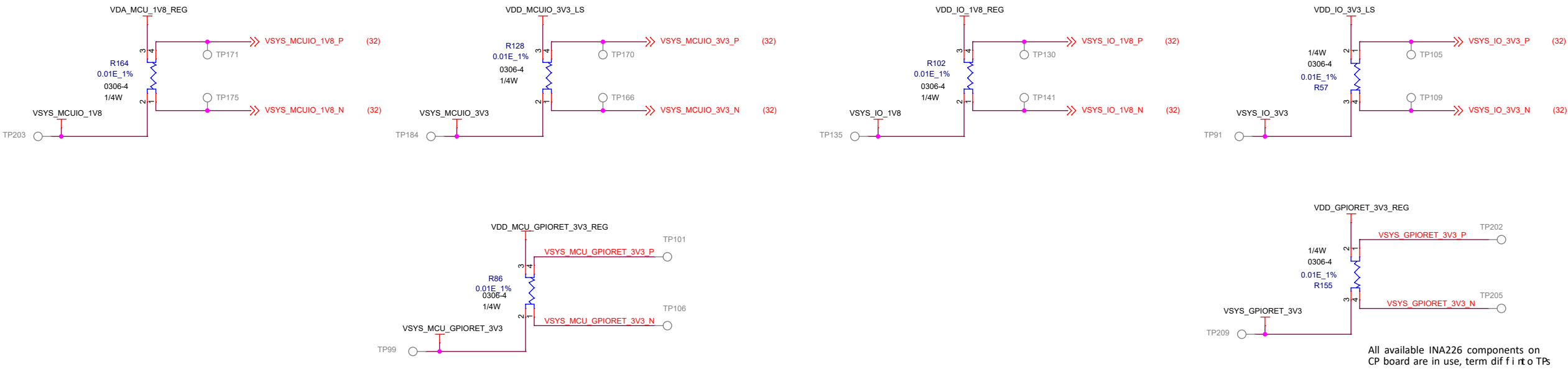
(TI EVM Only)

Project : J7 EVM		Title SOC Current Sense Resistors	
		Size C	Rev E1C
		Date: Thursday, October 14, 2021	Sheet 36 of 39

LPDDR4 SDRAM Current Sense Resistors



Peripheral Current Sense Resistors



# EVM Development & Evaluation test circuitry

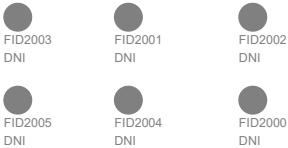
(TI EVM Only)

## NOTES, HW & LABELS

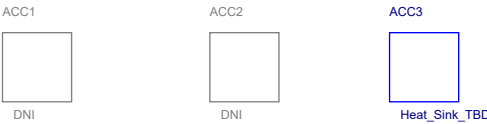
### ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

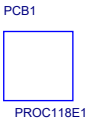
### FIDUCIALS



### SOCKET, PROCESSOR & HEATSINK AS ACCESSORIES



### BARE PCB



### LABELS

#### Board Serial No.



#### Assembly Revision.



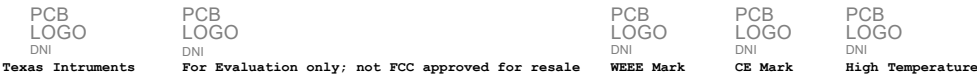
#### EVM Orderable No.



#### Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J721S2XSOMG01EVM
002:Soldered HS SoC	J721S2XSOMH01EVM
003:Socketed SoC	J721S2XSOMS01EVM

### LOGOs



# SI\_SIMULATION\_COUPON\_BD

Note: Test coupon not part of EVM design, to be used for TI test only

