

J784S4X Evaluation Board


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VER	4.5


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REVISION HISTORY #1

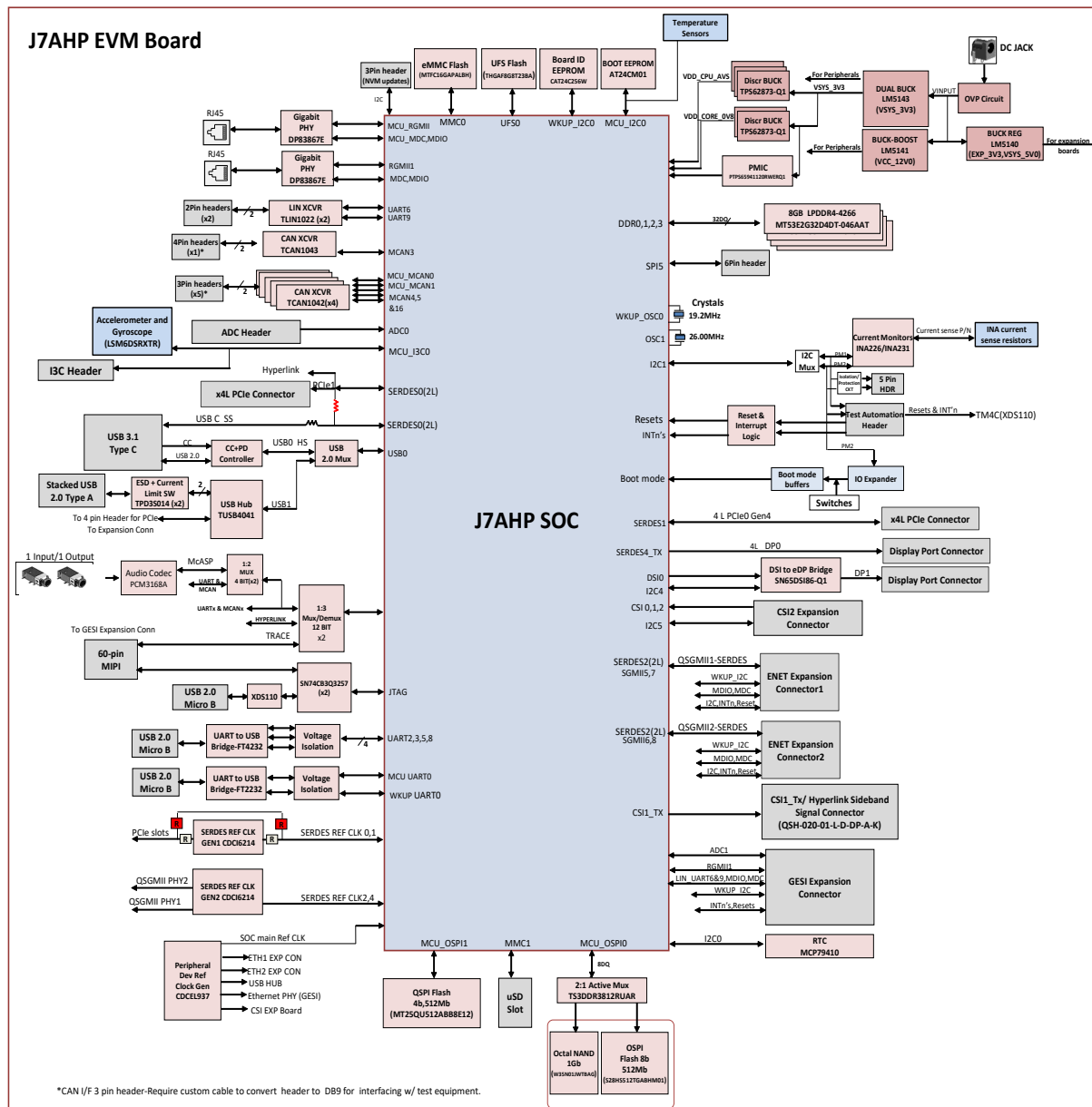
	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	2.7	05 APR 2022	Updates shared by TI for REV E2 is done Fix for VSYS_IO_1V8 rail is updated	Mistral Design Team		
	2.8	20 APR 2022	Updated PDN SCH notes (purple font) on pgs: 26-28, 30-33, 79, 80 Updated SoC Analog SCH pg 26 filtering component values	TI		
	2.9	21 APR 2022	Updated PMIC SCH pg 30 format & power inductor values optmzcd for Fsw = 4.4MHz per IPM sim results Ref clock for PCIe x2L set to SOC clock by default	Mistral Design Team		
	3.0	26 APR 2022	Updated for PCIe ref clock connection DNI'd termination for QSGMII ref clock Minor PDN SCH pg updates	Mistral Design Team		
	3.1	27 APR 2022	Updated resistor R1292 and R1293	Mistral Design Team		
E2A	3.2	20 JUN 2022	Added note for updated VCC_12V0 Enable supply DNI'd U29 and U159 (I2C buffers connected to XDS) to avoid leakage on VCC3V3_XDS Updated "EVM Bd Setting & Leo NVM Default" Table	Mistral Design Team		
	3.3	30 JUN 2022	DNI'd resistors R659 and R1122 DNI'd U29 and U159 (I2C buffers connected to XDS) to avoid leakage on VCC3V3_XDS	Mistral Design Team		
E3	3.4	06 JUL 2022	Updated sedres0 and serdes1 reference clock Changed R617 and R700 to 3k Changed VCC_12V0 enable to VSYS_3V3 Changed SW2 pin 8 pull up supply to VSYS_3V3	Mistral Design Team		
	3.5	12 JUL 2022	Updated VMON supplies connected to the SVS A and B as per PDN ver0.14d Updated sedres0 and serdes1 reference clock resistor option	Mistral Design Team		
	3.6	13 JUL 2022	Netname updated to XDS110_BUF_SELn Removed capacitor C748,C757 Updated I2C buffers used for PM_I2C connected to XDS110 to SN74CB3Q312 Provided resisor option for VCC_12V0 buck enable supply. Enable from VSYS_IO_3V3 by default	Mistral Design Team		
	3.7	19 JUL 2022	Updated for TI review comments Changed TP166 and TP177 to TP20_SMD	Mistral Design Team		
	3.8	20 JUL 2022	Updated for TI review comments	Mistral Design Team		
	3.9	21 JUL 2022	Updated SVS part number to PPS389006004NRTERQ1	Mistral Design Team		
	4.0	26 JUL 2022	Updated PDN Updated VDD_SD_DV Enable logic DNI'd R271 and R1063	Mistral Design Team		
	4.1	29 JUL 2022	DNI'd reserved current monitors for CORE,CPU_AVS and DDR rails	Mistral Design Team		
	4.2	1 AUG 2022	DNI'd SVS monitor IC's U87 and U89	Mistral Design Team		
	4.3	9 AUG 2022	INA231 IC's are made as populate and INA226 IC's as DNI	Mistral Design Team		
	4.4	12 AUG 2022	DNI'd resistor R752 Added thermal accessories to schematic hardware page	Mistral Design Team		
	4.5	12 SEP 2022	Few SoC deCaps were replaced with GCM Series murata caps 16GB eMMC is replaced with 32GB part with MFR# MTFC32GAZAQHD-AAT C1042, C901, C1018 were replaced with 4.7uF,4V,0402 cap(GCM155D70G475ME36)	Mistral Design Team		

Project :	J7 EVM		Title REVISION HISTORY		
			Size	PROC141 001 J784S4XG01EVM	Rev
			C		E3
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REVISION HISTORY #2

Project : J7 EVM		Title REVISION HISTORY	
		Size C	Rev E3
		Date: Tuesday, September 13, 2022	
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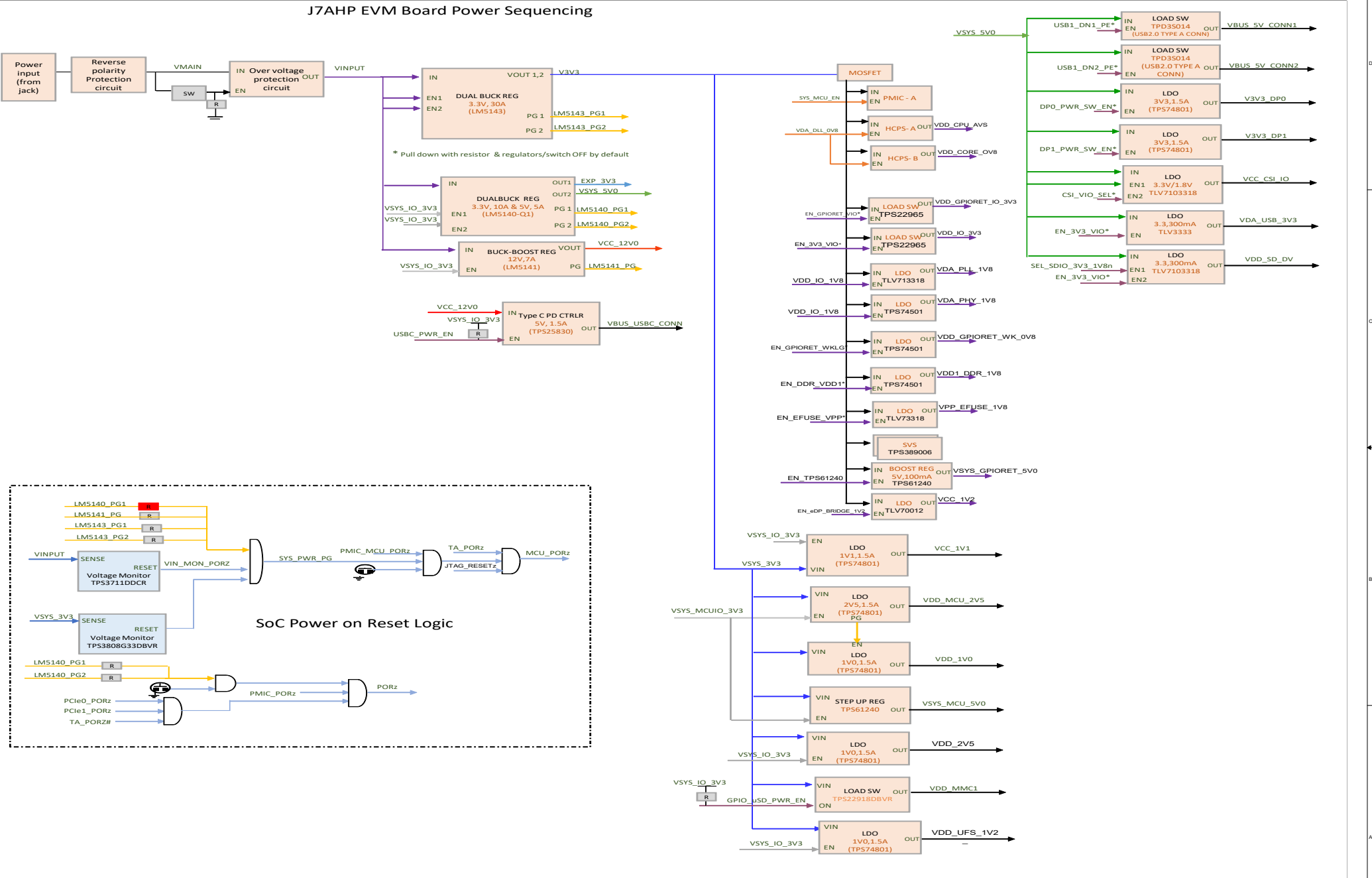
BLOCK DIAGRAM



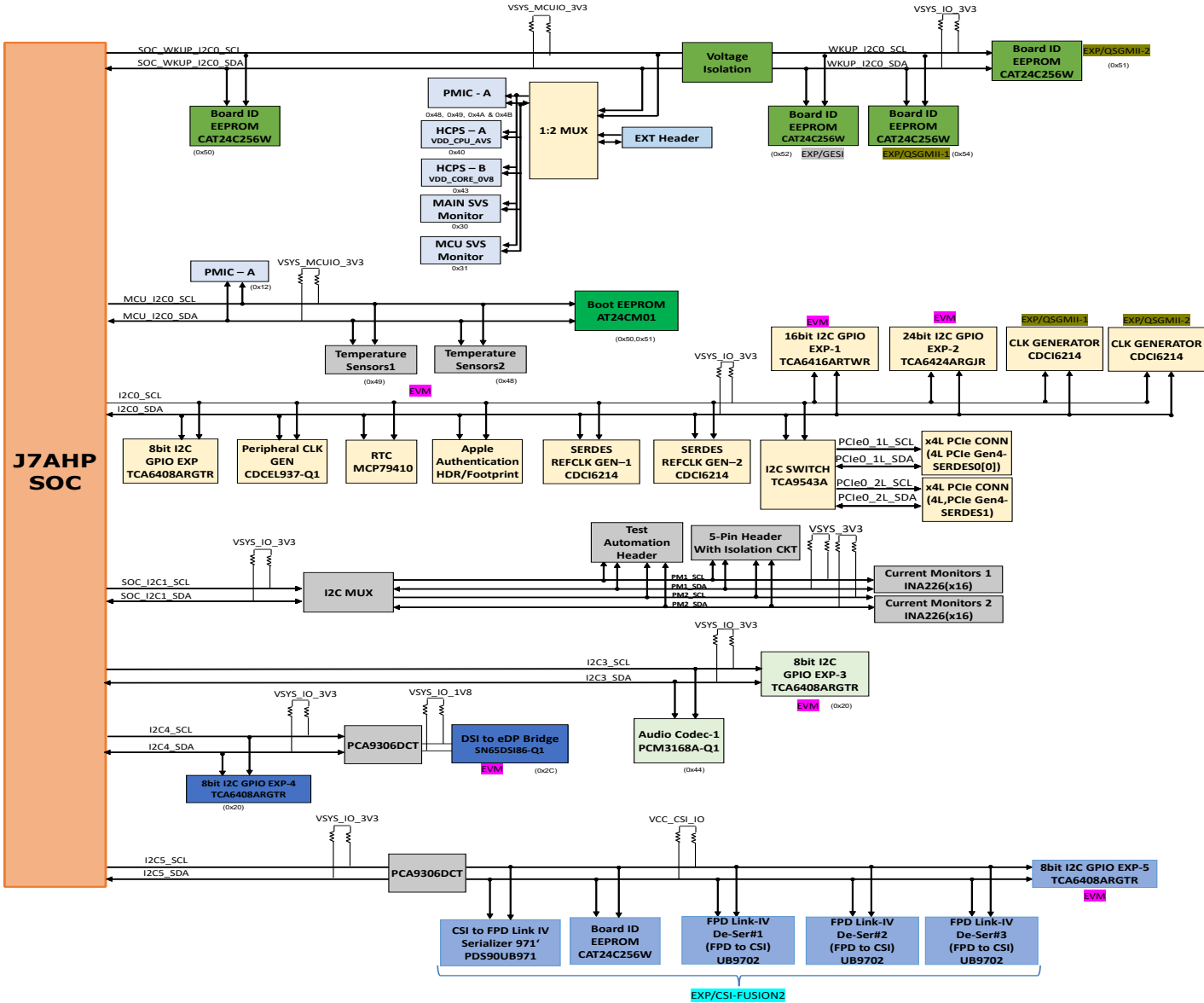
P EVM POWER Tree

POWER SEQUENCE

J7AHP EVM Board Power Sequencing



I2C TREE



I2C TABLE

Board	Interface name	Part#	Address	J7AHP Port mapping
EVM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0
EXP/QSGMII -1	Board ID EEPROM	CAT24C256WI-GT3	0x54	
EXP/QSGMII -2	Board ID EEPROM	CAT24C256WI-GT3	0x51	
EXP/GESI	Board ID EEPROM	CAT24C256W	0x52	
EVM	PMICs	PMIC A: TPS659413	PMIC A: 0x48, 0x49, 0x4A & 0x4B	
EVM	Tulip - VDD_CPU_AVS Regulator	TPS62873	0x40	
EVM	Tulip - VDD_CORE_OV8 Regulator	TPS62873	0x43	
EVM	MAIN SVS Monitor	PPS38900603NRTERQ1	0x30	
EVM	MCU SVS Monitor	PPS38900603NRTERQ1	0x31	
EVM	Temperature Sensors	TMP100NA/3K	0x48, 0x49	MCU_I2C0
EVM	Boot EEPROM	AT24CM01	0x50, 0x51	
EVM	I2C Switch for PCIe	TCA9543APWR	0x70	Main I2C0
EVM	RTC Clock	MCP79410-I/SN	0x57,0x6F	
EVM	SerDes Clock gen #1 Optional	CDCI6214	Optional	
EVM	SerDes Clock gen #2	CDCI6214	0x77,0x76	
EVM	Pheriphal Clock Gen	CDCEL937-Q1	0x6D	
EVM	16bit I2C GPIO EXPANDER1	TCA6424ARGJR	0x20	
EVM	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22	
EVM	8 bit I2C GPIO Expander4	TCA6408ARGTR	0x20	Main I2C4
EVM	DSI TO eDP BRIDGE	SN65DSI86IPAPQ1	0x2C	
EVM	DSI FPC Connector	<connector interface>		
EVM	I2C Switch for Automation header		0x22	Main I2C1
EVM	Current Monitors and Header		0x40 to 0x4F	
EVM	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3
EVM	AUDIO IF Codec	PCM3168A-Q1	0x44	
EXP	8bit GPIO Expander5	TCA6408ARGTR	0x20	Main I2C5
EXP/CSI-FUSION2	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	0x3D	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x30	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x32	
EXP/CSI-FUSION2	CSI to FPD Link IV Serializer 971	UB971	0x18	

GPIO EXPANDER MAP/TABLE

J7AHP EVM - GPIO Mapping Table						
WKUP Domain						
Net name	Package Signal Name	GPIO Number	Input/Output	Default	State	Remarks
EN_EFUSE_VPP	WKUP_GPIO0_54	WKUP_GPIO0_54	Output	BOOTMODE	Active High	VPP_EFUSE_LDO enable
BOOT_EEPROM_WP	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	BOOTMODE	Active High	Boot EEPROM Write protect
MCU_CAN1_STB	WKUP_GPIO0_2	WKUP_GPIO0_2	Output	BOOTMODE	Active High	MCU_CAN1 Standby
GPIO_MCU_RGMII1_RST#	WKUP_GPIO0_56	WKUP_GPIO0_56	Output	BOOTMODE	Active low	MCU_RGMII1_Reset
SYS_IRQz	WKUP_GPIO0_7	WKUP_GPIO0_7	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0'>'1' - interrupt pending, '1' - normal operation)
OSPI/HYPER_MUX_SEL	WKUP_GPIO0_6	WKUP_GPIO0_6	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - OCTAL NAND)
PMIC_MCU_INT# / H_MCU_INT#	WKUP_OSP11_CSN1	WKUP_GPIO0_39	Input	PU	Active low	Interrupt from PMIC
MCU_RGMII1_INT#	WKUP_GPIO0_3	WKUP_GPIO0_3	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
SYS_MCU_PWRDN	MCU_SPI0_D0	WKUP_GPIO0_55	Output	BOOTMODE	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_CAN0_STBz	MCU_SPI0_D1	WKUP_GPIO0_69	Output	BOOTMODE	Active low	MCU_CAN0 Standby
LSM6DSOX_INT/LSM6DSRX_INT	WKUP_GPIO0_57	WKUP_GPIO0_57	Input	BOOTMODE	NA	Interrupt from IIC Gyroscope sensor(*LSM6DSRX)
PM_I2C_SEL	WKUP_GPIO0_66	WKUP_GPIO0_66	Output	BOOTMODE	Active High	PM_I2C Mux selection, ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA)
USBC_DIR_SOC	MCU_OSP10_CSN1	WKUP_GPIO0_28	Input	PU	Active High	USB C direction pin
ENET1_EXP_INTB	MCU_ADC1_AIN5	WKUP_GPIO0_84	Output	PU	Active low	ENET expansion 1 Interrupt signal
ENET2_EXP_INTB	MCU_ADC1_AIN6	WKUP_GPIO0_85	Output	PU	Active Low	ENET expansion 2 Interrupt signal
I2C0_IDEXP_INT#	MCU_ADC1_AIN7	WKUP_GPIO0_86	Output	PU	Active Low	I2C0 IO expander interrupt signal
CAN0_RET_WAKE	MCU_SPI0_CS0	WKUP_GPIO0_70	Input	PU	NA	Push-button wake signal
Main Domain						
MAIN_RET_WAKE	GPIO0_11	GPIO0_11	Input	PU	NA	Push-button wake signal
I2C5_IO_EXPANDER_INTERRUPT	MCASPO_AXR2	GPIO0_18	Input	PU	Active Low	I2C5 IO expander interrupt. Muxed with trace and Hyperlink signals
SEL_SDIO_3V3_1V8N	MCAN15_RX	GPIO0_8	Output	NA	Active low	SW controls & transition Sd card to high speed 1.8V signaling If card type supports
CSI2_EXP_A_GPIO2(MCASPA4_AXR1/T_RC_DATA16_MUX)	MCAN0_RX	GPIO0_26	I/O	NA	NA	CSI2 Expansion Board Specific. Muxed with trace and Hyperlink signals
CSI2_EXP_A_GPIO4(MCASPA4_AXR3/T_RC_DATA5_MUX)	MCAN1_RX	GPIO0_28	I/O	NA	NA	CSI2 Expansion Board Specific. Muxed with trace and Hyperlink signals
TRC_DATA0_MUX	MCAN13_TX	GPIO0_3	Input	PU	NA	Interrupt signal from DSI to eDP bridge
SOC_GPIO0_21_MUX	MCASPA2_ACLKX	GPIO0_21	Input	PU	Active Low	RGMII1_INT signal
GPIO Expander - 1 Part# TCA6424ARGIR						
I2C0/0x20	P00	PCIE1_2L_MODE_SEL	Input	DIP_SEL	NA	PCIE1 4-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P01	PCIE1_4L_PERSTz	Input	PD	Active low	PCIE1 4-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P02	PCIE1_2L_RC_RSTz	Output	PD	Active low	PCIE1 4-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P03	PCIE1_2L_EP_RST_EN	Output	PD	Active low	PCIE1 4-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P04	PCIE0_4L_MODE_SEL	Input	DIP_SEL	NA	PCIE0 2-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P05	PCIE0_4L_PERSTz	Input	PD	Active low	PCIE0 2-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P06	PCIE0_4L_RC_RSTz	Output	PD	Active low	PCIE0 2-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P07	PCIE0_4L_EP_RST_EN	Output	PD	Active low	PCIE0 2-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P10	PCIE1_4L_PRSTN#	Input	PU	Active High	PCIE1 4-Lane Hot Plug/Card Detect ('0' - PCIE Card Detected, '1' - no card detected)
	P11	PCIE0_4L_PRSTN#	Input	PU	Active High	PCIE0 2-Lane Hot Plug/Card Detect ('0' - PCIE Card Detected, '1' - no card detected)
	P12	CDCl1_OE1/OE4	Output	PU	Active High	PCIE 2L Reference Clock Enable ('0' - clock disabled, '1' - clock enabled)
	P13	CDCl1_OE2/OE3	Output	PU	Active High	PCIE 1L Reference Clock Enable ('0' - clock disabled, '1' - clock enabled)
	P14	AUDIO_MUX_SEL	Output	PU	Active High	Mux select for McASP and trace signals
	P15	EXP_MUX2	Output	NA	NA	Expansion Board Mux control1
	P16	EXP_MUX3	Output	NA	NA	Expansion Board Mux control1
	P17	GESI_EXP_PHY_RSTz	Output	PU	Active High	EXP_RSTz - Terminated with Test point
GPIO Expander - 2 Part# TCA6424ARGIR						
I2C0/0x22	P00	R_GPIO_RGMII1_RST	Output	PU	Active low	Routed to INFO/GESI expansion connector. GESI - Used for GPIO_PRG0_RGMII1_RST; INFO - Not used
	P01	ENET2_I2CMUX_SEL	Output	PD	NA	Signal Mux Control ('0' - No Connect, '1' - I2C0)
	P02	GPIO_USD_PWR_EN	Output	PU	Active High	MicroSD Card Power Enable ('0' - power off, '1' - power on)
	P03	USBC_PWR_EN	Output	PU	Active High	USB-TypeC VBUS Controller Power Enable ('0' - power off, '1' - power on)
	P04	USBC_MODE_SEL1	Output	DIP_SEL	NA	USB-Type C Mode Select
	P05	USBC_MODE_SELO	Output	DIP_SEL	NA	USBC_MODE_SEL[1:0]: '00' = DFP, '01' = DRP, '1x' = UFP
	P06	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
	P07	R_CAN_STB	Output	PU	Active High	Standby signals for On BOARD and GESI CAN Transceiver
	P10	CTRL_PM_I2C_OE#	Output	PD	Active High	Gate drive for enable signal of PM I2C mux select
	P11	ENET2_EXP_PWRDN	Output	PU	Active low	Ethernet Expansion2 PHY Powerdown ('0' - normal operation, '1' - device power down)
	P12	ENET2_EXP_SPARE2	Input	NA	NA	Ethernet Expansion2 Spare2 ('0' - not defined, '1' - not defined)
	P13	CDCl2_RSTz	Output	PU	Active low	Peripheral Clock Generator ('0' - device reset, '1' - normal operation)
	P14	USB2_0_MUX_SEL	Output	PD	Active High	Signal Mux Control ('0' - USBC, '1' - USB Hub)
	P15	CANUART_MUX_SELO	Output	PD	Active High	Select line for both the CANUART MUX
	P16	CANUART_MUX2_SEL1	Output	PU	Active High	Select line for CANUART MUX2
	P17	CANUART_MUX1_SEL1	Output	PU	Active High	Select line for CANUART MUX1
	P20	ENET1_EXP_PWRDN	Output	PU	Active High	Ethernet Expansion1 PHY Powerdown ('0' - normal operation, '1' - device power down)
	P21	ENET1_EXP_RESETz	Output	PD	Active low	Ethernet Expansion1 Reset ('0' - device reset, '1' - normal operation)
	P22	ENET1_I2CMUX_SEL	Input	PD	NA	Signal Mux Control ('0' - No Connect, '1' - I2C0)
	P23	ENET1_EXP_SPARE2	Input	NA	NA	Ethernet Expansion1 Spare2 ('0' - not defined, '1' - not defined)
	P24	ENET2_EXP_RESETz	Output	PD	Active low	Ethernet Expansion2 Reset ('0' - device reset, '1' - normal operation)
	P25	USER_INPUT1	Input	DIP_SEL	NA	User Dip Switch Input1 ('0' - User Define, '1' - User Define)
	P26	USER_LED1	Output	PD	Active High	User LED1 Enable ('1' - LED Off, '0' - LED On)
	P27	USER_LED2	Output	PD	Active High	User LED2 Enable ('1' - LED Off, '0' - LED On)
GPIO Expander - 3 Part# TCA6408ARGTR						
I2C3/0x20	P0	CODEC_RSTz	Output	PD	Active low	Audio Codec Reset ('0' - device reset, '1' - normal operation)
	P1	CODEC_SPARE1	NA	UNUSED	NA	Not used (test point)
GPIO Expander - 4 Part# TCA6408ARGTR						
I2C40x20	P0	DP0_PWR_SW_EN	Output	PD	Active High	DisplayPort0 Power Enable ('0' - power off, '1' - power on)
	P1	DP1_PWR_SW_EN	Output	PD	Active High	DisplayPort1 Power Enable ('0' - power off, '1' - power on)
	P2	GPIO_eDP_ENABLE	Output	PU	Active High	DSI to eDP bridge enable
GPIO Expander - 5 Part# TCA6408ARGTR						
I2C5/0x20	P0	CSI2_EXP_RSTz	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	P1	CSI2_EXP_A_GPIO0	IO	NA	NA	CSI2 Expansion Board Specific.
	P2	CSI2_EXP_A_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific.
	P3	CSI2_EXP_A_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific.
	P4	CSI2_EXP_B_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific.
	P5	CSI2_EXP_B_GPIO2	IO	NA	NA	CSI2 Expansion Board Specific.
	P6	CSI2_EXP_B_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific.
	P7	CSI2_EXP_B_GPIO4	IO	NA	NA	CSI2 Expansion Board Specific.

Project :

J7 EVM



Title
GPIO EXPANDER MAP/TABLE

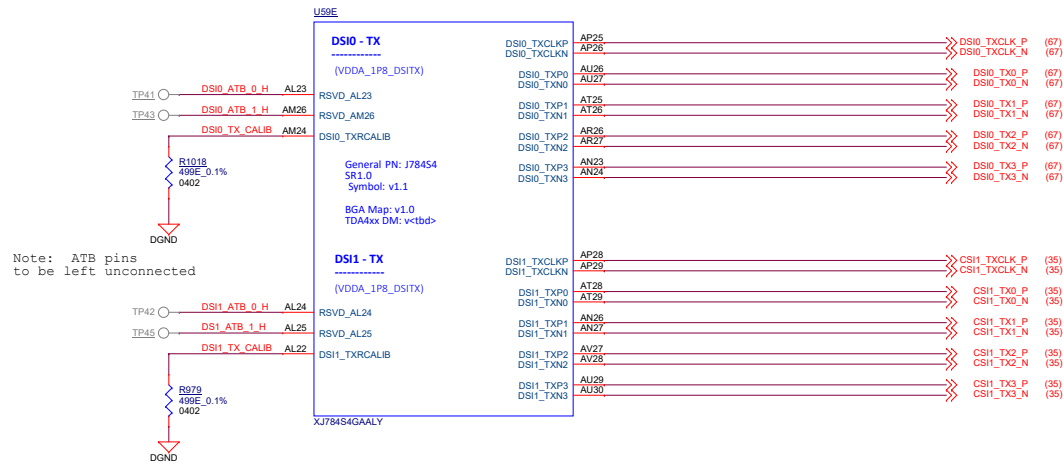
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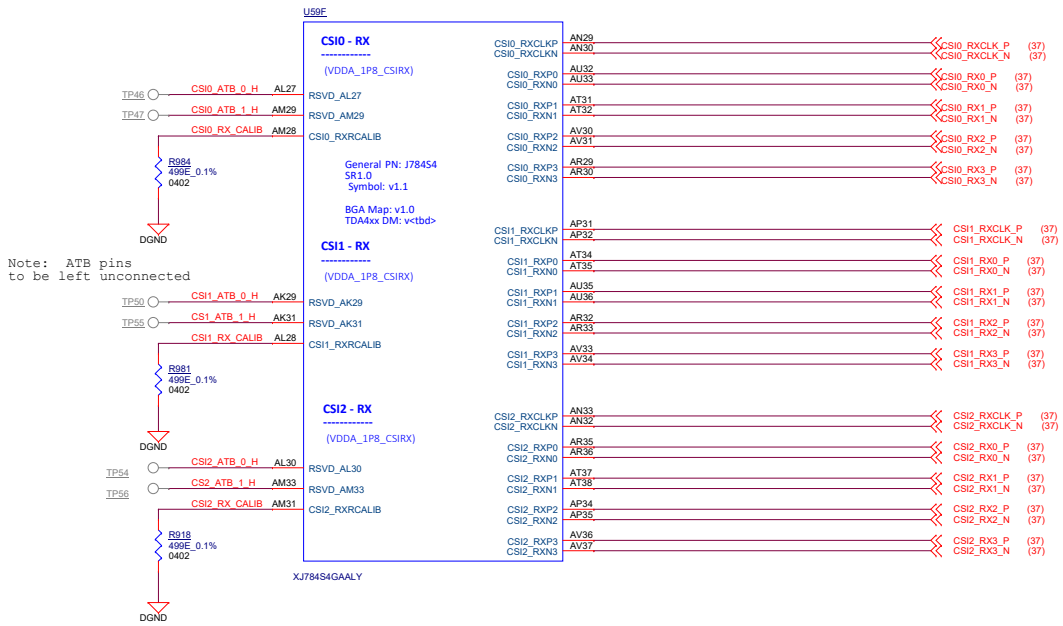
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E3

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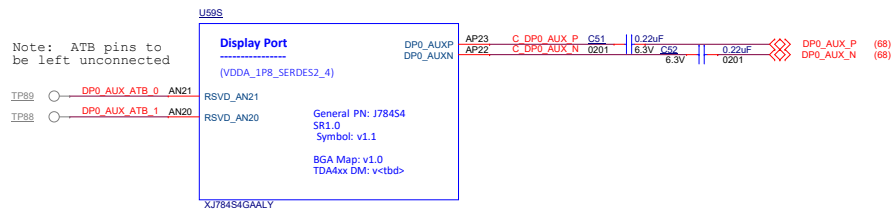
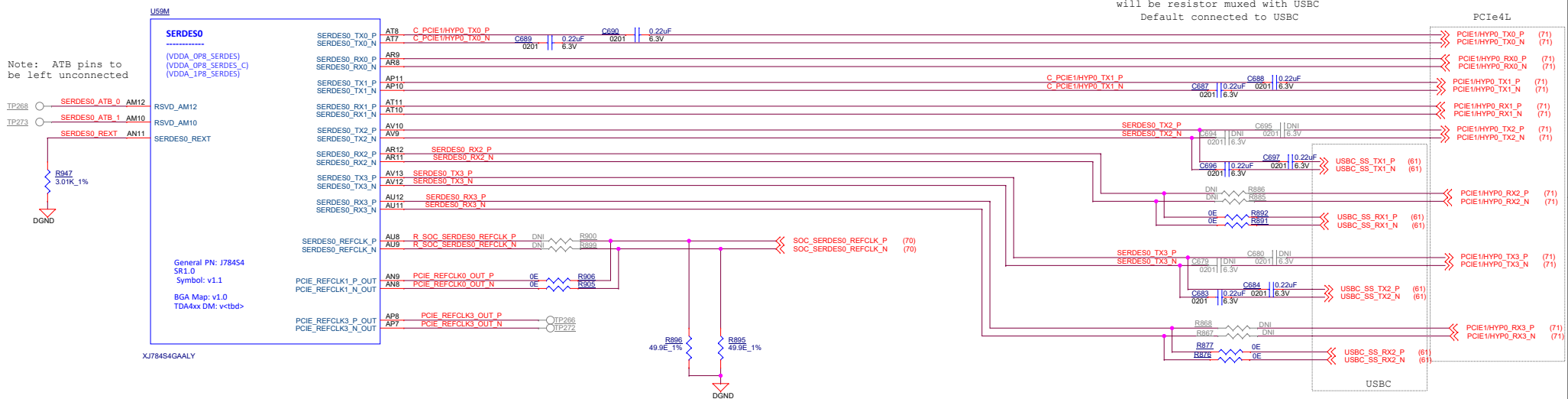
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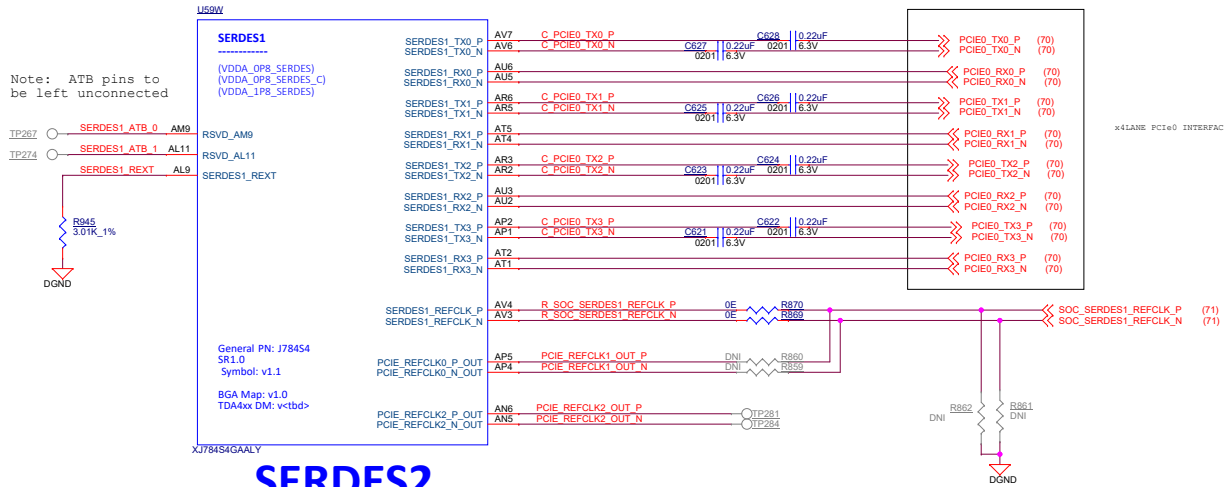
CSI



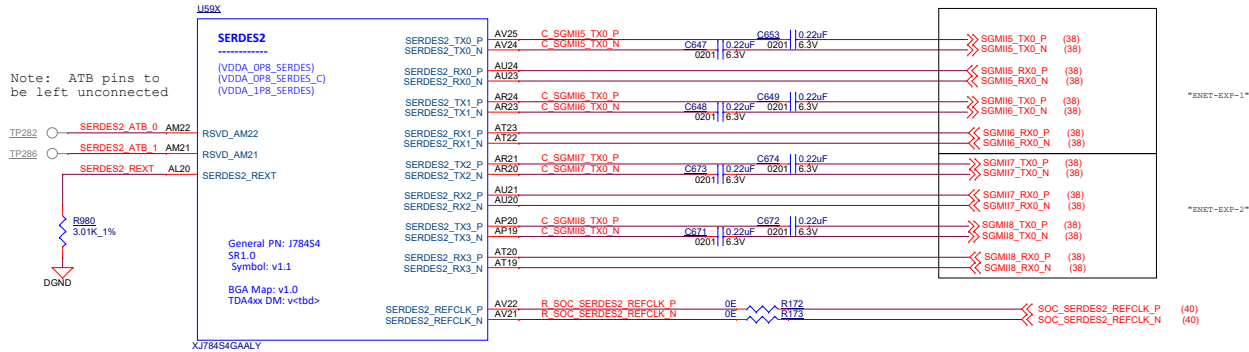
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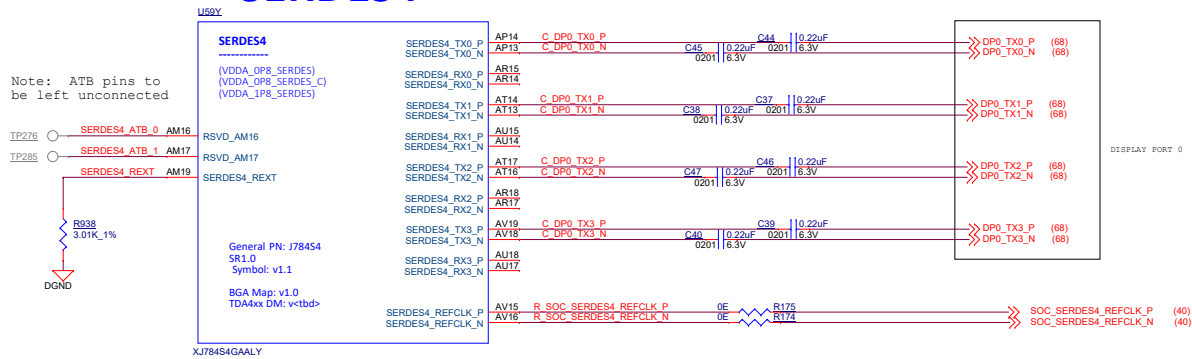
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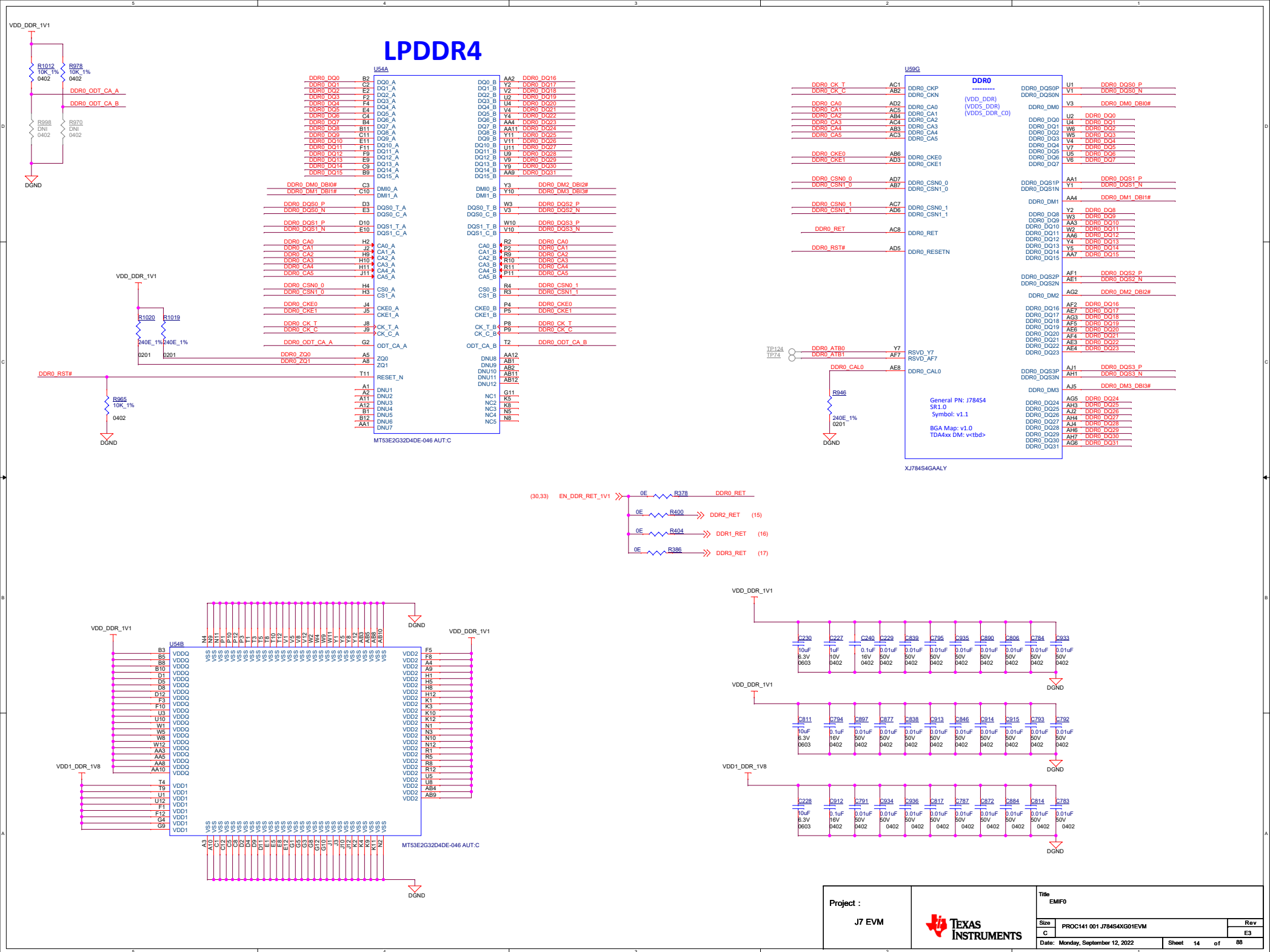
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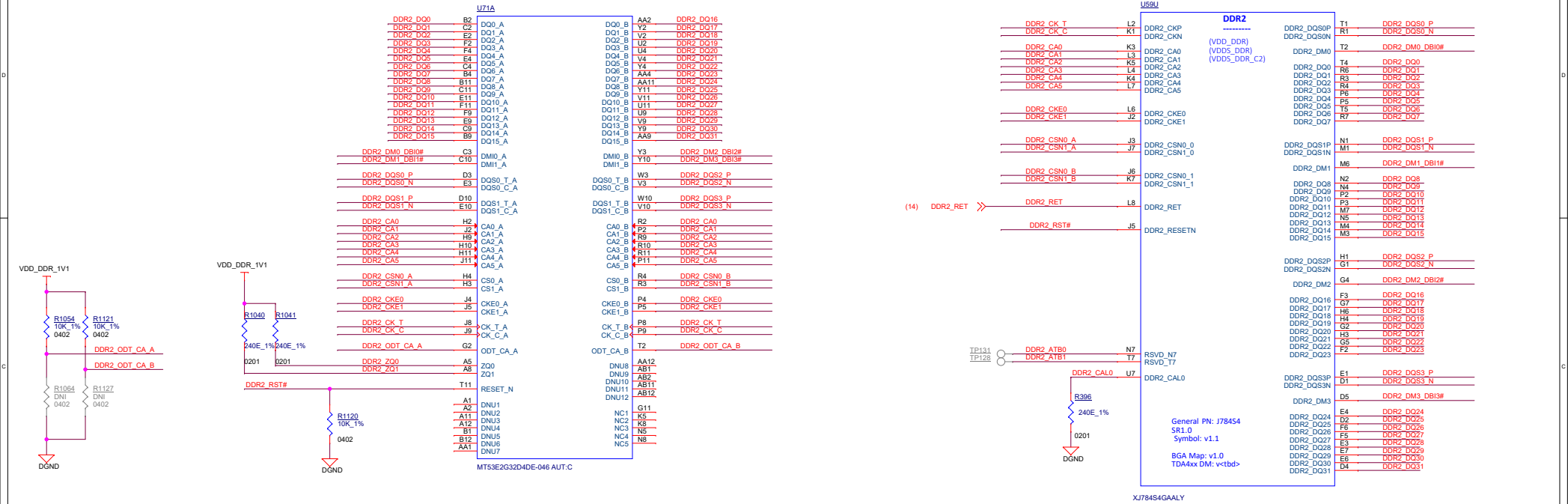
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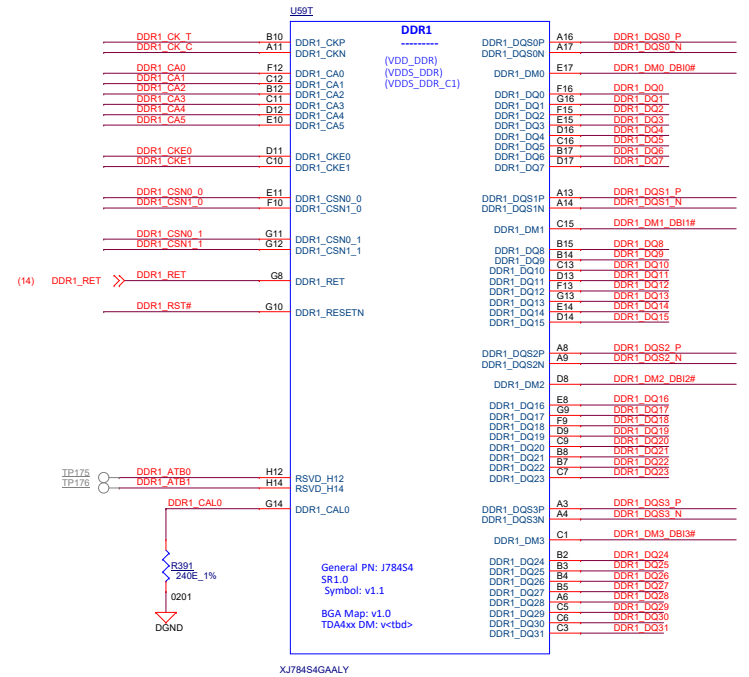
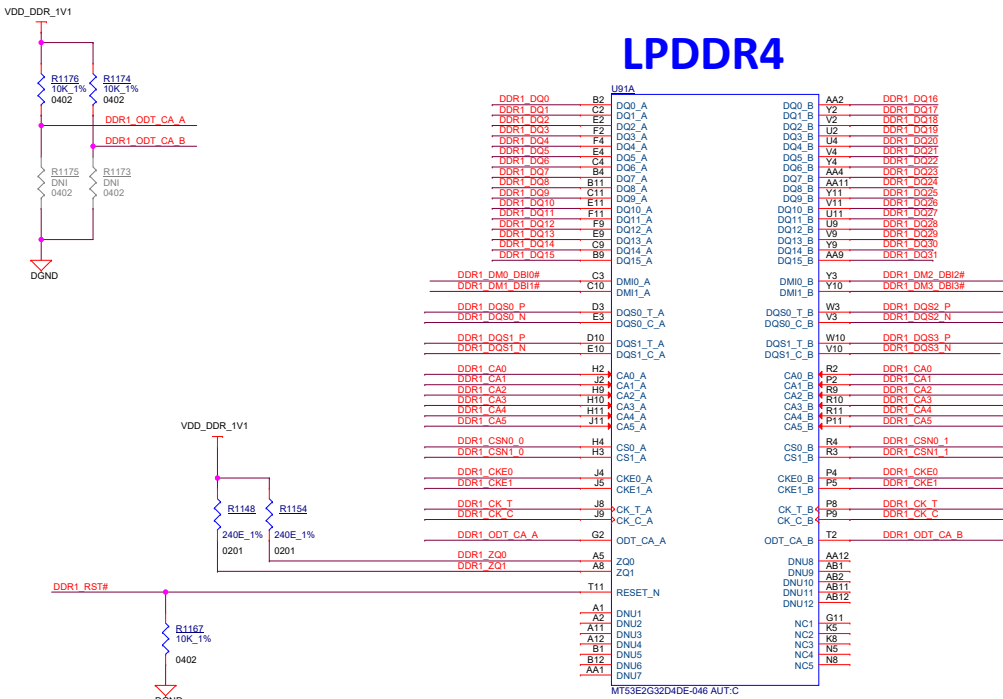
Project : J7 EVM		Title SERDES INTERFACE	
		Size C	Rev E3
		Date: Thursday, September 15, 2022	
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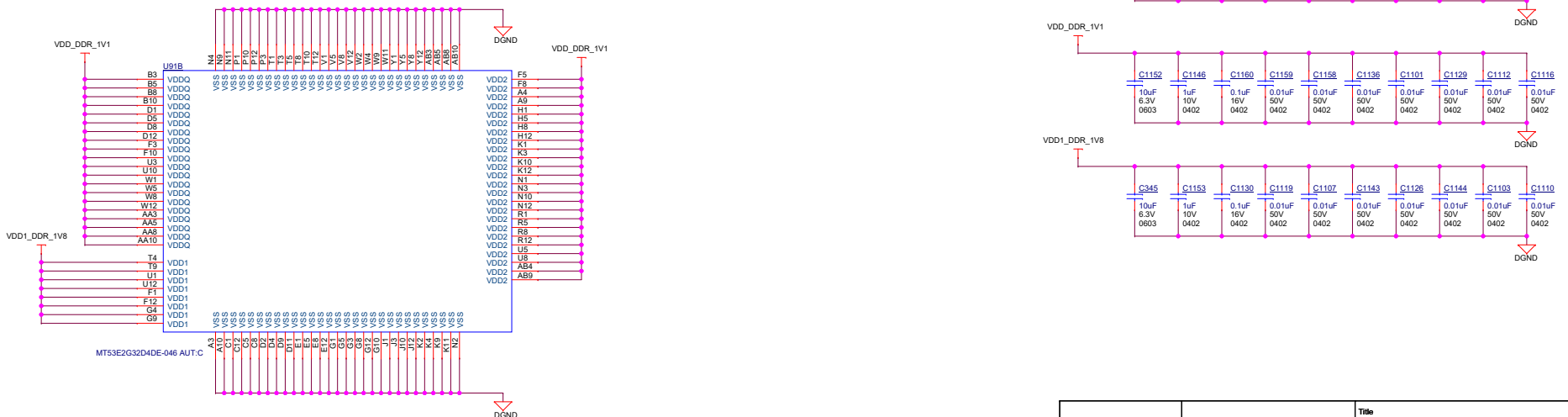
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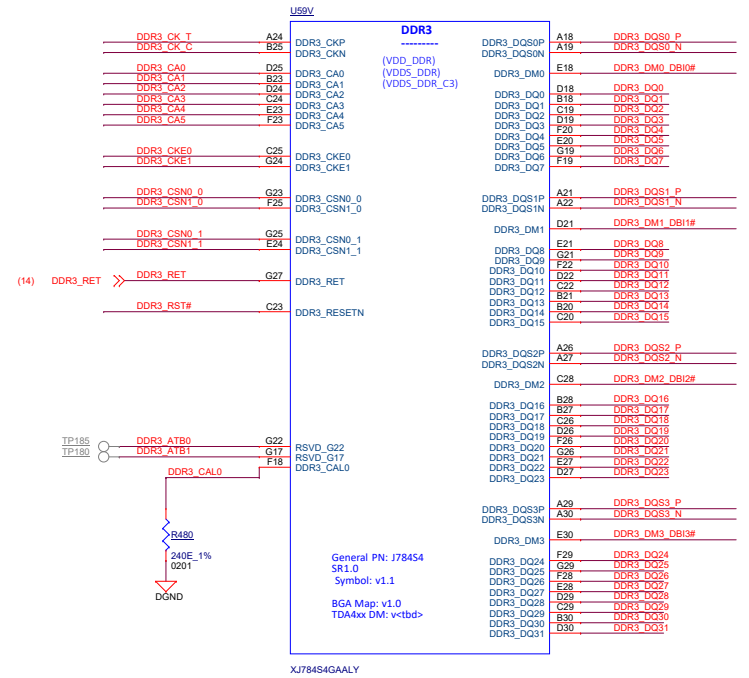
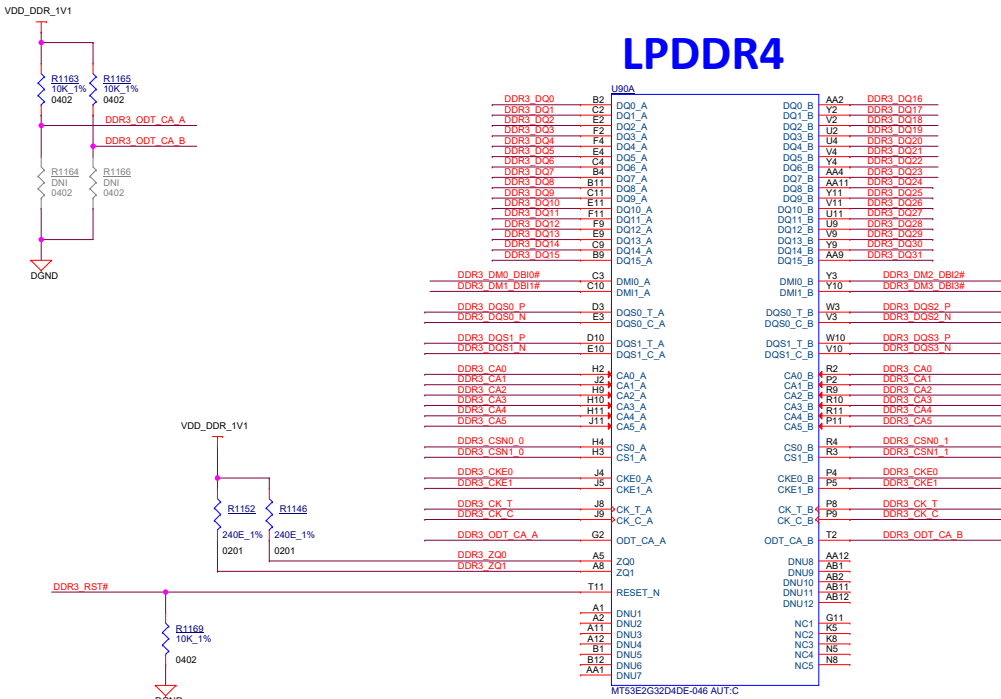
LPDDR4



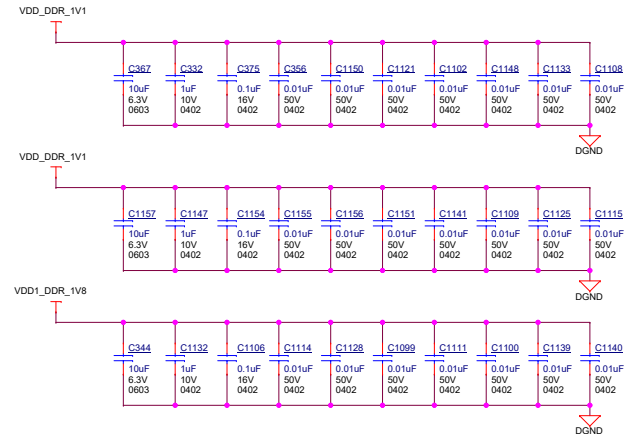
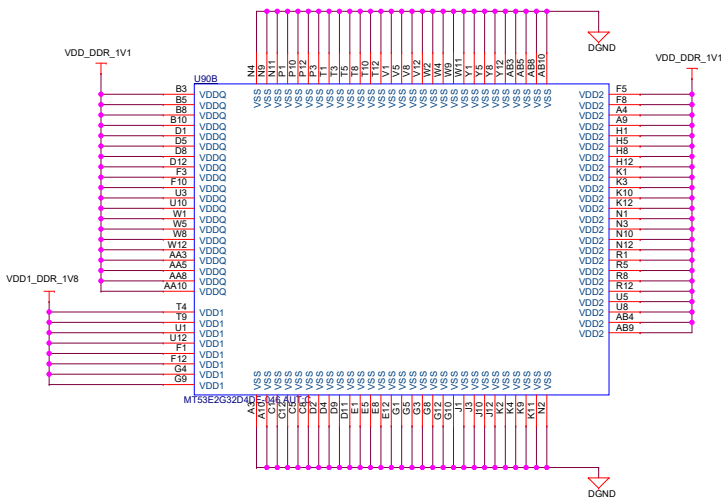
**DDR 1.8V Dcaps could be reduced.
Check on latest Micron recmd's for new PN.**



LPDDR4

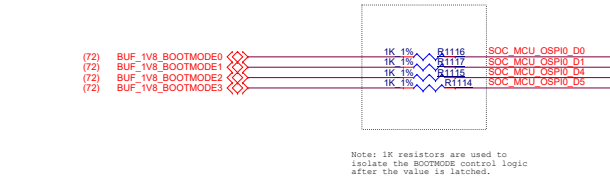
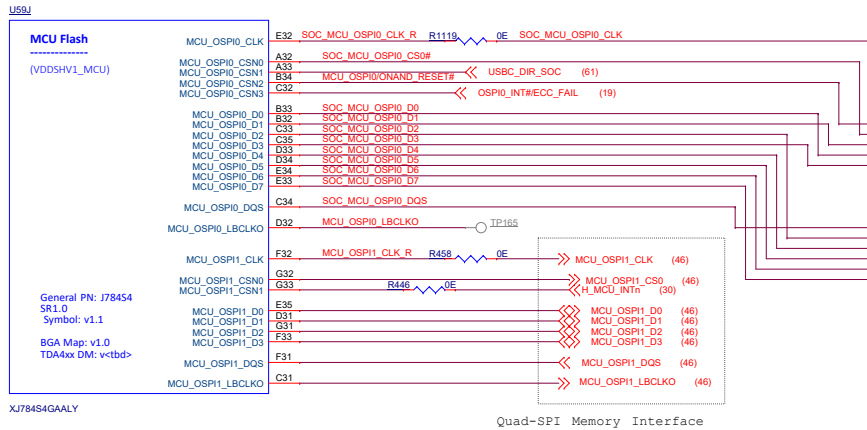


DDR 1.8V Dcaps could be reduced.
Check on latest Micron recmd's for new PN.

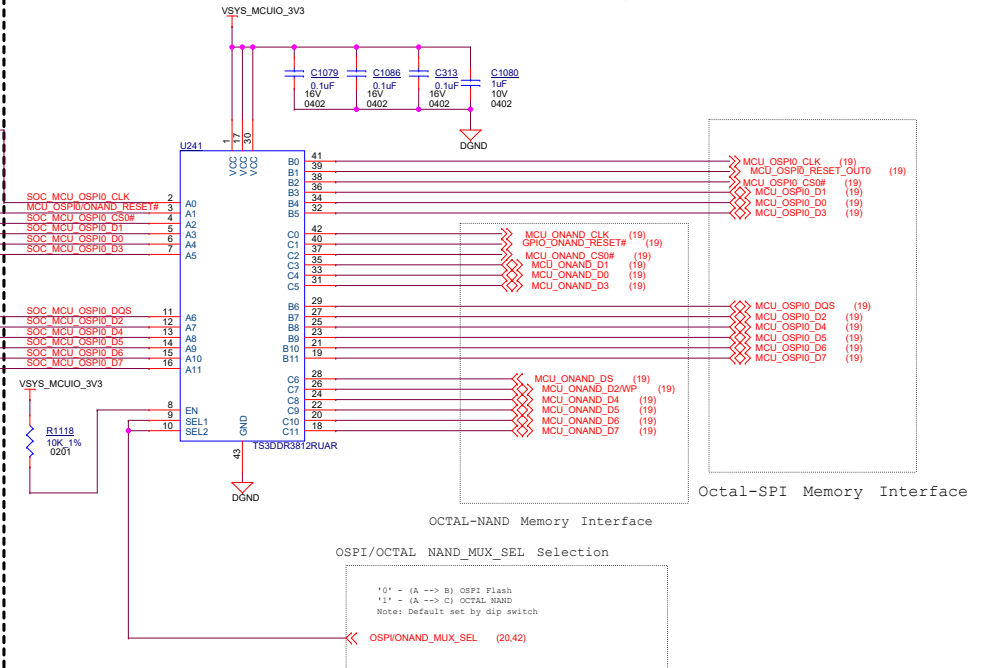


Project : J7 EVM		Title EMIF3	
Size PROC141 001 J78454XG01EVM		Rev E3	
Date: Monday, September 12, 2022		Sheet 17 of 88	

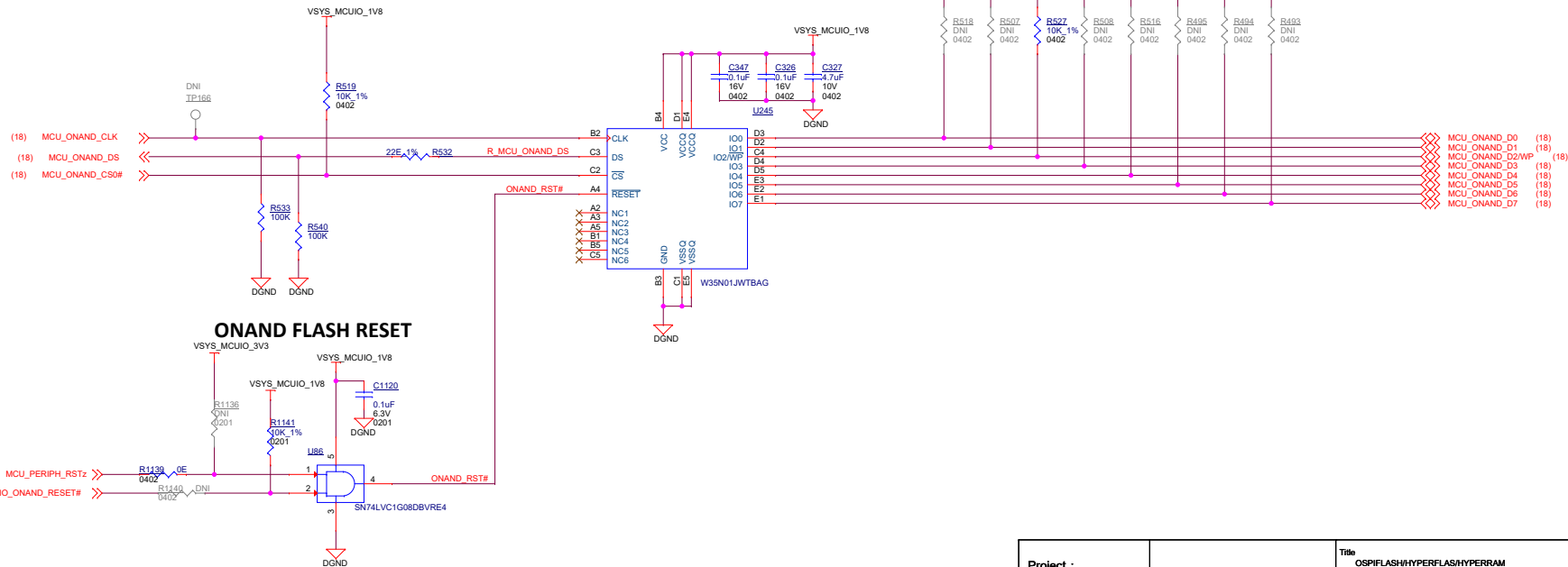
MCU FLASH



EVM development & evaluation test circuitry (TI EVM Only) 2:1 Mux for OSPI/OCTAL NAND

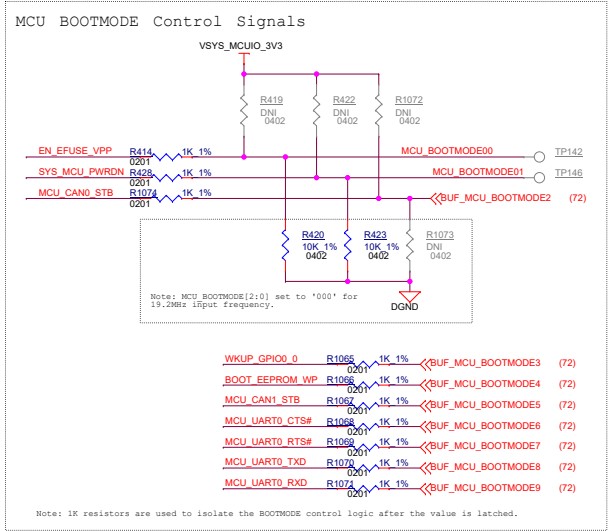
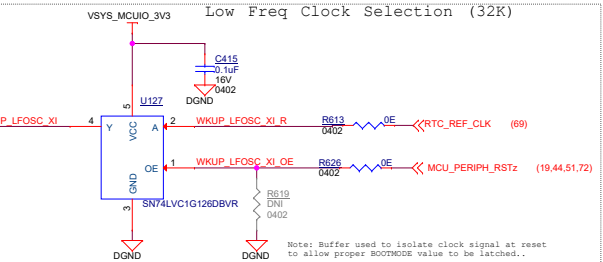
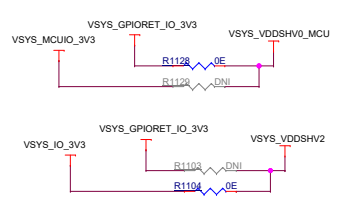
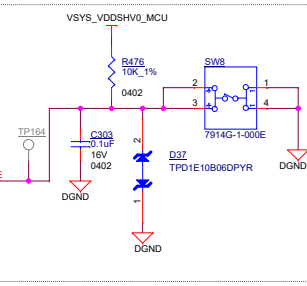
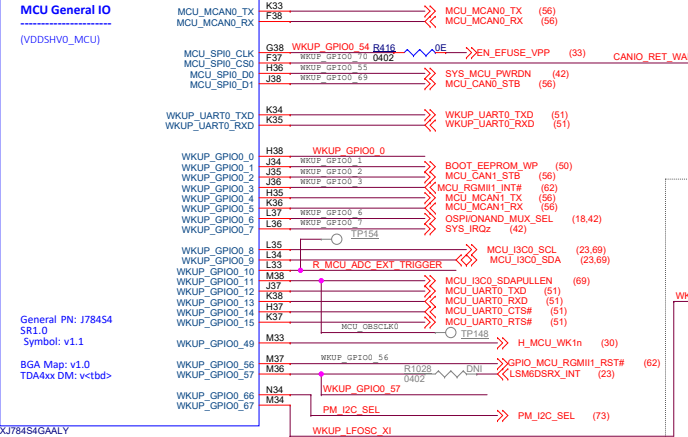


OCTAL NAND



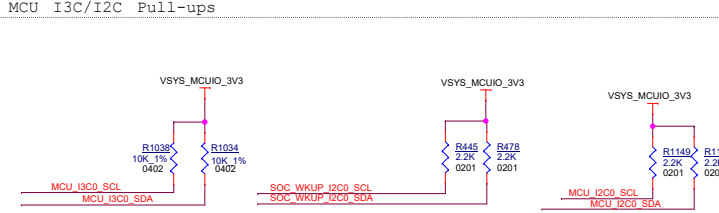
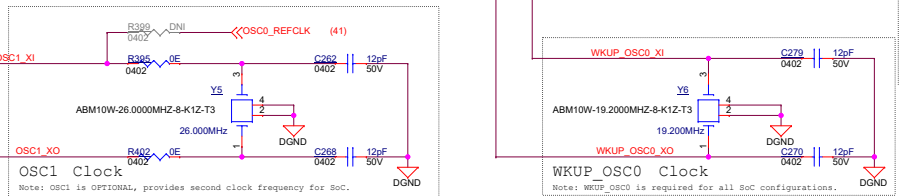
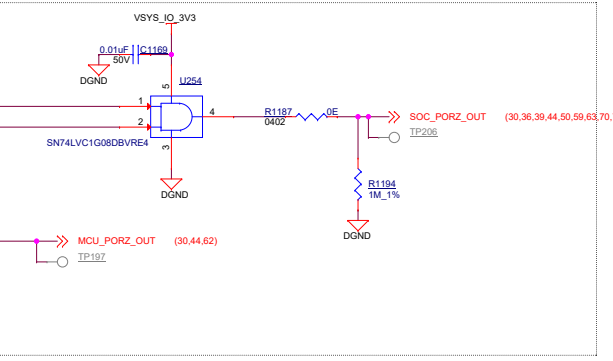
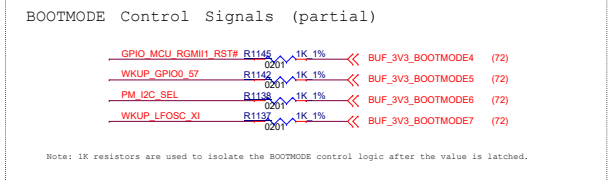
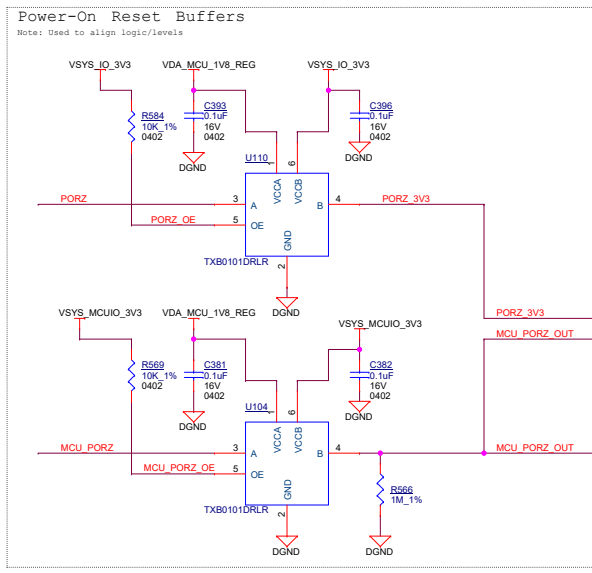
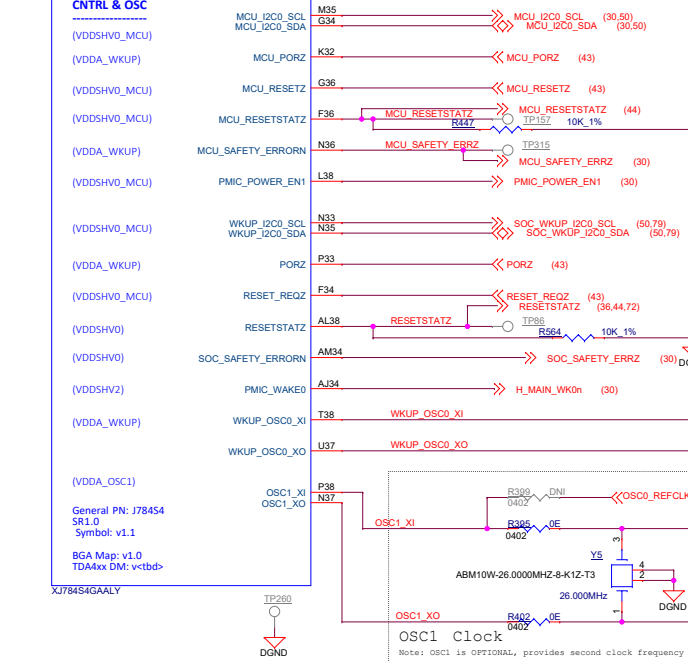
MCU & MAIN GENERAL IO, OSC CLKs

U58

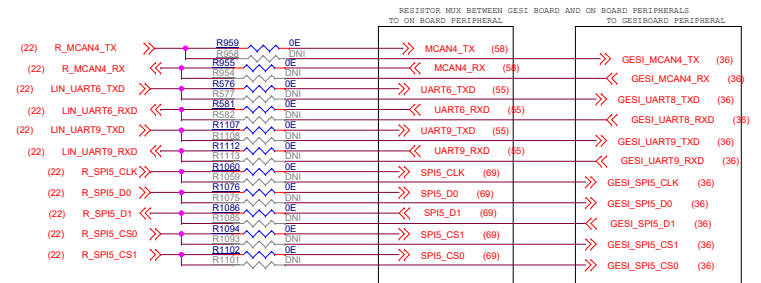
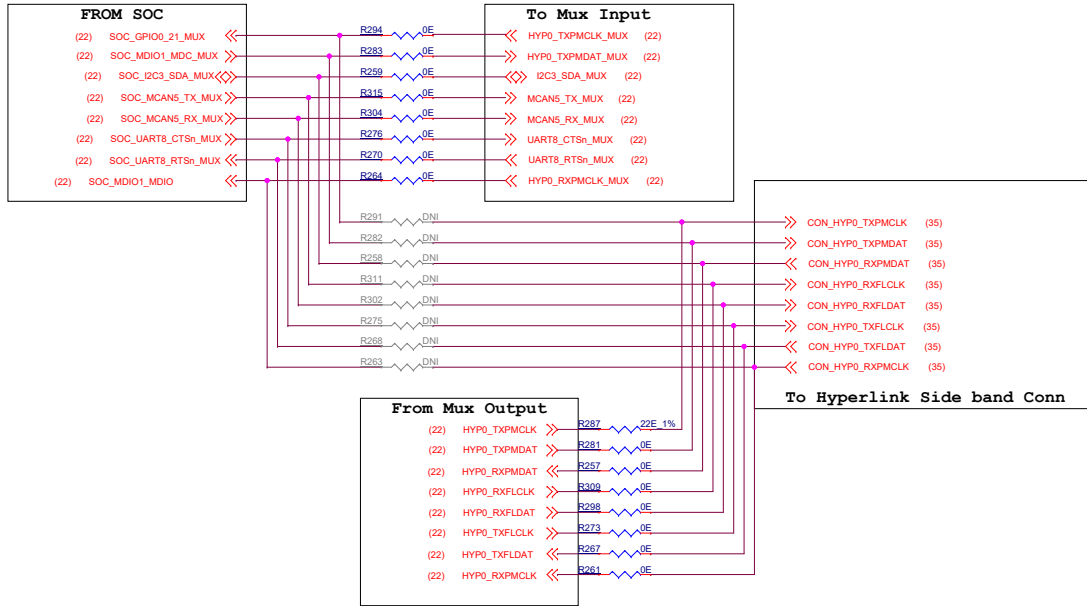


CONTROL & OSC

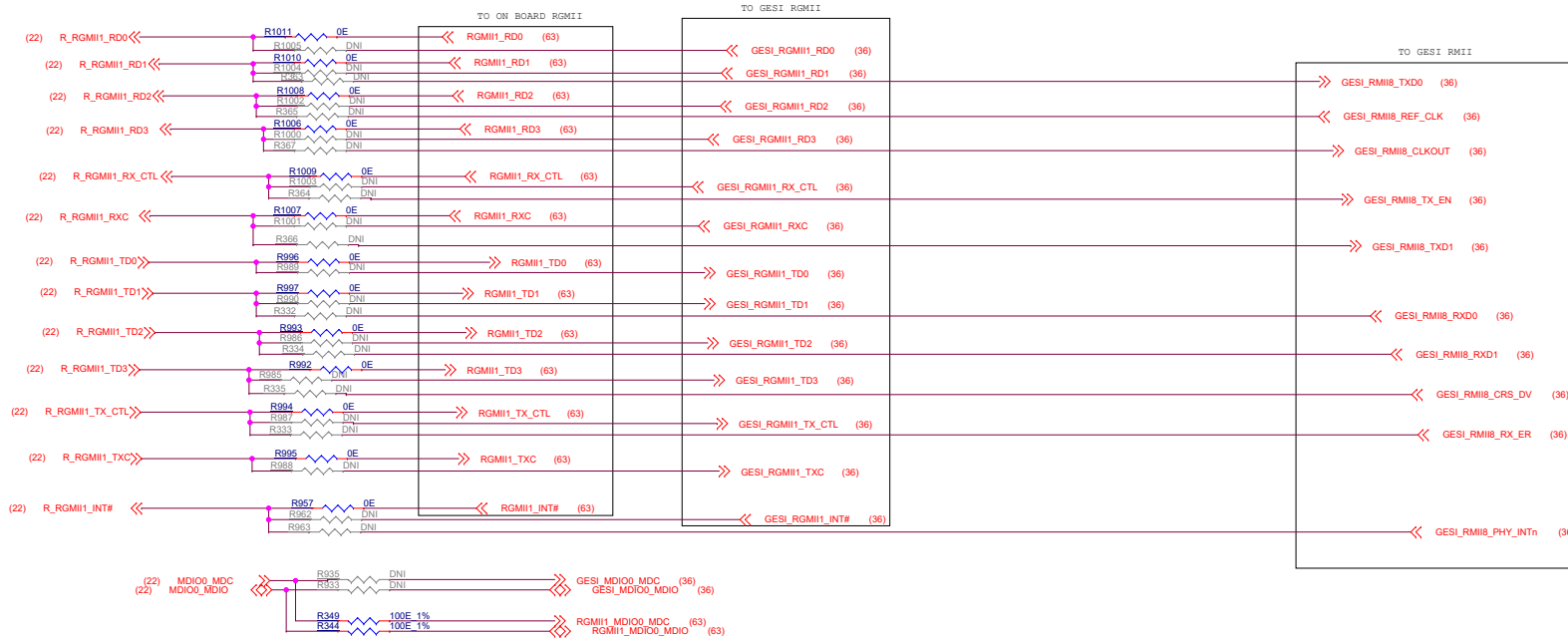
U58D



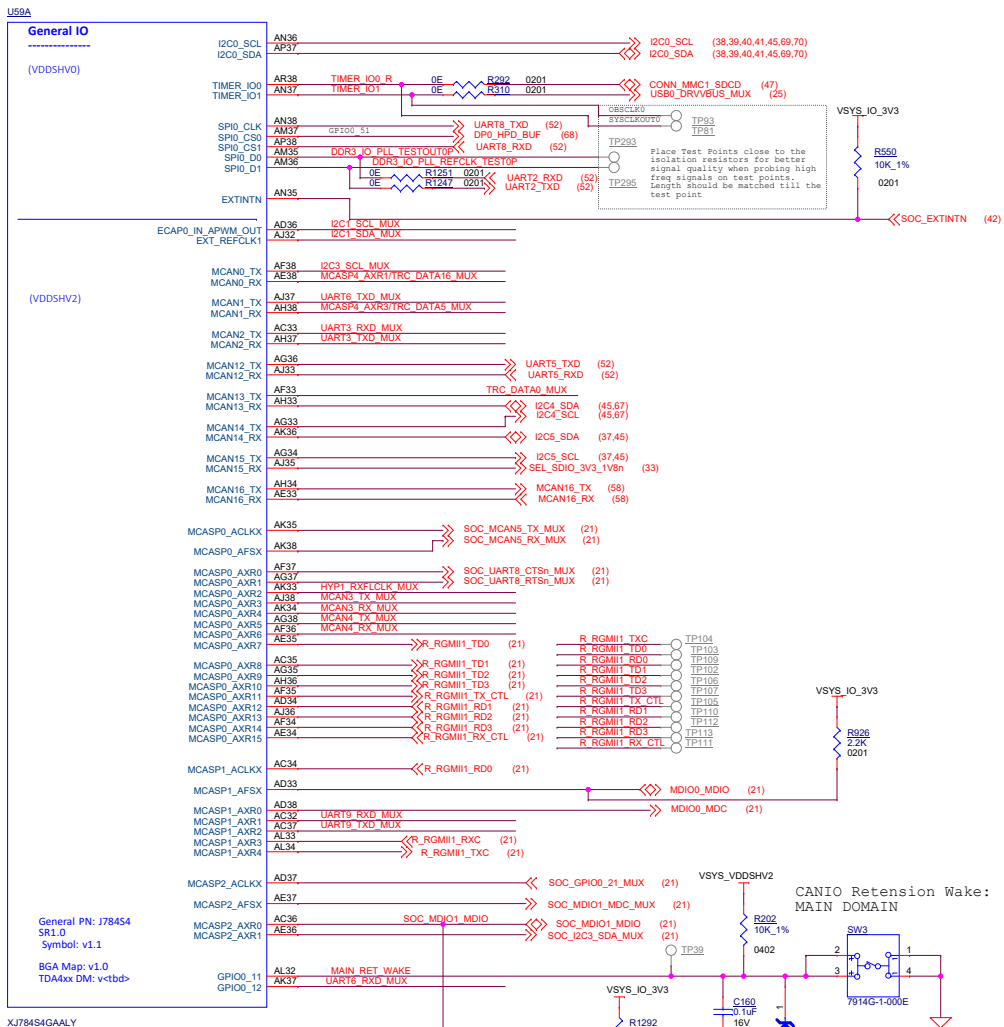
Resistor Mux option to By-pass MUX for Hyperlink sideband signals



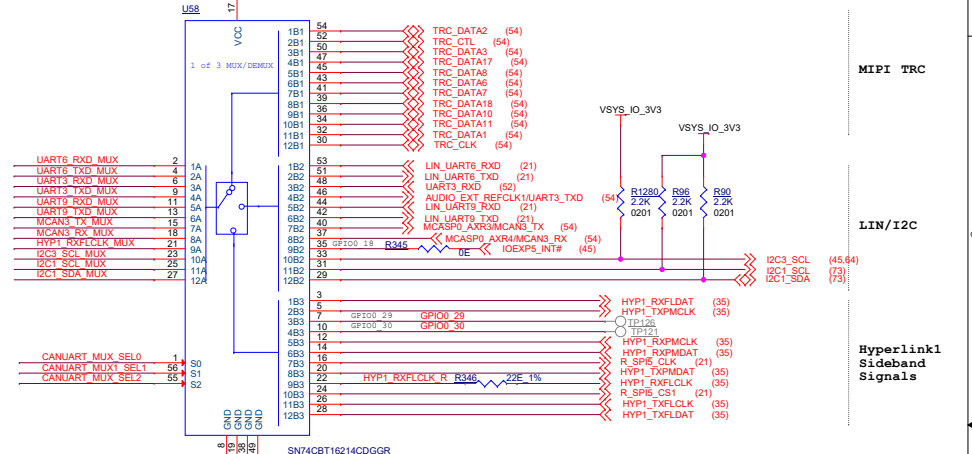
RESISTOR MUX BETWEEN ON BOARD RGMII AND GESI RMII



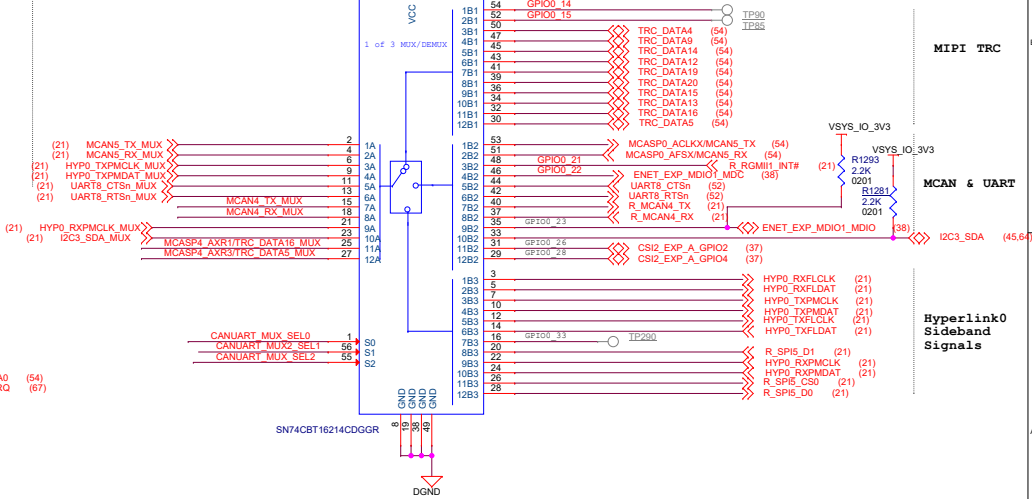
GENERAL IO



MUX1



MUX2



HYPERLINK/TRACE/MCAN/LIN - 1:3 MUX : Truth Table

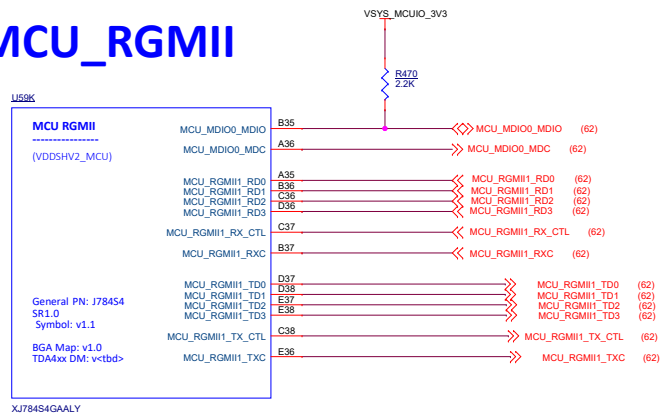
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port

(default)

Project : J7 EVM		Title: GENERAL IO	
Size	PROC141 001 J78454XG01EVM	Rev	E3
C			
Date:	Wednesday, July 27, 2022	Sheet	22 of 88



MCU_RGMII



MMC0 and MMC1



MCU_ADC

Place Beads, 0402 Cs & 0E Rs
outside SoC at FP edge
BOM = Install 0E Rs as default

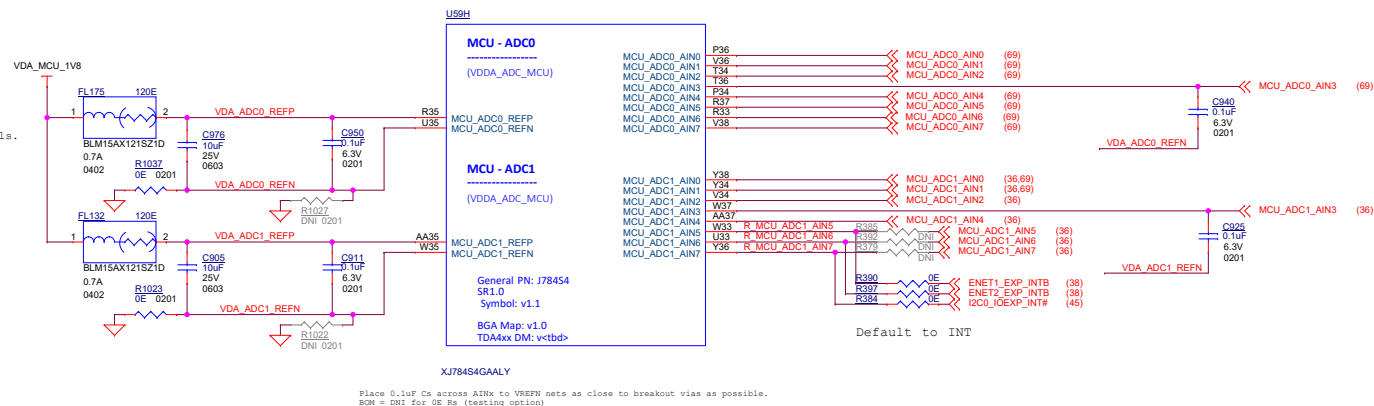
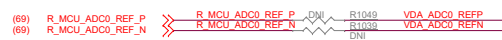
Place 0.1uF Cs across bkout vias & OE Rs
next to Dcaps under SoC
BOM = DNI for OE Rs (testing option)

```

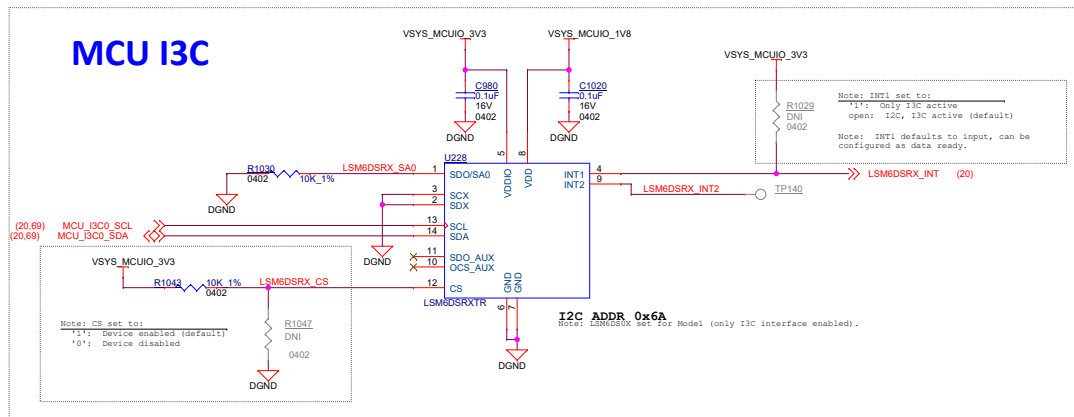
ADC 0 & 1 Filtering Scheme:
ADC0/1 VREF P have 2x independent input balls with same
in-line supply filtering as common VDA ADC_V8 pwr rail
(Provisioned supply filtering for PCB layout pending
feedback from TI analog design team)
-1x Ferrite bead to filter & reduce noise
-1x 0402 (2.2-10uF), SoC perimeter/near end
-1x 0201 for U.IuF pwr pwr ball, far end
-1x 0201 OE R to optional short REFN to board GND
(as area under SoC allows)

```

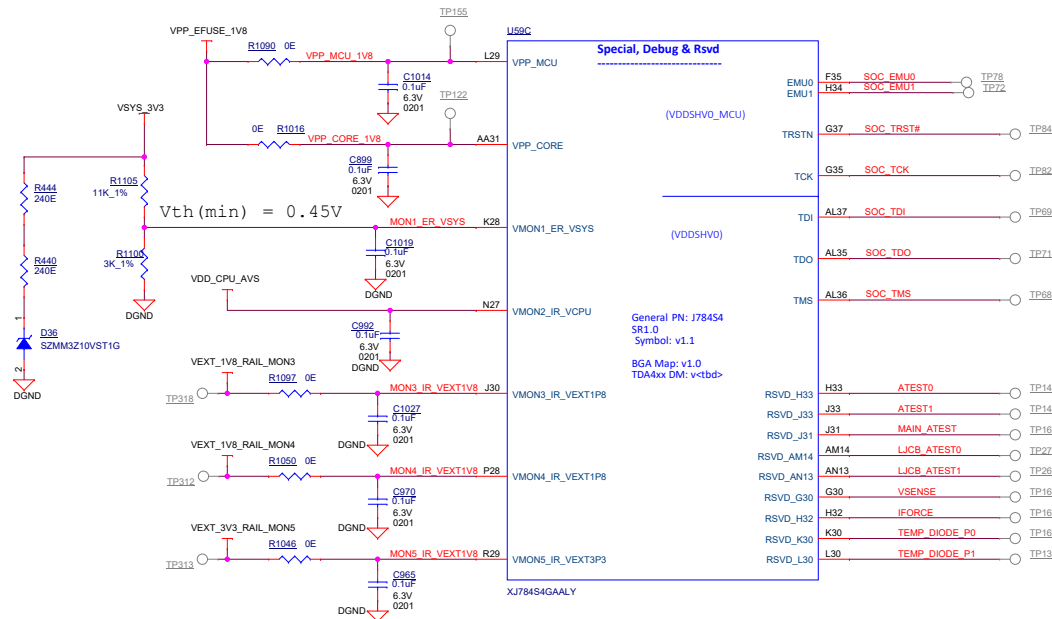
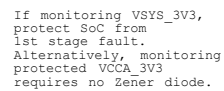
Place R5130 near FL358
Place R5131 near R2369



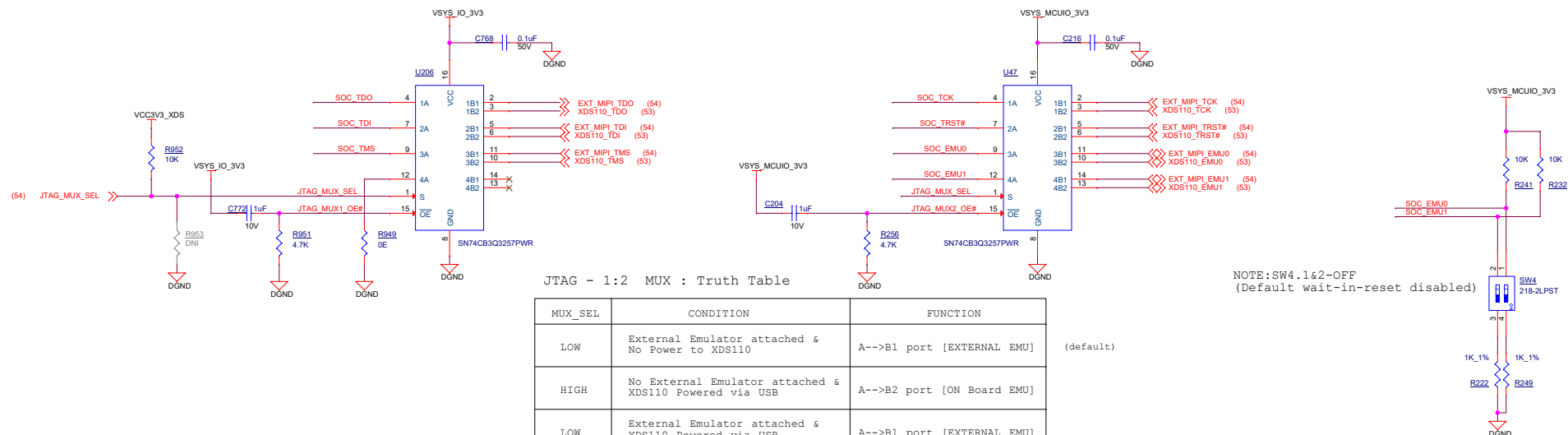
MCU I3C



SPECIAL, DEBUG & RSVD



JTAG AND TRACE MUX



JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]

NOTE:SW4.1&2-OFF
(Default wait-in-reset disabled)

By Pass USB MUX	Mount - R796, R795, R774, R775 DNI - R57, R56, R30, R29
USB MUX (Default)	Mount - R57, R56, R30, R29 DNI - R796, R795, R774, R775

The schematic diagram illustrates the USB2.0 MUX circuit. It features a USB0 block (XJ7845GAALY) connected to a USB2.0 MUX (U177) and a USB HUB (U178). The USB0 block provides signals for USB0_DP, USB0_DM, USB0_ID, and USB0_VBUS. The USB2.0 MUX is controlled by USB2.0_MUX_SEL and USB2.0_MUX_OEn. The USB HUB is connected to the USB2.0 MUX and provides signals for USB1_HUB_D_P, USB1_HUB_D_N, USB1_VBUS_SOC, and USB1_DRVVBUS. The circuit also includes various passive components like resistors (R138, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802

Note: Recommended VBUS circuit for USB connector. Supports 5V-10V VBUS

USB0_VBUS_SOC 16.5K 1% R13 3.4K 1% R9 VBUS_USBC_CONN (61)

R14 10K 1% 0402 DGNND

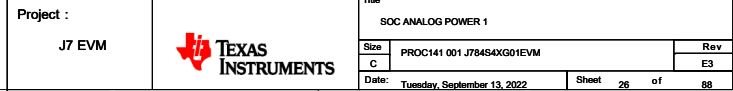
U3 BZX84C6V8LT1G

Note: Recommended VBUS circuit for embedded Hub

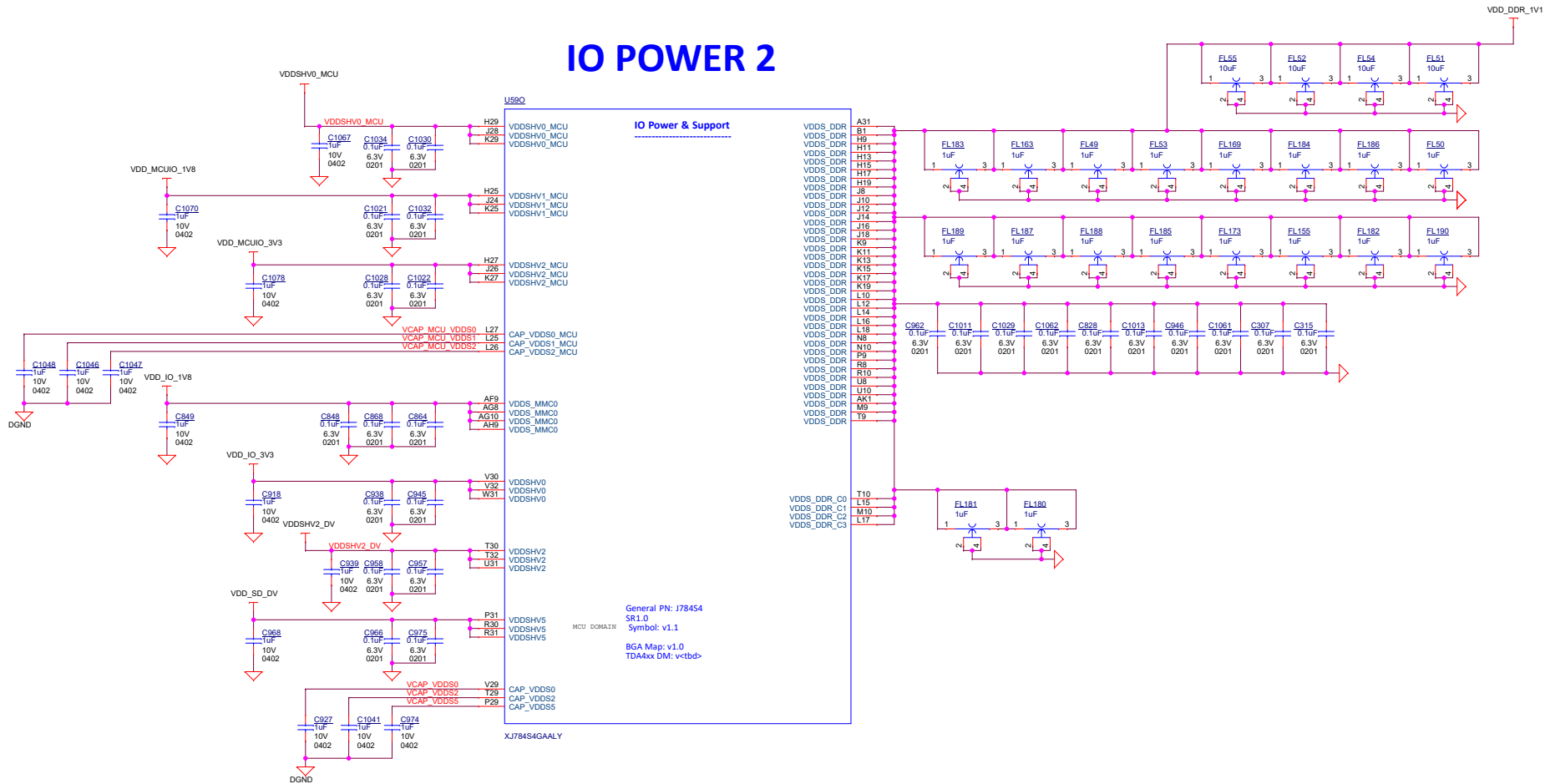
USB1_VBUS_SOC 9.09K 1% R0804 USB1_VBUS (59)

R0804 10K 1% 0402 DGNND

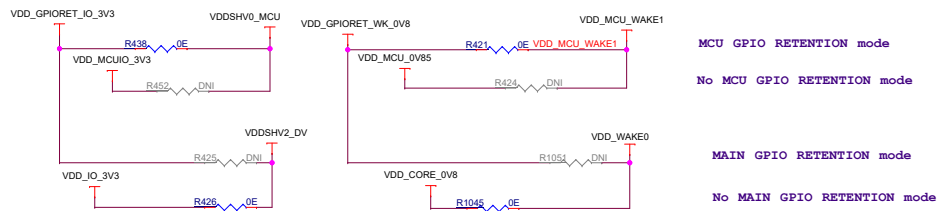
VDDA_0P8_CSIRX0_1



IO POWER 2



EVM development & evaluation Test circuitry
EVM GPIO Retention testing option
(TI EVM Only)



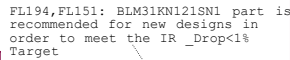
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).


Low power modes	Resistors to be Populated	Resistors to be DNI'd
No GPIO RET	R452,R424,R426,R1045	R438,R421,R425,R1051
MCU GPIO RET only	R438,R421,R426,R1045	R452,R424,R425,R1051
MAIN GPIO RET only	R452,R424,R425,R1051	R438,R421,R426,R1045
MCU & MAIN GPIO RET	R438,R421,R425,R1051	R452,R424,R426,R1045

Digital Power

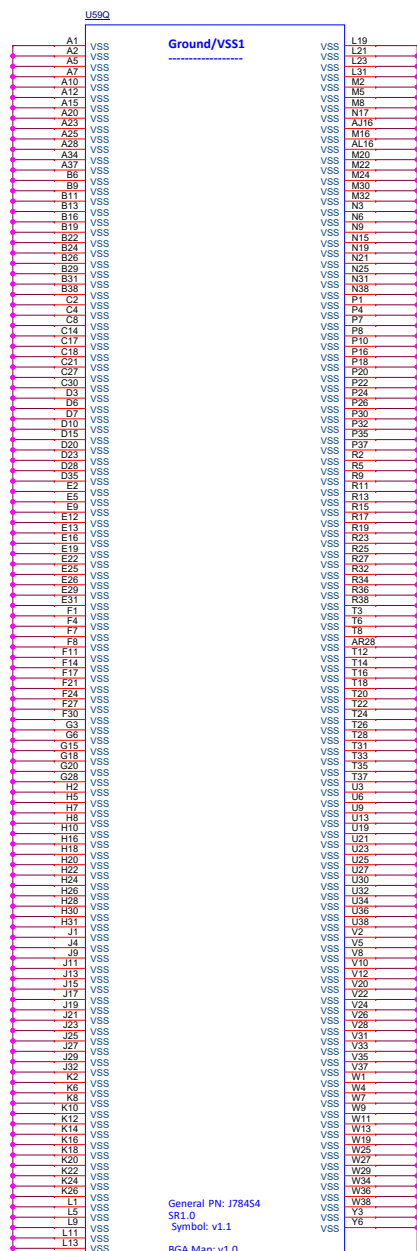


A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).

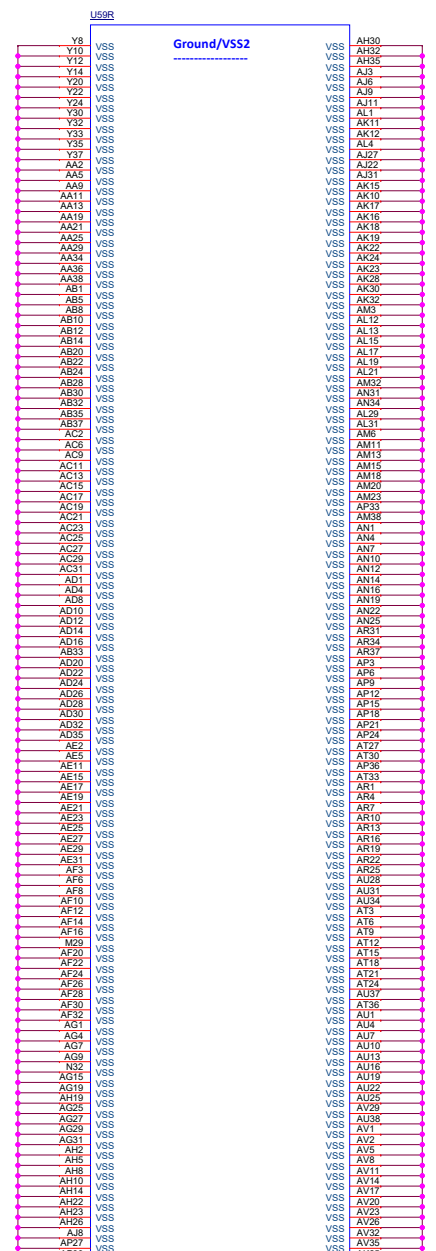
Project : J7 EVM		Title SOC DIGITAL POWER 3		
		Size	PROC141 001 J7B4S4XG01EVM	
		C		
			Rev E3	
		Date:	Thursday, September 15, 2022	Sheet 28 of 88

SOC GROUND



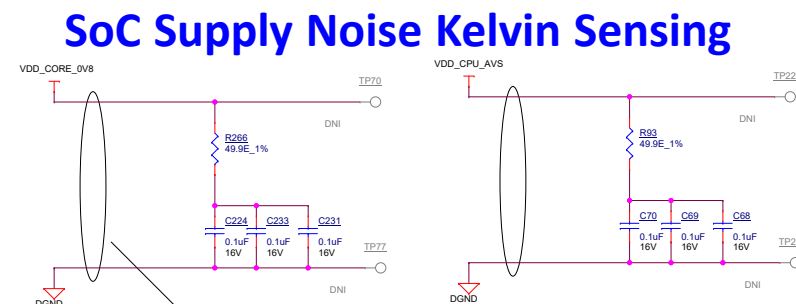
General PN: J78454
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: y<tb>

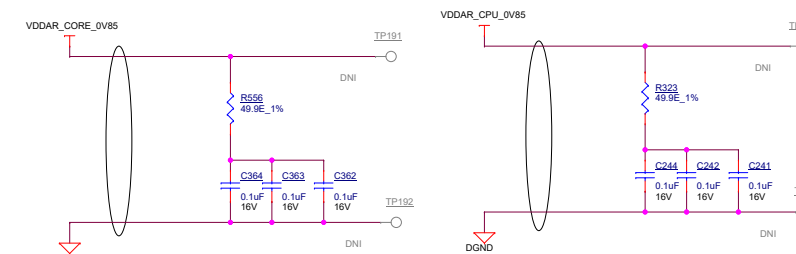
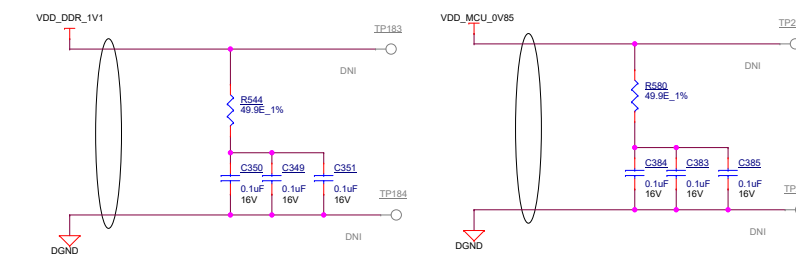


General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: v<td>



Route supply & Gnd connections from SoC PoL as a pseudo differential pair to TPs near R & C termination for easy access



PMIC

"PCB Notes":

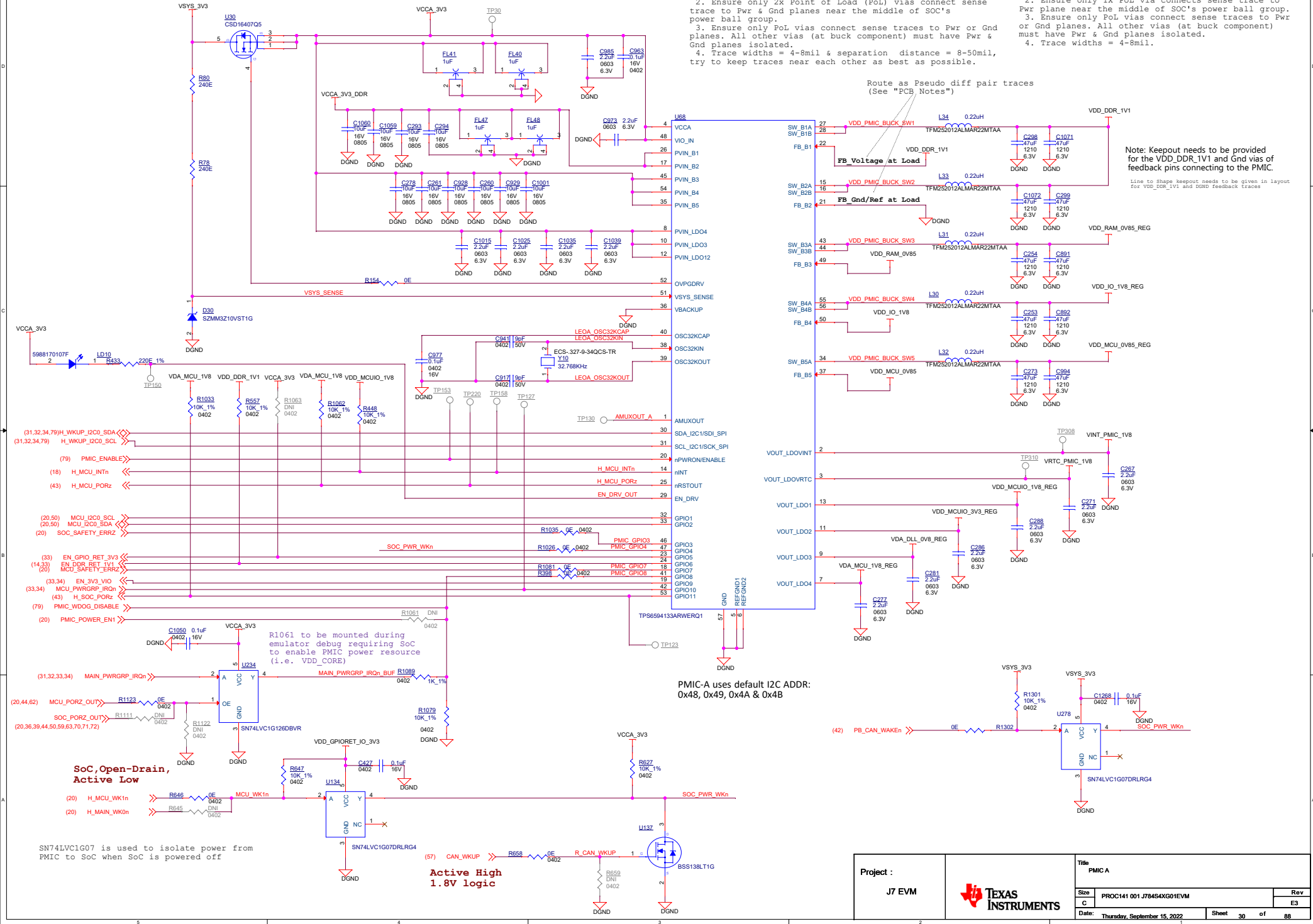
- For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
 2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
 3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
 4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

- For single-phase Buck converter configs, route remote sense feedback as follows:
1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
 2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
 3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
 4. Trace widths = 4-8mil.

Route as Pseudo diff pair traces (See "PCB Notes")

Note: Keepout needs to be provided for the VDD_DDR_1V1 and Gnd vias of feedback pins connecting to the PMIC.

Line to Shape keepout needs to be given in layout for VDD_DDR_1V1 and GND feedback traces

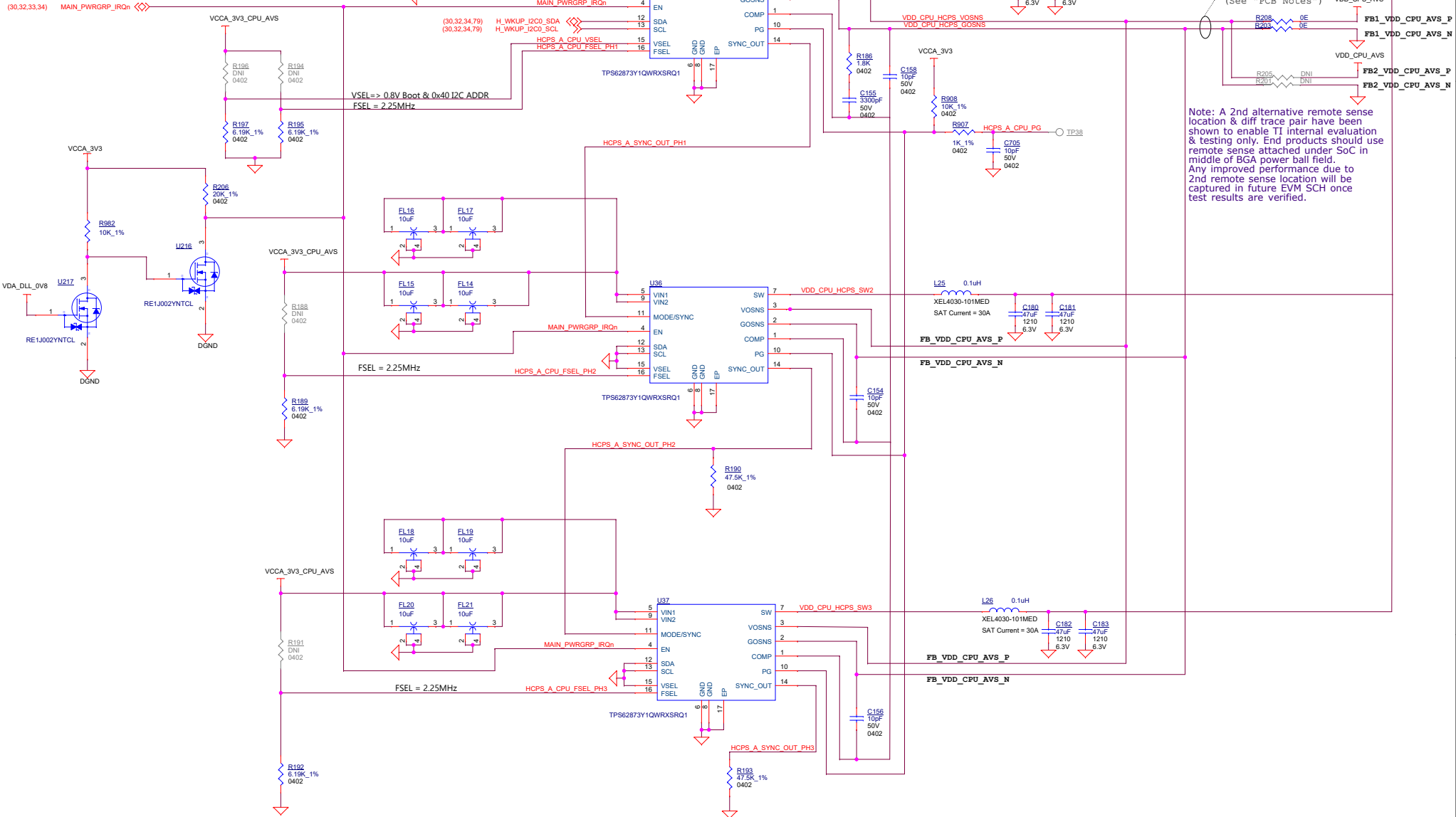


VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD_XXX_HCPS_VOSNS"/_GOSNS") both at the buck & along diff trace routing path between buck "xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

Line to Shape keepout needs to be given in layout for VDD_CPU_AVS and DGND feedback traces

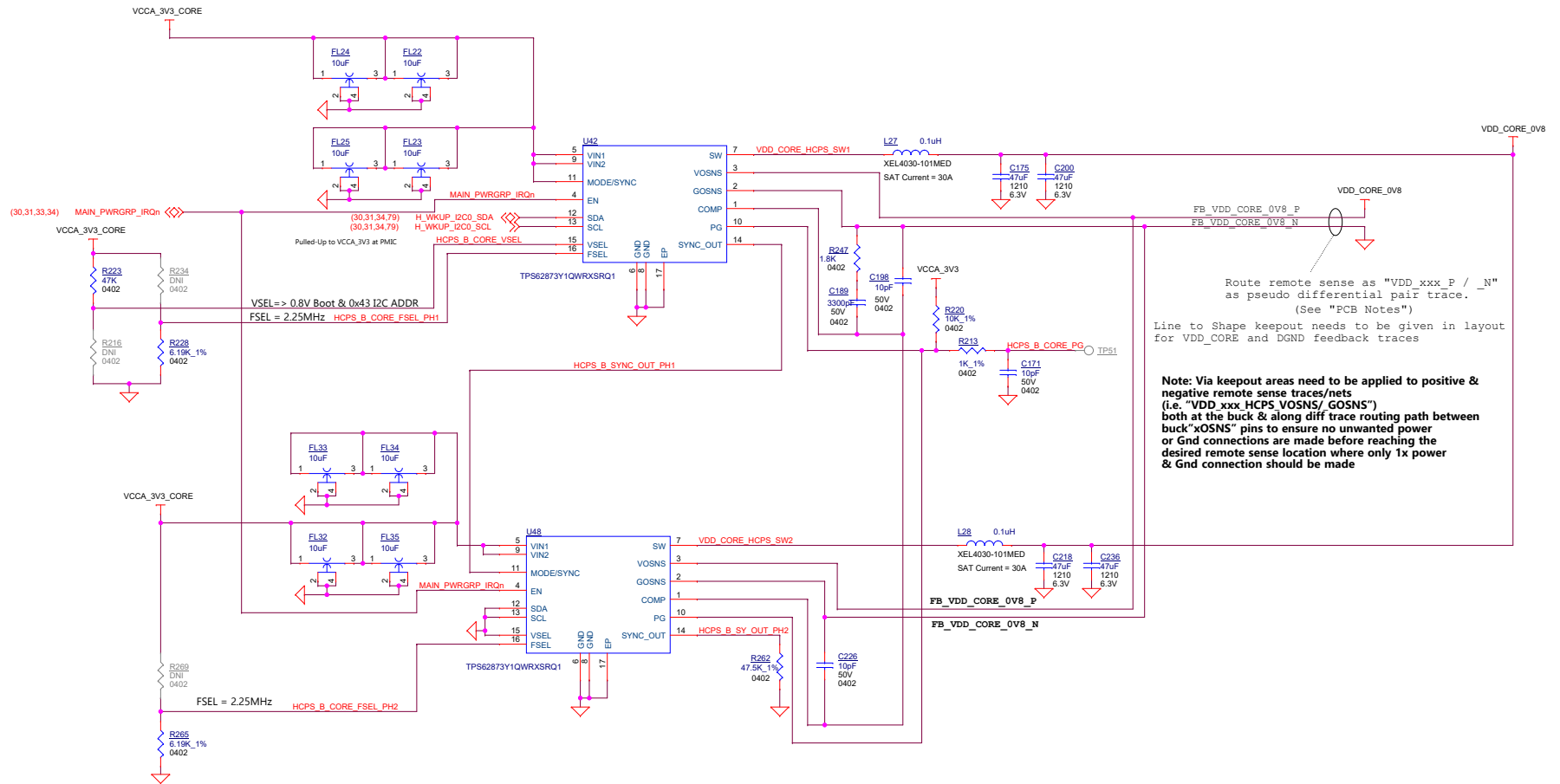
Buck EN control aligned to VDA_DLL_OV8 for power seqs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.



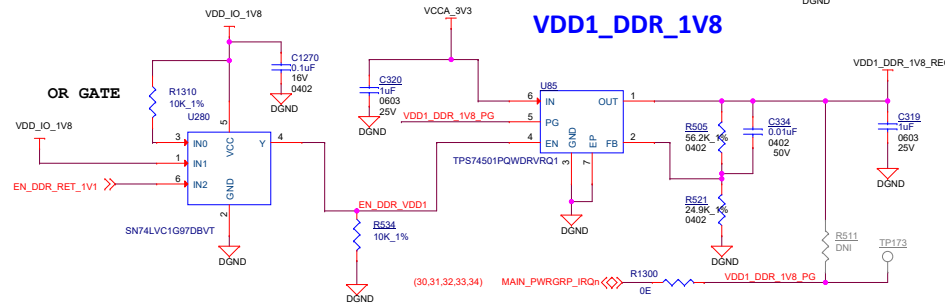
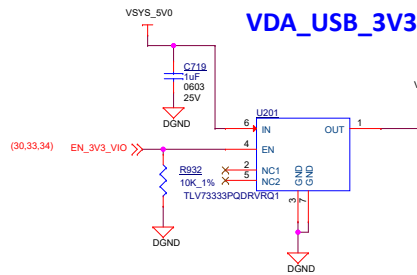
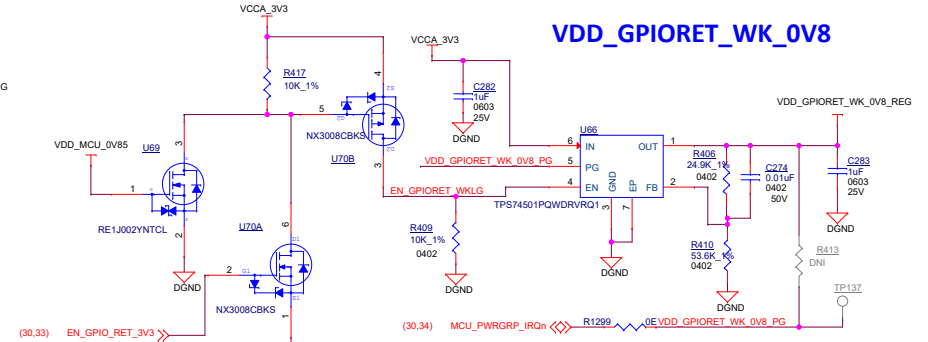
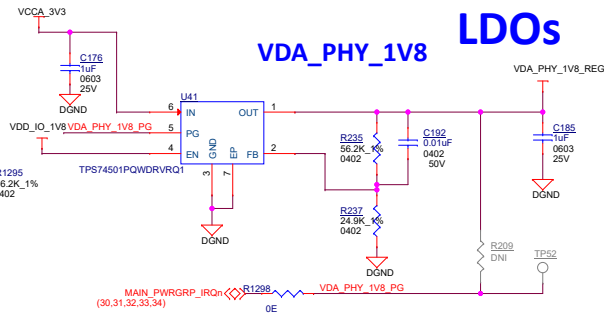
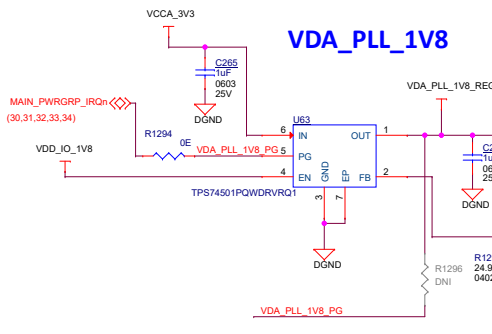
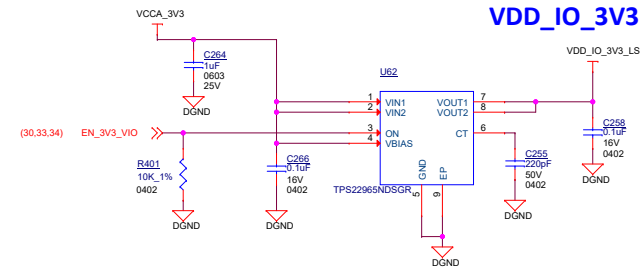
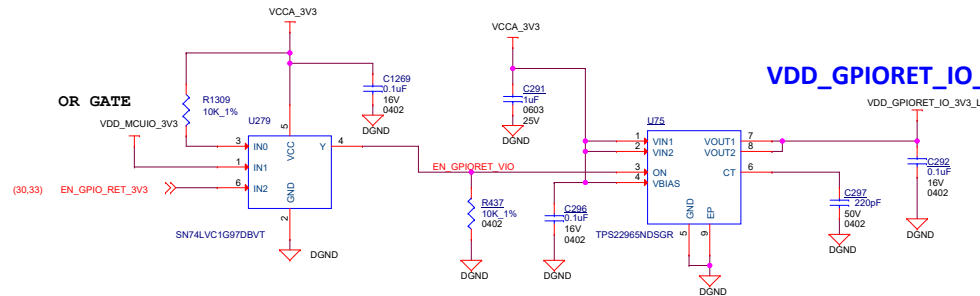
Note: A 2nd alternative remote sense location & diff trace pair have been shown to enable TI internal evaluation & testing only. End products should use remote sense attached under SoC in middle of BGA power ball field. Any improved performance due to 2nd remote sense location will be captured in future EVM SCH once test results are verified.

Project : J7 EVM		Title HCPS A	
Size PROC141 001 J78454XG01EVM		Rev E3	
Date: Wednesday, July 27, 2022		Sheet 31 of 88	

VDD_CORE_OV8 High-Current Power Stage A (HCPS-B)

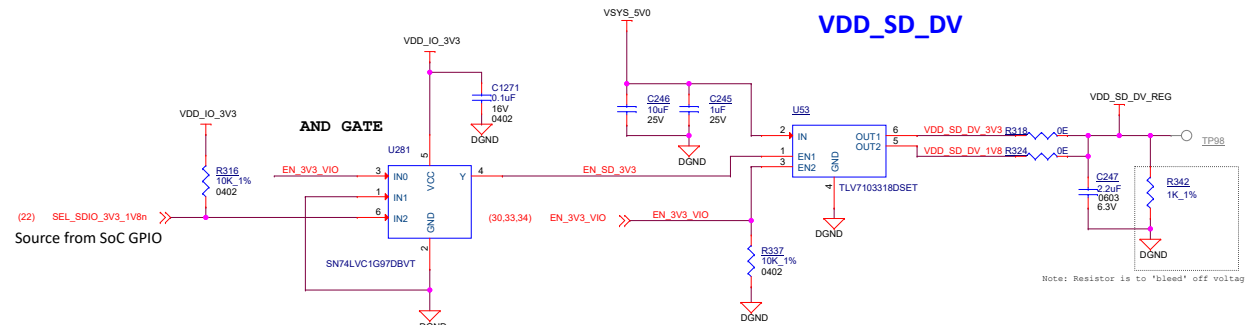
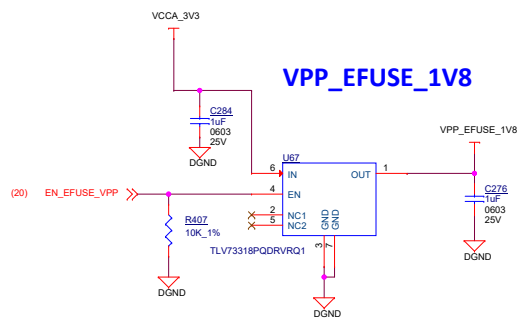


LOAD SWITCHES



EN_GPIORET_VIO & EN_GPIORET_WKLG & EN_DDR_VDD1 Truth table

"OR" Gate Logic			States		
X	Y	OUTPUT	Input - X	Input - Y	Output
0	0	0	OFF	OFF	OFF
0	1	1	OFF	ON	ON
1	0	1	ON	OFF	ON
1	1	1	ON	ON	ON



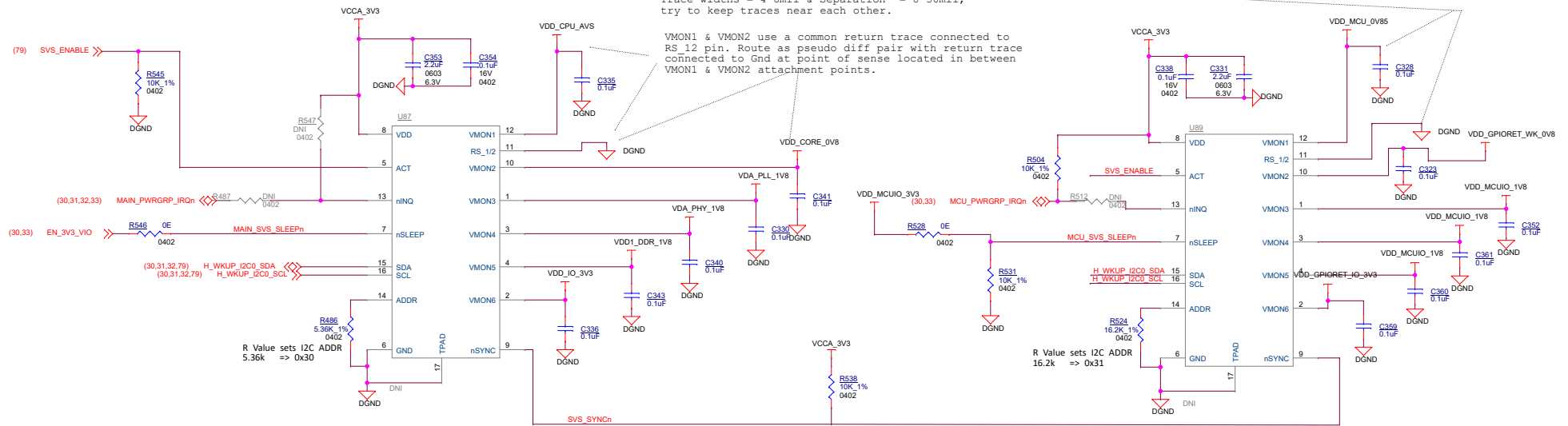
Note: Resistor is to 'bleed' off voltage.

Safety Voltage Supervisors

Power rail voltage > 1.0V can connect to VMON3-6 inputs using single-ended traces.
Trace widths = 4-8mil, as short as possible & try to avoid routing near HF signals.

Any power rail voltage < 1.0V should connect to VMON1 & VMON2 inputs using "Pseudo Diff Pair Trace" routes.
Trace widths = 4-8mil & Separation = 8-50mil, try to keep traces near each other.

VMON1 & VMON2 use a common return trace connected to RS 12 pin. Route as pseudo diff pair with return trace connected to Gnd at point of sense located in between VMON1 & VMON2 attachment points.



HYPERLINK SIDEBAND CONNECTOR

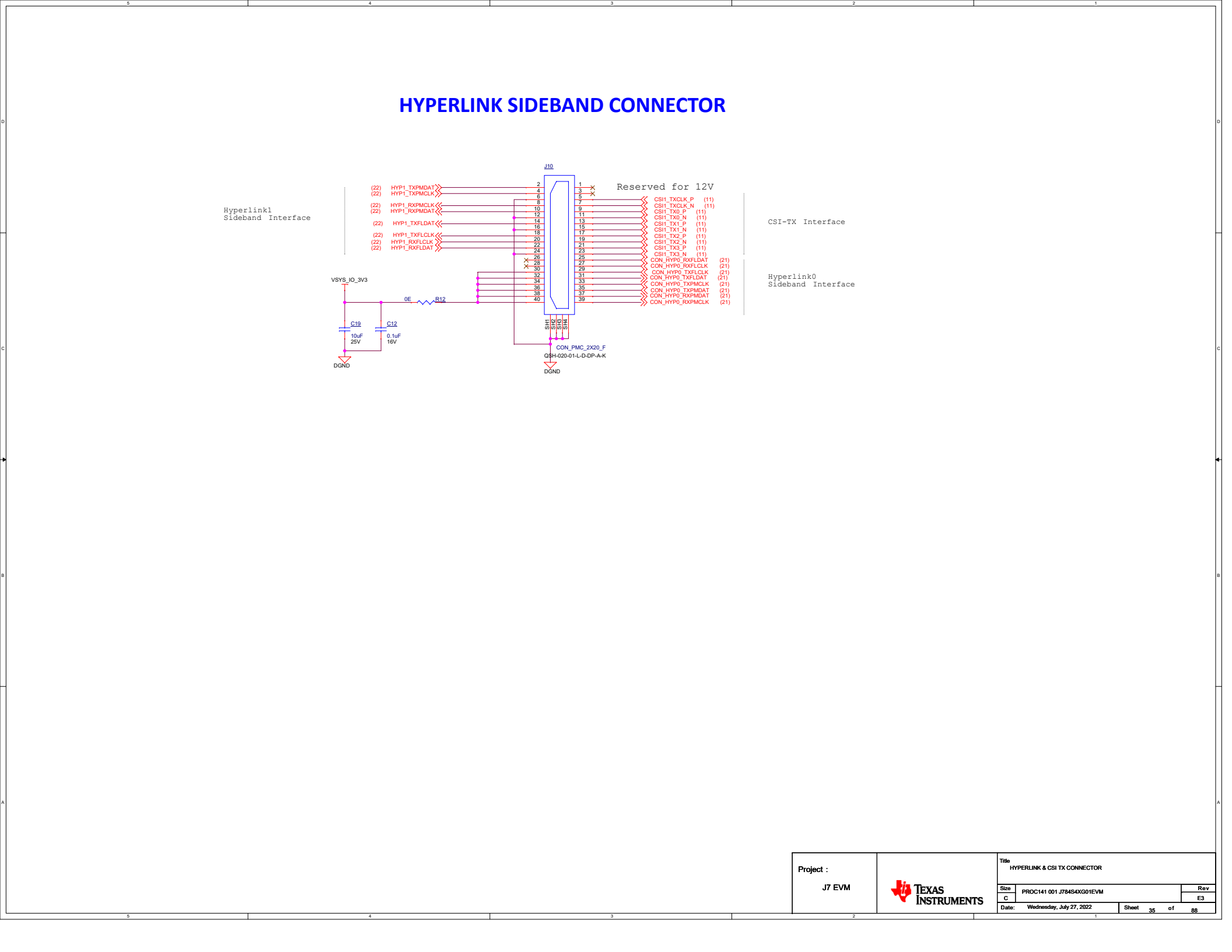
The diagram illustrates the pin configuration and signal connections for the Hyperlink Sideband Connector (J10). The connector is a 40-pin component with pins numbered 1 to 40. The connections are as follows:

- Hyperlink1 Sideband Interface:**
 - Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24: HYP1_TXPMDAT (22), HYP1_TXPMCLK (22), HYP1_RXPMCLK (22), HYP1_RXPMDAT (22), HYP1_TXFLDAT (22), HYP1_TXFLCLK (22), HYP1_RXFLCLK (22), HYP1_RXFLDAT (22).
- Reserved for 12V:**
 - Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39: Reserved for 12V.
- CSI-TX Interface:**
 - Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39: CSI_TXCLK_P (11), CSI_TXCLK_N (11), CSI_TX0_P (11), CSI_TX0_N (11), CSI_TX1_P (11), CSI_TX1_N (11), CSI_TX2_P (11), CSI_TX2_N (11), CSI_TX3_P (11), CSI_TX3_N (11).
- Hyperlink0 Sideband Interface:**
 - Pins 26, 28, 30, 32, 34, 36, 38, 40: CON_HYP0_RXFLDAT (21), CON_HYP0_RXFLCLK (21), CON_HYP0_TXFLCLK (21), CON_HYP0_TXFLDAT (21), CON_HYP0_TXPMCLK (21), CON_HYP0_TXPMDAT (21), CON_HYP0_RXPMDAT (21), CON_HYP0_RXPMCLK (21).

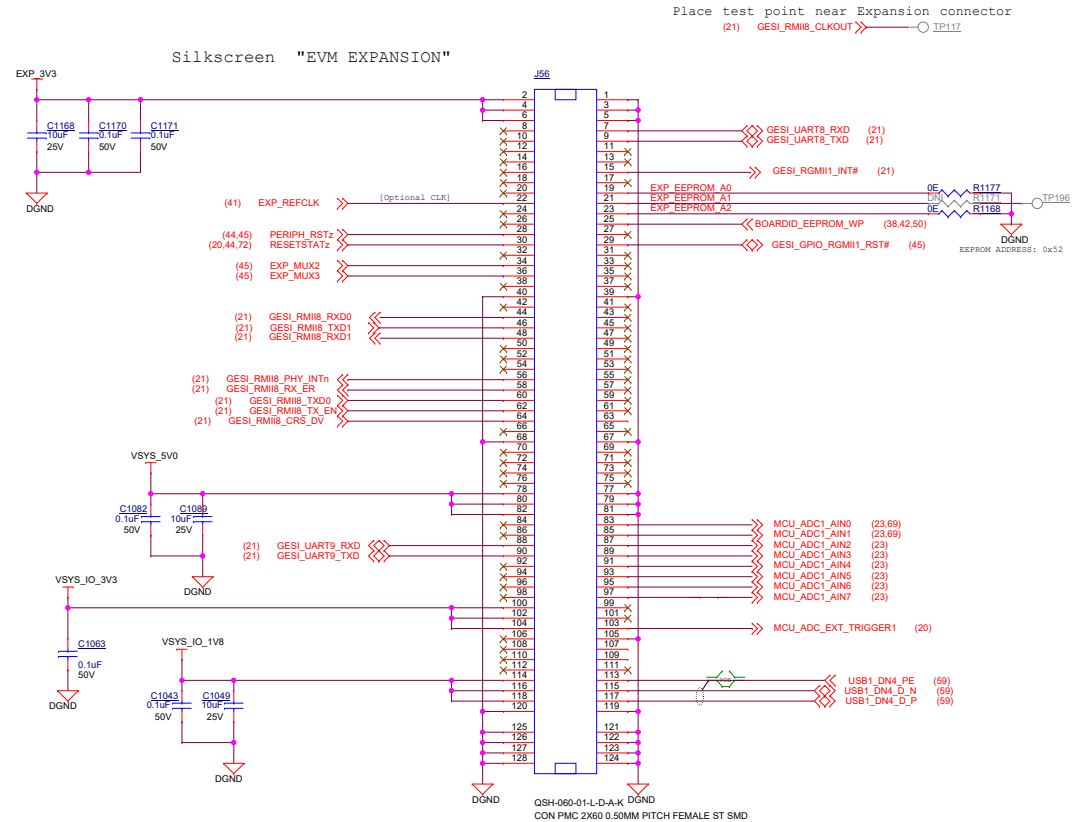
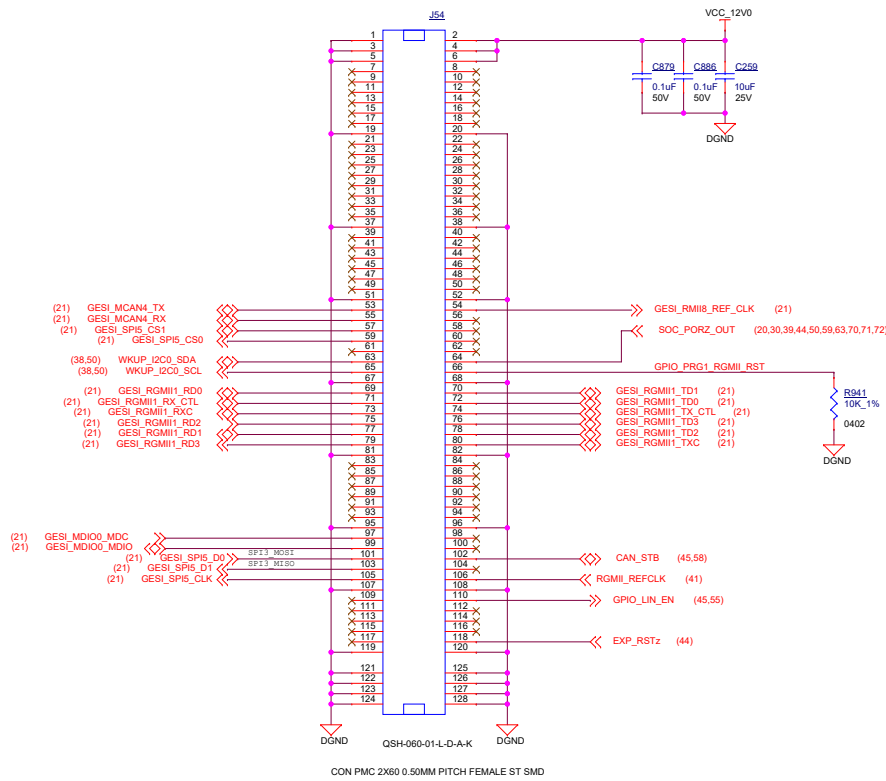
Additional components and connections include:

- Power and Grounding:** VSYS_IO_3V3 is connected to pin 10. A 10µF 25V capacitor (C19) and a 0.1µF 16V capacitor (C12) are connected to pin 10 and ground (DGND). A 0Ω resistor (R12) is connected to pin 10.
- Connector:** J10 is a 40-pin connector with pins numbered 1 to 40.
- Component:** CON_PMC_2X20_F is a 2x20 pin connector with pins numbered 1 to 20.

Project :		Title	
J7 EVM		HYPERLINK & CSI TX CONNECTOR	
		Size	PROC141 001 J78454XG01EVM
		Rev	E3
Date: Wednesday, July 27, 2022		Sheet	35 of 88



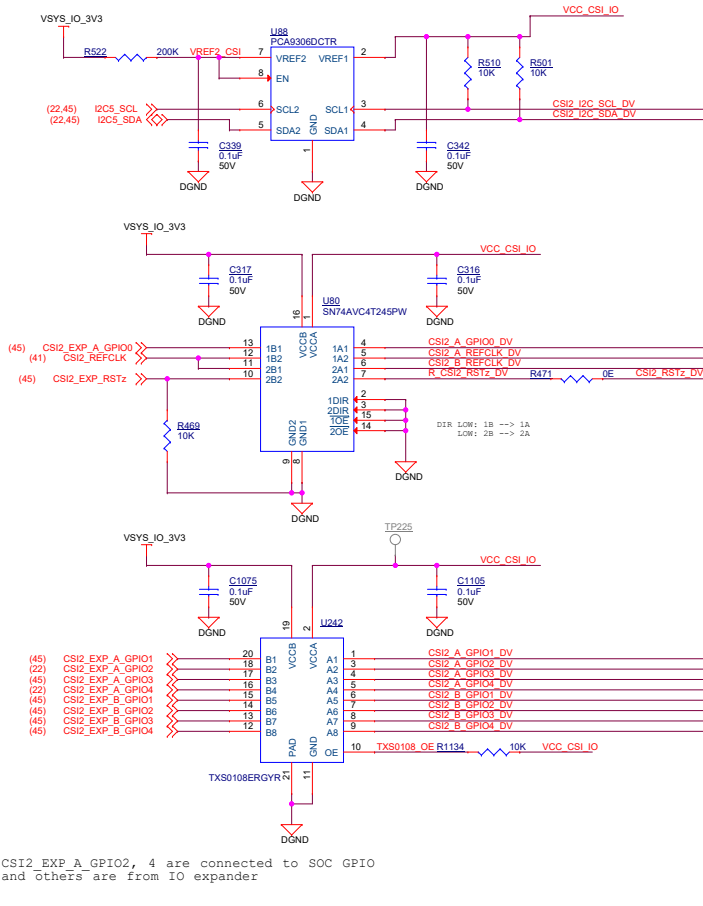
GESI_EXP_CONN



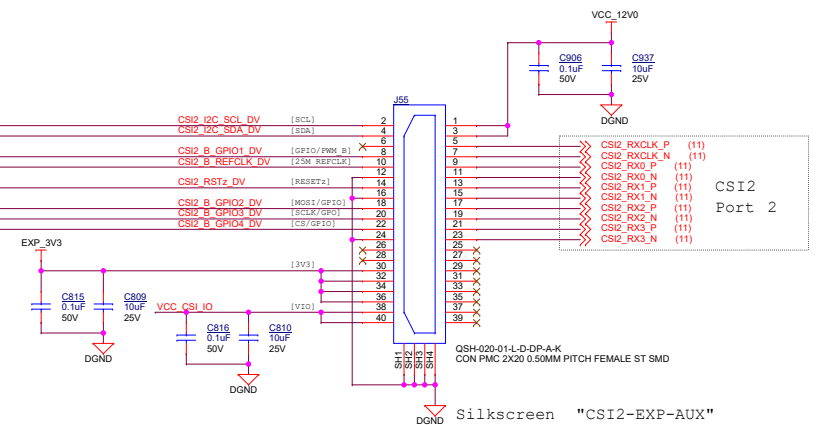
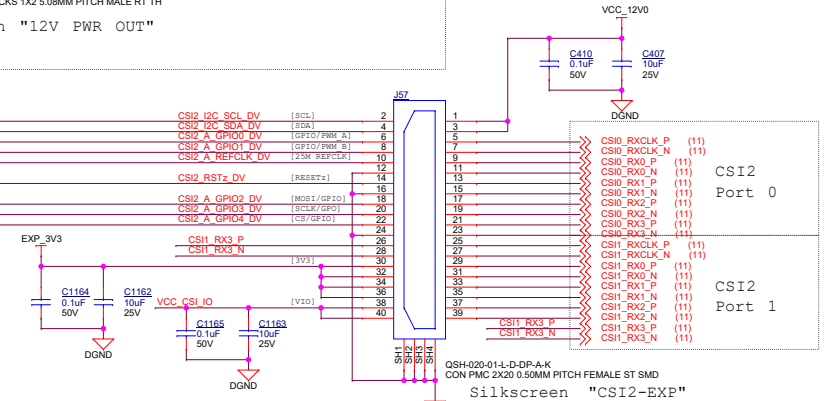
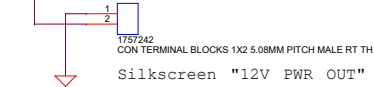
Project :		Title	
J7 EVM		GESI_EXP_CONN	
Size	PROC141 001 J78454XG01EVM	Rev	
C			E3
Date:	Wednesday, July 27, 2022	Sheet	36 of 88

CSI2 EXPANSION CONNECTORS

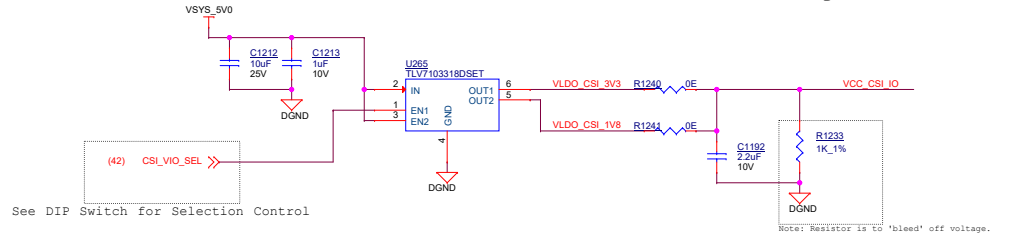
Level Translation for LVCMOS



Auxiliary 12V Power Output for CSI2

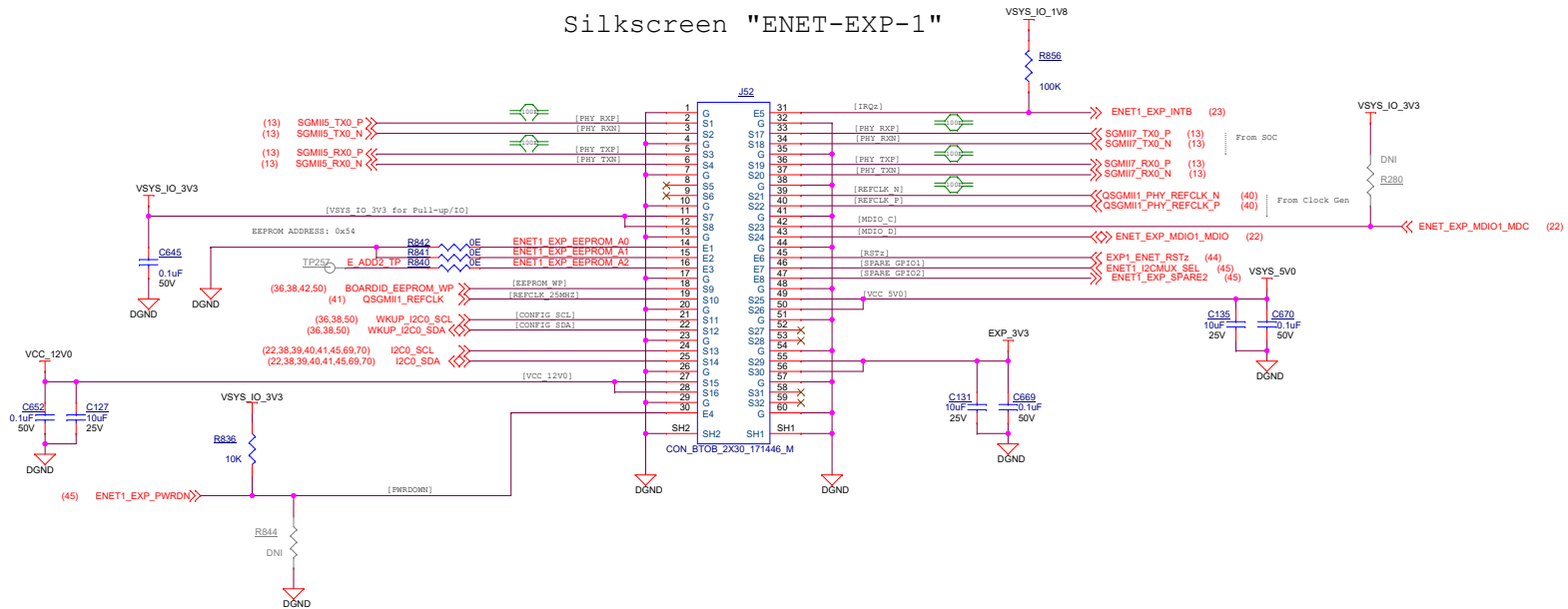


LVCMOS IO Voltage Selection

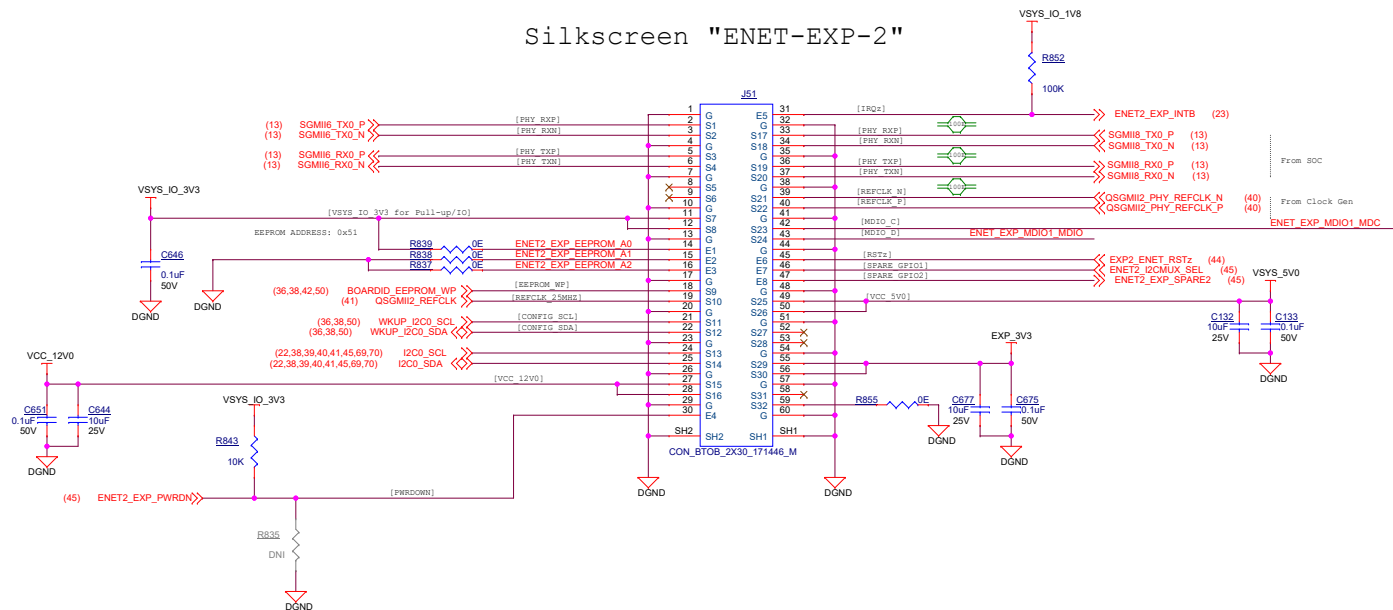


ENET EXPANSION CONNECTOR

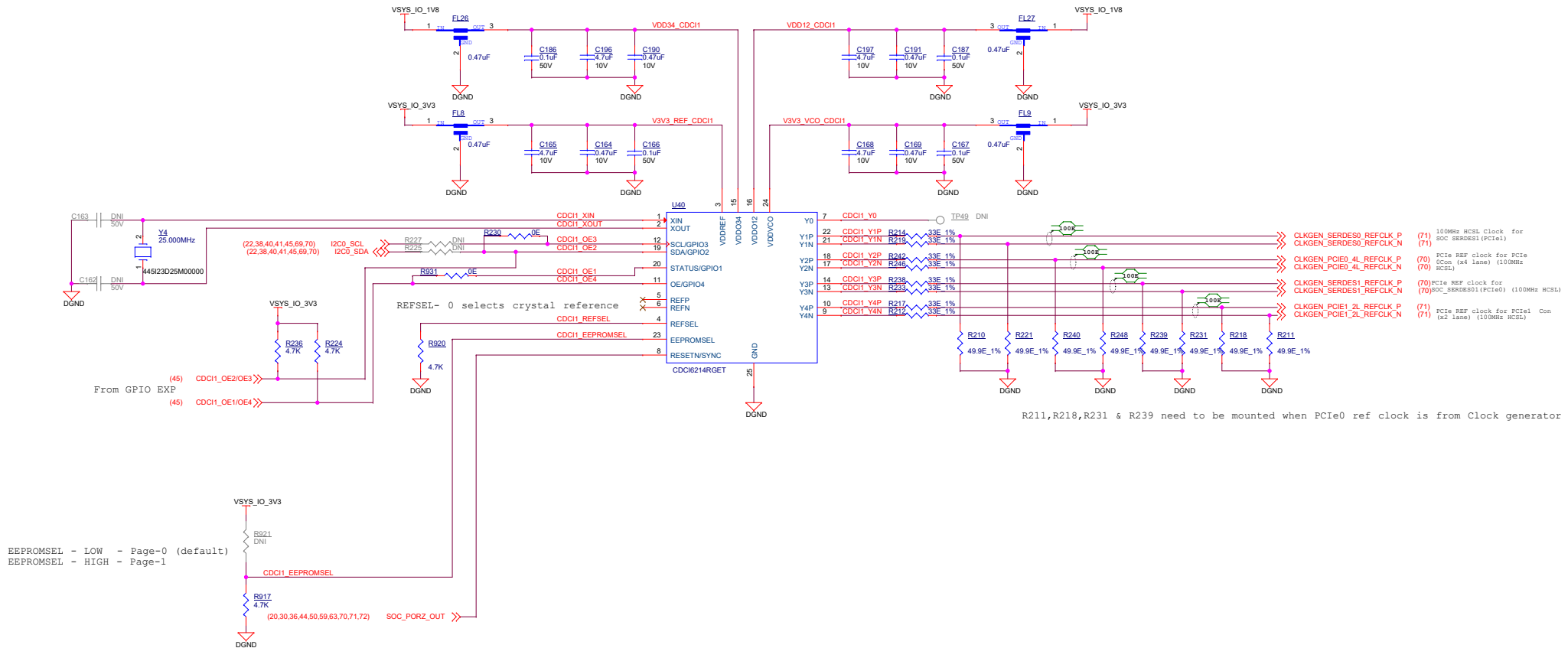
Silkscreen "ENET-EXP-1"



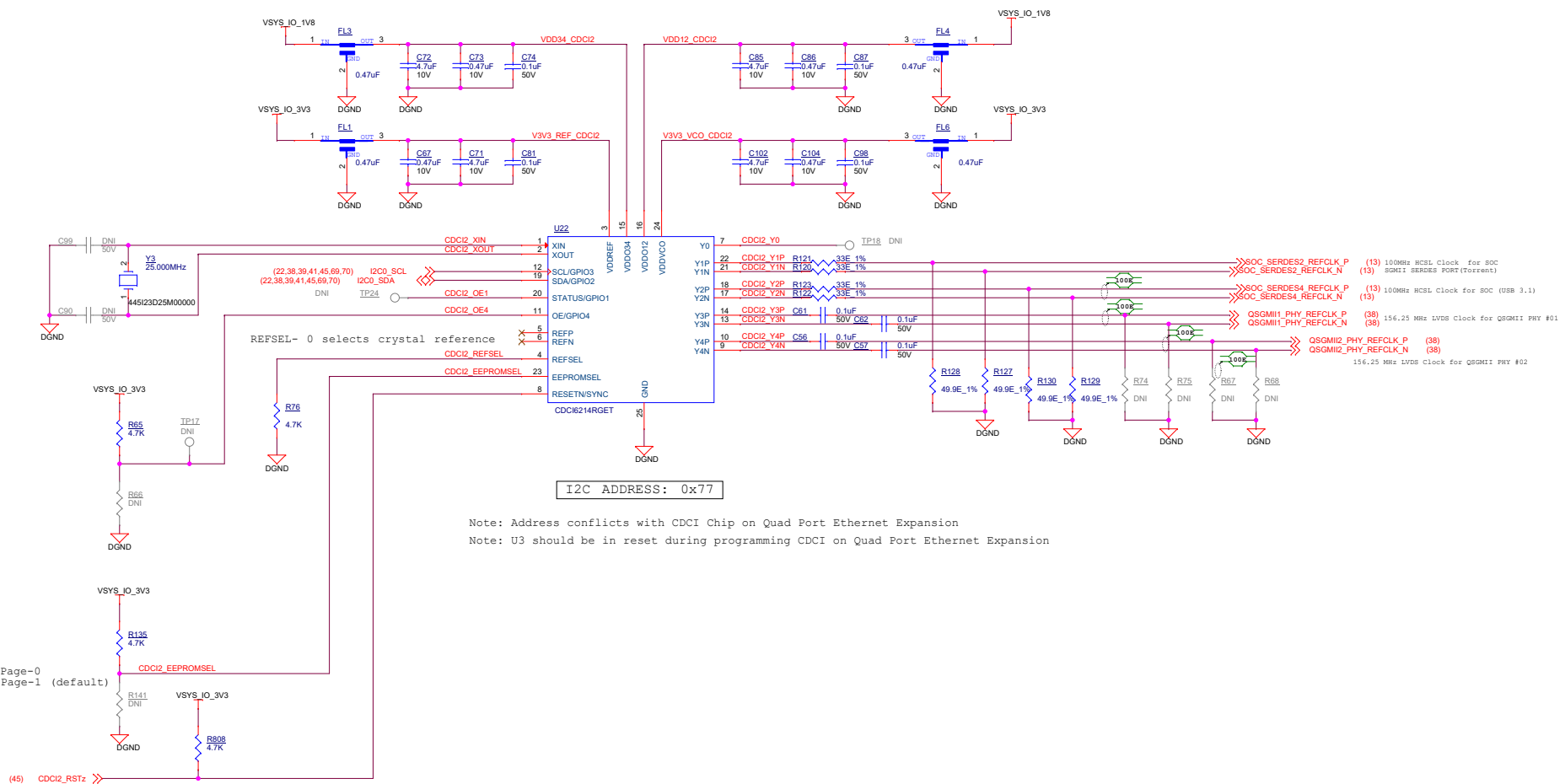
Silkscreen "ENET-EXP-2"



SERDES CLOCK GENERATOR #1

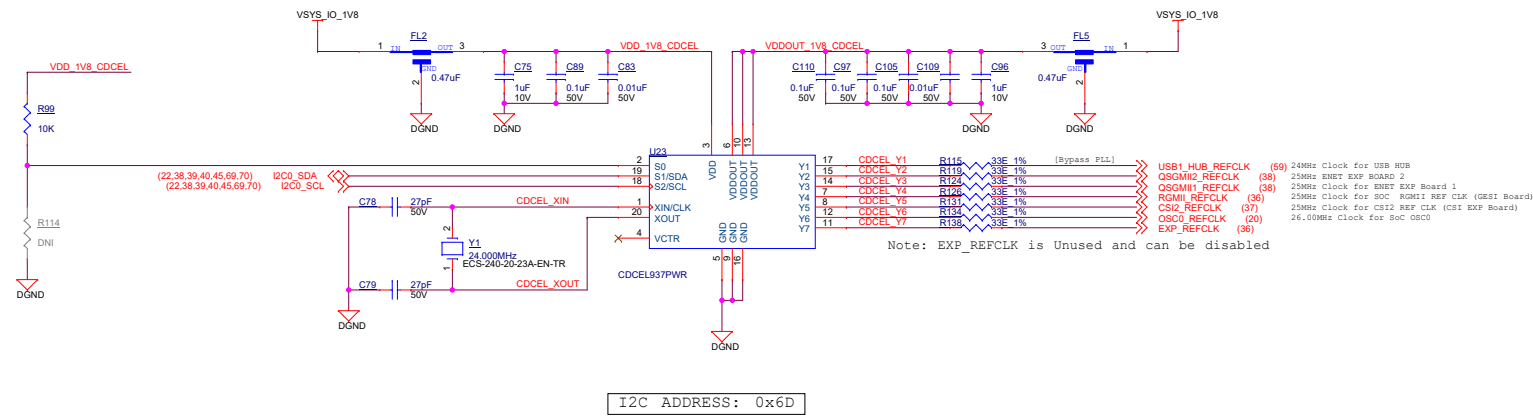


SERDES CLOCK GENERATOR #2

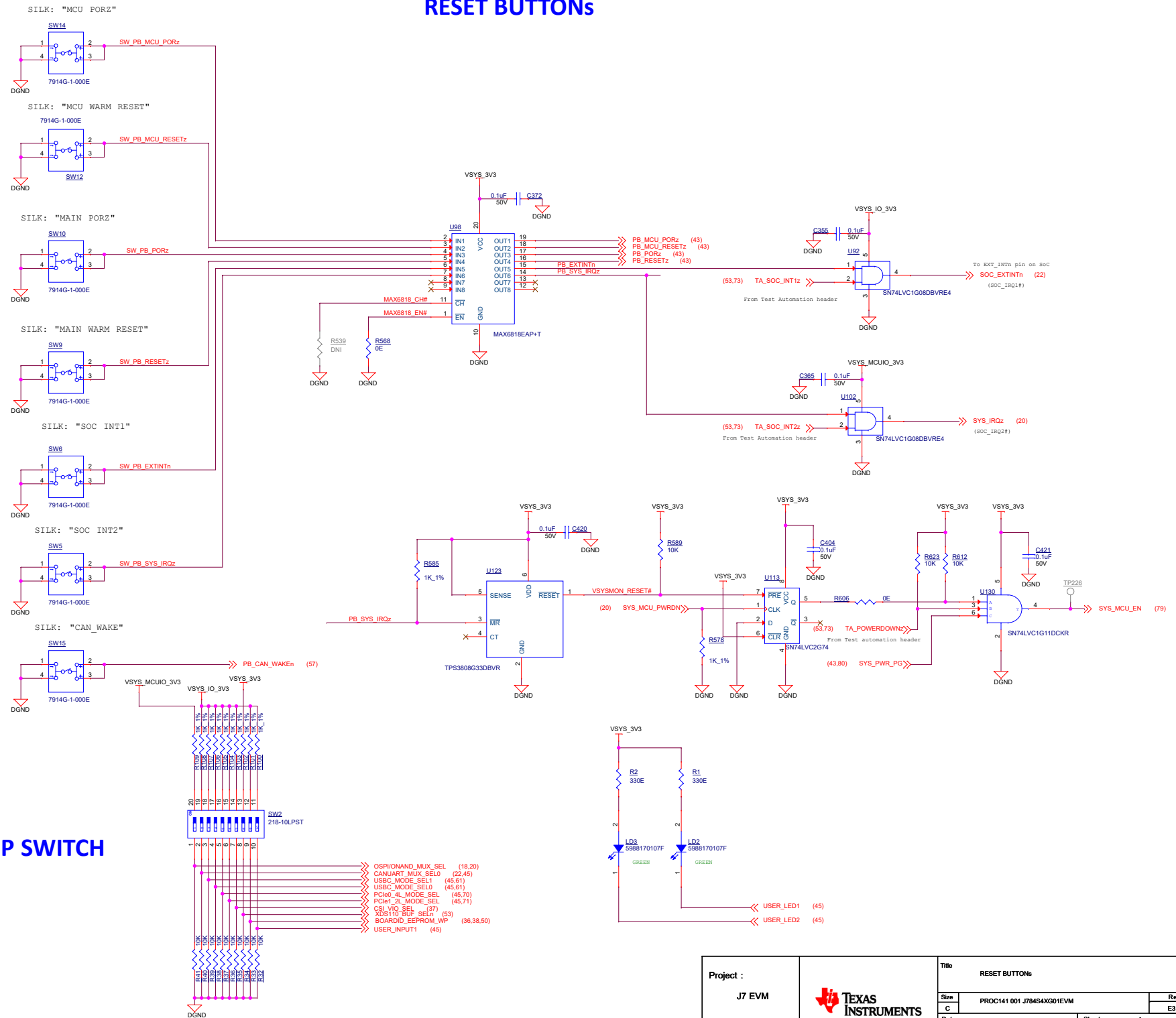


```
EEPROMSEL - LOW - Page-0
EEPROMSEL - HIGH - Page-1 (default)
```


PERIPHERAL CLOCK GENERATOR

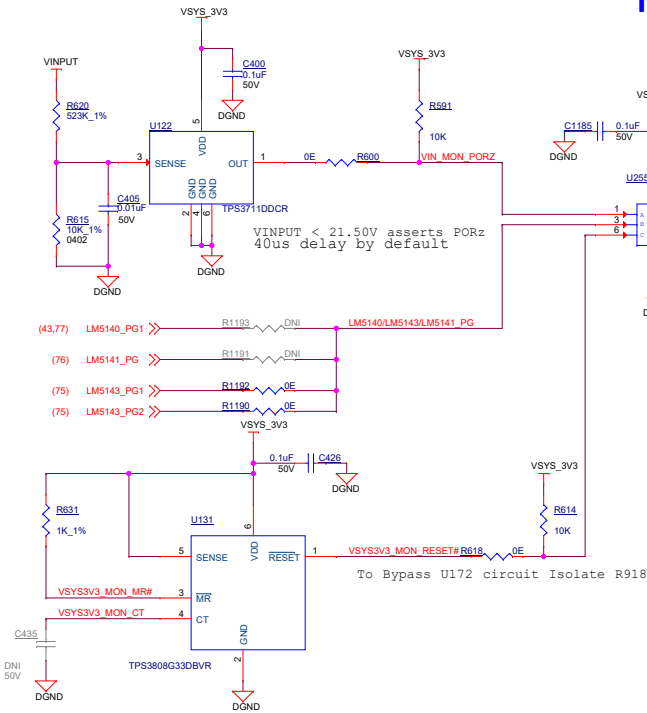


RESET BUTTONs

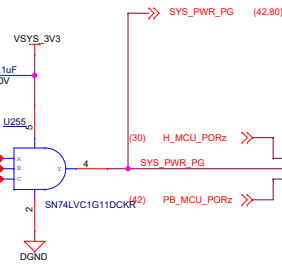


RESET INPUTS

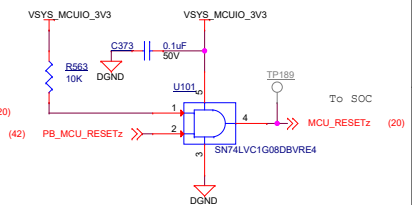
Under Voltage Monitor (VINPUT)



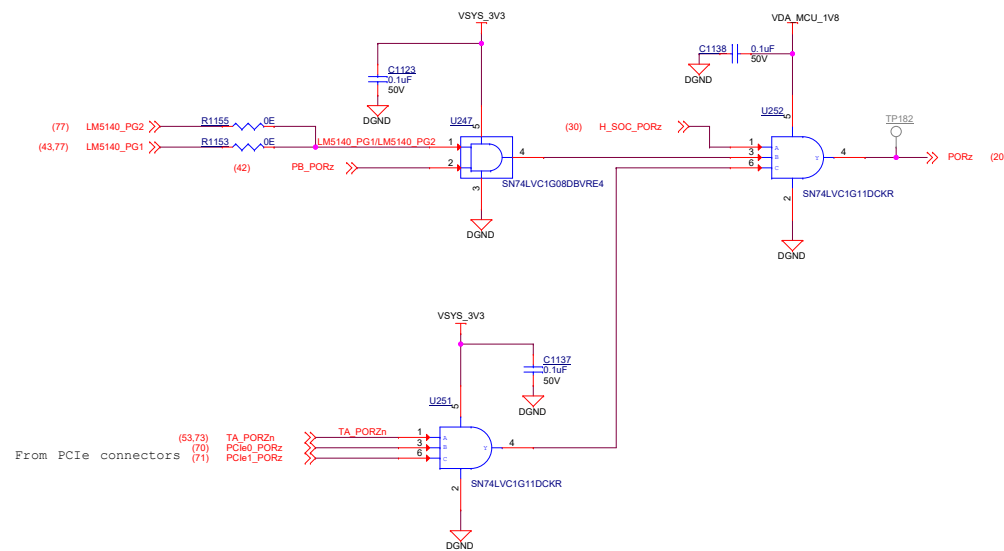
MCU PORz



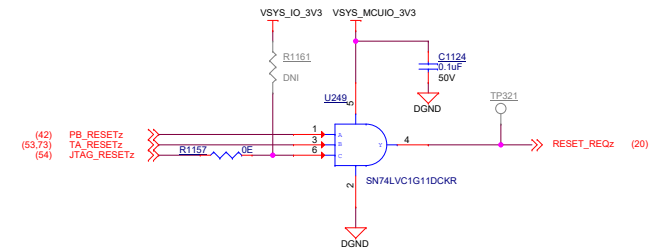
MCU_RESET



SOC PORz

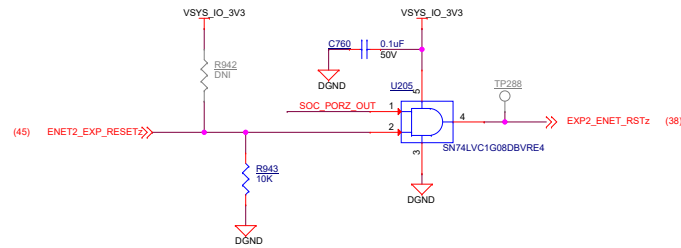
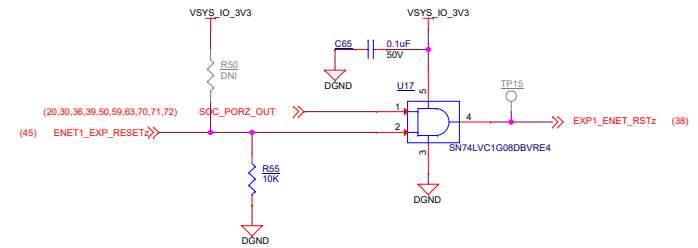
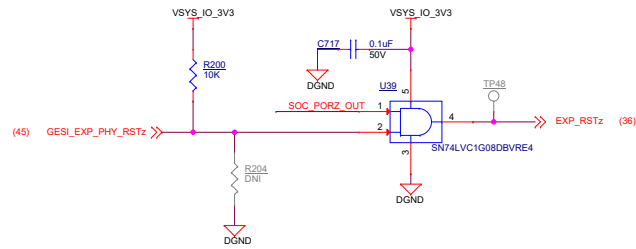
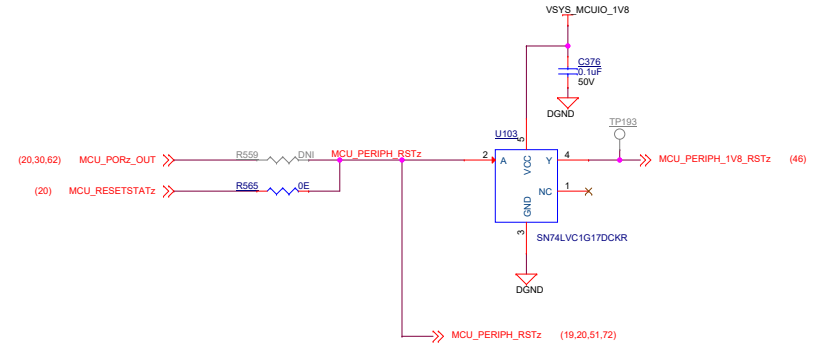
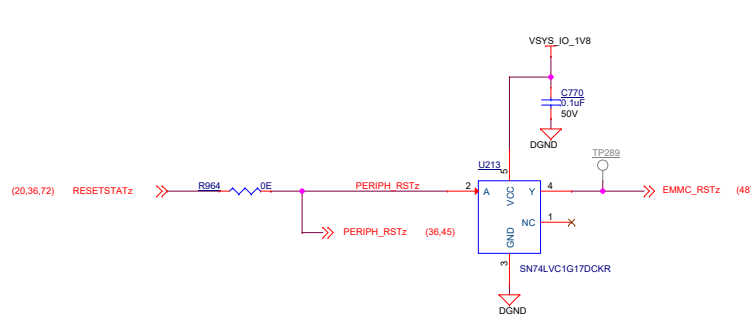


SOC RESET



Project : J7 EVM		Title RESET INPUTS	
		Size C	Rev E3
		Date: Wednesday, July 27, 2022	Sheet 43 of 88

RESET OUTPUTS

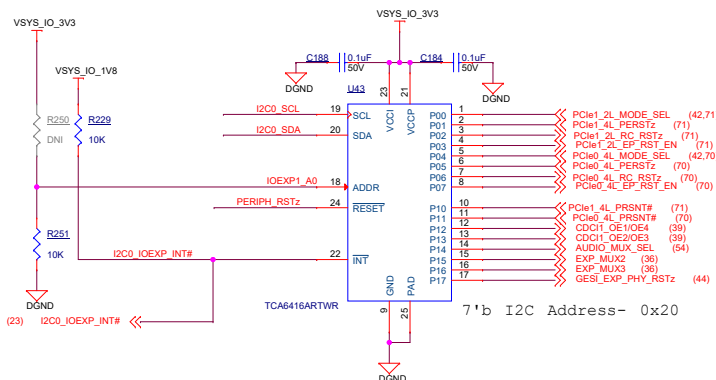


Project :		Title	
J7 EVM		RESET OUTPUTS	
		Size	Rev
		C	E3
		Date: Wednesday, July 27, 2022	Sheet 44 of 88

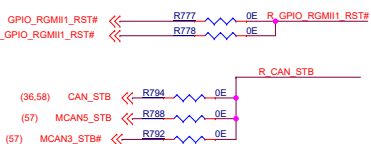
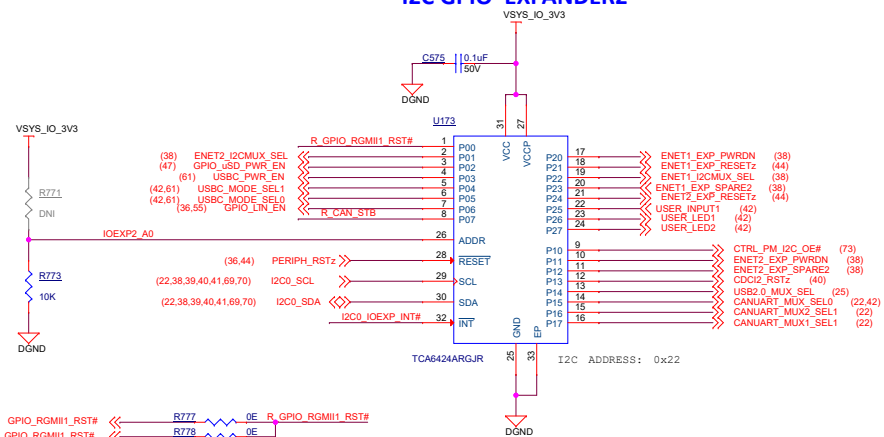


GPIO EXPANDERS

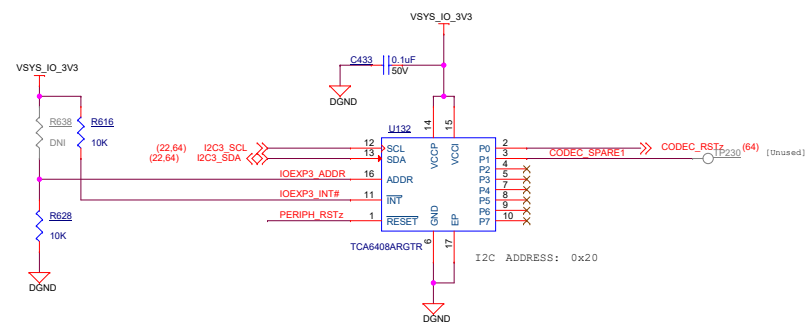
I2C GPIO EXPANDER1



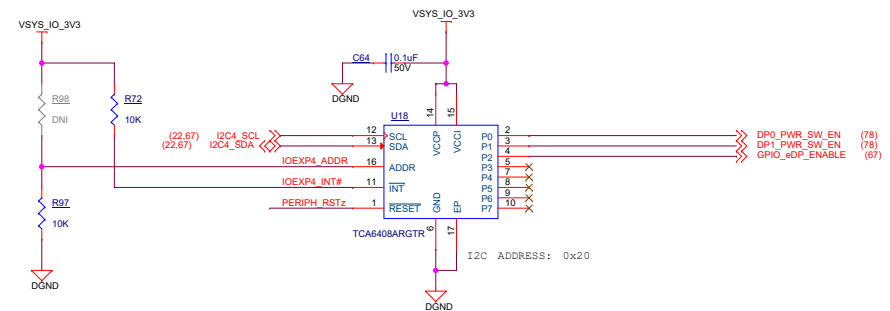
I2C GPIO EXPANDER2



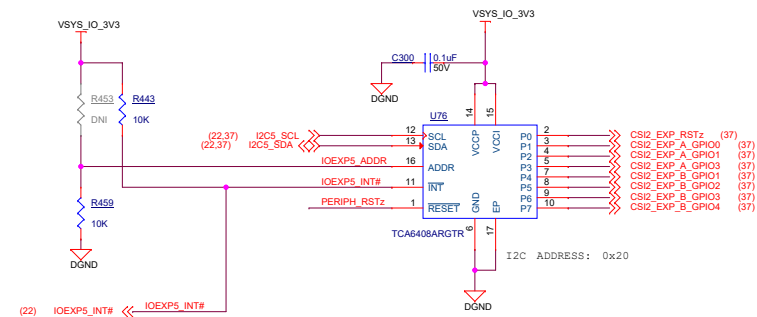
I2C GPIO EXPANDER3



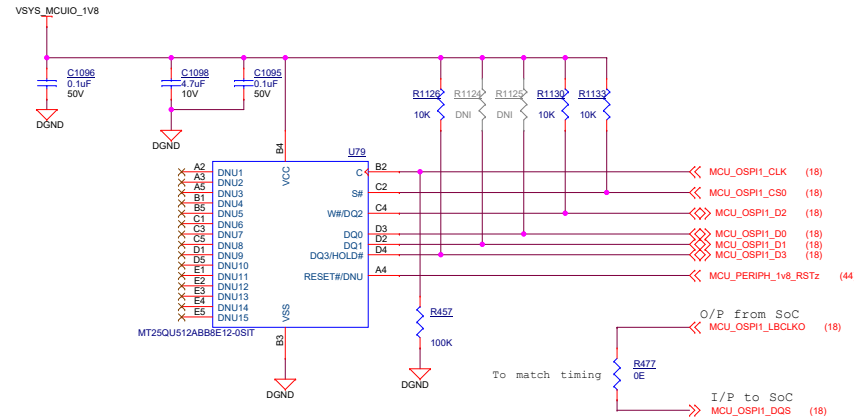
I2C GPIO EXPANDER4



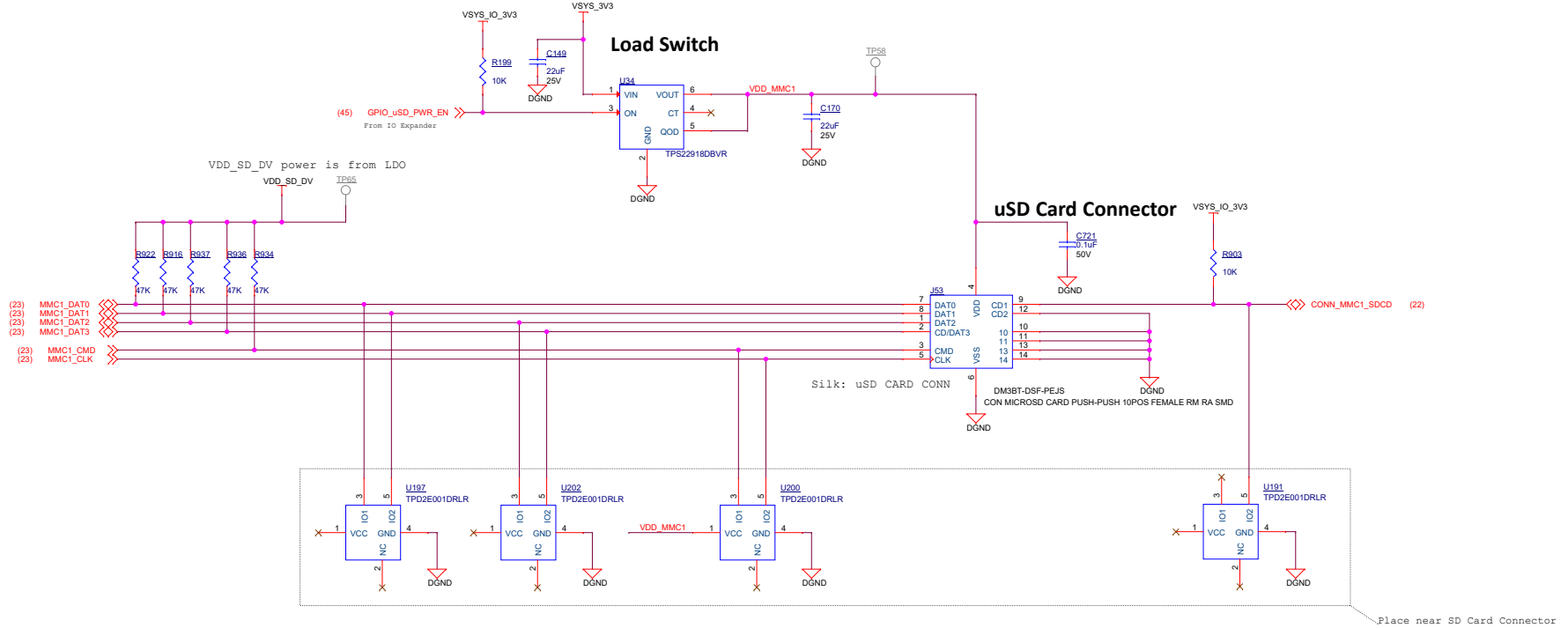
I2C GPIO EXPANDER5



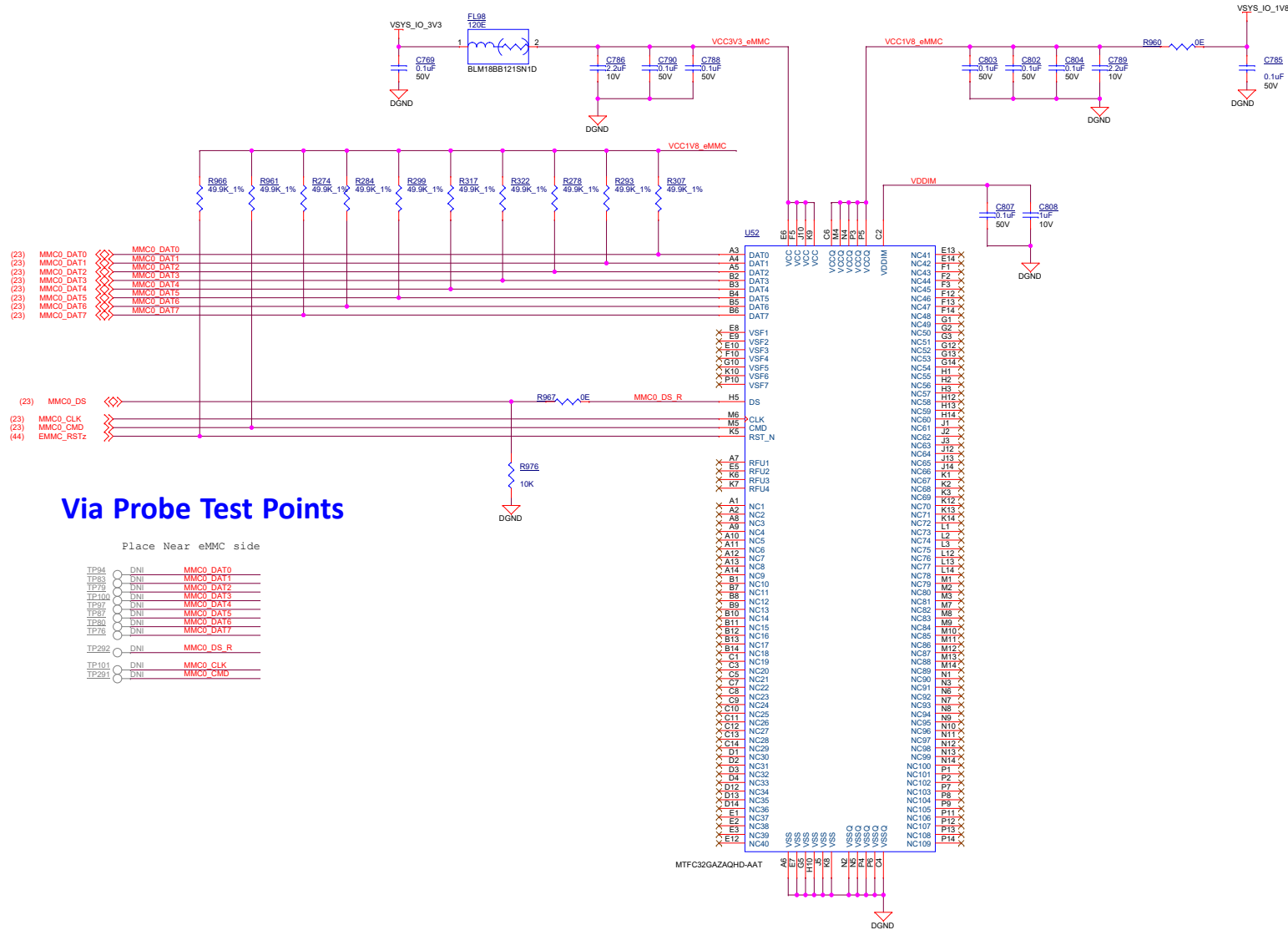
SPI NOR Flash



Micro SD CARD INTERFACE



eMMC FLASH

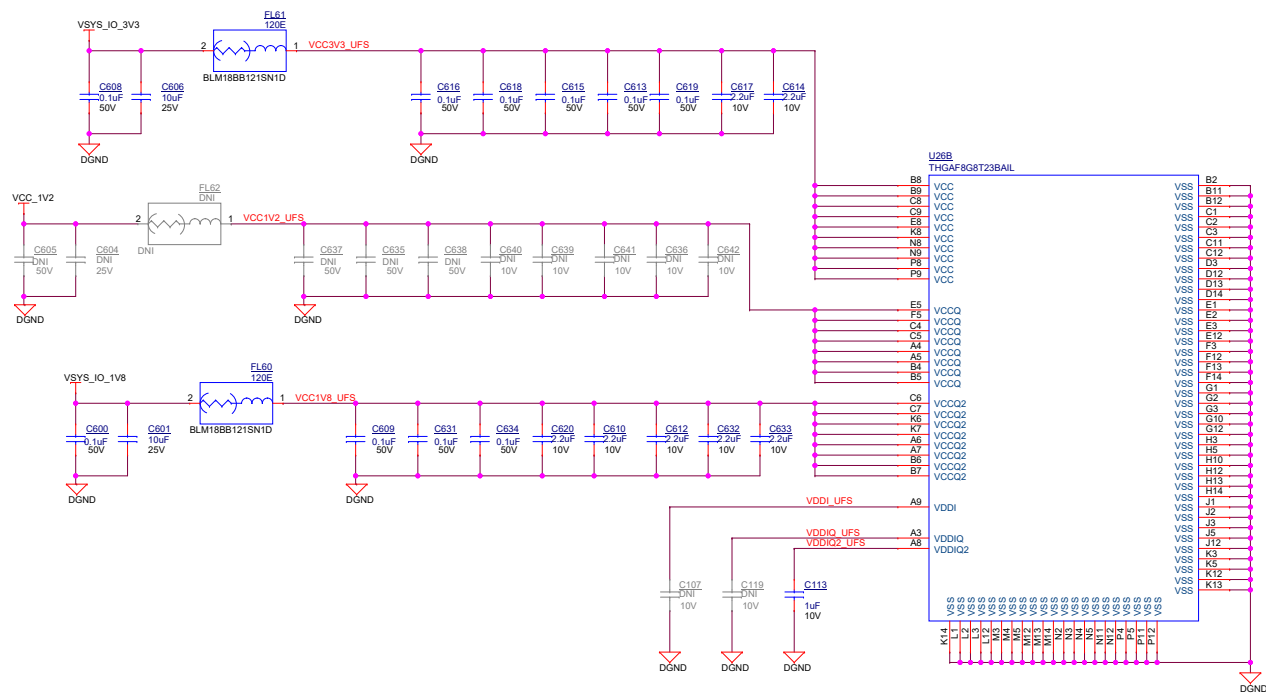
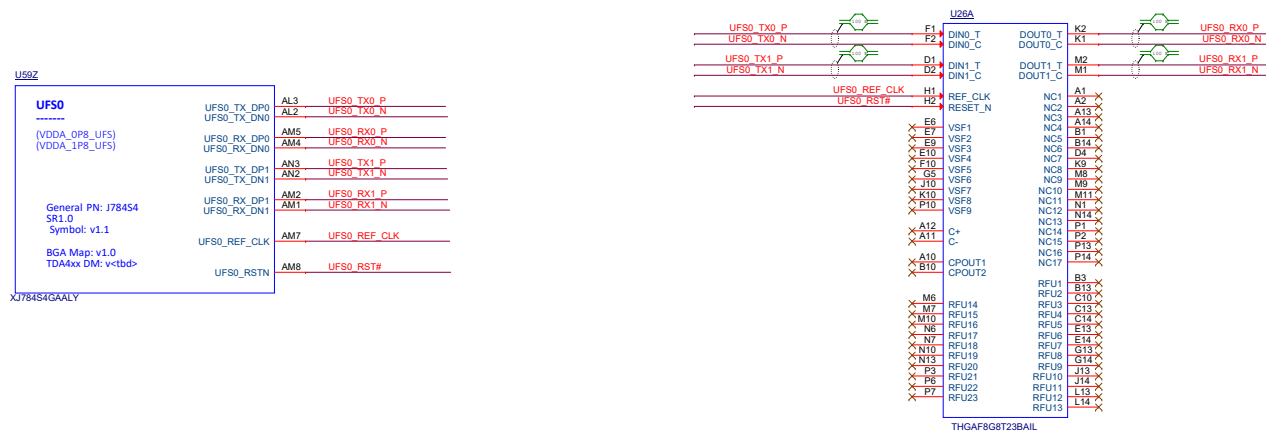


Via Probe Test Points

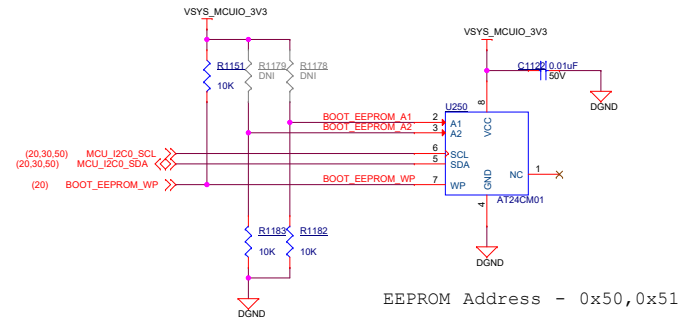
Place Near eMMC side

TP94	DNI	MMC0_DAT0
TP95	DNI	MMC0_DAT1
TP100	DNI	MMC0_DAT2
TP97	DNI	MMC0_DAT3
TP98	DNI	MMC0_DAT4
TP99	DNI	MMC0_DAT5
TP101	DNI	MMC0_DAT6
TP102	DNI	MMC0_DAT7
TP202	DNI	MMC0_DS_R
TP101	DNI	MMC0_CLK
TP201	DNI	MMC0_CMD

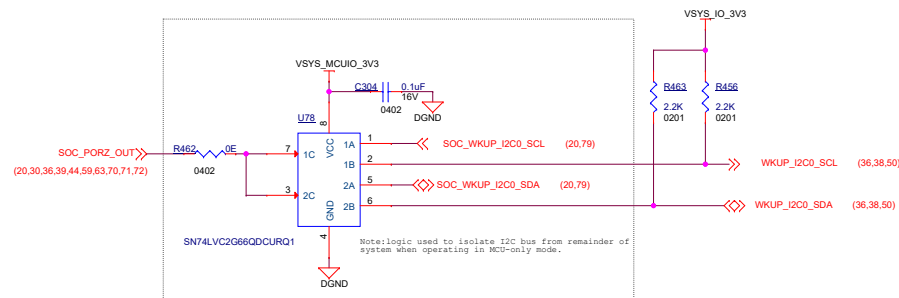
UFS FLASH



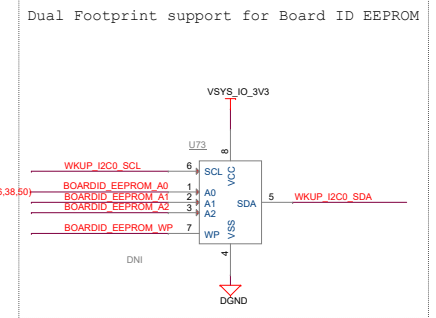
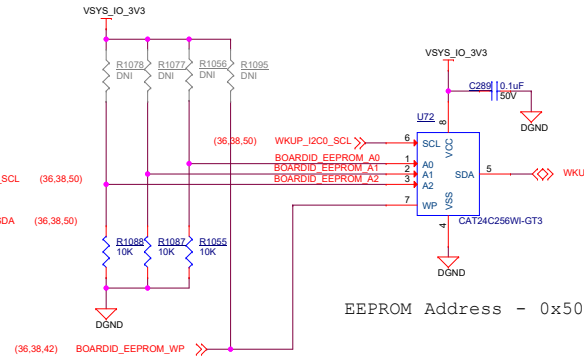
BOOT EEPROM



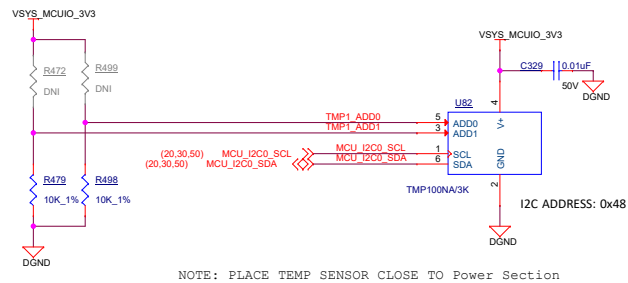
I2C for BOARD ID EEPROMs



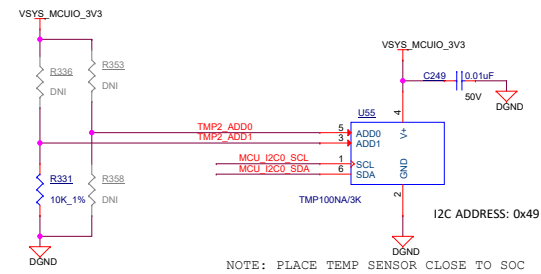
BOARD ID EEPROM



TEMPERATURE SENSORS (TI EVM Only)



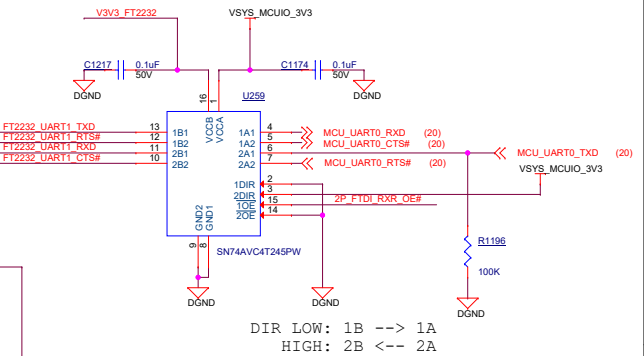
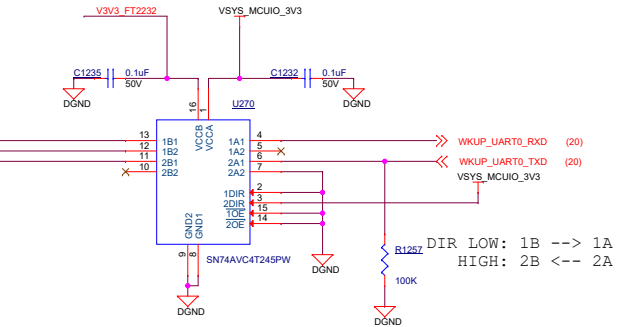
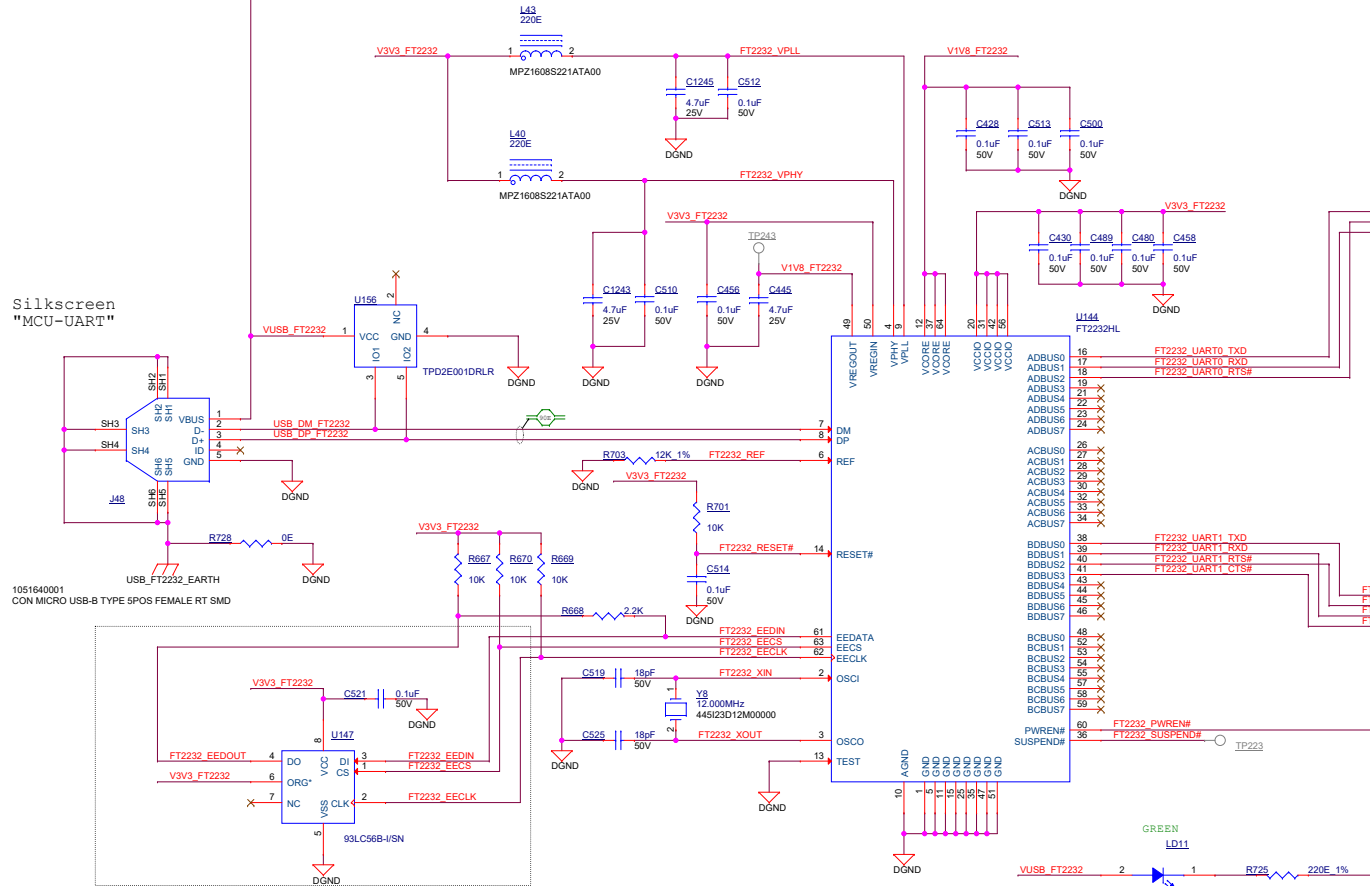
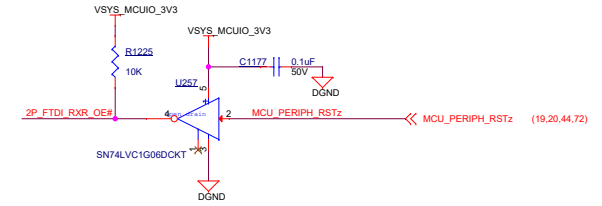
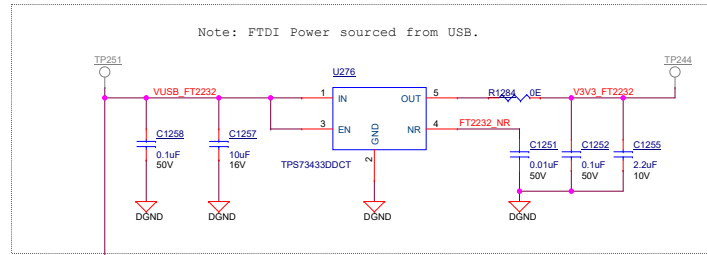
NOTE: PLACE TEMP SENSOR CLOSE TO Power Section



NOTE: PLACE TEMP SENSOR CLOSE TO SOC

Project : J7 EVM		Title EEPROM	
Size PROC141 001 J784S4XG01EVM		Rev E3	
Date: Thursday, September 15, 2022		Sheet 50 of 88	

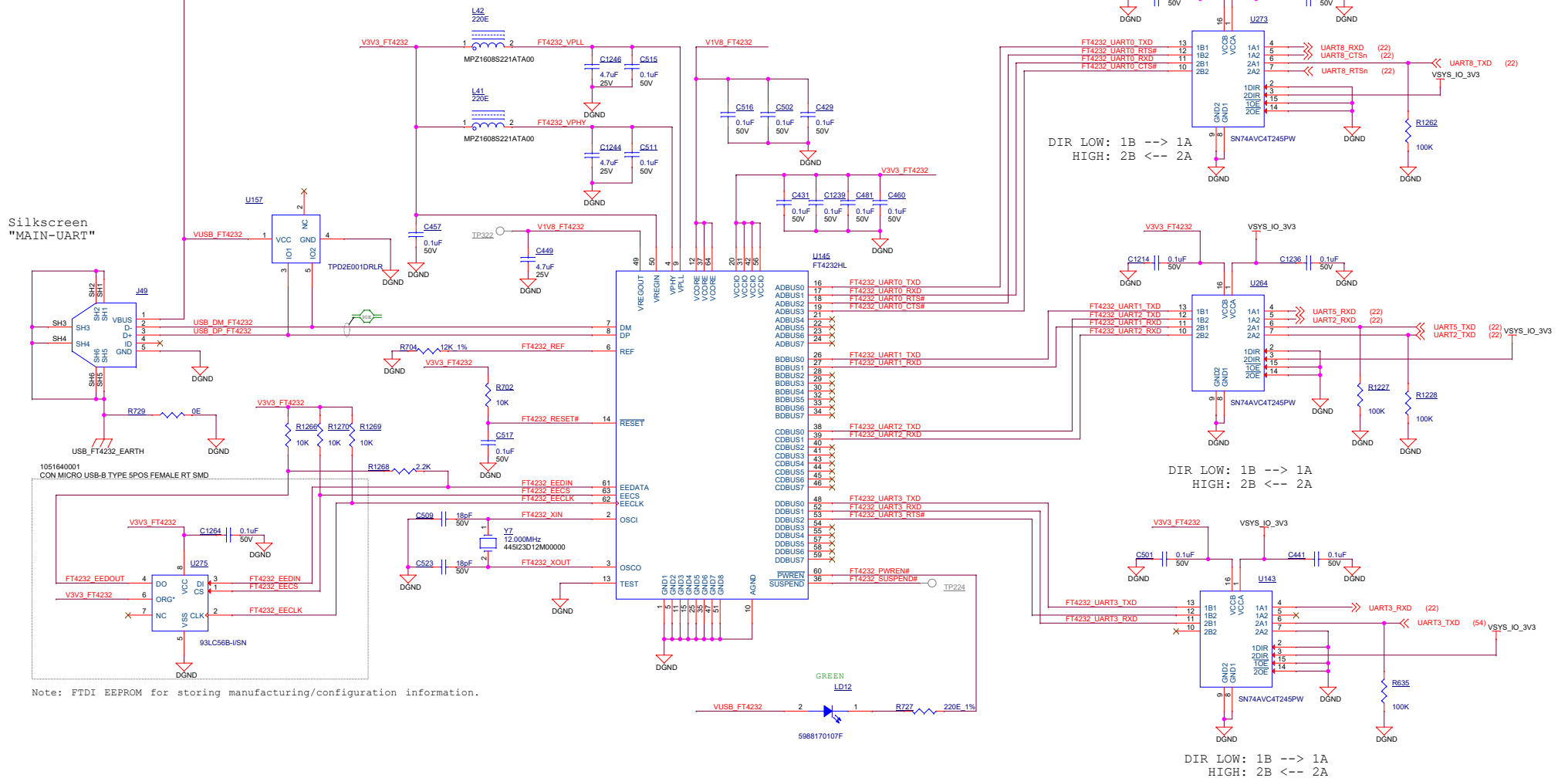
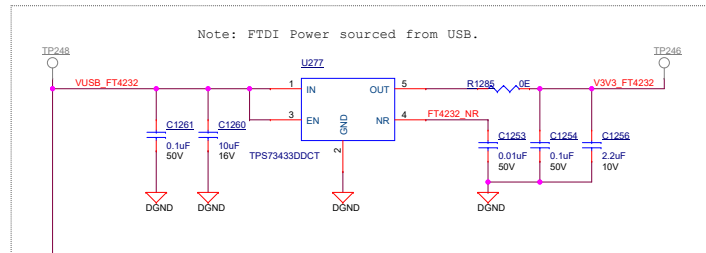
DUAL PORT FTDI




Note: FTDI EEPROM for storing manufacturing/configuration information.

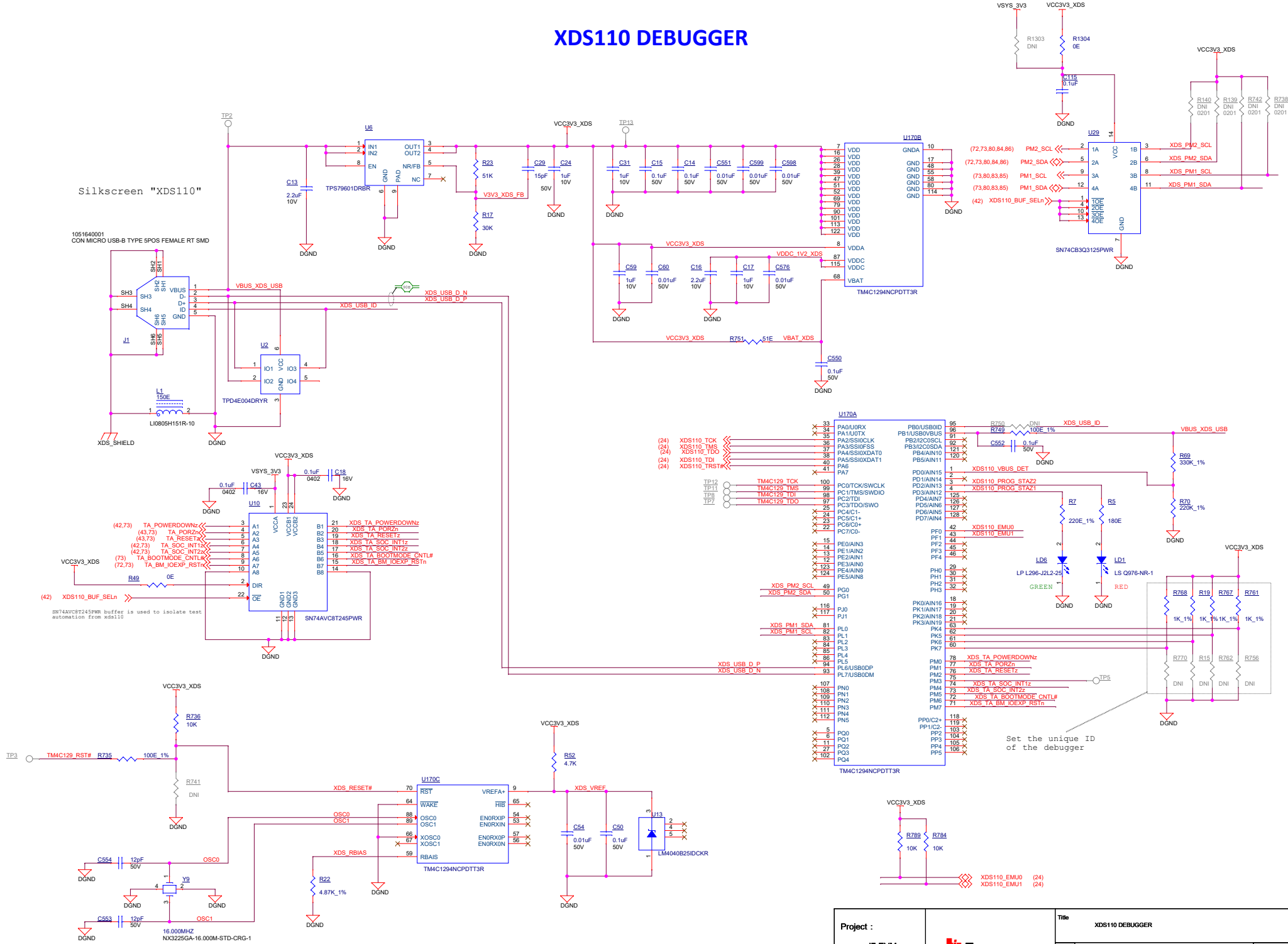
Project :		Title	
J7 EVM		DUAL PORT FTDI	
Size		PROC141 001 J784S4XG01EVM	Rev
C			E3
Date:		Wednesday, July 27, 2022	Sheet 51 of 88

QUAD PORT FTDI

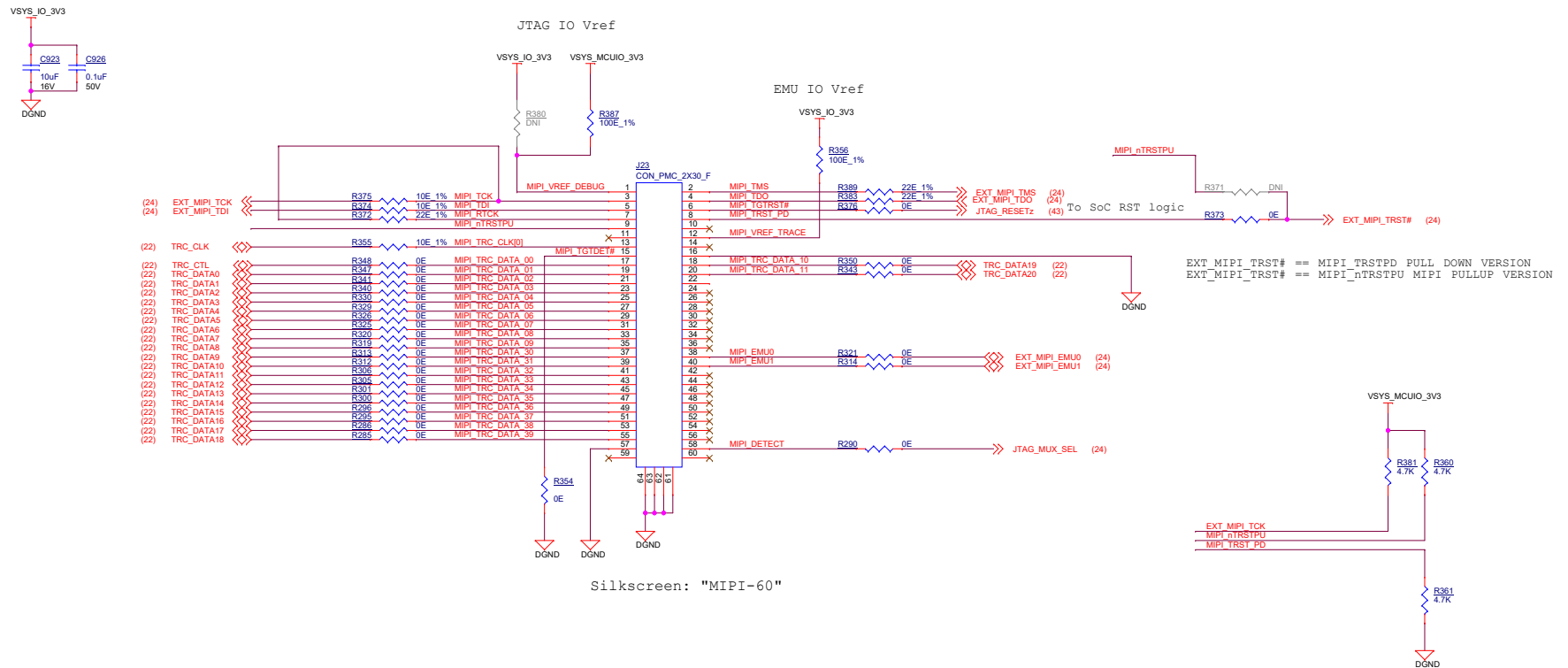


Project : J7 EVM		Title			
		QUAD PORT FTDI			
		Size	PROC141 001 J784S4XG01EVM		Rev
		C			E3
		Date:	Wednesday, July 27, 2022		Sheet 52 of 88

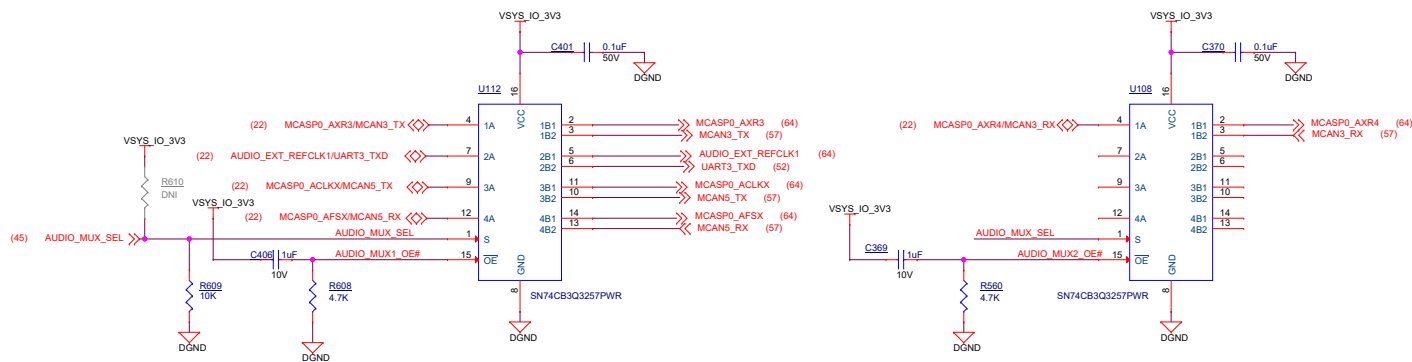
XDS110 DEBUGGER



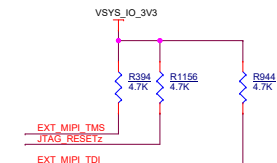
JTAG MIPI60 CONNECTOR



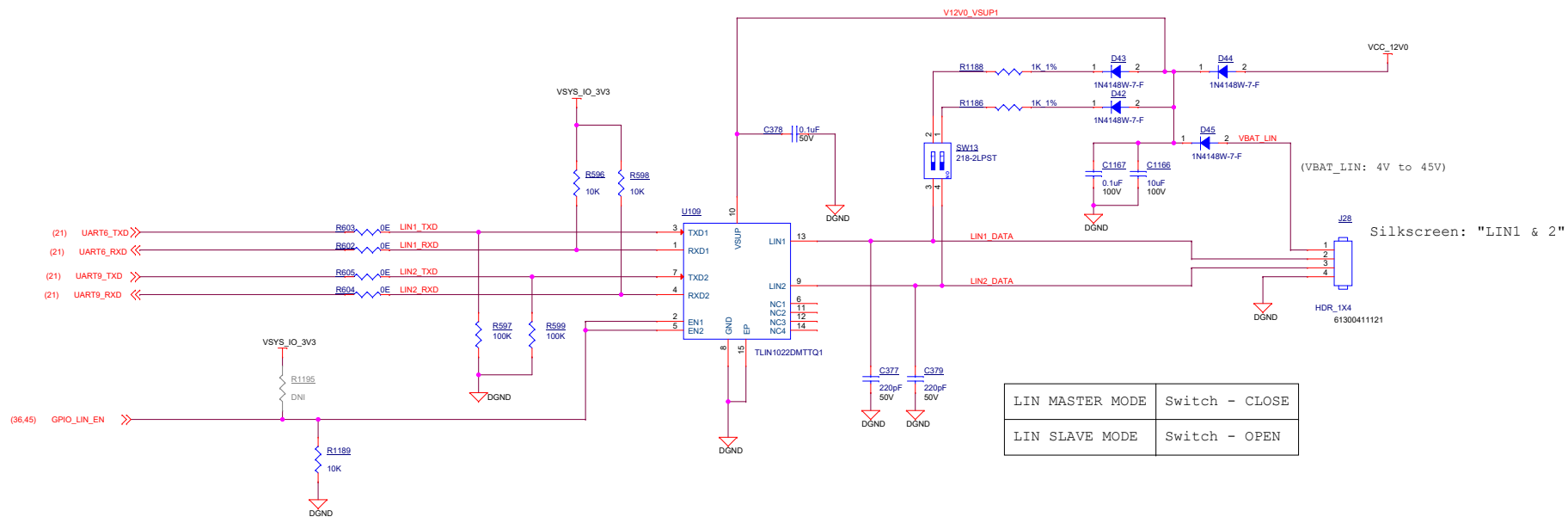
Silkscreen: "MIPI-60"



JTAG - 1:2 MUX : Truth Table



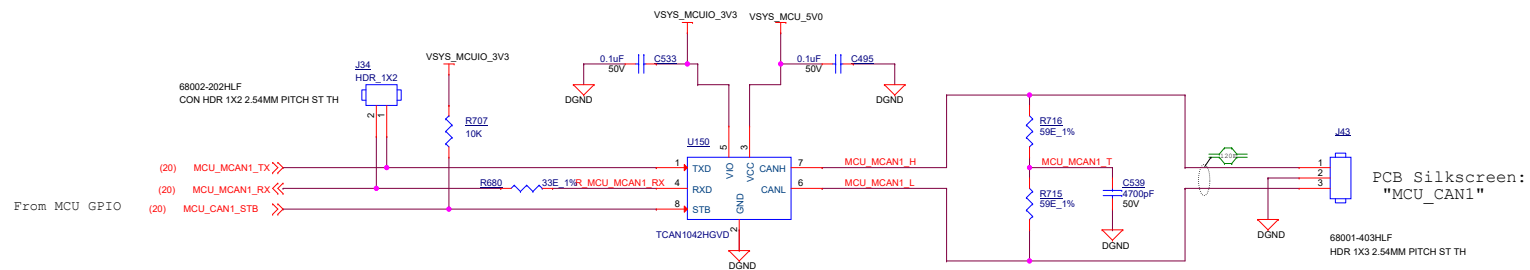
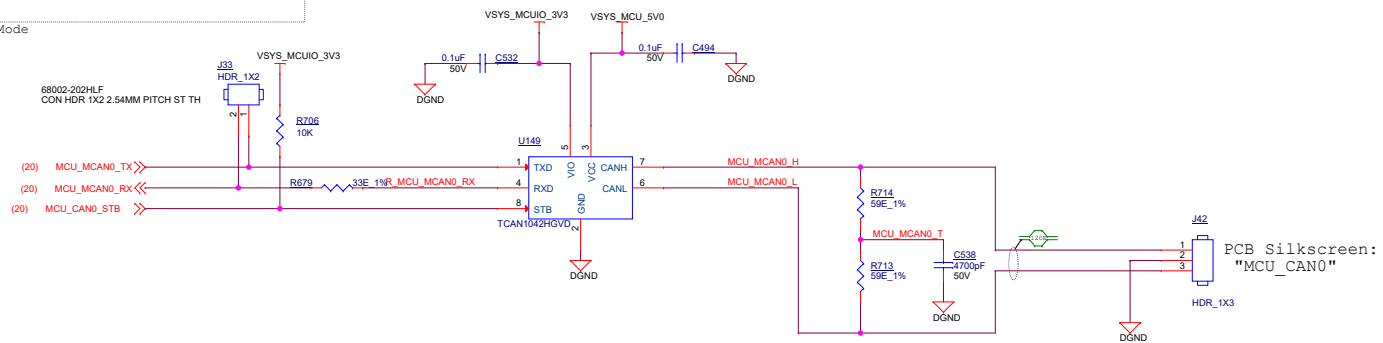
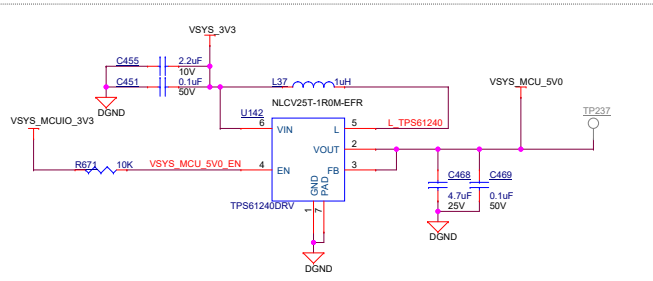
LIN INTERFACE



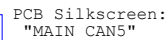
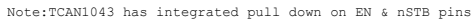
LIN MASTER MODE	Switch - CLOSE
LIN SLAVE MODE	Switch - OPEN

CAN TRANSCEIVERS #1-MCU DOMAIN

VSYS_MCU_5V0 GENERATION

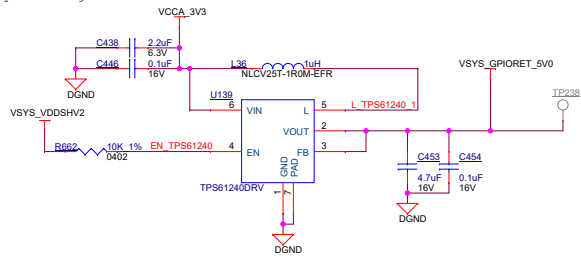


CAN TRANSCEIVERS #2-MAIN DOMAIN

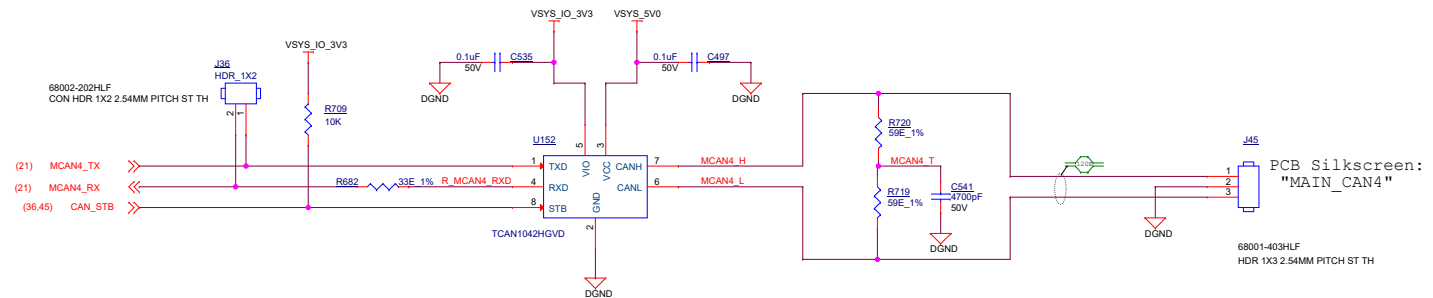
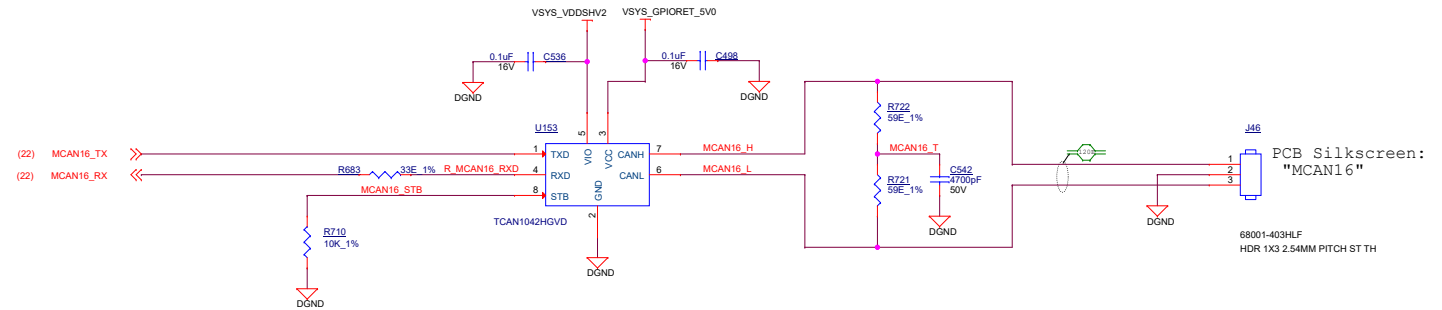


VSYS_GPIORET_5V0 GENERATION

Note: Booster convertor required for EVM due to system 5V supply shutting down in retention mode



CAN TRANSCEIVER



Project :

J7 EVM



Title
CAN TRANSCEIVER #3

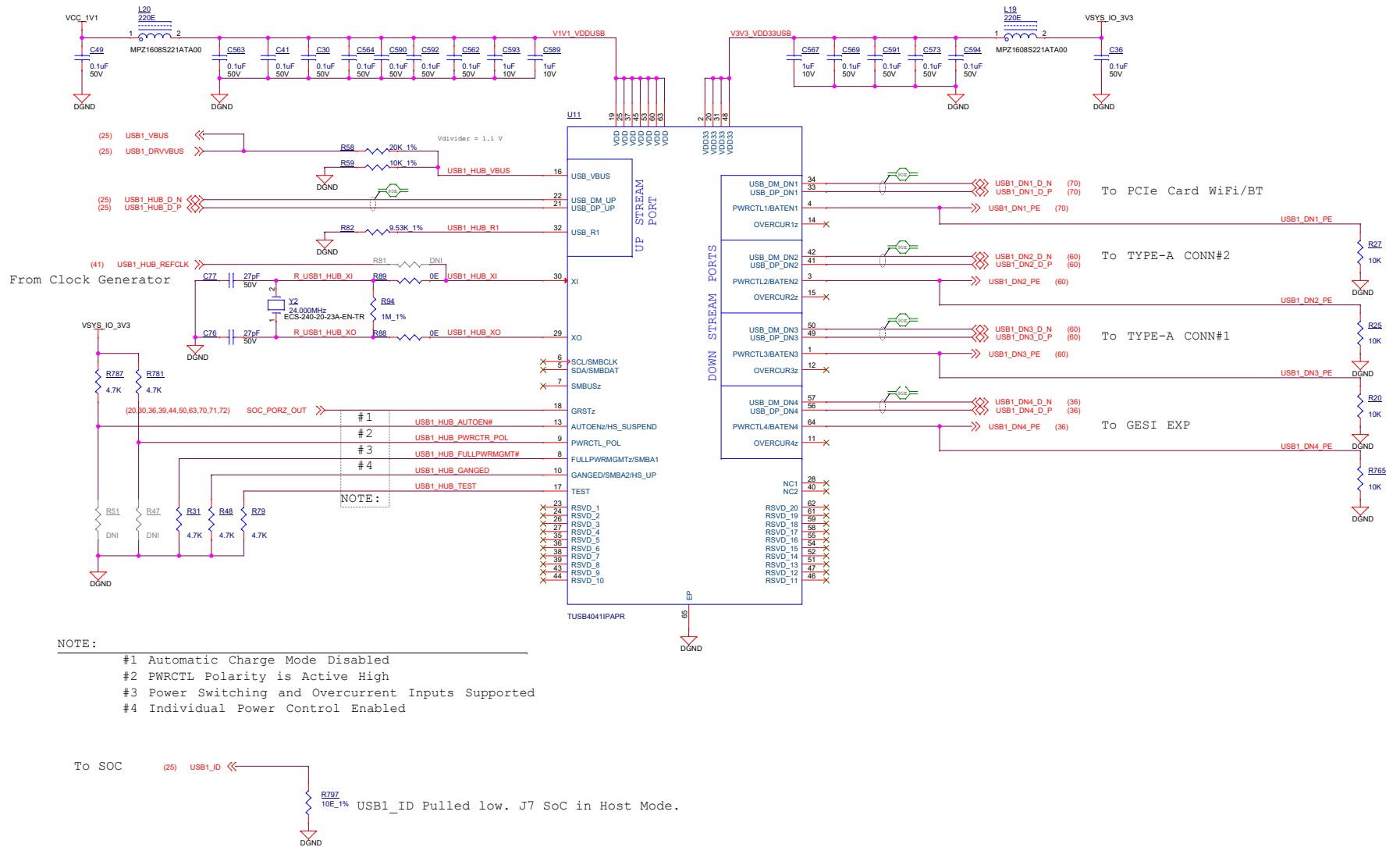
Size
PROC141 001 J78454XG01EVM

C
Date: Wednesday, July 27, 2022

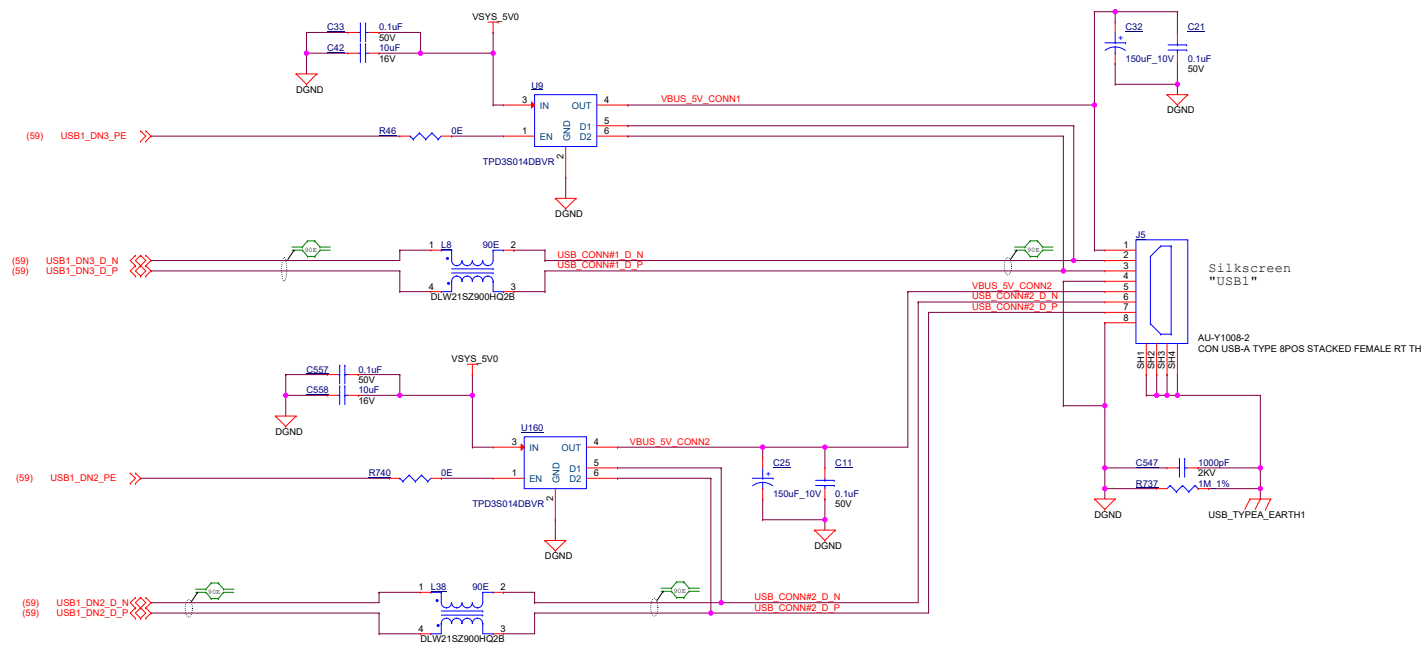
Sheet 58 of 88

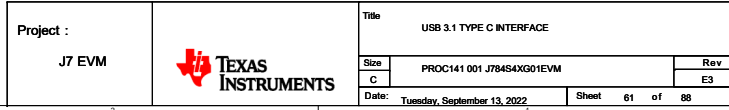
Rev
E3

USB HUB

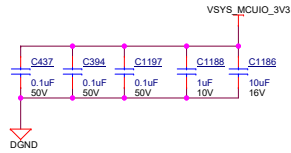


USB 2.0 TYPE-A CONNECTORS

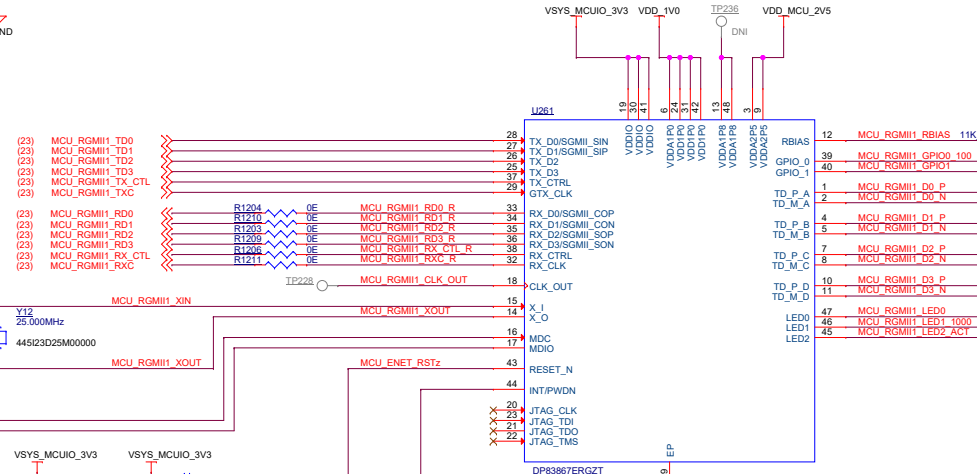
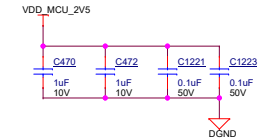
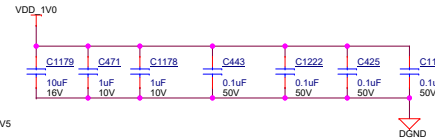




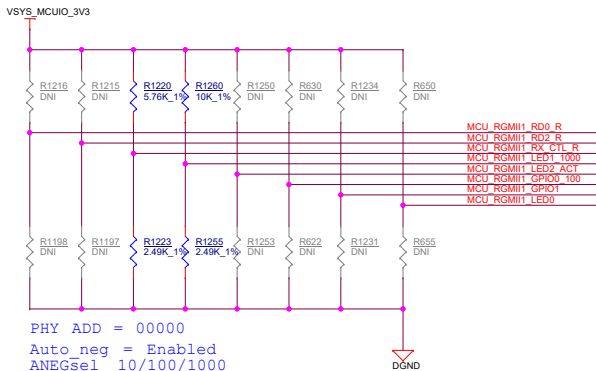
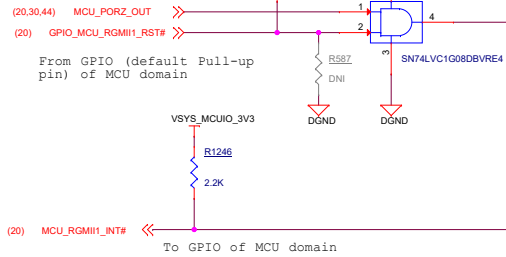
MCU GB ETHERNET



VDD1P0 supply voltage is connected to VCC_1V1.
VDD1P0 supply range is 0.95V to 1.155V.



RESET LOGIC

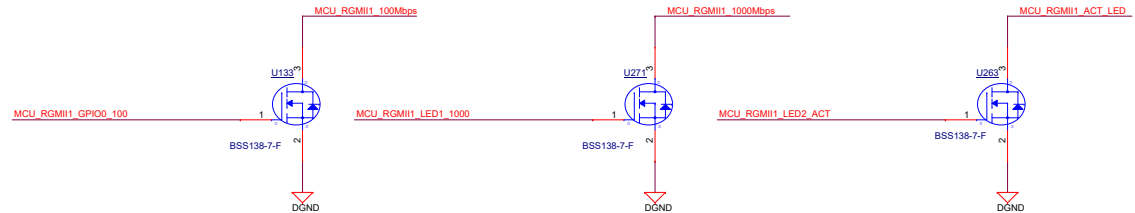


PHY ADD = 00000
Auto_neg = Enabled
ANEGsel 10/100/1000
RGMII Clock Skew TX = 0ns
RGMII Clock Skew RX = 2ns

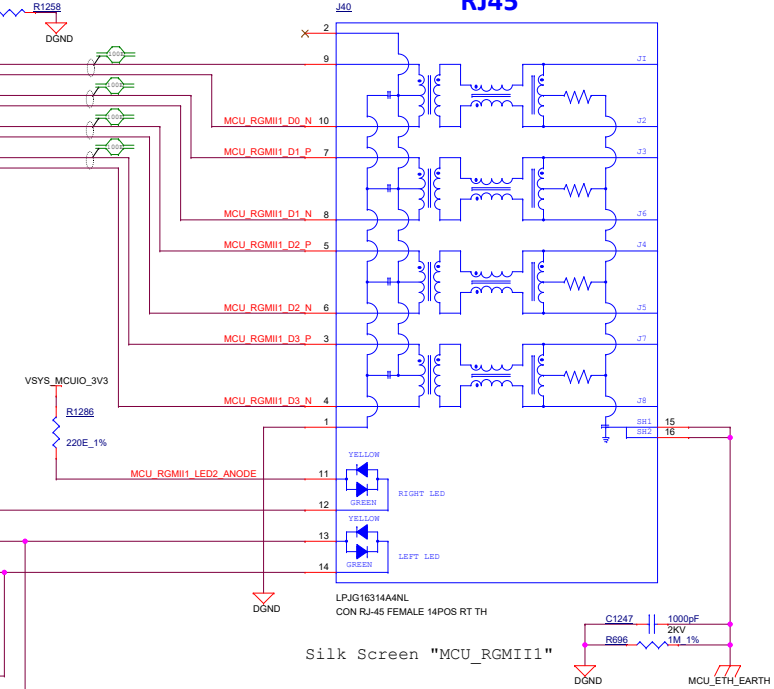
LED_2-MODE1 & LED_1-MODE2-TX SKEW=0ns
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

Set Mode 3 [Autoneg Disable - 0]

SPEED AND ACTIVITY LED DRIVERS



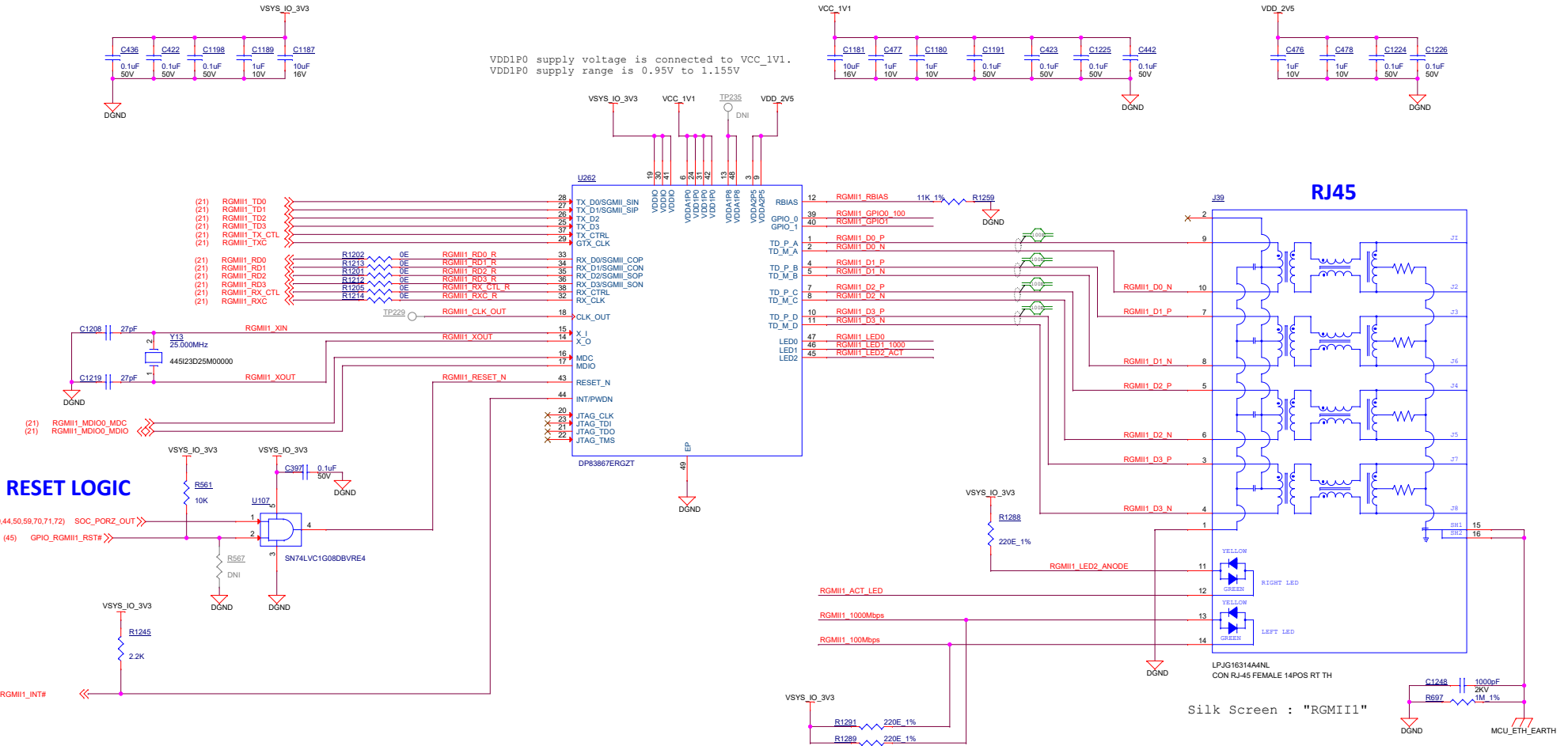
RJ45



RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

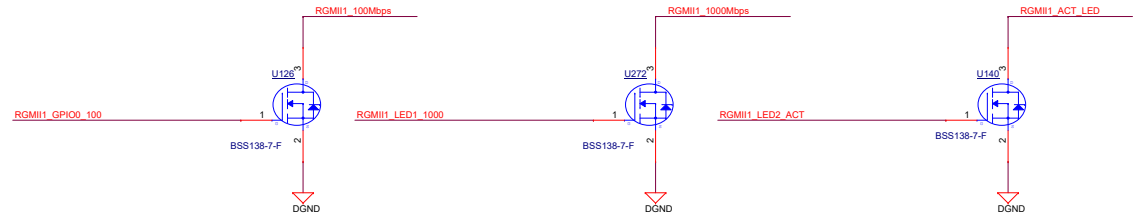
RGMII1

VDD1P0 supply voltage is connected to VCC_1V1.
VDD1P0 supply range is 0.95V to 1.155V



SPEED AND ACTIVITY LED DRIVERS

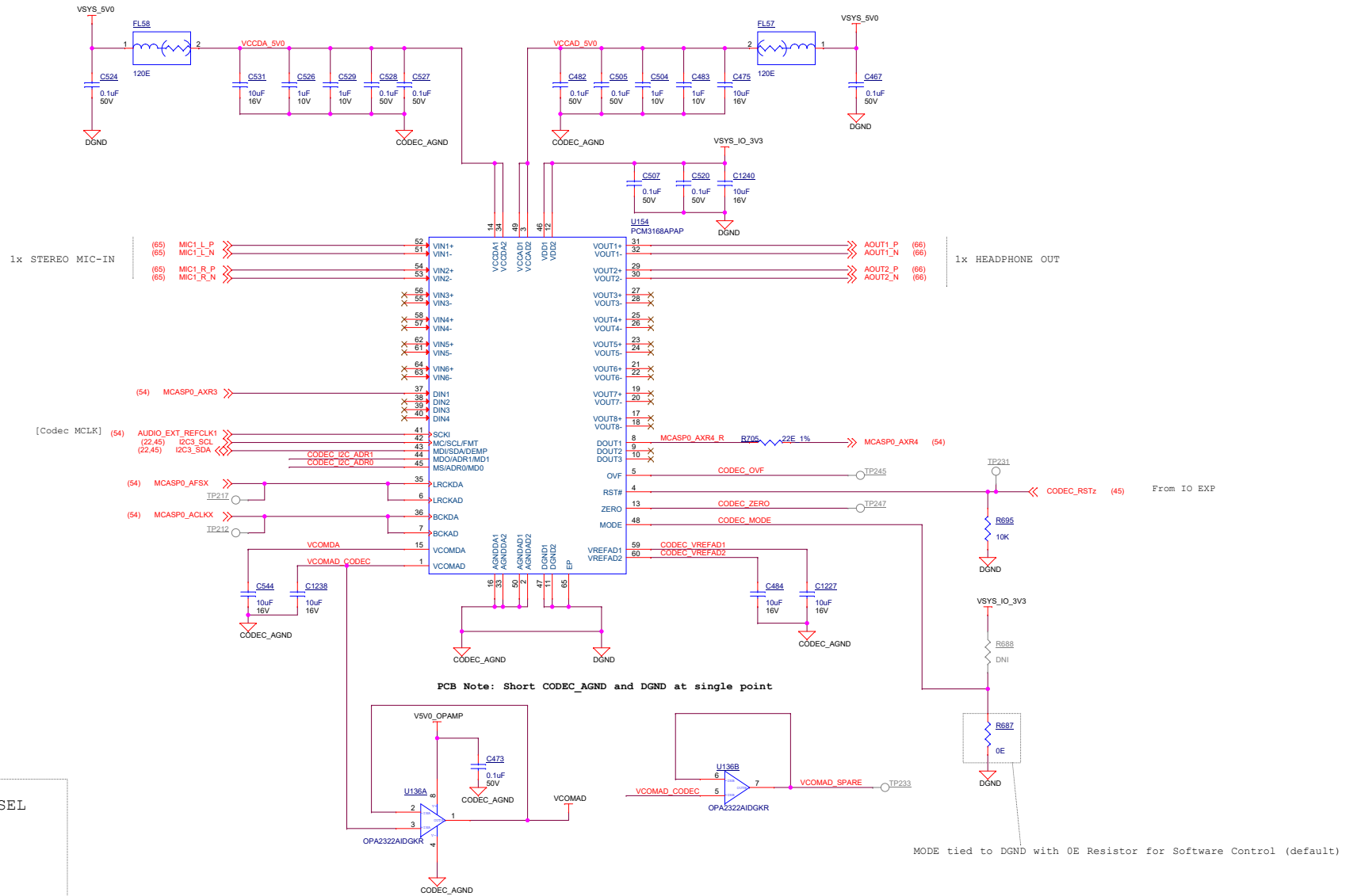
Set Mode 3 [Autoneg Disable - 0]



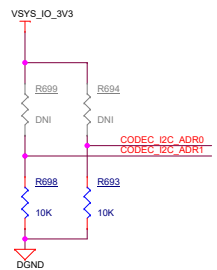
Project : J7 EVM	Title RGMII1	
	Size	PROC141 001 J78454XG01EVM
	C	E3
	Date: Wednesday, July 27, 2022	Sheet 63 of 88



AUDIO I/F CODEC



I2C Address SEL



7b' I2C Address 0x44 (default)

Project :

J7 EVM



Title AUDIO I/F CODEC

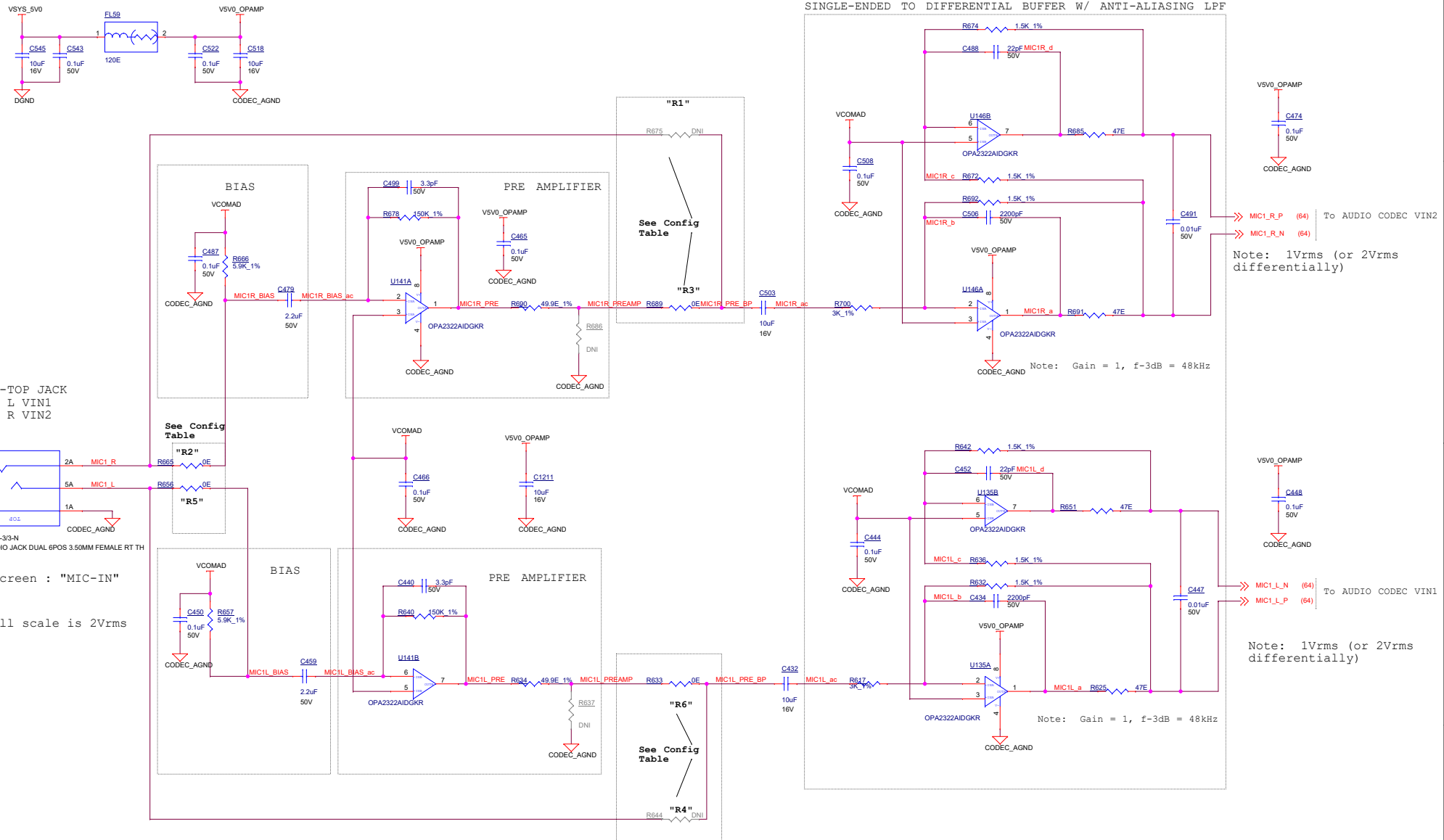
Size PROC141 001 J784S4XG01EVM

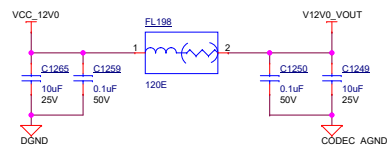
C Date: Wednesday, July 27, 2022

Rev E3

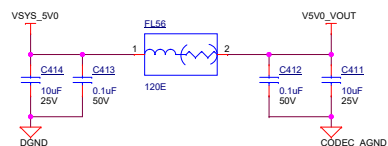
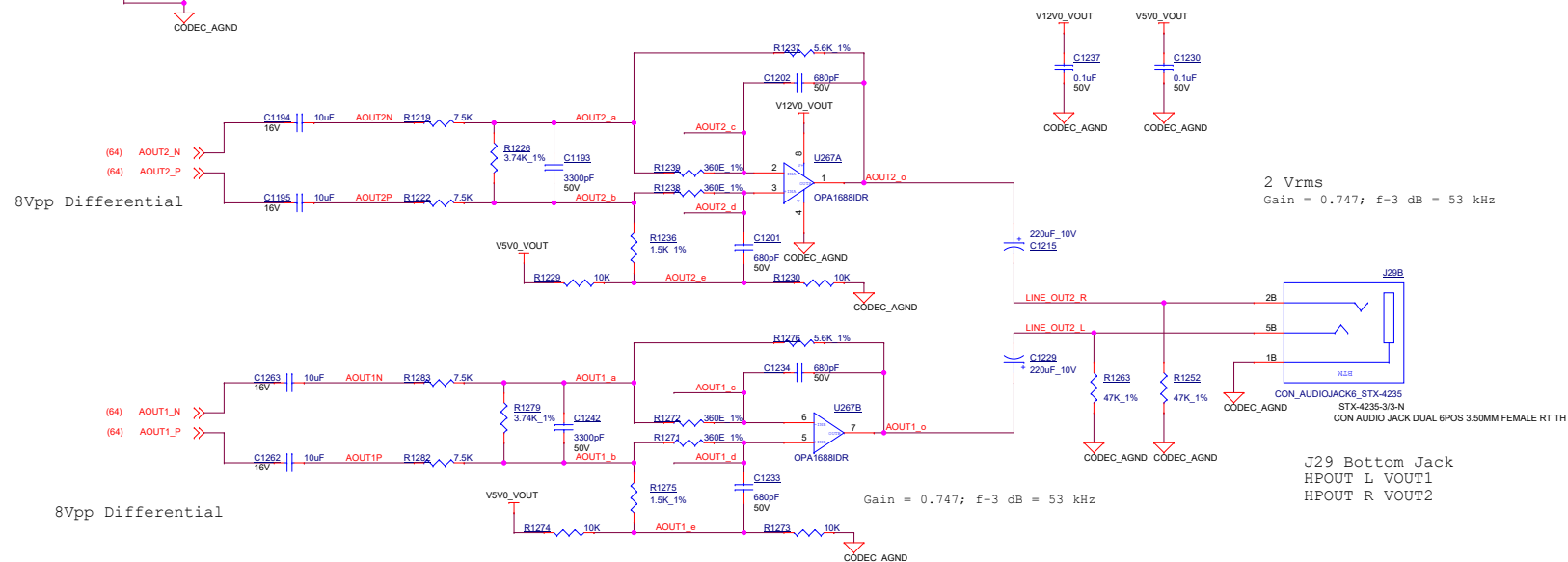
Sheet 64 of 88

AUDIO I/F - STEREO MIC #1





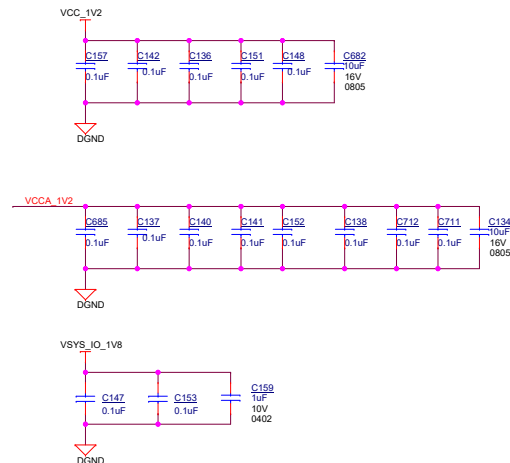
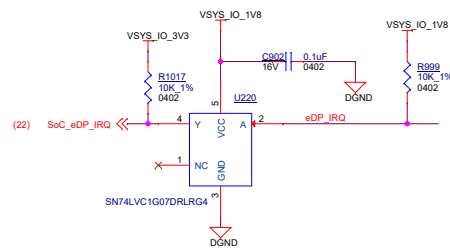
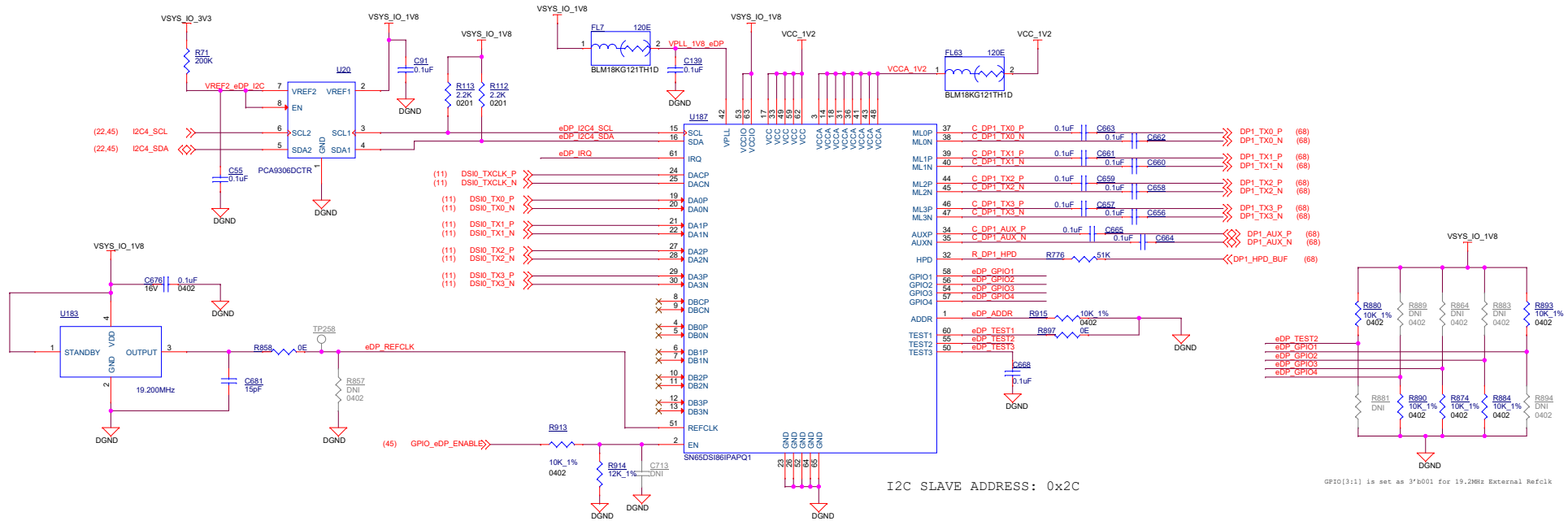
AUDIO I/F - STEREO HEADPHONE OUT # 1



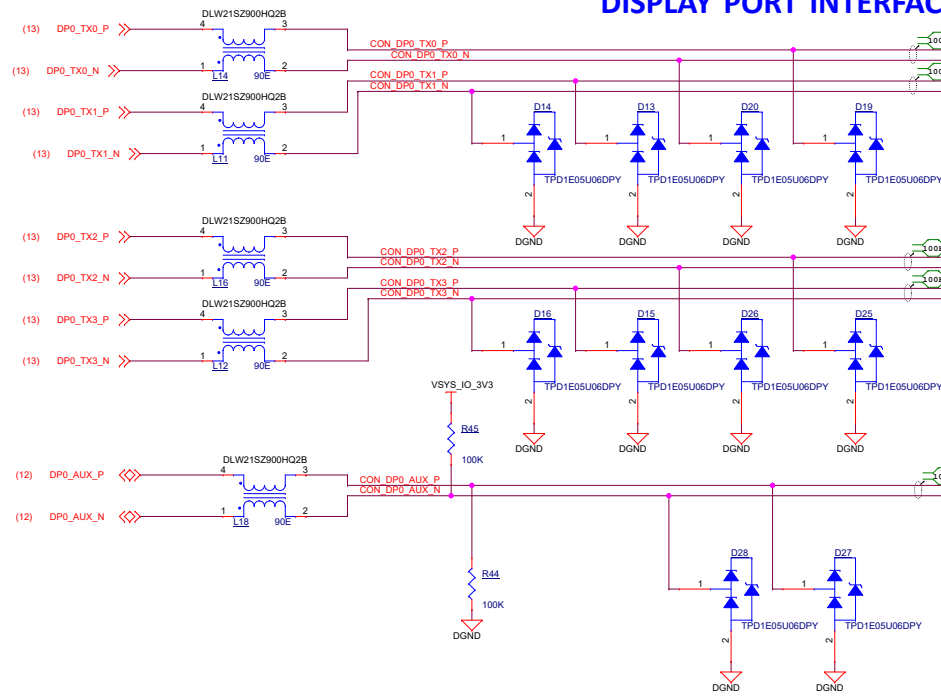
Project :		Title	
J7 EVM		AUDIO I/F - STEREO LINE OUT & HP OUT# 1	
Size		PROC141 001 J784S4XG01EVM	Rev
C			E3
Date:		Wednesday, July 27, 2022	Sheet 66 of 88



DSI to eDP Bridge



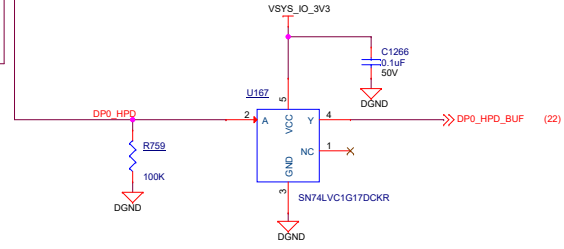
DISPLAY PORT INTERFACE



Display Port Connector1

Silkscreen: "DISPLAY
PORT CONN0"

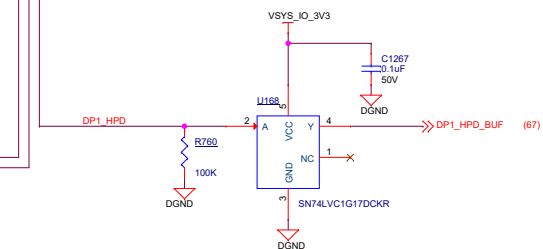
PCB Note: Place the ESD diodes close to DISPLAY PORT CONN1



Display Port Connector2

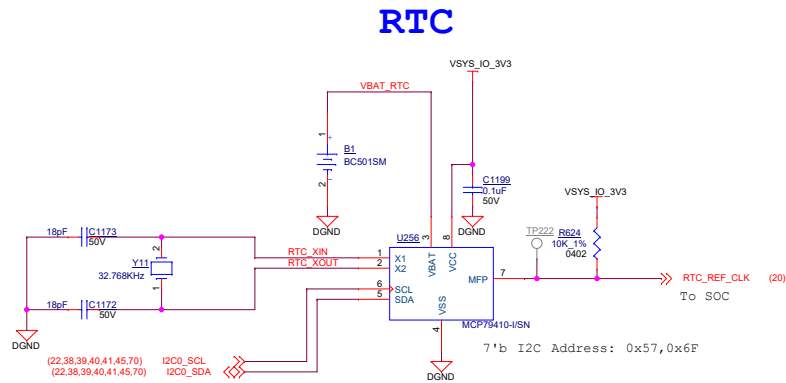
Silkscreen: "DISPLAY
PORT CONN1"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN2

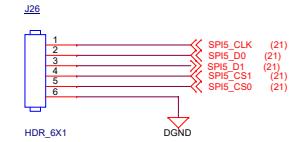


Project :		Title	
J7 EVM		DISPLAY PORT INTERFACE	
Size	PROC141 001 J784S4XG01EVM	Rev	
C			E3
Date:	Thursday, September 15, 2022	Sheet	68 of 68

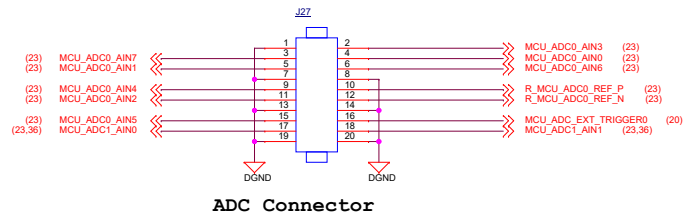




SPI Header



ADC INTERFACE



I3C Header

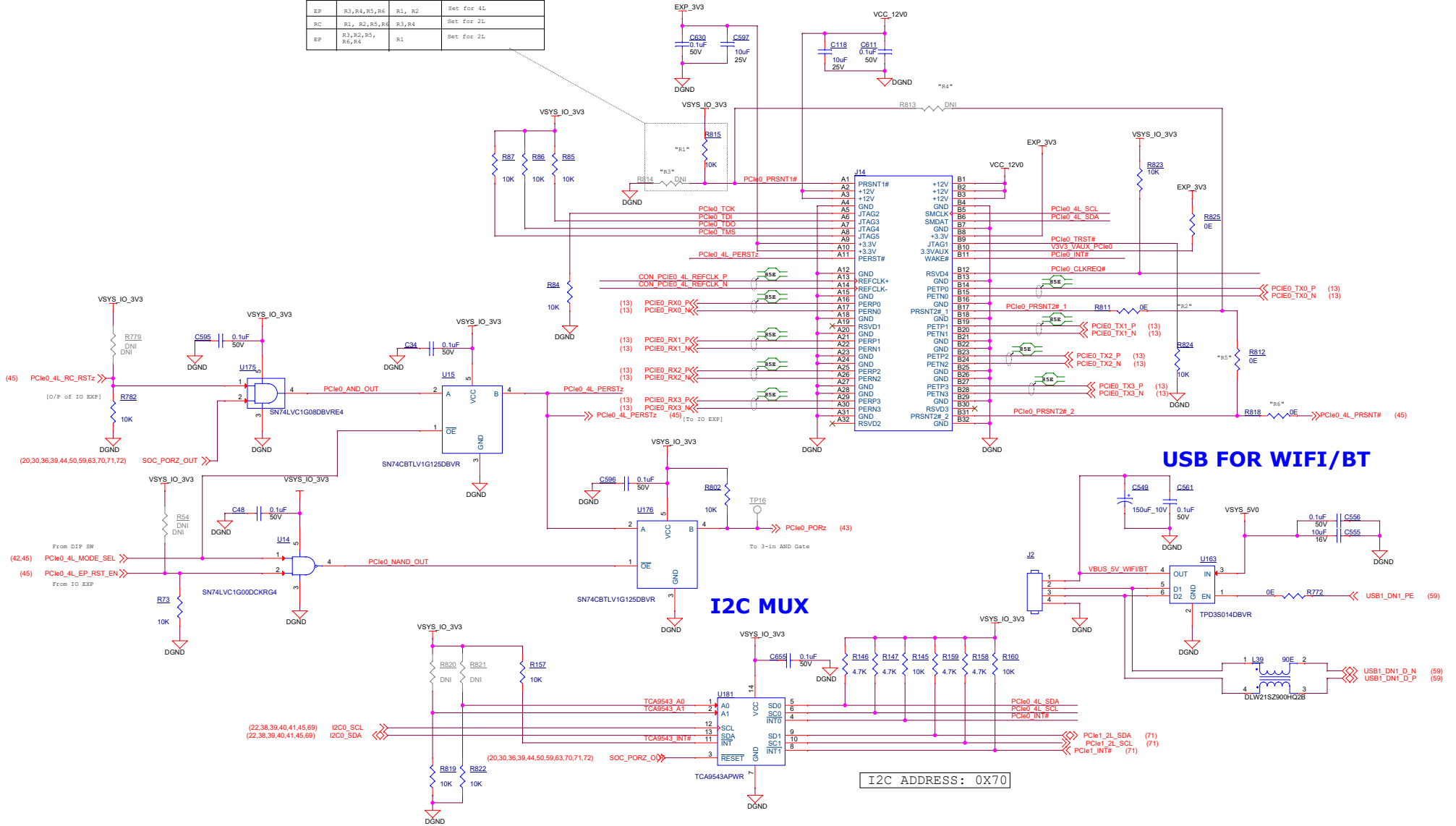


Silk Screen MCU-I3C

x4LANE PCIe0 Interface

x4 Lane PCIe Connector

MODE	INSTALL	DN1	PCIe Lanes
RC	R1, R6	R3, R4, R2, R5	Set for 4L
EP	R3, R4, R5, R6	R1, R2	Set for 4L
RC	R1, R2, R5, R6	R3, R4	Set for 2L
EP	R3, R2, R5, R6, R4	R1	Set for 2L



Project :

J7 EVM



Title
x1LANE PCIe INTERFACE

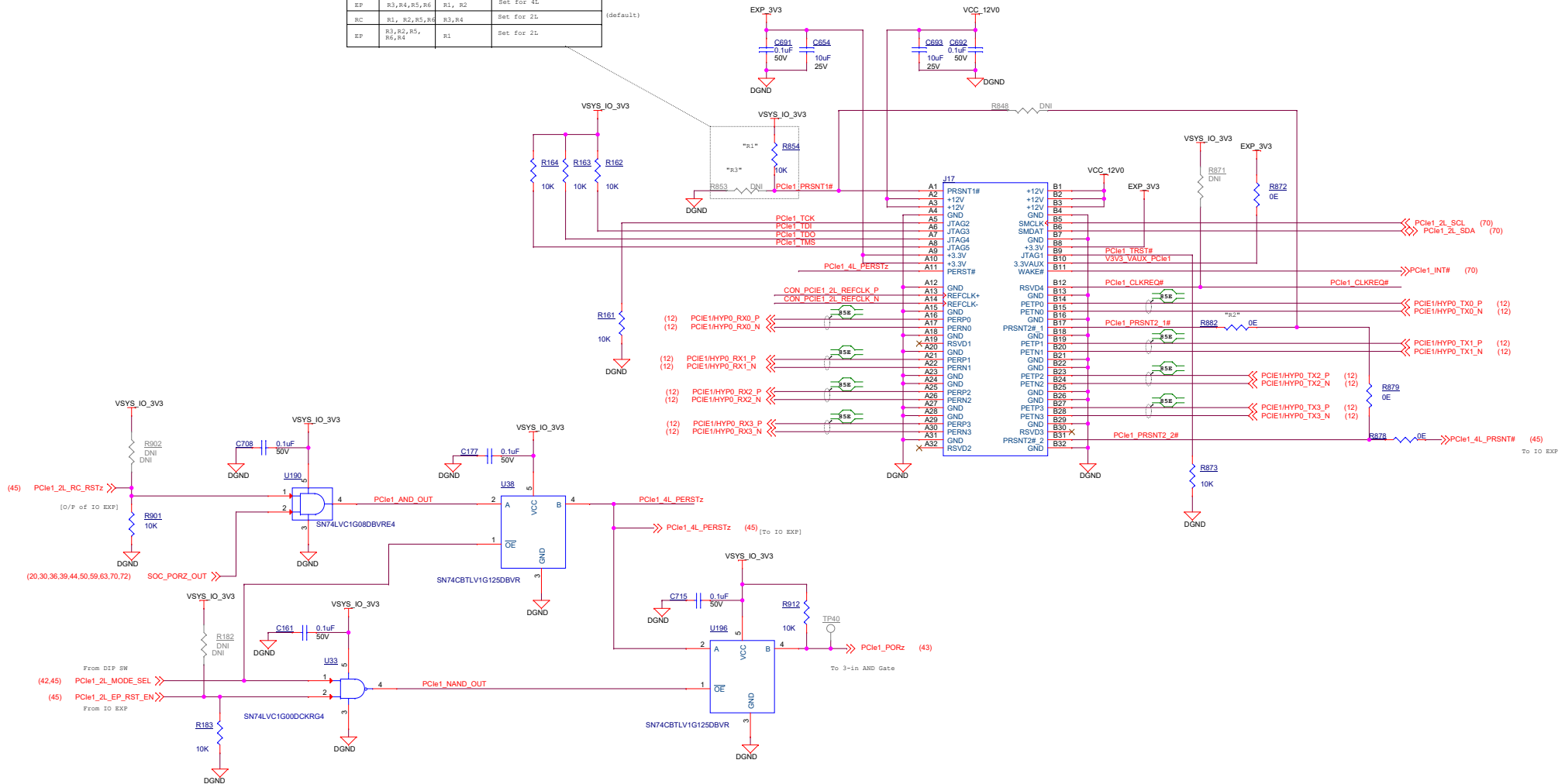
Size
PROC141 001 J784S4XG01EVM

C
Date: Thursday, September 15, 2022

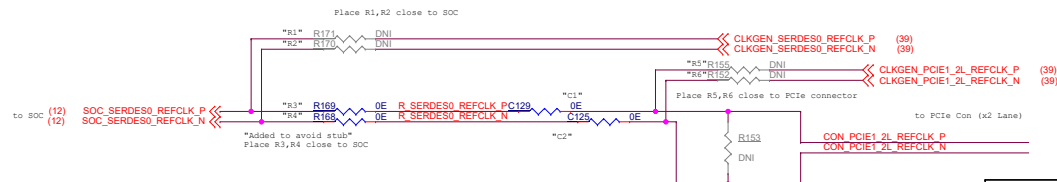
Rev
E3

Sheet 70 of 88

MODE	INSTALL	DNI	PCIe Lanes
RC	R1, R6	R3,R4,R2,R5	Set for 4L
EP	R3,R4,R5,R6	R1, R2	Set for 4L
RC	R1, R2,R5,R6	R3,R4	Set for 2L
EP	R3,R2,R5, R6,R4	R1	Set for 2L

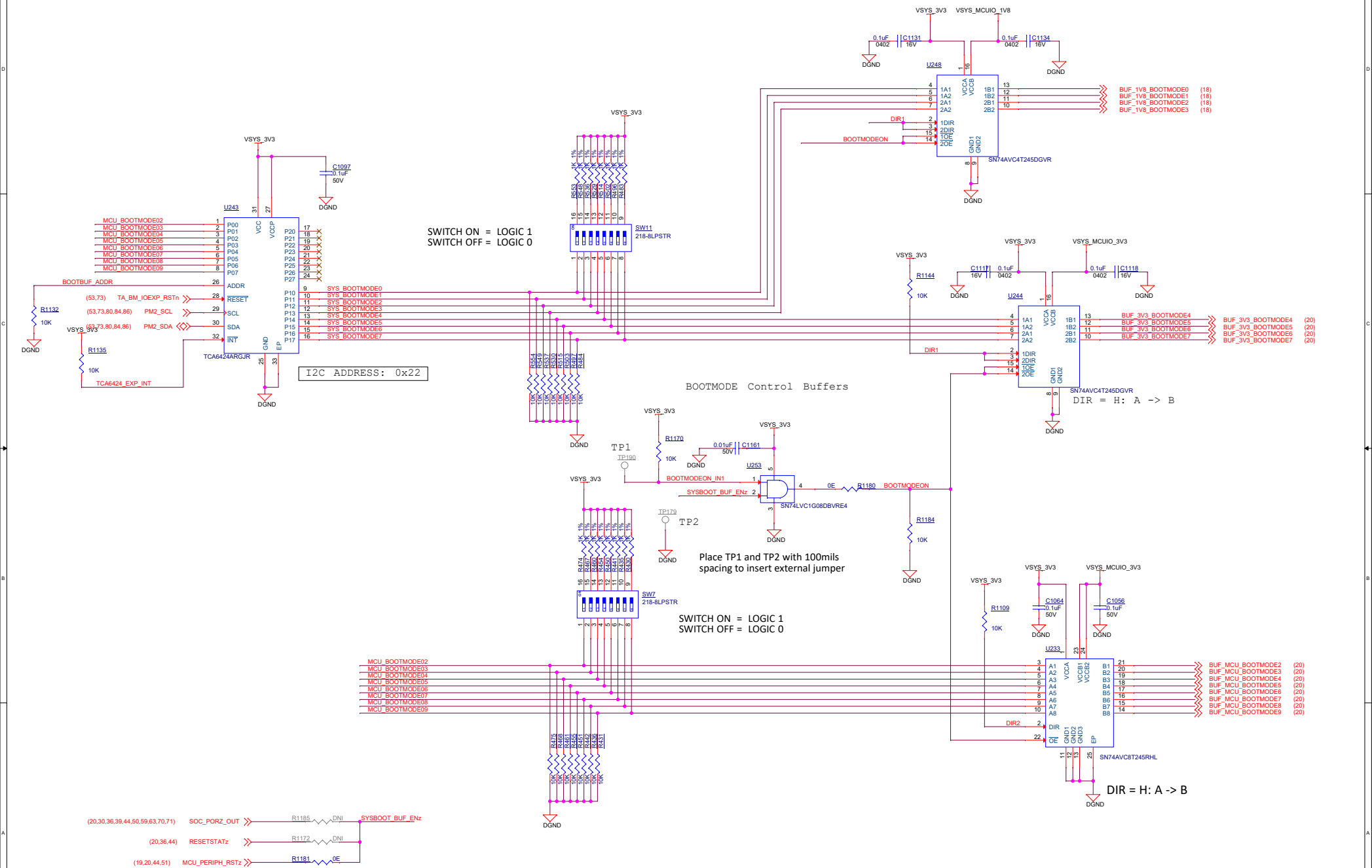


	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,
PCIe end point	R3,R4,C1,C2	R1,R2,R5,



Title			
x2LANE PCIe Interface			
Size	PROC141 001 J784S4XG01EVM		Rev
C			E3
Date:	Wednesday, July 27, 2022	Sheet	71 of 88

BOOT MODE BUFFER & SWITCHES



TA_BM_IOEXP_RSTn	SOC_PORZ_OUT	BOOTMODE Contro. from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

Project :

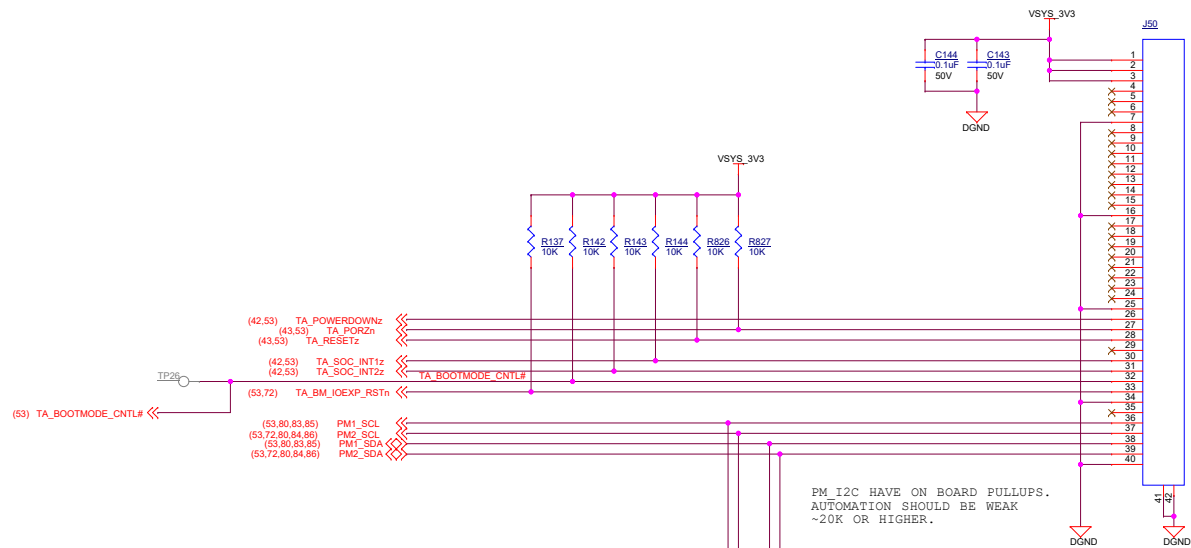
J7 EVM



Title	BOOT MODE BUFFER & SWITCHES
-------	-----------------------------

Size	PROC141 001 J784S4XG01EVM	Rev
C		E3
Date:	Wednesday, July 27, 2022	Sheet 72 of 88

TEST AUTOMATION HEADER

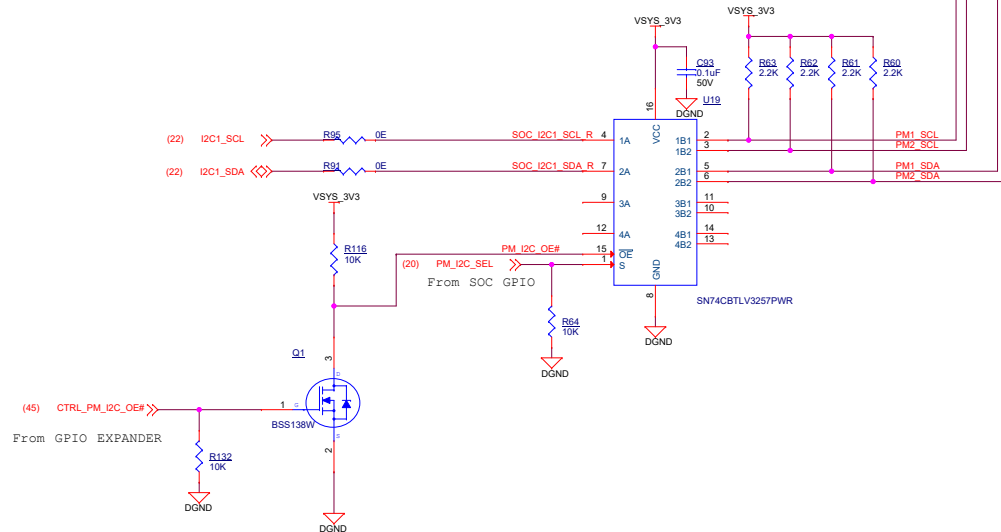


AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE
REFERENCED TO EVM_3V3

Cable : Parlex-050R40-76B, .5mm 3"

I2C SWITCH

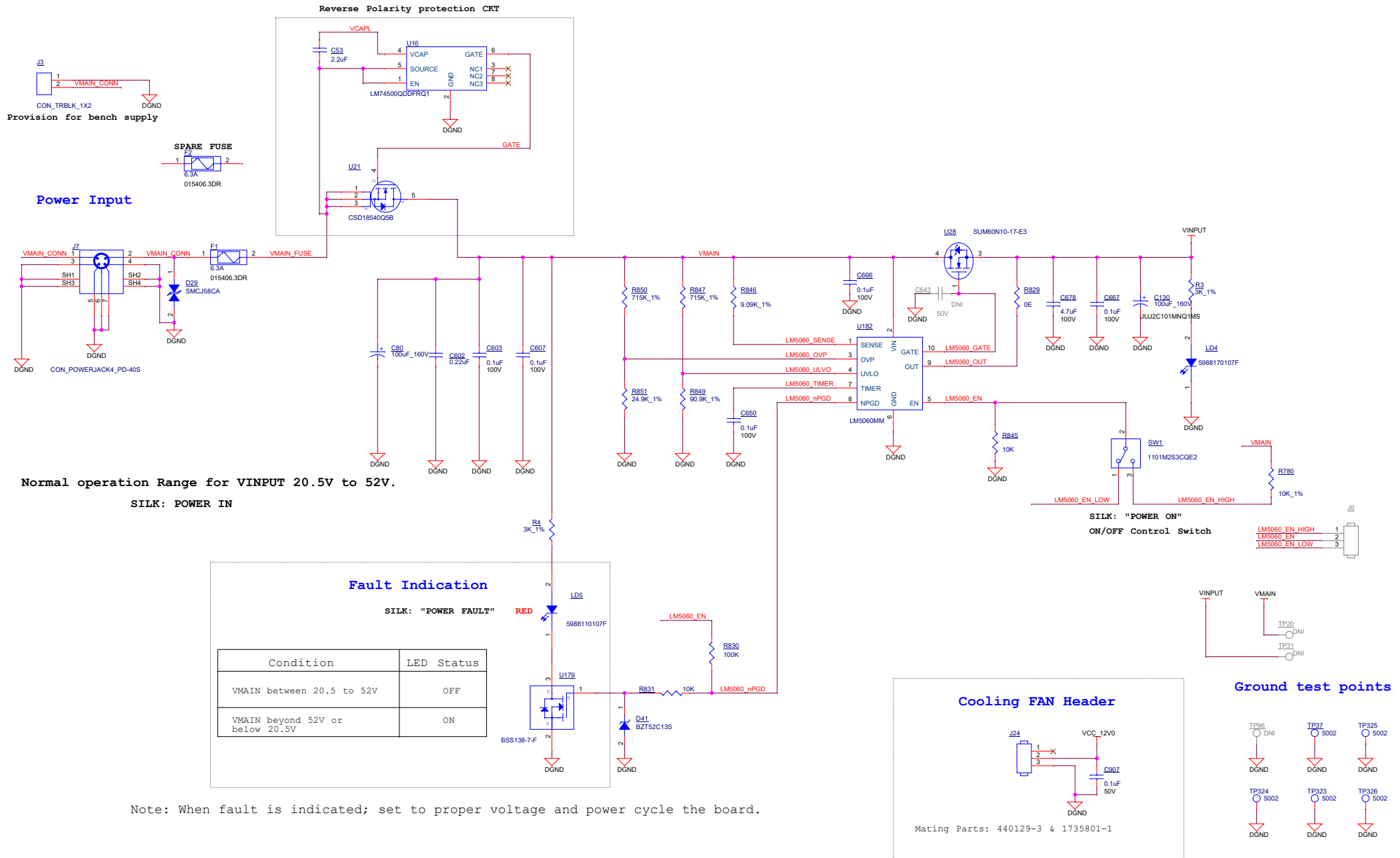


TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

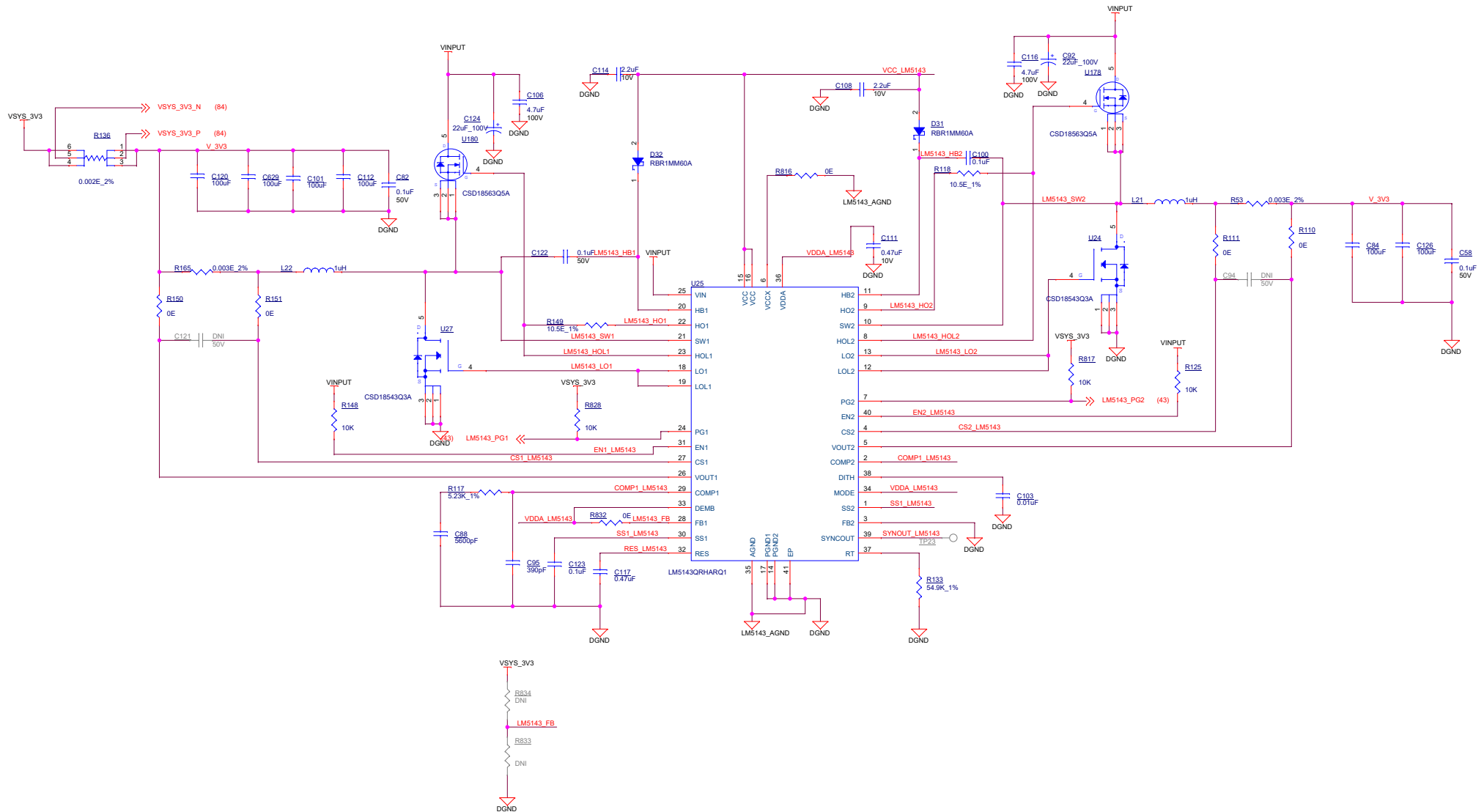
Project : J7 EVM		Title TEST AUTOMATION HEADER	
		Size C	Rev E3
		Date: Wednesday, July 27, 2022	Sheet 73 of 88


OVER VOLTAGE PROTECTION CIRCUIT



TI WEBENCH Simulation Inputs:
 Vin (min) = 24V Vin (max) = 48V
 Vout = 3.3V@30A
 Ta = 25 deg

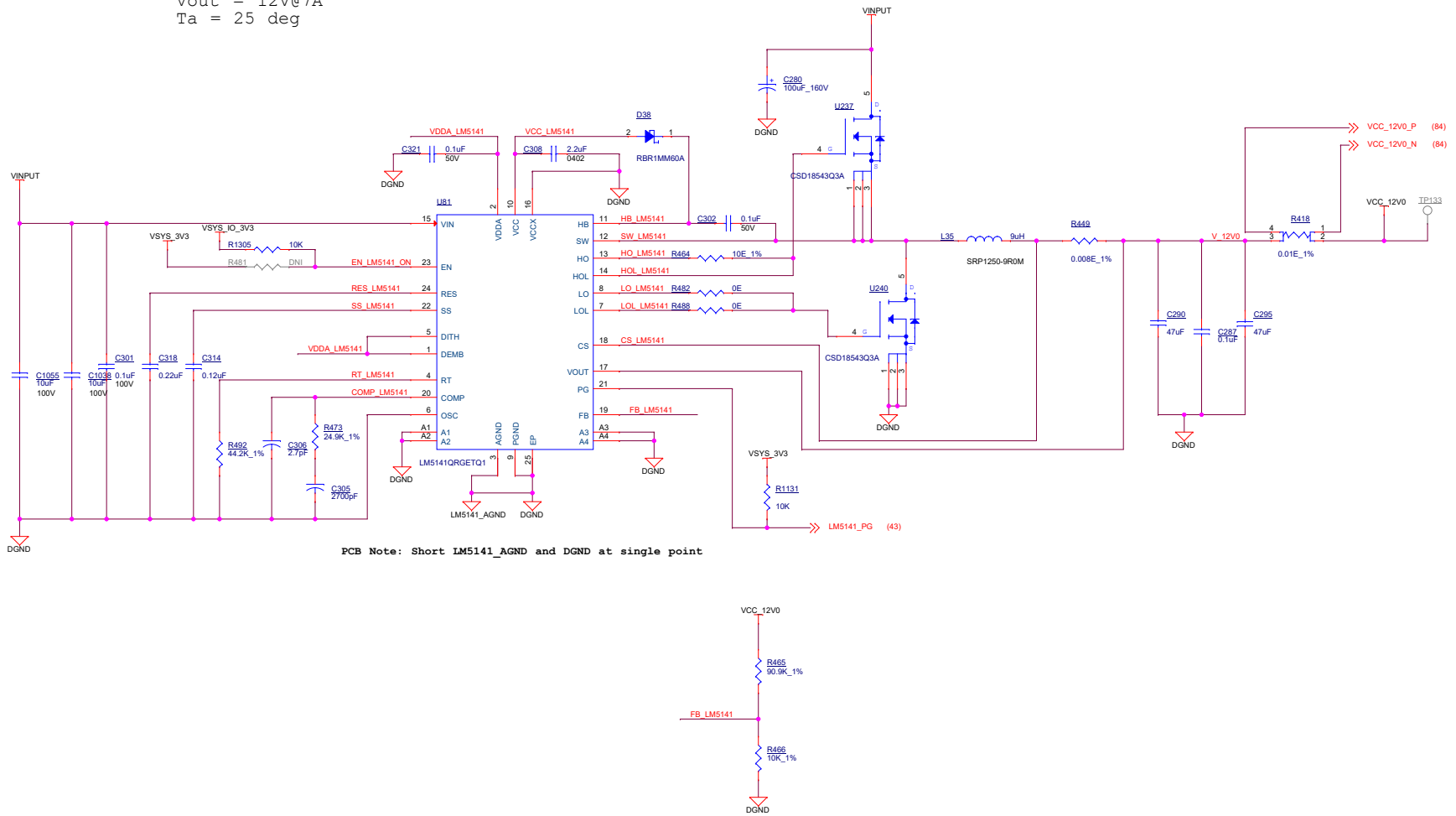
POWER SUPPLY #1



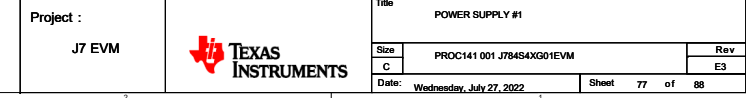
Project : J7 EVM		Title POWER SUPPLY #3		
		Size	PROC141 001 J78454XG01EVM	Rev
		C		E3
		Date:	Wednesday, July 27, 2022	Sheet 75 of 88

POWER SUPPLY #2

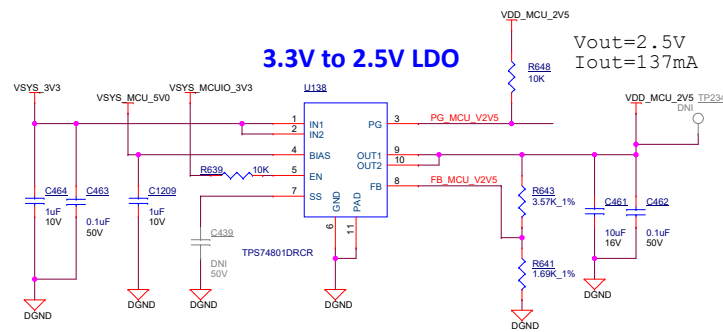
TI WEBENCH Simulation Inputs:
 Vin (min) = 24V Vin (max) = 48V
 Vout = 12V@7A
 Ta = 25 deg



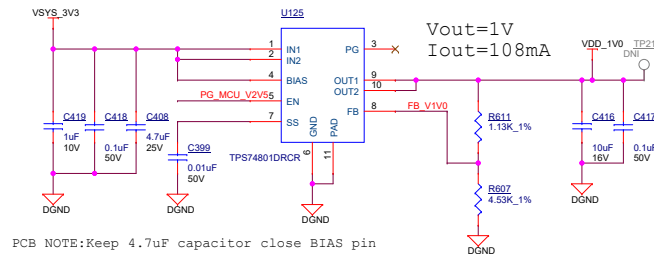
TI WEBENCH Simulation Inputs:
Vin (min) = 6V Vin (max) = 28V
Vout1 = 3.3V@10A; Vout2 = 5V@7A
Ta = 25 deg



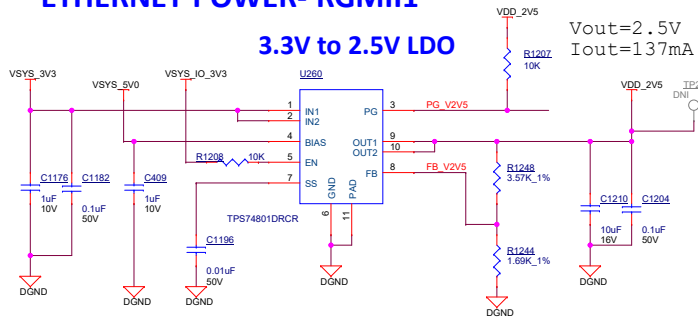
ETHERNET POWER- MCU RGMII



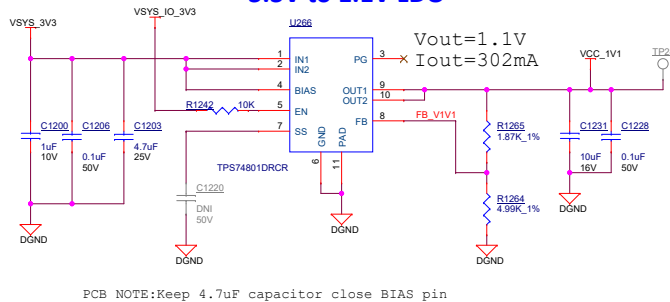
3.3V to 1.0V LDO



ETHERNET POWER- RGMII1

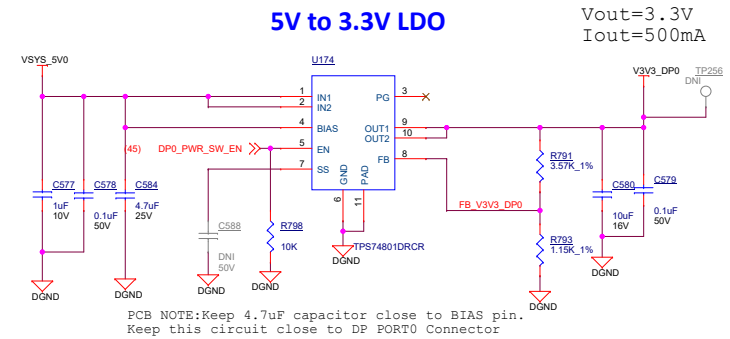


3.3V to 1.1V LDO

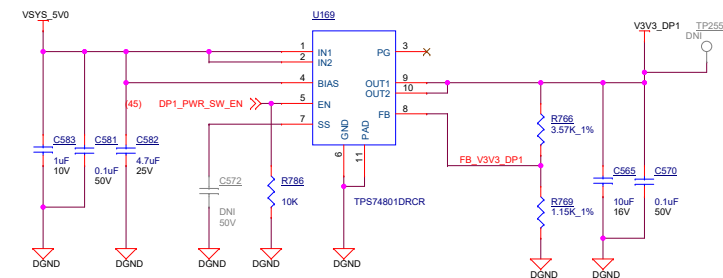


POWER SUPPLY #4

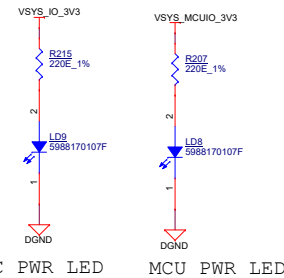
Display Port0



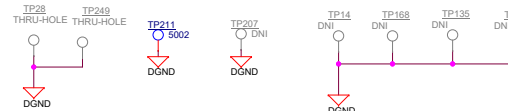
Display Port1 5V to 3.3V LDO



POWER INDICATION LED'S



GROUND TEST POINTS



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

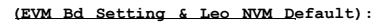
Project :

J7 EVM

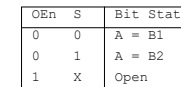


Title		
POWER SUPPLY #4		
Size	PROC141 001 J784S4XG01EVM	Rev
C		E3
Date:	Wednesday, July 27, 2022	Sheet 78 of 88

EVM development & evaluation Test circuitry
(TI EVM Only)

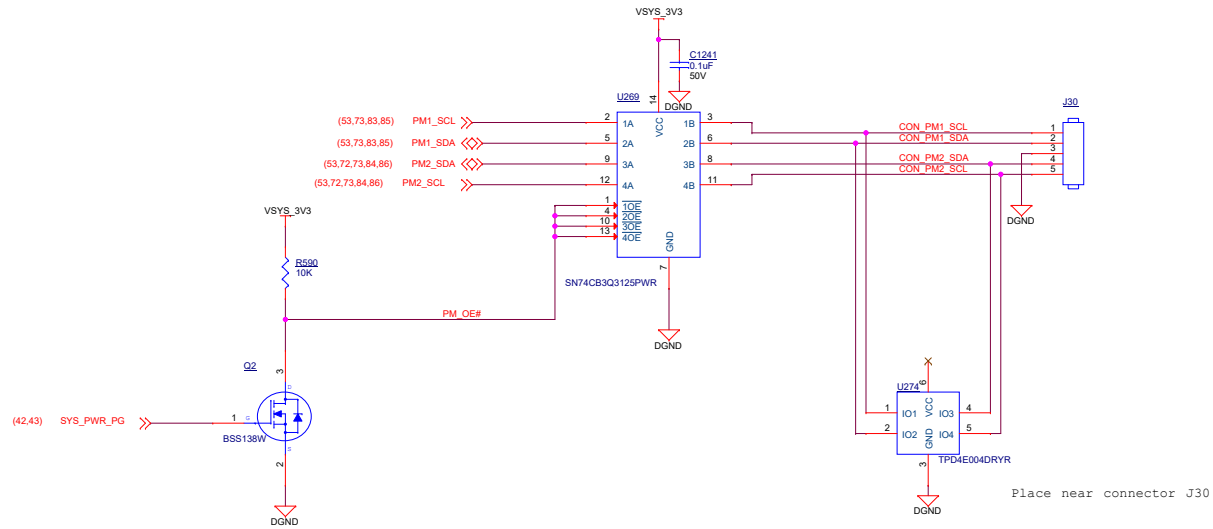


SW16	Function
-1 = Closed (High) = Open (Low)	Enable the PMIC by overriding SYS_MCU_ENABLE Enable the PMIC from SYS_MCU_EN
-2 = Closed (High) = Open (Low)	ENABLE SVS_EN from SW16.2 ENABLE SVS_EN FROM SYS_MCU_EN
-3 = Closed (High) = Open (Low)	1. PMIC_EN from SYS_MCU_EN 2. On Board WKUP I2C0 is selected 3. SVS_EN is controlled from SYS_MCU_EN 1. PMIC_EN is controlled from SW16.1 2. EXT_I2C is selected 3. SVS_EN is controlled from SW16.2
-4 = Closed (High) = Open (Low)	Disable WDOG Timer Enable WDOG Timer



EVM POWER MEASUREMENT I2C BUS ISOLATION

EVM development & evaluation Test circuitry
(TI EVM Only)



Project :

J7 EVM



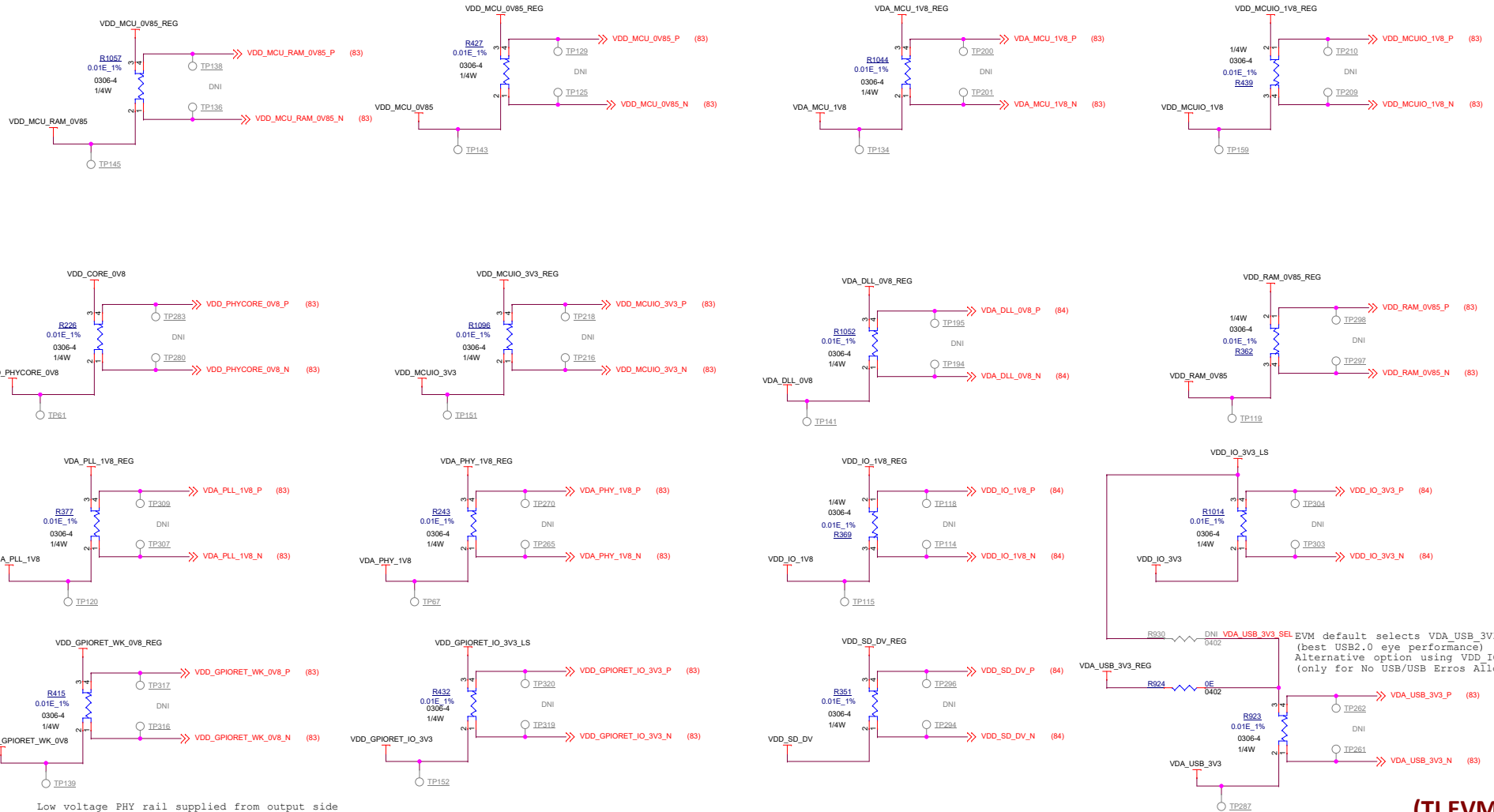
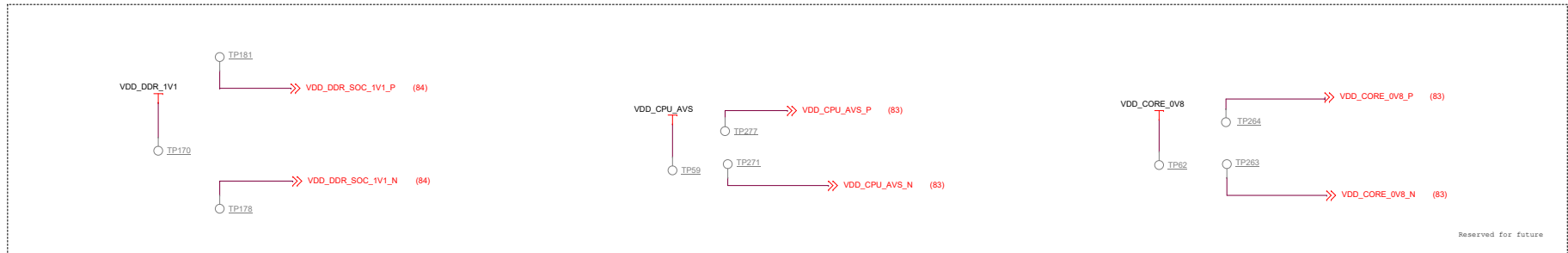
Title
EXTERNAL POWER MEASUREMENT WITH ISOLATION

Size
PROC141 001 J784S4XG01EVM

C
Date: Thursday, September 15, 2022

Rev
E3

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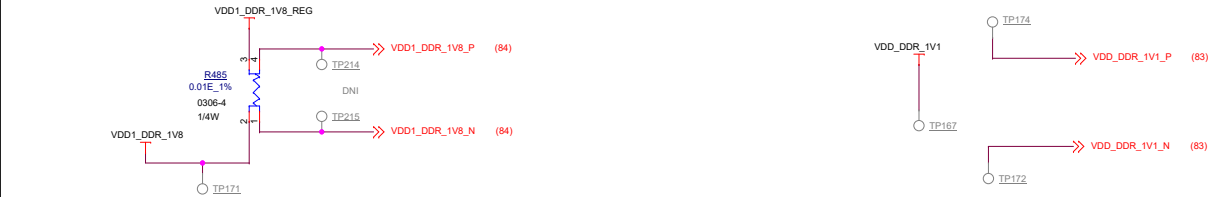


Project :		Title	
J7 EVM		SOC Current Sense Resistors	
		Size	Rev
		C	E3
Date: Thursday, September 15, 2022		Sheet	81 of 88

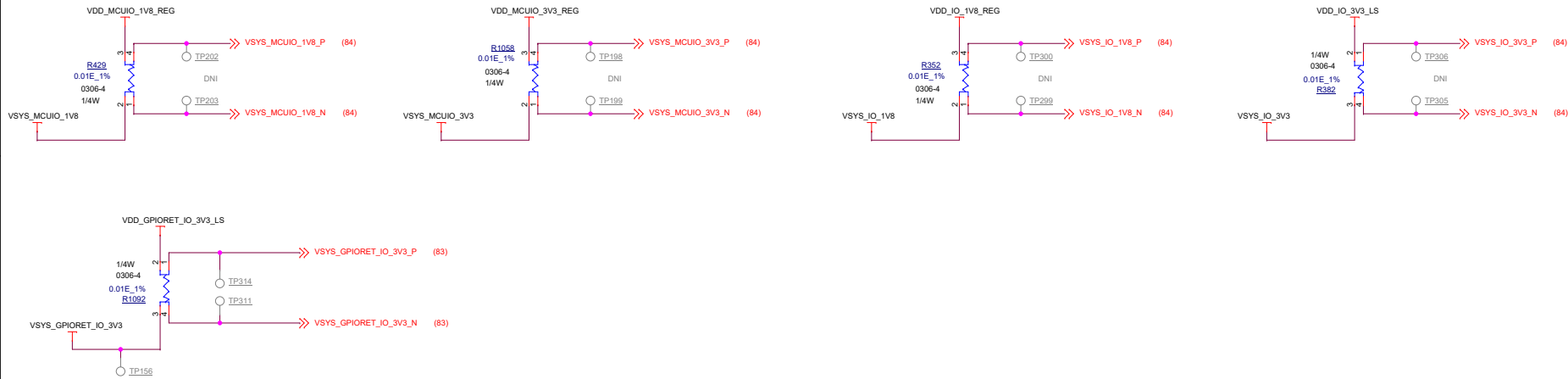


EVM development & evaluation on test circuitry

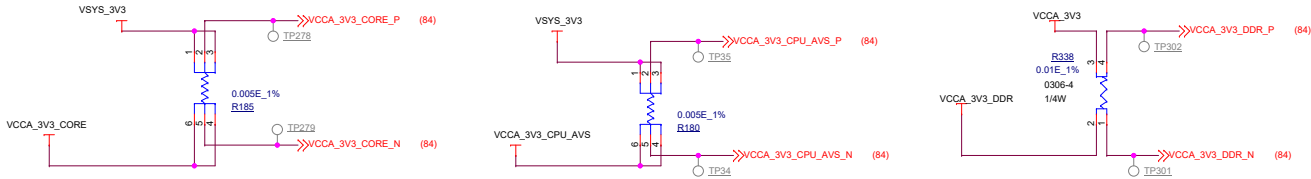
LPDDR4 SDRAM Current Sense Resistors



Peripheral Current Sense Resistors

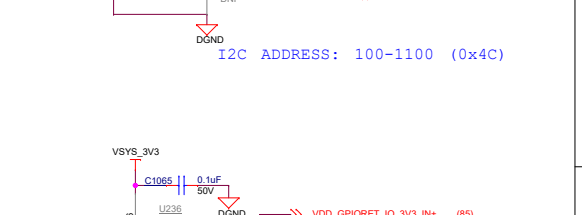
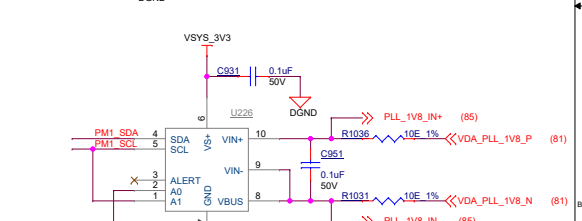
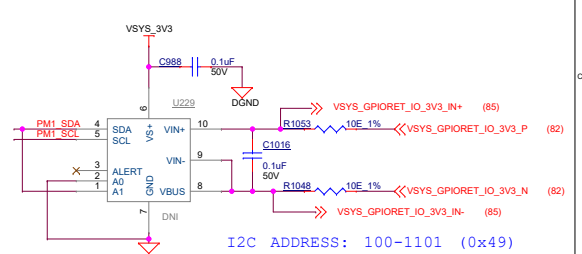
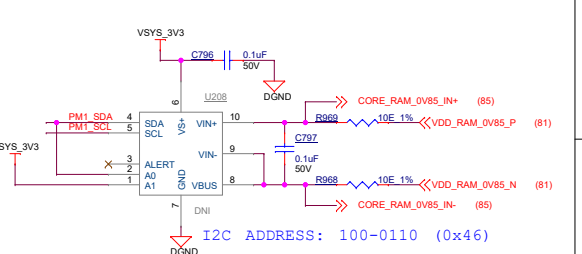
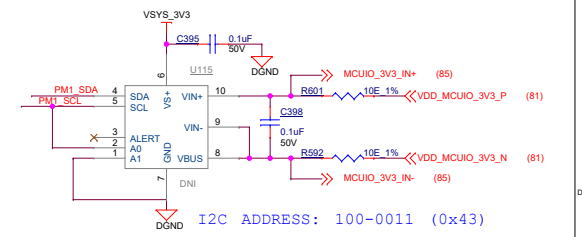
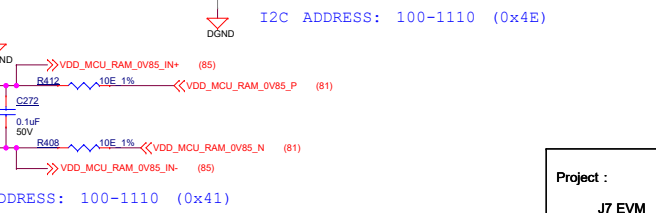
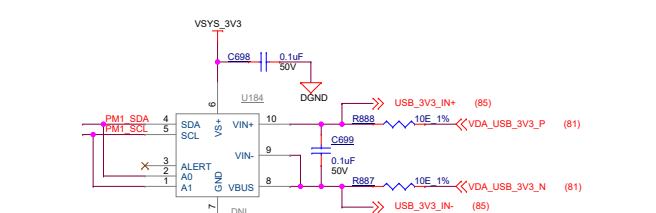
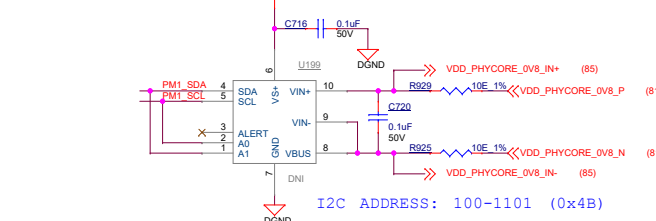
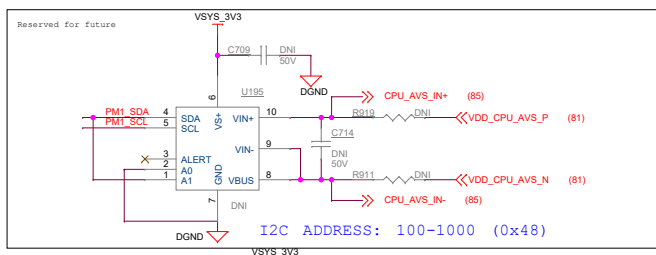
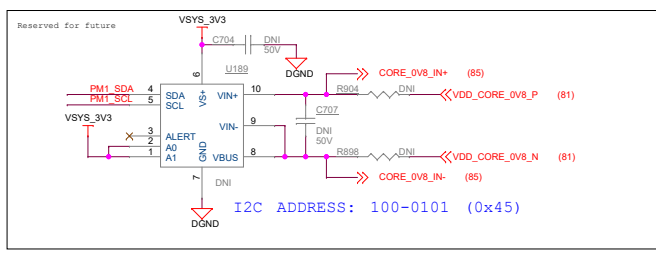
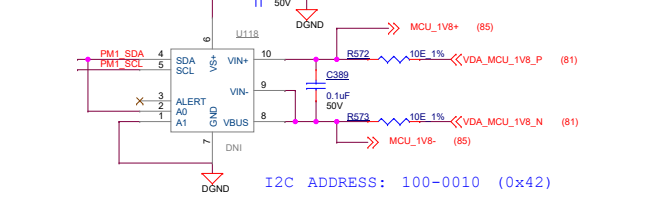
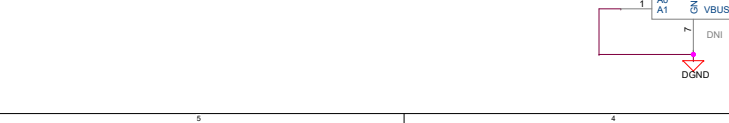
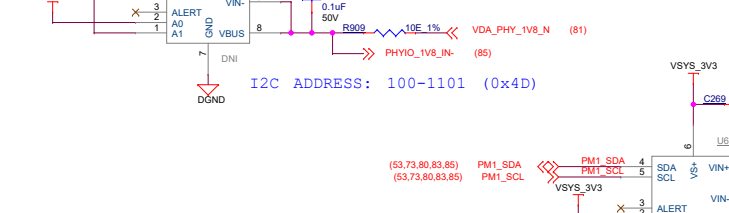
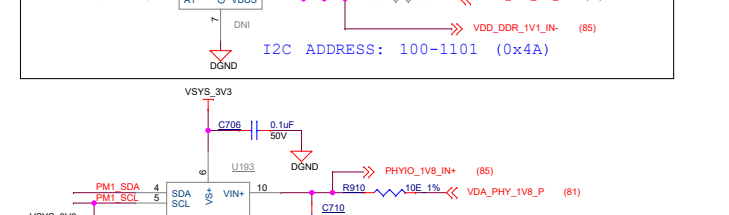
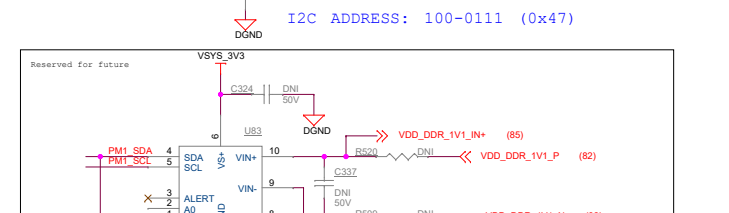
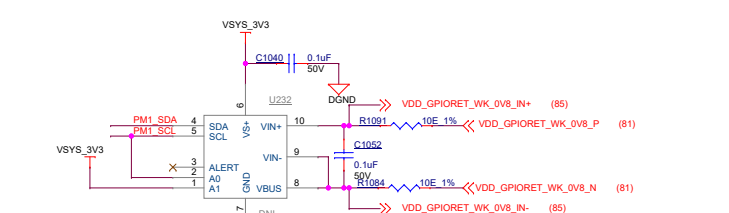
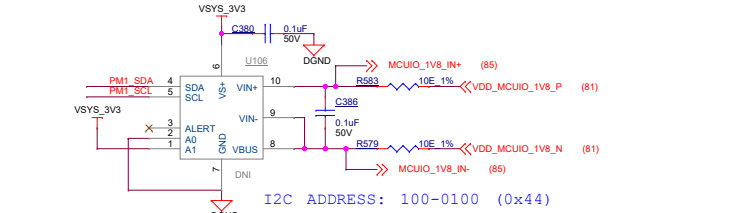
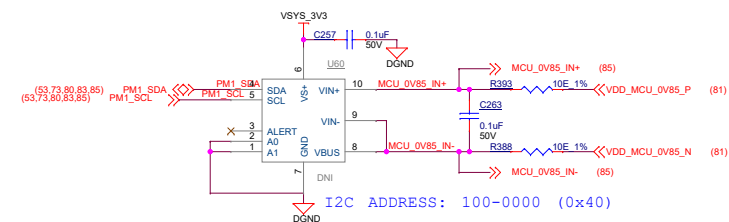


CORE, AVS and DDR input supply sense resistors



Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible - so functionality and performance should not be impacted with either INA

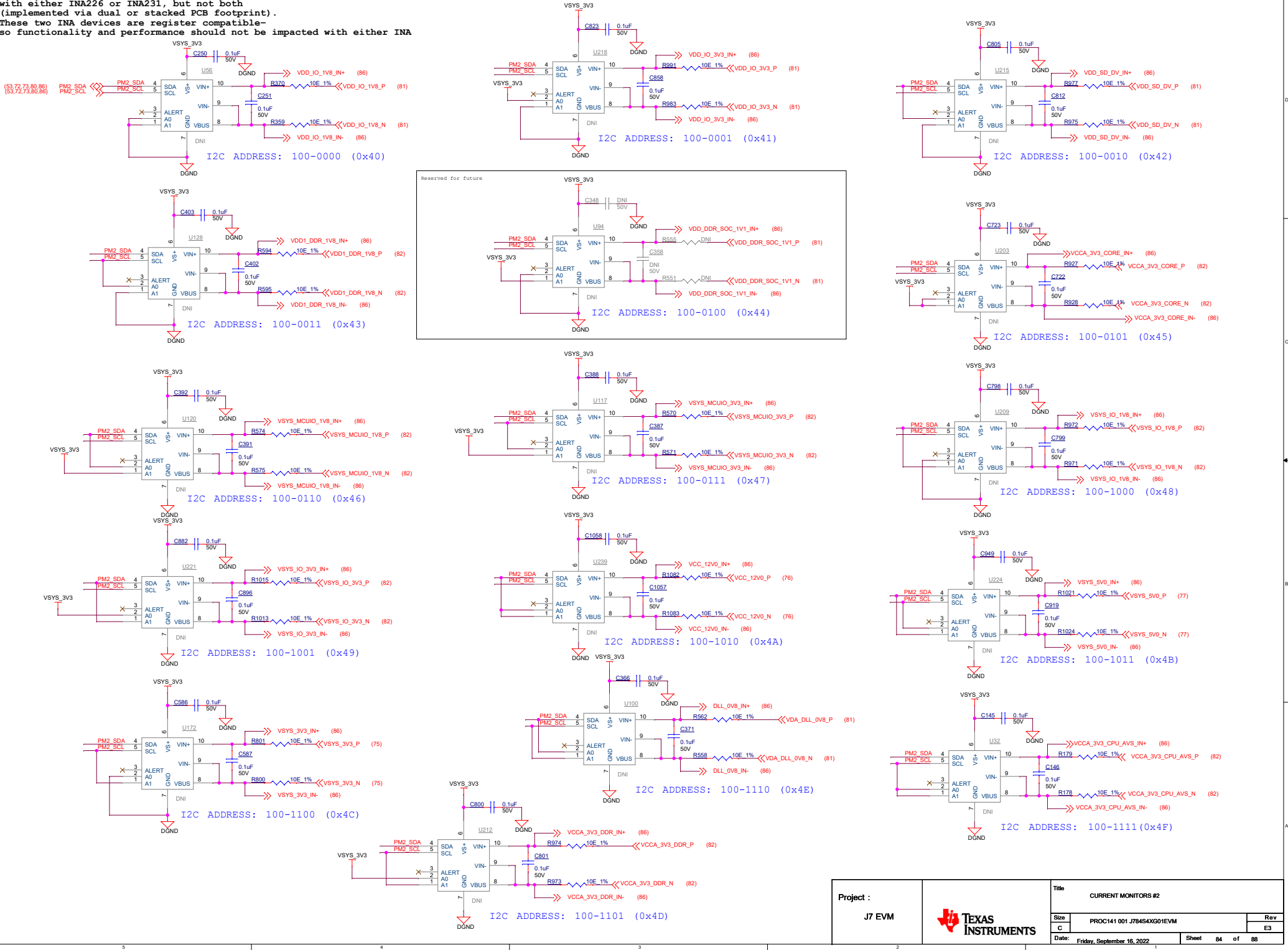
CURRENT MONITORS #1



Project : J7 EVM	Texas Instruments	Title CURRENT MONITORS #1	
		Size C	Rev E3
		Date: Wednesday, July 27, 2022	Sheet 83 of 88

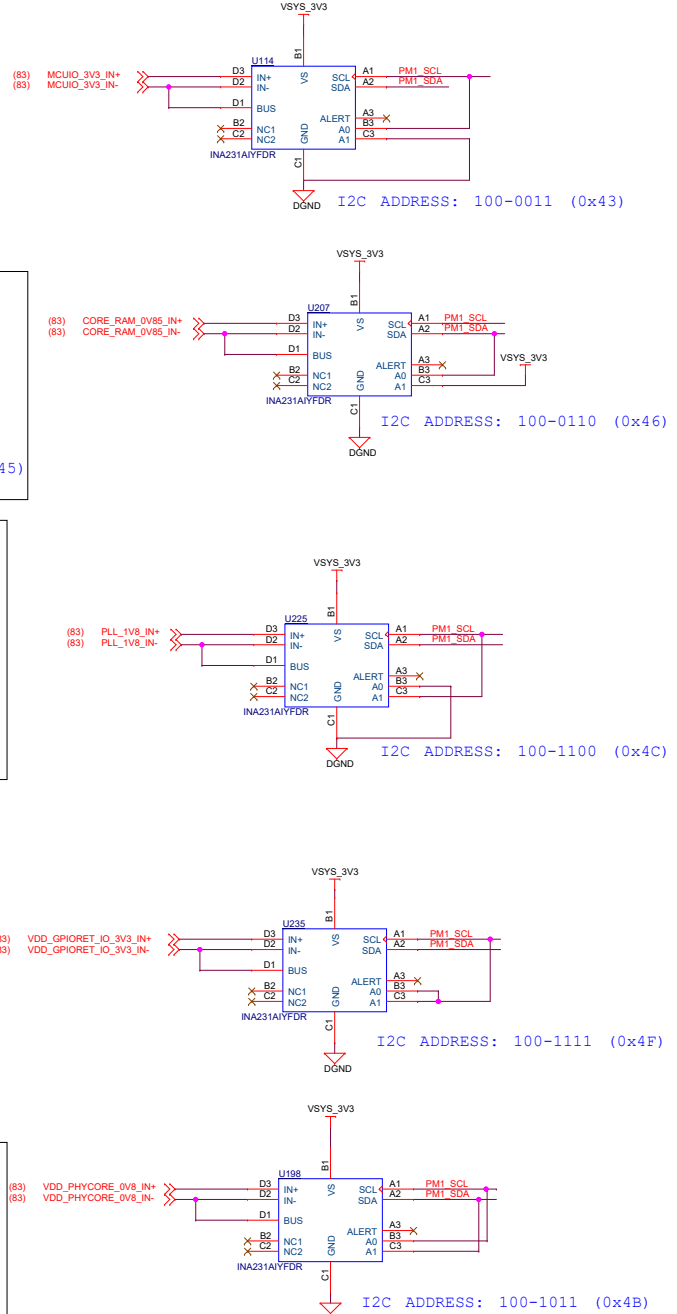
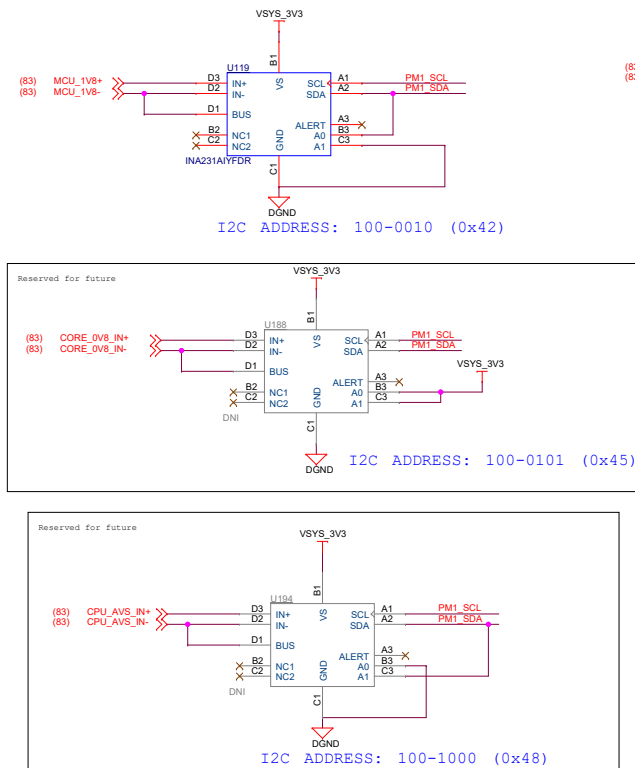
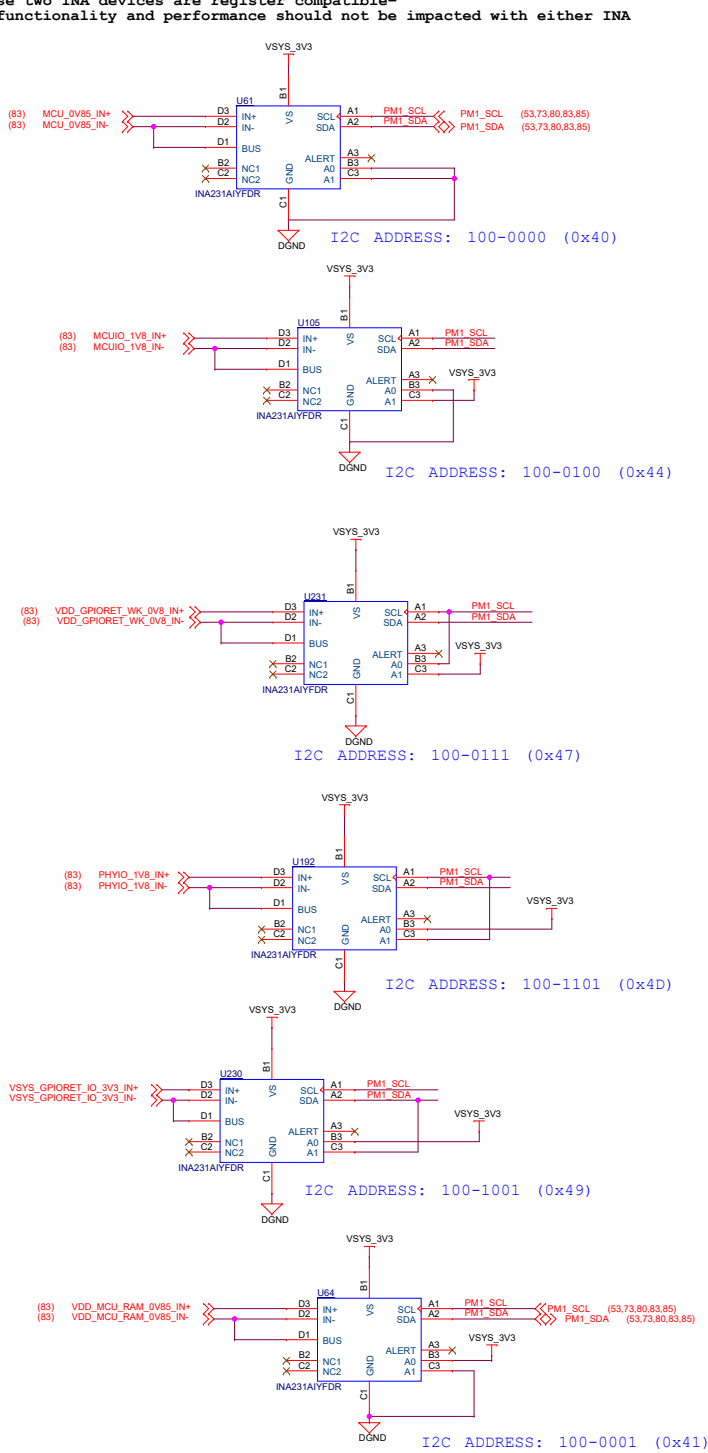
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS #2



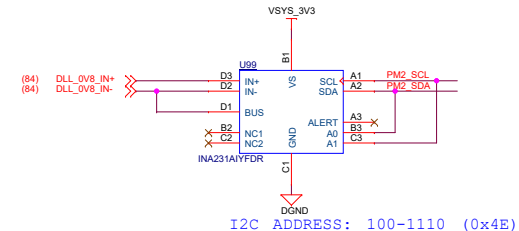
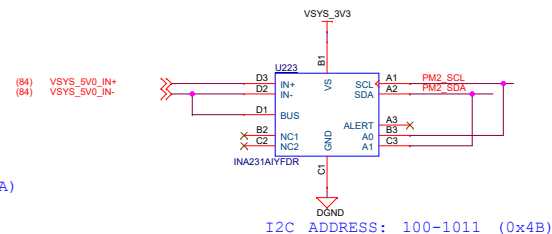
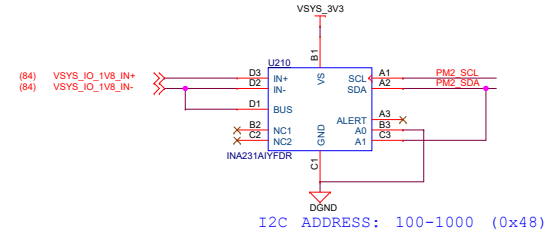
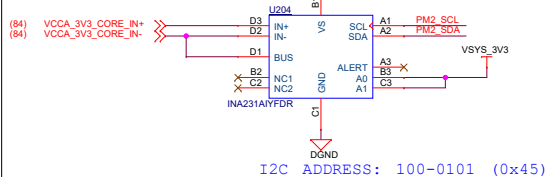
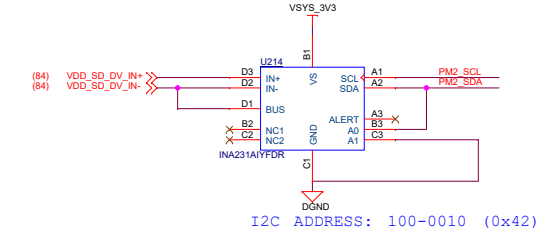
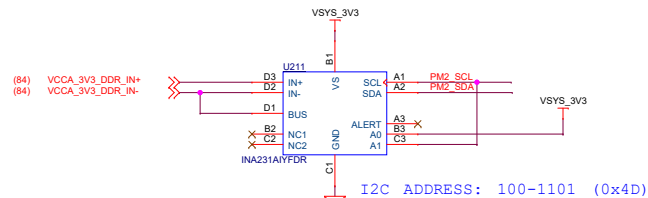
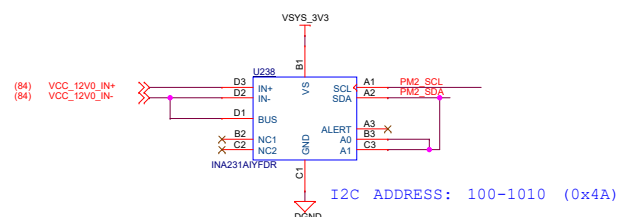
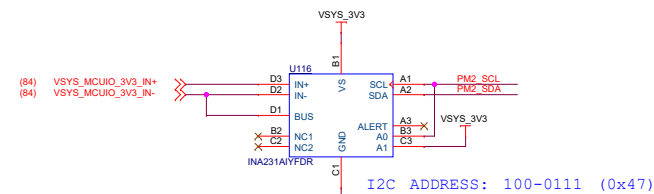
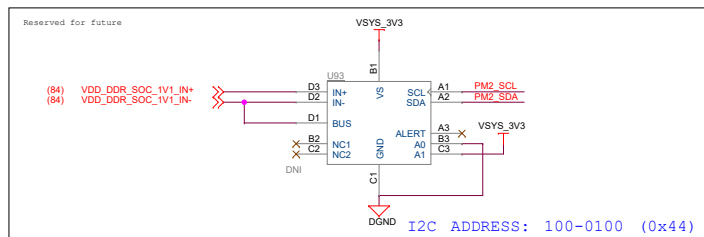
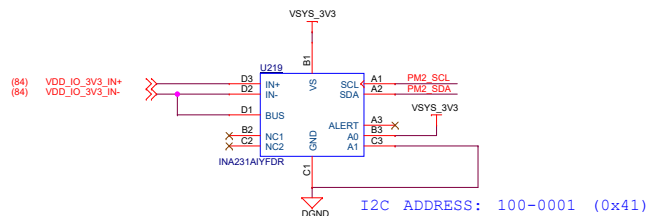
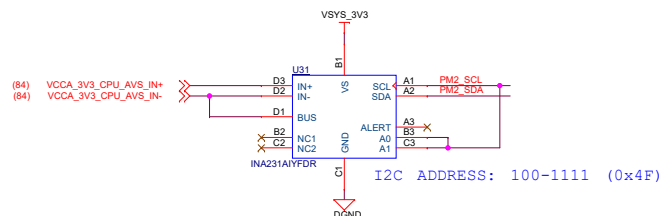
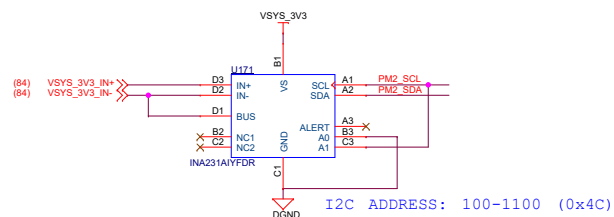
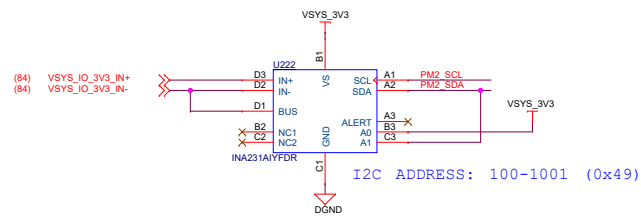
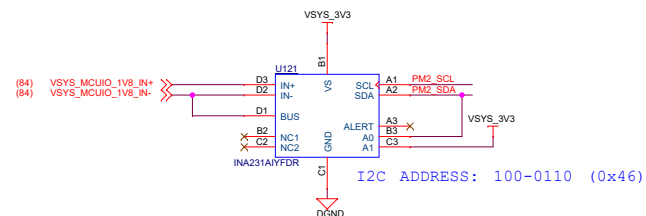
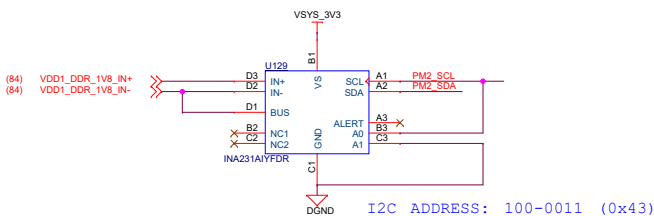
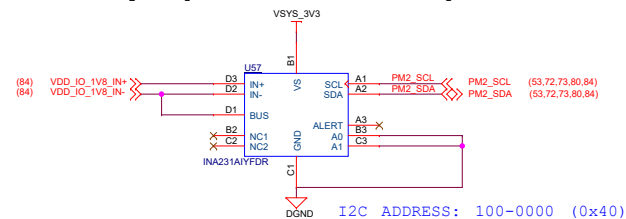
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA231



Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible—so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA231



Project :

J7 EVM



Title
CURRENT MONITORS#2- INA231

Size
PROC141 001 J78454XG01EVM

C
Date: Friday, September 16, 2022

Rev
E3

Sheet 86 of 88

SI_SIMULATION_COUPON_BD

Test coupon not part of EVM design, to be used for TI test only

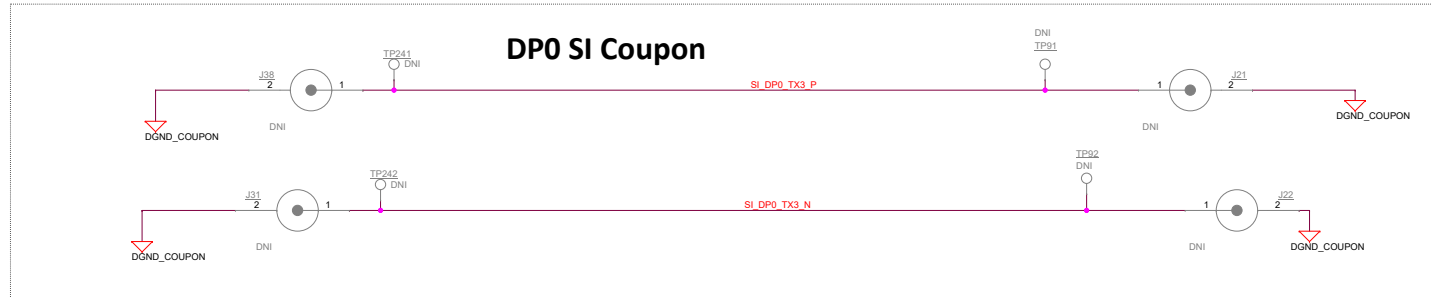
DDR SI Coupon



DDR1 - De-embedding



DP0 SI Coupon



Project :

J7 EVM



Title
SI_SIMULATION_COUPON_BD

Size
PROC141 001 J78454XG01EVM

Rev
E3

Date: Wednesday, July 27, 2022

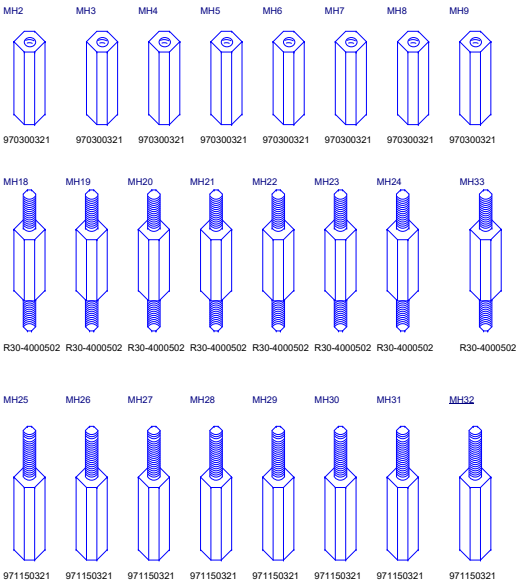
Sheet 87 of 88

HARDWARE SCHEMATICS

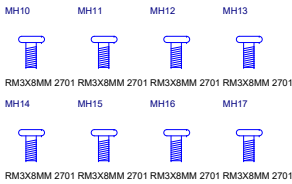
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

STANDOFFS



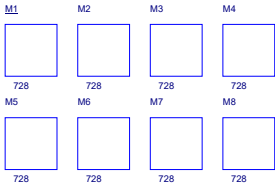
SCREWS



FIDUCIALS



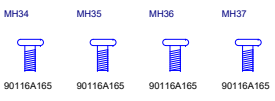
RUBBER FEET



BARE PCB



SCREW FOR FAN ASSEMBLY



LOGOs



LABELS

Board Serial No.



Assembly Revision.



EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J784S4XG01EVM
002:Soldered HS SoC	J784S4XH01EVM
003:Socketed SoC	J784S4XS01EVM

SOCKET



HEAT SINK



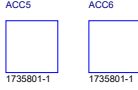
PROCESSOR



FAN



CRIMP PIN



CONN HOUSING



Project :
J7 EVM



Title HARDWARE SCHEMATICS	
Size PROC141 001 J784S4XG01EVM	Rev E3
Date Friday, August 19, 2022	Sheet 88 of 88