

J784S4X Evaluation Board

TABLE OF CONTENTS

REV	E2A
VER	3.4

PAGE	CONTENTS	PAGE	CONTENTS	PAGE	CONTENTS
01	TABLE OF CONTENTS	35	HYPERLINK & CSI CONNECTOR	69	ADC, RTC, I3C, APPLE AUTH
02	REVISION HISTORY #1	36	GESI CONNECTOR	70	x1LANE PCIe CONN
03	REVISION HISTORY #2	37	CSI EXPANSION CONNECTOR	71	x4LANE PCIe CONN
04	BLOCK DIAGRAM	38	ENET_EXPANSION_CONN	72	BOOT MODE BUFFER & SWITCHES
05	POWER FLOW DIAGRAM	39	SERDES CLOCK GENERATOR #1	73	TEST AUTOMATION HEADER
06	POWER SEQUENCE	40	SERDES CLOCK GENERATOR #2	74	OVER VOLTAGE PROTECTION CKT
07	PDN	41	PERIPHERAL CLOCK GENERATOR	75	POWER SUPPLY #1
08	I2C TREE	42	RESET BUTTONS	76	POWER SUPPLY #2
09	I2C Address table	43	RESET INPUTS	77	POWER SUPPLY #3
10	GPIO MAPPING TABLE	44	RESET OUTPUTS	78	POWER SUPPLY #4
11	SOC: CSI & DSI INTERFACES	45	GPIO EXPANDERS	79	PMIC SUPPORT CIRCUIT
12	SOC: SERDES0 INTERFACE	46	SPI NOR FLASH	80	EXTERNAL POWER MEASUREMENT
13	SOC: SERDES1,2 & 4 INTERFACE	47	MICRO SD CARD INTERFACE	81	SOC CURRENT SENSE
14	SOC: DDR0 - LPDDR4 INTERFACE	48	eMMC FLASH	82	PERIPHERAL CURRENT SENSE
15	SOC: DDR2 - LPDDR4 INTERFACE	49	UFS FLASH	83	CURRENT MONITORS #1
16	SOC: DDR1 - LPDDR4 INTERFACE	50	EEPROM	84	CURRENT MONITORS #2
17	SOC: DDR3 - LPDDR4 INTERFACE	51	DUAL PORT FTDI	85	CURRENT MONITORS#1 -INA231
18	SOC: MCU FLASH	52	QUAD PORT FTDI	86	CURRENT MONITORS#2 -INA231
19	OSPI & ONAND INTERFACE	53	XDS110 DEBUGGER	87	SI_SIMULATION_COUPON_BD
20	SOC: MCU & MAIN GENERAL IOS & CLKS	54	JTAG MIPI 60 CONN	88	HARDWARE SCHEMATICS
21	GENERAL	55	LIN TRANSCEIVER		
22	SOC: GENERAL & USB	56	CAN TRANSCEIVERS #1		
23	SOC: MCU RGMII, MMC & ADC	57	CAN TRANSCEIVERS #2		
24	SOC: JTAG & DEBUG	58	CAN TRANSCEIVERS #3		
25	SOC: USB	59	USB HUB		
26	SOC: ANALOG POWER 1	60	USB 2.0 TYPE-A CONN		
27	SOC: IO POWER 2	61	USB TYPE C 3.1		
28	SOC: DIGITAL POWER	62	MCU GB ETHERNET		
29	SOC: GROUND & KELVIN SENSING	63	RGMII1		
30	PMIC A	64	AUDIO I/F CODEC		
31	HCPS A	65	AUDIO I/F- STEREO MIC #1		
32	HCPS B	66	AUDIO I/F - LINE OUT		
33	SOC LDOS & LOAD SWITCHES	67	DSI TO eDP BRIDGE		
34	SVS MONITOR	68	DISPLAY PORT INTERFACE		

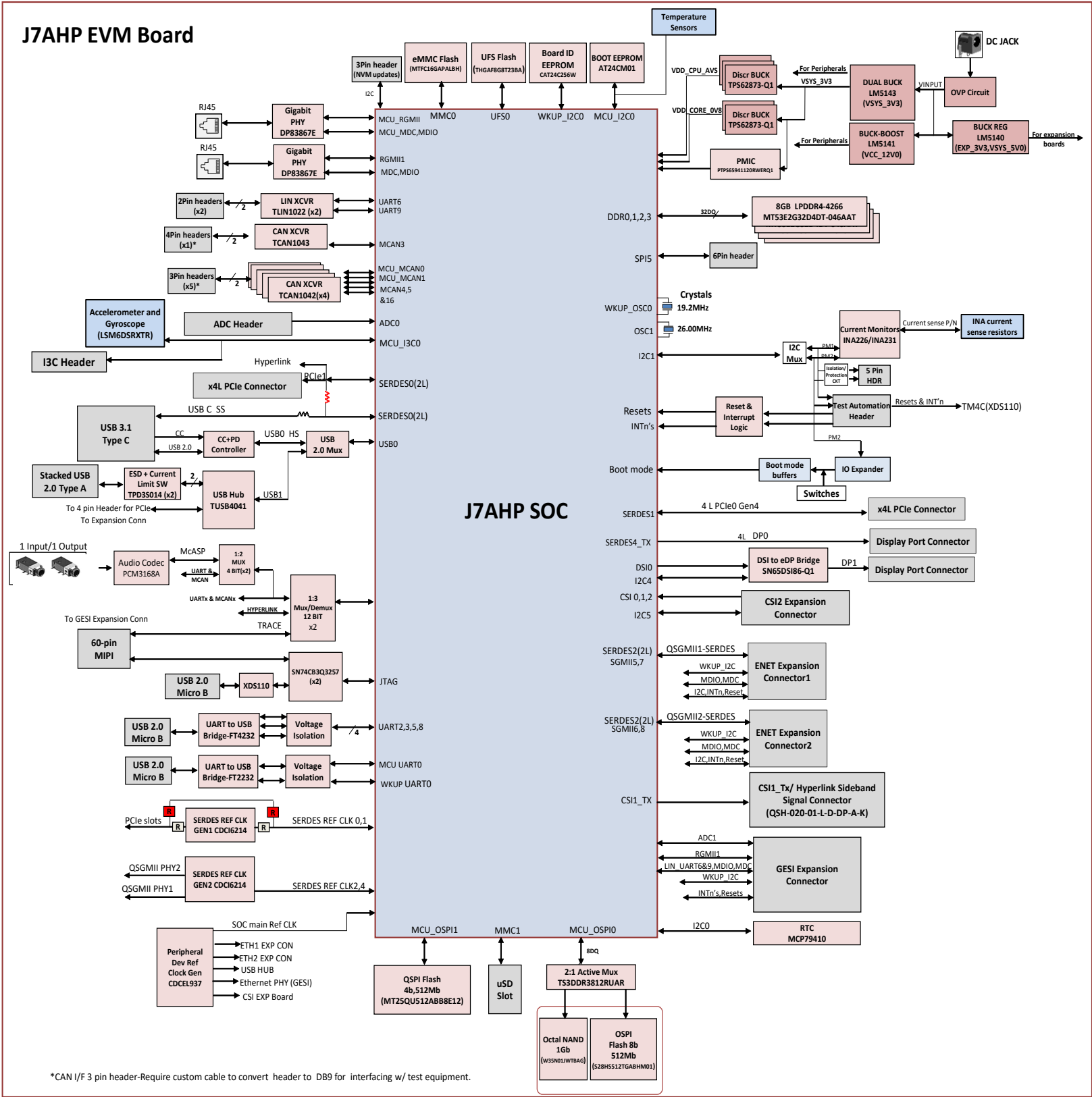
REVISION HISTORY #1

E1	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
	0.1	20 JAN 2022	Created	Mistral Design Team		
	0.2	31 JAN 2022	Updated variants	Mistral Design Team		
	0.3	04 FEB 2022	Updated for TI review comments Part -1	Mistral Design Team		
	0.4	09 FEB 2022	Changed LM5175 to LM5141 regulator for VCC_12V generation	Mistral Design Team		
	0.5	10 FEB 2022	Updated for TI review comments Part - 2	Mistral Design Team		
	0.6	14 FEB 2022	Updated for TI review comments Part - 3(partially)	Mistral Design Team		
	0.7	16 FEB 2022	Updated for TI review comments Part - 3(partially)	Mistral Design Team		
	0.8	18 FEB 2022	Imported breakout study schematics v35 Updated sense resistor section Updated SOC symbol to version v1.1	Mistral Design Team		
	0.9	21 FEB 2022	Updated resistor values for TPS3711 Updated resistor values for LM5141 feedback network	Mistral Design Team		
	1.0	22 FEB 2022	Updated Mosfet for enable of VDD_GPIORET_WK_0V8_REG supply (Changed mosfet used for VDD_MCU_0V85 supply)	Mistral Design Team		
	1.1	23 FEB 2022	Updated I2C0_IO_EXP_INT , VPP_EFUSE_EN connection and updated breakout study v36 schematics'	Mistral Design Team		
	1.2	24 FEB 2022	Updated for internal review Updated block diagrams Updated 50E resistor to 49.9E and 500E resistor to 499E	Mistral Design Team		
	1.3	28 FEB 2022	Updated for TI review comments Part - 4	Mistral Design Team		
	1.4	1 MAR 2022	BoM optimization	Mistral Design Team		
	1.5	3 MAR 2022	Removed 1.2V LDO for eDP bridge and combined the 1.2 supply for UFS and eDP Updated for TI review comments partially	Mistral Design Team		
	1.6	7 MAR 2022	Updated for TI review comments Updated for PDN v10 Added sesnse resistors for VDD_CORE_0V8, VDD_CPU_AVS, VDD_DDR_1V1 and current monitors for the same	Mistral Design Team		
	1.7	11 MAR 2022	Updated for TI review comments Added open drain buffer for DP_HPD signals	Mistral Design Team		
	1.8	15 MAR 2022	Updated for TI review comments	Mistral Design Team		
	1.9	16 MAR 2022	Updated for TI review comments Replace 4x 10uf, 3-T caps (U2088, U2089, U2091 & U2093) with 2x 100uf 2 -T caps C5816,C5817	Mistral Design Team		
	2.0	18 MAR 2022	Added 4x decaps for VMON inputs for SVS monitor. Added resistor option for feedback for VDD_CPU_AVS supply	Mistral Design Team		
	2.1	21 MAR 2022	Updated for internal review	Mistral Design Team		
	2.2	23 MAR 2022	Updated for internal review	Mistral Design Team		
	2.3	25 MAR 2022	Sense resistor for VDD_CORE, VDD_CPU_AVS and VDD_DDR_1V1 were removed.	Mistral Design Team		
	2.4	26 MAR 2022	Updated pull ups for I2C	Mistral Design Team		
	2.5	26 MAR 2022	Updated for TI review comments	Mistral Design Team	TI	
	2.6	05 APR 2022	Updated for TI review comments	Mistral Design Team		
E2	2.7	05 APR 2022	Updates shared by TI for REV E2 is done Fix for VSYS_IO_1V8 rail is updated	Mistral Design Team		
	2.8	20 APR 2022	Updated PDN SCH notes (purple font) on pgs: 26-28, 30-33, 79, 80 Updated SoC Analog SCH pg 26 filtering component values Updated PMIC SCH pg 30 format & power inductor values optmzcd for Fsw = 4.4MHz per IPM sim results	TI		
	2.9	21 APR 2022	Ref clock for PCIe x2L set to SOC clock by default	Mistral Design Team		

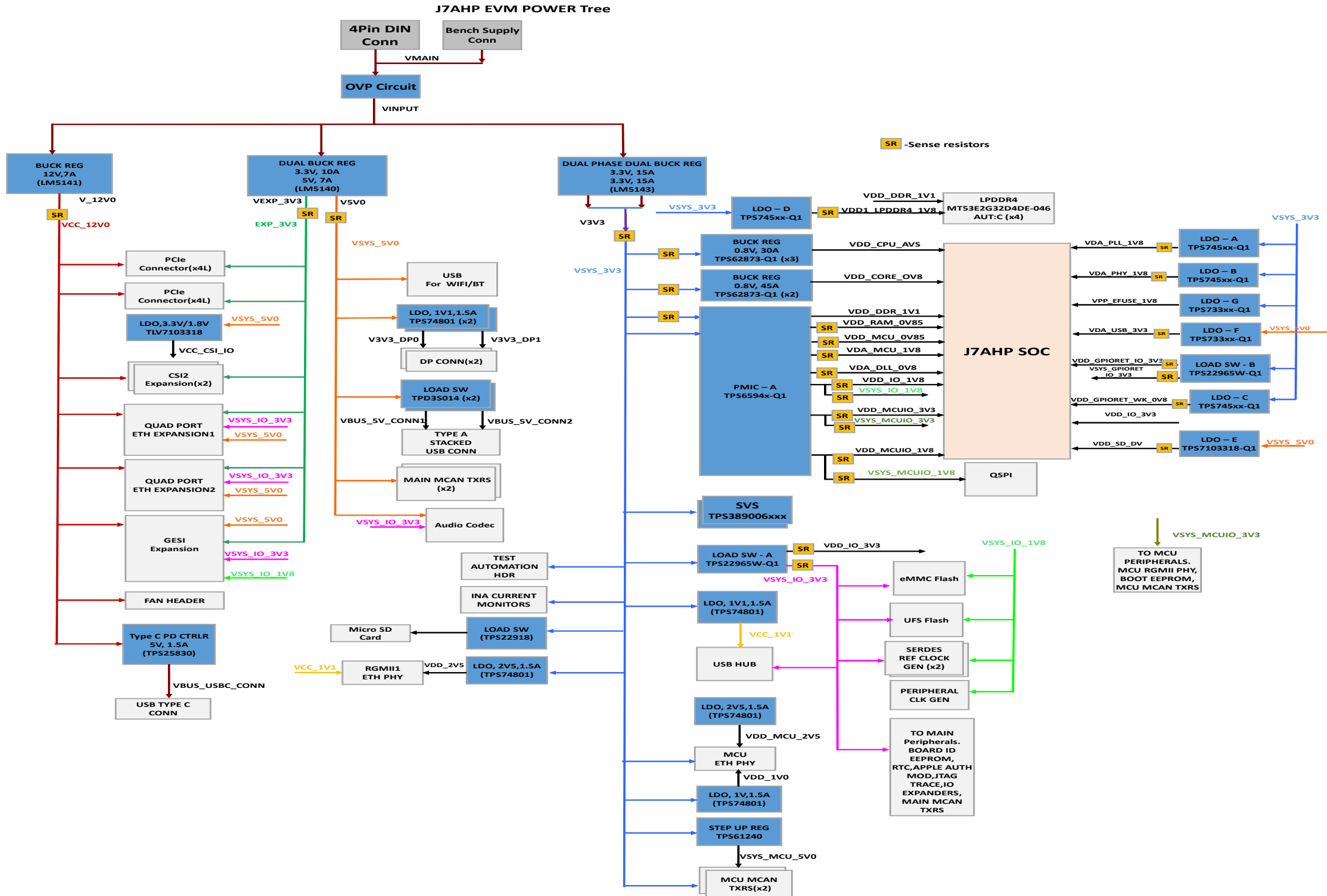
REVISION HISTORY #2

	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	3.0	26 APR 2022	Updated for PCIe ref clock connection DNI'd termination for QSGMII ref clock Minor PDN SCH pg updates	Mistral Design Team		
	3.1	27 APR 2022	Updated resistor R1292 and R1293	Mistral Design Team		
E2A	3.2	20 JUN 2022	Added note for updated VCC_12V0 Enable supply DNI'd U29 and U159 (I2C buffers connected to XDS) to avoid leakage on VCC3V3_XDS Updated "EVM Bd Setting & Leo NVM Default" Table	Mistral Design Team		
	3.3	30 JUN 2022	DNI'd resistors R659 and R1122 Added note for SW2 pin 8 pull up supply controlling the test automation signals from XDS110	Mistral Design Team		
	3.4	12 JUL 2022	R700 and R617 changed to 3K ohm resistor			

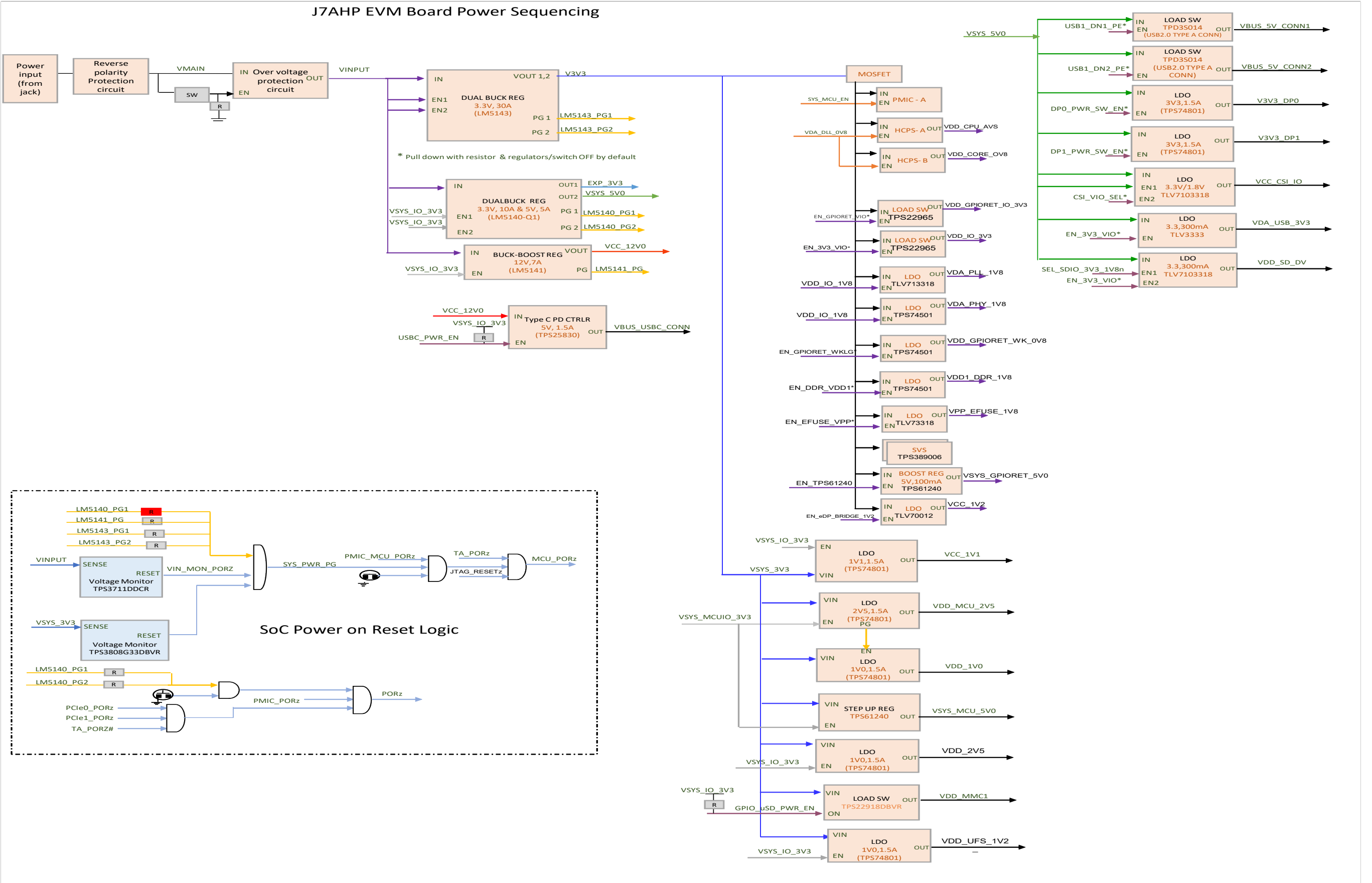
BLOCK DIAGRAM



POWER FLOW DIAGRAM



POWER SEQUENCE



PDN

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3A Details

(All SoC PN variants: TDA4AP/VP/AH/VH)
(Power Rail & GPIO Mapping Overview)

- 1/28/2022 Updated during 2nd NVM settings review
2/5/2022 Updated SVS connections following detailed reviews with VRS team
2/5/2022 Updated SVS ESEEP control signals as follows: Main SVS-A connect EN_V3S_VIO to nSLEEP input, MCU SVS-B connect VDD_MCUIO_V3S to nSLEEP.
3/9/2022 Removed R-Muxes showing alternative, EVN test mode only connecting MCU_GPIORET_0.BV & 3.3V supplies to Main domain supplies
3/9/2022 Created "Detailed EVM_PDN-3A" specific PDN diagram from v0.10 to show provisioned alternative connections for EVM optional testing & to meet EVN requirements
3/9/2022 1. Added 4x 8-Muxes to enable all GPIO_RET test modes: Standard (no GPIORET), MCU_GPIORET, MAIN_GPIORET & combined MCUMAIN_GPIORET
2. Updated net names to Q7 & Q8 from EN_GPIO_RET to revised name EN_GPIO_RET_V3S aligned to GPIO_V3S OD output with PU resistor to 3.3V supply
3. Replace inverter on MAIN_PWRGRP_INTN with tri-state Buffer & OE connected to H_MCU_PDR2 to "Time-Mux" vs "Wire-Mux" w/ b/w WDOG_DISABLE
4. Updated "NOTES" & added "SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features" table
3/17/2022 1. Changed Tulp Back Vio supply from VCCA_V3S to V3S_V3S per worst case analysis (see new Note #10) to reduce PMIC Safety FET voltage drop
3/31/22 2. Improve margins on all 3.3V power rails supplied by VCCA_V3S (i.e. Load Switches supplying SoC's VDD_IO_V3S & VDD_MCUIO_V3S)
4/4/2022 1. Added voltage translation to MCU_PDR2_V3S for DIR control of Tri-State Buffer creating MAIN_PWRGRP_IRQn_BUF signal on PMIC GPIO_8.
2. Updated Note 9 to show 2x options for single bit, low voltage translation components.

Legend:

- Power Rails
PDN base
MCU Only/Island
MCU Retention
DDR Retention (aka S2R)
End Product option
Peripheral loads (SW config'd after boot)
DDR Retention (aka S2R)
End Product option
Peripheral comps
Debug/Development option
- Control Signals:
General ctrl & logic
(italic = SW config'd after boot)
PDN base ctrl
Func Safety
MCU Only/Island
GPIO Retention
DDR Retention (aka S2R)
End Product option
Peripheral comps
Debug/Development option
- Note items
On-Chip "Pwr OK" Monitors (UV & VU)
On-Chip "Pwr OK" Monitors (UV only)
Provisioned In-Line Supply Filter
High-lighted diagram changes

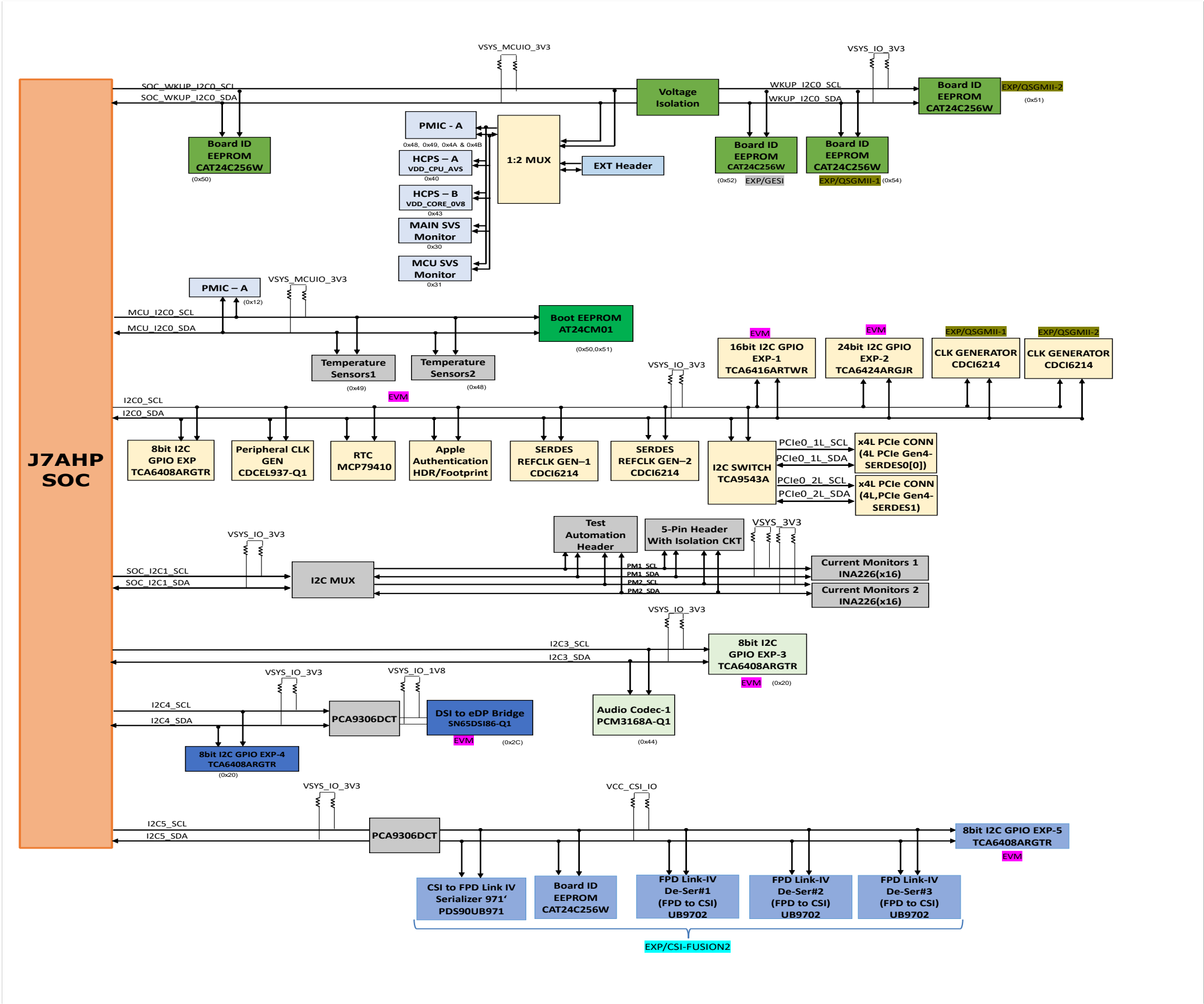
- Notes:
- 1) Functional Safety requires monitoring all "safety critical" power rails (i.e. V3S_V3S input, key SoC supplies) that could cause severe system failures. This classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (PWR_OK) status bits. Optional SoC voltage monitoring inputs (i.e. VMON_IR_VDETn) can be used to extend SoC's OV/UV monitoring to a few board level power rails if desired (i.e. load switch Vo = VDD_IO_V3S). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPD004_1V8.
- 2) Load Switches (LSWs) have been used to create VDD_MCUIO_V3S, VDD_GPIORET_V3S & VDD_IO_V3S power rails from VCCA_V3S to provide the following benefits:
A) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resource outputs) with desired start-up & shut-down timing delays per NVM settings.
B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC to disconnect 3.3V power rails from SoC if OV condition is detected.
C) Enables low power modes (MCU Only, GPIO_RET & DDR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
D) Connecting VCCA_V3S directly to SoC 3.3V supplies is not recommended since this will leave SoC partially energized for extended periods of time that can negatively impact PWR reliability.
- 3) PMIC's GPIO_8 has been provisioned to support multiple interface signals. The PMIC PN default function sets GPIO_8 = DISABLE_WDOG function following NVM initialization. This GPIO's default function can be reassigned by system SW following SoC boot if another interface signal is needed that is not required for SoC power sequencing.
1. Default: GPIO_8 = DISABLE_WDOG function operates with PMIC's DISABLE_WDOG signal that is latched on rising edge of PMIC's nSLEEP_H_MCU_PDR2_V3S at end of power-up seq. A logic low enables normal watchdog timer operation while a logic high disables watchdog timer following a power up seq.
2. Option1: After system SW boots, SW can reassign GPIO_8 = GPI function to operate with PMIC's MAIN_PWRGRP_IRQn (asserted high or low) signal. System SW must mask GPIOS before changing GPIORET assigned function. After selecting GPI function, SW must unmask GPI input and select whether the GPI will be either rising or falling edge sensitive. If any Main domain processing supply rail has a fault, the changing logic level on GPIORET will set internal register bit that is monitored by PMIC's power state machine and cause a transition from Full Active state to MCU Safe state. At the board level, the WDOG_DISABLE & MAIN_PWRGRP_IRQn signals are "time mux" onto GPIORET's input pin by using a tri-state buffer with OE control connected to H_MCU_PDR2_V3S. This enables WDOG_DISABLE net to set GPIORET's logic level during power up seq when H_MCU_PDR2_V3S is low since buffer is tri-stated. After power up seq, H_MCU_PDR2_V3S = high enabling buffer to drive MAIN_PWRGRP_IRQn logic level into GPIORET input.
3. Option2: GPIO_8 = WKUP1 function can be selected by SW to operate with SoC's PMIC_PWR_EN1 signal for emulator debug control of PMIC power resources (i.e. enabling VDD_CORE to activate core logic required to support ITAG signaling across the device). Combining board level WDOG_DISABLE & PMIC_PWR_EN1 signals using a resistor network is possible since WDOG_DISABLE pulls logic level high when switch is closed. Afterwards, switch can be opened and PMIC_PWR_EN1 signal will drive GPIO_8.
- 4) GPIO Retention (aka DOR_RET, IO_RET, IO Wake) low power mode requires:
A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
1. VDD_GPIORET_V3S supplying MCU's VDD_MCU_WAKE1 for MCU's 0.8V wake-up logic
2. VDD_GPIORET_V3S supplying PMIC's WDOGnVIO for MCU's 3.3V I/O toggle activity
C) PDN system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored I/O signals or to VDDSHV5_MCU supply. Then H_MCU_WAKE1n in SoC's Open-Drain PMIC_WAKEn1 active low signal connected to PMIC GPIO_4 = WKUP1 default function for Full Active or WKUP2 for MCU Only destination state is asserted and PMIC state machine transitions PDN system to desired targeted wake-up state.
D) The Open-Drain Buffer nTALVCIGDTRn1 (tri-states IO when power is off) connects PMIC_WAKEn1 to SoC_PWR_Wktn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from always-on VCCA_V3S used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DOR_RET) when VDD_GPIORET_V3S is typically disabled.
- 5) DDR Retention (aka DOR_RET, Suspend-to-RAM, S2R) low power mode requires:
A) PMIC PN to assign GPIO_8 = Regulator Enable (REGEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DOR_RET_V3S is pulled up to VDD_DOR_V3S & connected to SoC's DOR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DOR_RET mode.
B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DOR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
C) After entering DOR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
1. VDD_DOR_V3S supplying both SoC EMIF & SDRAM I/O voltages
2. VDD1_DOR_V3S supplying SDRAM only
D) PDN system exits DOR_RET upon detecting a CAN_WAKE signal edge toggle on PMIC's GPIO_4 = UP_WKUP1 function per NVM settings that initiates exiting DOR_RET mode & restores Full Active processor operations.
- 6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-field updates, then on-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vo will need a high impedance output. Recommended PNs: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EM_EFUSE_VPP control signal must be sourced from an SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control EFUSE VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC EFuses (see SoC DM for details).
- 7) PDN shows SoC's VDDA_3P3_USB domain supplied from a low noise LDO with a V3S_V3S input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 (F is not used or is only needed for development tasks, then the digital VDD_IO_V3S rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_V3S rail to support USB 2.0 (F removes a discrete LDO & V3S_V3S input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.
- 8) PDN shows SoC's Main domain's VDDSHV5 supply being sourced from a dual voltage LDO with a V3S_V3S input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_V3S rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_V3S rail to support SD Card operation requires dual voltage, discrete LDO & V3S_V3S input but will restrict data rates to standard 12Mb/s with VIO = 3.3V.
- 9) A discrete FET or voltage translation IC with low VGS or VIH is needed to ensure a logic high level output will result with an input min 0.75V (5% supply toll). Examples shown below:
- 10) Worst case analysis for very high thermal use cases could result in VCCA_V3S load current in 15-18A range. This large load current range could lead to a 60 - 70mV voltage drop across Safety FET (RDS(on) = 4mOhm). The TPS22965-Q1 load switches have max RDS(on) = 27mOhm with 4A max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 155mV. Total RDS(on) drops across Safety FET & Load Switcher range from 168 - 180mV which exceed SoC's min voltage limit. For this reason, the Tulp back input voltage will be moved from VCCA_V3S to V3S_V3S since VDD_CPU_AVS & VDD_CORE_V3S rails account for more than 70% of VCCA_V3S worst case load currents.

Work-In-Progress

SoC Input Supply to Power Rail Groupings vs PDN Low Power Mode Features

PDN Features	Isolated MCU & Main PDN Power Rails							
	VDD_MCU_0V8S	VDD_CORE_0V8	VDD_MCUIO_3V3	VDD_IO_1V8	VDD_IO_3V3	VDD1_DDR_1V8	VDD_GPIORET_0v8	VDD_GPIORET_3V3
Standard Operation & MCU Only	vdd_mcu							
	vddar_mcu	vdd_core	vddshv0_mcu	vdds_mmc0	vddshv0			
DDR Retention	vdd_mcu							
	vddar_mcu	vdd_wake0	vddshv2_mcu	vddshv2_mcu	vddshv2	DDR: vdd1		
GPIO Retention-MCU & Main	vdd_mcu							
	vddar_mcu	vdd_core	vddshv2_mcu	vdds_mmc0	vddshv0		vdd_mcu_wake1	vddshv0_mcu
GPIO Retention-MCU	vdd_mcu							
	vddar_mcu	vdd_wake0	vddshv2_mcu	DDR: vdd1	vddshv2		vdd_mcu_wake1	vddshv0_mcu
GPIO Retention-Main	vdd_mcu							
	vddar_mcu	vdd_core	vddshv0_mcu	vdds_mmc0	vddshv0		vdd_wake0	vddshv2
Notes:								
	1) Power rail names shown in "ALL CAPITAL LETTERS"							
	2) SoC input supplies shown in "all lower case letters"							

I2C TREE



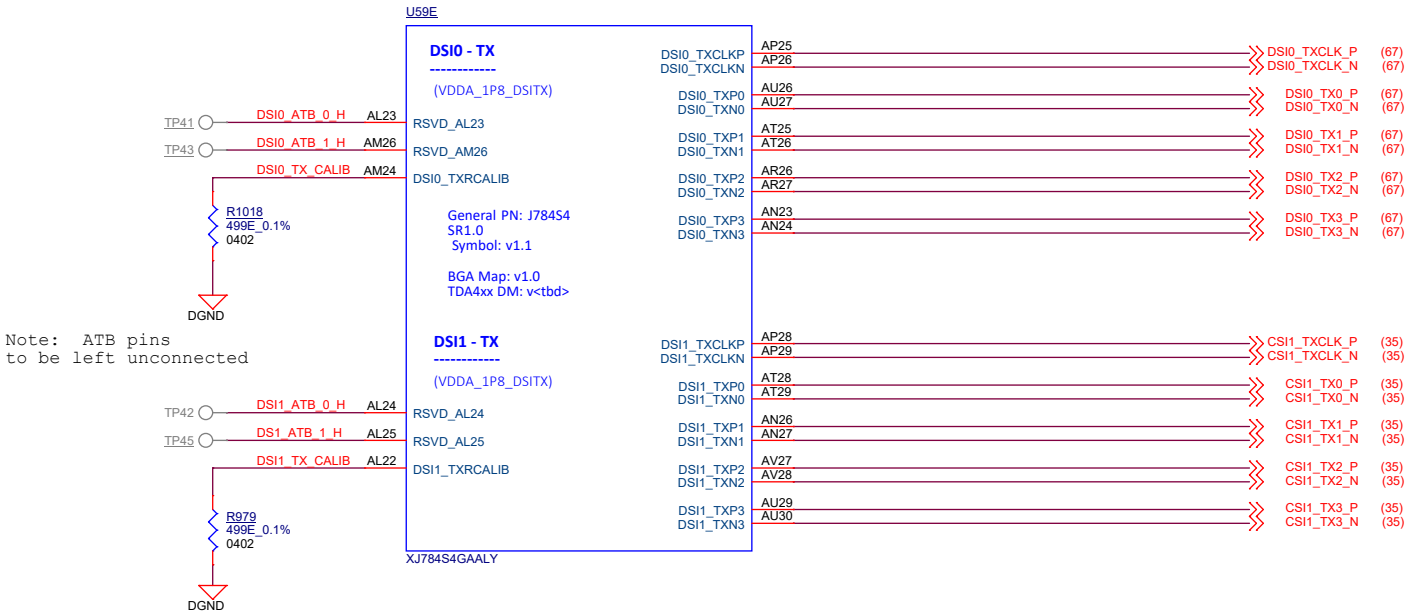
I2C TABLE

Board	Interface name	Part#	Address	J7AHP Port mapping
EVM	Board ID EEPROM	CAV24C256WE-GT3	0x50	WKUP_I2C0
EXP/QSGMII -1	Board ID EEPROM	CAT24C256WI-GT3	0x54	
EXP/QSGMII -2	Board ID EEPROM	CAT24C256WI-GT3	0x51	
EXP/GESI	Board ID EEPROM	CAT24C256W	0x52	
EVM	PMICs	PMIC A: TPS659413	PMIC A: 0x48, 0x49, 0x4A & 0x4B	
EVM	Tulip - VDD_CPU_AVS Regulator	TPS62873	0x40	
EVM	Tulip - VDD_CORE_OV8 Regulator	TPS62873	0X43	
EVM	MAIN SVS Monitor	PPS38900603NRTERQ1	0X30	
EVM	MCU SVS Monitor	PPS38900603NRTERQ1	0X31	
EVM	Temperature Sensors	TMP100NA/3K	0x48, 0x49	MCU_I2C0
EVM	Boot EEPROM	AT24CM01	0x50, 0x51	
EVM	I2C Switch for PCIe	TCA9543APWR	0x70	Main I2C0
EVM	RTC Clock	MCP79410-I/SN	0x57,0x6F	
EVM	SerDes Clock gen #1 Optional	CDCI6214	Optional	
EVM	SerDes Clock gen #2	CDCI6214	0x77,0x76	
EVM	Pheriphal Clock Gen	CDCEL937-Q1	0x6D	
EVM	16bit I2C GPIO EXPANDER1	TCA6424ARGJR	0x20	
EVM	24bit I2C GPIO EXPANDER2	TCA6424ARGJR	0x22	
EVM	8 bit I2C GPIO Expander4	TCA6408ARGTR	0x20	Main I2C4
EVM	DSI TO eDP BRIDGE	SN65DSI86IPAPQ1	0x2C	
EVM	DSI FPC Connector	<connector interface>		
EVM	I2C Switch for Automation header		0x22	Main I2C1
EVM	Current Monitors and Header		0x40 to 0x4F	
EVM	8bit GPIO Expander3	TCA6408ARGTR	0x20	Main I2C3
EVM	AUDIO IF Codec	PCM3168A-Q1	0x44	
EXP	8bit GPIO Expander5	TCA6408ARGTR	0x20	Main I2C5
EXP/CSI-FUSION2	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	0x3D	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x30	
EXP/CSI-FUSION2	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	0x32	
EXP/CSI-FUSION2	CSI to FPD Link IV Serializer 971	UB971	0x18	

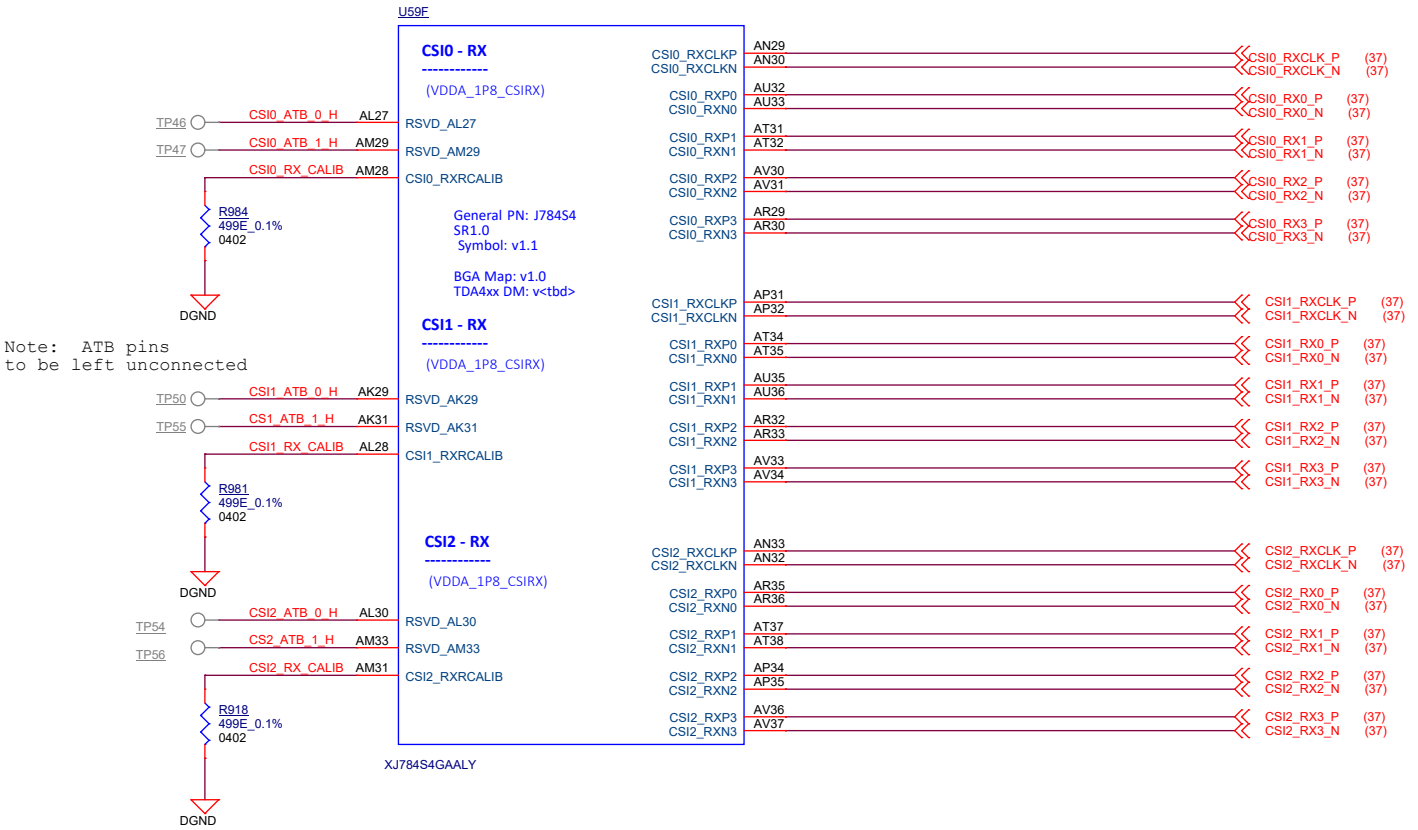
GPIO EXPANDER MAP/TABLE

J7AHP EVM - GPIO Mapping Table						
WKUP Domain						
Net name	Package Signal Name	GPIO Number	Input/Output	Default	State	Remarks
EN_EFUSE_VPP	WKUP_GPIO0_54	WKUP_GPIO0_54	Output	BOOTMODE	Active High	VPP_EFUSE LDO enable
BOOT_EEPROM_WP	WKUP_GPIO0_1	WKUP_GPIO0_1	Output	BOOTMODE	Active High	Boot EEPROM Write protect
MCU_CAN1_STB	WKUP_GPIO0_2	WKUP_GPIO0_2	Output	BOOTMODE	Active High	MCU_CAN1 Standby
GPIO_MCU_RGMII1_RST#	WKUP_GPIO0_56	WKUP_GPIO0_56	Output	BOOTMODE	Active low	MCU_RGMII1_Reset
SYS_IRQz	WKUP_GPIO0_7	WKUP_GPIO0_7	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0>1' - interrupt pending, '1' - normal operation)
OSPI/HYPER_MUX_SEL	WKUP_GPIO0_6	WKUP_GPIO0_6	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - OCTAL NAND)
PMIC_MCU_INT# / H_MCU_INT#	MCU_OSPi1_CSN1	WKUP_GPIO0_39	Input	PU	Active low	Interrupt from PMIC
MCU_RGMII1_INT#	WKUP_GPIO0_3	WKUP_GPIO0_3	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
SYS_MCU_PWRDN	MCU_SPI0_D0	WKUP_GPIO0_55	Output	BOOTMODE	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_CAN0_STBz	MCU_SPI0_D1	WKUP_GPIO0_69	Output	BOOTMODE	Active low	MCU_CAN0 Standby
LSM6DSOX_INT/LSM6DSRX_INT	WKUP_GPIO0_57	WKUP_GPIO0_57	Input	BOOTMODE	NA	Interupt from I3C Gyroscope sensor(*LSM6DSRX)
PM_I2C_SEL	WKUP_GPIO0_66	WKUP_GPIO0_66	Output	BOOTMODE	Active High	PM_I2C Mux selection. ('0' - SOC_I2C2_SCL/SDA -> PM1_SCL/SDA, '1' - SOC_I2C2_SCL/SDA -> PM2_SCL/SDA)
USBC_DIR_SOC	MCU_OSPi0_CSN1	WKUP_GPIO0_28	Input	PU	Active High	USB C direction pin
ENET1_EXP_INTB	MCU_ADC1_AIN5	WKUP_GPIO0_84	Output	PU	Active low	ENET expansion 1 Interrupt signal
ENET2_EXP_INTB	MCU_ADC1_AIN6	WKUP_GPIO0_85	Output	PU	Active Low	ENET expansion 2 Interrupt signal
I2C0_IOEXP_INT#	MCU_ADC1_AIN7	WKUP_GPIO0_86	Output	PU	Active Low	I2C0 IO expander interrupt signal
CANIO_RET_WAKE	MCU_SPI0_CS0	WKUP_GPIO0_70	Input	PU	NA	Push-button wake signal
Main Domain						
MAIN_RET_WAKE	GPIO0_11	GPIO0_11	Input	PU	NA	Push-button wake signal
HYP1_RXFLCLK_MUX	MCASP0_AXR2	GPIO0_13	Input	PU	Active Low	I2C5 IO expander interrupt. Muxed with trace and Hyperlink signals
SEL_SDIO_3V3_1V8n	MCAN15_RX	GPIO0_8	Output	NA	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
CSI2_EXP_A_GPIO2(MCASP4_AXR1/T_RC_DATA16_MUX)	MCAN0_RX	GPIO0_26	I/O	NA	NA	CSI2 Expansion Board Specific. Muxed with trace and Hyperlink signals
CSI2_EXP_A_GPIO4(MCASP4_AXR3/T_RC_DATA5_MUX)	MCAN1_RX	GPIO0_28	I/O	NA	NA	CSI2 Expansion Board Specific. Muxed with trace and Hyperlink signals
TRC_DATA0_MUX	MCAN13_TX	GPIO0_3	Input	PU	NA	Interrupt signal from DSI to eDP bridge
SOC_GPIO0_21_MUX	MCASP2_ACLKX	GPIO0_21	Input	PU	Active Low	RGMII1 INT signal
GPIO Expander - 1 Part# TCA6424ARGJR						
I2C0/0x20	P00	PCie1_2L_MODE_SEL	Input	DIP_SEL	NA	PCie1 4-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P01	PCie1_4L_PERSTz	Input	PD	Active low	PCie1 4-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P02	PCie1_2L_RC_RSTz	Output	PD	Active low	PCie1 4-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P03	PCie1_2L_EP_RST_EN	Output	PD	Active low	PCie1 4-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P04	PCie0_4L_MODE_SEL	Input	DIP_SEL	NA	PCie0 2-Lane Mode Select ('0' - Root Complex, '1' - End Point)
	P05	PCie0_4L_PERSTz	Input	PD	Active low	PCie0 2-Lane Bus Reset ('0' - device reset, '1' - normal operation)
	P06	PCie0_4L_RC_RSTz	Output	PD	Active low	PCie0 2-Lane RC Reset Control ('0' - device reset, '1' - normal operation)
	P07	PCie0_4L_EP_RST_EN	Output	PD	Active low	PCie0 2-Lane EP Reset Enable ('0' - PERSTz isolated from PORz, '1' PERSTz connected to PORz)
	P10	PCie1_4L_PRSTn#	Input	PU	Active High	PCie1 4-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P11	PCie0_4L_PRSTn#	Input	PU	Active High	PCie0 2-Lane Hot Plug/Card Detect ('0' - PCIe Card Detected, '1' - no card detected)
	P12	CDCI1_OE1/OE4	Output	PU	Active High	PCIE 2L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P13	CDCI1_OE2/OE3	Output	PU	Active High	PCIE 1L Reference Clock Enable ('0 - clock disabled, '1' - clock enabled)
	P14	AUDIO_MUX_SEL	Output	PU	Active High	Mux select for McASP and trace signals
	P15	EXP_MUX2	Output	NA	NA	Expansion Board Mux control1 GESI - MDIO_MDC_SEL0
	P16	EXP_MUX3	Output	NA	NA	Expansion Board Mux control1 GESI - MDIO_MDC_SEL1
	P17	GESI_EXP_PHY_RSTz	Output	PU	Active High	EXP_RSTz - Terminated with Test point
GPIO Expander - 2 Part# TCA6424ARGJR						
I2C0/0x22	P00	R_GPIO_RGMII1_RST	Output	PU	Active low	Routed to INFO/GESI expansion connector. GESI - Used for GPIO_PRG0_RGMII1_RST; INFO - Not used
	P01	ENET2_I2CMUX_SEL	Output	PD	NA	Signal Mux Control ('0' - No Connect , '1' - I2C0)
	P02	GPIO_USD_PWR_EN	Output	PU	Active High	MicroSD Card Power Enable ('0' - power off, '1' - power on)
	P03	USBC_PWR_EN	Output	PU	Active High	USB-TypeC VBUS Controller Power Enable ('0' - power off, '1' - power on)
	P04	USBC_MODE_SEL1	Output	DIP_SEL	NA	USB-Type C Mode Select
	P05	USBC_MODE_SEL0	Output	DIP_SEL	NA	USBC_MODE_SEL[1:0]: '00' = DFP, '01' = DRP, '1x' = UFP
	P06	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
	P07	R_CAN_STB	Output	PU	Active High	Standby signals for On BOARD and GESI CAN Transceiver
	P10	CTRL_PM_I2C_OE#	Output	PD	Active High	Gate drive for enable signal of PM I2C mux select
	P11	ENET2_EXP_PWRDN	Output	PU	Active low	Ethernet Expansion2 PHY Powerdown ('0' - normal operation, '1' - device power down)
	P12	ENET2_EXP_SPARE2	Input	NA	NA	Ethernet Expansion2 Spare2 ('0' - not defined, '1' - not defined)
	P13	CDCI2_RSTZ	Output	PU	Active low	Peripheral Clock Generator ('0' - device reset, '1' - normal operation)
	P14	USB2.0_MUX_SEL	Output	PD	Active High	Signal Mux Control ('0' - USBC, '1' - USB Hub)
	P15	CANUART_MUX_SEL0	Output	PD	Active High	Select line forboth the CANUART_MUX
	P16	CANUART_MUX2_SEL1	Output	PU	Active High	Select line for CANUART_MUX2
	P17	CANUART_MUX1_SEL1	Output	PU	Active High	Select line for CANUART_MUX1
	P20	ENET1_EXP_PWRDN	Output	PU	Active High	Ethernet Expansion1 PHY Powerdown ('0' - normal operation, '1' - device power down)
	P21	ENET1_EXP_RESETz	Output	PD	Active low	Ethernet Expansion1 Reset ('0' - device reset, '1' - normal operation)
	P22	ENET1_I2CMUX_SEL	Input	PD	NA	Signal Mux Control ('0' - No Connect , '1' - I2C0)
	P23	ENET1_EXP_SPARE2	Input	NA	NA	Ethernet Expansion1 Spare2 ('0' - not defined, '1' - not defined)
	P24	ENET2_EXP_RESETz	Output	PD	Active low	Ethernet Expansion2 Reset ('0' - device reset, '1' - normal operation)
	P25	USER_INPUT1	Input	DIP_SEL	NA	User Dip Switch Input1 ('0' - User Define, '1' - User Define)
	P26	USER_LED1	Output	PD	Active High	User LED1 Enable ('1' - LED Off, '0' - LED On)
	P27	USER_LED2	Output	PD	Active High	User LED2 Enable ('1' - LED Off, '0' - LED On)
GPIO Expander - 3 Part# TCA6408ARGTR						
I2C3/0x20	P0	CODEC_RSTZ	Output	PD	Active low	Audio Codec Reset ('0' - device reset, '1' - normal operation)
	P1	CODEC_SPARE1	NA	UNUSED	NA	Not used (test point)
GPIO Expander - 4 Part# TCA6408ARGTR						
I2C40x20	P0	DP0_PWR_SW_EN	Output	PD	Active High	DisplayPort0 Power Enable ('0' - power off, '1' - power on)
	P1	DP1_PWR_SW_EN	Output	PD	Active High	DisplayPort1 Power Enable ('0' - power off, '1' - power on)
	P2	GPIO_eDP_ENABLE	Output		Active High	DSI to eDP bridge enable
GPIO Expander - 5 Part# TCA6408ARGTR						
I2C5/0x20	P0	CSI2_EXP_RSTZ	Output	PD	Active low	CSI2 Expansion Interface Reset ('0' - device reset, '1' - normal operation)
	P1	CSI2_EXP_A_GPIO0	IO	NA	NA	CSI2 Expansion Board Specific.
	P2	CSI2_EXP_A_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific.
	P3	CSI2_EXP_A_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific.
	P4	CSI2_EXP_B_GPIO1	IO	NA	NA	CSI2 Expansion Board Specific.
	P5	CSI2_EXP_B_GPIO2	IO	NA	NA	CSI2 Expansion Board Specific.
	P6	CSI2_EXP_B_GPIO3	IO	NA	NA	CSI2 Expansion Board Specific.
	P7	CSI2_EXP_B_GPIO4	IO	NA	NA	CSI2 Expansion Board Specific.

DSI



CSI

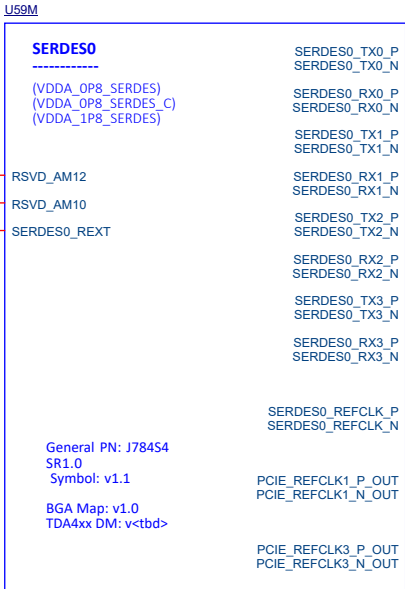
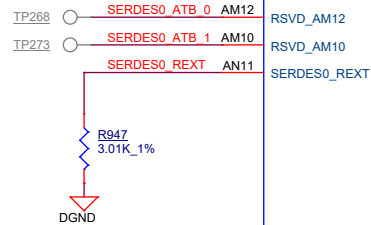


SERDES0

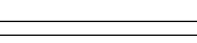
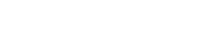
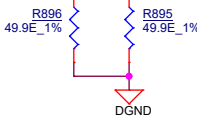
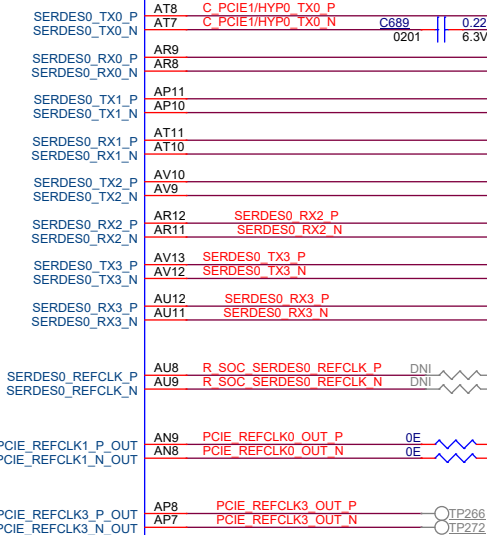
Note: Place DC blocking caps near PCIe Connector

Dedicated 2L to PCIe4L connector, x2L will be resistor muxed with USBC
Default connected to USBC

Note: ATB pins to be left unconnected

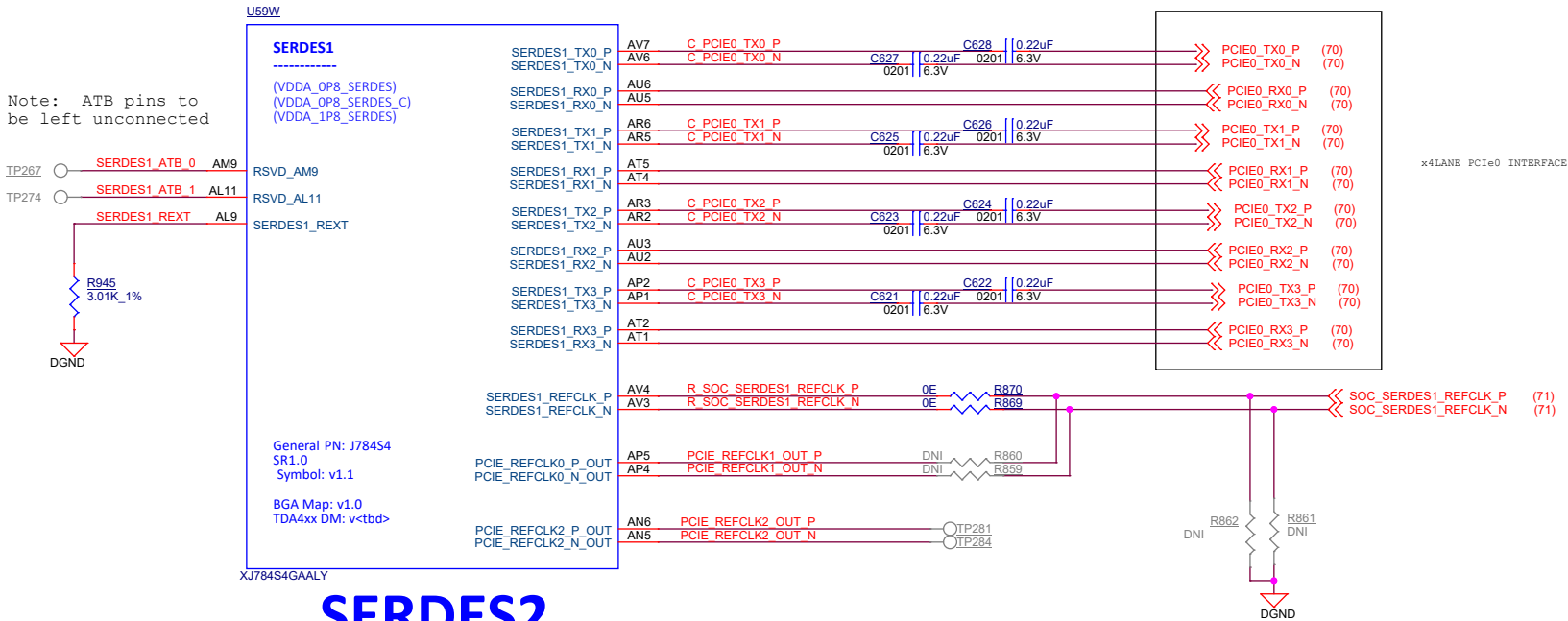


XJ784S4GAALY



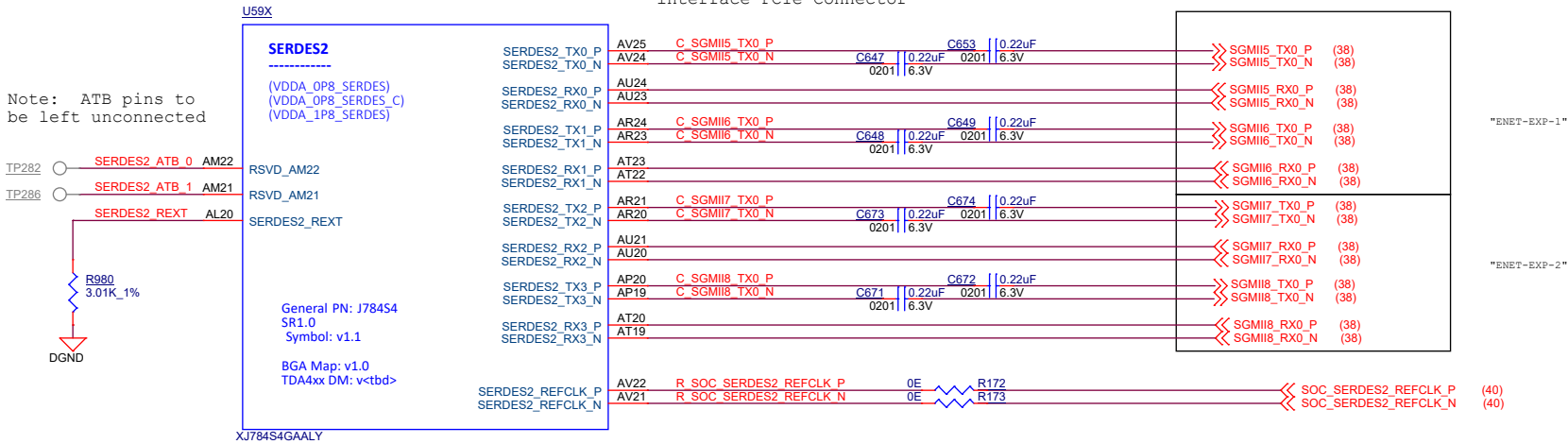
SERDES1

Note: Place DC blocking caps near interface PCIe Connector



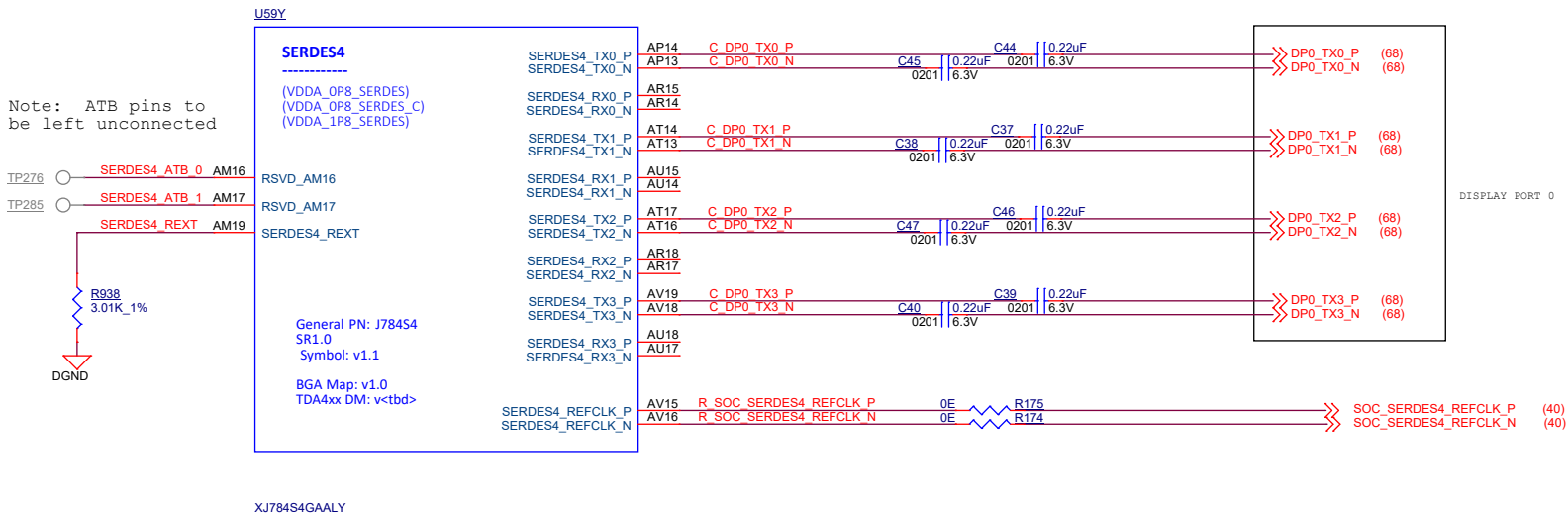
SERDES2

Note: Place DC blocking caps near interface PCIe Connector

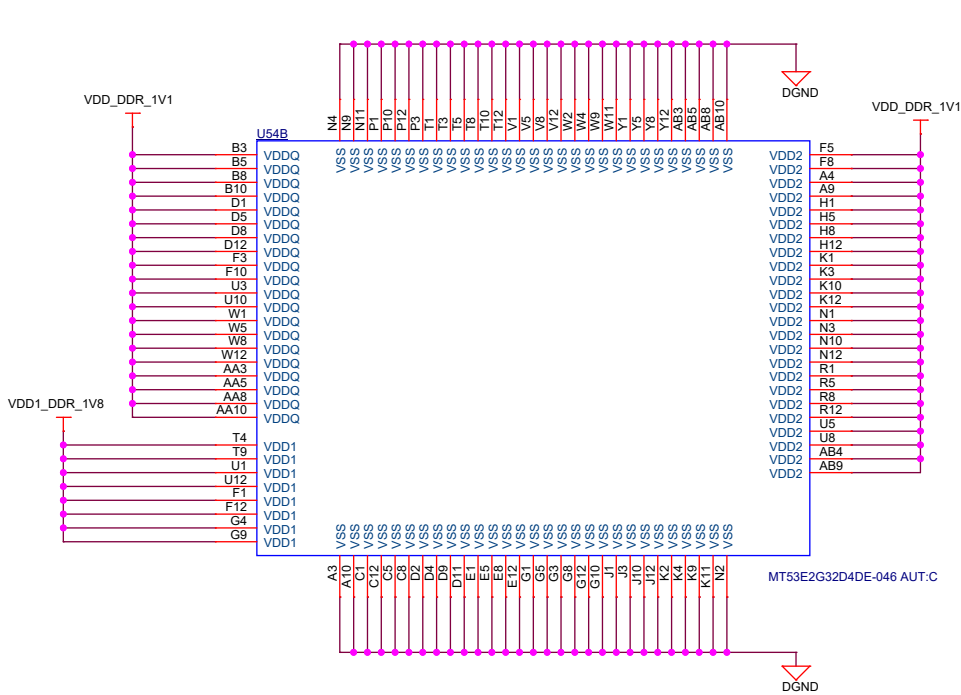
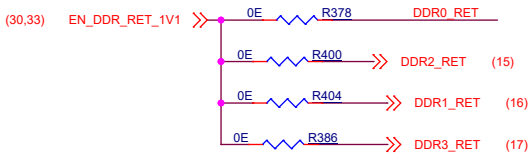
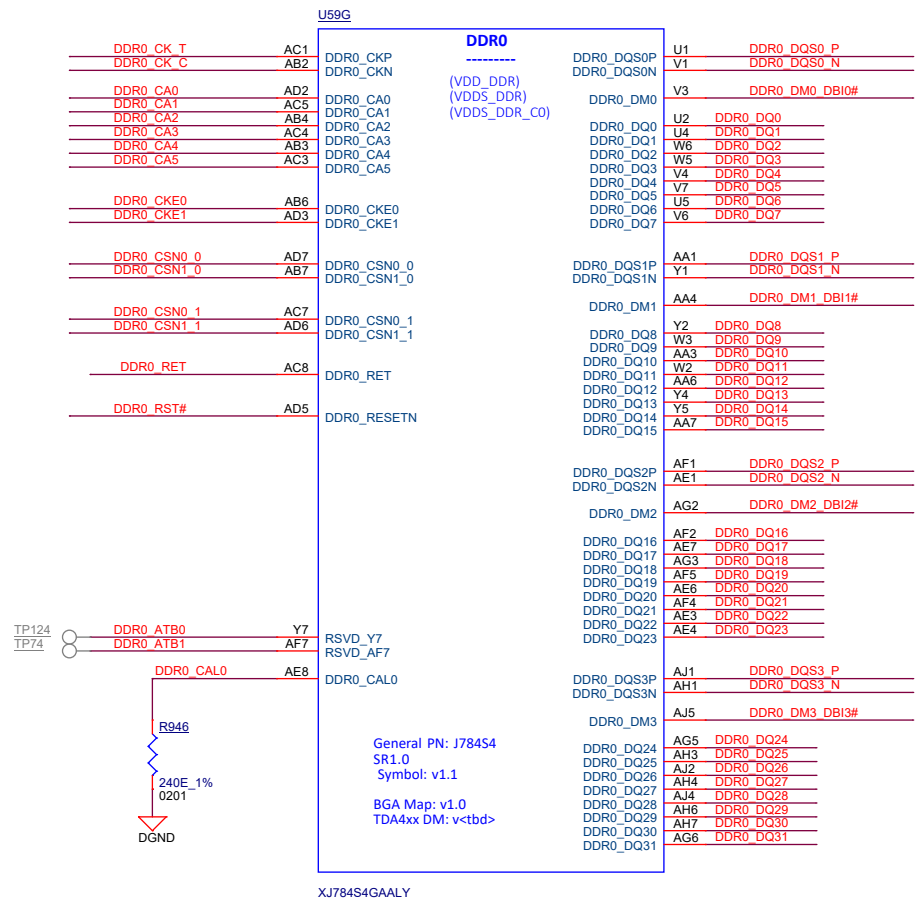
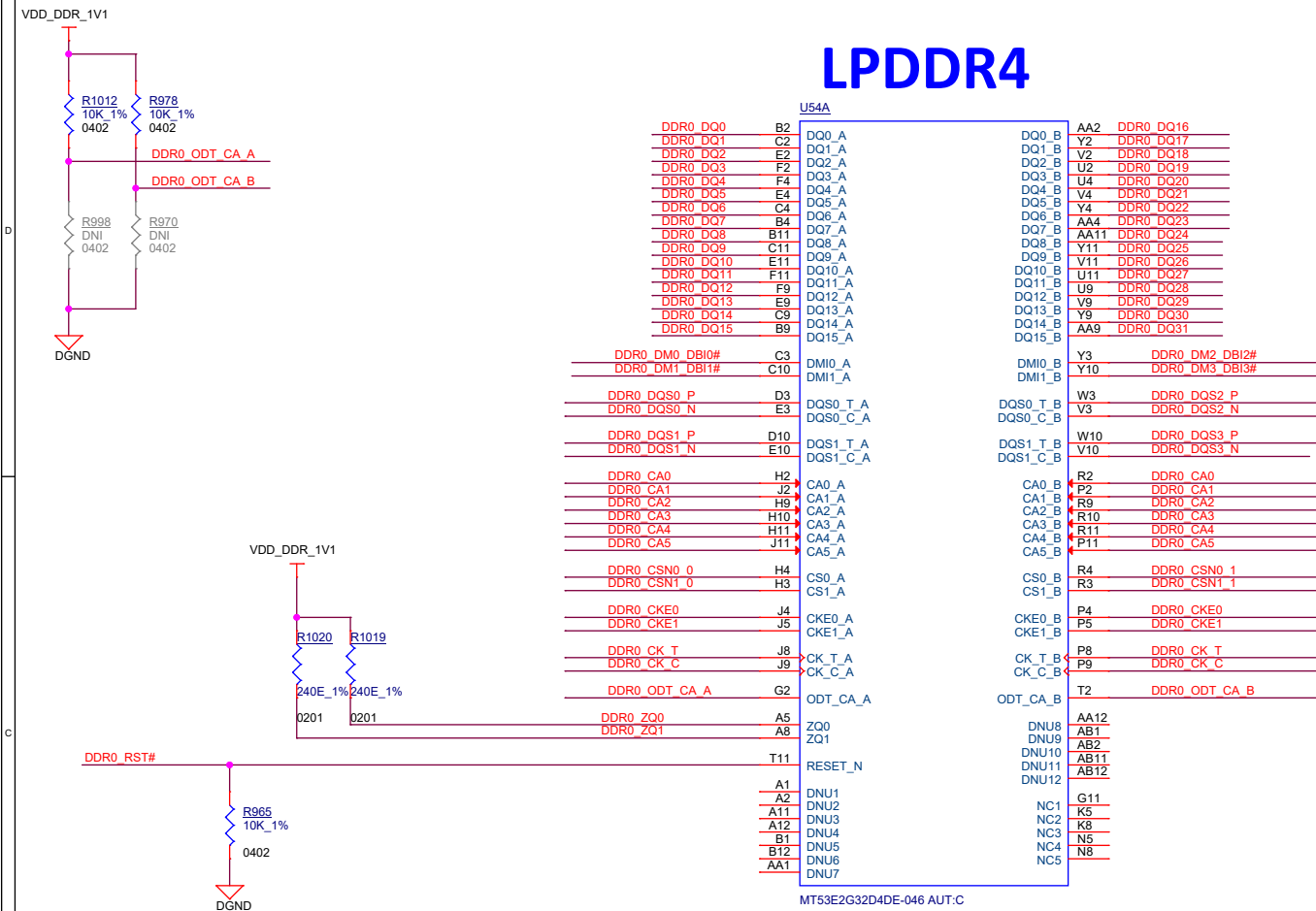


SERDES4

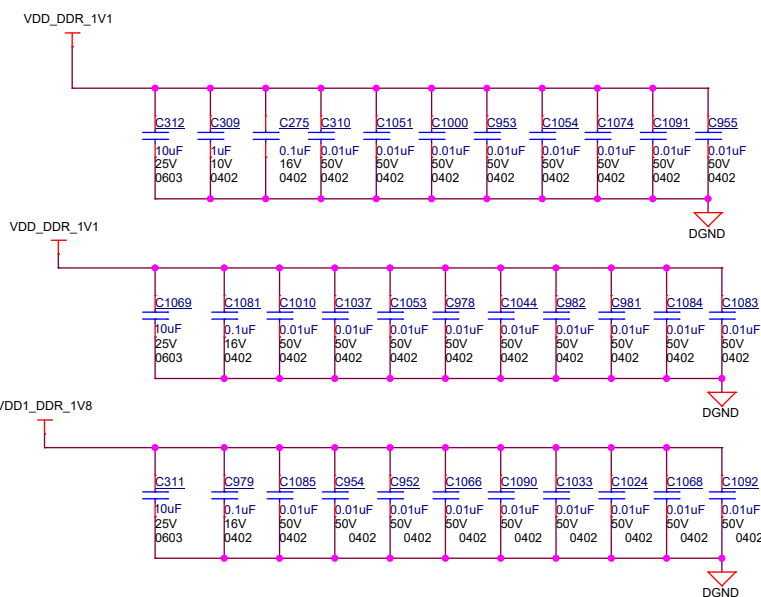
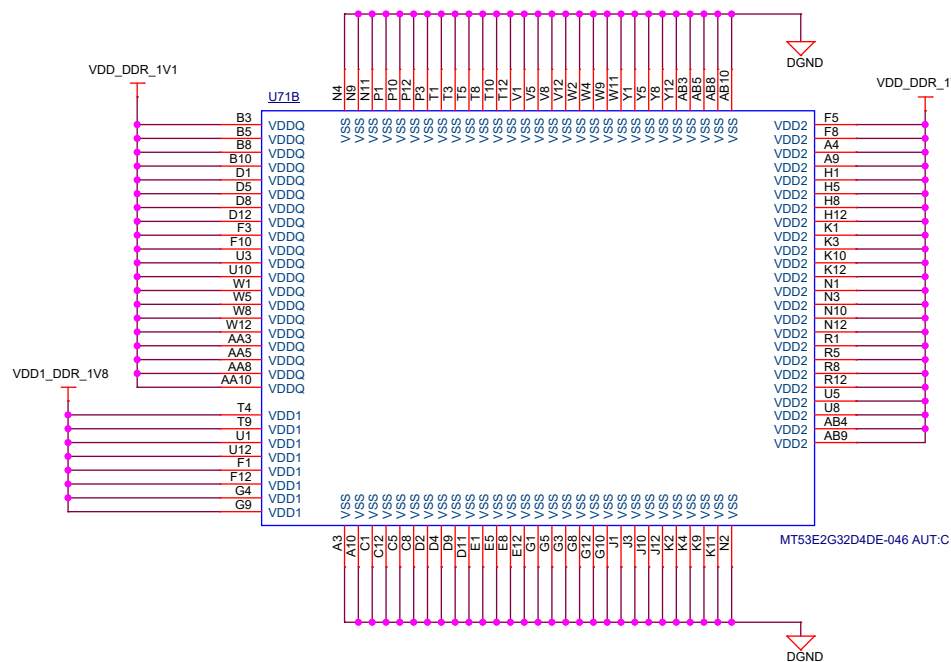
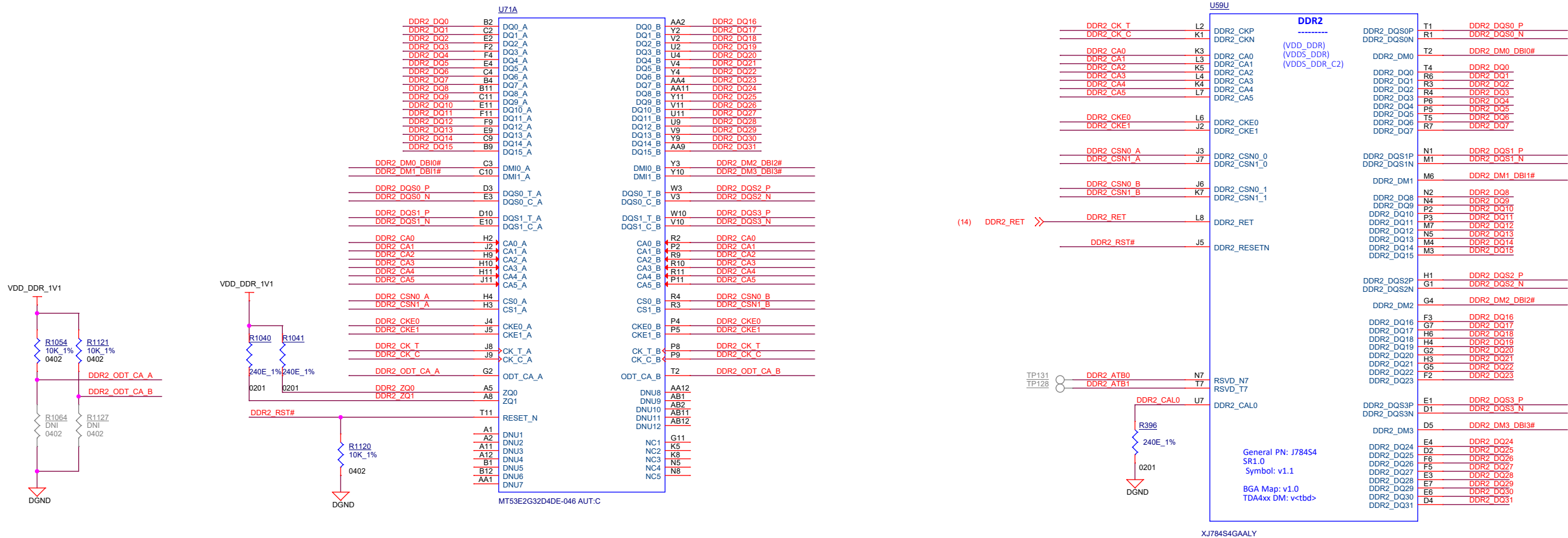
Note: Place DC blocking caps near interface PCIe Connector



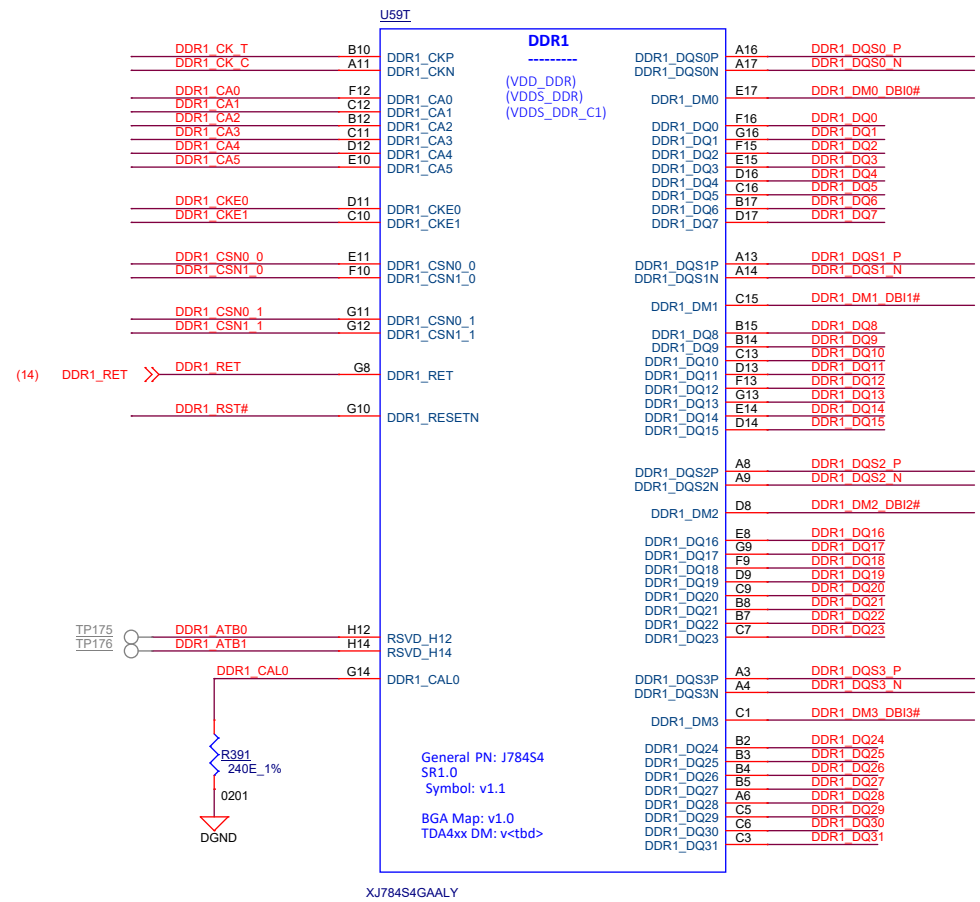
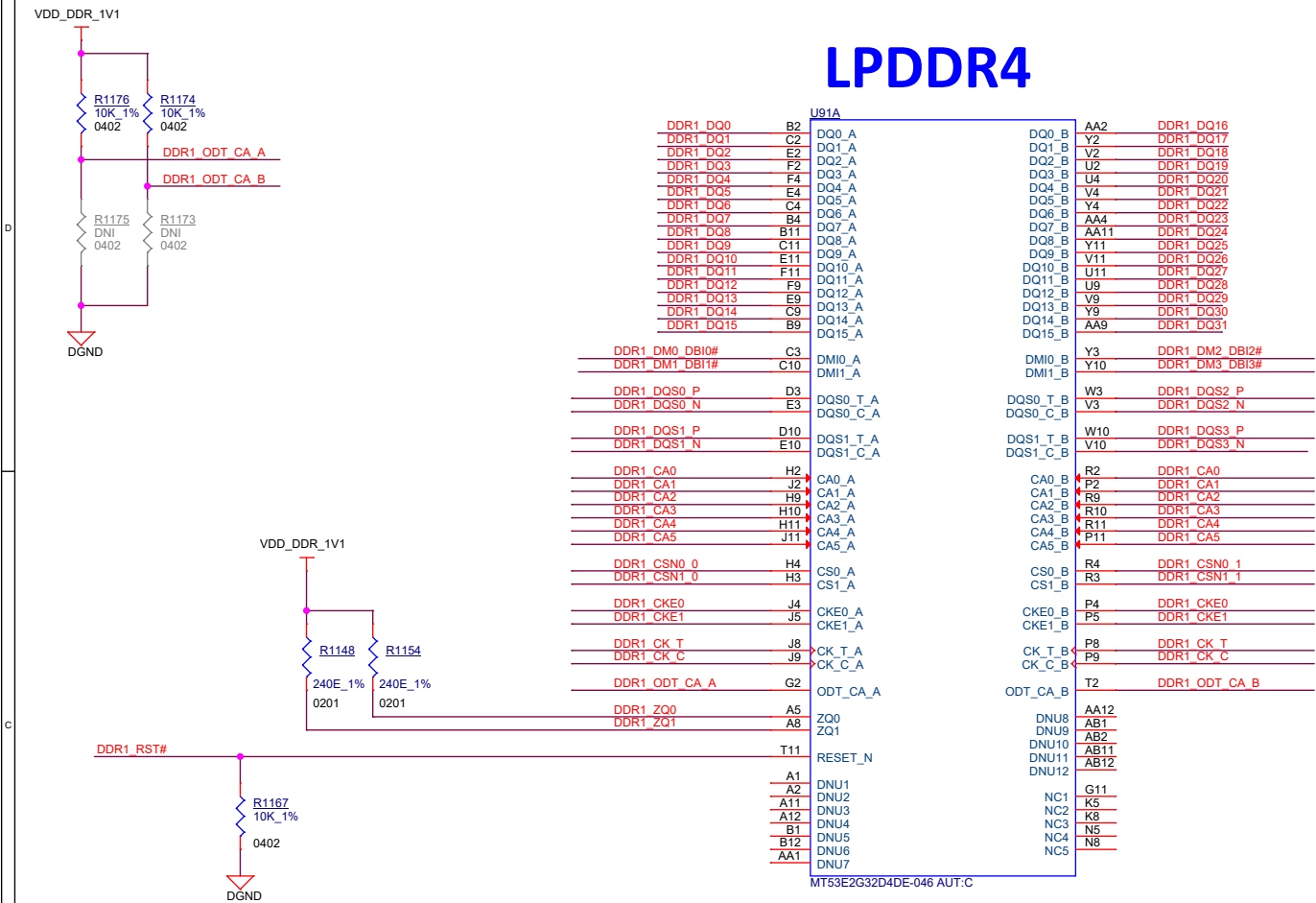
LPDDR4



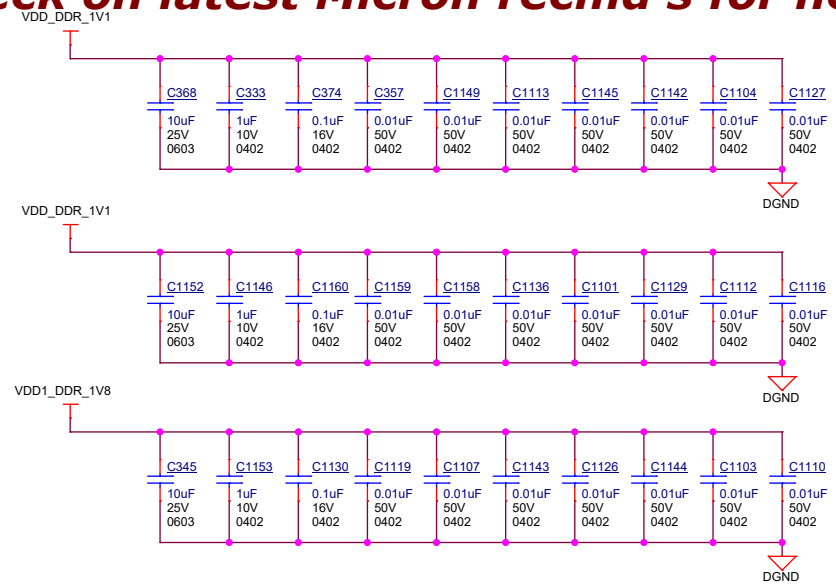
LPDDR4



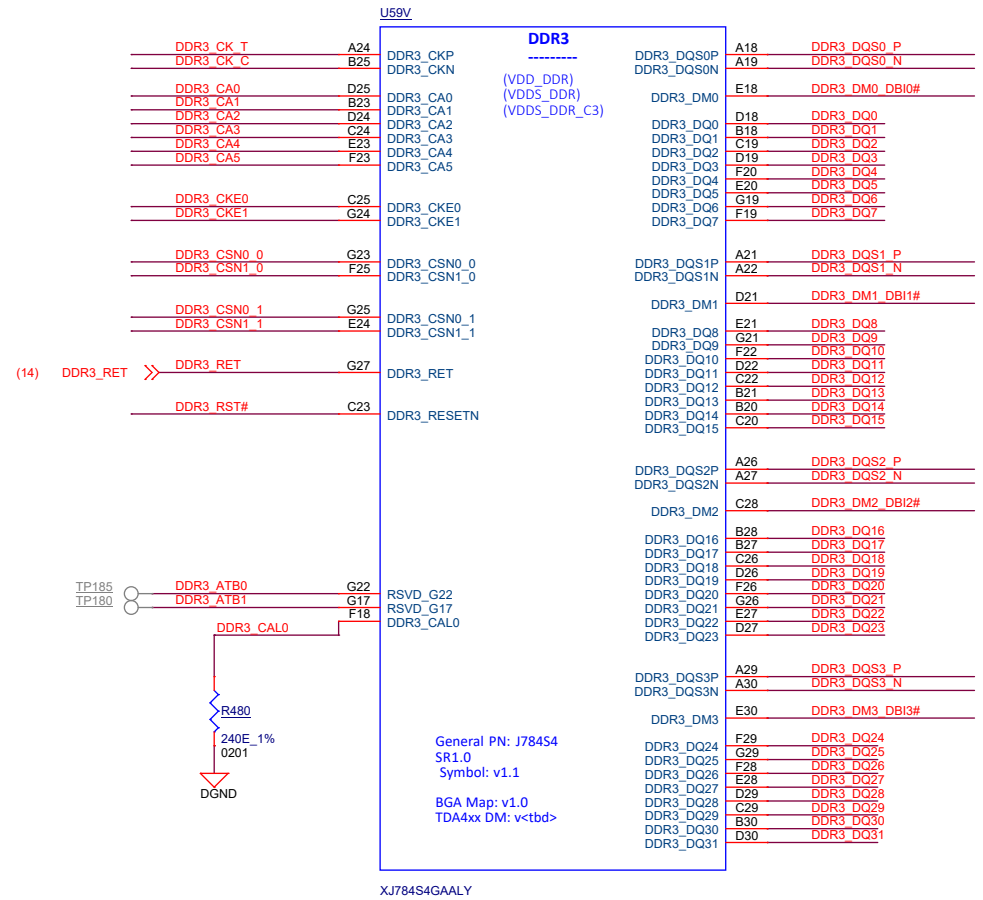
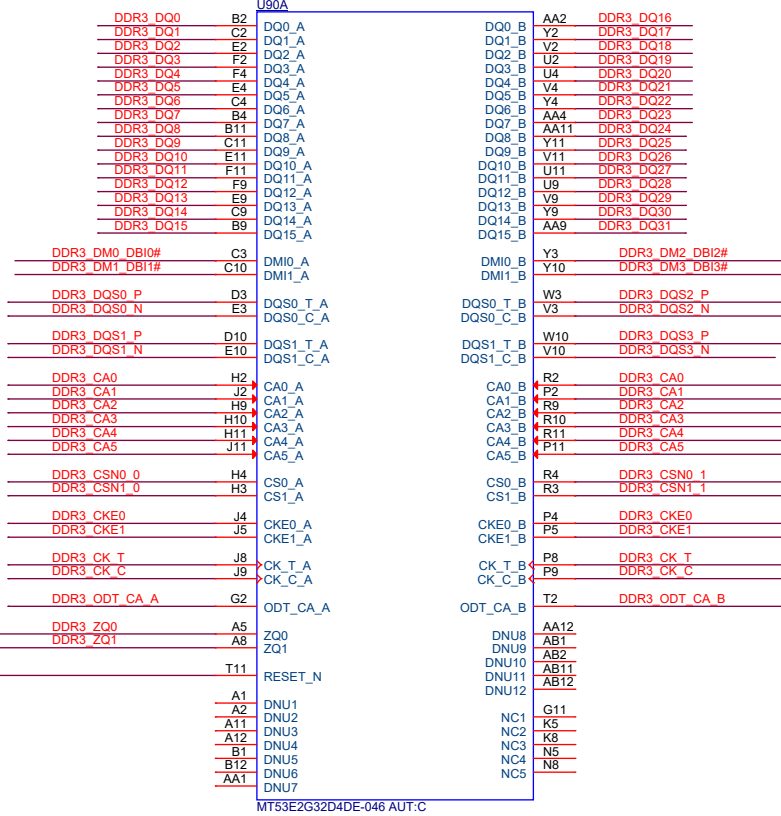
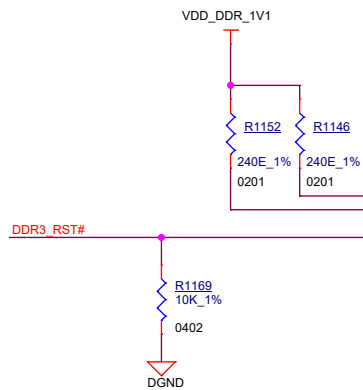
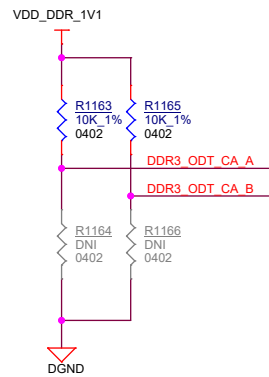
LPDDR4



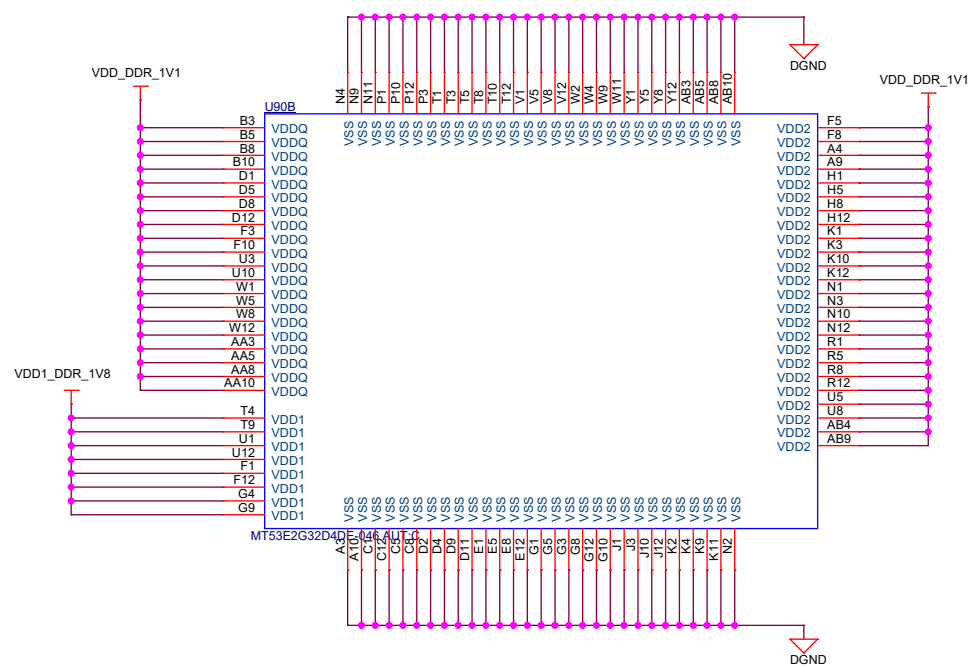
**DDR 1.8V Dcaps could be reduced.
Check on latest Micron recmd's for new PN.**



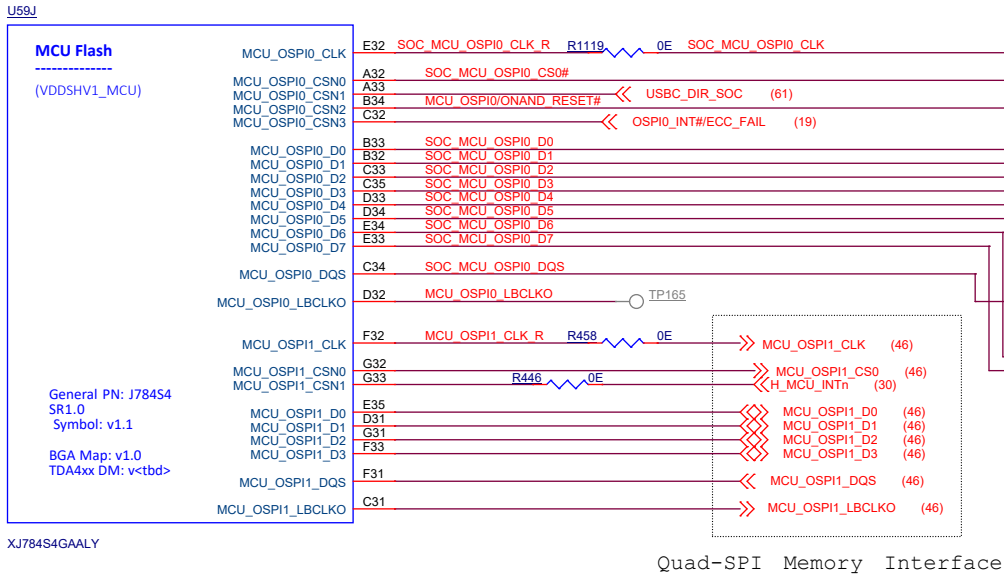
LPDDR4



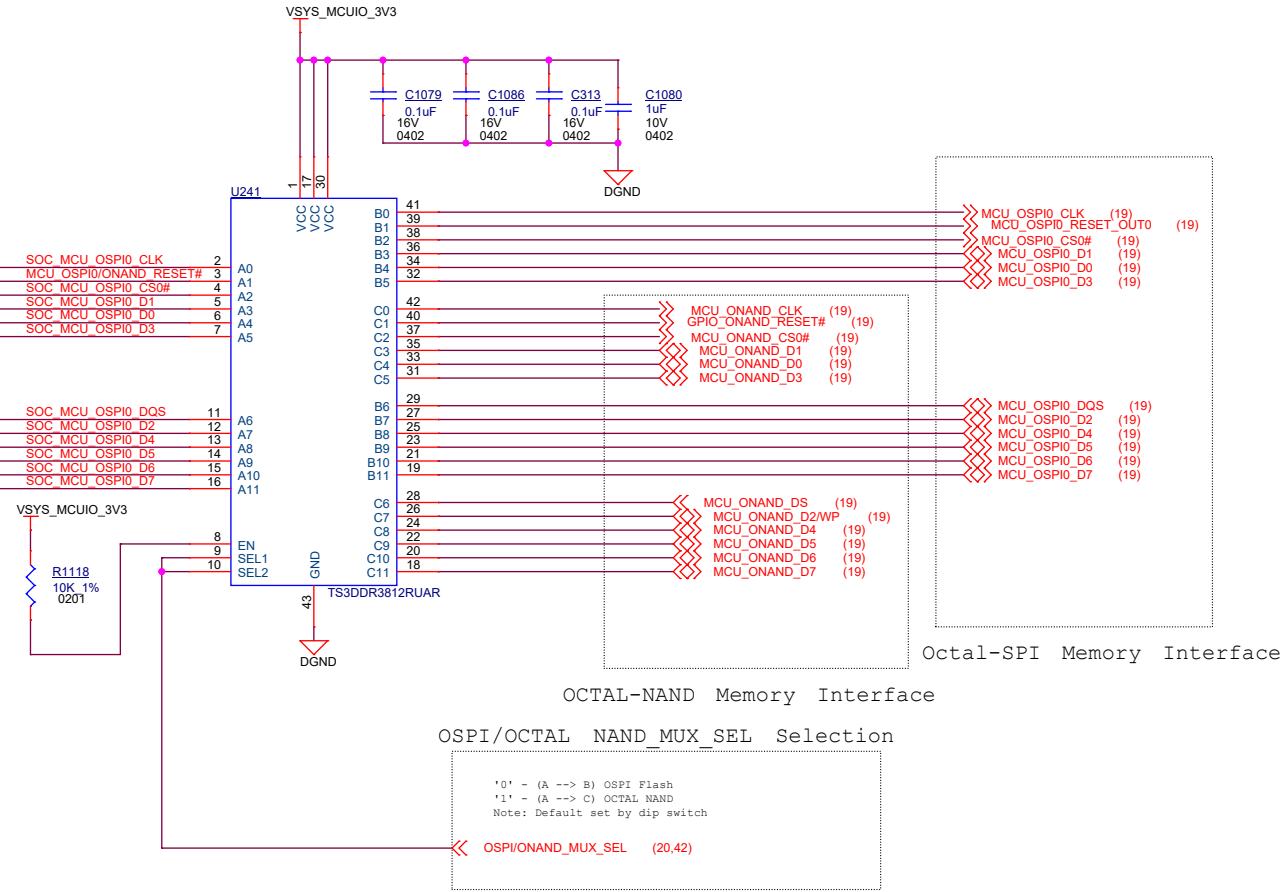
**DDR 1.8V Dcaps could be reduced.
Check on latest Micron recmd's for new PN.**



MCU FLASH

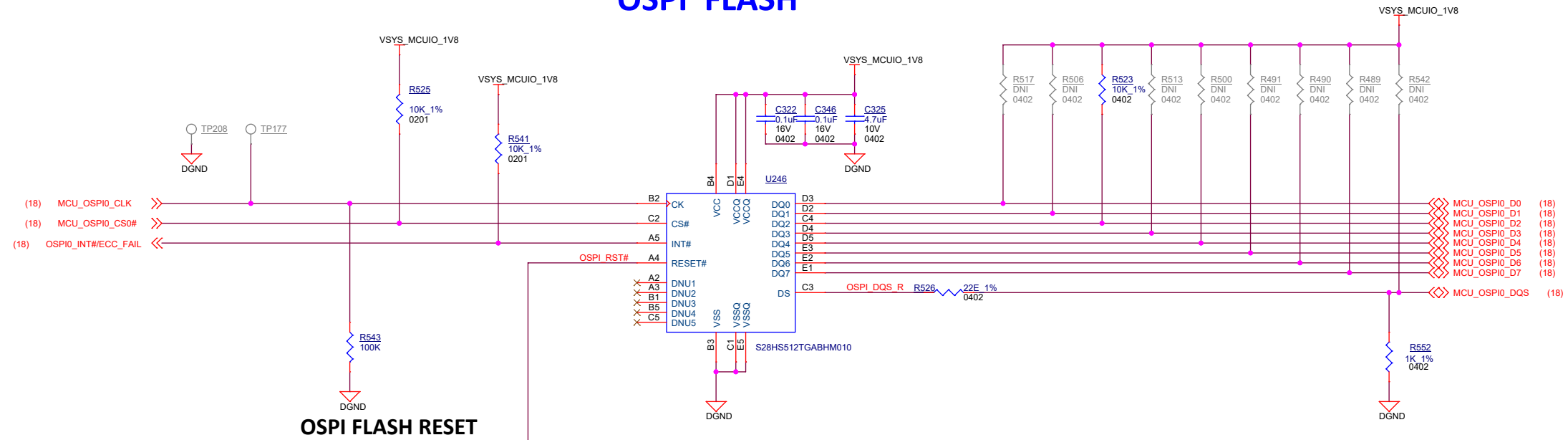


EVM development & evaluation test circuitry
(TI EVM Only)
2:1 Mux for OSPI/OCTAL NAND

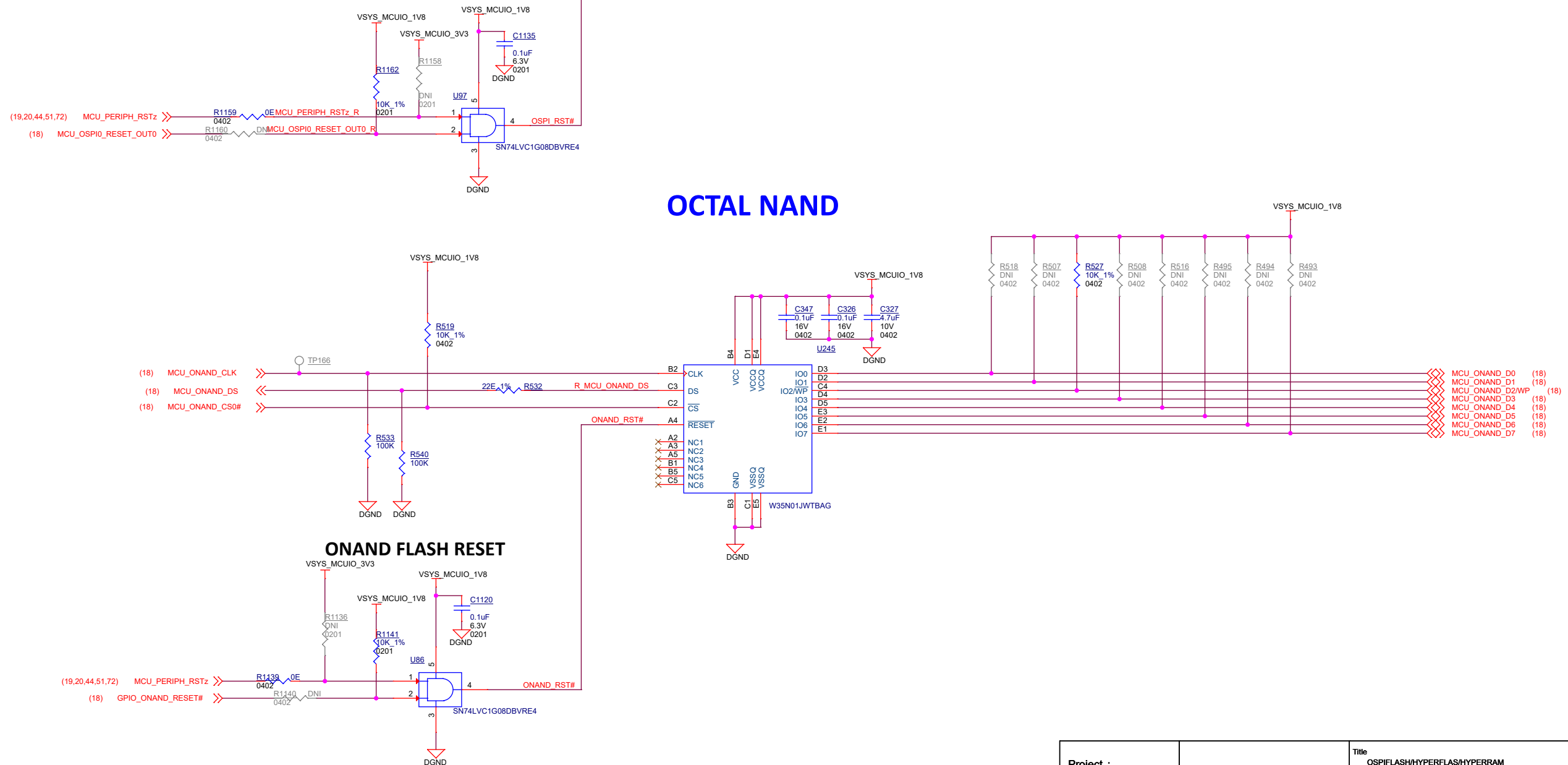


Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

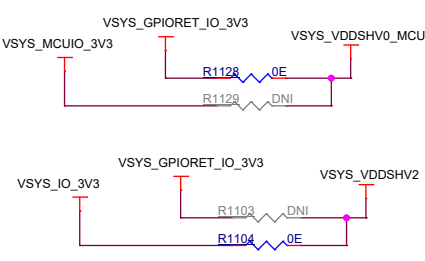
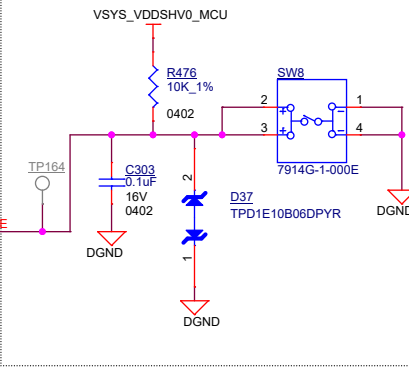
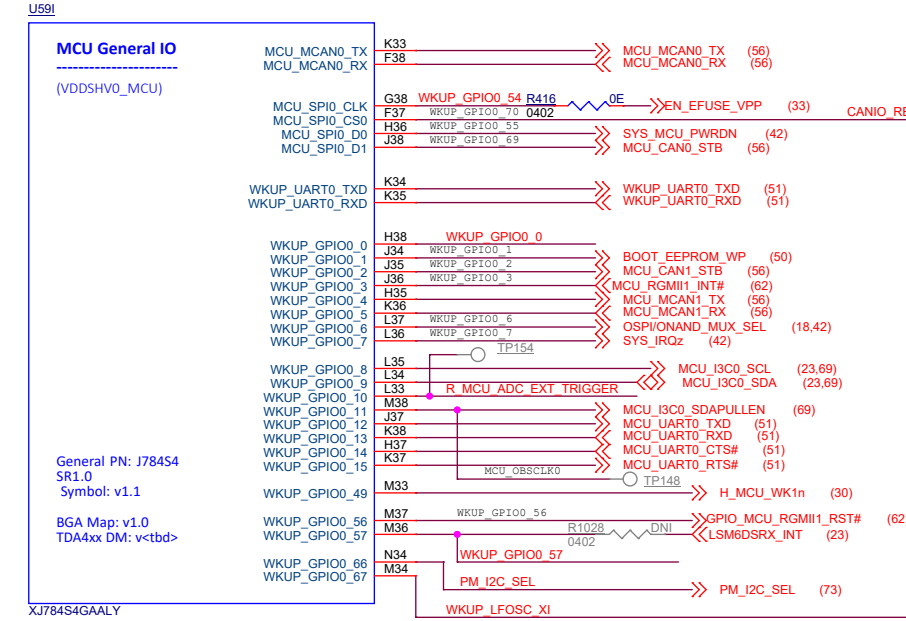
OSPI FLASH



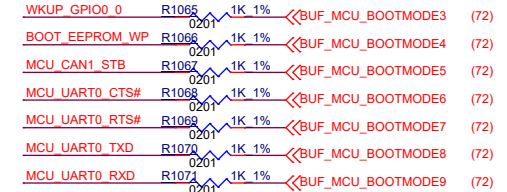
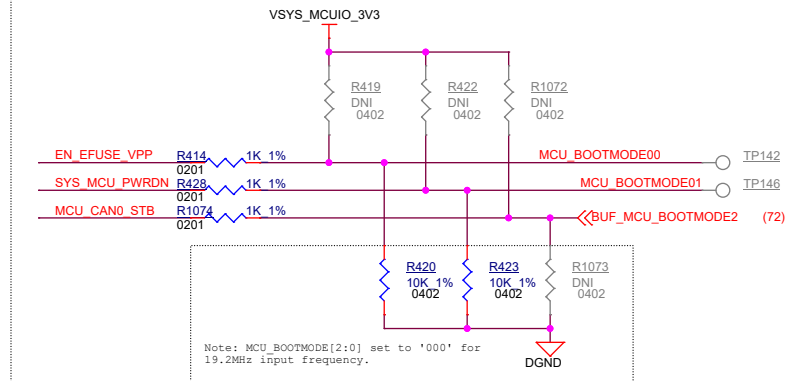
OCTAL NAND



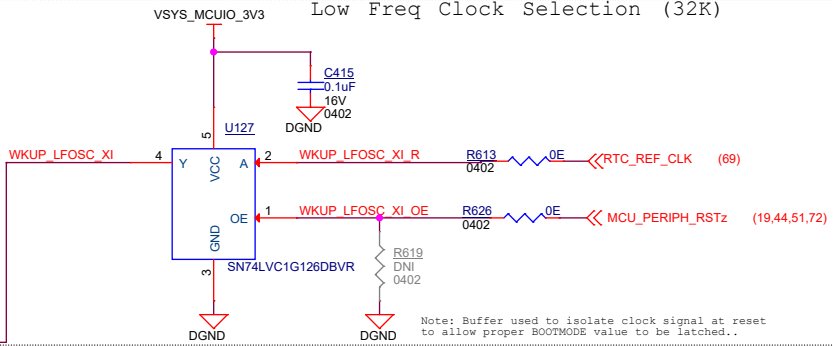
MCU & MAIN GENERAL IO, OSC CLKS



MCU BOOTMODE Control Signals

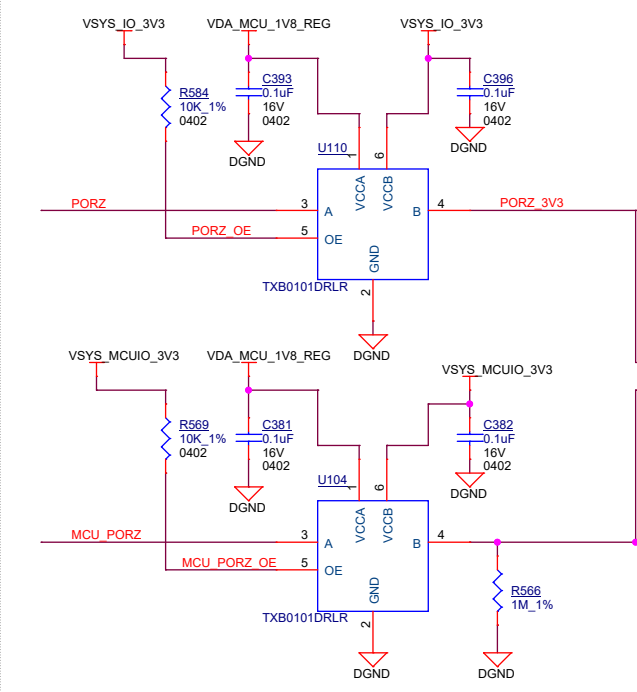


Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

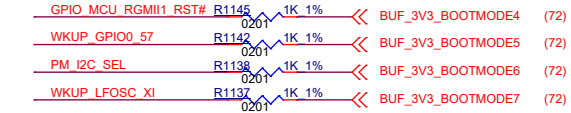


Power-On Reset Buffers

Note: Used to align logic/levels

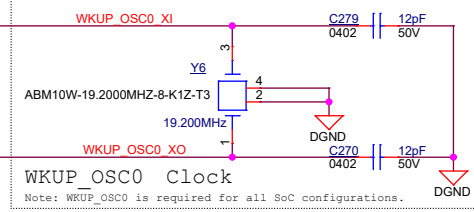
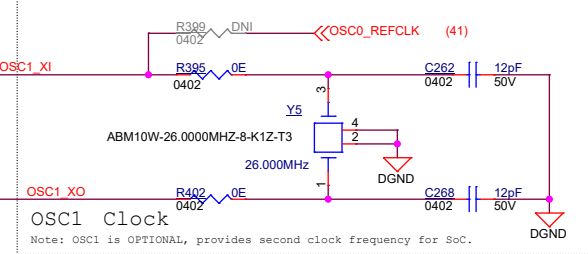
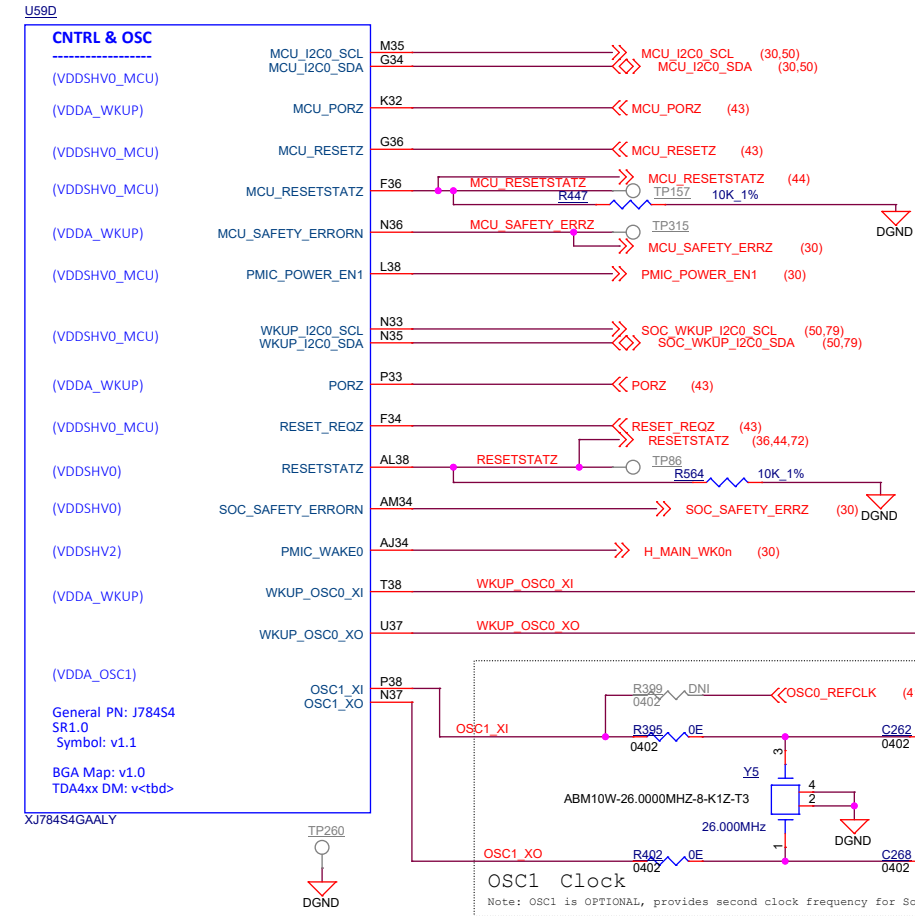


BOOTMODE Control Signals (partial)

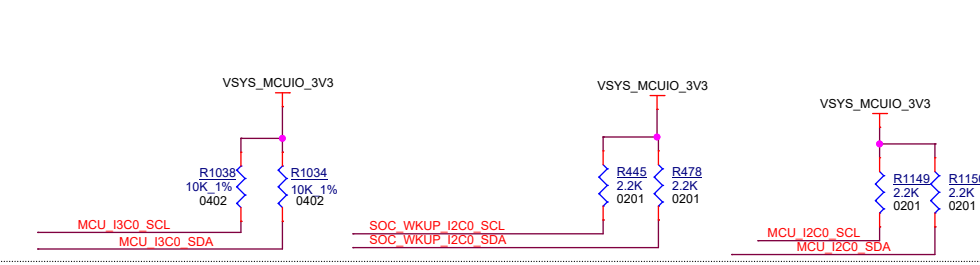


Note: 1K resistors are used to isolate the BOOTMODE control logic after the value is latched.

CONTROL & OSC



MCU I3C/I2C Pull-ups

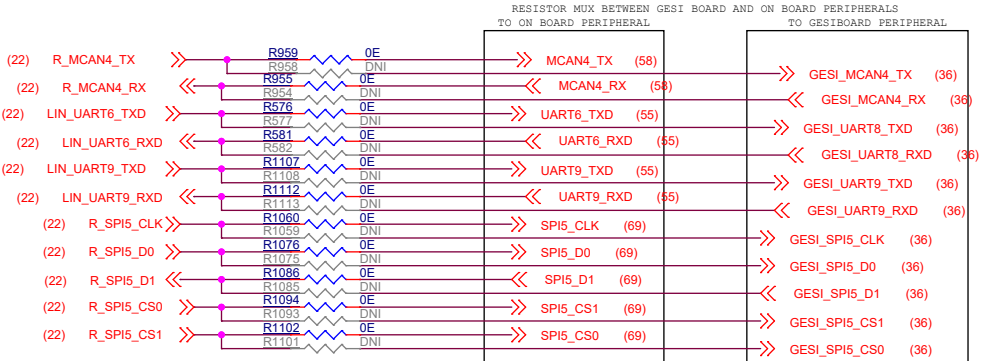
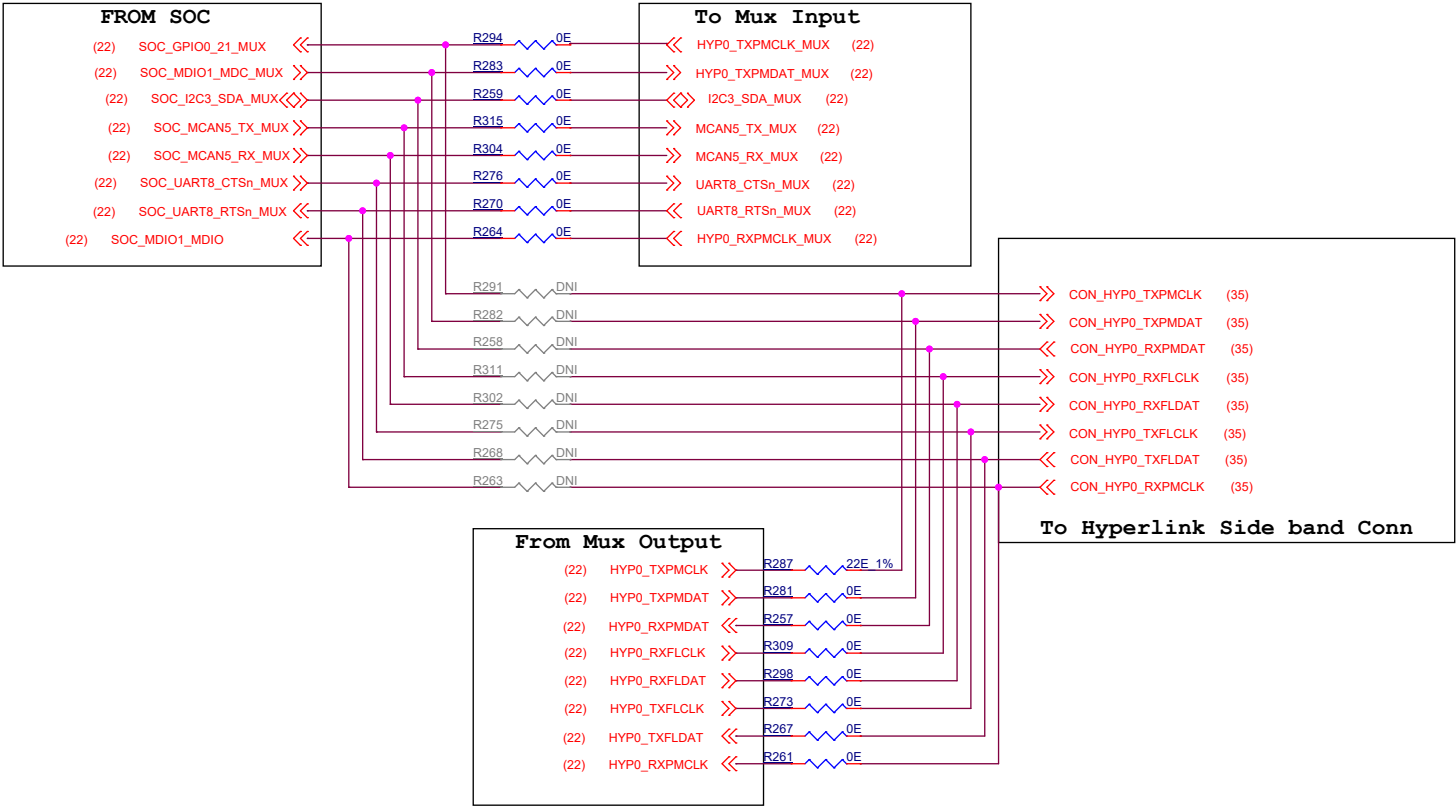


Project :
J7 EVM



Title SOC MCU & MAIN GENERAL		
Size C	PROC141 001 J78454XG01EVM	Rev E2A
Date: Monday, June 20, 2022	Sheet 20 of 88	

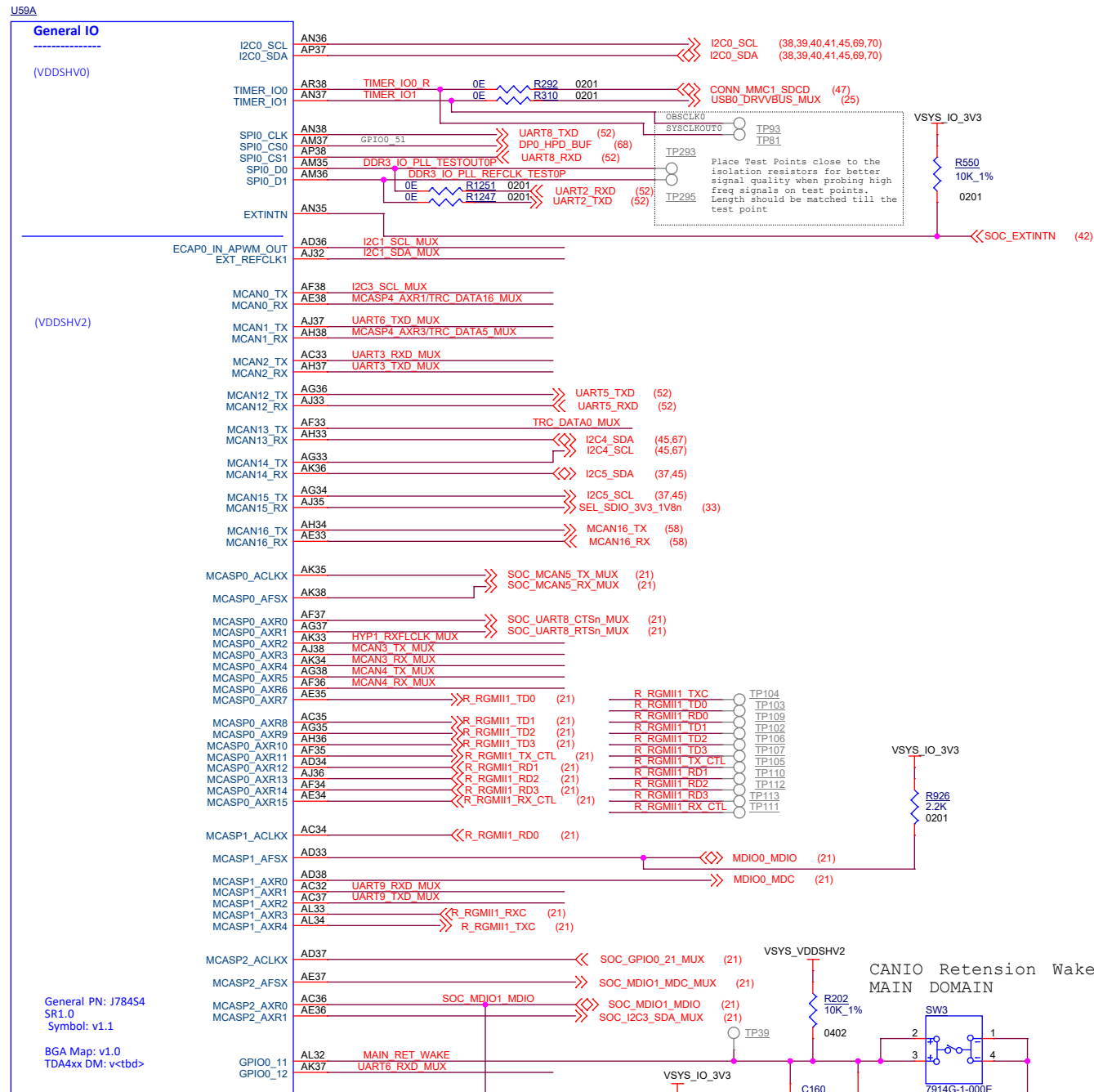
Resistor Mux option to By-pass MUX for Hyperlink sideband signals



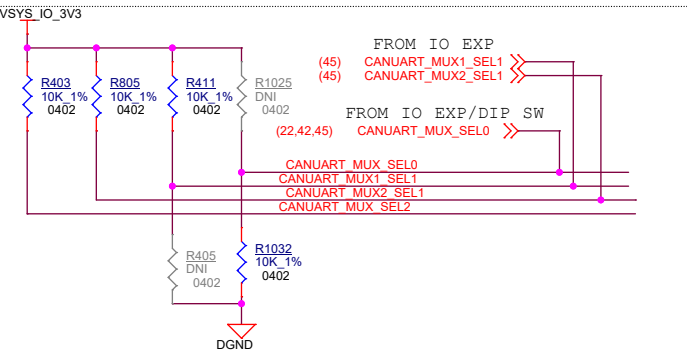
RESISTOR MUX BETWEEN ON BOARD RGMII AND GESI RMII



GENERAL IO

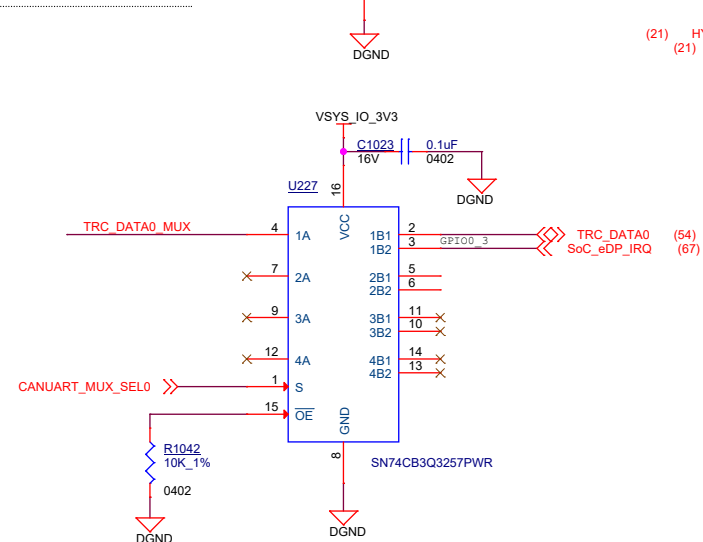


XJ78454GAALY

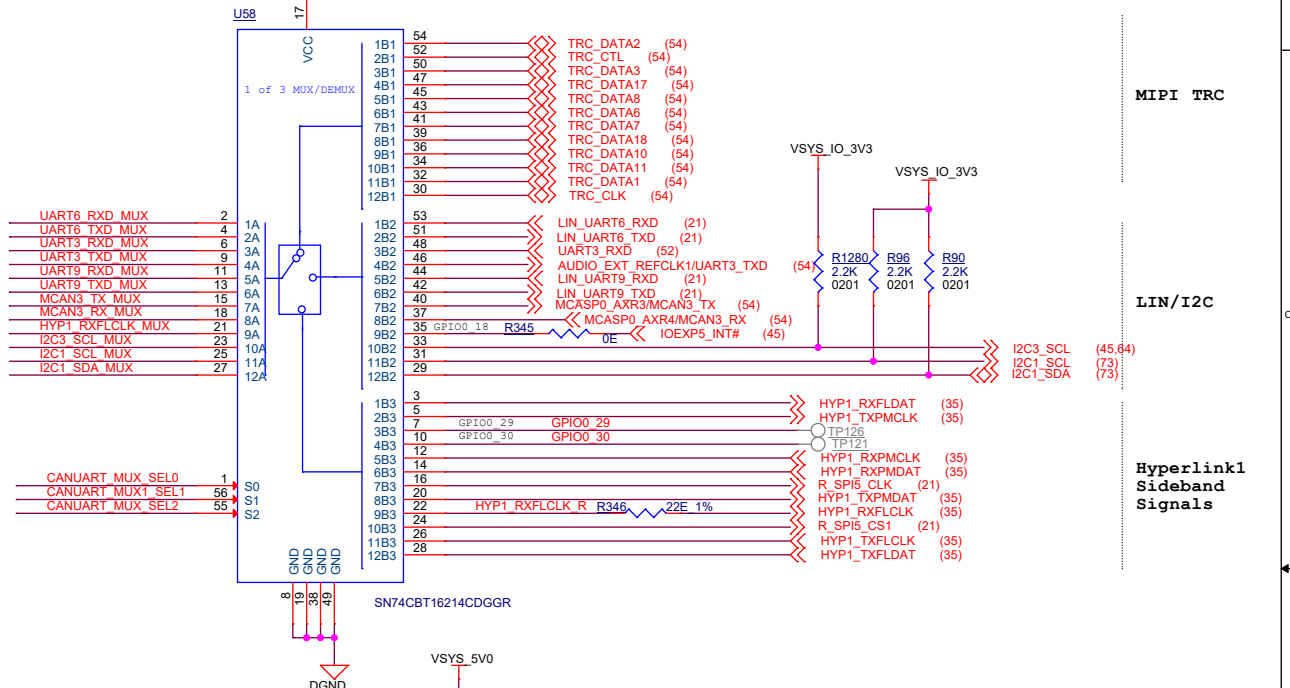


HYPERLINK/TRACE/MCAN/LIN - 1:3 MUX : Truth Table (22,42,45)

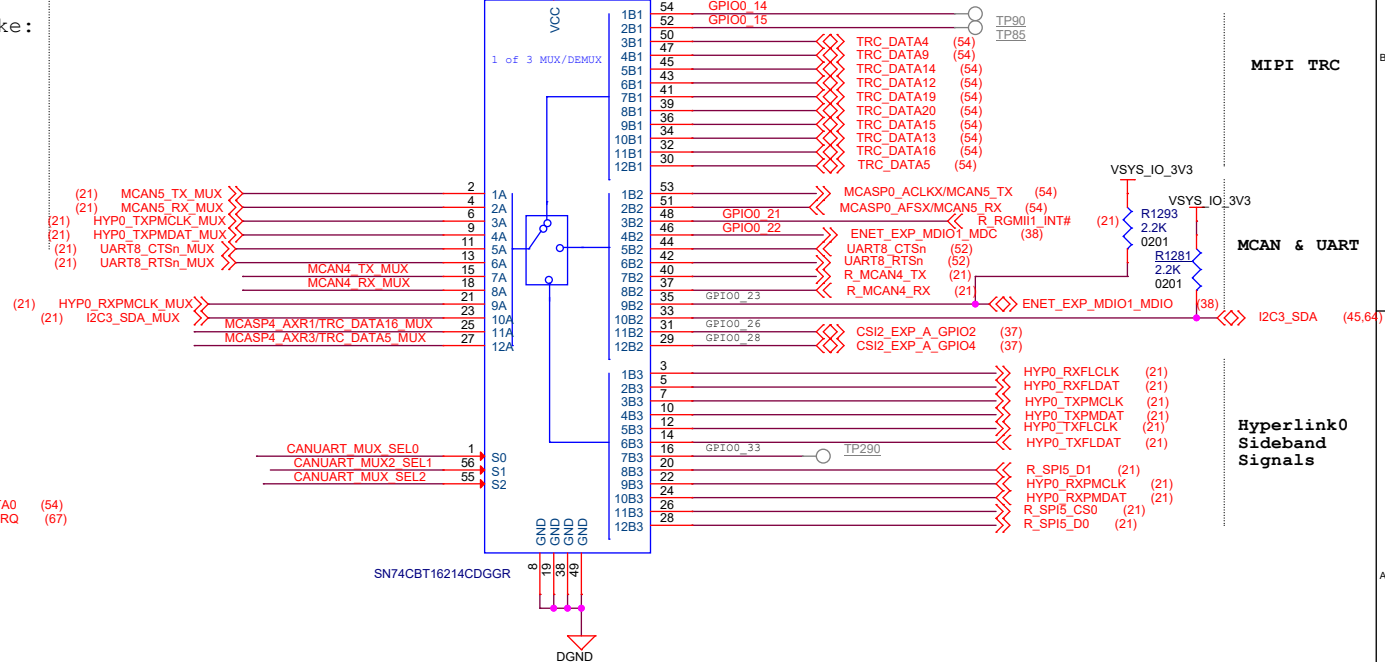
MUX_SEL2	MUX_SEL1	MUX_SEL0	FUNCTION
HIGH	HIGH	LOW	A port = B1 port (default)
HIGH	HIGH	HIGH	A port = B2 port
HIGH	LOW	HIGH	A port = B3 port



MUX1

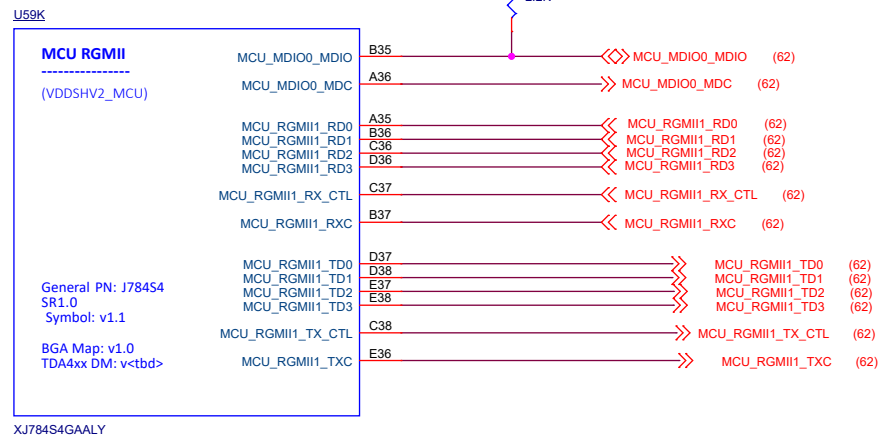


MUX2

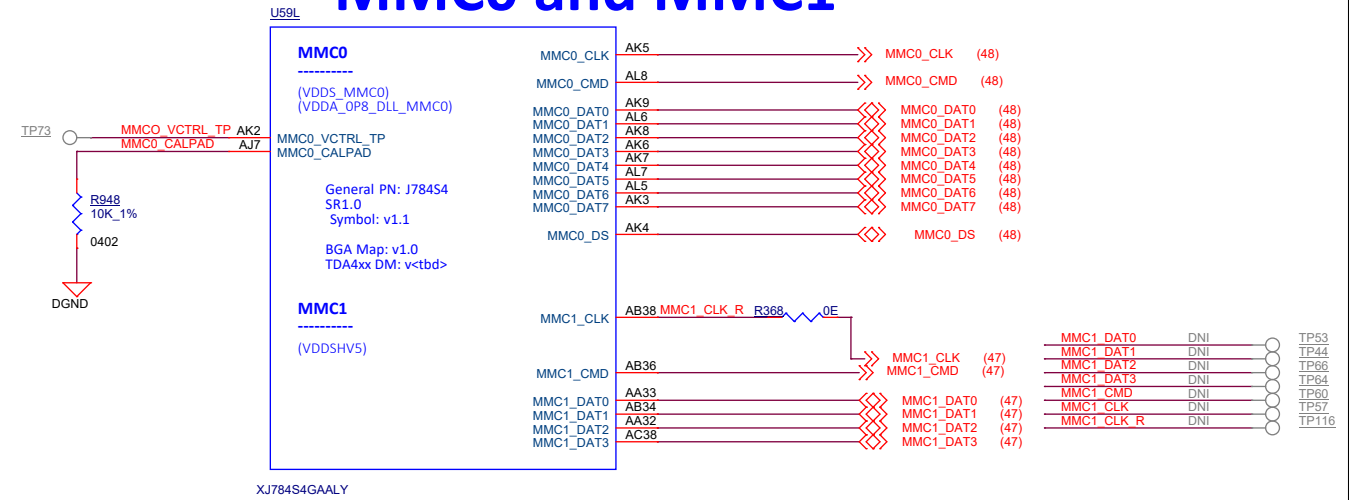


Project : J7 EVM		Title GENERAL IO	
Size C		PROC141 001 J78454XG01EVM	Rev E2A
Date: Monday, June 20, 2022		Sheet 22 of 88	

MCU_RGMII



MMC0 and MMC1



MCU_ADC

Place Beads, 0402 Cs & 0E Rs outside SoC at FP edge
BOM = Install 0E Rs as default

Place 0.1uF Cs across bkout vias & 0E Rs next to Dcaps under SoC
BOM = DNI for 0E Rs (testing option)

ADC 0 & 1 Filtering Scheme:
ADC0/1 VREF P have 2x independent input balls with same in-line supply filtering as common VDA_ADC1V8 pwr rail supplying VDDA_ADC0/1 balls.
(Provisioned supply filtering for PCB layout pending fdbk from TI analog design team.)
-1x Ferrite bead to filter & reduce noise
-1x 0402 (2.2-10uF), SoC perimeter/near end
-1x 0201 for 0.1uF per pwr ball, far end
-1x 0201 0E R to optional short REFN to board GND (as area under SoC allows)

Place R5130 near FL358

Place R5131 near R2369

(69) R_MCU_ADC0_REF_P

(69) R_MCU_ADC0_REF_N

R_MCU_ADC0_REF_P

R_MCU_ADC0_REF_N

DNI

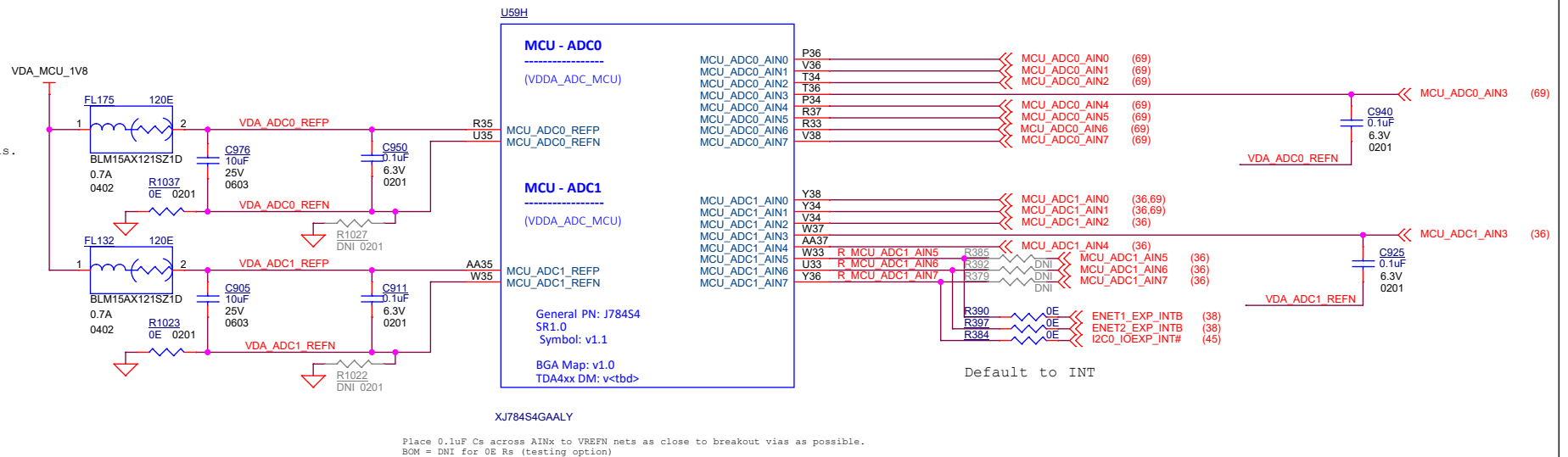
R1049

R1039

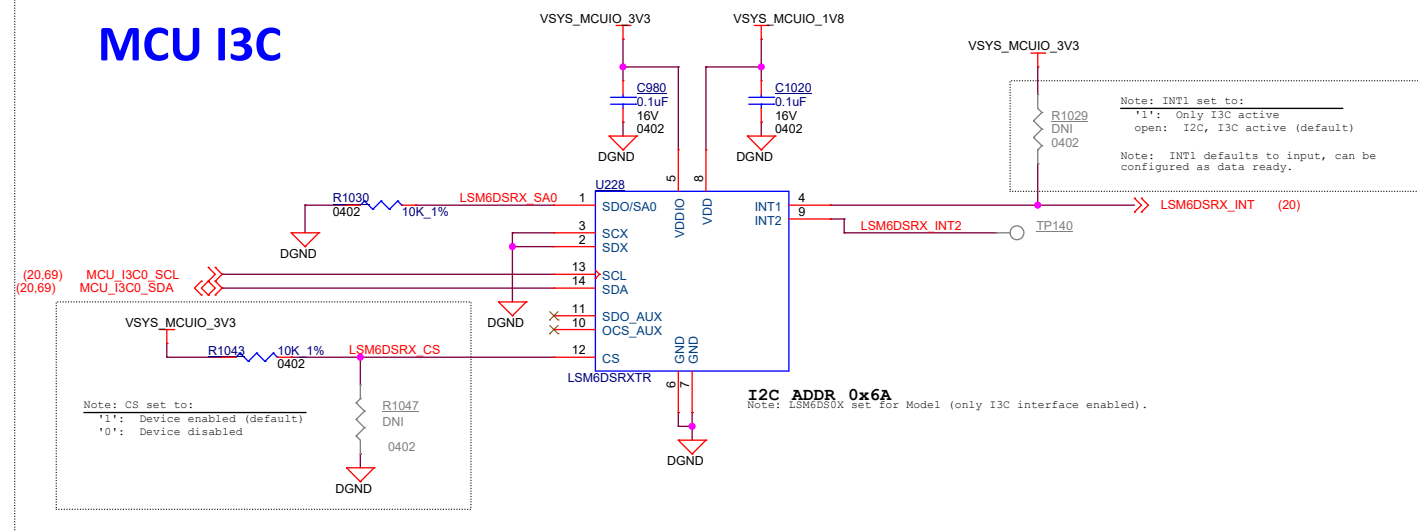
VDA_ADC0_REFP

VDA_ADC0_REFN

DNI



MCU I3C



Project :

J7 EVM



Title
MCU RGMII & ADC

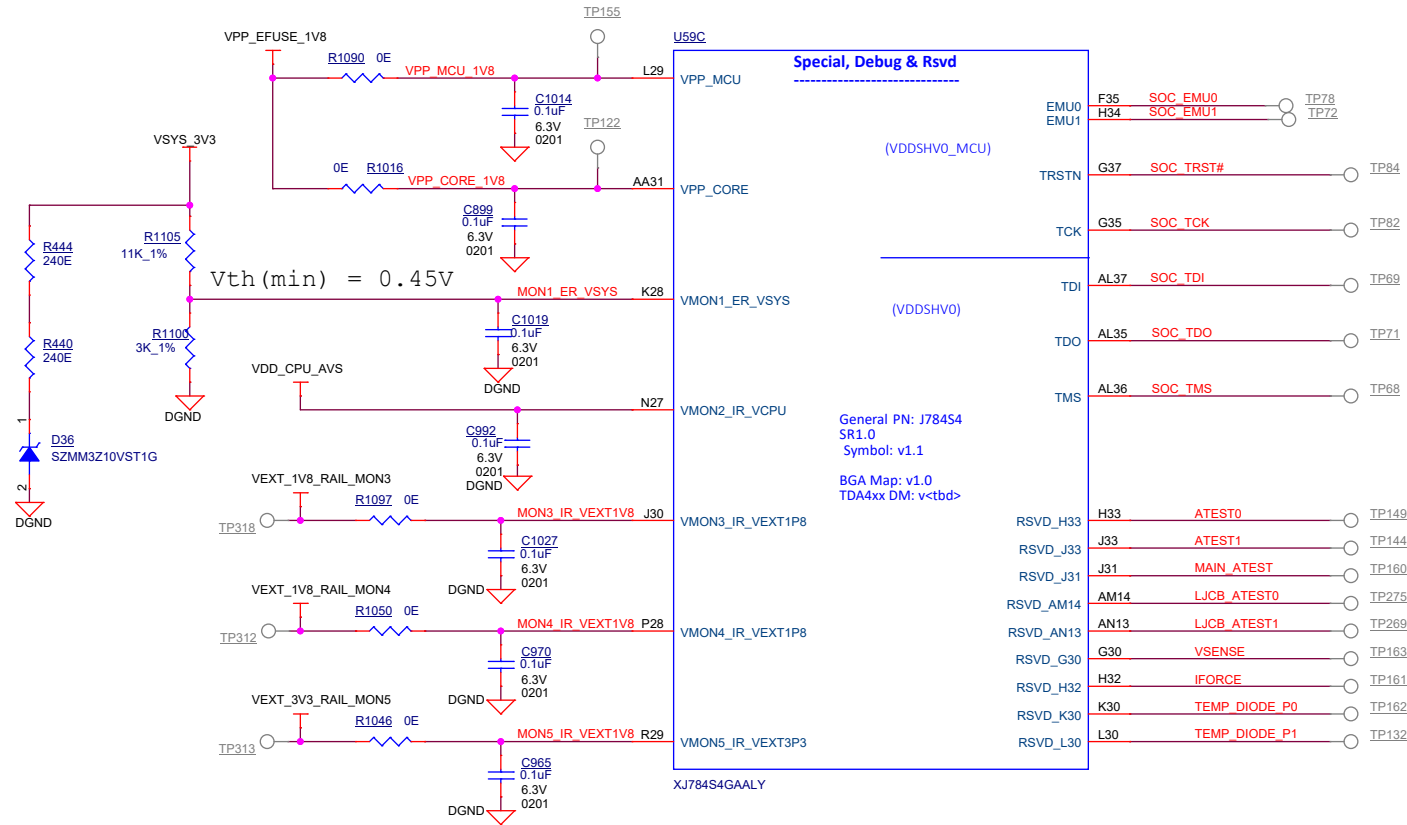
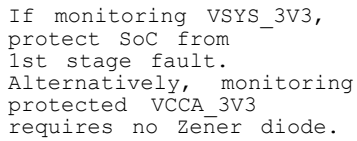
Size
C PROC141 001 J784S4XG01EVM

Date: Monday, June 20, 2022

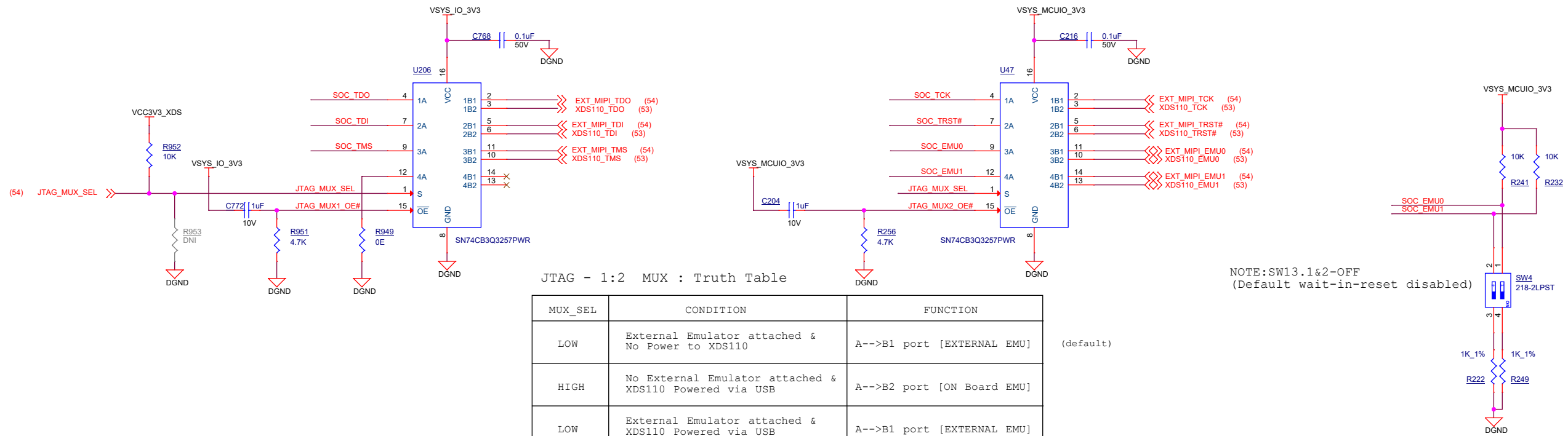
Sheet 23 of 88

Rev
E2A

SPECIAL, DEBUG & RSVD



JTAG AND TRACE MUX



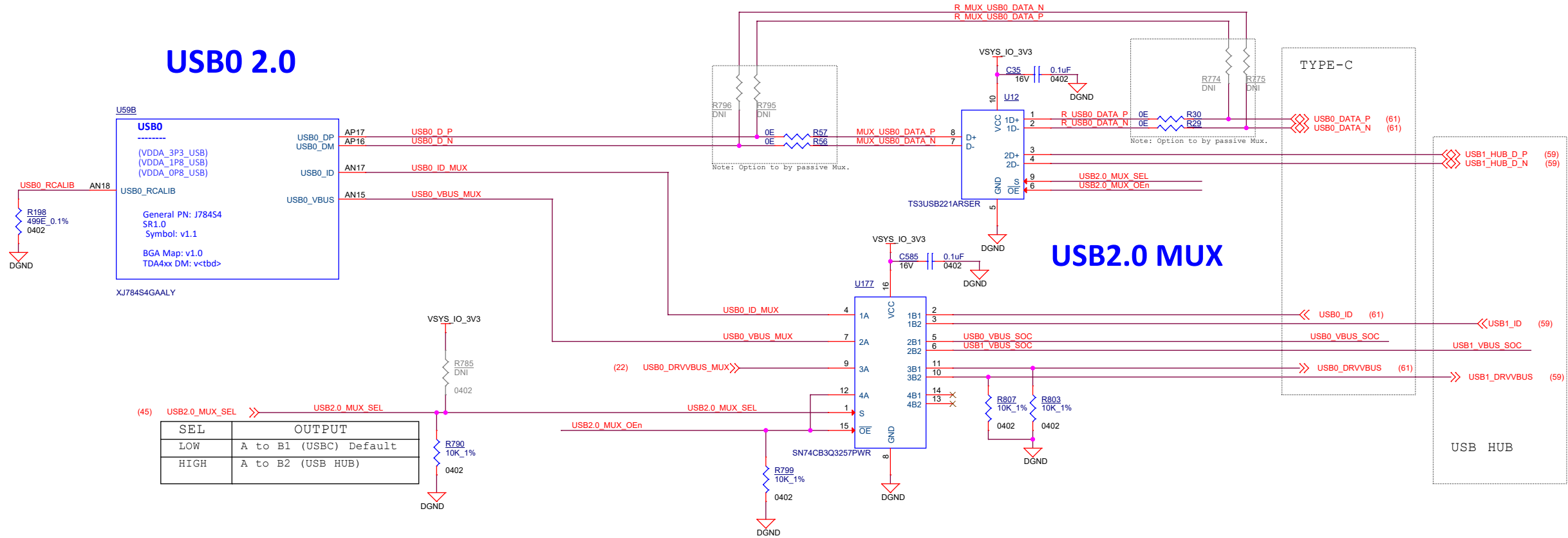
JTAG - 1:2 MUX : Truth Table		DGND
MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU] (default)
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]
LOW	External Emulator attached & XDS110 Powered via USB	A-->B1 port [EXTERNAL EMU]
LOW	No External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]

NOTE:SW13.1&2-OFF
(Default wait-in-reset disabled)

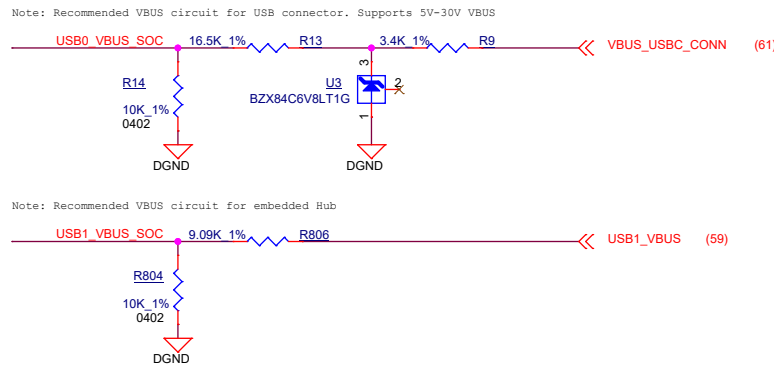
USB0 2.0

By Pass USB MUX	Mount - R796,R795,R774,R775 DNI -R57,R56,R30,R29
USB MUX (Default)	Mount -R57,R56,R30,R29 DNI - R796,R795,R774,R775

USB0 2.0



USB VBUS Resistor divider circuit



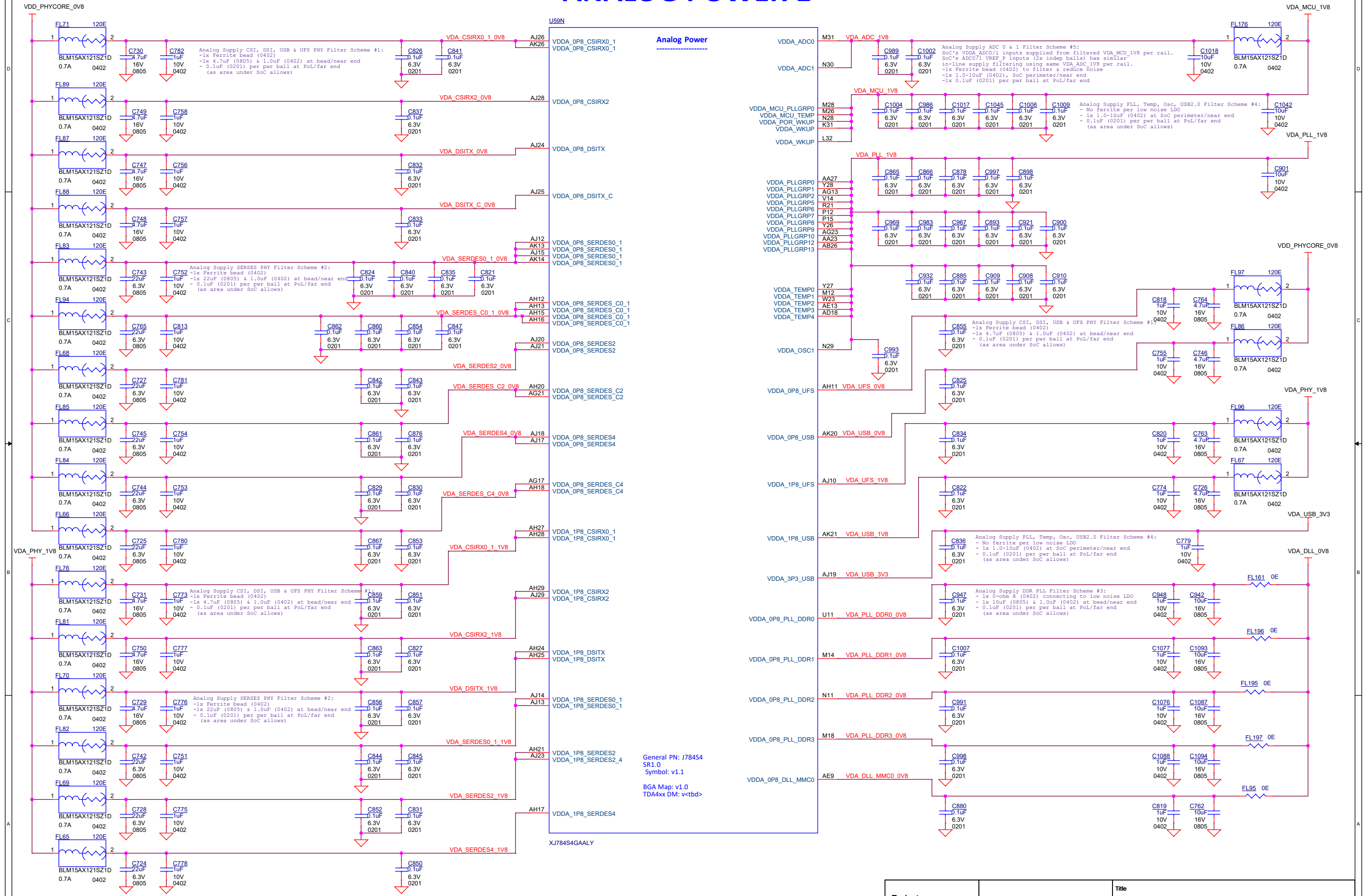
Project :
J7 EVM



Title	SOC USB 2.0
-------	-------------

Size	PROC141 001 J784S4XG01EVM	Rev
C		E2A
Date:	Monday, June 20, 2022	Sheet 25 of 88

ANALOG POWER 1

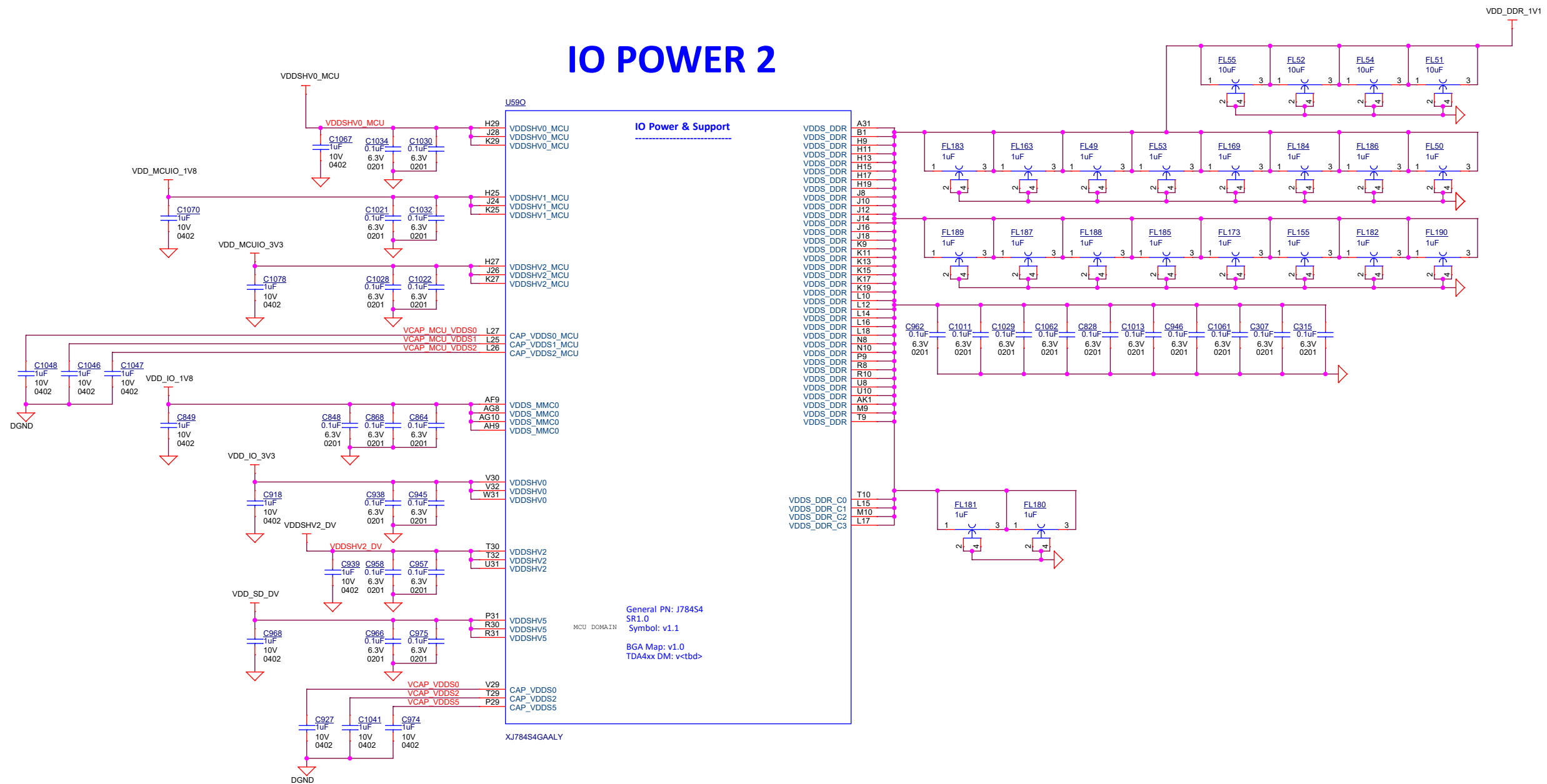


Project :
J7 EVM

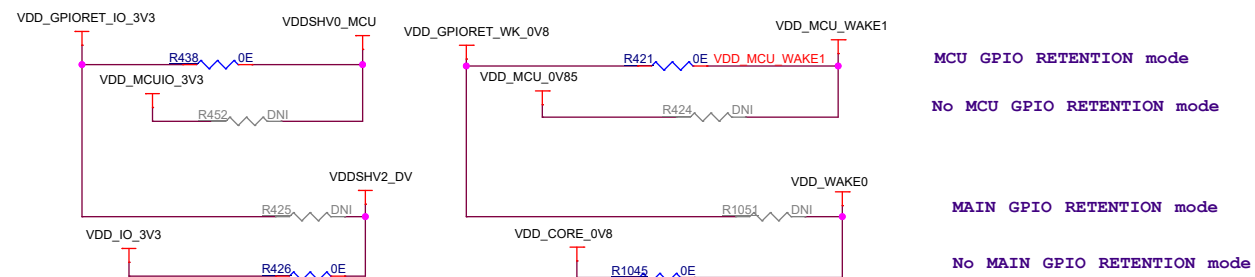


Title			
SOC ANALOG POWER 1			
Size	PROC141 001 J784S4XG01EVM		Rev
C			E2A
Date:	Monday, June 20, 2022	Sheet 26 of	88

IO POWER 2



EVM development & evaluation Test circuitry
EVM GPIO Retention testing option
(TI EVM Only)



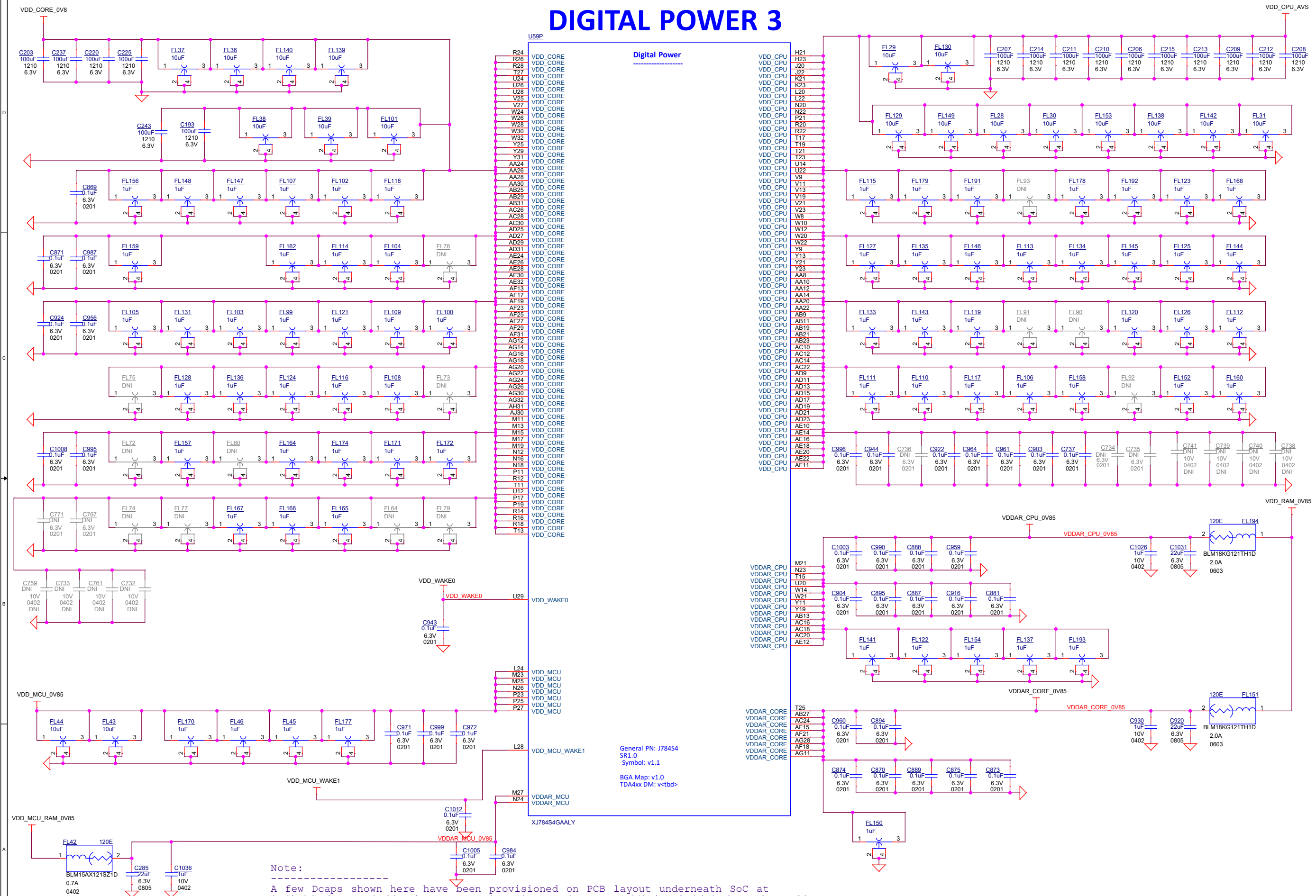
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

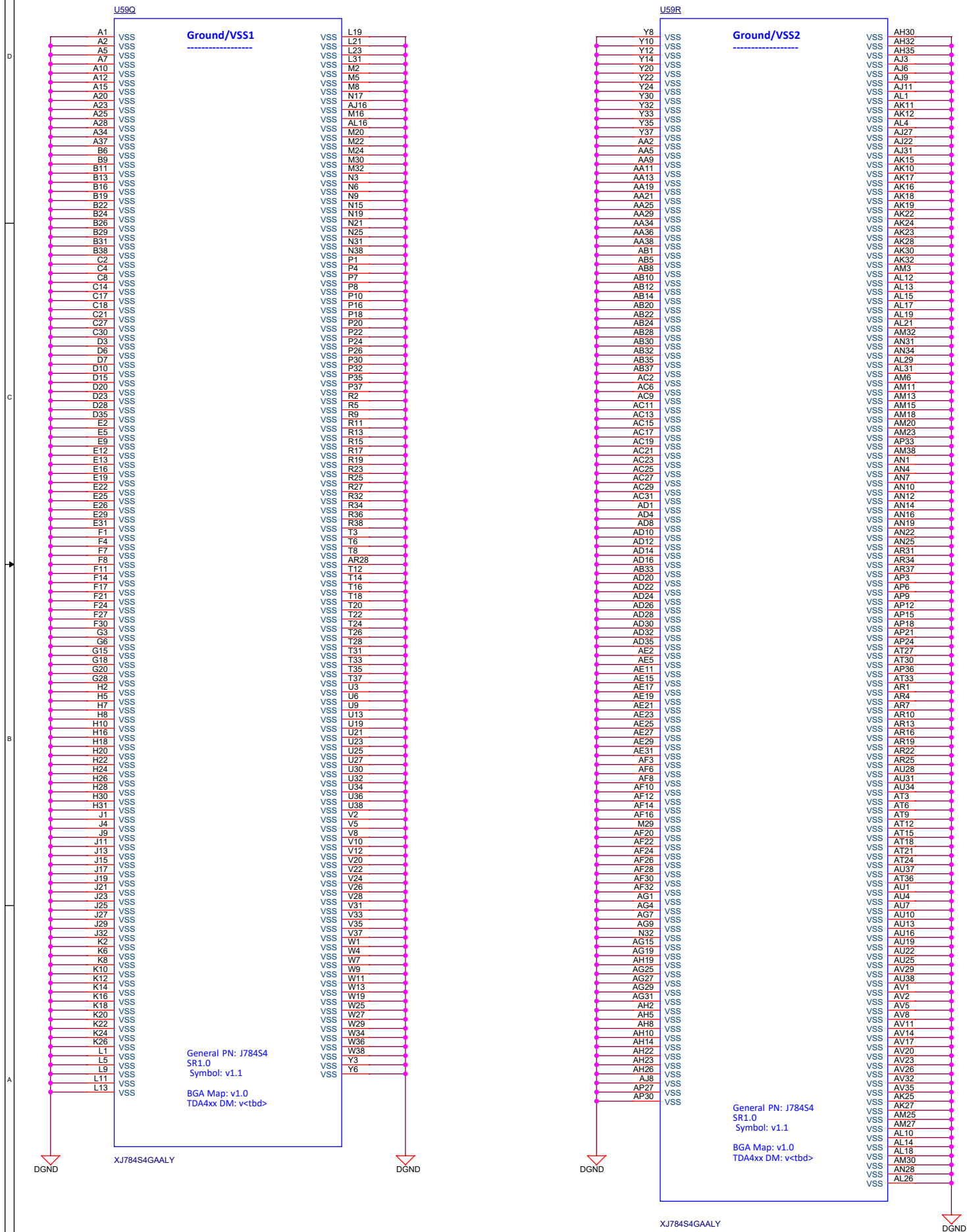
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Low power modes	Resistors to be Populated	Resistors to be DNI'd
No GPIO RET	R452,R424,R426,R1045	R438,R421,R425,R1051
MCU GPIO RET only	R438,R421,R426,R1045	R452,R424,R425,R1051
MAIN GPIO RET only	R452,R424,R426,R1051	R438,R421,R426,R1045
MCU & MAIN GPIO RET	R438,R421,R425,R1051	R452,R424,R426,R1045

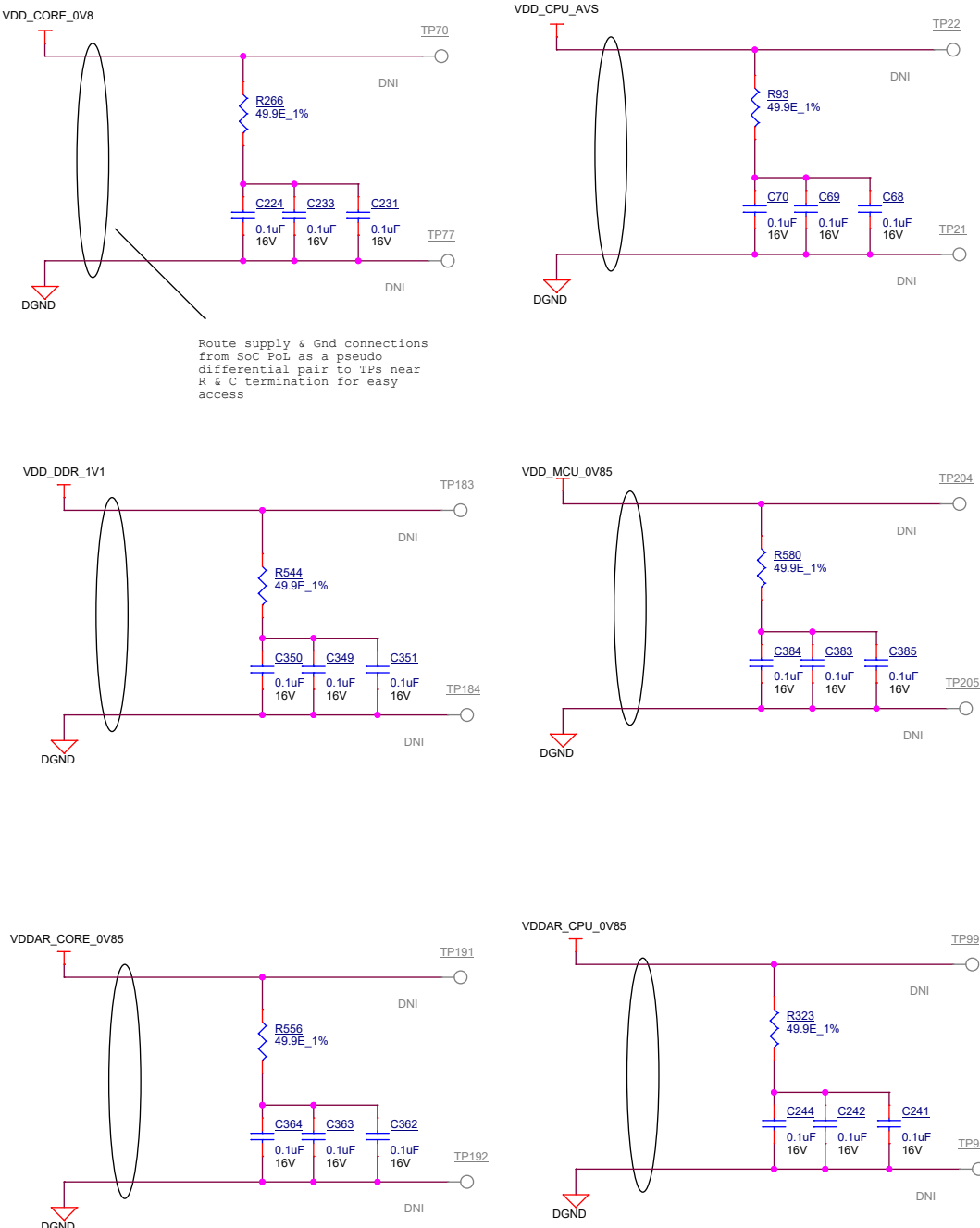
DIGITAL POWER 3



SOC GROUND



SoC Supply Noise Kelvin Sensing



PMIC

"PCB Notes":

For multi-phase Buck converter configs, route remote sense feedback as follows:

1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs, route remote sense feedback as follows:

1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.

Route as Pseudo diff pair traces (See "PCB Notes")

Note: Keepout needs to be provided for the VDD_DDR_1V1 and Gnd vias of the feedback pins connecting to the PMIC.

Line to Shape keepout needs to be given in layout for VDD_DDR_1V1 and DGND feedback traces

PMIC-A uses default I2C ADDR: 0x48, 0x49, 0x4A & 0x4B

SoC, Open-Drain, Active Low

Active High 1.8V logic

SN74LVC1G07 is used to isolate power from PMIC to SoC when SoC is powered off

Project :

J7 EVM



Title PMIC A		
Size C	PROC141 001 J784S4XG01EVM	Rev E2A
Date: Monday, June 20, 2022	Sheet 30 of 88	

VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

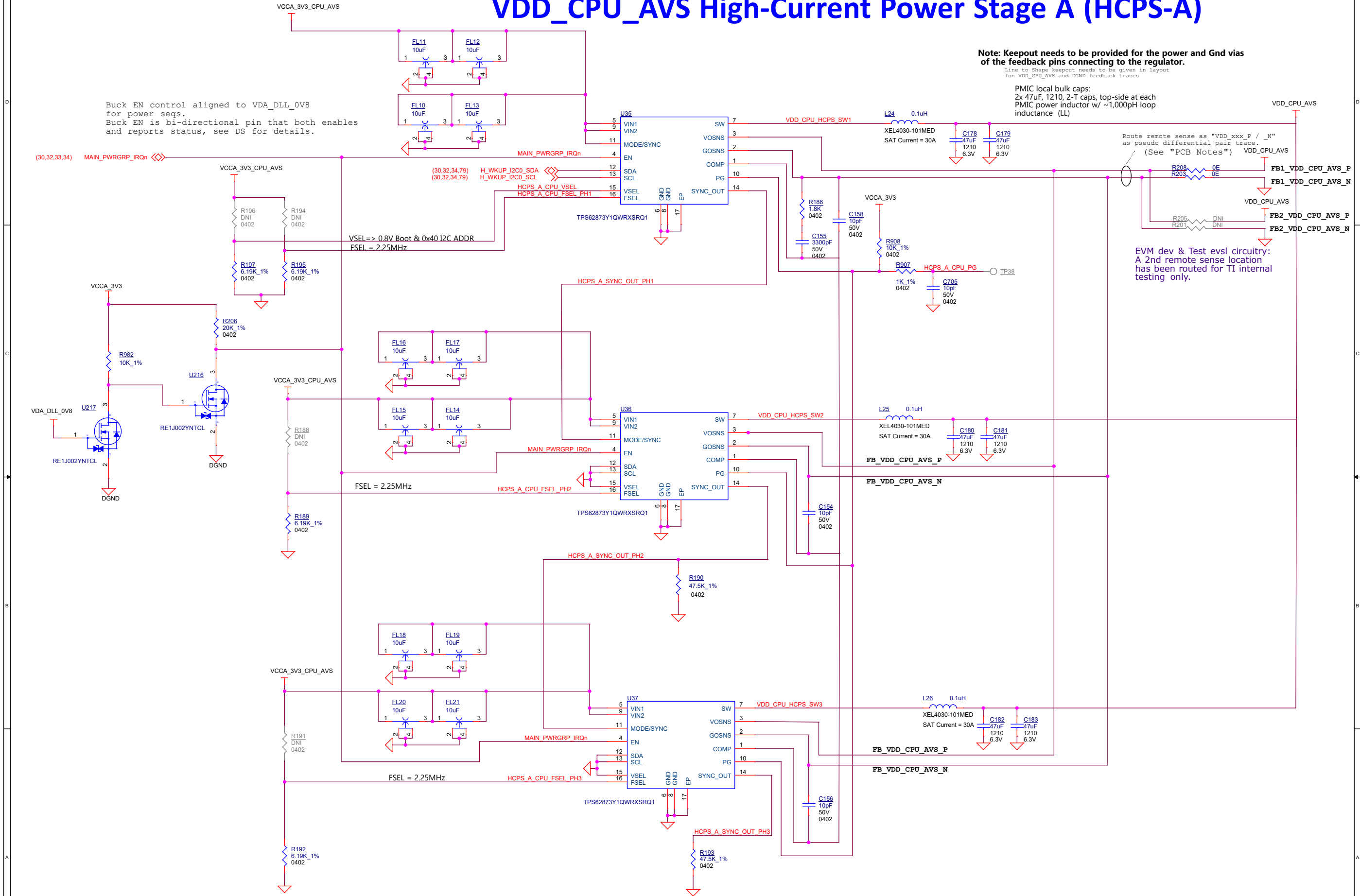
Note: Keepout needs to be provided for the power and Gnd vias of the feedback pins connecting to the regulator.
Line to Shape keepout needs to be given in layout for VDD_CPU_AVS and DGND feedback traces

PMIC local bulk caps:
2x 47uF, 1210, 2-T caps, top-side at each
PMIC power inductor w/ ~1,000pH loop inductance (LL)

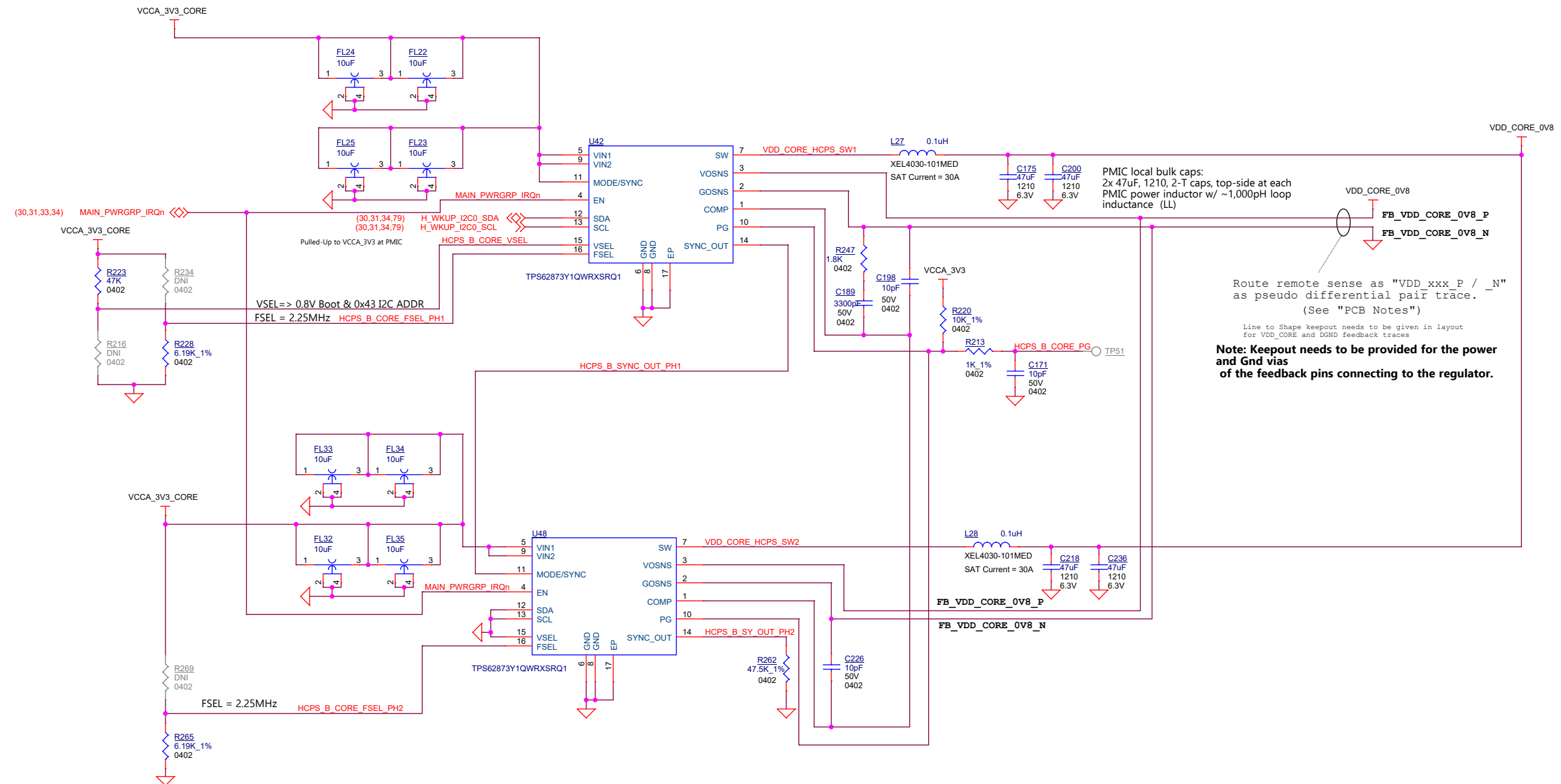
Buck EN control aligned to VDA_DLL_0V8 for power seqs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.

Route remote sense as "VDD_XXX_P / _N" as pseudo differential pair trace. (See "PCB Notes")

EVM dev & Test evsl circuitry: A 2nd remote sense location has been routed for TI internal testing only.



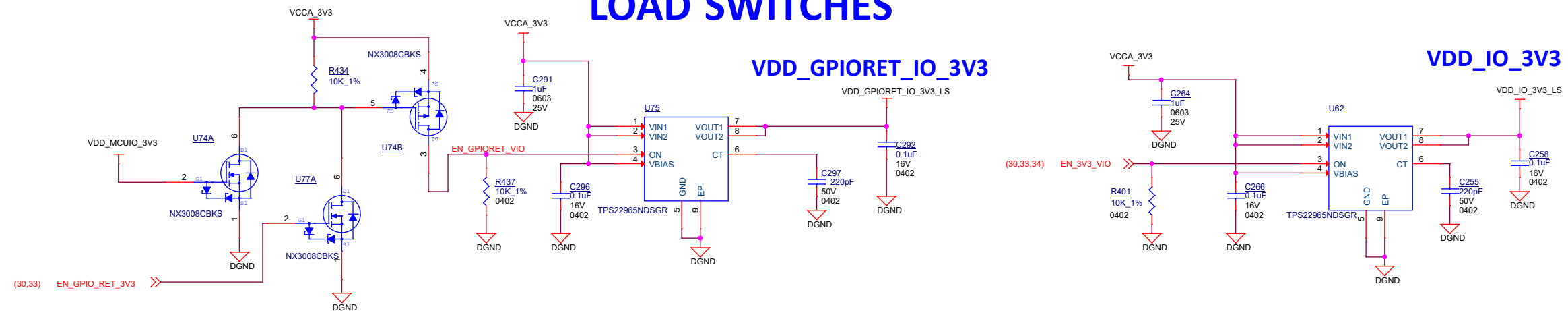
VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)



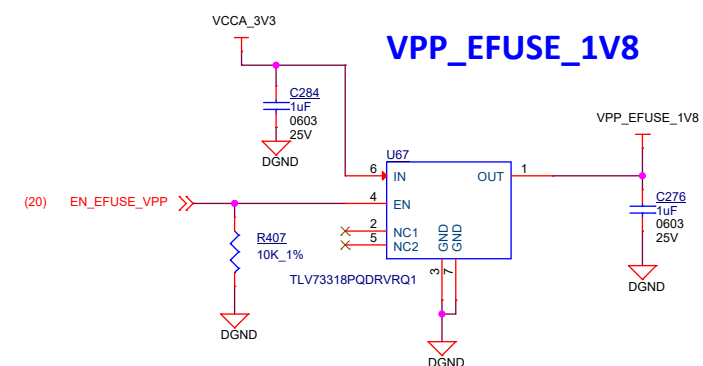
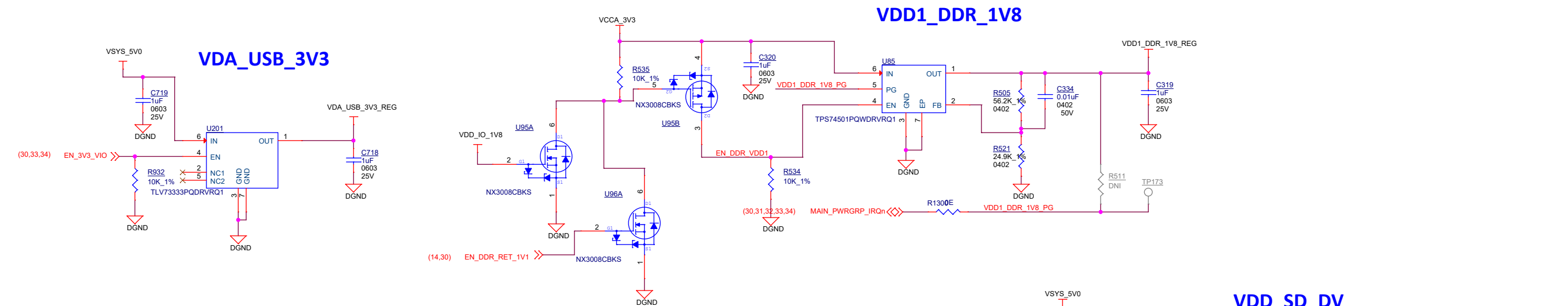
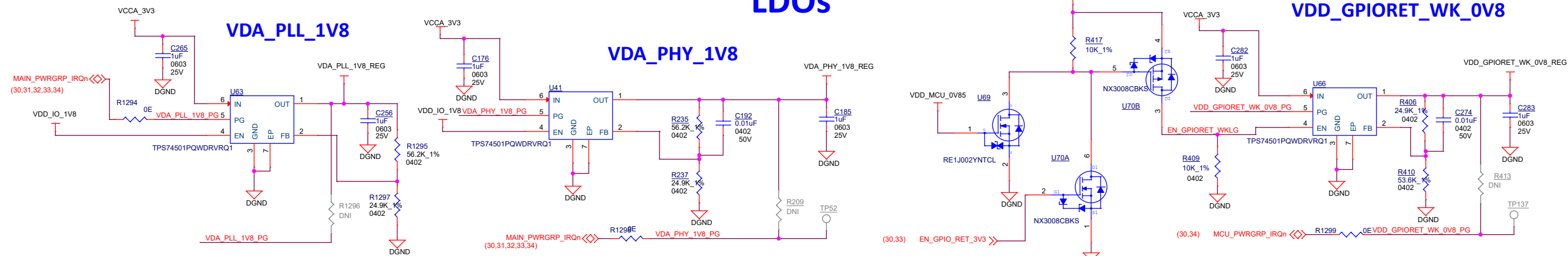
Route remote sense as "VDD_XXX_P / _N"
as pseudo differential pair trace.
(See "PCB Notes")

Note: Keepout needs to be provided for the power and Gnd vias of the feedback pins connecting to the regulator.

LOAD SWITCHES

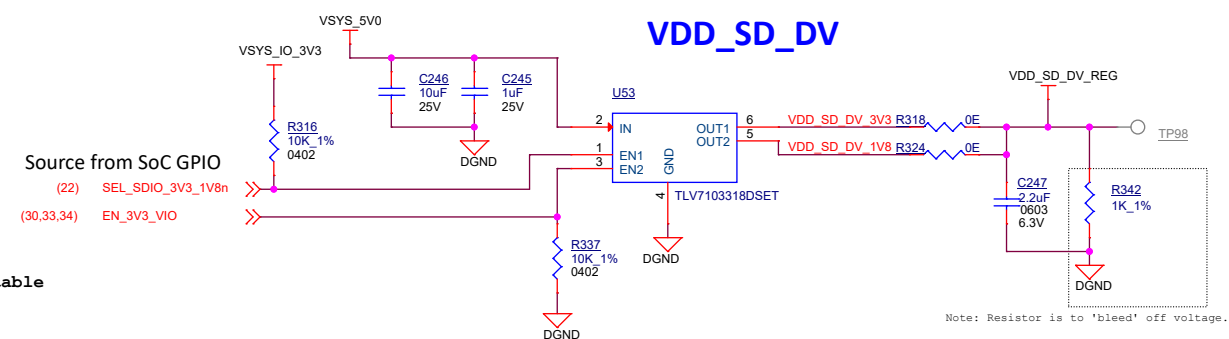


LDOs



EN GPIORET VIO & EN GPIORET WKLG & EN DDR VDD1 Truth table

"OR" Gate Logic			FET States		
X	Y	OUTPUT	Input - X	Input - Y	Output
0	0	0	OFF	OFF	OFF
0	1	1	OFF	ON	ON
1	0	1	ON	OFF	ON
1	1	1	ON	ON	ON



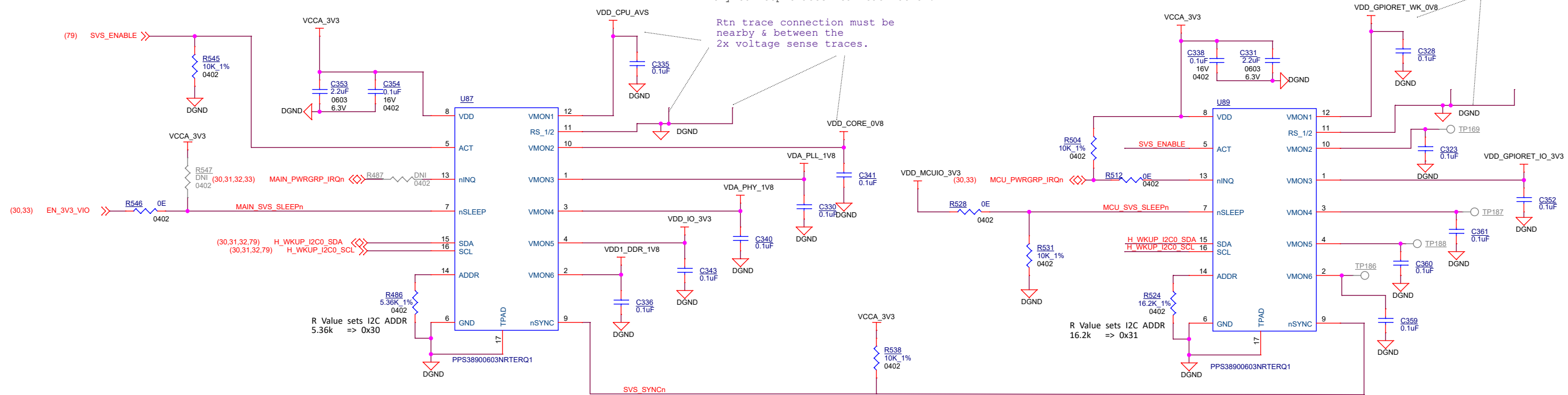
Note: Resistor is to 'bleed' off voltage.

Safety Voltage Supervisors

Power rail voltage > 1.0V can connect to VMON3-6 inputs using single-ended traces.
Trace widths = 4-8mil, as short as possible & try to avoid routing near HF signals.

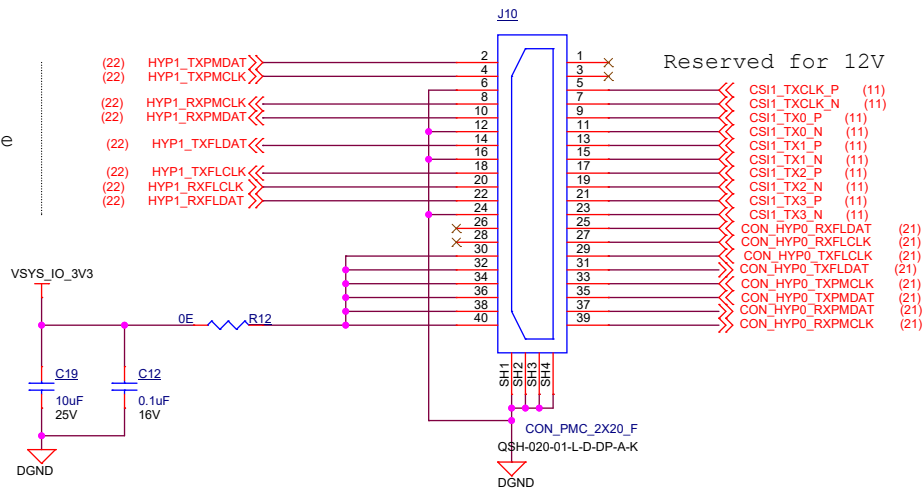
Any power rail voltage < 1.0V should connect to VMON1 & VMON2 inputs using "Pseudo Diff Pair Trace" routes.
Trace widths = 4-8mil & Separation = 8-50mil, try to keep traces near each other.

Rtn trace connection must be nearby & between the 2x voltage sense traces.



HYPERLINK SIDEBAND CONNECTOR

Hyperlink1
Sideband Interface



CSI-TX Interface

Hyperlink0
Sideband Interface

Project :

J7 EVM



Title
HYPERLINK & CSI TX CONNECTOR

Size
C PROC141 001 J784S4XG01EVM

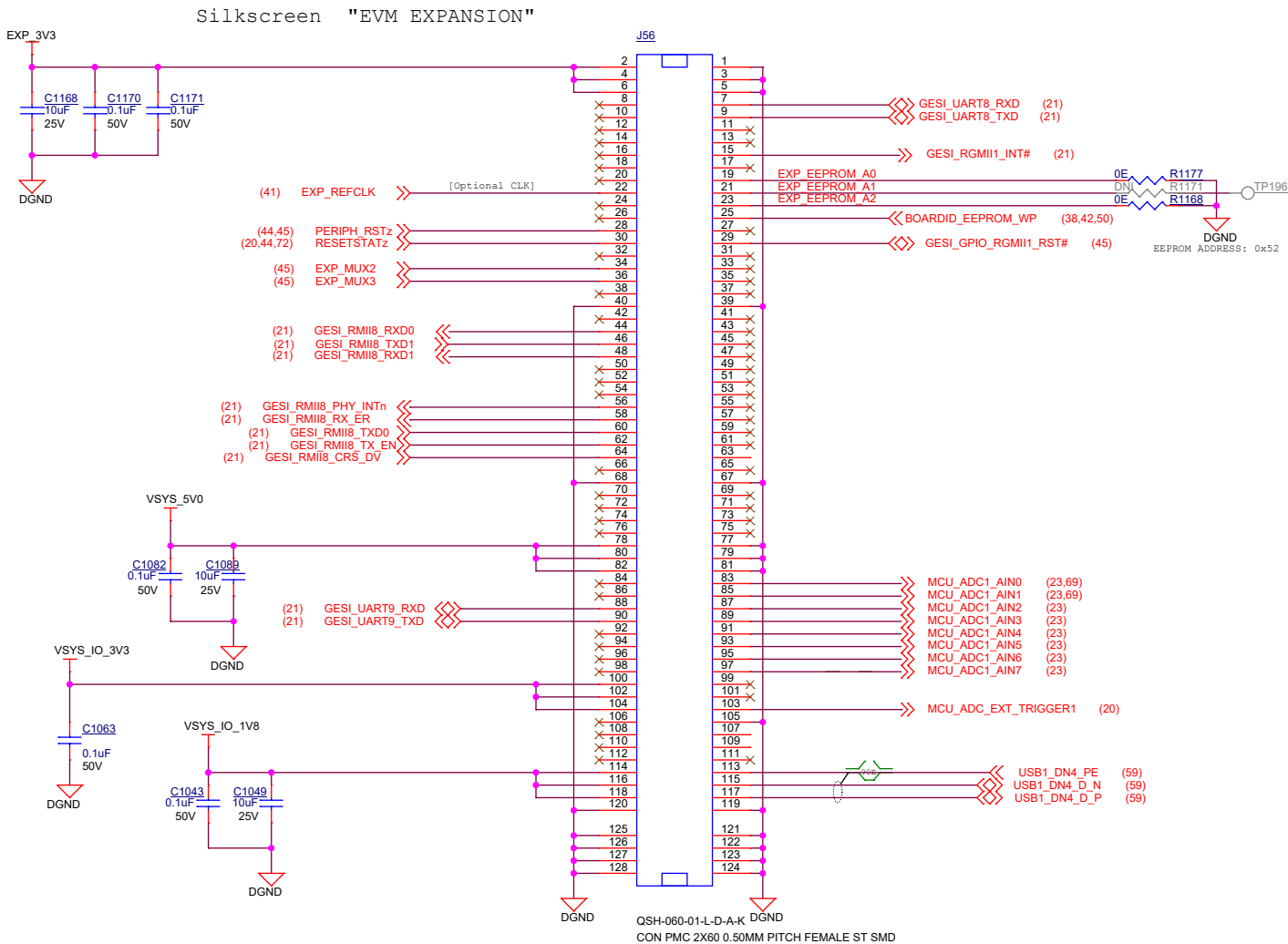
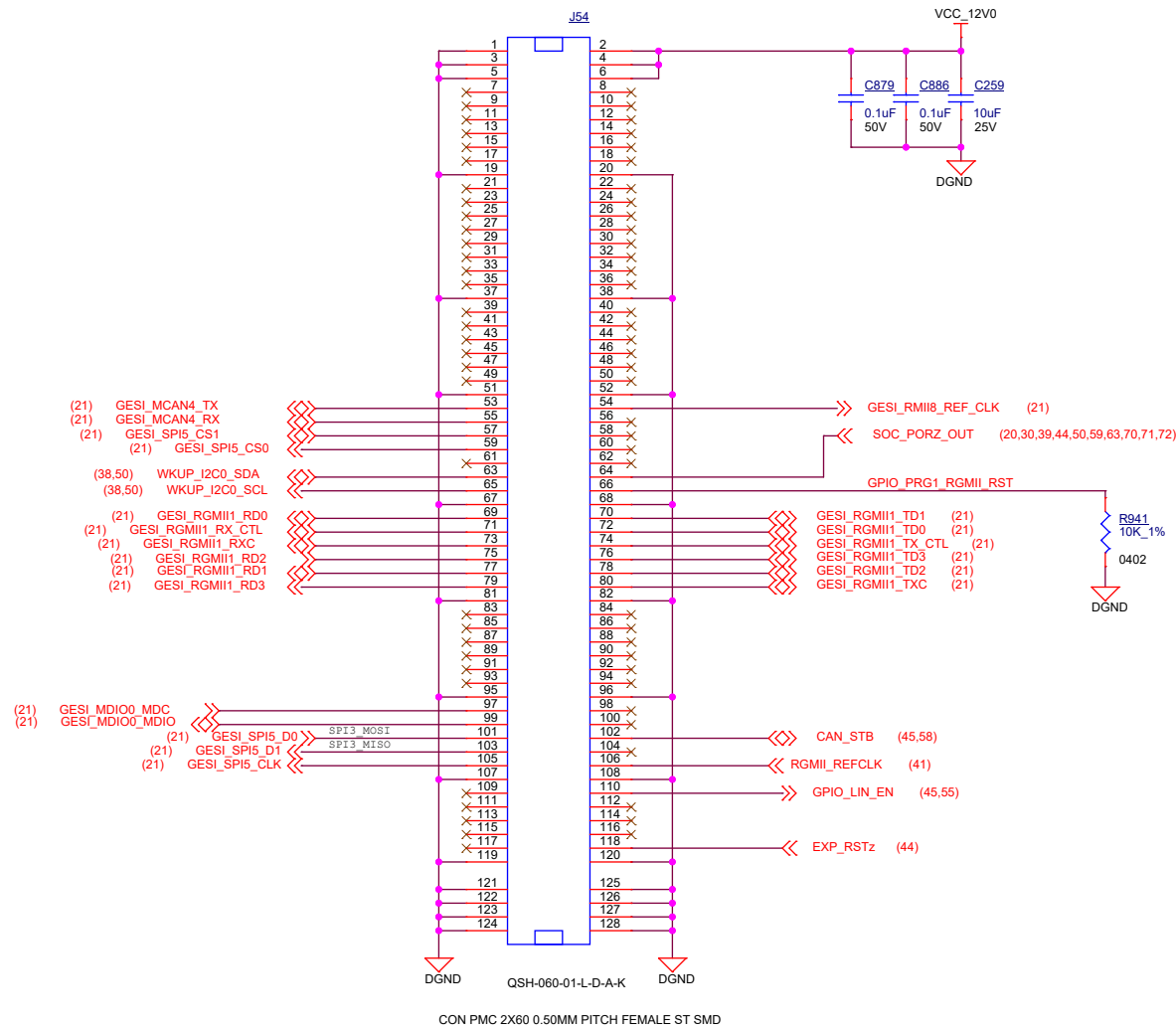
Date: Monday, June 20, 2022

Sheet 35 of 88

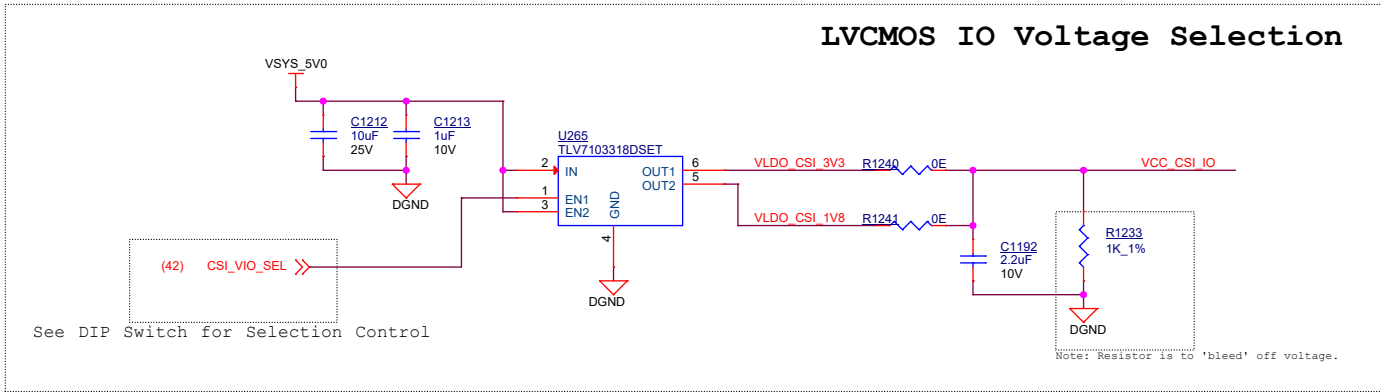
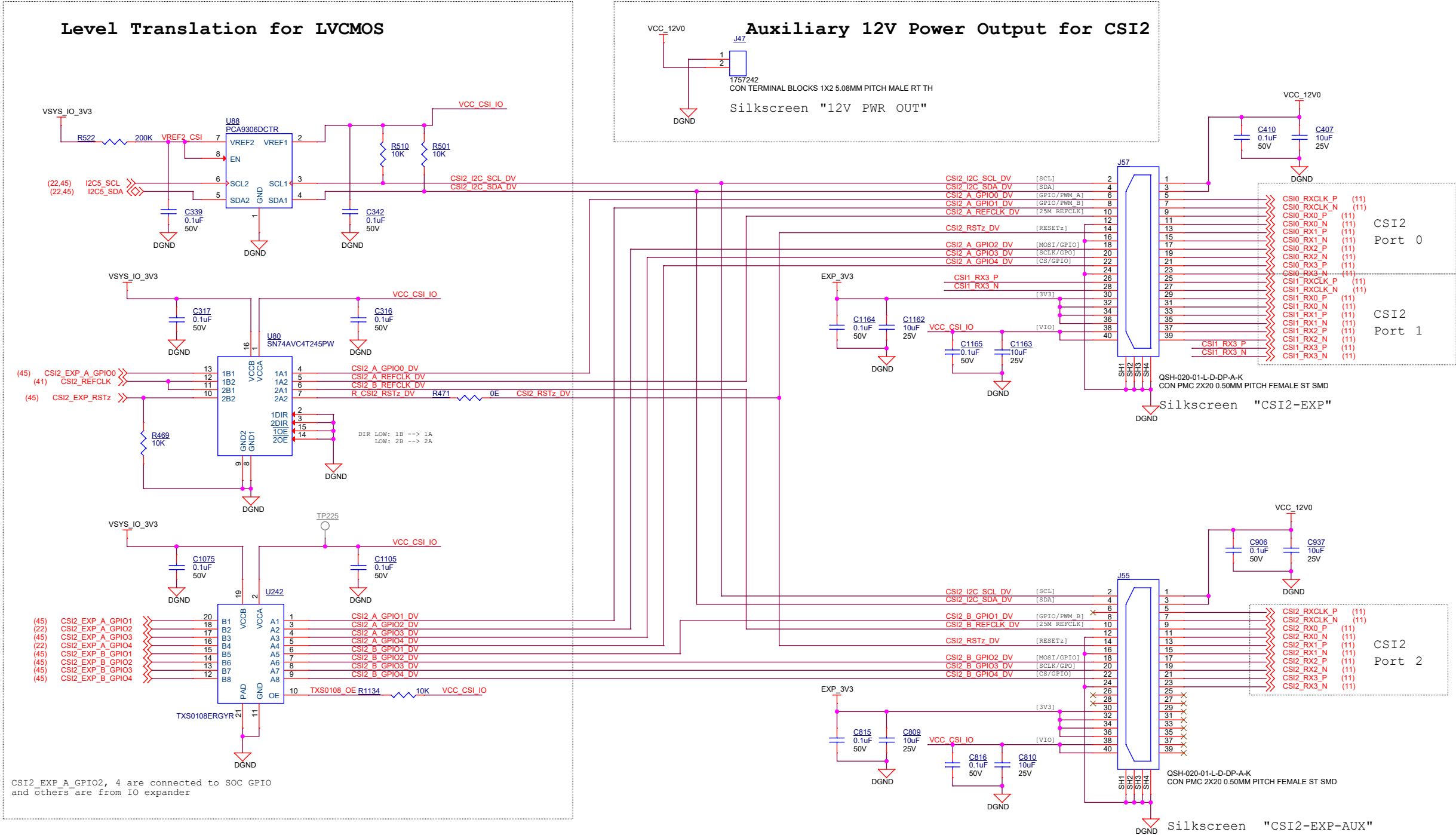
Rev

E2A

GESI_EXP_CONN

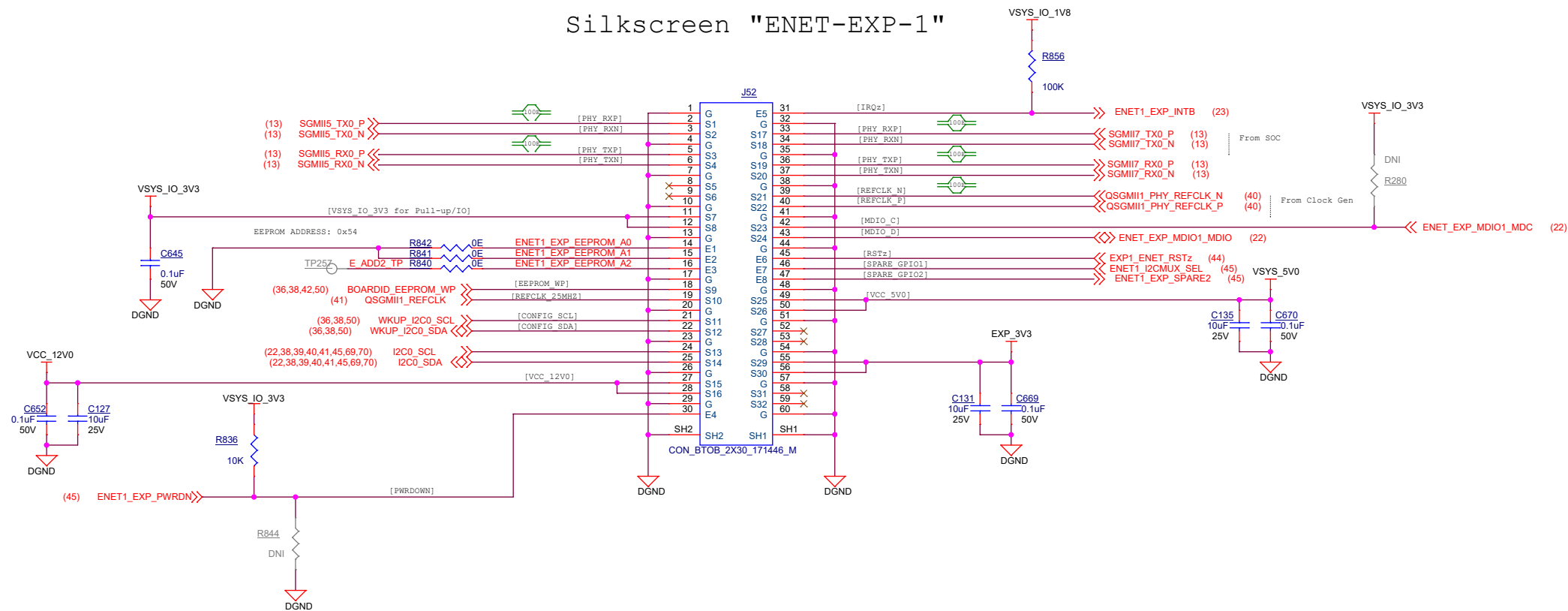


CSI2 EXPANSION CONNECTORS

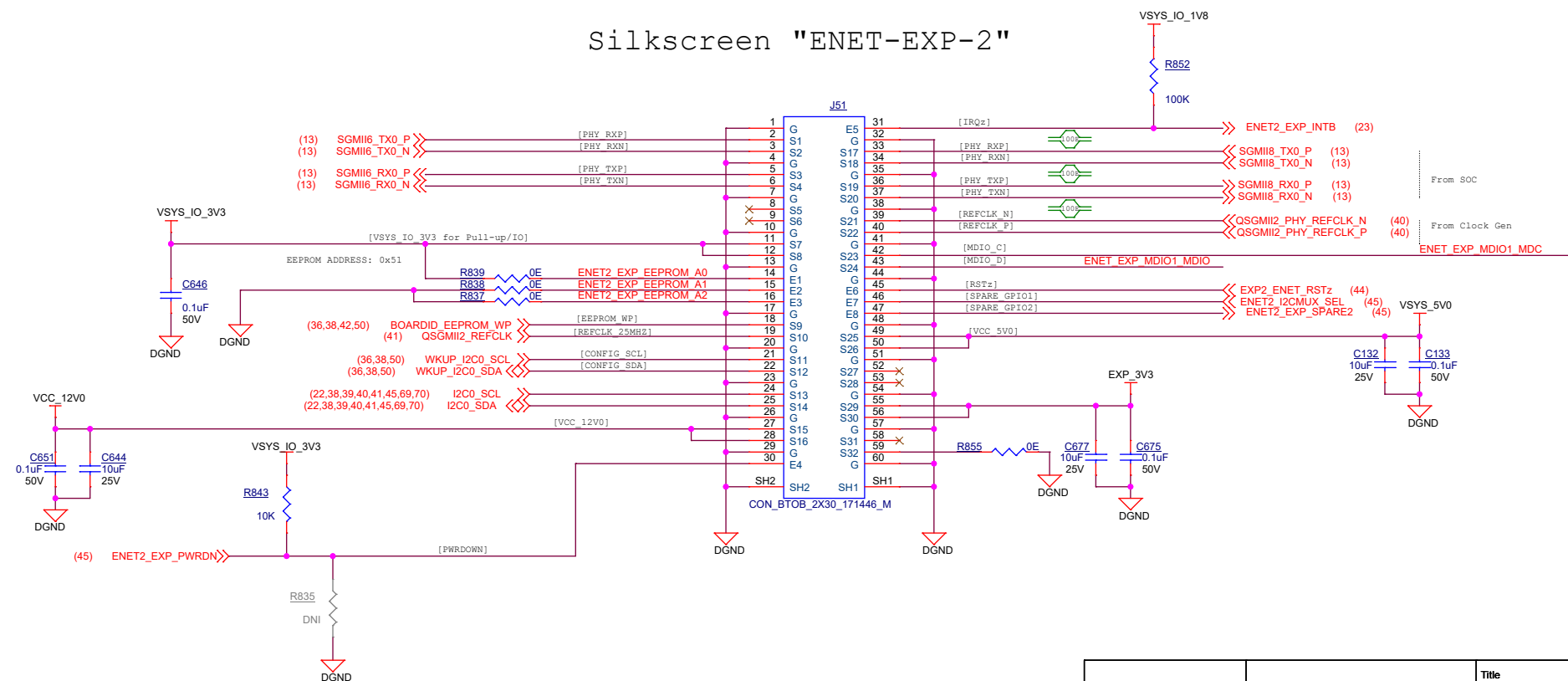


ENET EXPANSION CONNECTOR

Silkscreen "ENET-EXP-1"



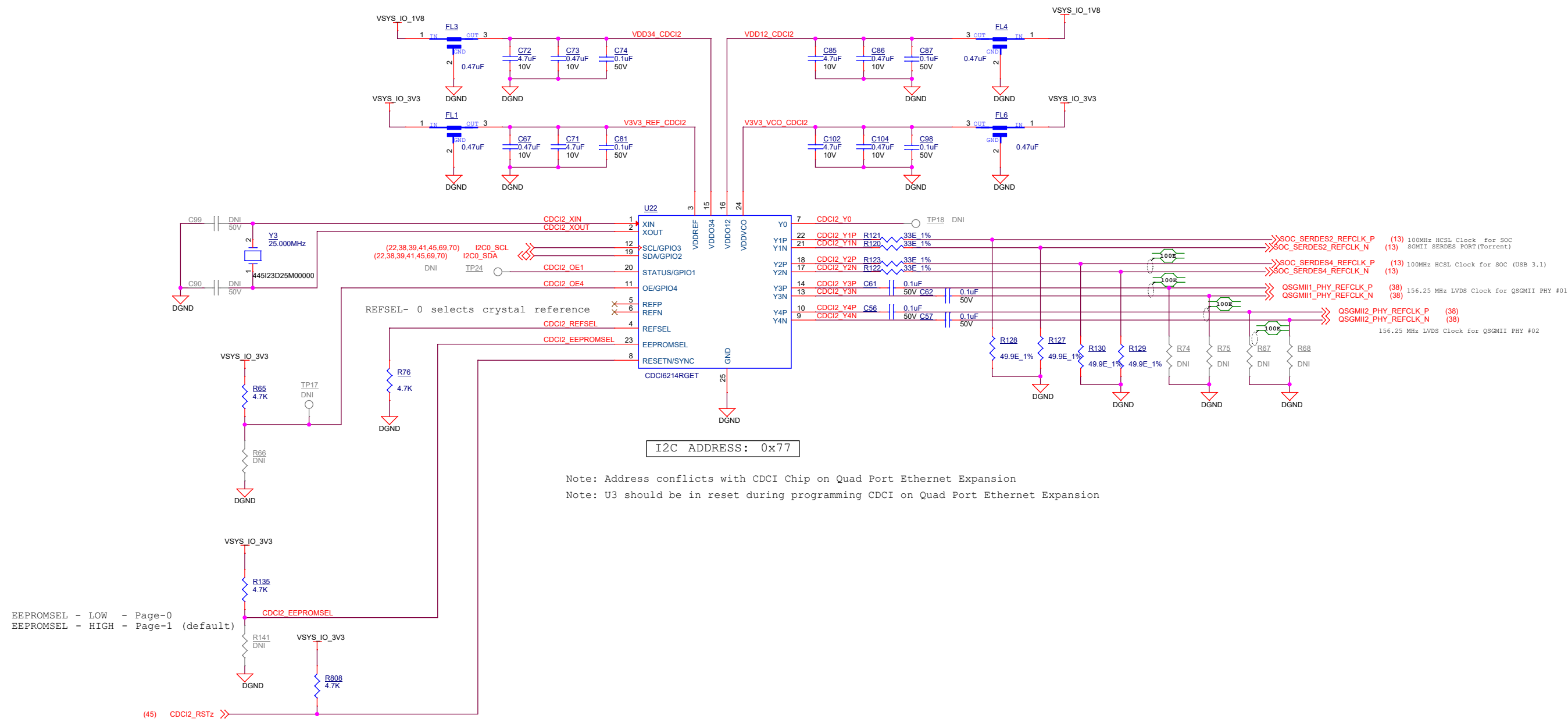
Silkscreen "ENET-EXP-2"



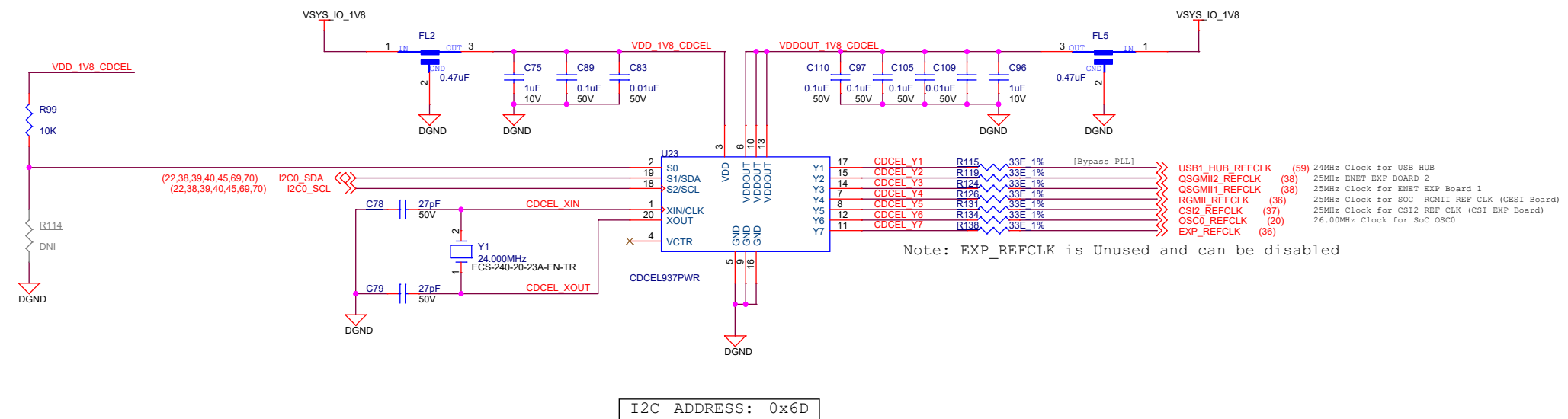
A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B contains a right-pointing arrow.



SERDES CLOCK GENERATOR #2

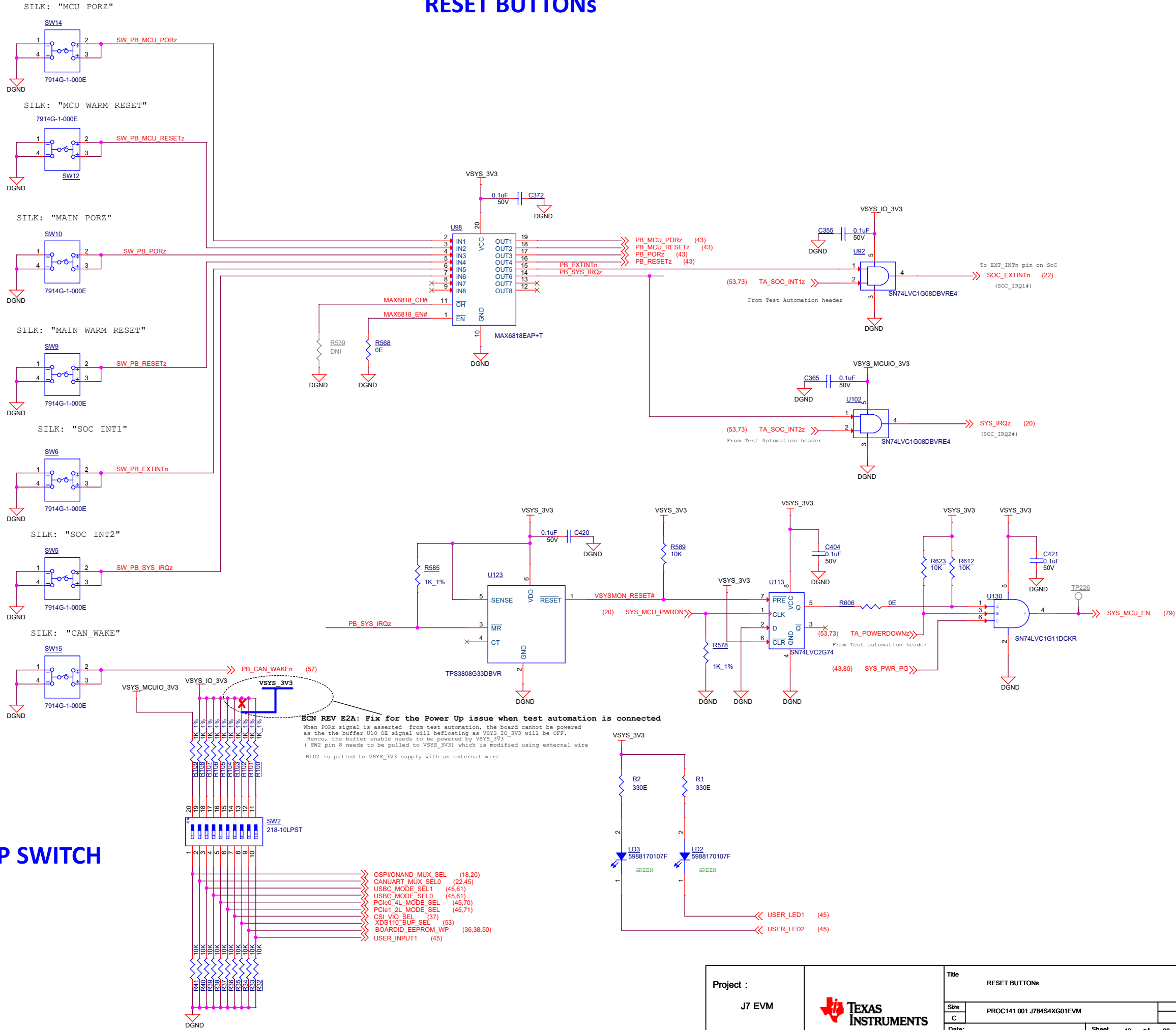


PERIPHERAL CLOCK GENERATOR



RESET BUTTONs

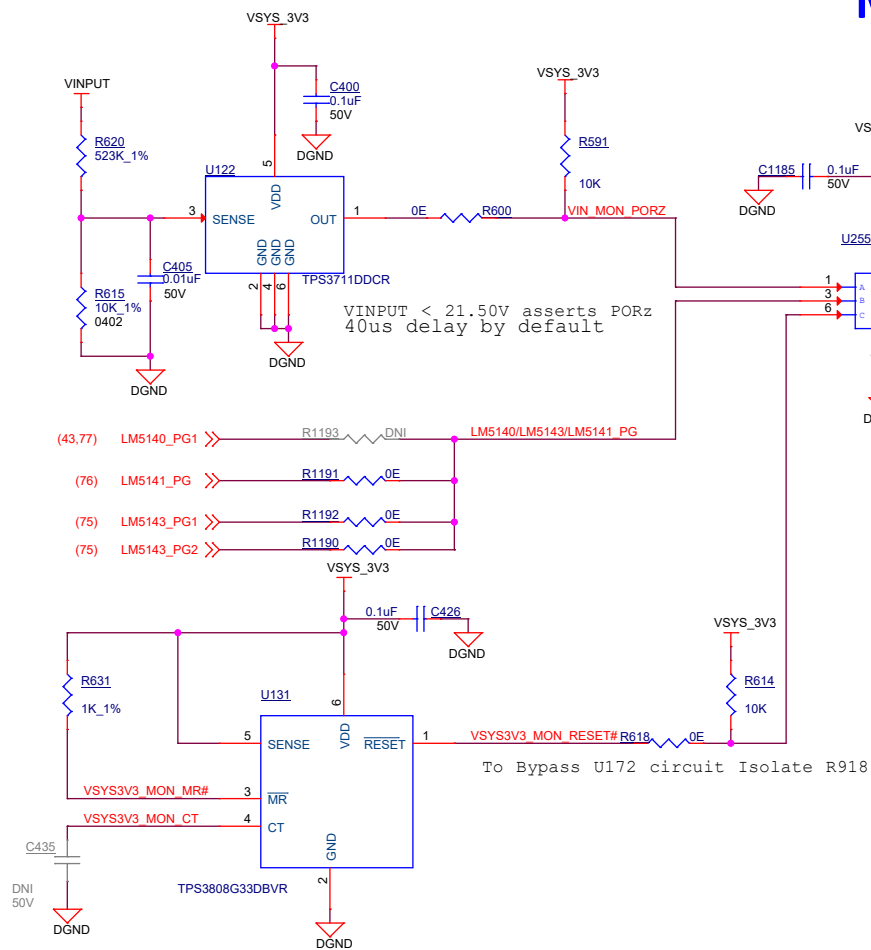
CONFIG DIP SWITCH



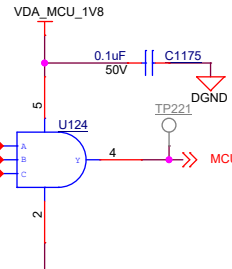
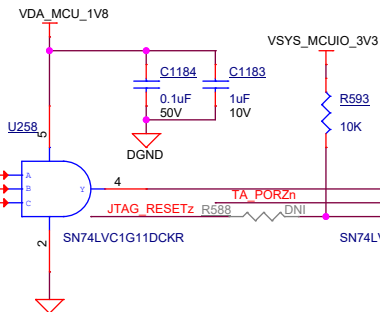
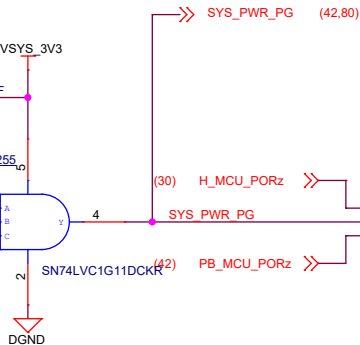
ECN REV E2A: Fix for the Power Up issue when test automation is connected
When PORz signal is asserted from test automation, the board cannot be powered as the the buffer U10 OE signal will be floating as VSYS_IO_3V3 will be OFF. Hence, the buffer enable needs to be powered by VSYS_3V3 (SW2 pin 8 needs to be pulled to VSYS_3V3) which is modified using external wire R102 is pulled to VSYS_3V3 supply with an external wire

RESET INPUTS

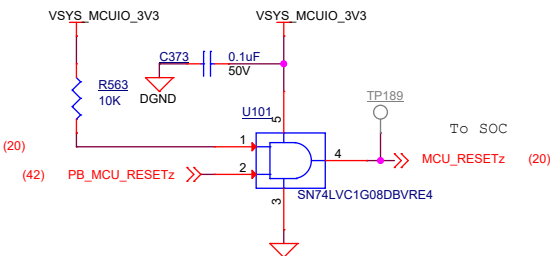
Under Voltage Monitor (VINPUT)



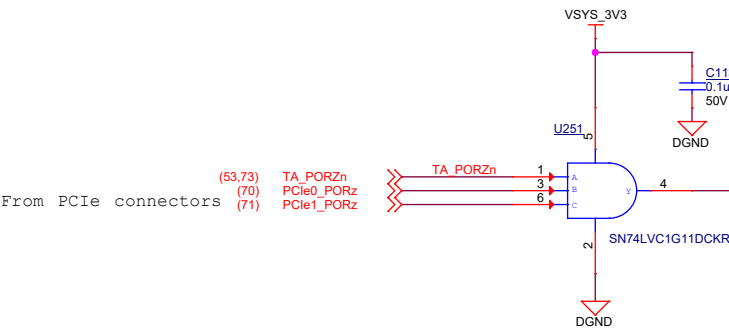
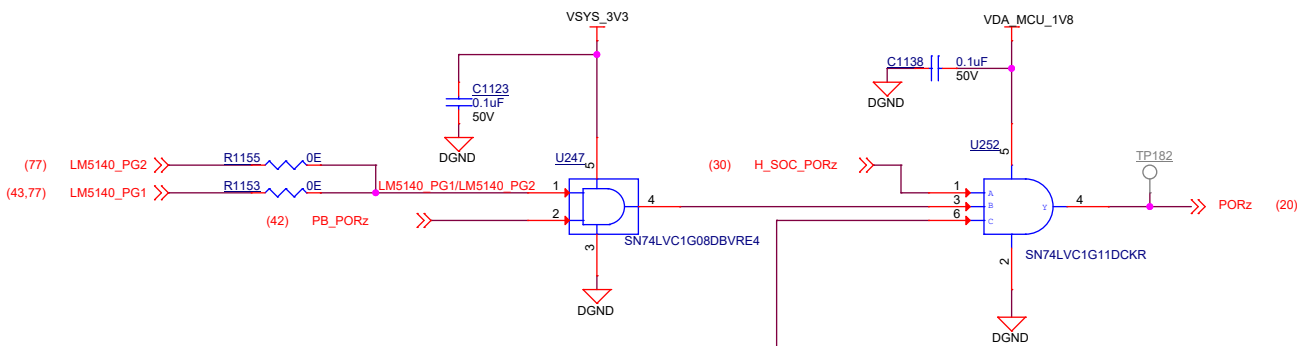
MCU PORz



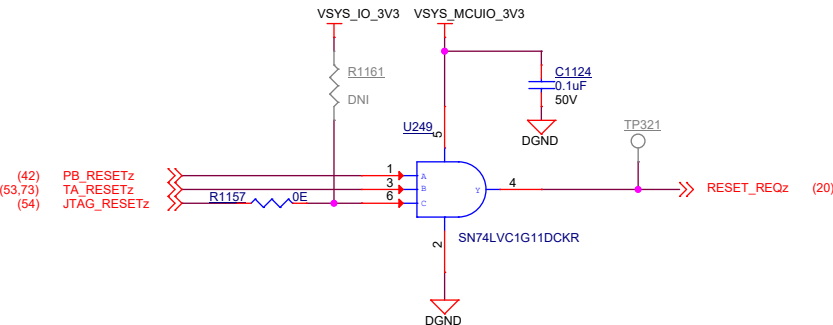
MCU_RESET



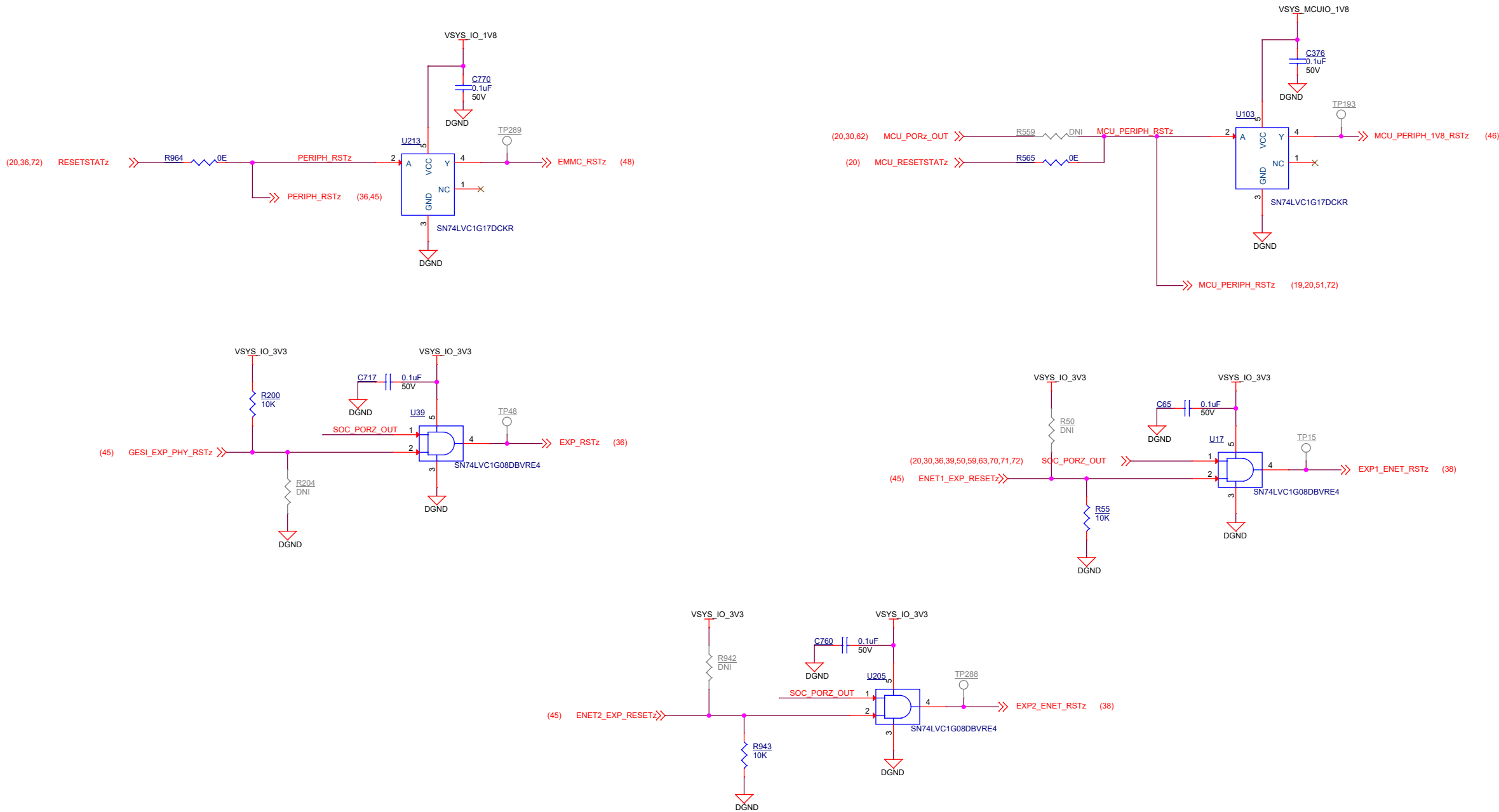
SOC PORz



SOC RESET

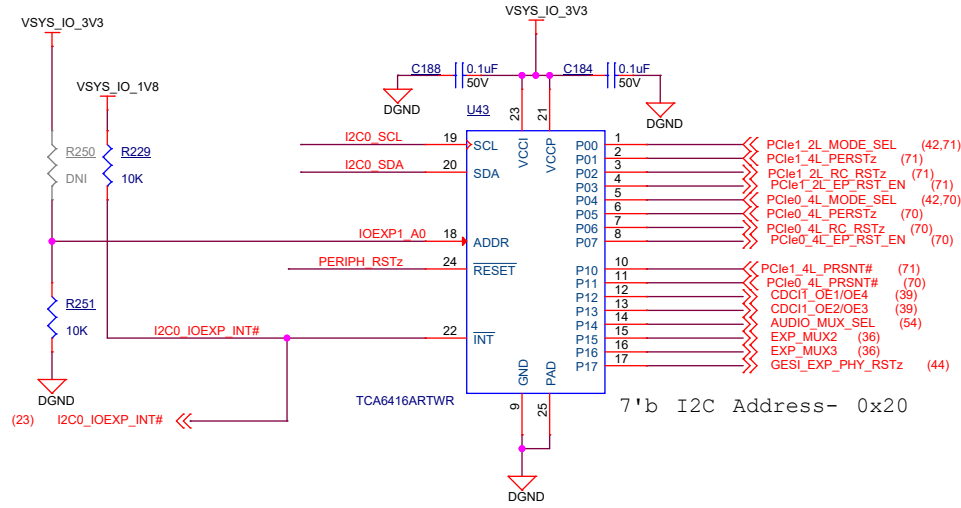


RESET OUTPUTS

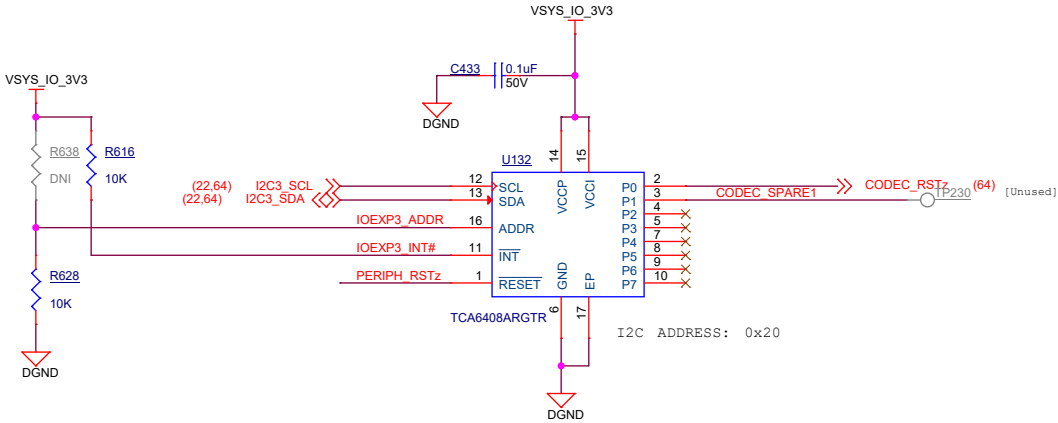


GPIO EXPANDERS

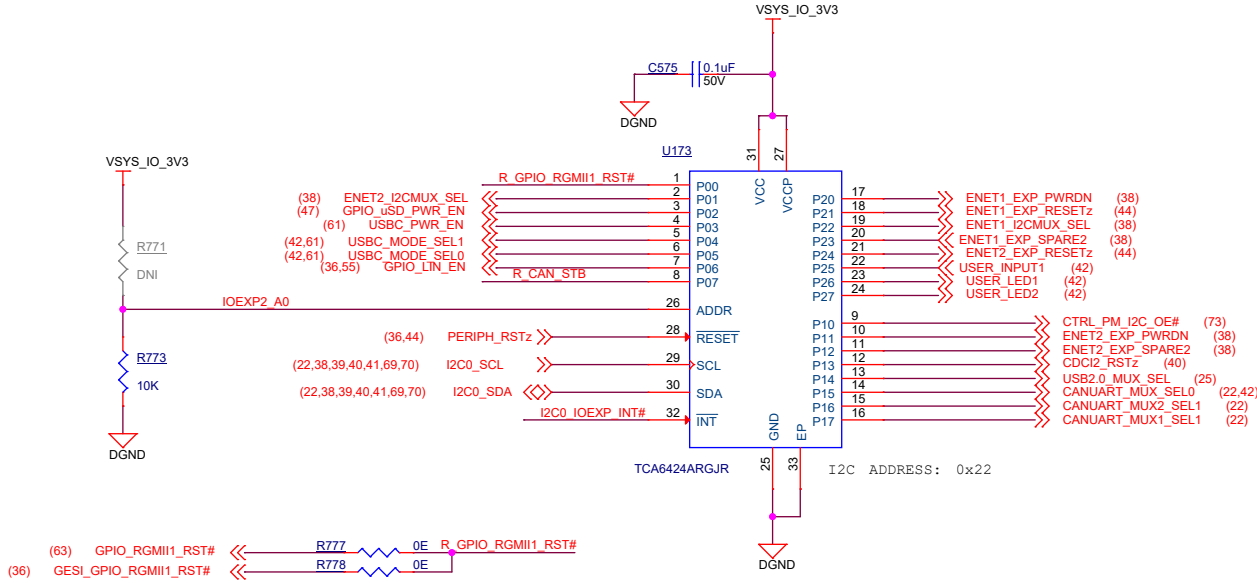
I2C GPIO EXPANDER1



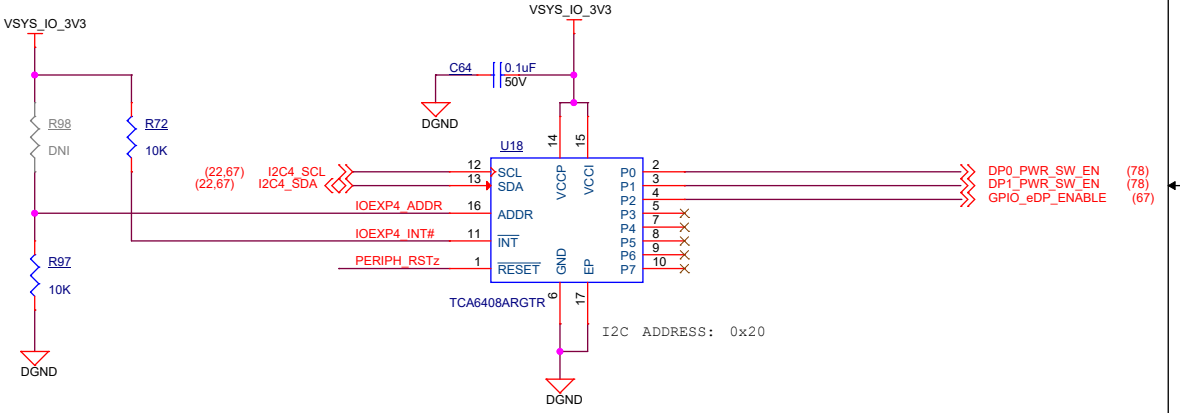
I2C GPIO EXPANDER3



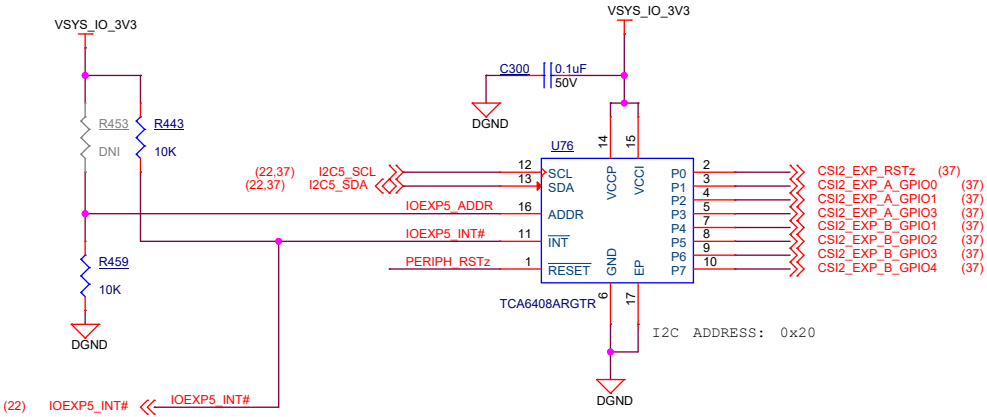
I2C GPIO EXPANDER2



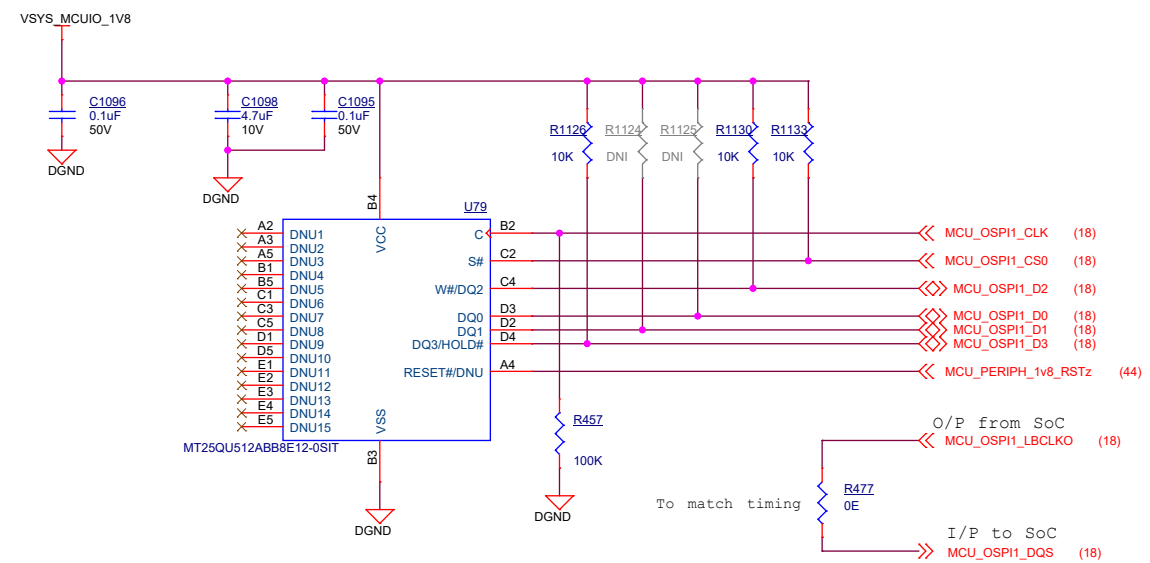
I2C GPIO EXPANDER4



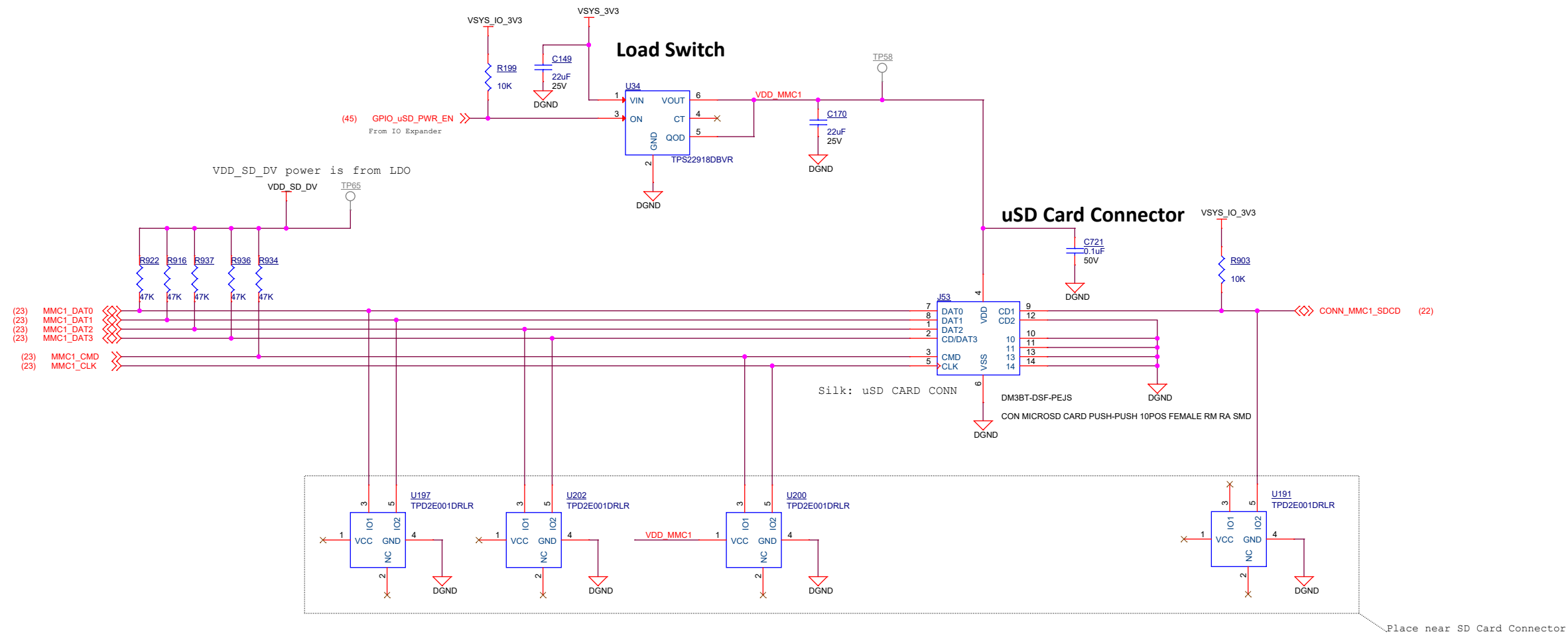
I2C GPIO EXPANDERS



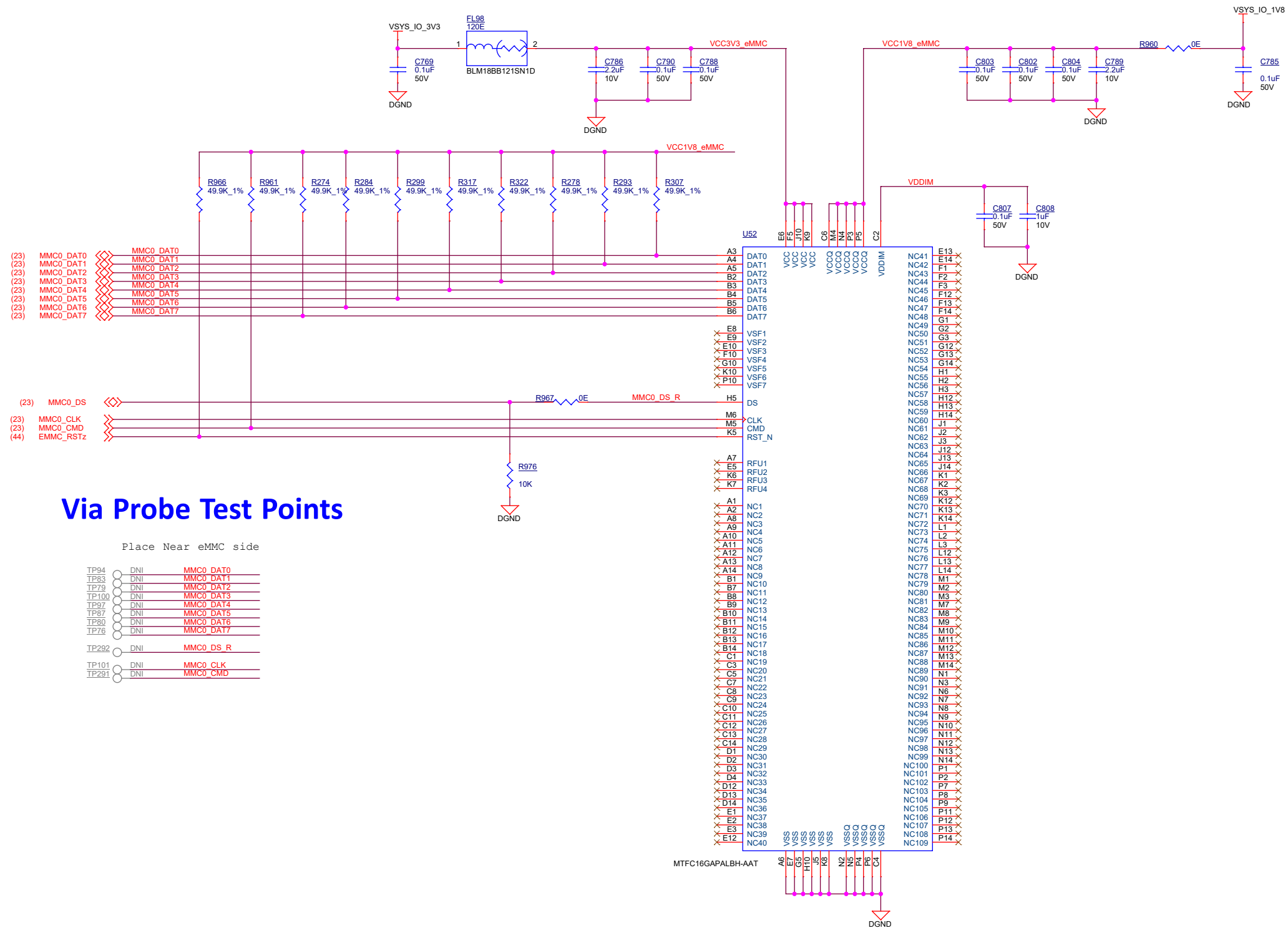
SPI NOR Flash



Micro SD CARD INTERFACE



eMMC FLASH

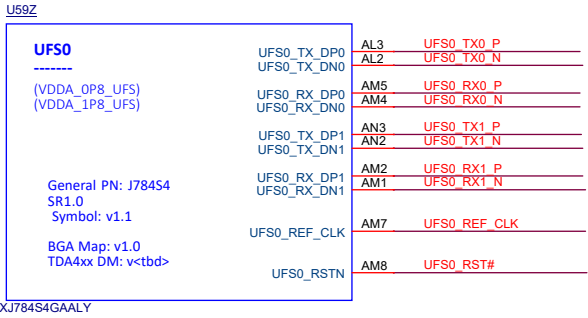


Via Probe Test Points

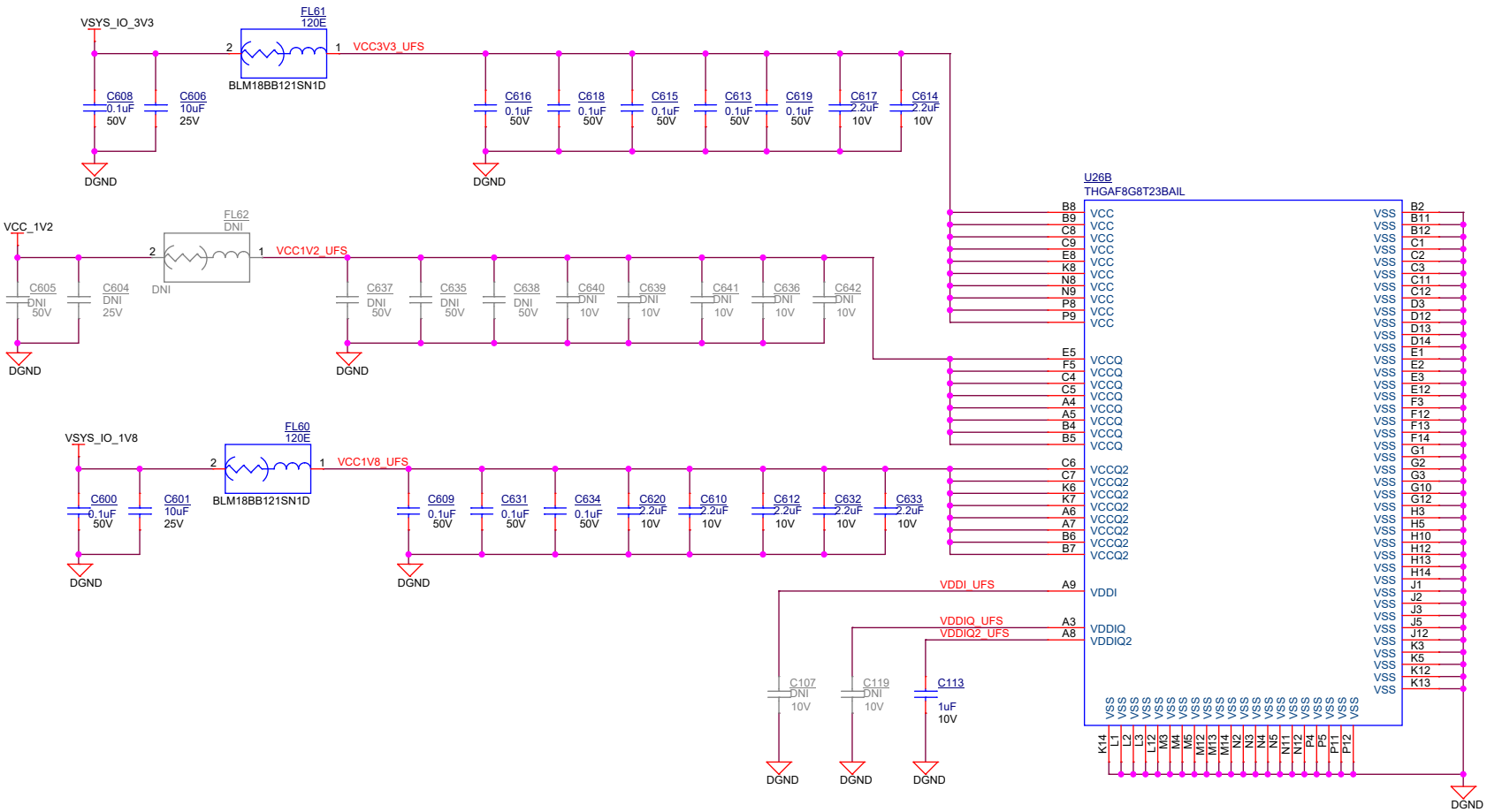
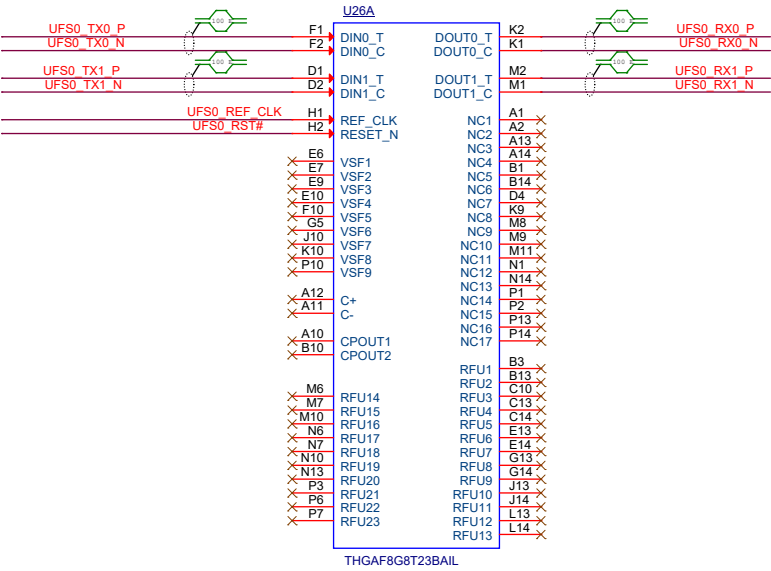
Place Near eMMC side

TP94	DNI	MMC0_DAT0
TP83	DNI	MMC0_DAT1
TP79	DNI	MMC0_DAT2
TP100	DNI	MMC0_DAT3
TP97	DNI	MMC0_DAT4
TP87	DNI	MMC0_DAT5
TP80	DNI	MMC0_DAT6
TP76	DNI	MMC0_DAT7
TP292	DNI	MMC0_DS_R
TP101	DNI	MMC0_CLK
TP291	DNI	MMC0_CMD

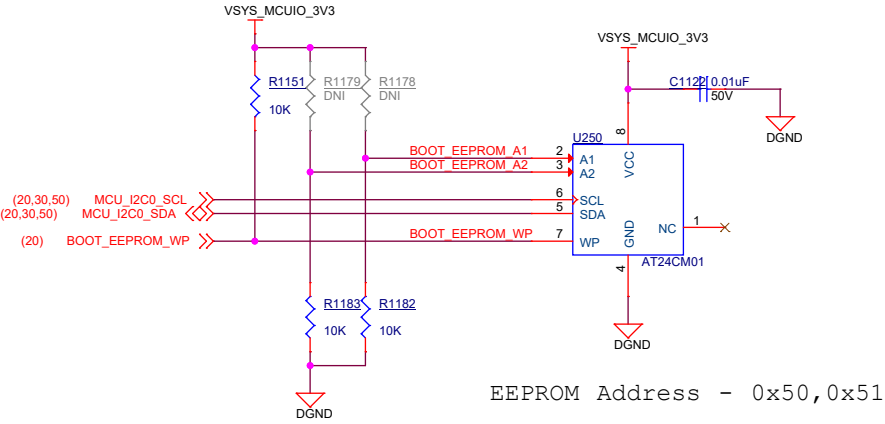
UFS FLASH



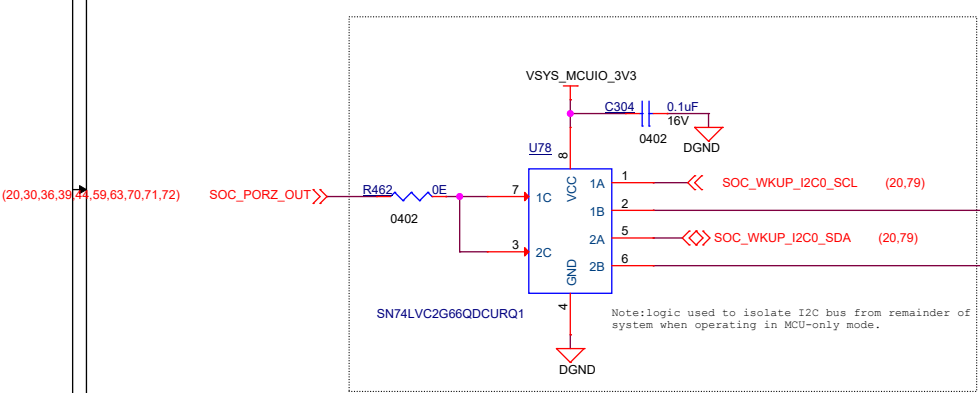
XJ784S4GAALY



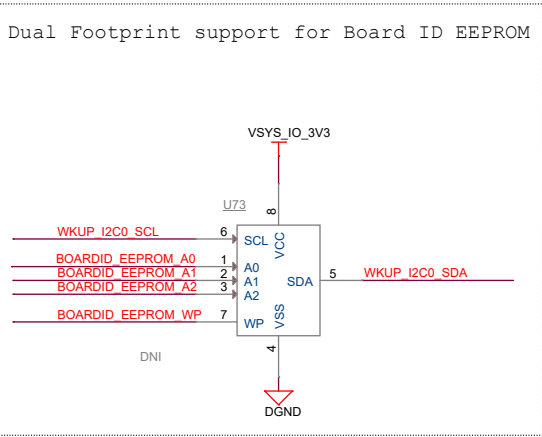
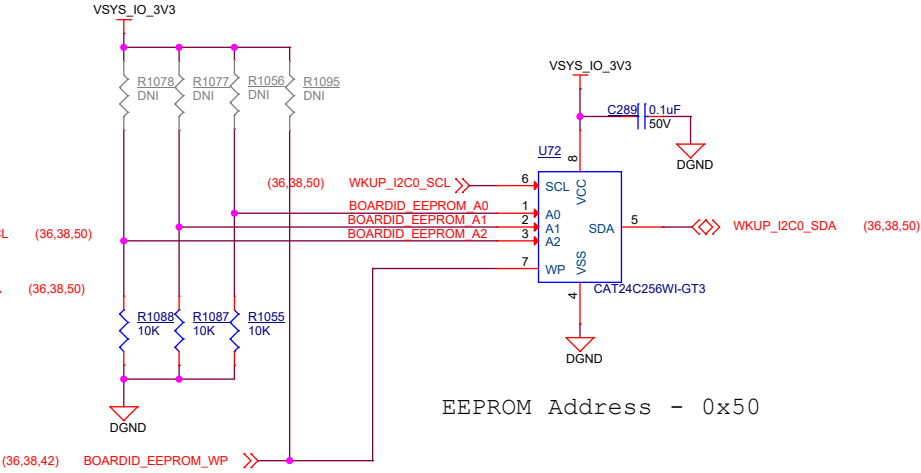
BOOT EEPROM



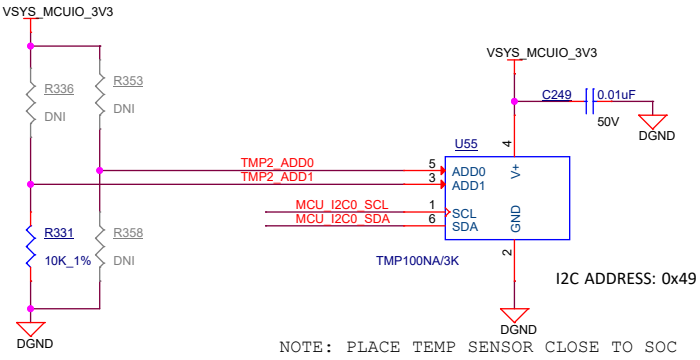
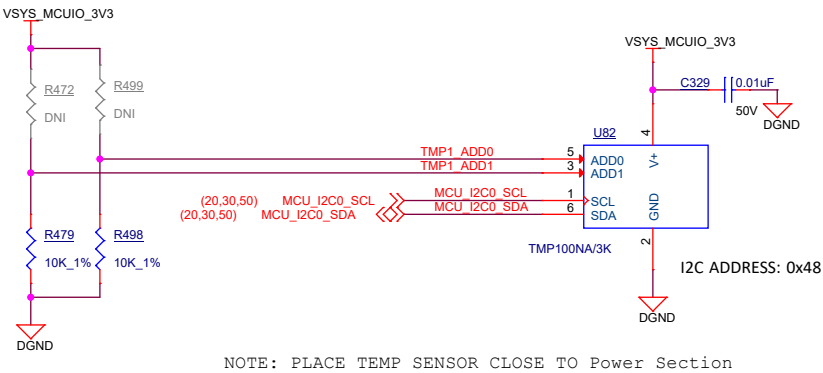
I2C for BOARD ID EEPROMs



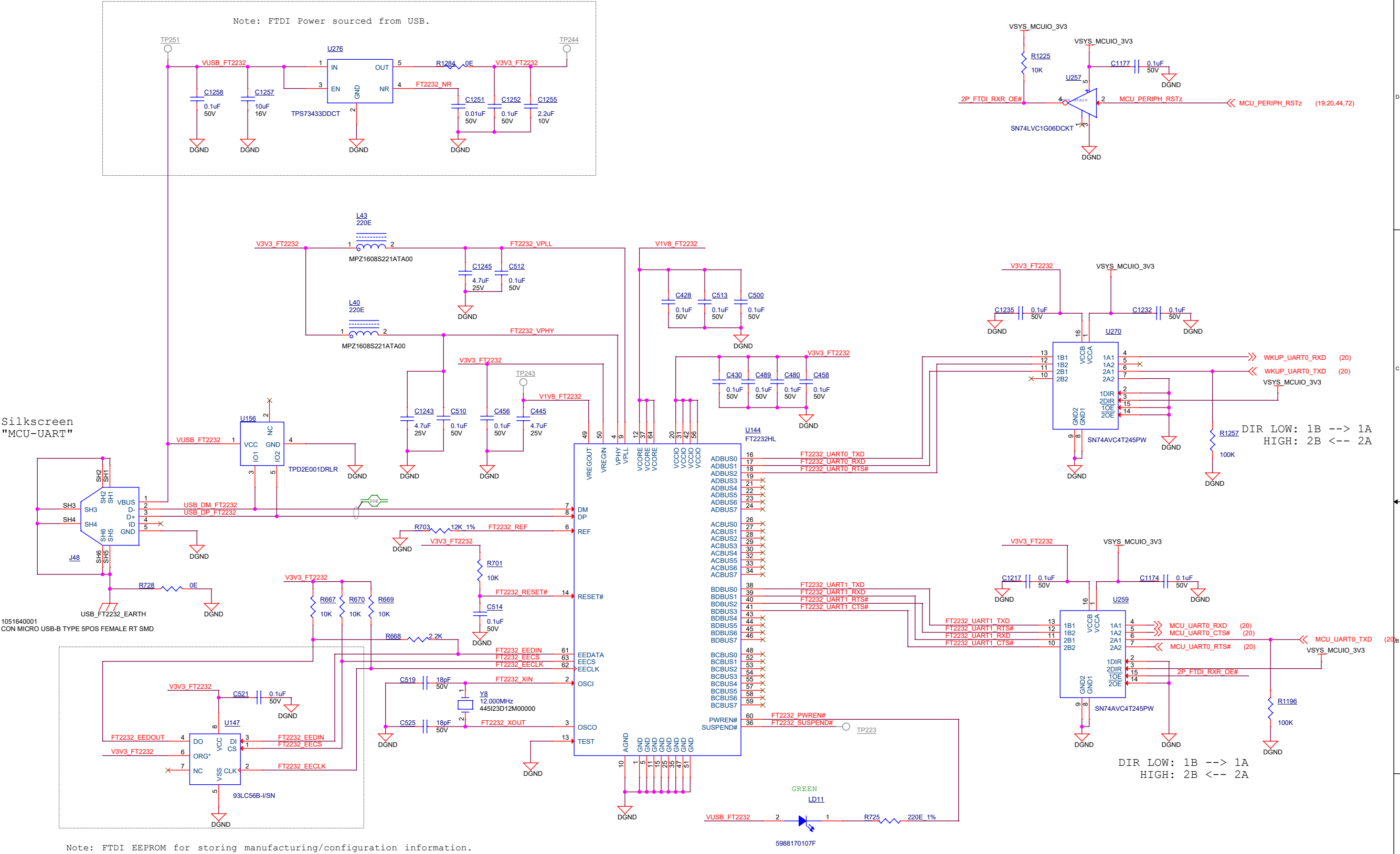
BOARD ID EEPROM



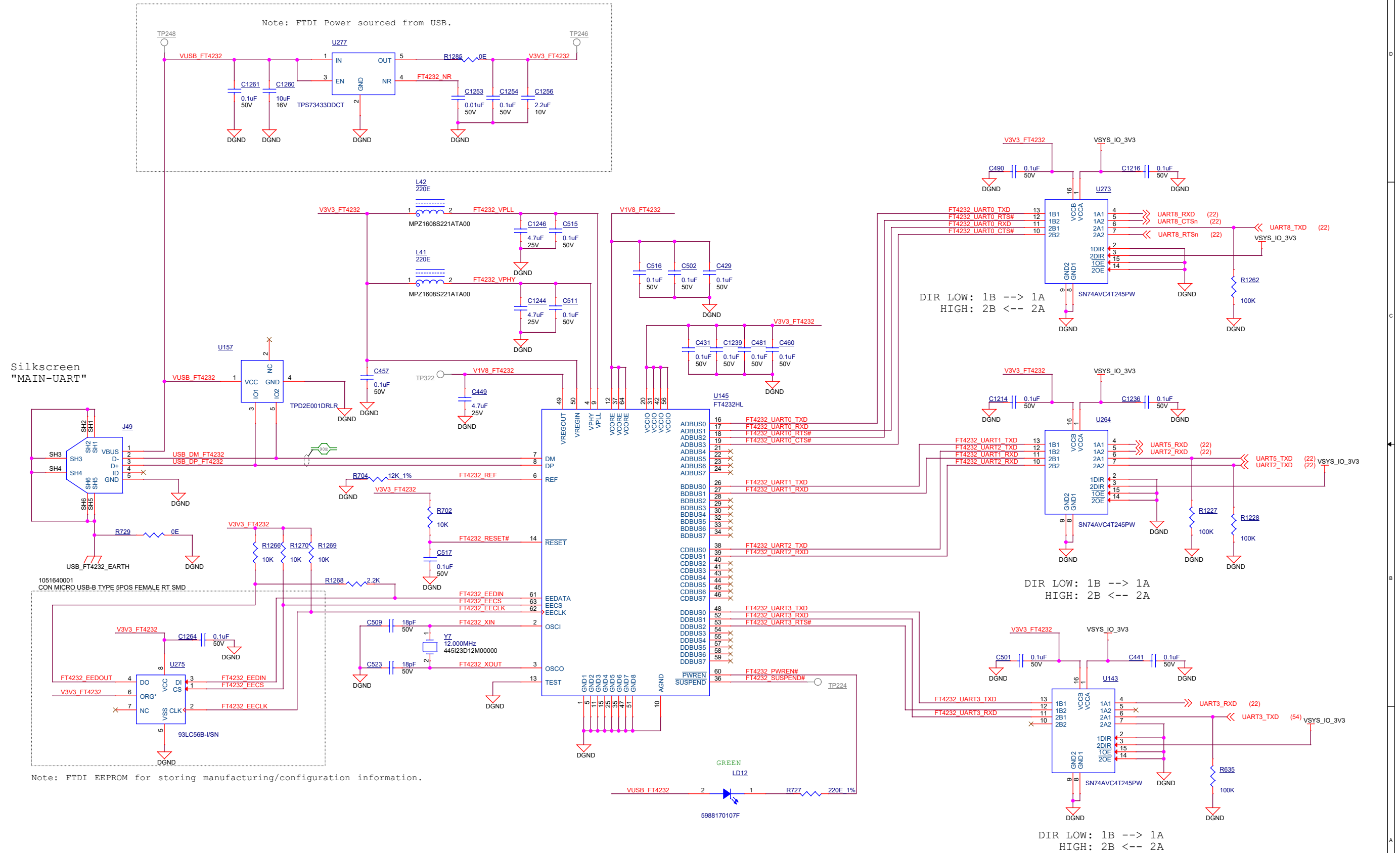
TEMPERATURE SENSORS (TI EVM Only)



DUAL PORT FTDI



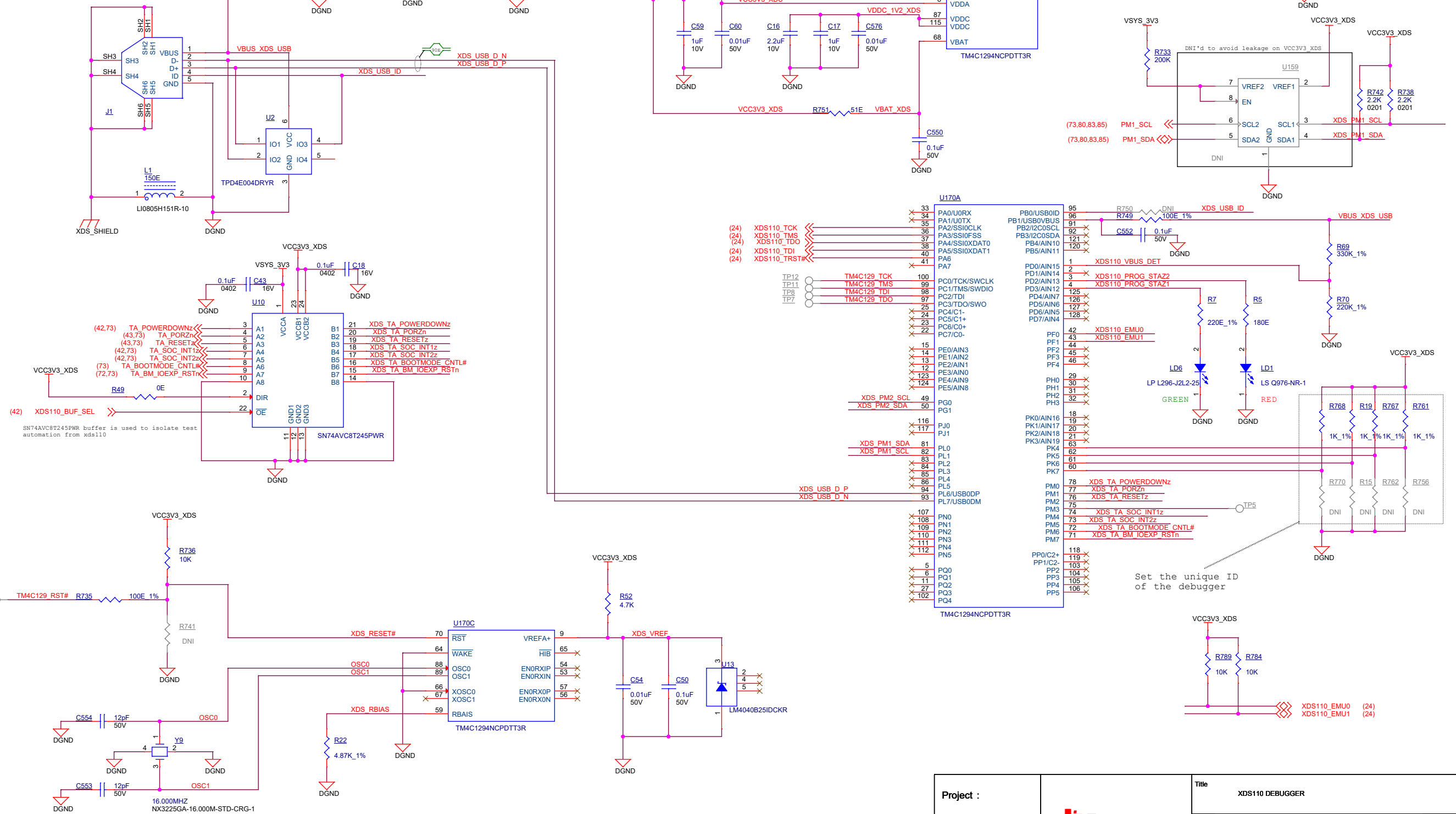
QUAD PORT FTDI



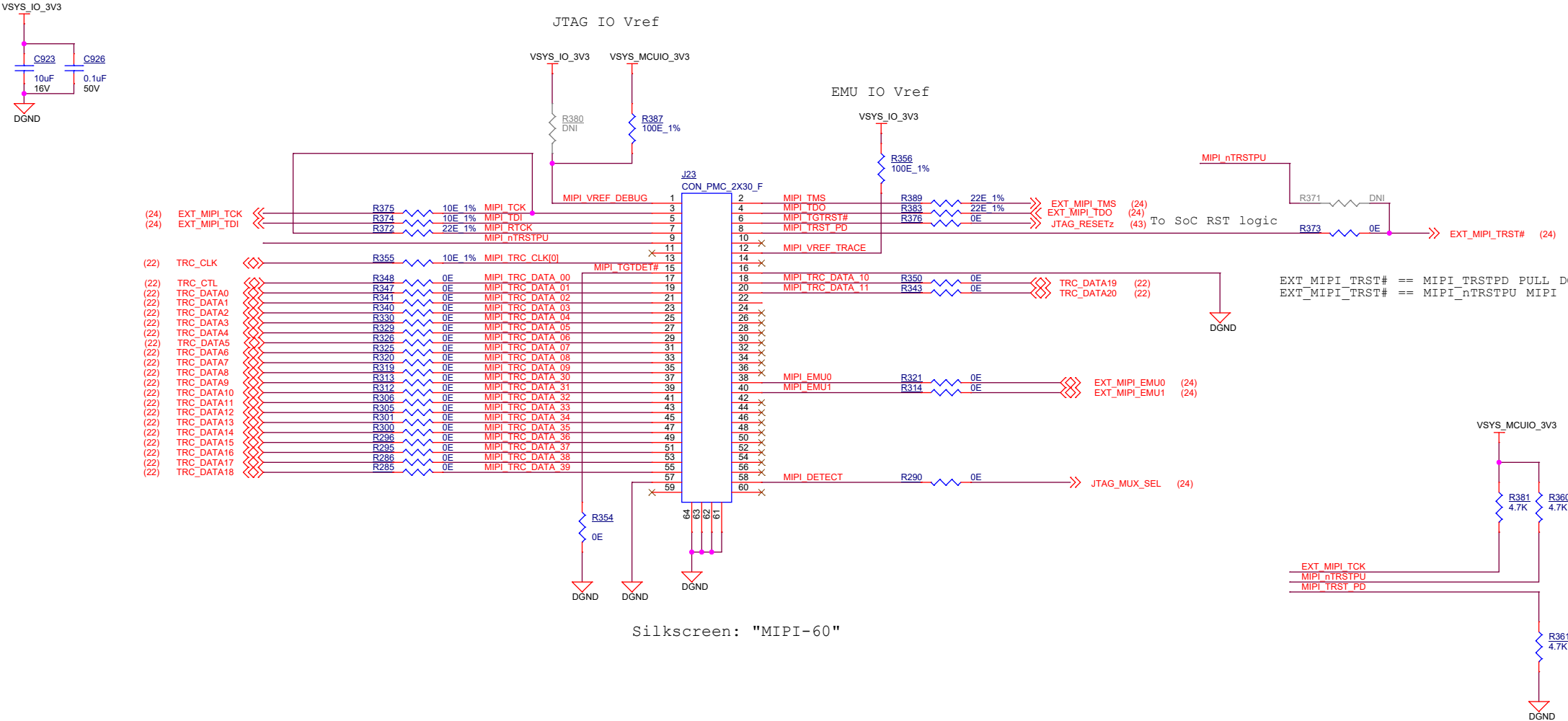
XDS110 DEBUGGER

Silkscreen "XDS110"

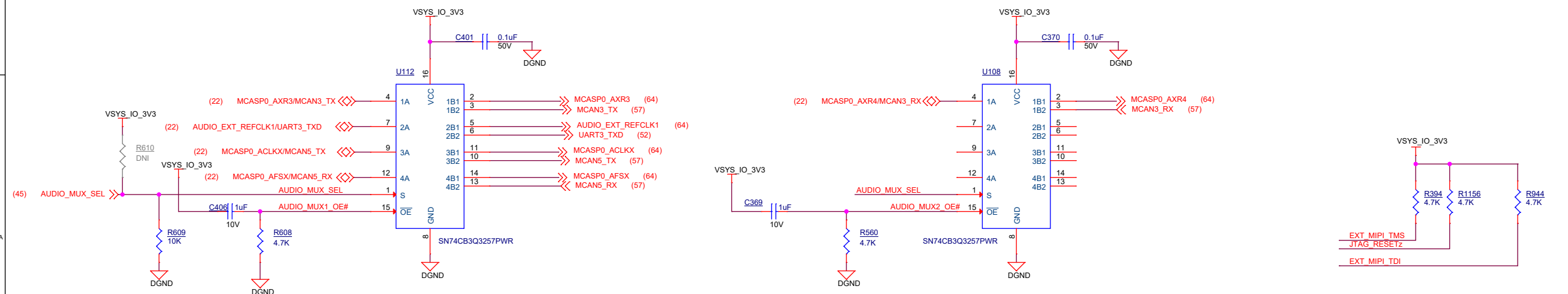
1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD



JTAG MIPI60 CONNECTOR



```
Silkscreen: "MIPI-60
```



JTAG - 1:2 MUX : Truth Table

Project

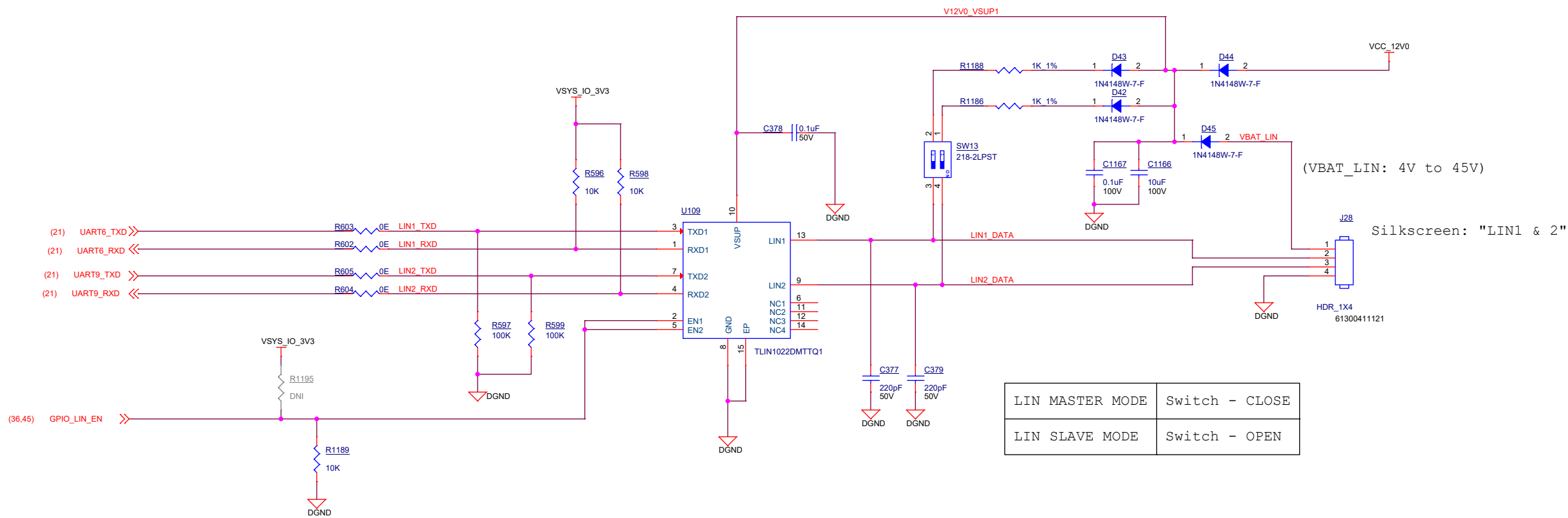
J7 EVI



JTAG MIPI60 CONNECTOR

Size	PROC141 001 J784S4XG01EVM	
C		
Date:	Monday, June 29, 2022	Sheet 54 of 88

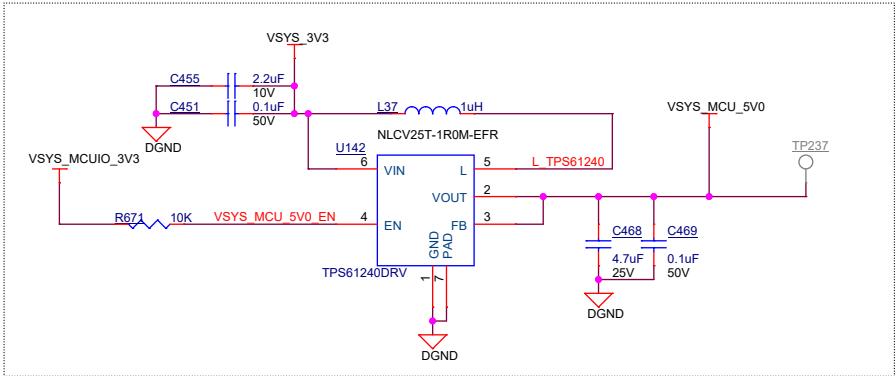
LIN INTERFACE



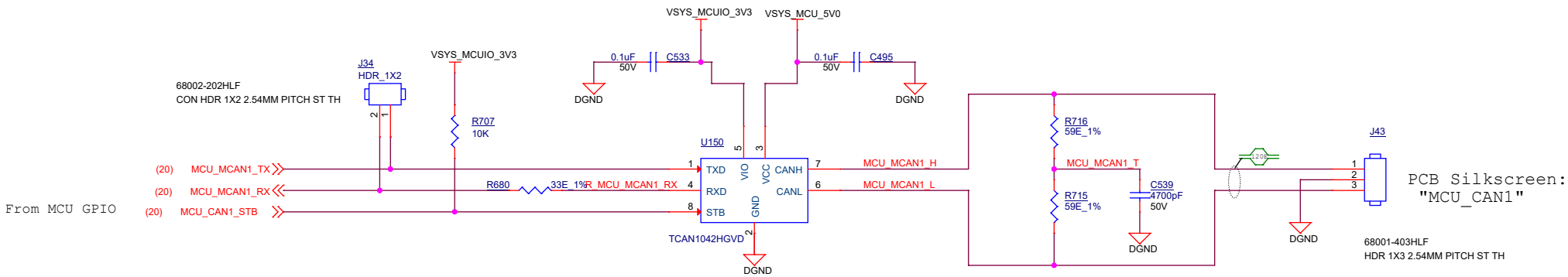
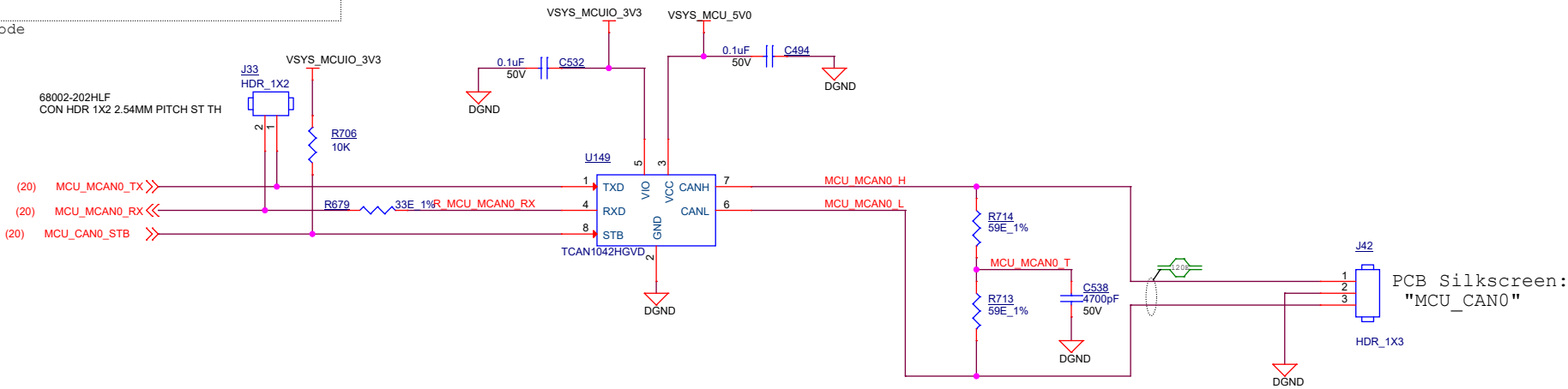
LIN MASTER MODE	Switch - CLOSE
LIN SLAVE MODE	Switch - OPEN

CAN TRANSCEIVERS #1-MCU DOMAIN

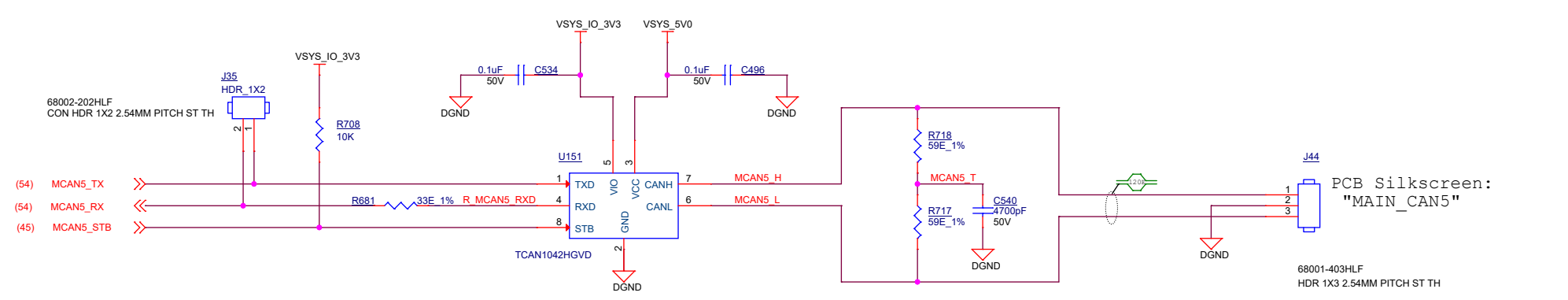
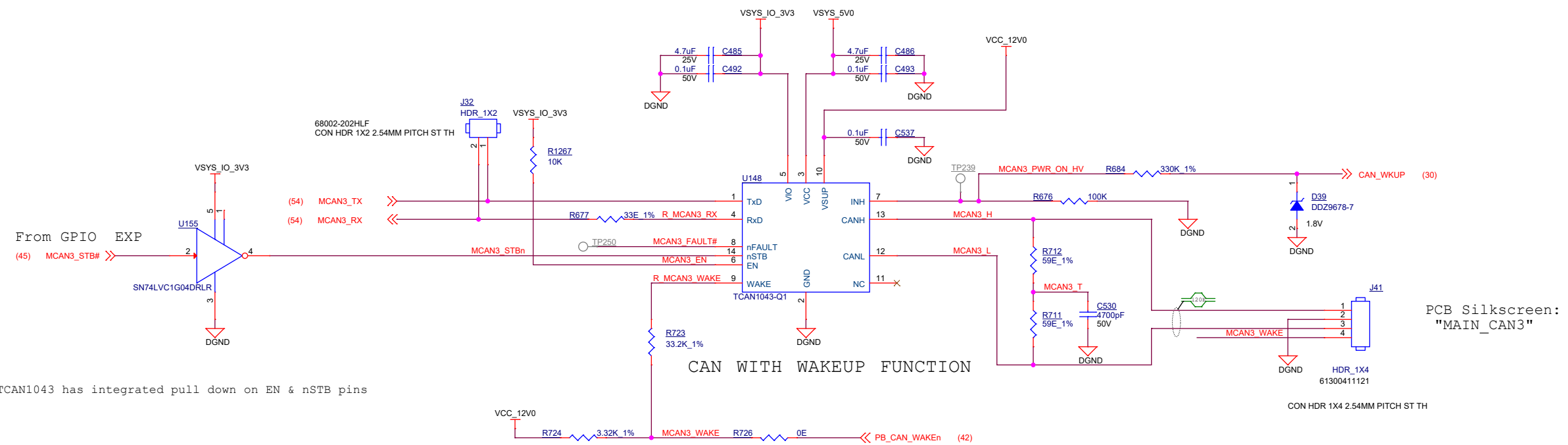
VSYS_MCU_5V0 GENERATION

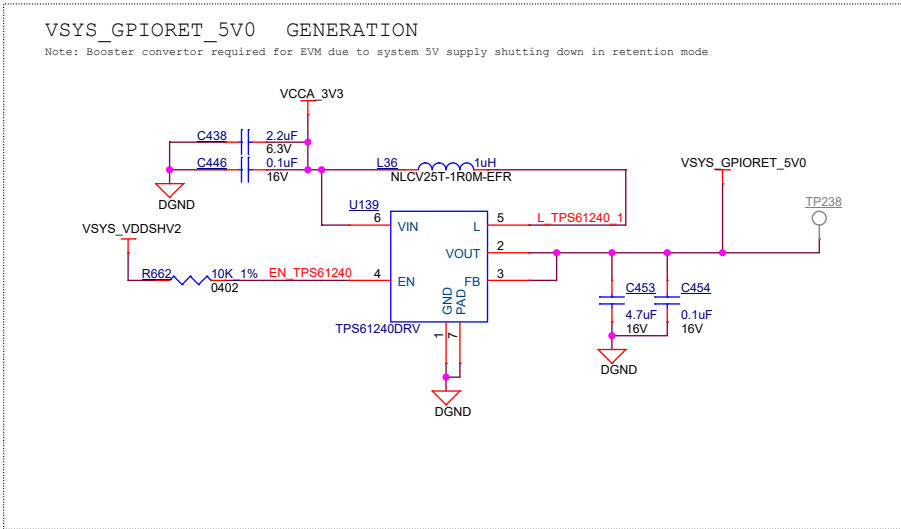


Separate 5V0 supply required for MCU-Only Mode

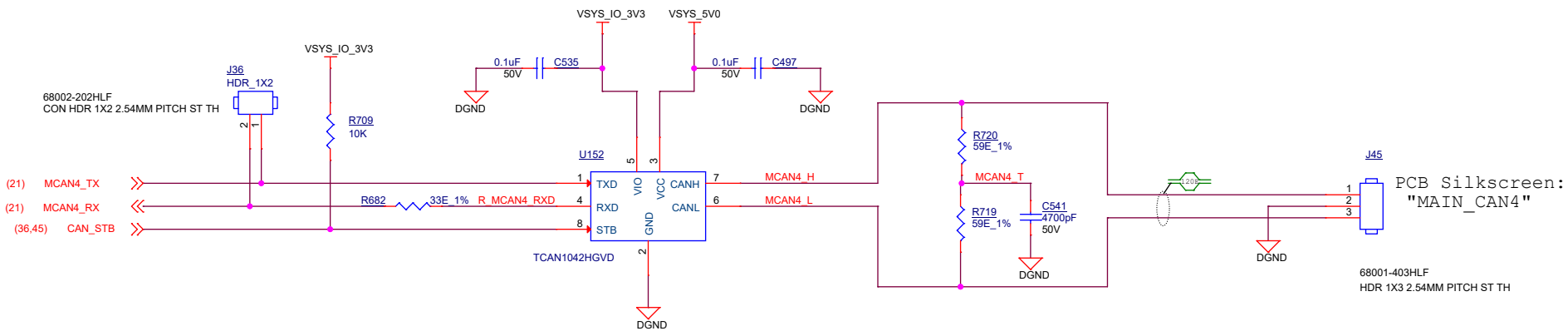
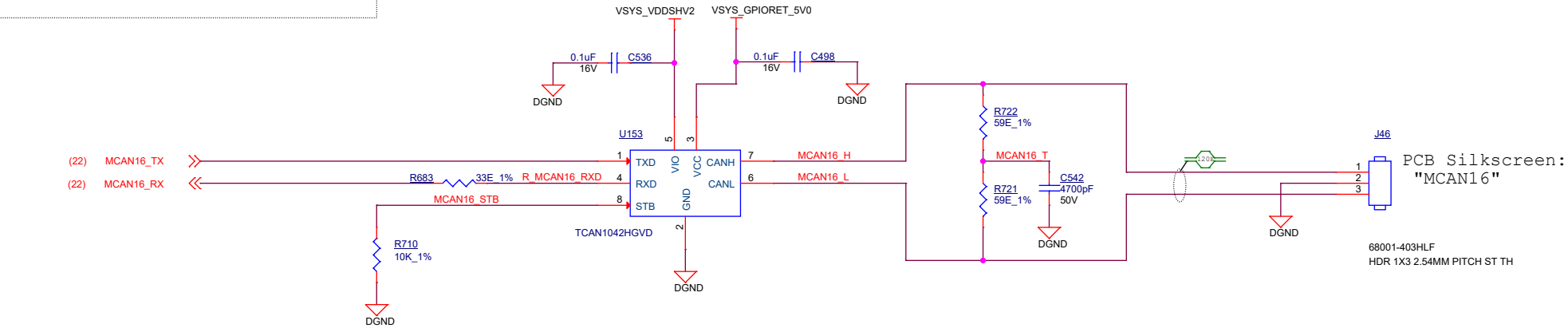


CAN TRANSCEIVERS #2-MAIN DOMAIN

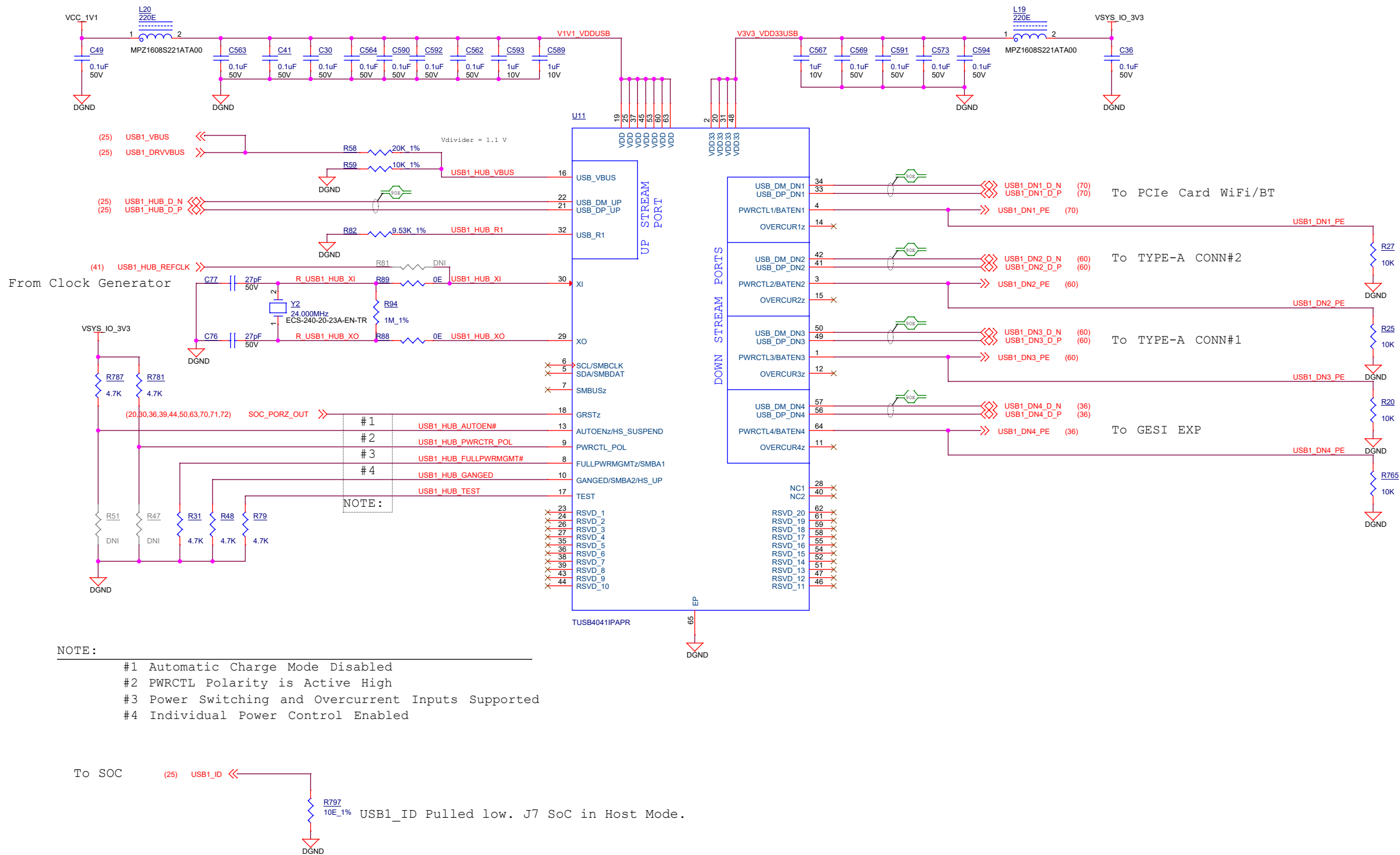




CAN TRANSCEIVER



USB HUB



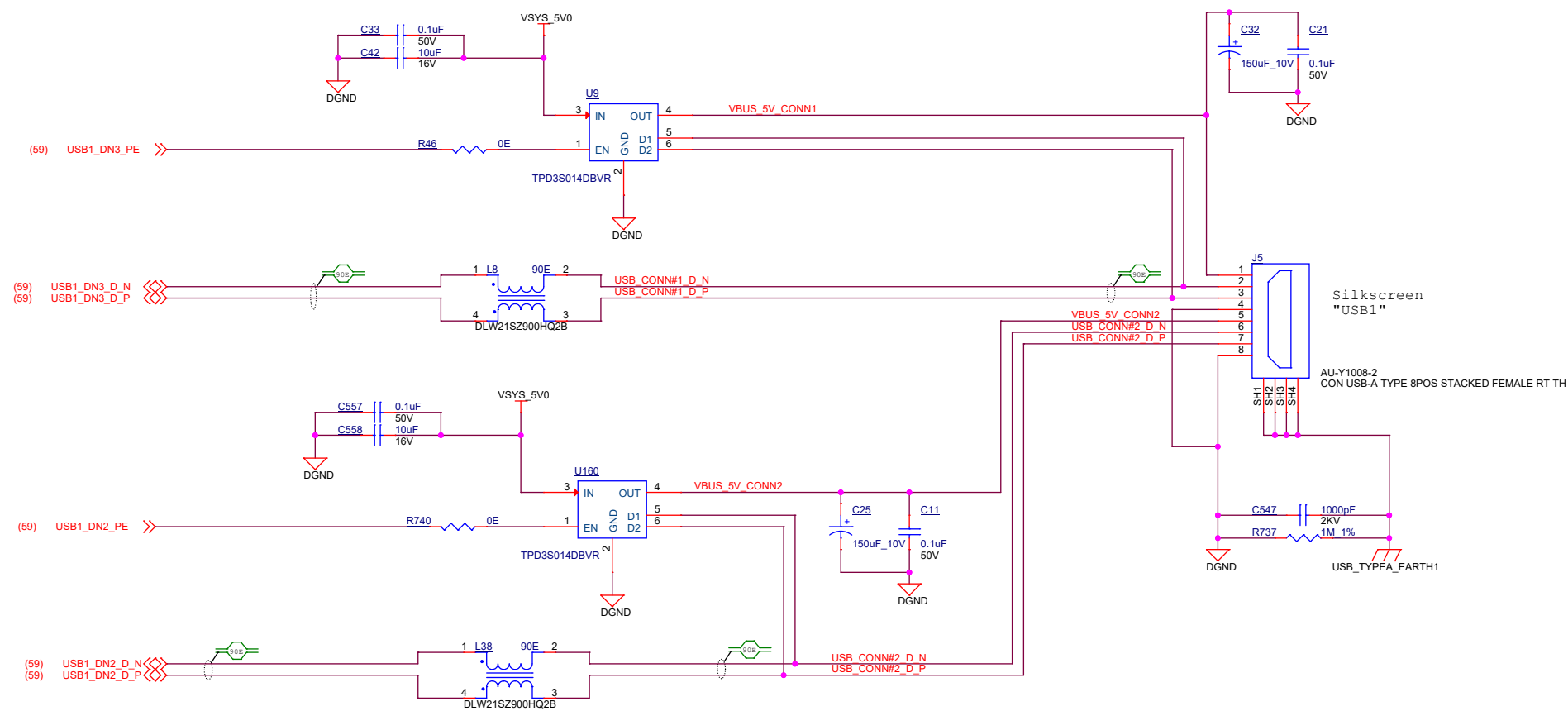
NOTE:

- #1 Automatic Charge Mode Disabled
- #2 PWRCTL Polarity is Active High
- #3 Power Switching and Overcurrent Inputs Supported
- #4 Individual Power Control Enabled

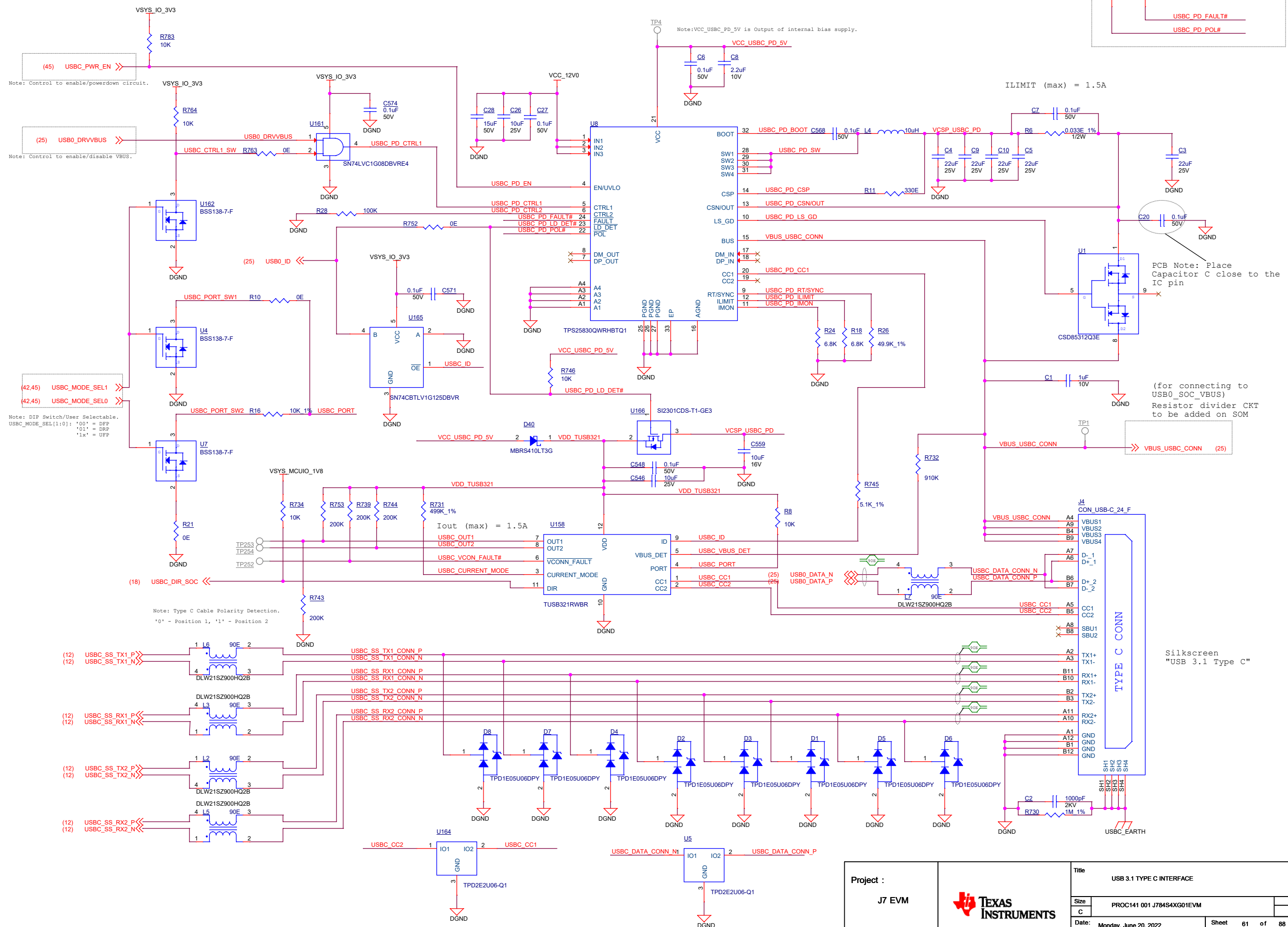
To SOC (25) USB1_ID <<<

R797 10E_1% USB1_ID Pulled low. J7 SoC in Host Mode.

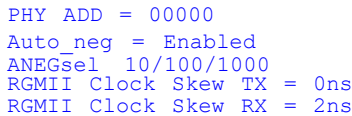
USB 2.0 TYPE-A CONNECTORS



USB 3.1 TYPE C INTERFACE

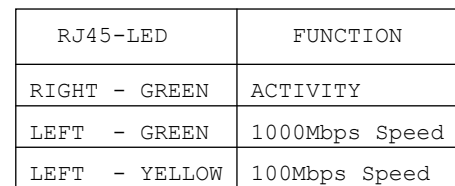


MCU GB ETHERNET



```
Set Mode 3 [Autoneg Disable - 0]
```

SPEED AND ACTIVITY LED DRIVERS



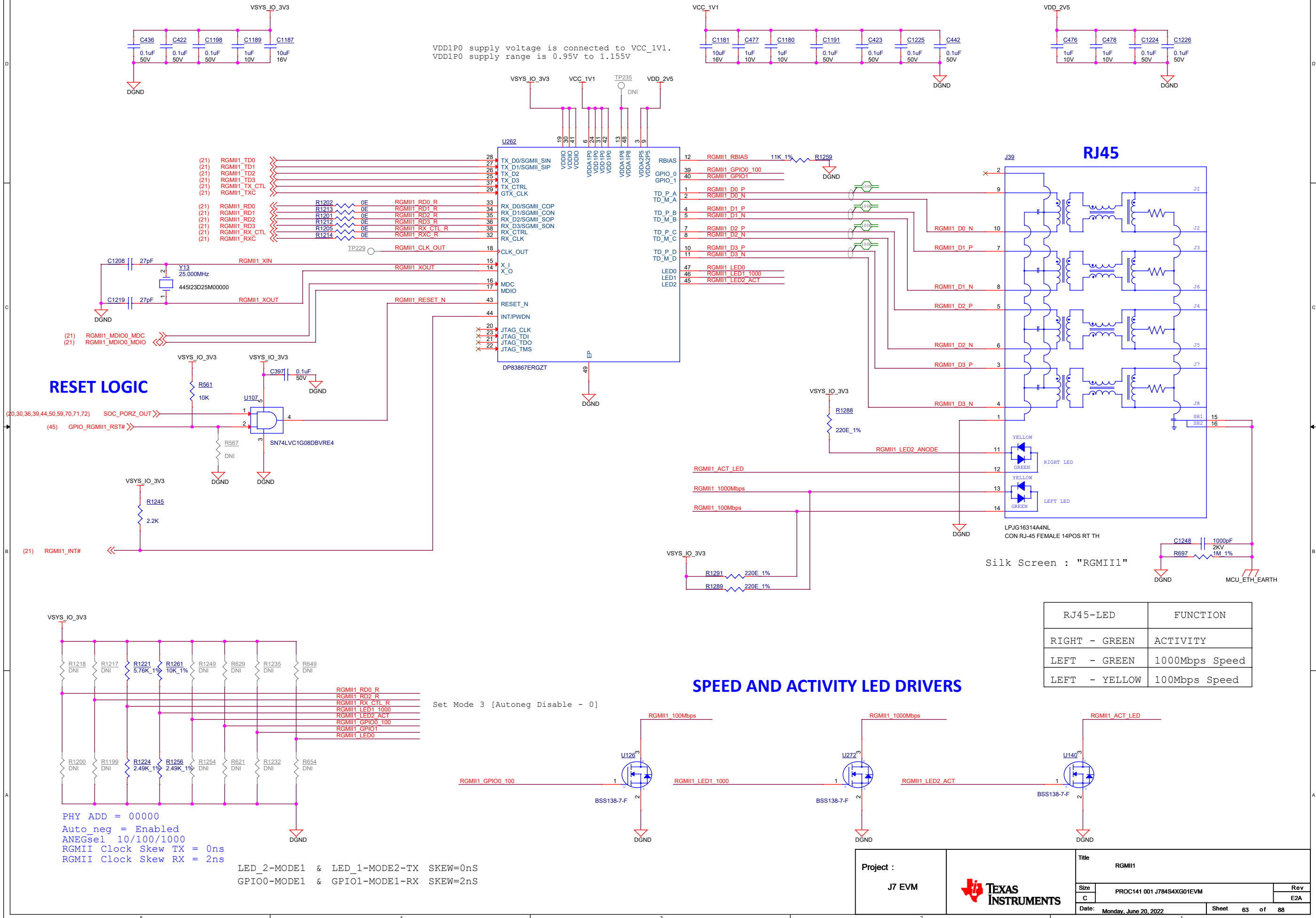
RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	100Mbps Speed
LEFT - YELLOW	100Mbps Speed



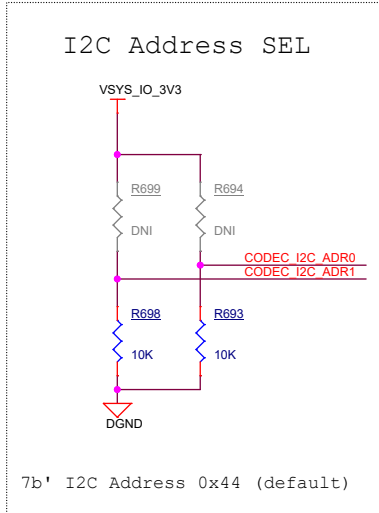
Title	MCU GB ETHERNET
-------	-----------------

Size	PROC141 001 J784S4XG01EVM			
C				
Date:	Monday, June 20, 2022	Sheet	62	of 88

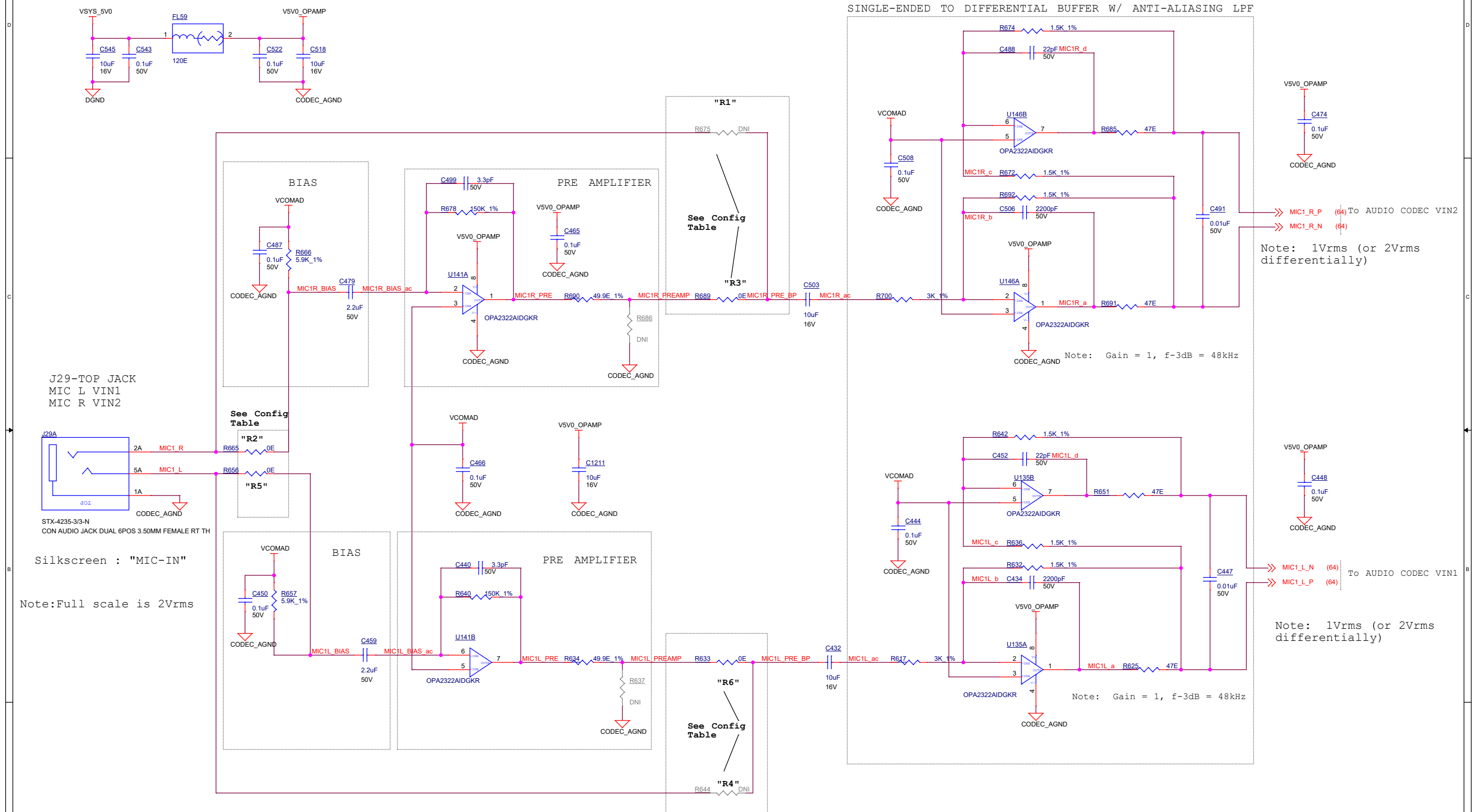
RGMII1



AUDIO I/F CODEC

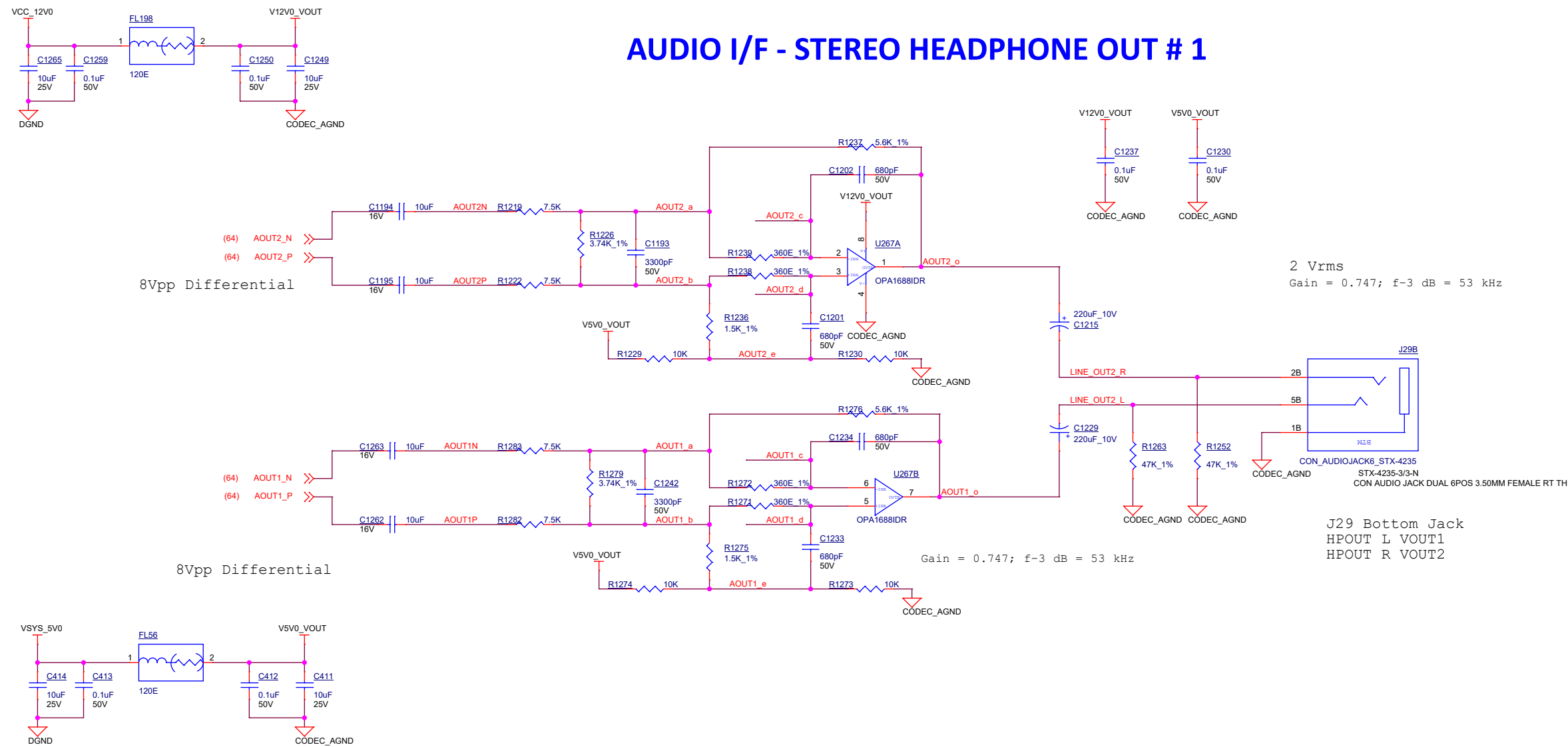


AUDIO I/F - STEREO MIC #1

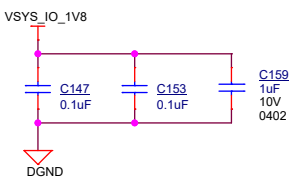
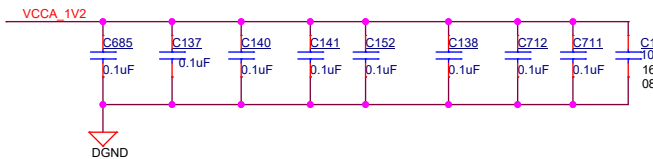
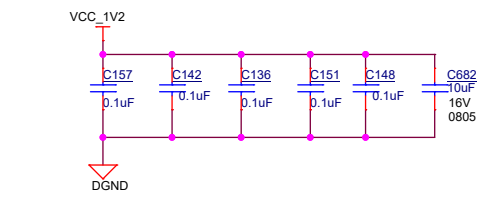
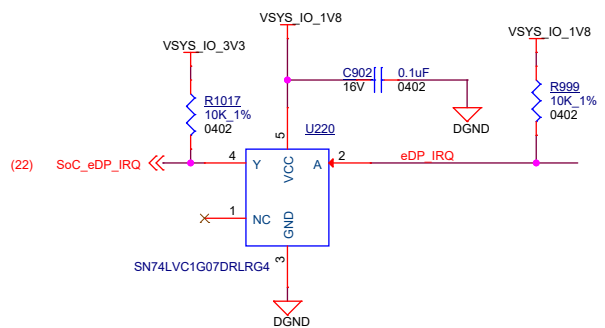
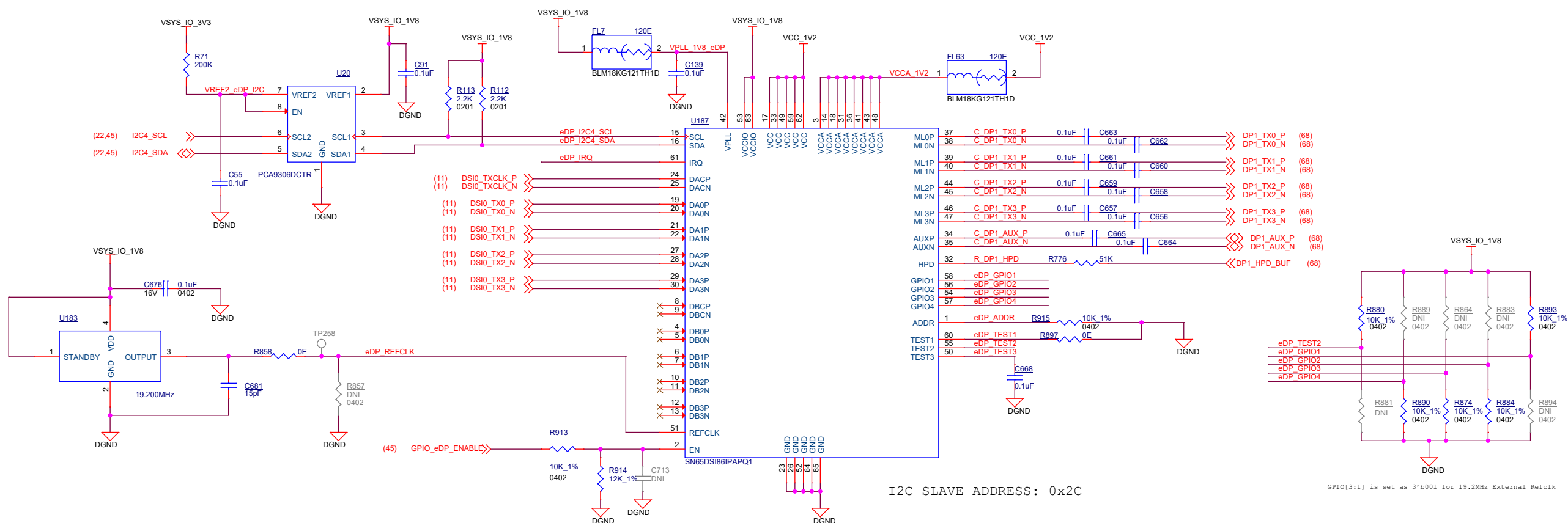


		Install	Remove
PASSIVE-MIC (default)	BIAS + PREAMP	R2,R3,R5,R6	R1,R4
ACTIVE-MIC	BIAS ONLY	R1,R2,R4,R5	R3,R6
LINE-INPUT	NO BIAS/PREAMP	R1,R4	R2,R3,R5,R6

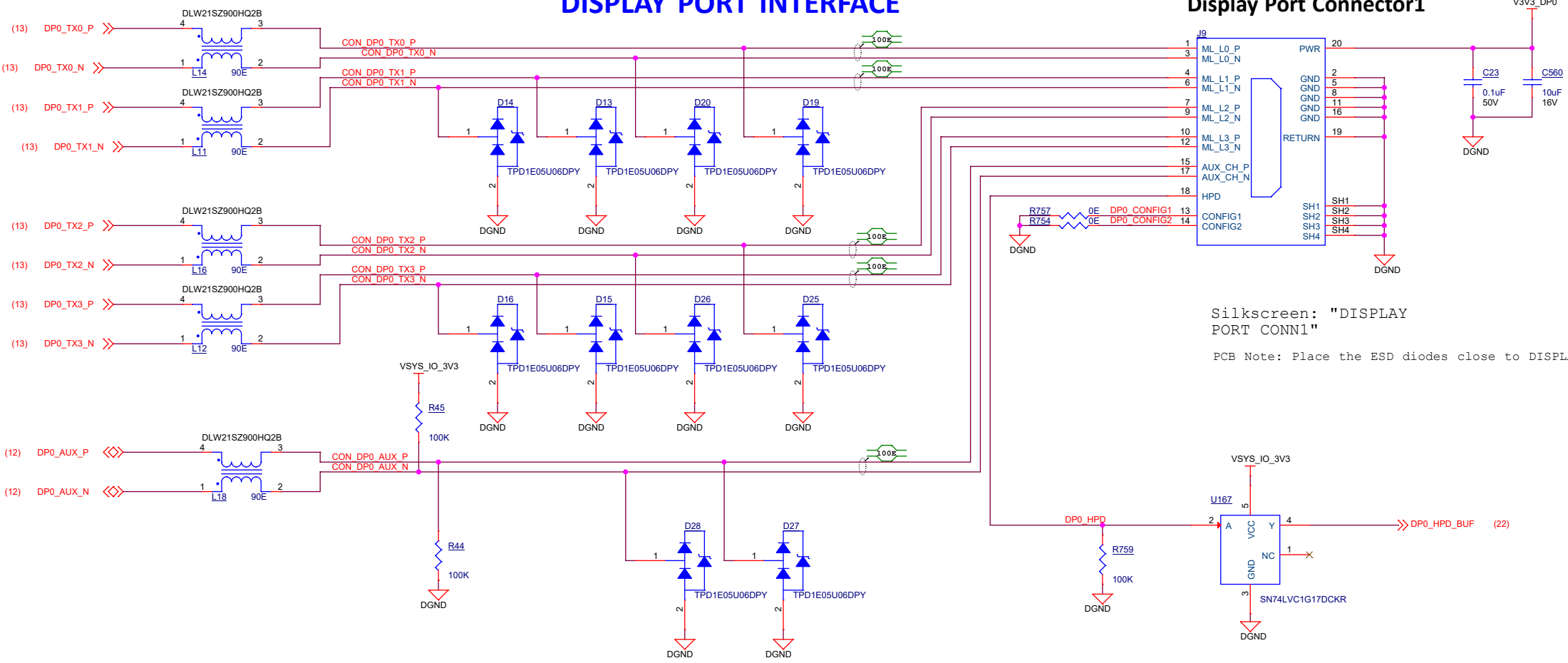
AUDIO I/F - STEREO HEADPHONE OUT # 1



DSI to eDP Bridge

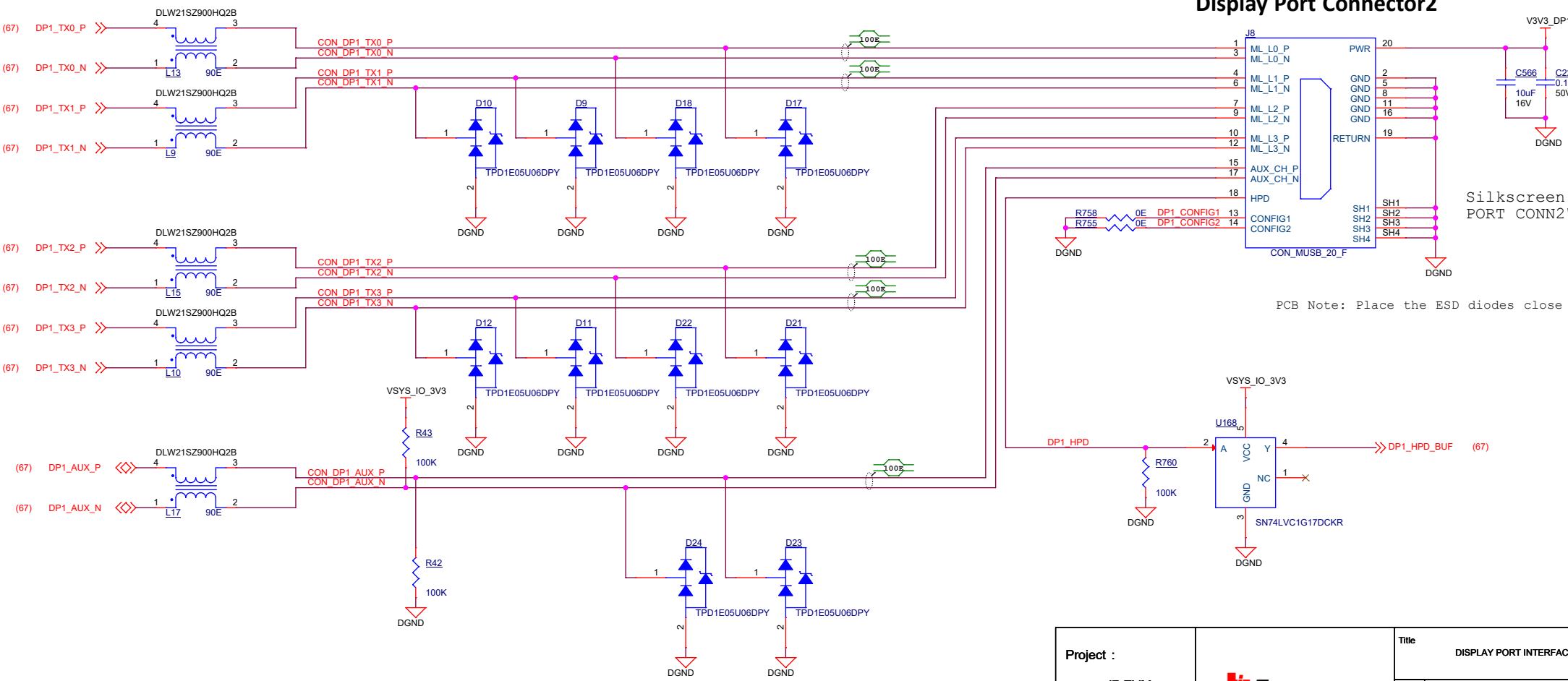


DISPLAY PORT INTERFACE



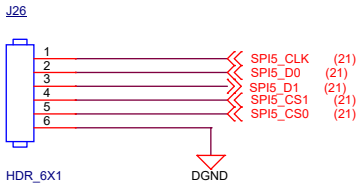
Silkscreen: "DISPLAY
PORT CONN1"
PCB Note: Place the ESD diodes close to DISPLAY PORT CONN1

Display Port Connector2

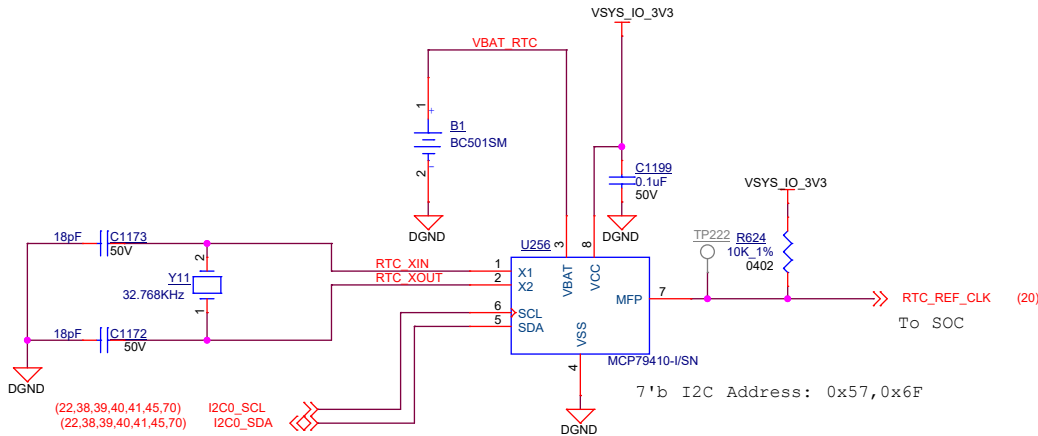


Silkscreen: "DISPLAY
PORT CONN2"
PCB Note: Place the ESD diodes close to DISPLAY PORT CONN2

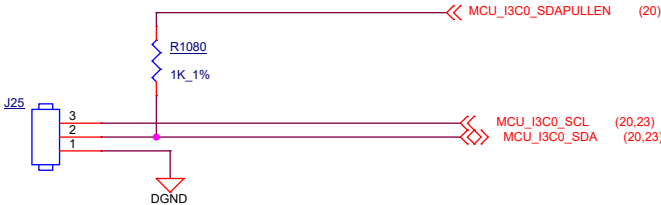
SPI Header



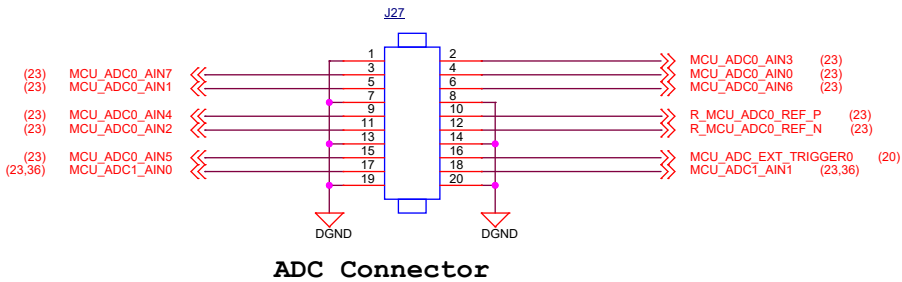
RTC



I3C Header



ADC INTERFACE



Silk Screen MCU-I3C

x4 Lane PCIe Connector

[illegible]

The schematic diagram illustrates the I2C MUX circuit. It features two 3-input AND gates, U175 and U176, and two 1:4 decoders, U15 and U14. The AND gates are configured to generate the PCIe0 AND OUT and PCIe0 NAND OUT signals. The decoders are configured to generate the PCIe0 4L PERSTz and PCIe0 4L MODE_SEL signals. The I2C MUX (U181) is connected to the I2C bus (SDA, SCL) and the RESET signal. The circuit is powered by VSYS_IO_3V3 and DGND. Various components like resistors (R779, R782, R54, R73, R820, R821, R157, R819, R822), capacitors (C595, C596, C34, C48), and diodes (DNI) are shown. Signal pins are labeled with their functions and pin numbers.

TBU	Install	Remove
PCIe root complex	R1, R2, R5, R6	R3, R4, C1, C2
PCIe end point	R3, R4, C1, C2	R1, R2, R5, R6

to SOC (12)
SOC_SERDES0_REFCLK_P (12)
SOC_SERDES0_REFCLK_N

Place R1, R2 close to SOC

"R1" R176 DNI
"R2" R166 DNI

CLKGEN_SERDES0_REFCLK_P (39)
CLKGEN_SERDES0_REFCLK_N (39)

"R3" R177 DNI
"R4" R167 DNI

"C1" R_SERDES0_REFCLK_P C63
R_SERDES0_REFCLK_N

"Added to avoid stub"
Place R3, R4 close to SOC

Place R5, R6 close to PCIe connector

"R5" R77 OE
"R6" R92 OE

CLKGEN_PCIE0_4L_REFCLK_P (39)
CLKGEN_PCIE0_4L_REFCLK_N (39)

to PCIe Con (x1 Lane)


CON_PCIE0_4L_REFCLK_P
CON_PCIE0_4L_REFCLK_N

Place C1, C2 close to PCIe connector

"C2" 50V C66
50V

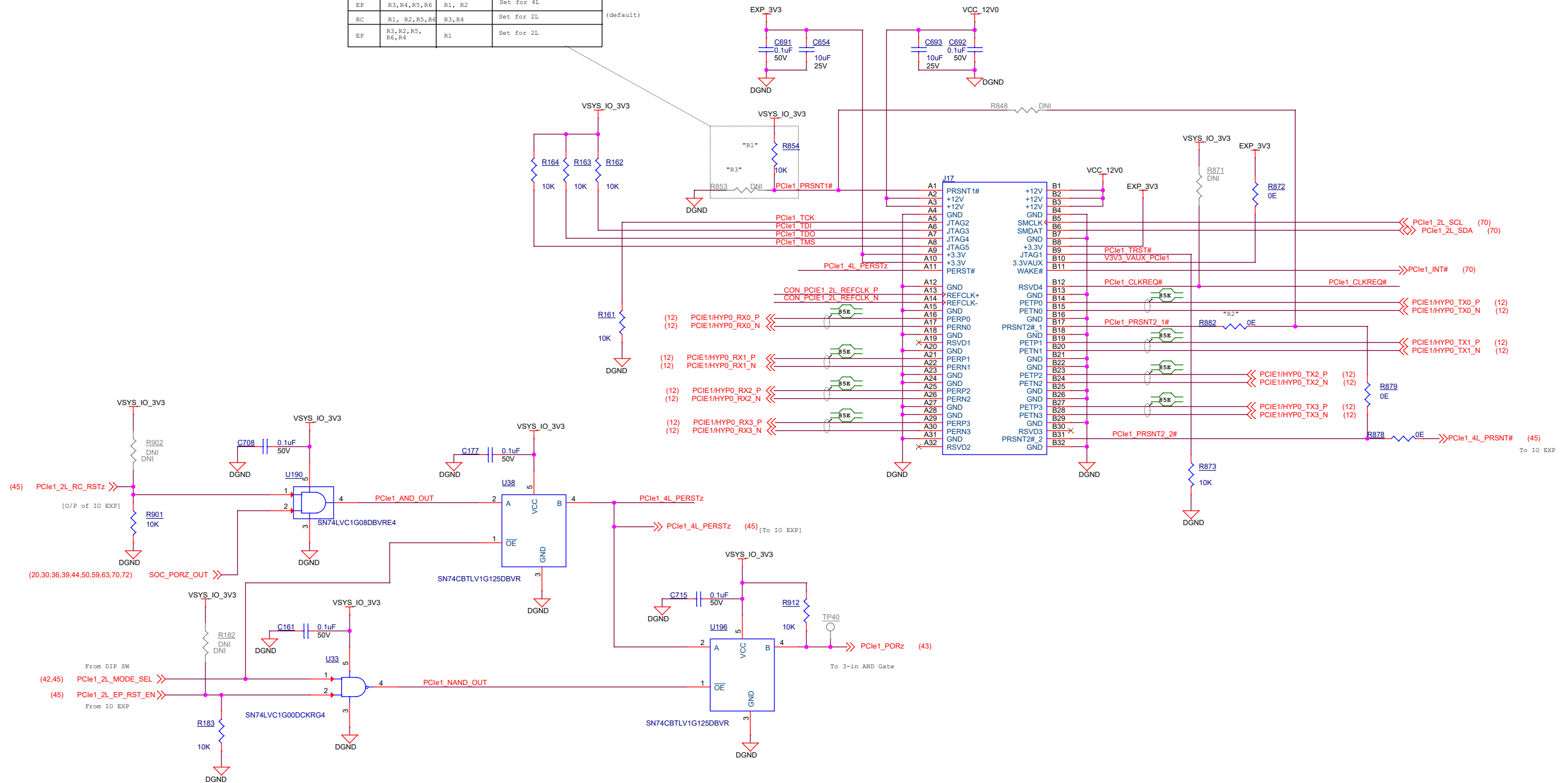
R83 DNI

Source for PCIe1 REFCLK
and R169

Project : J7 EVM		Title x1LANE PCIe INTERFACE		
		Size	PROC141 001 J784S4XG01EVM	Rev
		C		E2A
		Date:	Monday, June 20, 2022	Sheet 70 of 88

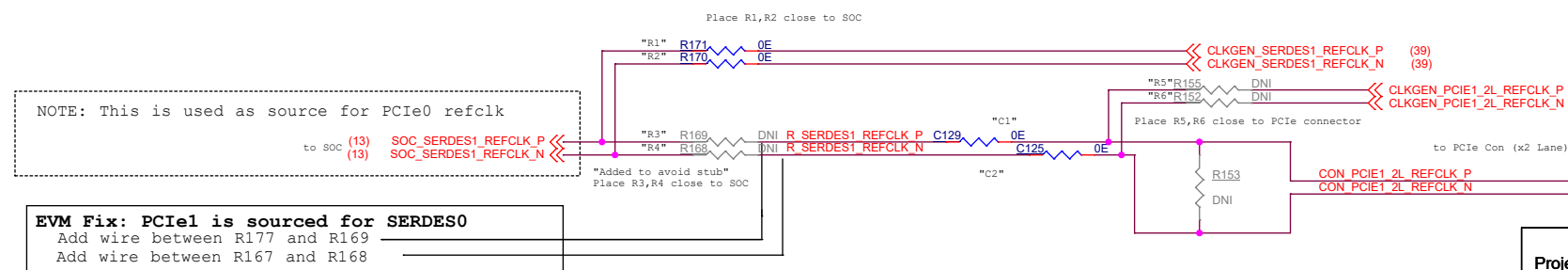
x2LANE PCIe1 Interface(J17)
x4 Lane PCIe Connector

MODE	INSTALL	DNI	PCIe Lanes
RC	R1, R6	R3,R4,R2,R5	Set for 4L
EP	R3,R4,R5,R6	R1, R2	Set for 4L
RC	R1, R2,R5,R6	R3,R4	Set for 2L
EP	R3,R2,R5, R6,R4	R1	Set for 2L

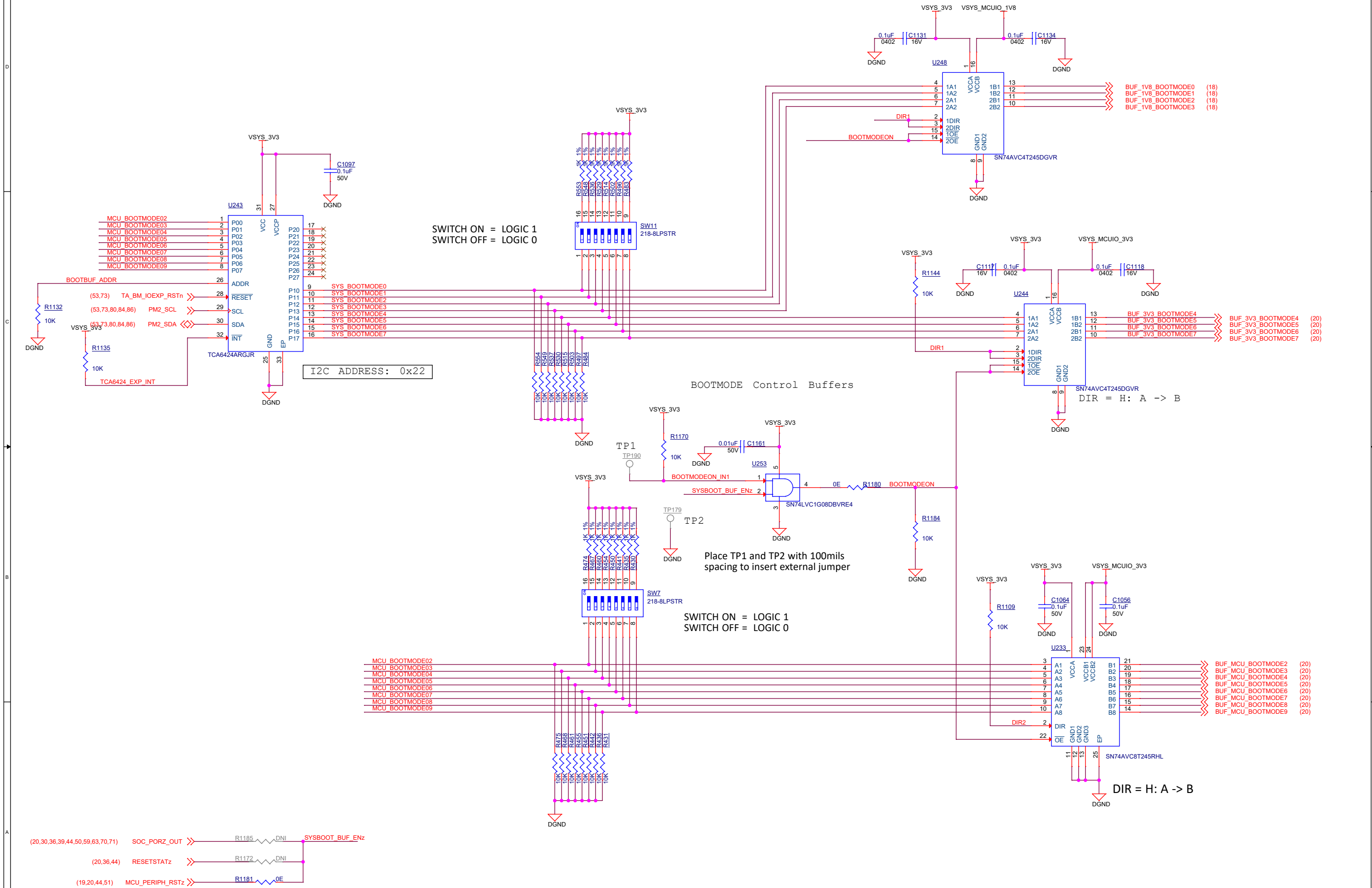


CLOCK ROOT SELECTION

TBU	Install	Remove
PCIe root complex	R1,R2,R5,R6	R3,R4,C1,C2
PCIe end point	R3,R4,C1,C2	R1,R2,R5,R6



BOOT MODE BUFFER & SWITCHES



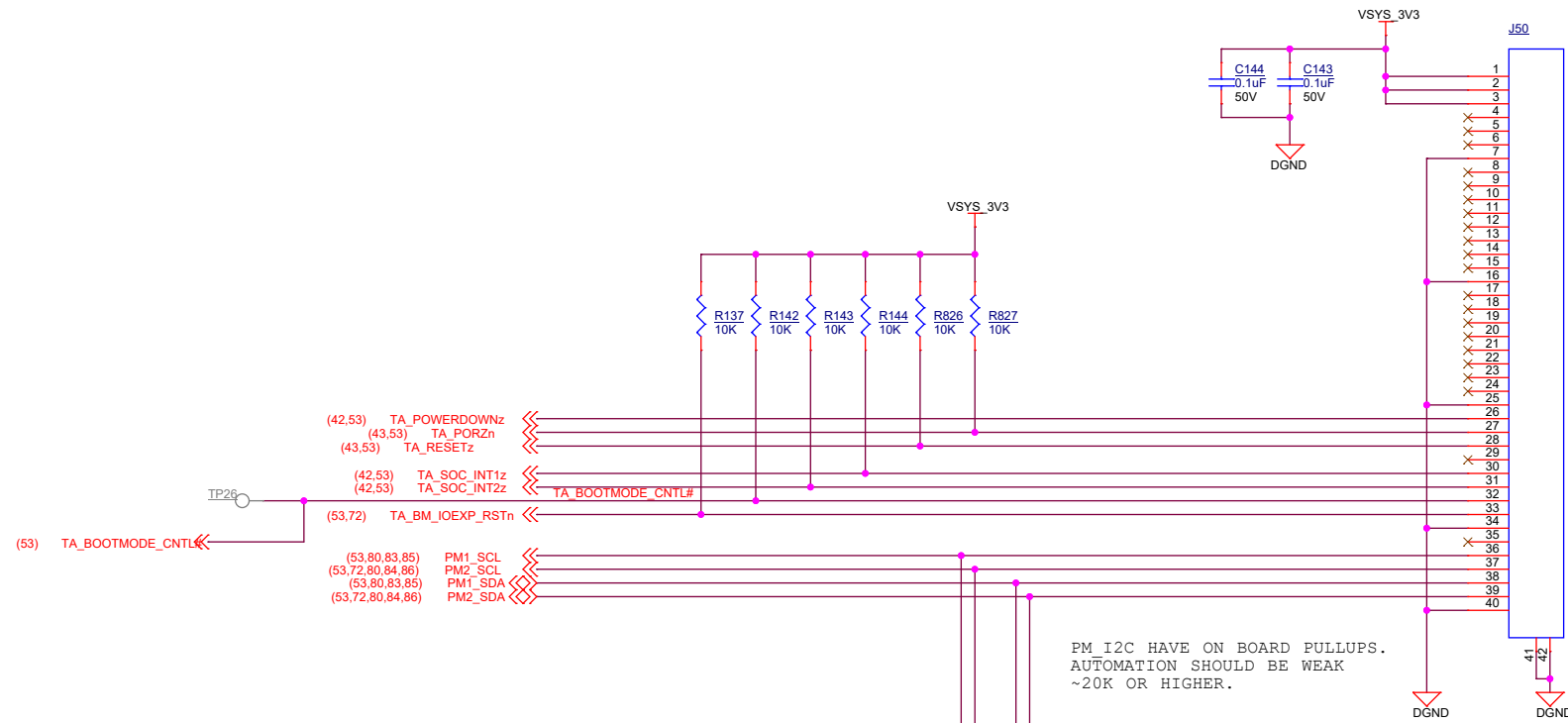
TA_BM_IOEXP_RSTn	SOC_PORZ_OUT	BOOTMODE Control from Test Automation HDR
HIGH	LOW	Enabled
HIGH	HIGH	Disabled

Project :
J7 EVM

TEXAS
INSTRUMENTS

Title BOOT MODE BUFFER & SWITCHES	
Size C	PROC141 001 J784S4XG01EVM
Date: Monday, June 20, 2022	Sheet 72 of 88

TEST AUTOMATION HEADER

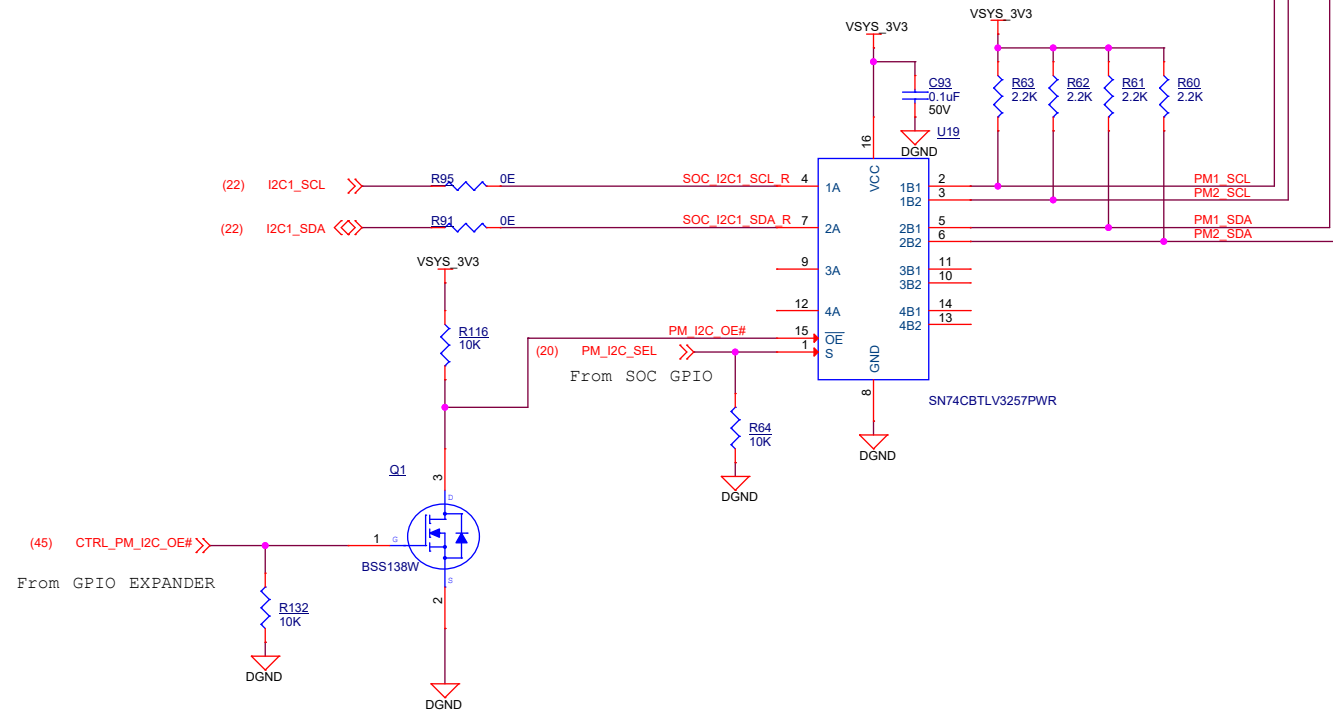


AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE
REFERENCED TO EVM_3V3

Cable : Parlex-050R40-76B, .5mm 3"

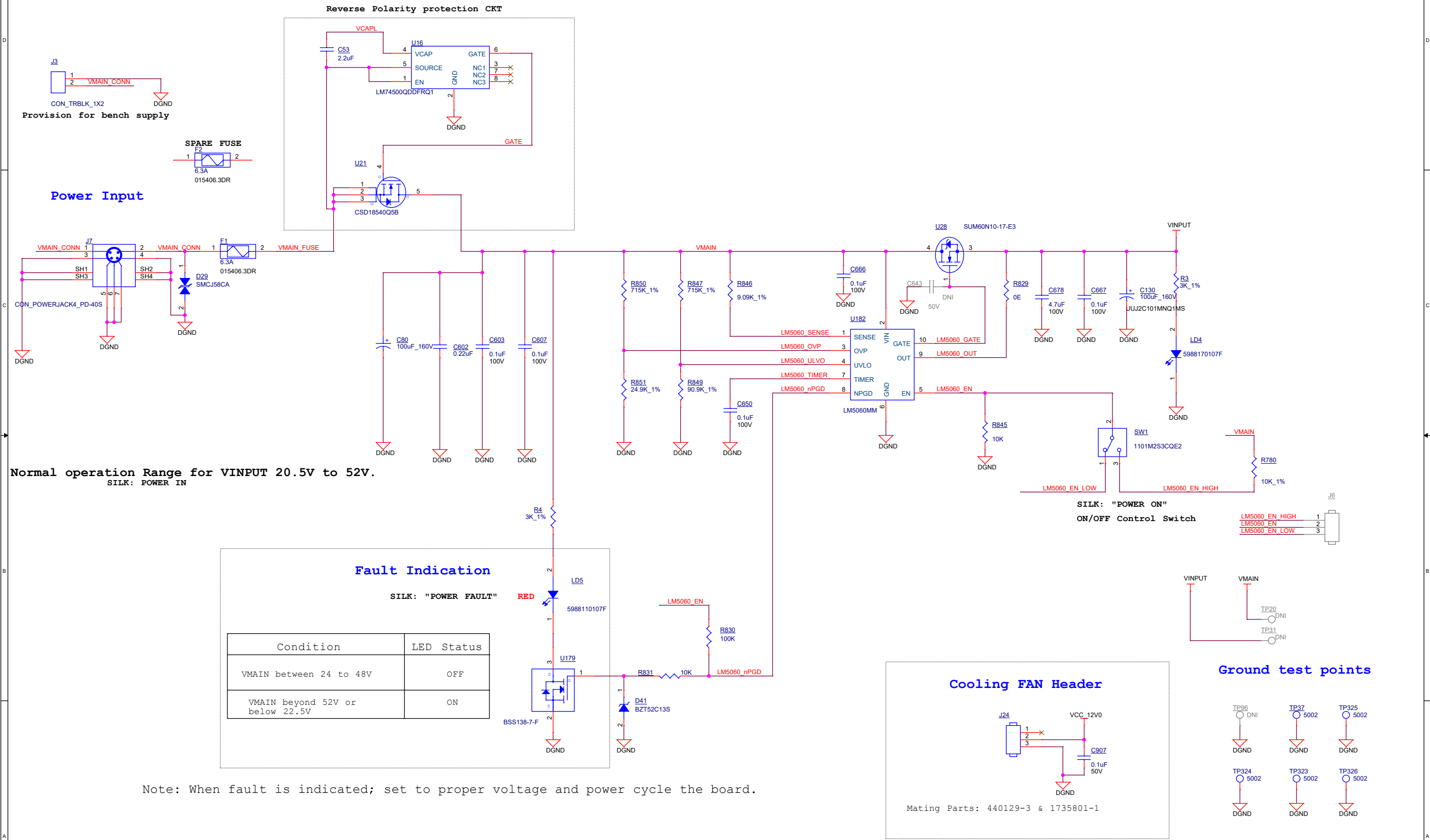
I2C SWITCH



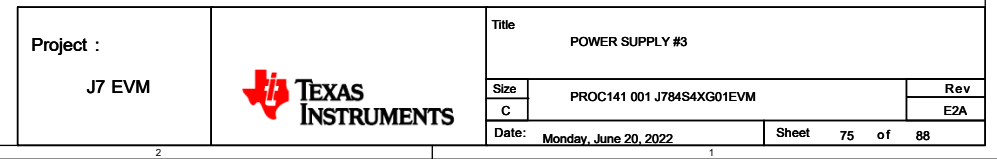
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

OVER VOLTAGE PROTECTION CIRCUIT

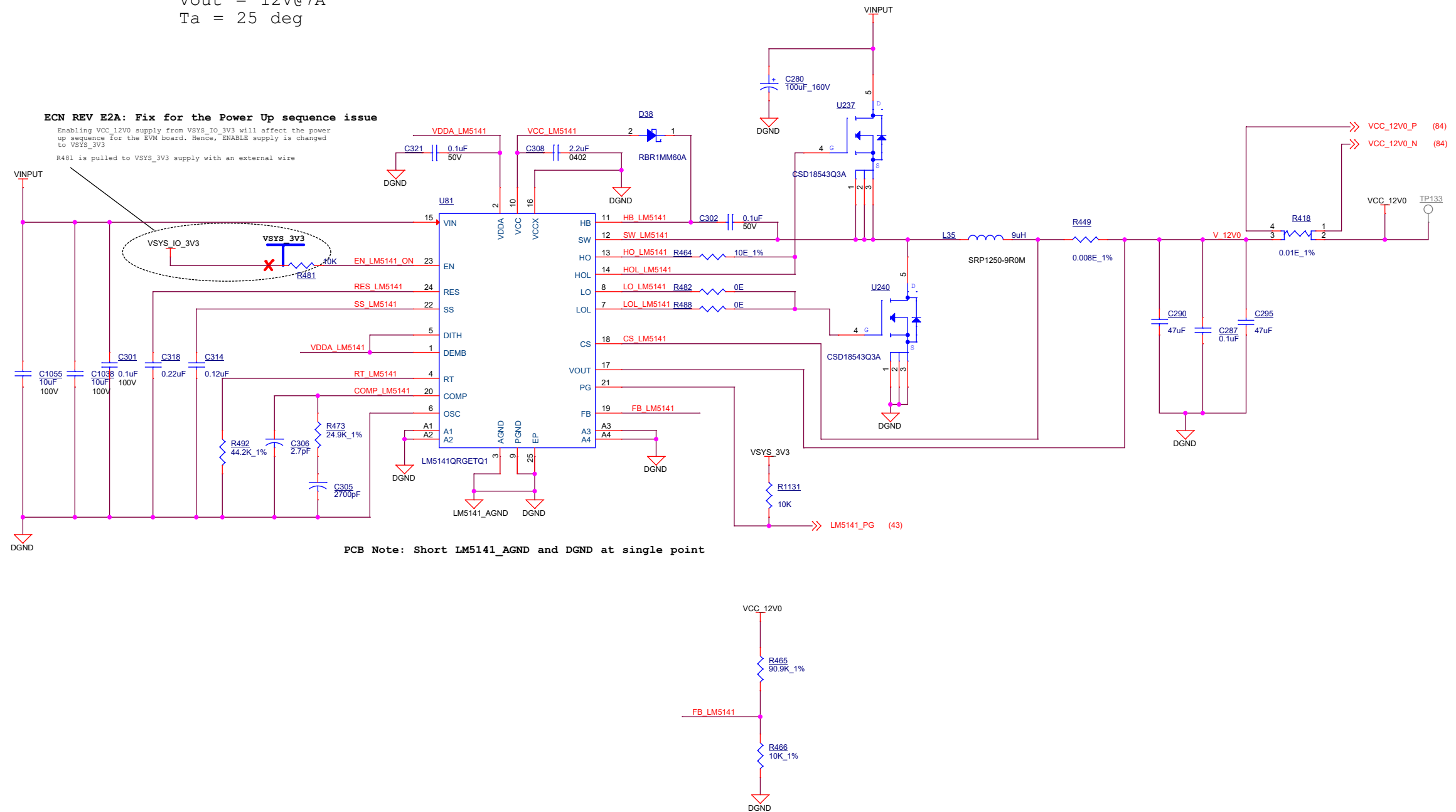


POWER SUPPLY #1



POWER SUPPLY #2

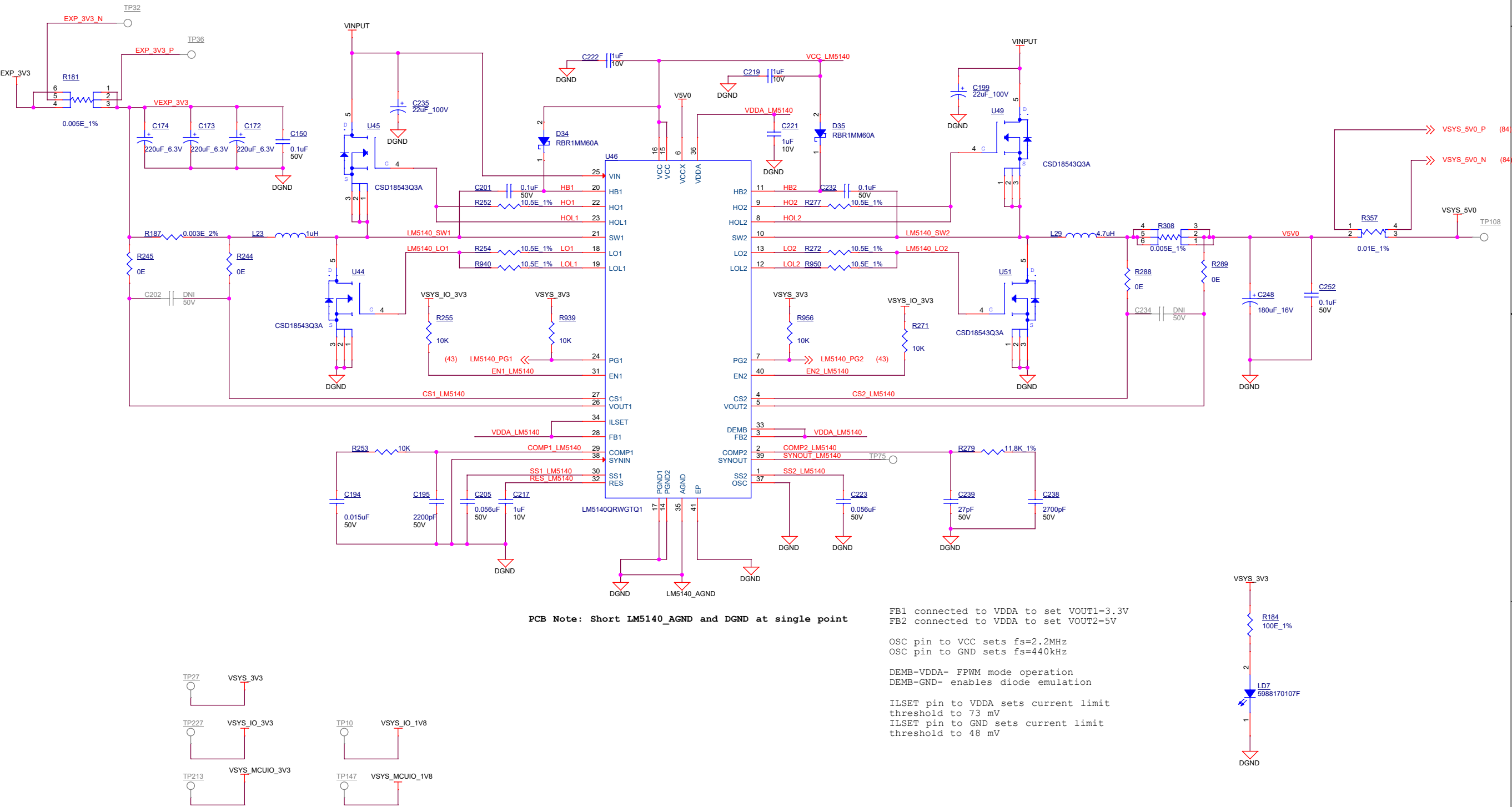
TI WEBENCH Simulation Inputs:
 Vin (min) = 24V Vin (max) = 48V
 Vout = 12V@7A
 Ta = 25 deg



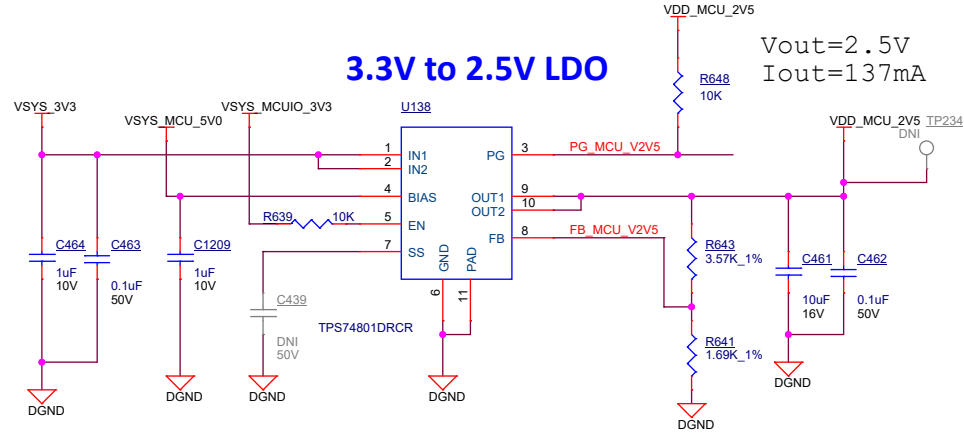
POWER SUPPLY #3

3.3V AND 5V GENERATION

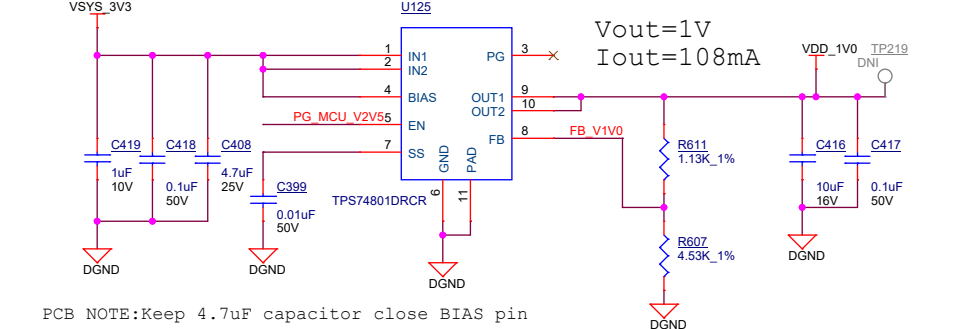
TI WEBENCH Simulation Inputs:
Vin (min) = 6V Vin (max) = 28V
Vout1 = 3.3V@10A; Vout2 = 5V@7A
Ta = 25 deg



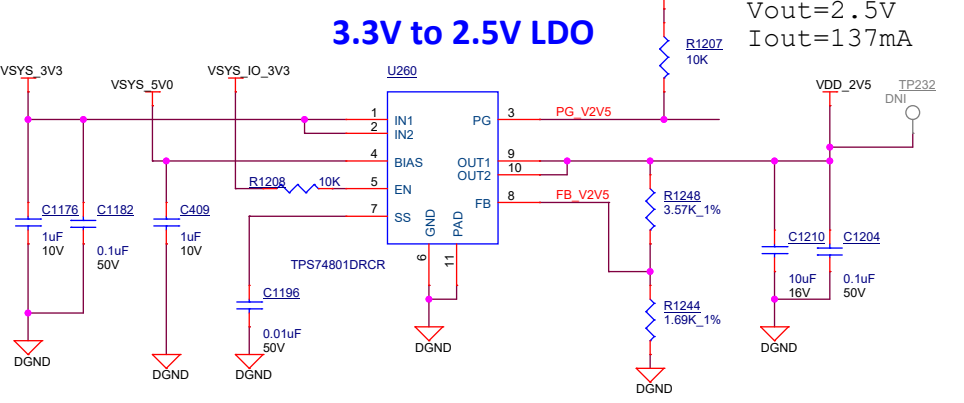
ETHERNET POWER- MCU RGMII



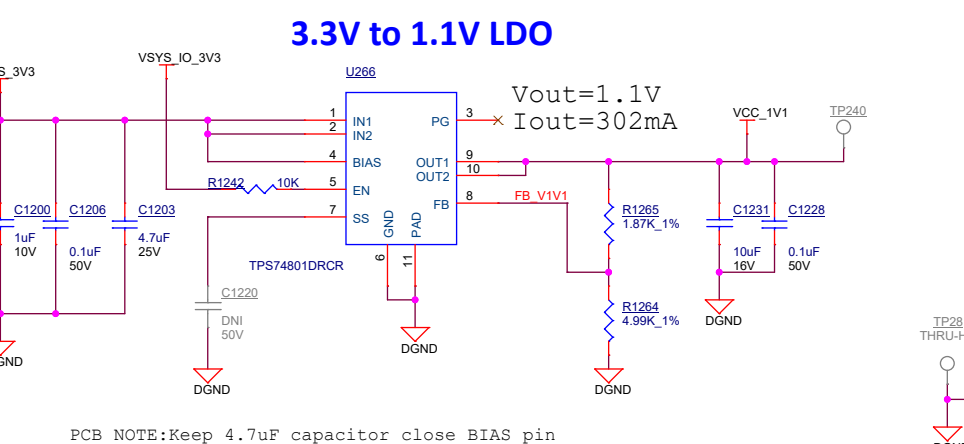
3.3V to 1.0V LDO



ETHERNET POWER- RGMII1

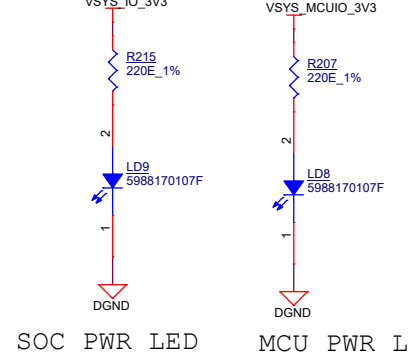


USB HUB POWER & ETHERNET POWER - RGMII1

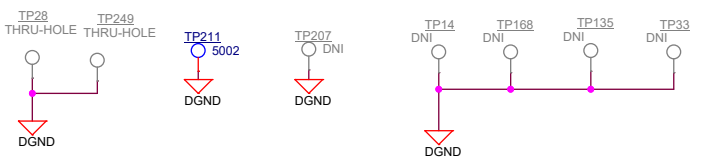


POWER SUPPLY #4

POWER INDICATION LED's

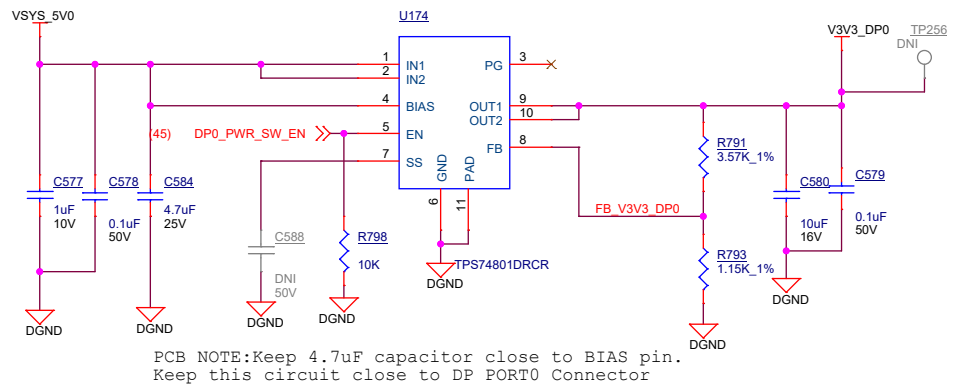


GROUND TEST POINTS

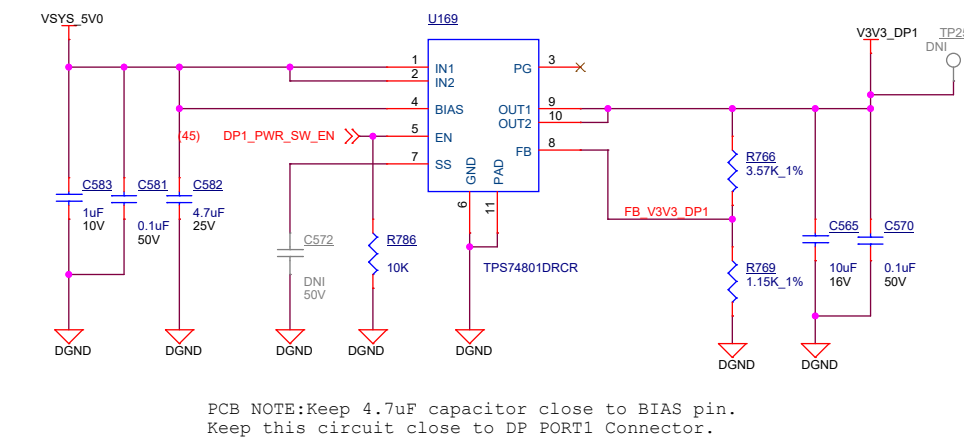


Display Port0

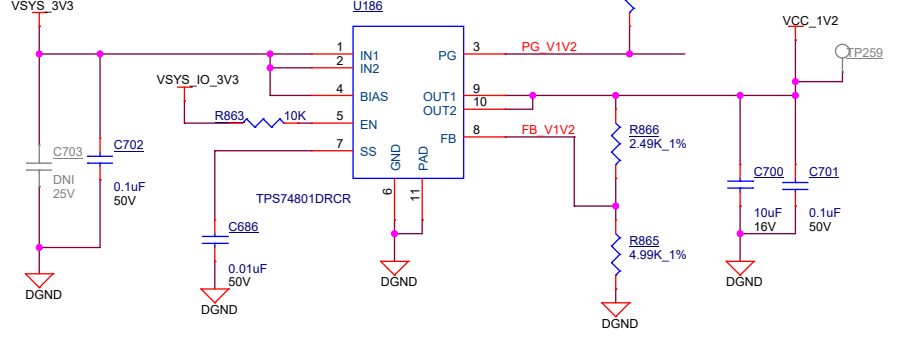
5V to 3.3V LDO



Display Port1
5V to 3.3V LDO



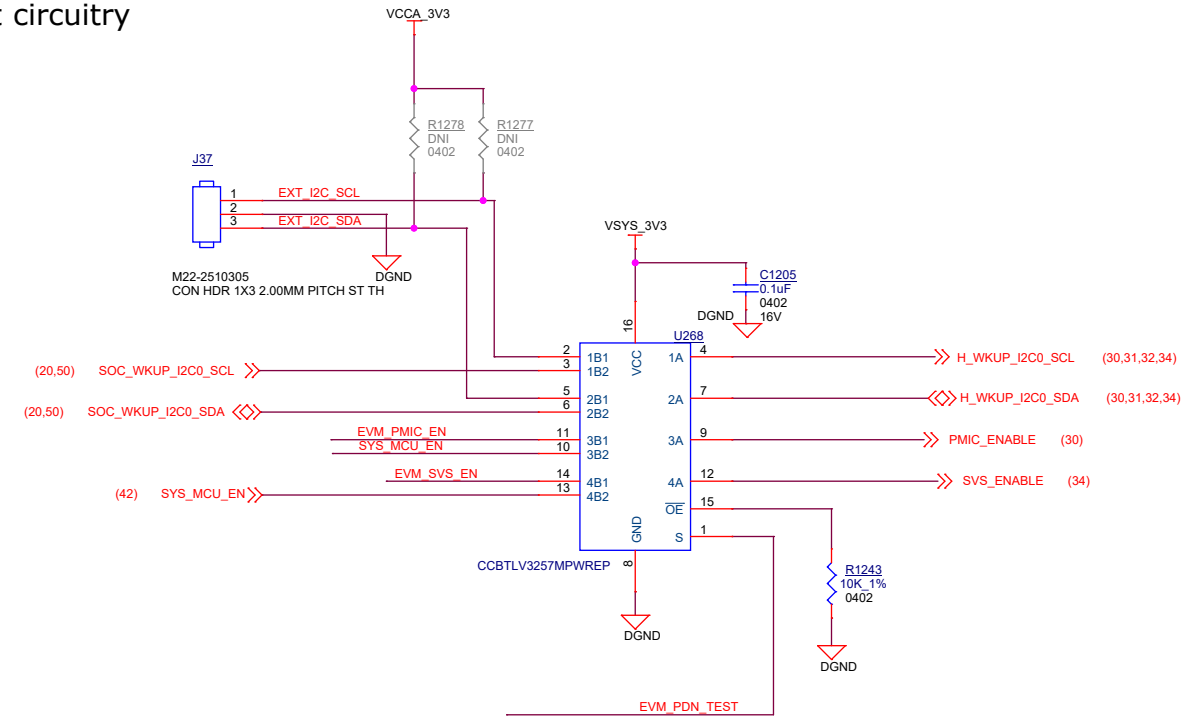
3.3V to 1.2V LDO



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

Project : J7 EVM		Title POWER SUPPLY #4	
		Size C	Rev E2A
		Date: Monday, June 20, 2022	
		Sheet 78 of 88	

EVM development & evaluation Test circuitry
(TI EVM Only)

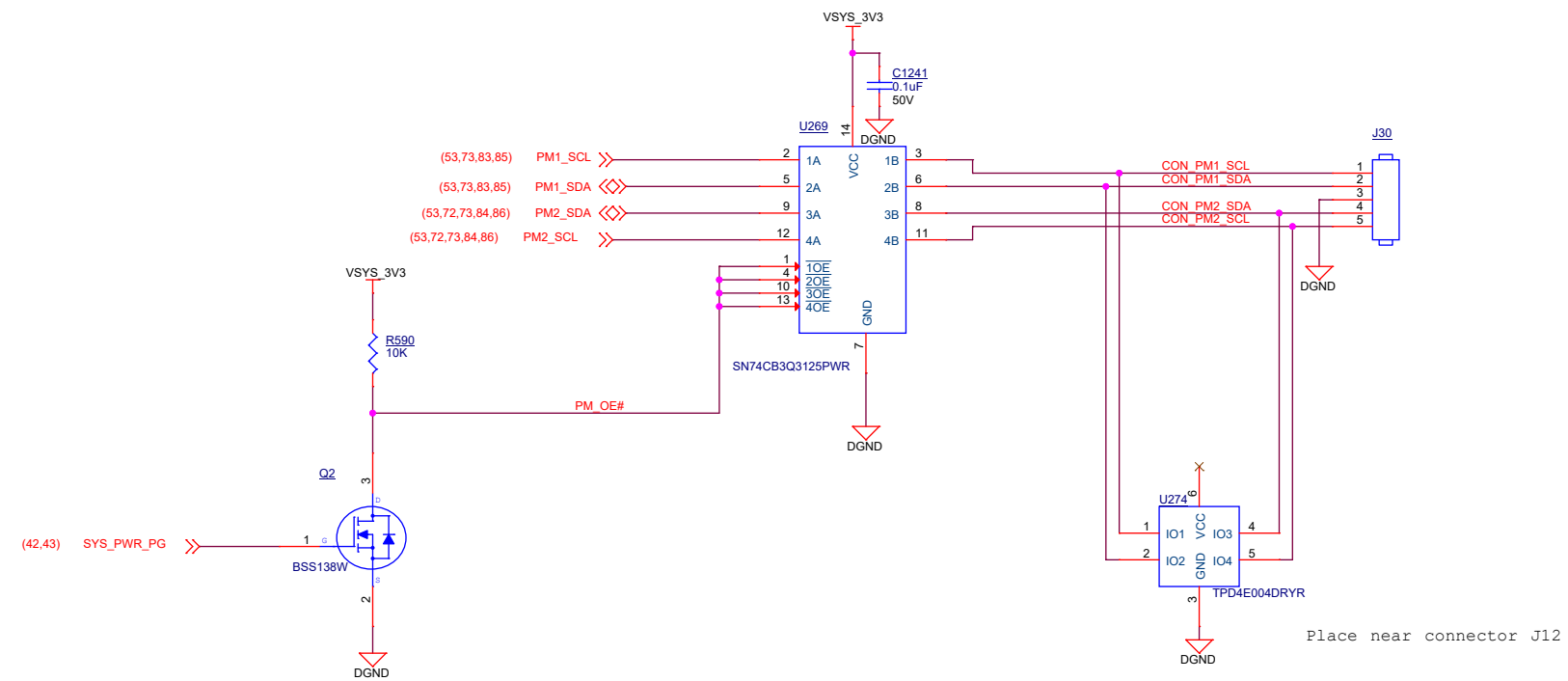



OEn	S	Bit State
0	0	A = B1
0	1	A = B2
1	X	Open

SW16	Function
-1 = Closed (High) = Open (Low)	Enable the PMIC by overriding SYS_MCU_ENABLE Enable the PMIC from SYS_MCU_EN
-2 = Closed (High) = Open (Low)	ENABLE SVS_EN from SW16.2 ENABLE SVS_EN FROM SYS_MCU_EN
-3 = Closed (High) = Open (Low)	1. PMIC_EN from SYS_MCU_EN 2. On Board WKUP I2C0 is selected 3. SVS_EN is controlled from SYS_MCU_EN 1. PMIC_EN is controlled from SW16.1 2. EXT_I2C is selected 3. SVS_EN is controlled from SW16.2
-4 = Closed (High) = Open (Low)	Disable WDOG Timer Enable WDOG Timer

EVM POWER MEASUREMENT I2C BUS ISOLATION

EVM development & evaluation Test circuitry (TI EVM Only)

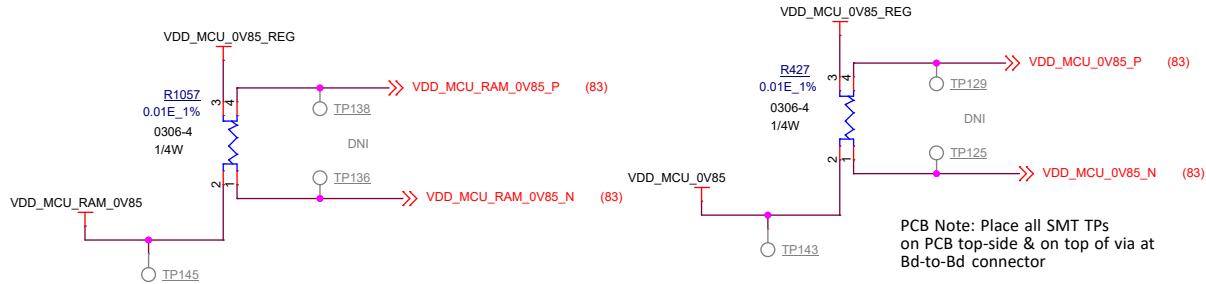
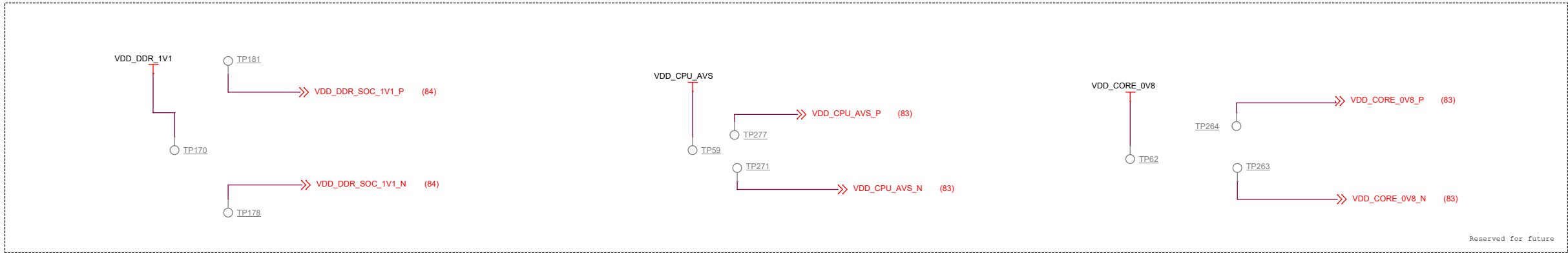


<div>Project : J7 EVM</div>	<div> TEXAS INSTRUMENTS</div>	<div>Title<div>EXTERNAL POWER MEASUREMENT WITH ISOLATION</div></div>			
		Size	PROC141 001 J784S4XG01EVM		Rev
		C			E2A
		Date:	Monday, June 20, 2022	Sheet	80 of 88

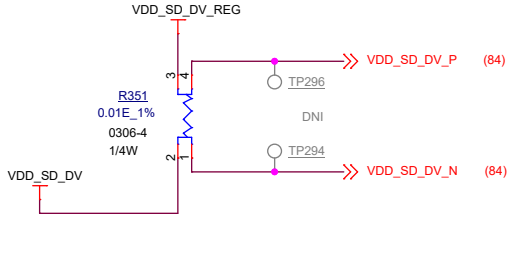
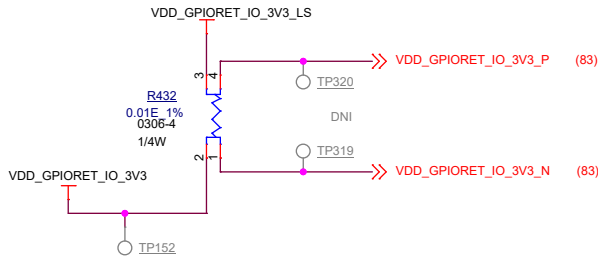
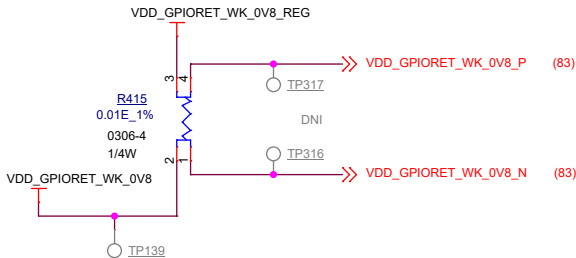
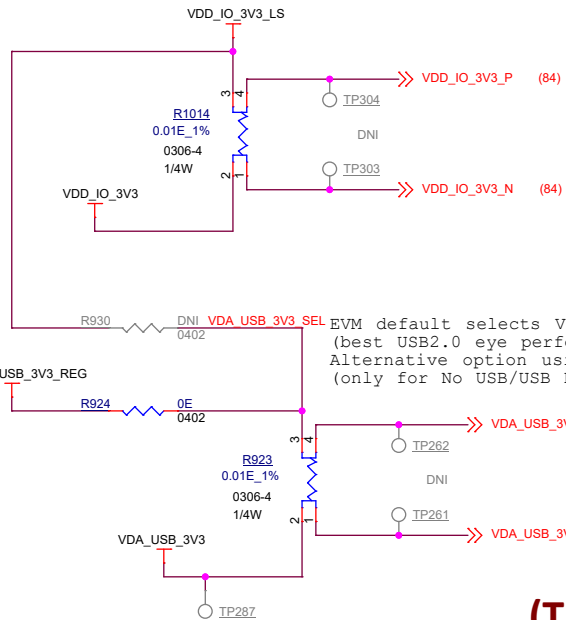
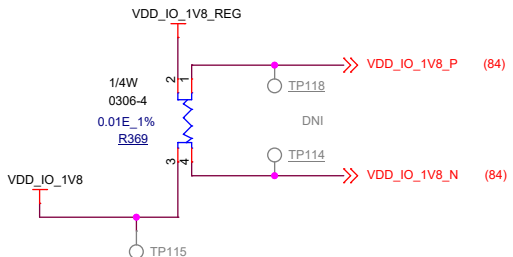
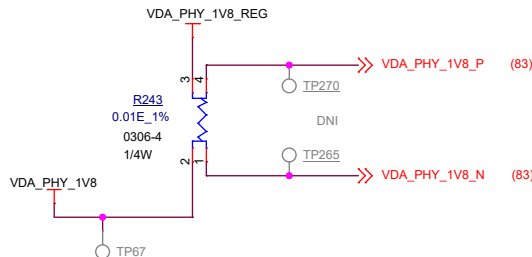
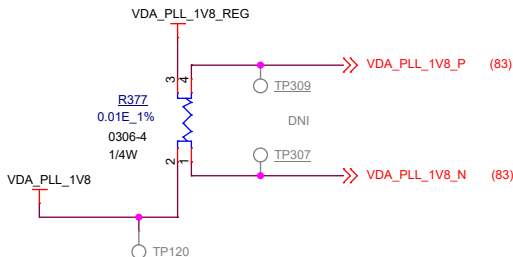
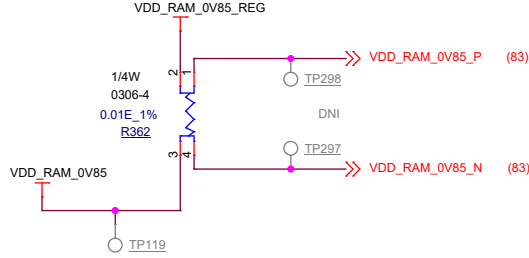
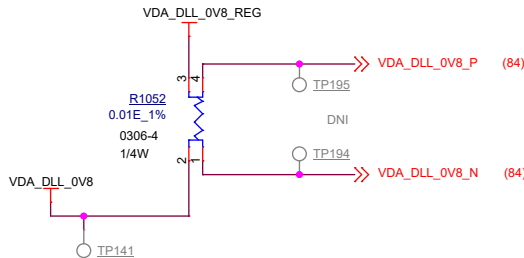
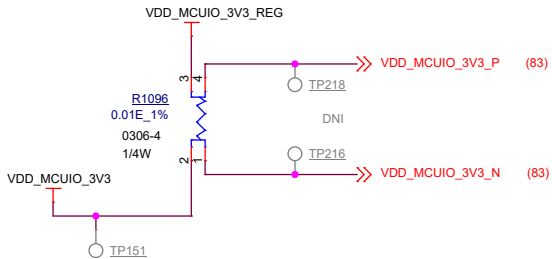
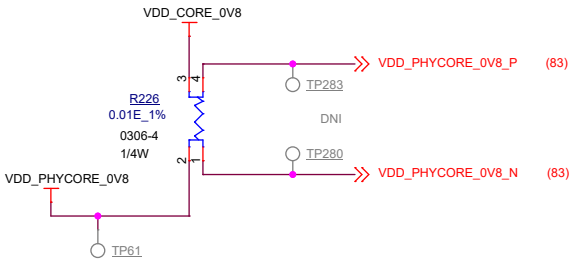
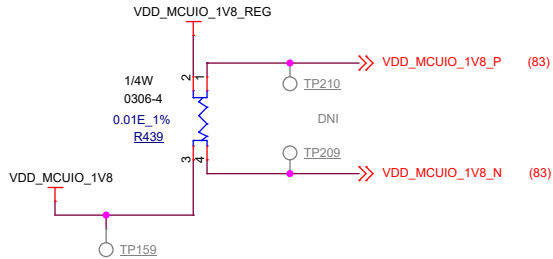
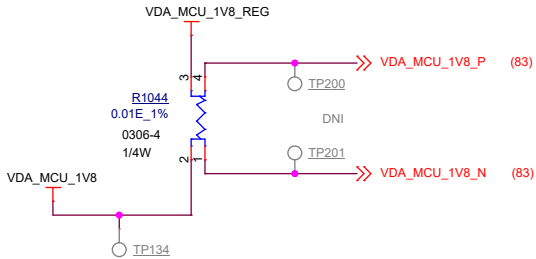
(TI EVM Only)

SOC Current Sense Resistors

(TI EVM Only)



PCB Note: Place all SMT TPs on PCB top-side & on top of via at Bd-to-Bd connector



Low voltage PHY rail supplied from output side of CORE current sense R in order to minimize voltage differences btw Core logic & PHY modules.

(TI EVM Only)

(TI EVM Only)

Project :

J7 EVM



Title
SOC Current Sense Resistors

Size
C PROC141 001 J784S4XG01EVM

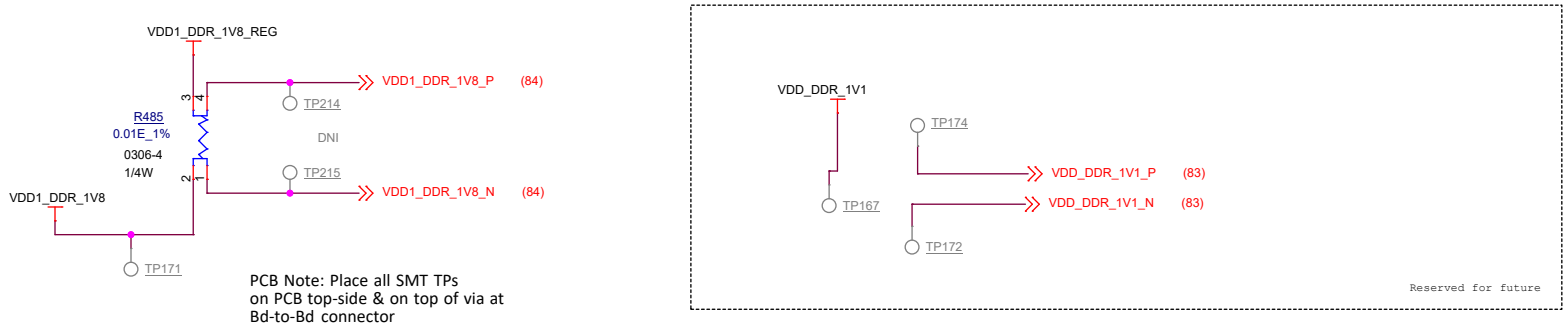
Rev
E2A

Date: Monday, June 20, 2022

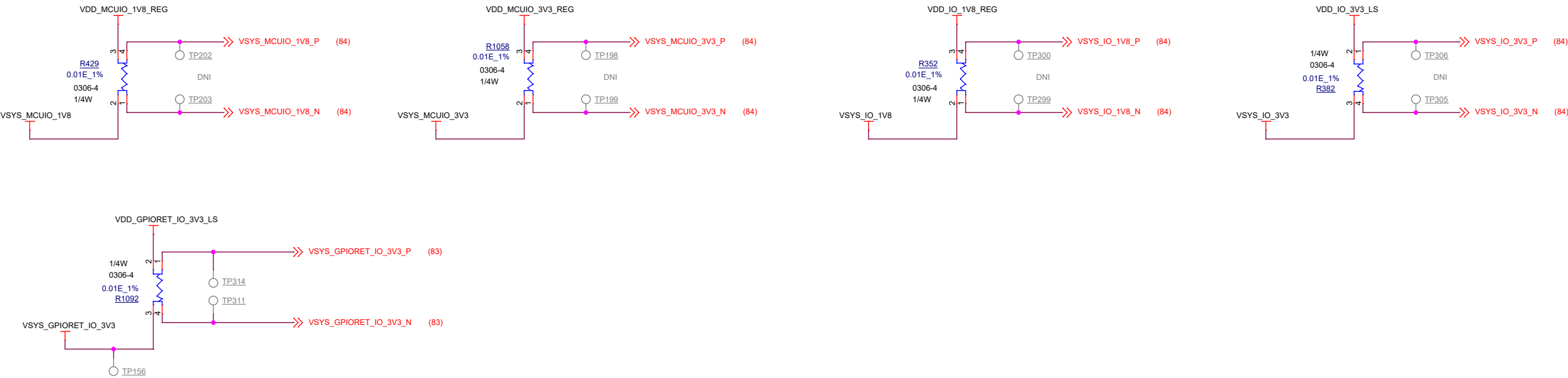
Sheet 81 of 88

EVM development & evaluation test circuitry

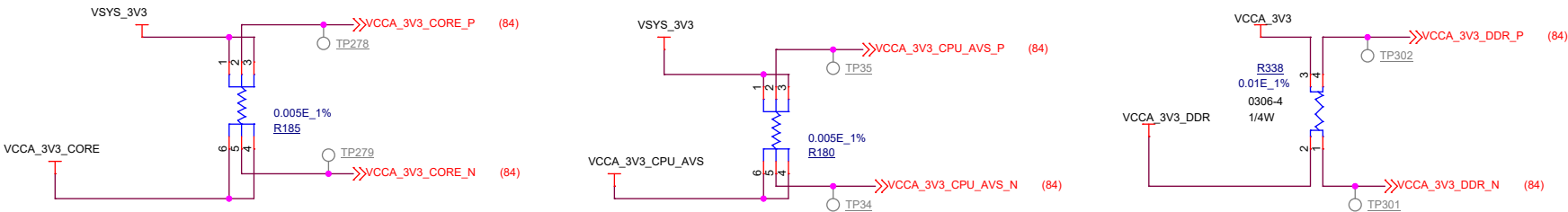
LPDDR4 SDRAM Current Sense Resistors



Peripheral Current Sense Resistors

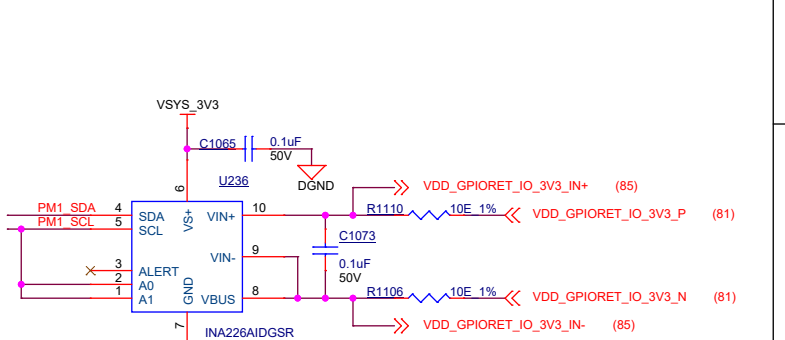
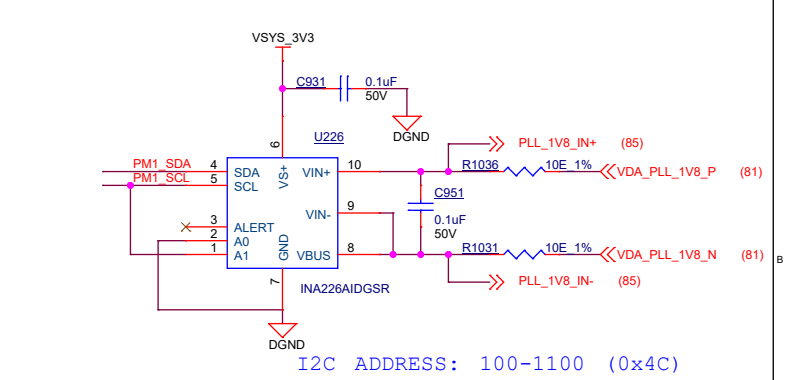
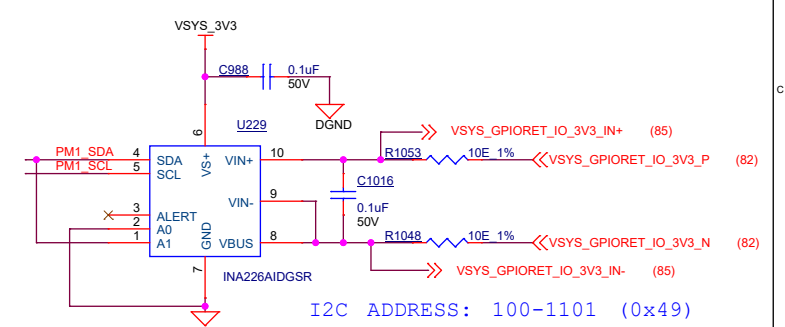
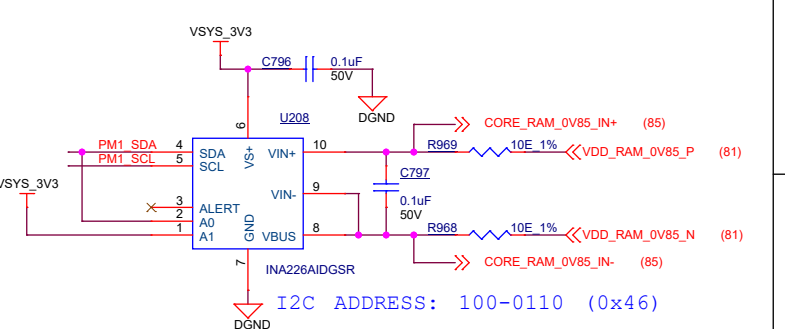
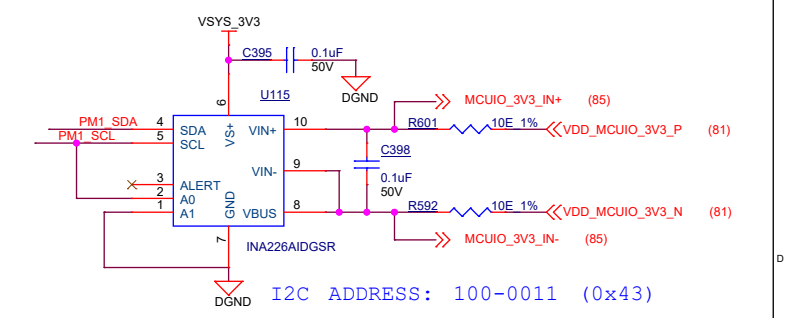
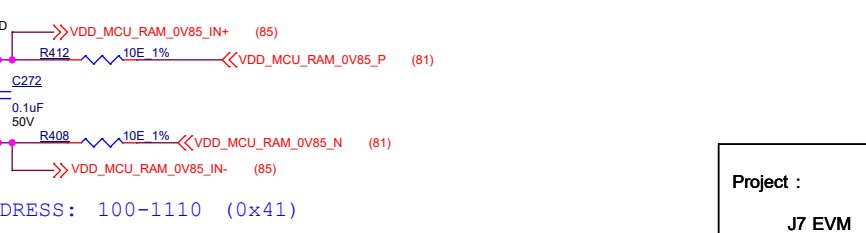
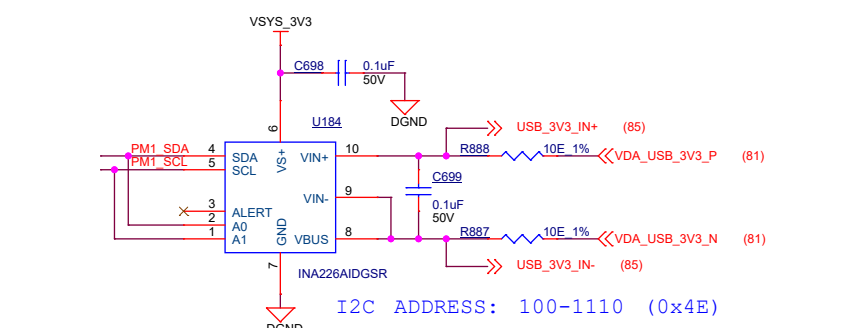
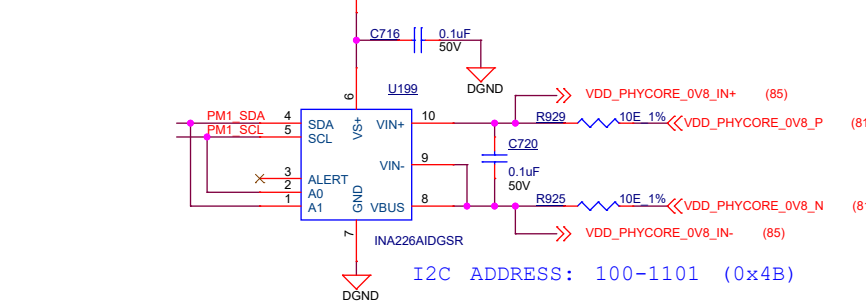
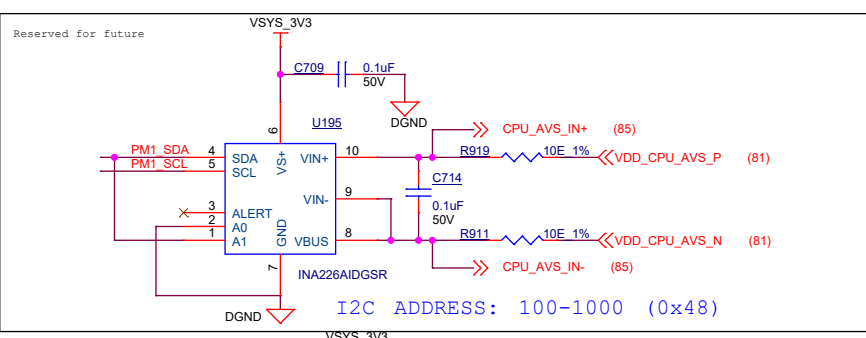
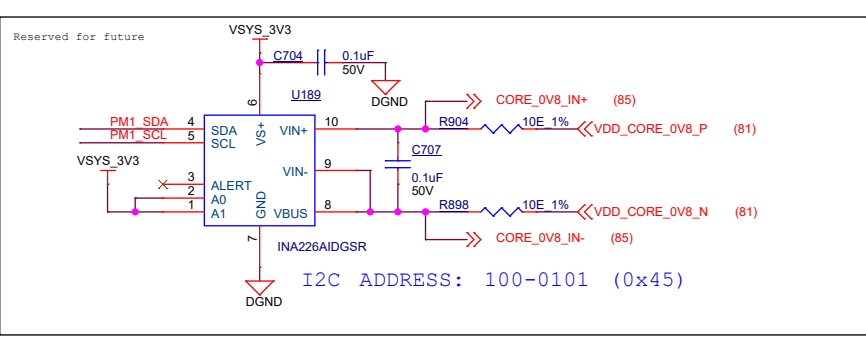
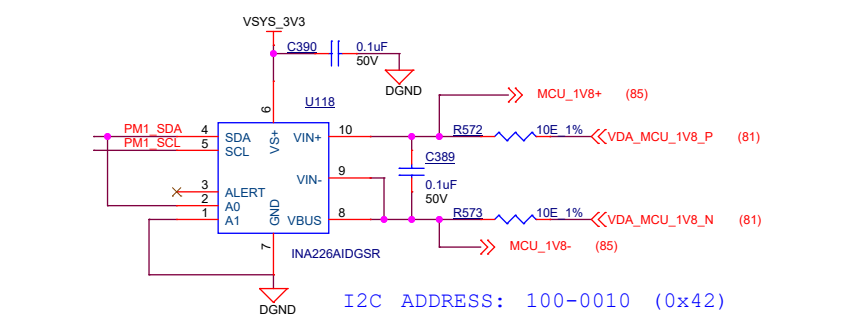
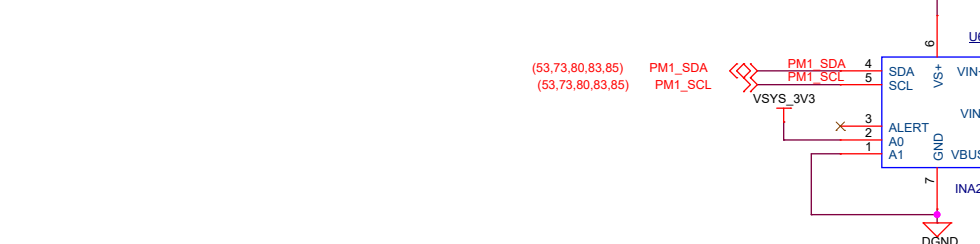
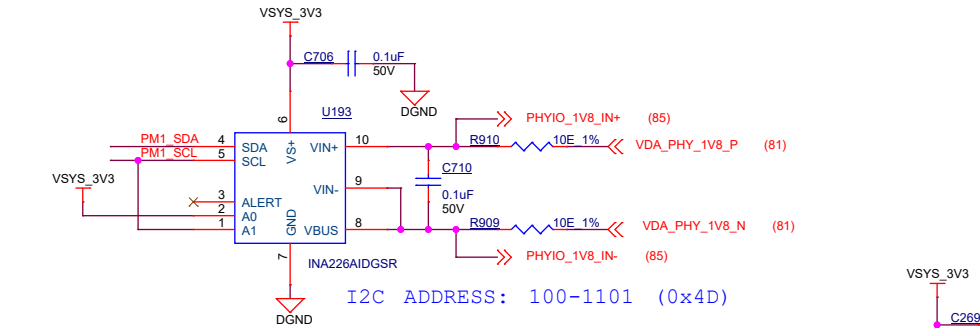
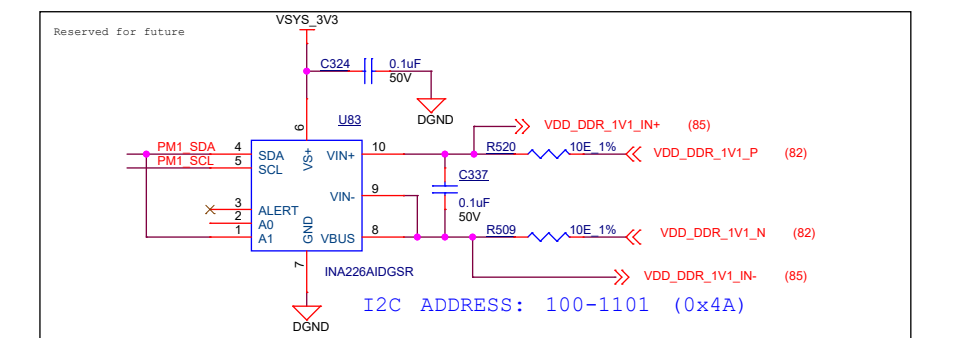
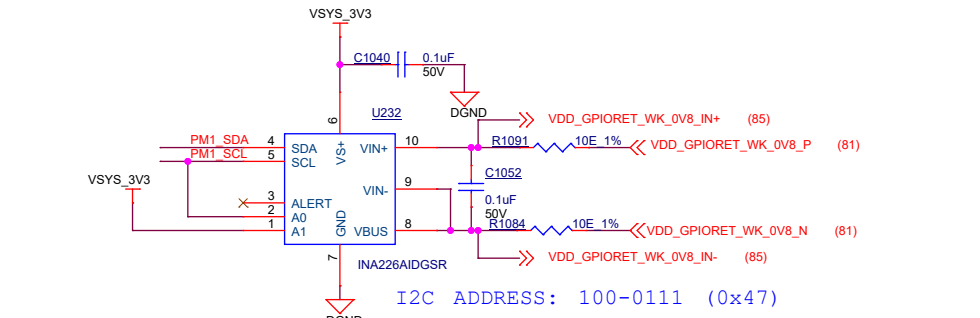
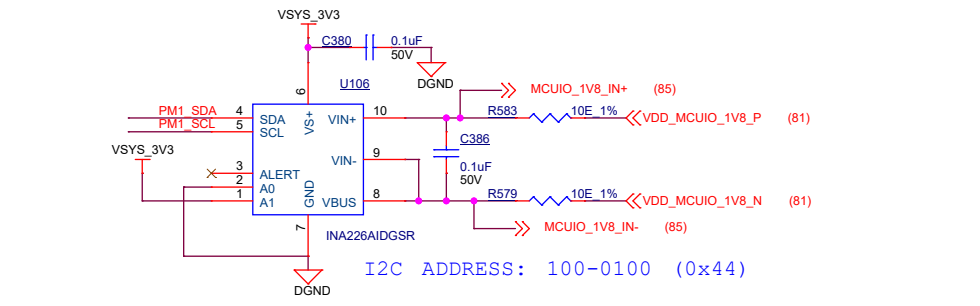
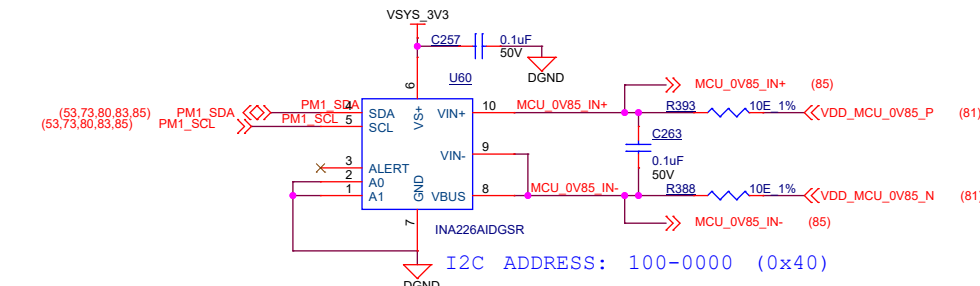


CORE, AVS and DDR input supply sense resistors



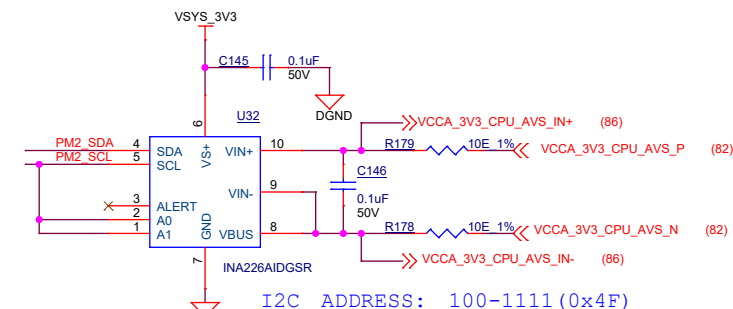
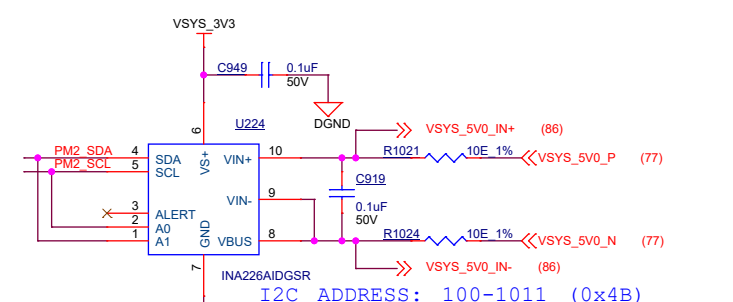
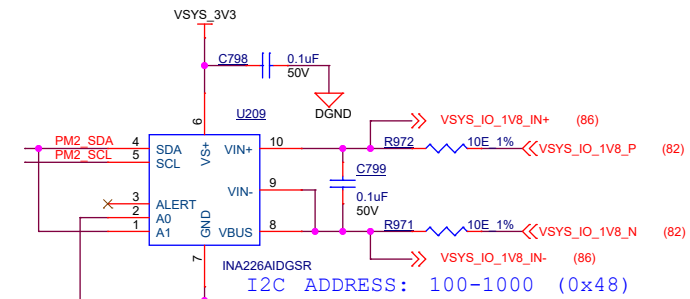
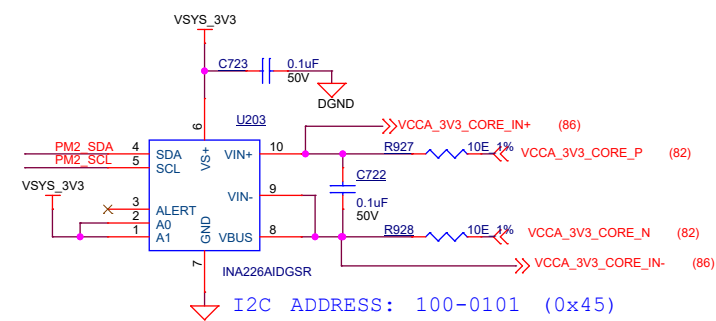
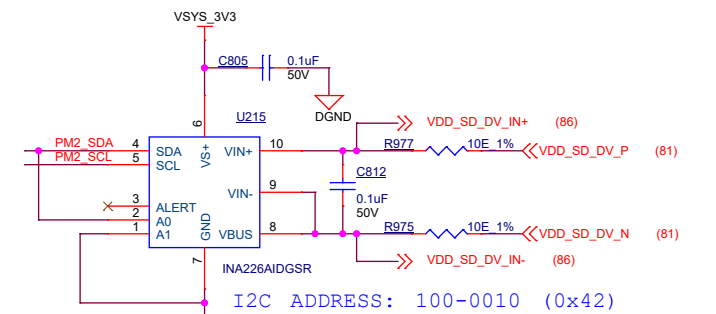
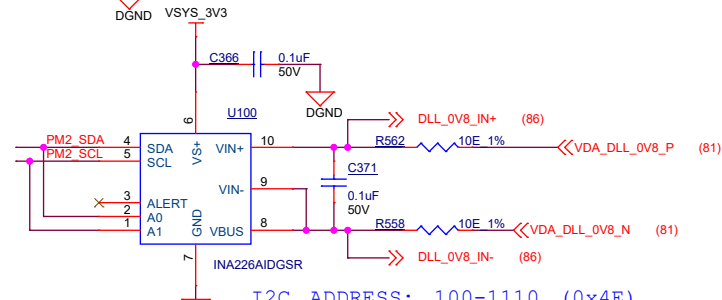
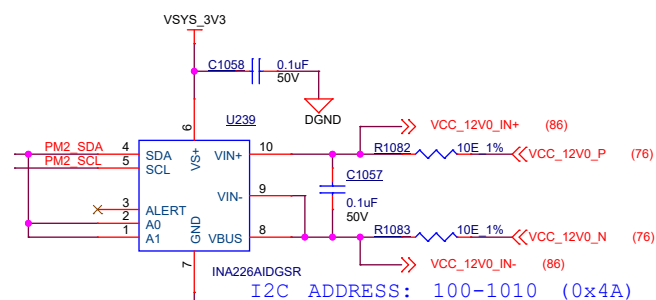
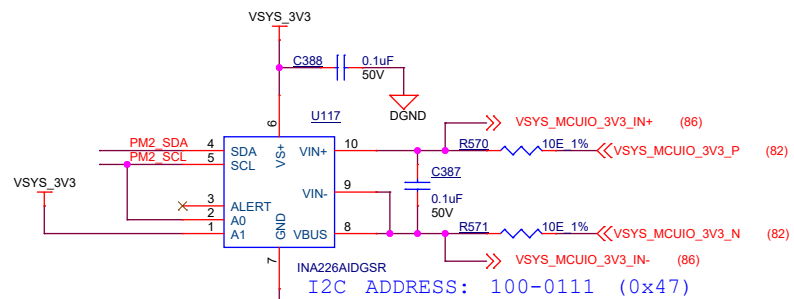
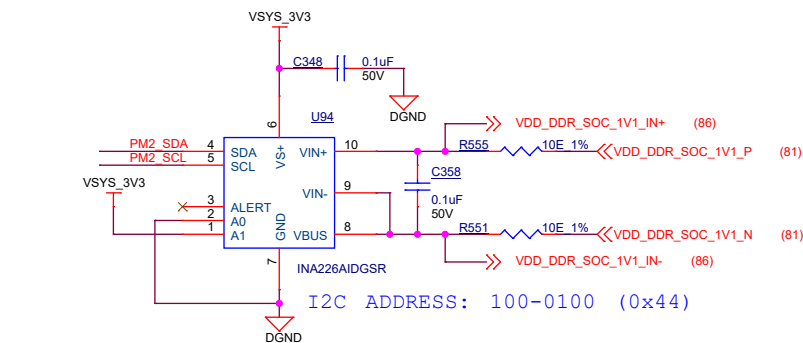
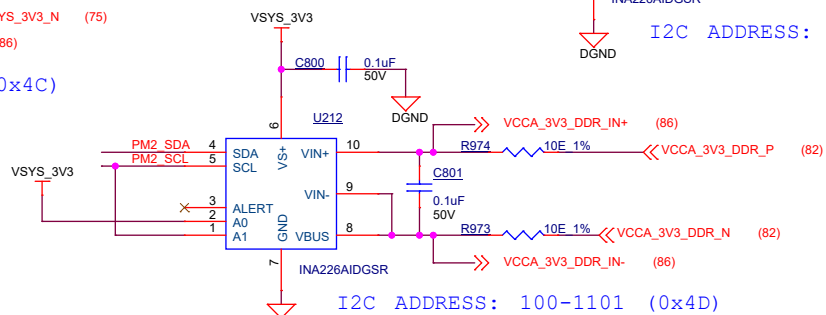
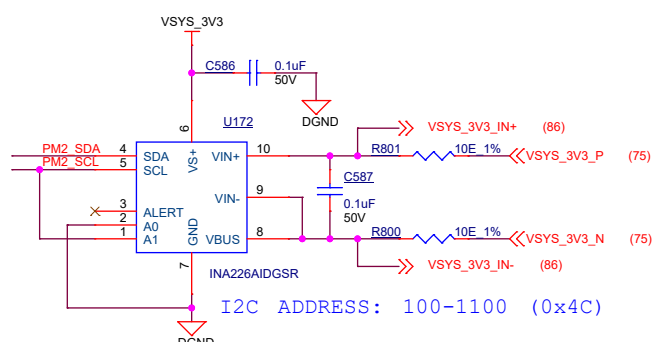
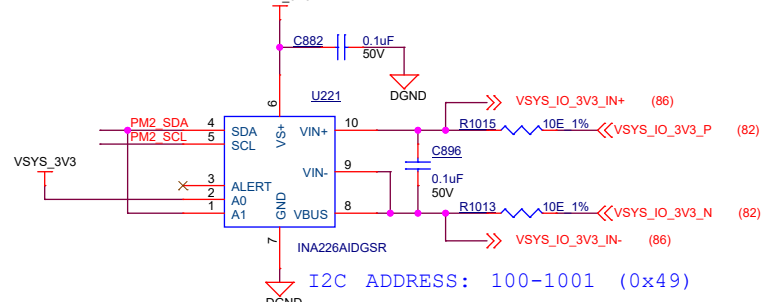
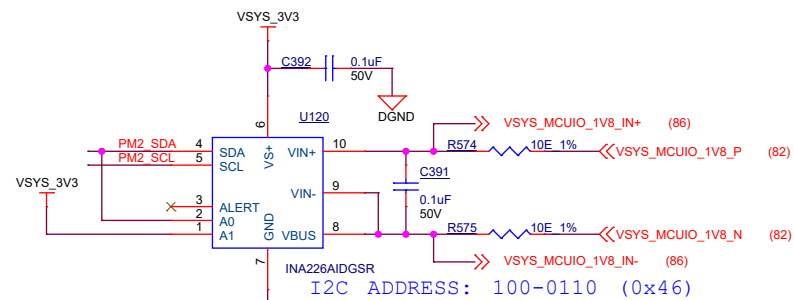
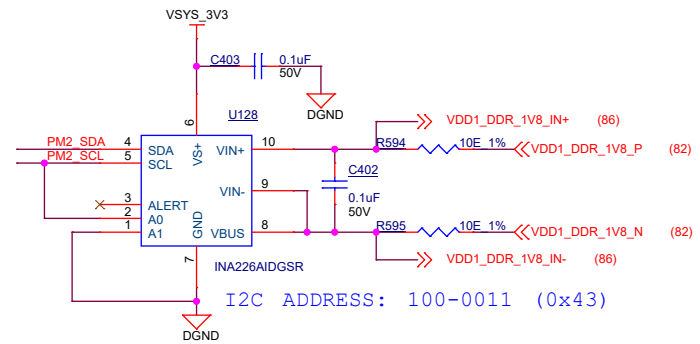
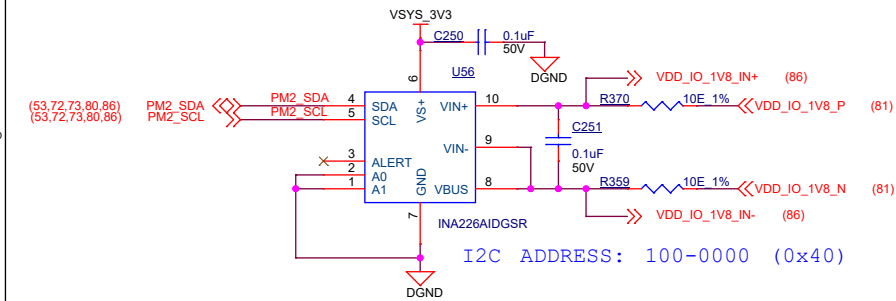
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible - so functionality and performance should not be impacted with either INA


CURRENT MONITORS #1



Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

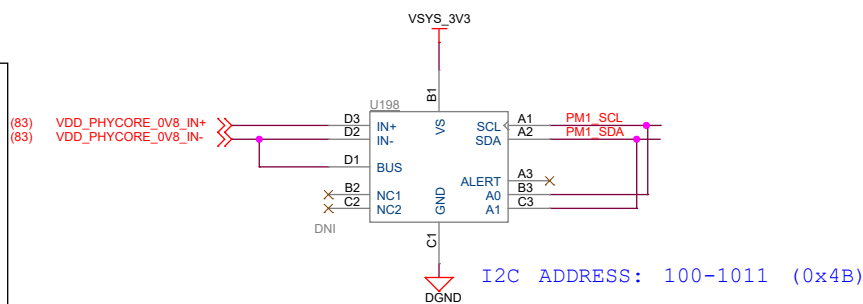
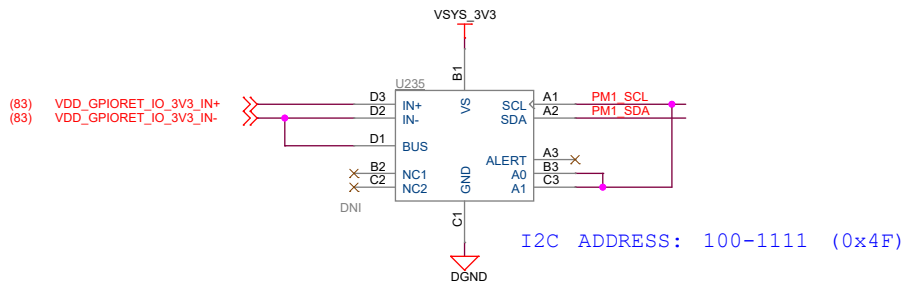
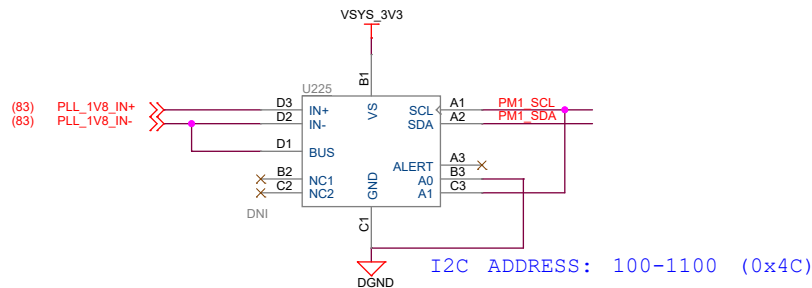
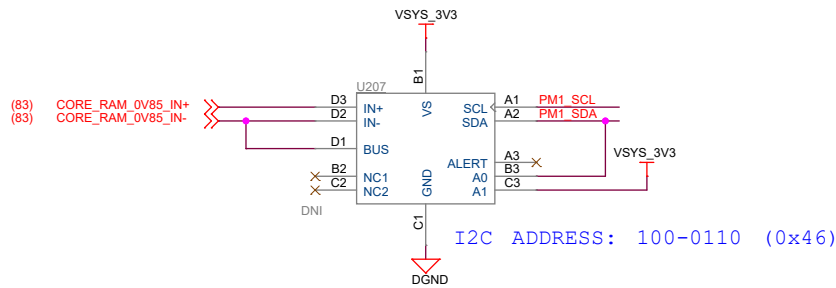
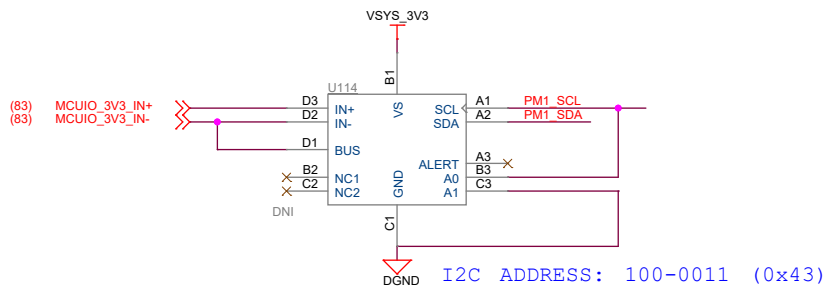
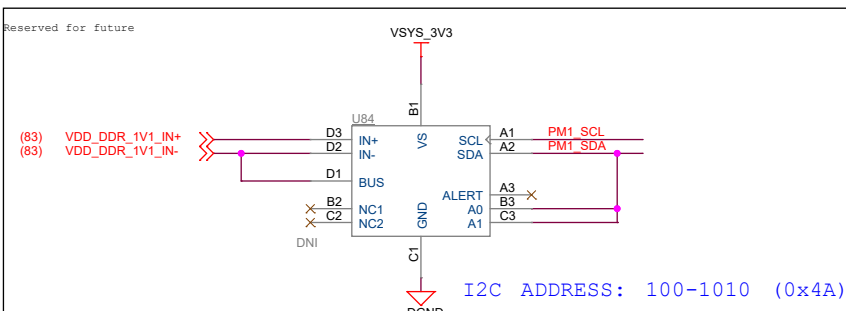
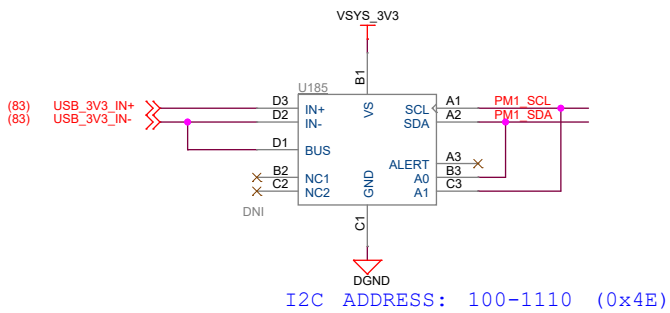
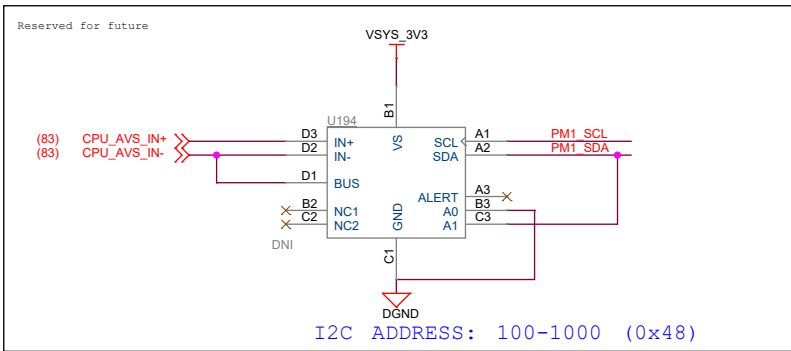
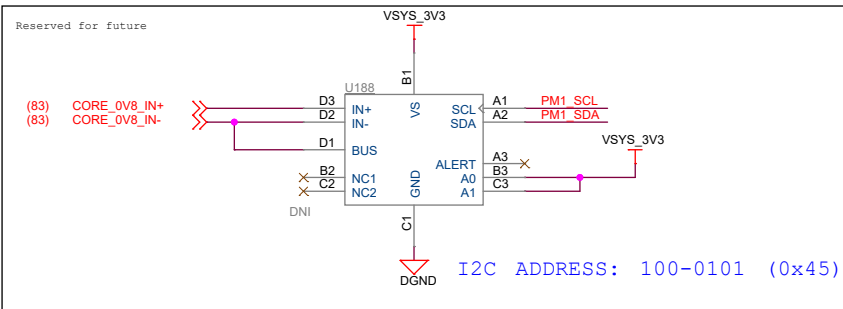
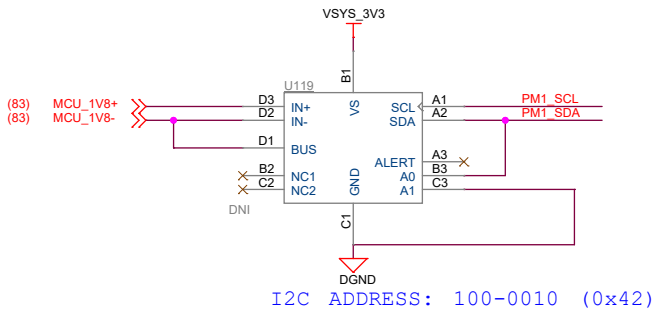
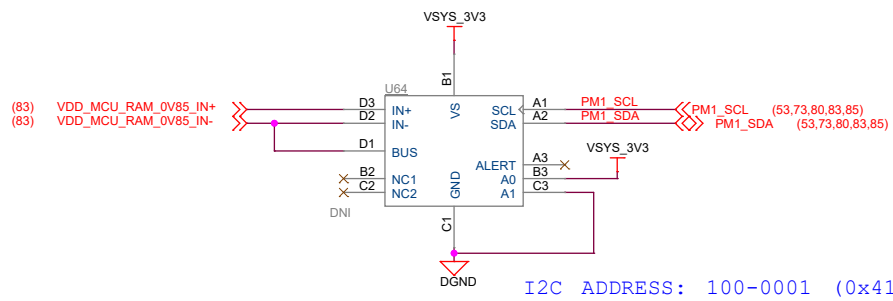
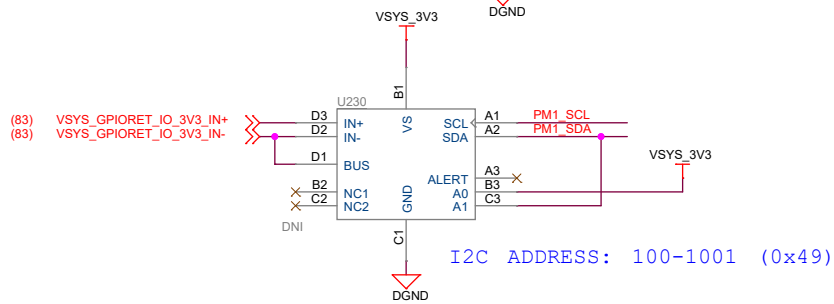
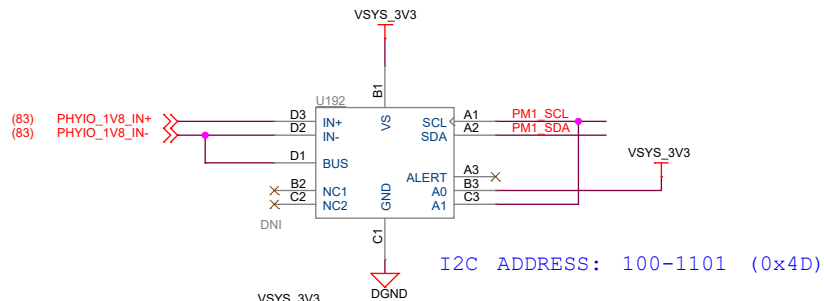
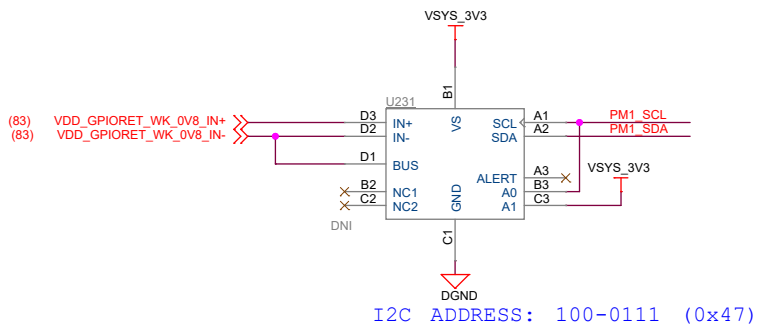
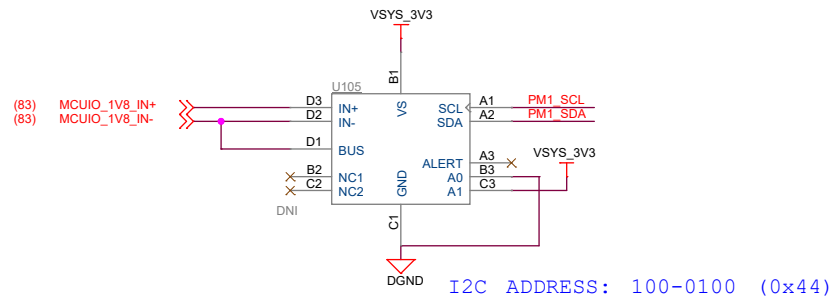
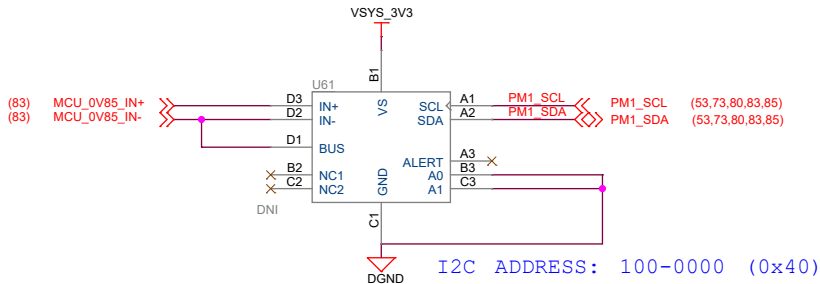
CURRENT MONITORS #2



Project : J7 EVM		Title CURRENT MONITORS #2			
		Size	PROC141 001 J784S4XG01EVM	Rev	
		C		E2A	
		Date: Monday, June 20, 2022		Sheet	84

Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA231



Project :

J7 EVM



Title
CURRENT MONITORS#1- INA231

Size
C
PROC141 001 J784S4XG01EVM

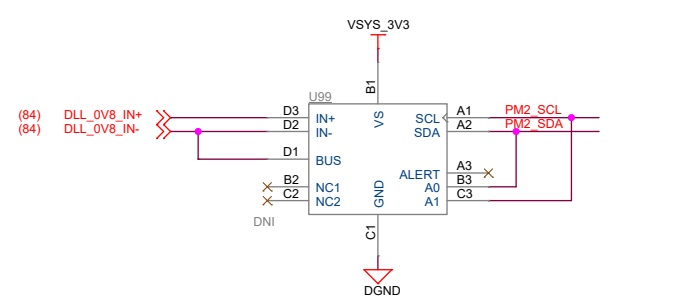
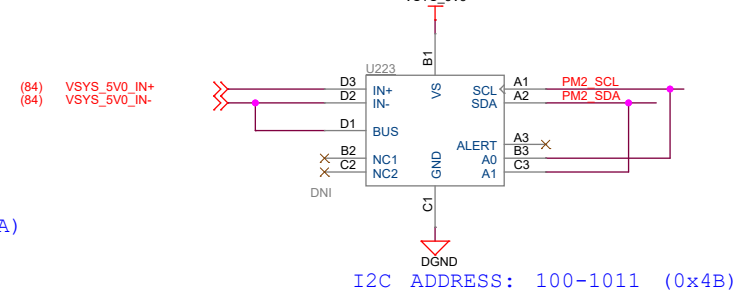
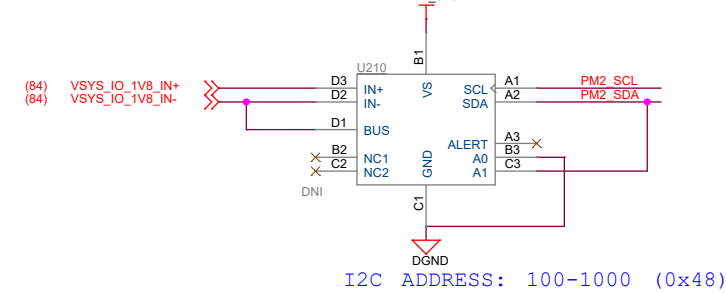
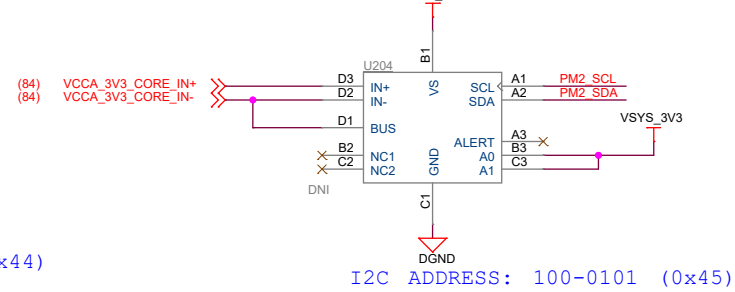
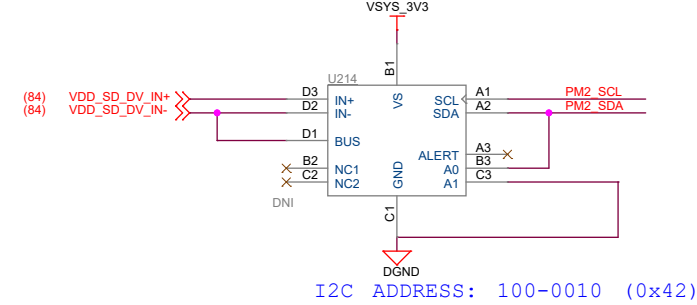
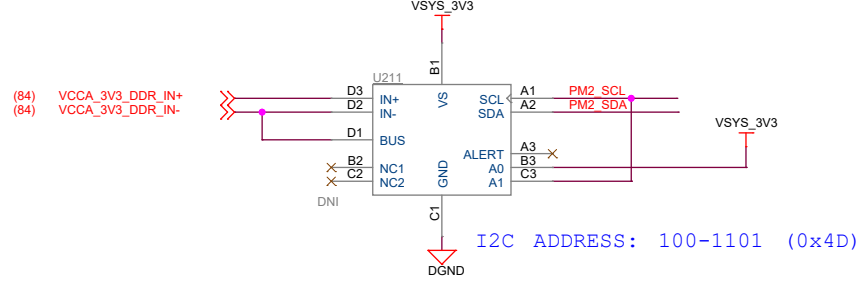
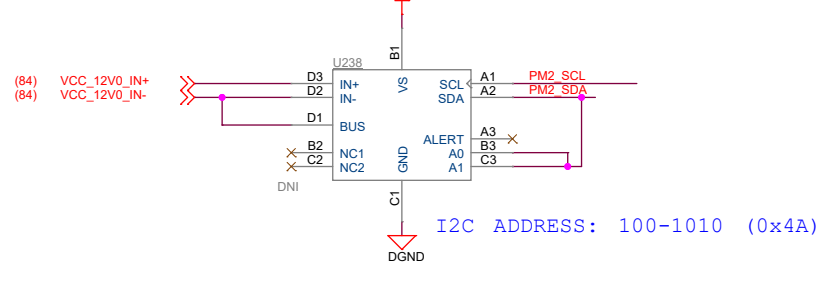
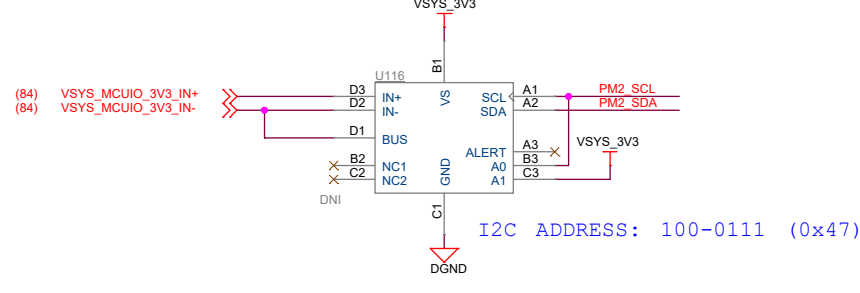
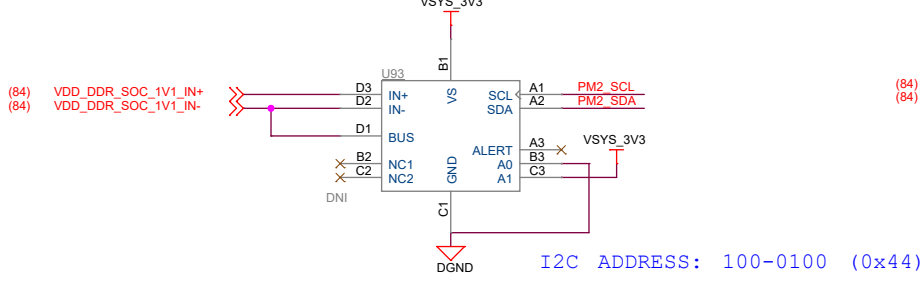
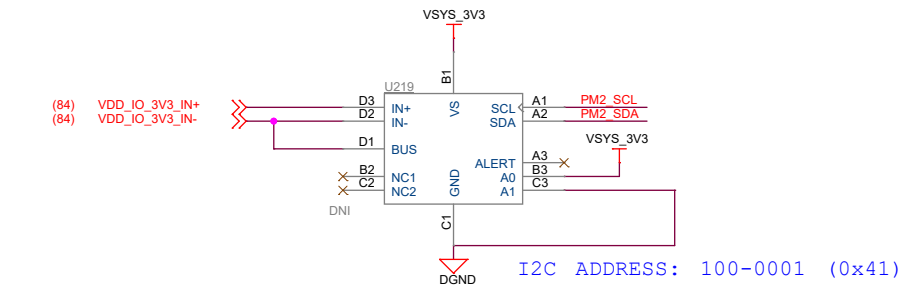
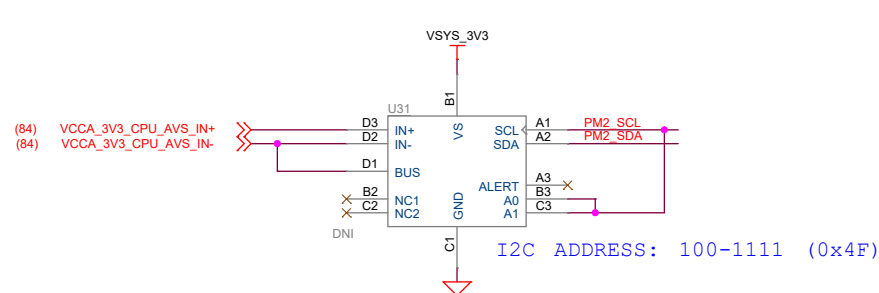
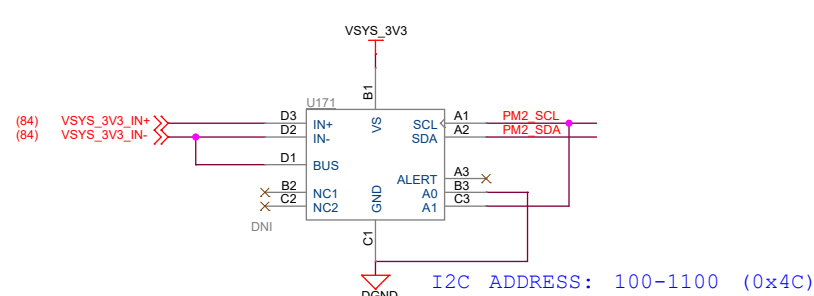
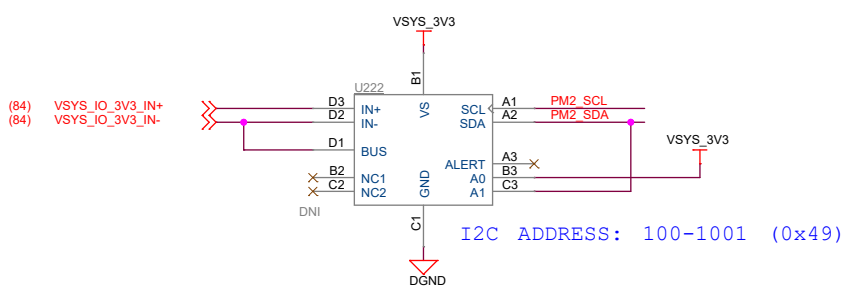
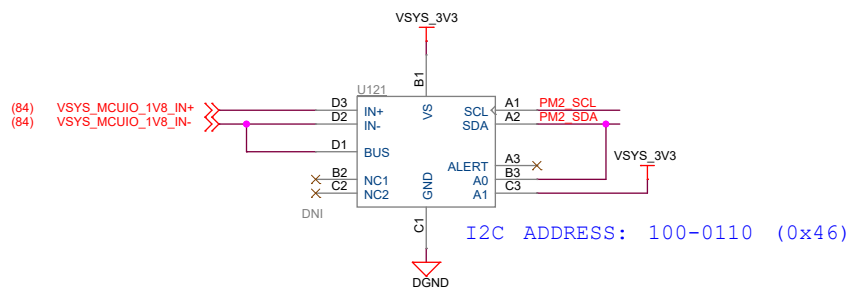
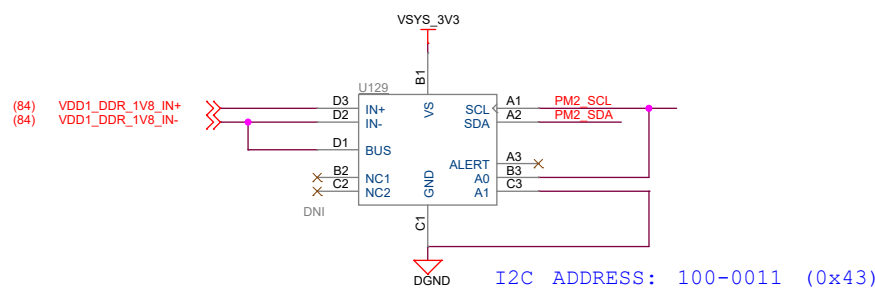
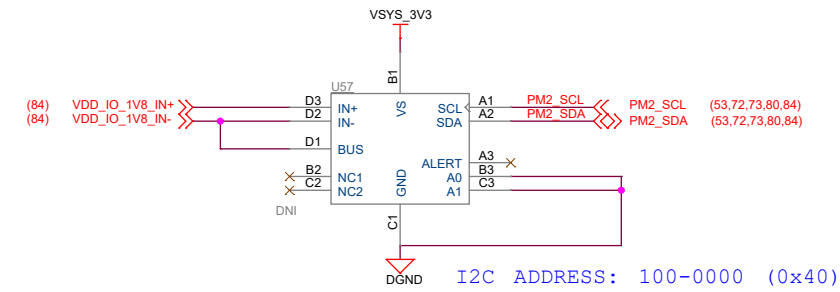
Date: Monday, June 20, 2022

Sheet 85 of 88

Rev
E2A

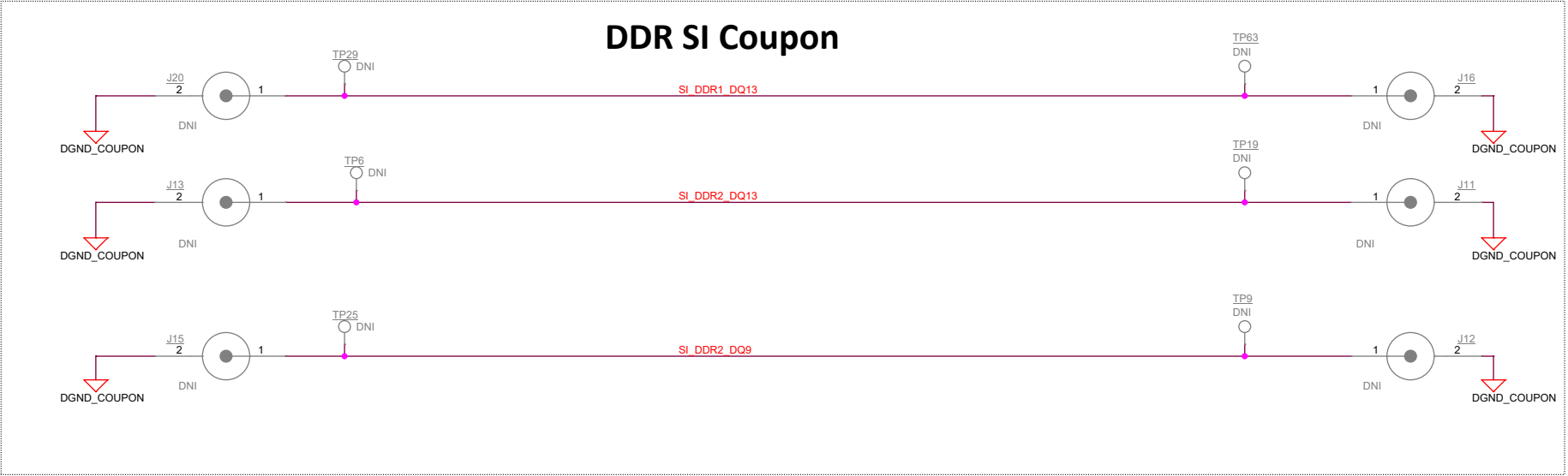
Note: The design supports current/voltage measurements using either INA226 or INA231. The EVM will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA231



SI_SIMULATION_COUPON_BD

Test coupon not part of EVM design, to be used for TI test only

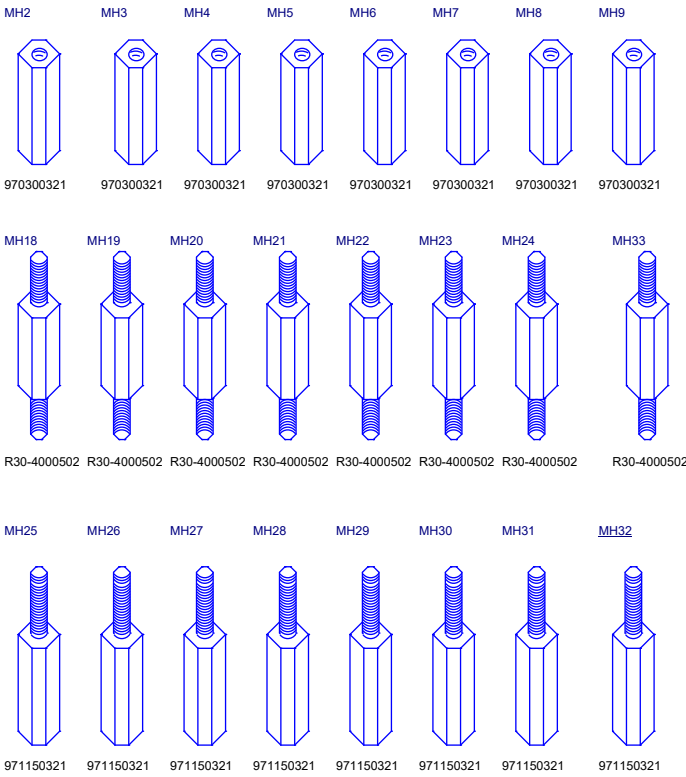


HARDWARE SCHEMATICS

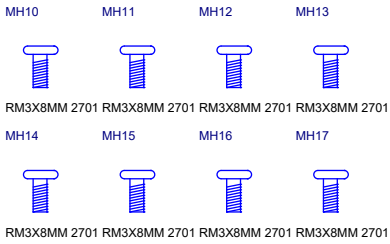
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

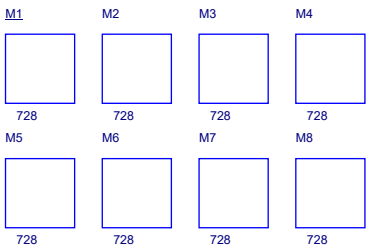
STANDOFFS



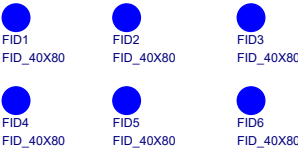
SCREWS



RUBBER FEET



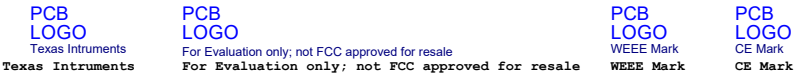
FIDUCIALS



CPB BARE PCB



LOGOs



LABELS

Board Serial No.



Assembly Revision.



EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001:Soldered GP SoC	J784S4XG01EVM
002:Soldered HS SoC	J784S4XH01EVM
003:Socketed SoC	J784S4XS01EVM

SOCKET



HEAT SINK

TBD

PROCESSOR



Project :
J7 EVM



Title		
HARDWARE SCHEMATICS		
Size	Rev	
C	PROC141 001 J784S4XG01EVM	E2A
Date: Monday, June 20, 2022		Sheet 88 of 88