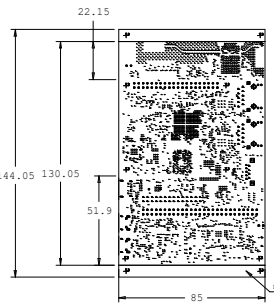
REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

FABRICATION NOTES:

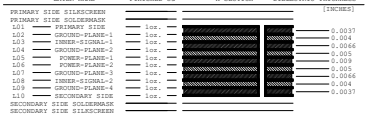
1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012D, CLASS 2; PER IPC-4011.
2. MATERIALS:
   1. LAMINATE AND PREPREG (M-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126. (NOM.TG 170)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED, ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 35um (1 OZ.). FOR OUTER LAYERS 35um (1 OZ). COPPER WEIGHT IS TO BE CONSIDERED "FINISHED". THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 4012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.150mm DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125mm.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE NEUTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. BOARD FINISHED SHALL BE ACCORDING TO IPC-4012D CLASS 2.
7. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
8. PLATING:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE HASL, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. TENTING OF VIAS IS ACCEPTABLE. ALL COMPONENT HOLES SHALL BE COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES THAN SHALL BE 0.08(0.003") THEN SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE RED.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN INK ON EXPOSED PADS OR SOLDERABLE AREAS. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN INK IS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20um (0.00079"), INCASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM (0.00047") AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM (0.0006").
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANCE TO IPC4011, CLASS 2.
9. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE MENTERED IN SILKSCREEN.
10. TEST REQUIREMENTS:
   1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
11. THERVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
12. TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
13. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
14. FINISHED PCB THICKNESS SHALL BE 0.062" +/-10%.
15. MIN TRACE WIDTH/SPACING ON BOARD IS 0.0036"/0.0036".
16. ENSURE THAT UL REGISTERED E-FILE NUMBER SHALL BE PRINTED ON THE PCB SILKSCREEN.



IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	EDGE COUPLED MICROSTRIP	S1,L10	4.25	7.15	100	L2,L9
02	EDGE COUPLED STRIPLINE	L3,L8	3.7	7	90	L2/L4/L7/L9
03	EDGE COUPLED MICROSTRIP	S1,L10	5.2	4.3	90	L2,L9
04	EDGE COUPLED STRIPLINE	L3,L8	3.7	4.3	90	L2/L4/L7/L9
05	STRIPLINE	L3,L8	5.2	NA	60	L2/L4/L7/L9
06	STRIPLINE	L3,L8	9.6	NA	50	L2/L4/L7/L9
07	MICROSTRIP	S1,L10	5.8	NA	50	L2,L9
08	BIPLANAR	L5	16	14	50	L4
09						
10						
11						

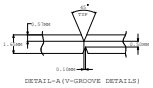
LAYER STACKUP



DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY.
-	8.0	+3.0/-3.0	PLATED	3943
+	28.0	+3.0/-3.0	PLATED	9
x	32.0	+3.0/-3.0	PLATED	2
*	36.0	+3.0/-3.0	PLATED	68
▲	40.0	+2.0/-2.0	PLATED	4
♦	60.0	+3.0/-3.0	PLATED	104
■	64.0	+3.0/-3.0	PLATED	4
●	80.0	+3.0/-3.0	PLATED	2
▶	92.0	+2.0/-2.0	NON-PLATED	2
▼	92.0	+3.0/-3.0	NON-PLATED	4
✱	108.0	+3.0/-3.0	NON-PLATED	10
⊗	126.0	+3.0/-3.0	NON-PLATED	4
◥	48.0x20.0	+3.0/-3.0	PLATED	4
◀	62.0x24.0	+2.0/-2.0	PLATED	2
◆	68.0x36.0	+3.0/-3.0	PLATED	4
▬	82.0x24.0	+2.0/-2.0	PLATED	2



DETAIL-A(V-GROOVE DETAILS)
SCALE:NTS

MISTRAL SOLUTIONS PVT.LTD.,
#60, ADARSH REGENT, 100' FEET RING ROAD,
DOMLUR EXTENSION, BANGALORE 560 071.

MISTRAL

PCB,
SK-AM64 BOARD

	APPROVALS	DATE	SIZE	DRAWING NO.	REV
DRAWN	UD	150622	D	PROC100	A
CHECKED	ZA	150622			
APPROVED	KD	150622	SCALE:NONE	FILE NAME:	SHEET 1 OF 17