

AM69 Processor Starter Kit

TABLE OF CONTENTS

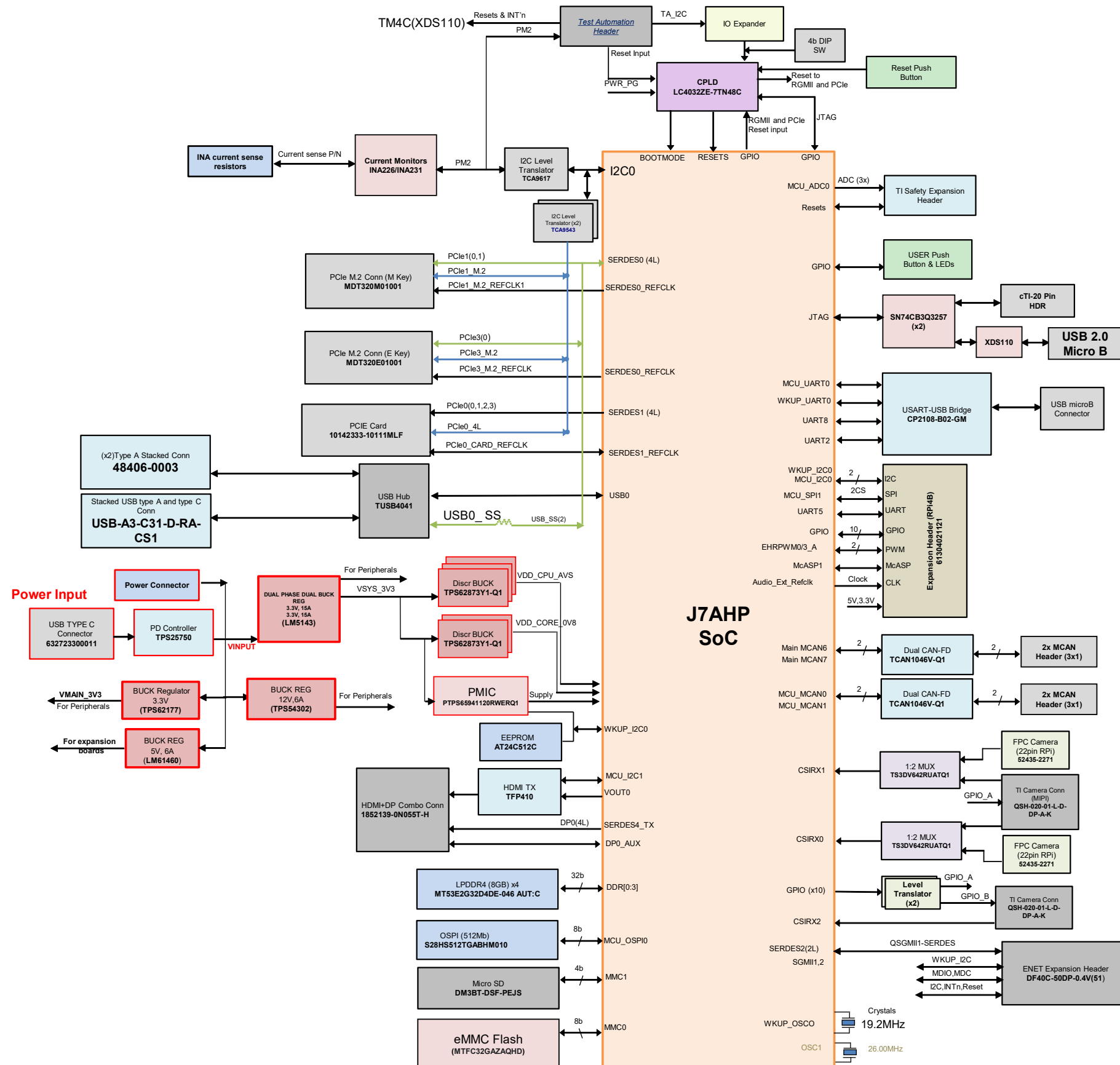
PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	SYSTEM BLOCK DIAGRAM
04	3-Phase DUAL PMIC PDN-0B DIAGRAM
05	Power Flow Diagram
06	I2C Tree
07	I2C TABLE
08	GPIO MAPPING TABLE
09	SOC : CSI & DSI INTERFACE
10	SOC : SERDES0 INTERFACE
11	SOC : SERDES1 INTERFACE
12	SoC: LPDDR4 - DDR0
13	SoC: LPDDR4 - DDR2
14	SoC: LPDDR4 - DDR1
15	SoC: LPDDR4 - DDR3
16	SOC: OSPI FLASH
17	SOC: MCU & MAIN GENERAL IO, OSC CLKS
18	SOC: GENERAL IO
19	SOC: MCU RGMII / MMC[0:1] / ADC
20	SOC: DEBUG and XDS110 MUX
21	SOC: USB2.0
22	SOC: ANALOG POWER 1
23	SOC: IO POWER 2
24	SOC : DIGITAL POWER 3
25	SOC: GROUND
26	RESET BUTTONS
27	CPLD
28	Board ID EEPROM & 40 Pin EXP Header
29	eMMC FLASH
30	Micro SD CARD INTERFACE
31	USB3.0 HUB

PAGE	CONTENTS
32	USB 3.0 TYPE-A CONNECTORS - 1
33	USB 3.0 TYPE-A CONNECTORS - 2
34	USB 3.0 TYPE C INTERFACE
35	PCIe_M.2_INTERFACE(M Key)
36	PCIe_M.2_INTERFACE(E Key)
37	PCIe x4 Card Slot
38	MCU GB ETHERNET
39	CSI MUX - DATA
40	CSI2 EXPANSION CONNECTOR
41	CSI2 FPC CAMERA CONNECTORS
42	DISPLAY PORT INTERFACE
43	DVI/HDMI TRANSMITTER
44	ENET EXPANSION CONNECTOR
45	CAN TRANSCEIVERS #2-MAIN DOMAIN
46	QUAD PORT CONSOLE
47	XDS110 DEBUGGER
48	TEST AUTOMATION HEADER
49	Power Input
50	POWER SUPPLY #1
51	POWER SUPPLY #2
52	POWER SUPPLY #3
53	HCPS A - VDD CPU
54	HCPS A - VDD CORE
55	SOC PMIC
56	SOC LDO's
57	SOC CURRENT SENSE RESISTORS
58	CURRENT MONITORS - INA226
59	CURRENT MONITORS - INA231
60	PMIC SUPPORT CIRCUIT
61	RESERVED
62	SK NOTES & ACCESSORIES

REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	08 AUG 2022	Drafted from J7ES SK Rev B and J7AHP EVM version E3	Mistral Design Team		
	22 AUG 2022	Internal Review comments updated	Mistral Design Team		
	26 AUG 2022	1. I2C Instance mapping updated as per TI block diagram. 2. UART mapping updated. 3. CSI2 is now connected to a separate TI connector.	Mistral Design Team		
	30 AUG 2022	1. EXP_3V3 and VSYS_5V0 regulator split to separate regulators from one dual channel regulator. 2. 12V0 controller replaced with a regulator part LM73606-Q1. 3. Additional power header added J124.	Mistral Design Team		
	02 SEP 2022	Replaced external power measurement circuit with a simple header option.	Mistral Design Team		
	19 SEP 2022	1. EXP_3V3 removed and the peripherals are now sourced from VSYS_IO_3V3. 2. L21 and L22 updated to support 35A load current. C116, C92,C124,C106,C120, C629, C101, C82, C84, C126, C58, C112, U178, U24, U180, U27 modified to support the new load. 3. Added GPIO expander U3155 and U3169 for GPIO control.	Mistral Design Team		
	20 SEP 2022	Updated GPIO mapping as per TI review comments and replaced U3155 from TCA6416 to TCA6408ARGTR	Mistral Design Team		
	23 SEP 2022	Updated TI review comments: 1. Pull Ups R3828, R3829, R5946, R5953, R5950, R595, R3433 connected to VSYS_IO_1V8 2. Added U3170 and MCU_CLKOUT0 and CSI_RSTz moved to U3170	Mistral Design Team		
	7 OCT 2022	Updated TI review comments: 1. Connected VDD_SD_DV_PMIC to SD card regulator using 0E resistor (R6108) 2. CSI2_BUFF_EN is made ground 3. CAM0_INT#, CAM1_INT# is pulled to 1.8V 4. Changed part numbers of J87 and J88 to 52435-2271	Mistral Design Team		
	8 OCT 2022	Updated TI review comments: 1. Provided optional connection of SEL_SDIO_3V3_1V8n from PMIC GPIO6 2. Added Kelvin sensing for VDD_CORE_0V8 and VDD_CPU_AVS 3. Deleted R205 and R201	Mistral Design Team		
	11 OCT 2022	Schematic Back Annotated	Mistral Design Team		
	31 OCT 2022	Organized VDD_CORE_0V8 Dcaps (pg 24), HCPS-A (53) & HCPS-B (pg 54) remote sense notes for readability	TI Design Team		

SYSTEM BLOCK DIAGRAM



Project :
TDA4VM Edge AI Kit



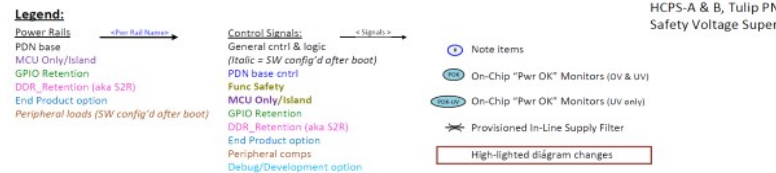
Title	BLOCK DIAGRAM
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Size	<Core Design>	Rev	
C		E1	
Date:	Monday, October 17, 2022	Sheet	3 of 62

PDN Recommended for New Designs

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3H

(All SoC PN variants: TDA4AP/VP/AH/VH)
(Power Rail & GPIO Mapping Overview)



- Notes:**
- Functional Safety requires monitoring all "safety critical" power rails (i.e. VVS_V3 input, key SoC supplies) that could cause severe system failures. This classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal DV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMON_U, VMON_V) can be used to extend SoC's DV/UV monitoring to a few board level power rails if desired (i.e. load switch V_o = VDD_IO_V3). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD card), VPP_MCU, VDDA_3P3_USB & VDD_I_LPDDR4_V1B.
 - Load Switches (LDSw) have been used to create VDD_MCUIO_V3, VDD_GPIORET_V3 & VDD_IO_V3 power rails from VCCA_V3 to provide the following benefits:
 - A) Correct SoC power supply sequencing by using PMIC resources (GPIO signals & power resources outputs) with desired start-up & shut-down timing delays per NVM settings.
 - B) PMIC monitoring of VCCA Over Voltage (+1% to +10%) allows PMIC to disconnect 3.3V power rails from SoC if OV condition is detected.
 - C) Enables low power modes (MCU Only, GPIO_RET & DOR_RET) since the different 3.3V power rails must be disabled independently for different low power modes.
 - D) Connecting VCCA_V3 directly to SoC 3.3V supplies is not recommended since this will leave SoC partially energized for extended periods of time that can negatively impact PoR reliability.
 - PMIC's GPIO_8 has been provisioned to support multiple interface signals. The PMIC PN default function sets GPIO_8 = DISABLE_WDOG function following NVM initialization. This GPIO's default function can be reprogrammed by system SW following SoC boot if another interface signal is needed that is not required for SoC power sequencing.
 - 1. Default: GPIO_8 = DISABLE_WDOG function to operate with EVM's DISABLE_WDOG signal that is latched on rising edge of PMIC's nRSTOUT = H_MCU_POR2_V1B at end of power-up seq. A logic low enables normal watch dog timer operation while a logic high disables watch dog timer following a power up seq.
 - 2. Option1: After system SW boots, SW can reassign GPIO_8 = GPI function to operate with PMIC's MAIN_PWIRGRF_IRQ2_n (asserted high or low) signal. System SW must mask GPIOs before changing GPIO's assigned function. After selecting GPI function, SW must unmask GPI input and select whether the GPI will be either rising or falling edge sensitive. If any Main domain processing supply rail has a fault, the changing logic level on GPIO8 will set internal register bit that is monitored by PMIC's power state machine and cause a transition from Full Active state to MCU Safe state. At the board level, the WDOG_DISABLE & MAIN_PWIRGRF_IRQ2_n signals are "time mux'd" onto GPIO8's input pin by using a tri-state buffer with OE control connected to H_MCU_POR2_V1B. This enables WDOG_DISABLE net to set GPIO8's logic level during power up seq when H_MCU_POR2_V1B = low since buffer is tri-stated. After power up seq, H_MCU_POR2_V1B = high enabling buffer to drive MAIN_PWIRGRF_IRQ2_n logic level into GPIO8 input.
 - 3. Option2: GPIO_8 = WKUP1 function can be selected by SW to operate with SoC's PMIC_PWR_EN1 signal for emulator debug control of PMIC power resources (i.e. enabling VDD_CORE to activate core logic required to support JTAG signaling across the device). Combining board level WDOG_DISABLE & PMIC_POWER_EN1 signals using a resistor network is possible since WDOG_DISABLE pulldown logic level high when switch is closed. Afterwards, switch can be opened and PMIC_PWR_EN1 signal will drive GPIO_8.
 - GPIO Retention (aka GPIO_RET_IO_RET_IO Wake) low power mode requires:
 - A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
 - B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
 - 1. VDD_GPIORET_V3 supplying MCU's VDD_MCUIO_V3 & VDD_MCUIO_V3 wake-up logic
 - 2. VDD_GPIORET_V3 supplying MCU's VDDSHV5_MCU for MCU's 3.3V I/O toggle activity
 - C) PMIC system exits GPIO_RET state upon receiving logic toggles on SoC's MCU monitored IO signals ref to VDDSHV5_MCU supply. Then H_MCU_WAKEIN is SoC's Open-Drain PMIC_WAKEIN, active low signal connected to PMIC_GPIO_4 = WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PMIC system to desired targeted wake up state.
 - D) The Open-Drain Buffer (DVB) VDDSHV5_MCU (Hi-Z state IO when power is Off) connects PMIC_WAKEIN to SoC_PWR_V3Wn net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always-on VCCA_V3 used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DOR_RET) when VDD_GPIORET_V3 is typically disabled.
 - DOR Retention (aka DOR_RET, Suspend-to-RAM, S2R) low power mode requires:
 - A) PMIC PN to assign GPIO_6 = Regulator Enable (REGEN) function with an open-drain output buffer type per NVM default settings. The board level net H_DOR_RET_V1 signal is pulled up to VDD_DOR_V1B & connected to SoC's DOR_RET input. When this input is set high, SoC's EMIF IO buffers are set to high-Z state as part of entering DOR_RET mode.
 - B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DOR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
 - C) After entering DOR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
 - 1. VDD_DOR_V1B supplying both SoC EMIF & SDRAM IO voltages
 - 2. VDD_DOR_V1B supplying SDRAM only
 - D) PMIC system exits DOR_RET upon detecting a CAN_WAKE signal toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DOR_RET mode & restores Full Active processor operation.
 - SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires capability for in-the-field updates, then on-board EFUSE programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's V_o will need a high impedance output. Recommended PNs: TP573101-01, fixed 1.8V TP573118-01 or TLV70118-01. The EN_EFUSE_VPP control signal must be sourced from an SoC GPIO for this Pn (due to limited number of PMIC GPIOs). This allows SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).
 - PDN shows SoC's VDDA_3P3_USB domain supplied from a low noise LDO with a VVS_V3 input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_V3 rail to support USB 2.0 I/F removes a discrete LDO & VVS_V3 input but will negatively impact data eye performance due to higher supply noise causing data eye mask violations.
 - PDN shows SoC's Main domain VDDSHV5 supply being sourced from a dual voltage LDO with a VVS_V3 input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_V3 rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_V3 rail to support SD card operation removes dual voltage, discrete LDO & VVS_V3 input but will restrict data rates to standard 128MB/s with VIO = 3.3V.
 - A discrete FET w/ low V_{th} uses industrial rated Pn or auto qualified voltage translation IC with low VGS or V_{th} is needed to ensure a logic high level output will result with an input min 0.75V (-5% supply tol). Examples shown below:

Work-In-Progress

Modular PDNs support flexible feature sets

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC EFUSE Programming	Discrete LDO	SoC VPP >> No connects
Compliant, USB 2.0 data eye	VPP_EFUSE_V1B	SoC VDDA_3P3_USB >> Filtered VDD_IO_V3
Compliant, High-Speed SD Card	Discrete LDO	SoC VDDSHV5 >> VDD_IO_V3 or VDD_IO_V1B
DOR Retention low power mode	Discrete LDO	[FDRDR_VDD] >> VDD_IO_V1B
MCU GPIO Retention low power mode	Discrete LDO	VDD_I_LPDDR4_V1B
	Discrete LDO	Isolated MCU & Main PDN Schemes: SoC VDD_MCUIO_V3 >> VDD_MCUIO_V1B
	Discrete LDO	Grouped MCU & Main PDN Schemes: SoC VDD_MCUIO_V3 >> VDD_CORE_V1B
	Discrete LDO	Isolated MCU & Main PDN Schemes: SoC VDDSHV5_MCU >> VDD_MCUIO_V3 or VDD_MCUIO_V1B
	Discrete LDO	Grouped MCU & Main PDN Schemes: SoC VDDSHV5_MCU >> VDD_IO_V3 or VDD_IO_V1B
Main GPIO Retention low power mode	Discrete SIS	PMIC_GPIO_10 pulled up to VCCA_V3
	Discrete LDO	PMIC_GPIO_10 pulled up to VCCA_V3
	Discrete LDO	PMIC_GPIO_10 pulled up to VCCA_V3
	Discrete LDO	PMIC_GPIO_10 pulled up to VCCA_V3
	Discrete SIS	PMIC_GPIO_10 pulled up to VCCA_V3

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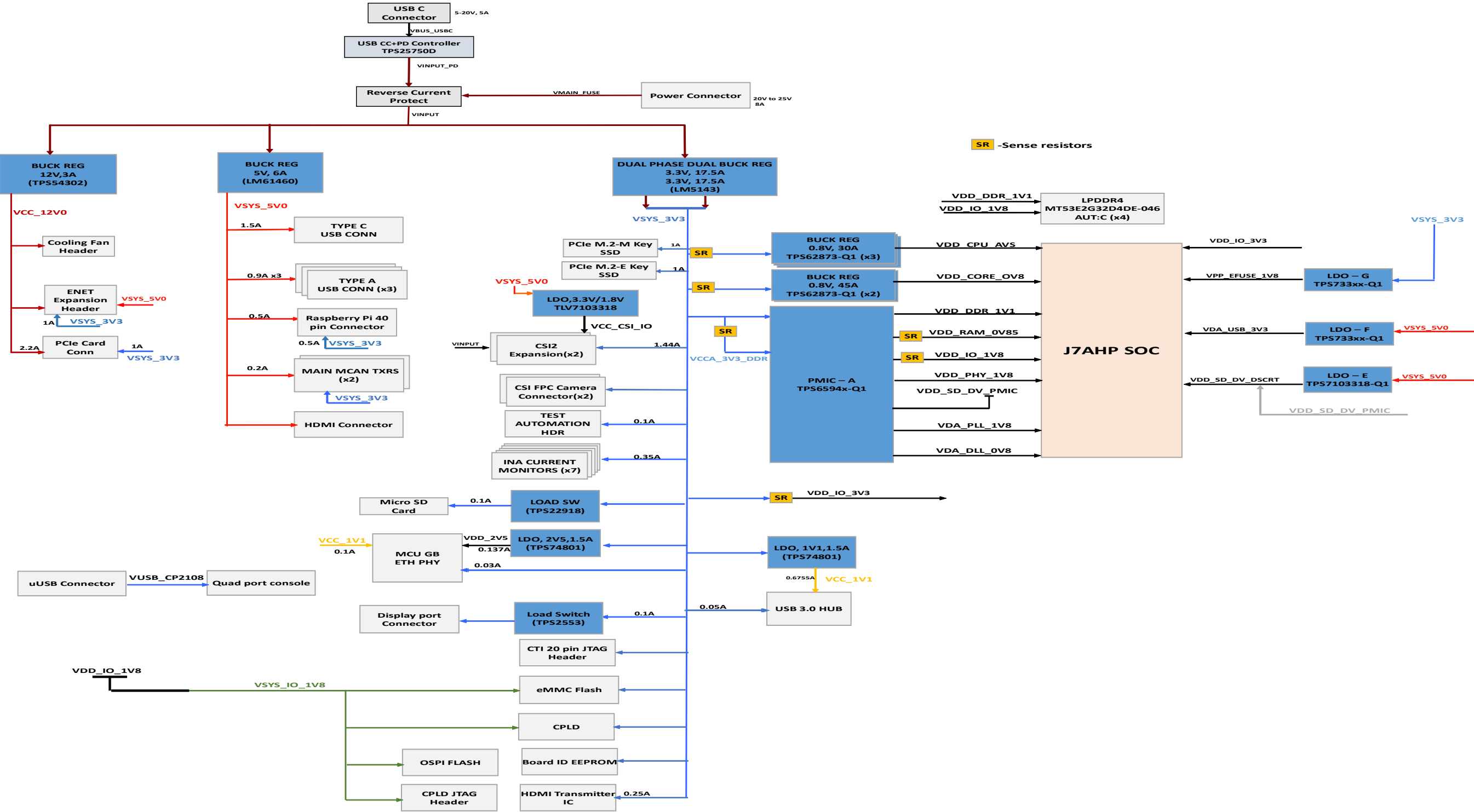
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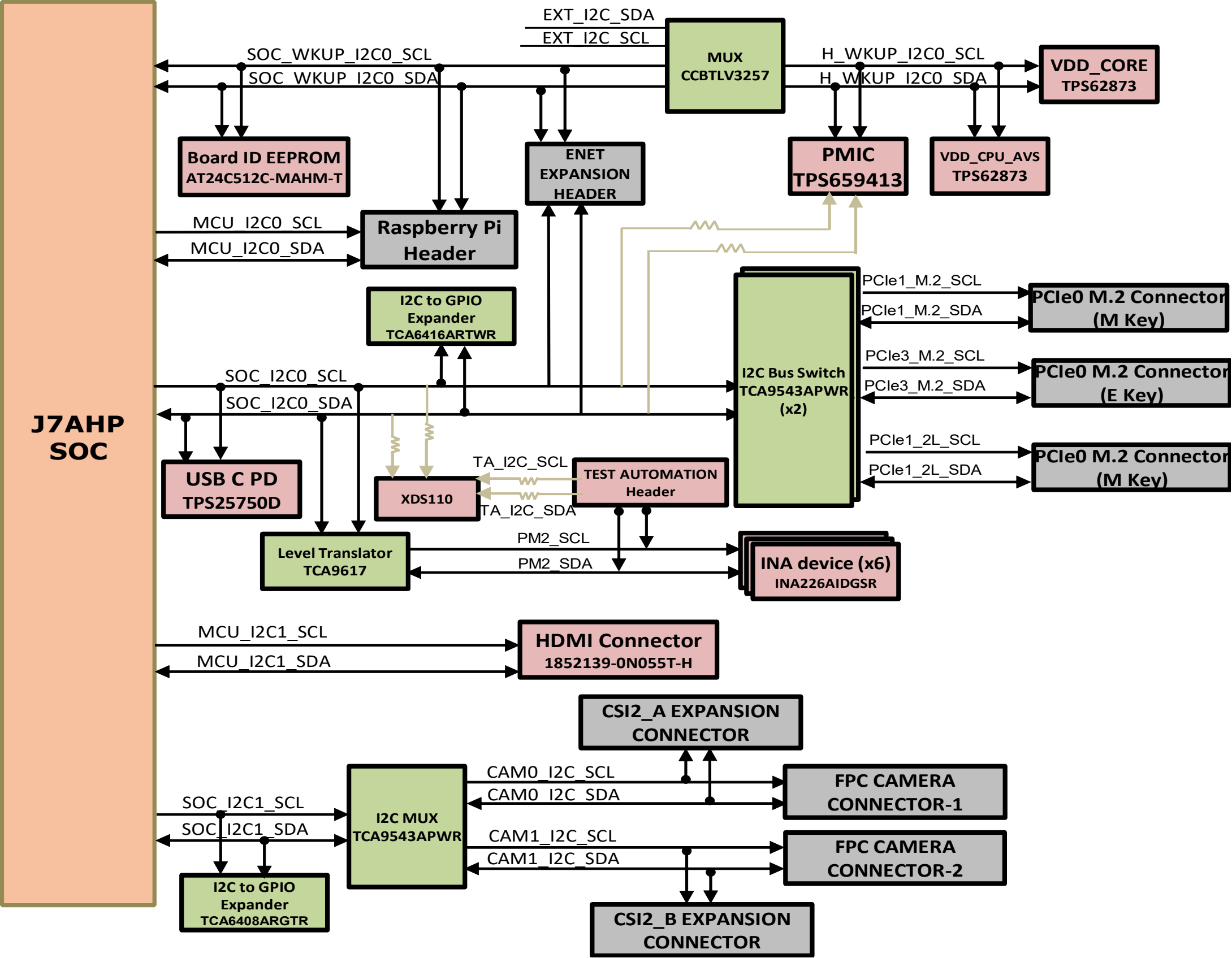
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AM69 SK POWER FLOW DIAGRAM



I2C TREE



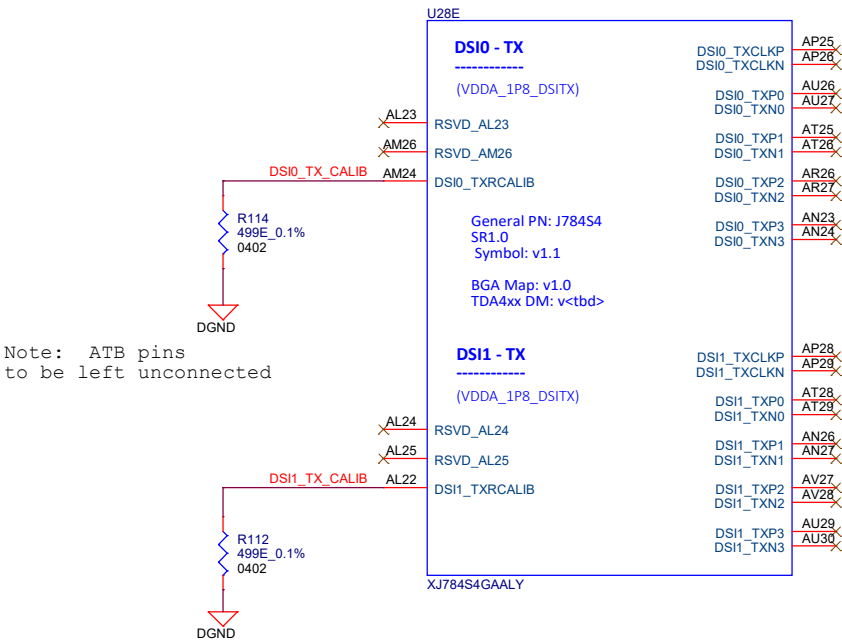
I2C TABLE

AM69 SK I2C Slave Address Table			
SOC I2C Port	Device Description	Part#	I2C Address
WKUP_I2C0	PMIC	TPS6594133ARWERQ1	0x48, 0x49, 0x4A & 0x4B
	VDD_CPU_AVS High-Current Power Stage A	TPS62873Y1QWRXSRQ1	0x40
	VDD_CORE_0V8 High-Current Power Stage B	TPS62873Y1QWRXSRQ1	0x43
	Raspberry Pi Header	61304021121	
	Board ID EEPROM	AT24C512C-MAHM-T	0x51
	ENET Expansion Header	171446-1109	0x57
MCU_I2C0	Raspberry Pi Header	61304021121	
MAIN_I2C0	Test Automation Header	687140183622	
	INA226 device for VCCA_3V3_CORE	INA226AIDGSR	0x45
	INA226 device for VCCA_3V3_CPU_AVS	INA226AIDGSR	0x4F
	INA226 device for VCCA_3V3_DDR	INA226AIDGSR	0x4D
	INA226 device for VDD_RAM_0V85	INA226AIDGSR	0x46
	INA226 device for VDD_IO_3V3	INA226AIDGSR	0x41
	INA226 device for VDD_IO_1V8	INA226AIDGSR	0x40
	PCIe_M.2_Interface M Key	MDT320M01001	
	PCIe_M.2_Interface E Key	MDT320E01001	
	Ext Power Measurement Header	61300311121	
	PCIe Card Slot	10018783-10202TLF	
	USB C PD Controller	TPS25750D	0x20
	Level Translator-1	TCA9543APWR	0x71
	Level Translator-2	TCA9543APWR	0x72
	GPIO Expander	TCA6416ARTWR	0x21
	PMIC	TPS6594133ARWERQ1	
	ENET Expansion Header	171446-1109	0x77
MCU_I2C1	HDMI Connector	1852139-0N055T-H	
MAIN_I2C1	FPC Camera Connector 1	52435-2271	
	FPC Camera Connector 2	52435-2271	
	CSI2_A Expansion Connector	QSH-020-01-L-D-DP-A-K	
	CSI2_B Expansion Connector	QSH-020-01-L-D-DP-A-K	
	GPIO Expander	TCA6408ARGTR	0x21
	Level Translator	TCA9543APWR	0x70

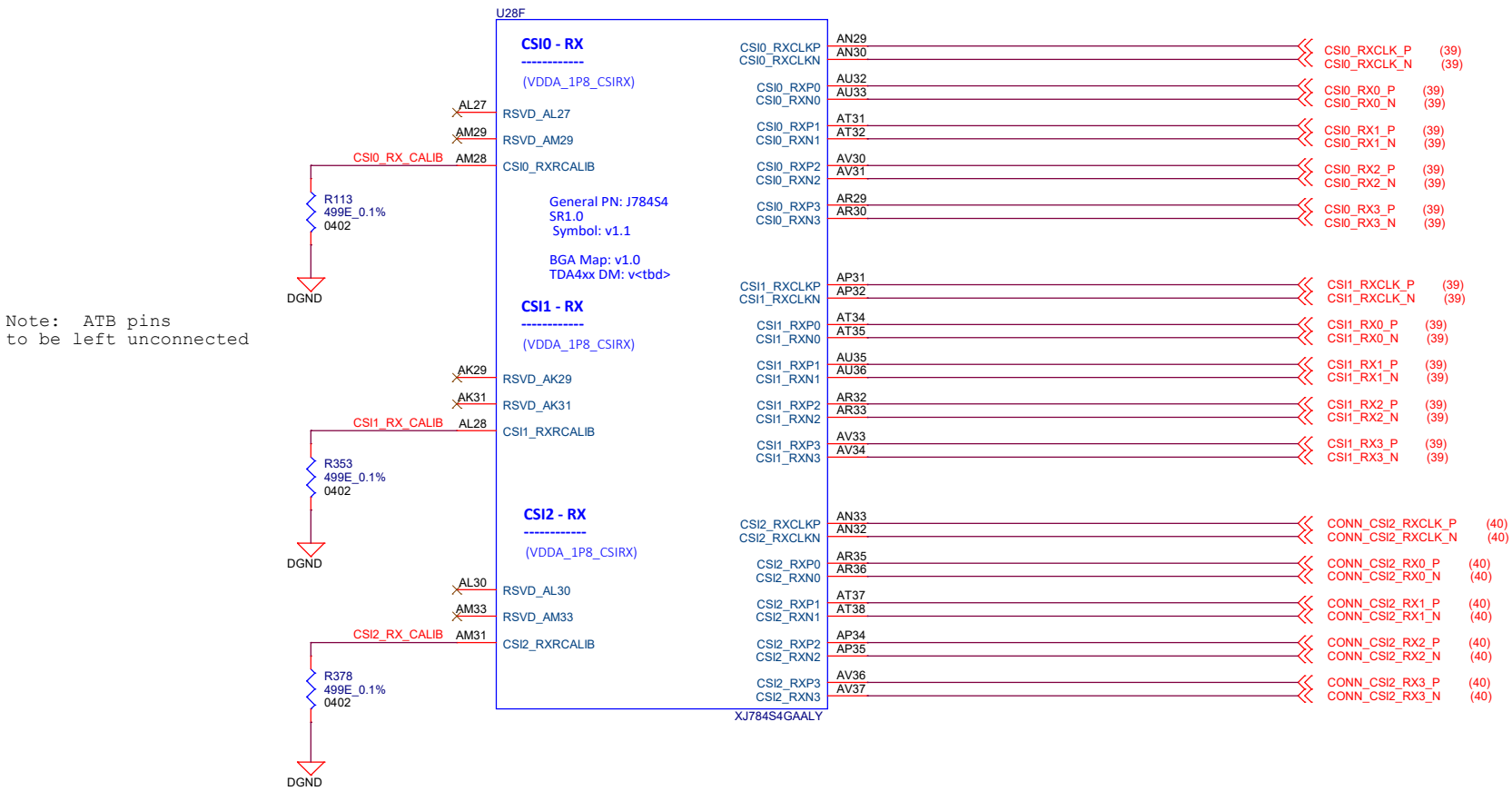
GPIO MAPPING TABLE

GPIO Mapping						
WKUP Domain						
J7AHP Mapping		Net Name	Input/Output	Default	State	Usage
Package Signal Name	GPIO					
MCU_OSPI0_CSn1	WKUP_GPIO0_28	EN_EFUSE_VPP	O	PD	Active High	Enable for VPP_EFUSE_1V8 LDO
MCU_OSPI0_CSn2	WKUP_GPIO0_29	CPLD_TMS/CSIB_EXP_GPIO1	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_CLK	WKUP_GPIO0_31	CPLD_TCK/CSIB_EXP_GPIO2	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_LBCLKO	WKUP_GPIO0_32	CSI_EXP_GPIO_1	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_DQS	WKUP_GPIO0_33	CPLD_TDO/CSIB_EXP_GPIO3	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_D0	WKUP_GPIO0_34	CPLD_TDI/CSIB_EXP_GPIO4	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_D1	WKUP_GPIO0_35	CSI_EXP_GPIO_5	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_D2	WKUP_GPIO0_36	CSI_EXP_GPIO_2	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_D3	WKUP_GPIO0_37	CSI_EXP_GPIO_3	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_CSn0	WKUP_GPIO0_38	CSI_EXP_GPIO_4	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_OSPI1_CSn1	WKUP_GPIO0_39	CSIB_EXP_GPIO5	IO	NA	NA	GPIO signal for CSI2 EXPANSION Connector
MCU_SPIO_CLK	WKUP_GPIO0_54	WKUP_GPIO0_54	O	Bootmode	Active High	Select line for CPLD's Mux
MCU_SPIO_D0	WKUP_GPIO0_55	USER_LED1	O	Bootmode	Active High	User LED
MCU_SPIO_D1	WKUP_GPIO0_69	SYS_MCU_PWRDN	O	Bootmode	Active High	System Power Down ('0' - normal operation '1' - system power down)
MCU_SPIO_CS0	WKUP_GPIO0_70	WKUP_GPIO0_70	IO	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO0_10	WKUP_GPIO0_10	HDMI_LS_OE	O	PU	Active High	Level Shifter Output Enable for HDMI
WKUP_GPIO0_14	WKUP_GPIO0_14	HDMI_PDn	O	Bootmode	Active Low	Power Down Signal for HDMI
WKUP_GPIO0_49	WKUP_GPIO0_49	WKUP_GPIO0_49	IO	NA	NA	GPIO signal for 40 pin Expansion Header
PMIC_POWER_EN1	WKUP_GPIO0_88	WKUP_GPIO0_88	IO	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO0_56	WKUP_GPIO0_56	WKUP_GPIO0_56	IO	NA	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO0_57	WKUP_GPIO0_57	WKUP_GPIO0_57	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCU_ADC1_AIN0	WKUP_GPIO0_79	SOC_INT1z	I	PU	Active Low	Test Automation INT signal
MCU_ADC1_AIN1	WKUP_GPIO0_80	SOC_INT2z	I	PU	Active Low	Test Automation INT signal
MCU_ADC1_AIN2	WKUP_GPIO0_81	MCU_RGMII_INT#	I	PU	Active Low	Interrupt Signal from RGMII
MCU_ADC1_AIN3	WKUP_GPIO0_82	SOC_WAKE	I	PU	Active High	SOC wake signal from Push Button
MCU_ADC1_AIN4	WKUP_GPIO0_83	PMIC_INTn	I	PU	Active Low	PMIC interrupt signal
MCU_ADC1_AIN5	WKUP_GPIO0_84	ENET1_EXP_INTB	I	NA	NA	Interrupt Signal from ENET Expansion Header
MCU_ADC1_AIN6	WKUP_GPIO0_85	IO_EXP_I2C0_INTB	O	NA	NA	I2C0 Interrupt Signal to ENET Expansion Header
WKUP_GPIO0_66	WKUP_GPIO0_66	WKUP_GPIO0_66	IO	PU	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO0_67	WKUP_GPIO0_67	WKUP_GPIO0_67	IO	NA	NA	GPIO signal for 40 pin Expansion Header
Main Domain						
EXTINTn	GPIO0_0	HDMI_HPD	I	NA	Active High	HDMI hot plug detect signal
MCAN13_TX	GPIO0_3	GPIO0_3	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCAN13_RX	GPIO0_4	DPO_3V3_EN	O	PD	Active High	Enable signal for Display port Current Limiter
MCAN1_TX	GPIO0_27	GPIO0_27	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCASP0_AXR8	GPIO0_36	GPIO0_36	IO	NA	NA	GPIO signal for 40 pin Expansion Header
ECAP0_IN_APWM_OUT	GPIO0_49	SEL_SDIO_3V3_1V8n	O	PU	Active Low	One of Enable signal for VDD_SD_DV
GPIO Expander						
Port No	GPIO	I2C	Input/Output	Default	State	Usage
P0	CSI_VIO_SEL	MAIN_I2C1 Address : 0x21 Part No - TCA6408ARGTR	O	PD	Active High	Enable signal for Camera IO supply
P1	CSI_MUX_SEL_2		O	PD	Active High	Select lines for CSI mux
P2	CSI2_RSTz		O	PD	Active Low	Reset signal for CSI Expansion Connector
P3	IO_EXP_CAM0_GPIO1		IO	NA	NA	GPIO signals for FPC Camera Connector
P4	IO_EXP_CAM1_GPIO1		IO	NA	NA	GPIO signals for FPC Camera Connector
P00	BOARDID_EEPROM_WP	MAIN_I2C0 Address : 0x21 Part No - TCA6416ARTWR	O	PD	Active High	Board ID EEPROM Write Protect
P01	CAN_STB		O	PD	Active High	Stand By Input for CAN Transceiver
P02	GPIO_uSD_PWR_EN		O	PU	Active High	One of Enable signal for Micro SD Load Switch
P03	IO_EXP_MCU_RGMII_RST#		O	NA	Active Low	MCU_RGMII Resetz signal to CPLD
P04	IO_EXP_PCIE0_4L_PERST#		O	NA	Active Low	PCIe 4 lane Resetz signal to CPLD
P05	IO_EXP_PCIE1_M.2_RTSz		O	NA	Active Low	PCIe M Key Resetz signal to CPLD
P06	IO_EXP_PCIE3_M.2_RTSz		O	NA	Active Low	PCIe E Key Resetz signal to CPLD
P07	PM_INA_BUS_EN		O	PU	Active High	Enable signal for PM2 I2C lines
P10	ENET1_EXP_PWRDN		O	PU	Active High	Power Down Signal for Enet Expansion Header
P11	EXP1_ENET_RSTz		O	NA	Active Low	Reset Signal for Enet Expansion Header
P12	ENET1_I2CMUX_SEL		O	NA	Active High	I2C mux select Signal for Enet Expansion Header
P13	PCIe0_CLKREQ#		I	PU	Active Low	PCIe Card Clock request Signal
P14	PCIe1_M.2_CLKREQ#		I	PU	Active Low	PCIe M Key Clock request Signal
P15	PCIe3_M2_CLKREQ#		I	PU	Active Low	PCIe E Key Clock request Signal
P16	PCIe0_PRSENT2#_1		I	NA	Active Low	Reset Signal for PCIe card Slot
P17	PCIe0_PRSENT2#_2		I	PU	Active Low	Reset Signal for PCIe card Slot
P0	SW_CPLD_CONTROL_IN1	TEST AUTOMATION I2C Address : 0x20 Part No - TCA6408ARGTR	O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P1	SW_CPLD_CONTROL_IN2		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P2	SW_CPLD_CONTROL_IN3		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P3	SW_CPLD_CONTROL_IN4		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic

DSI

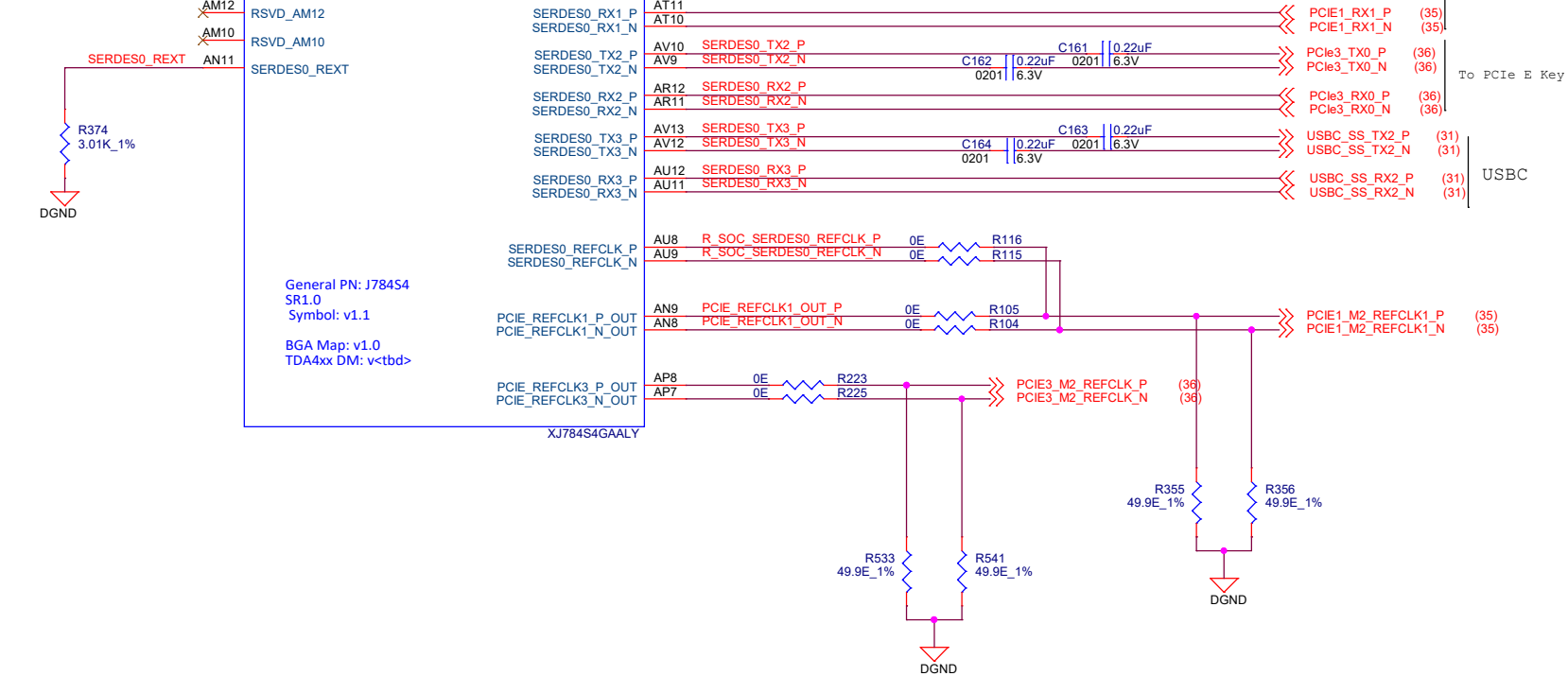


CSI



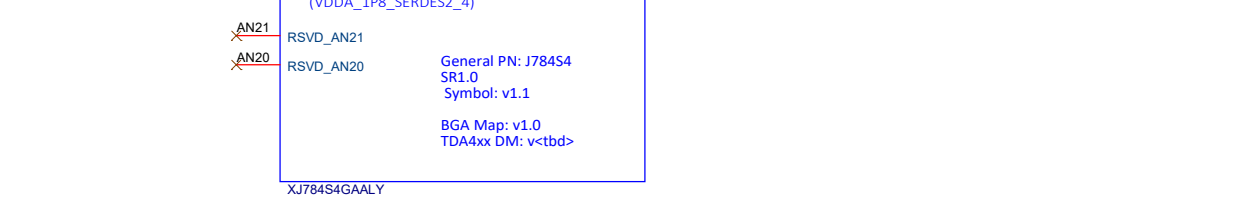
SERDES0

Note: ATB pins to be left unconnected



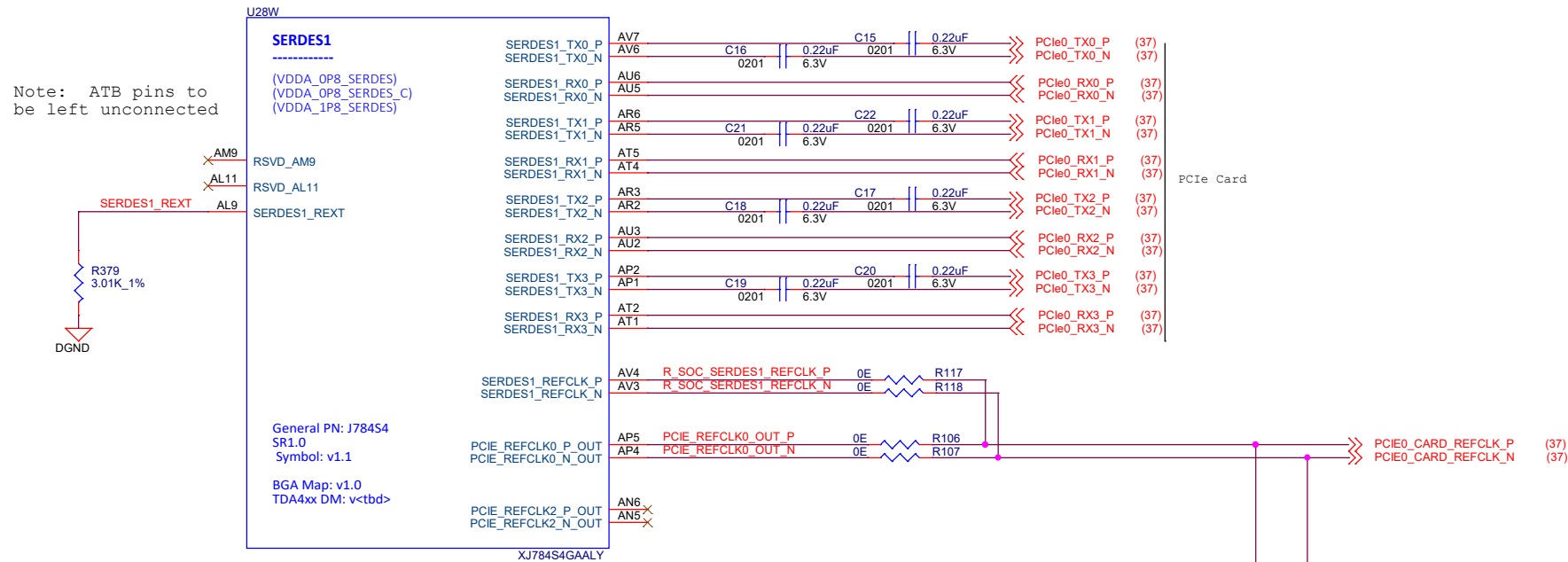
DP_AUX

Note: ATB pins to be left unconnected



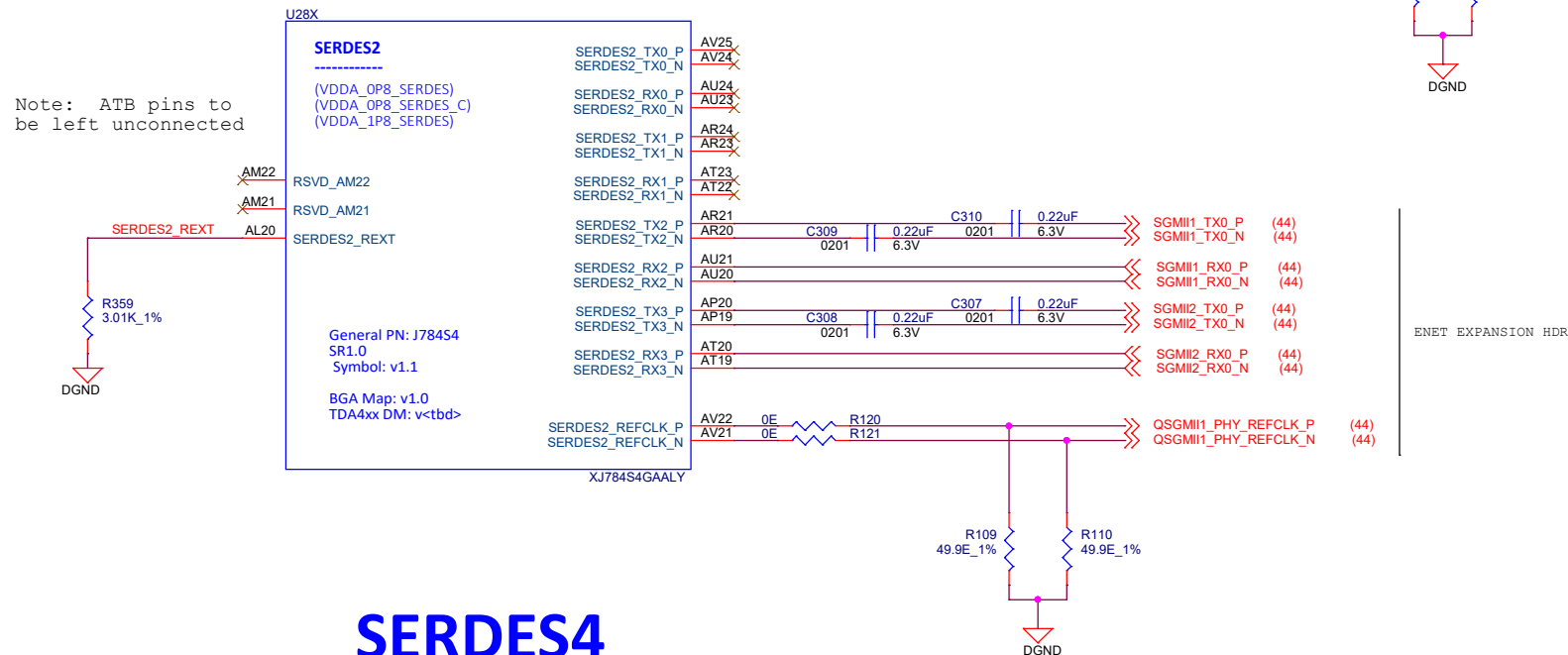
SERDES1

Note: ATB pins to be left unconnected



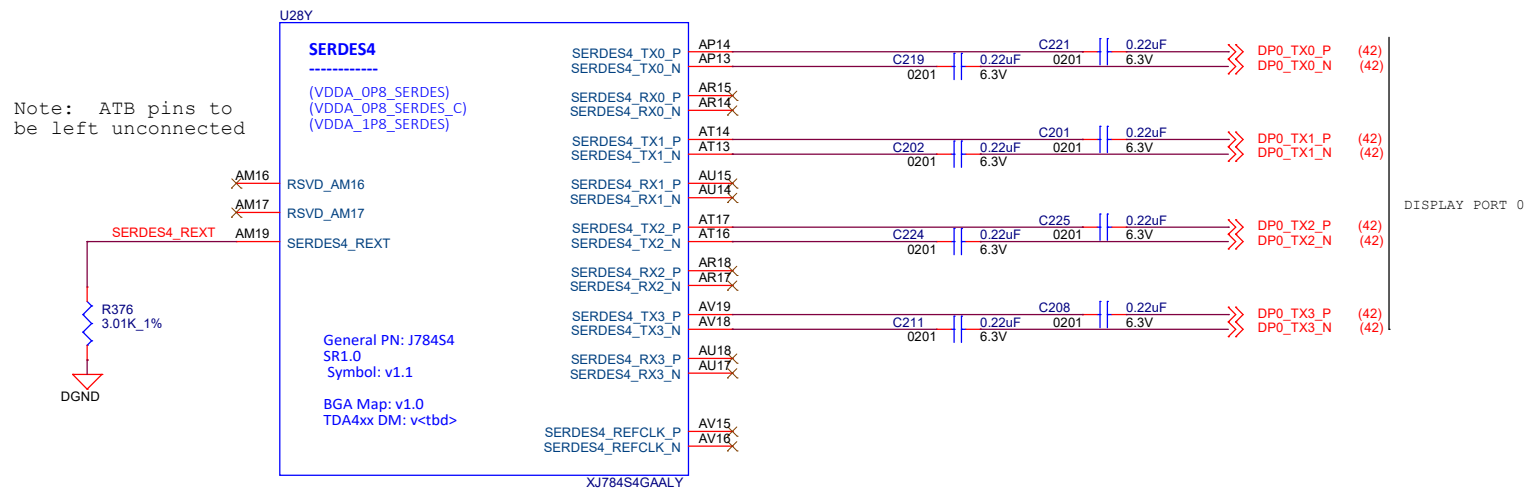
SERDES2

Note: ATB pins to be left unconnected



SERDES4

Note: ATB pins to be left unconnected



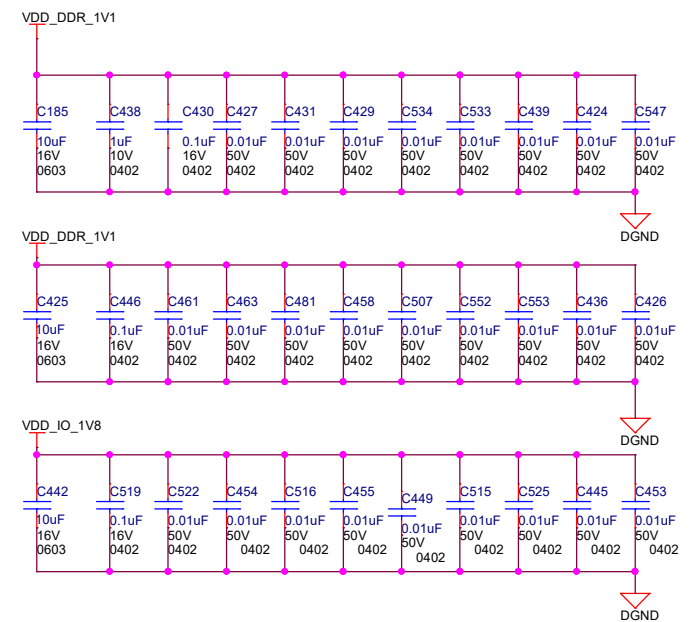
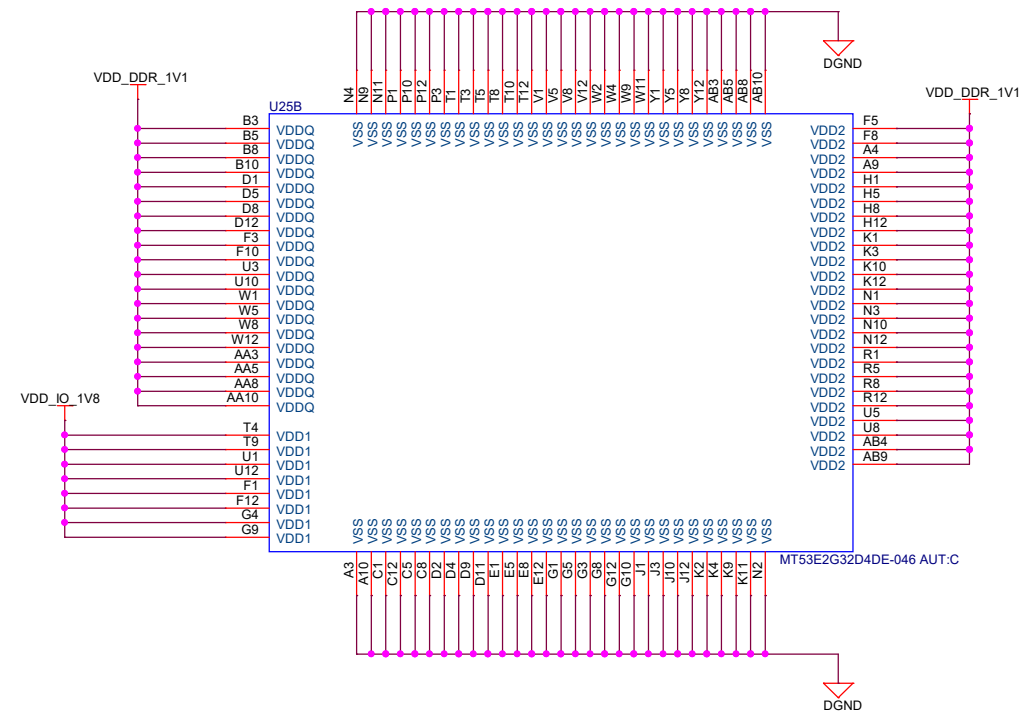
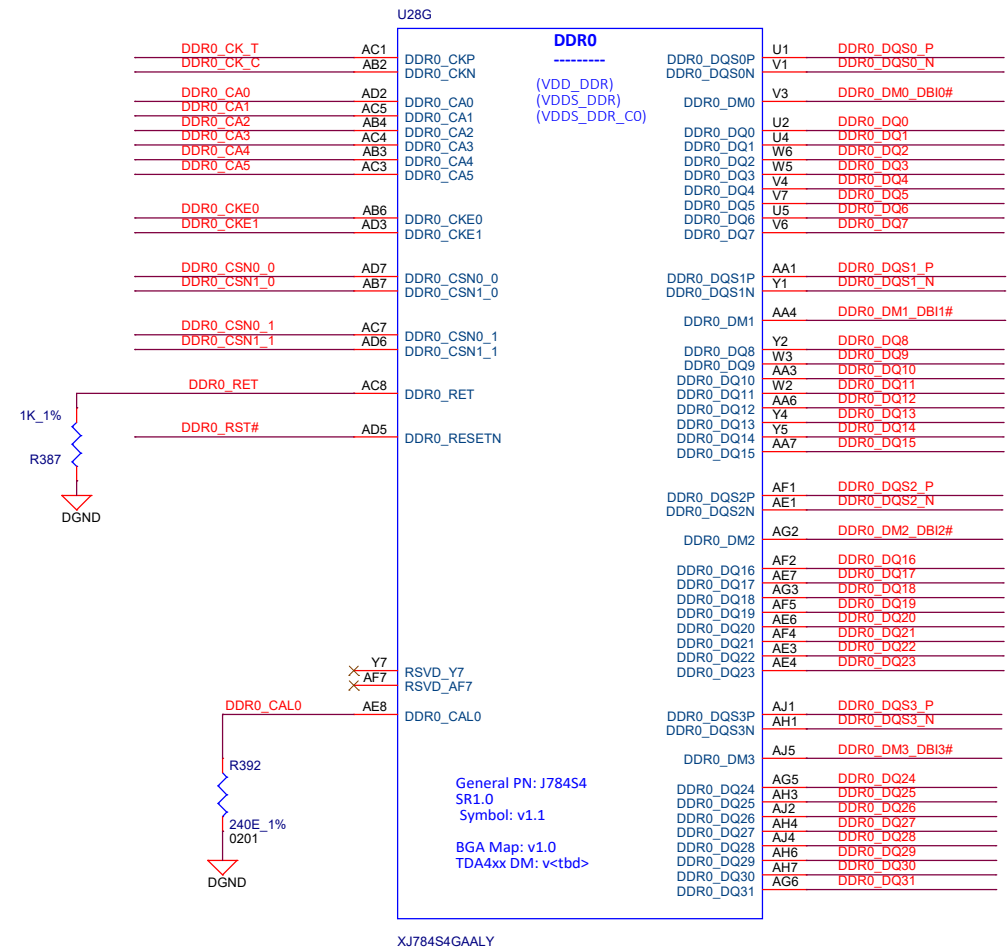
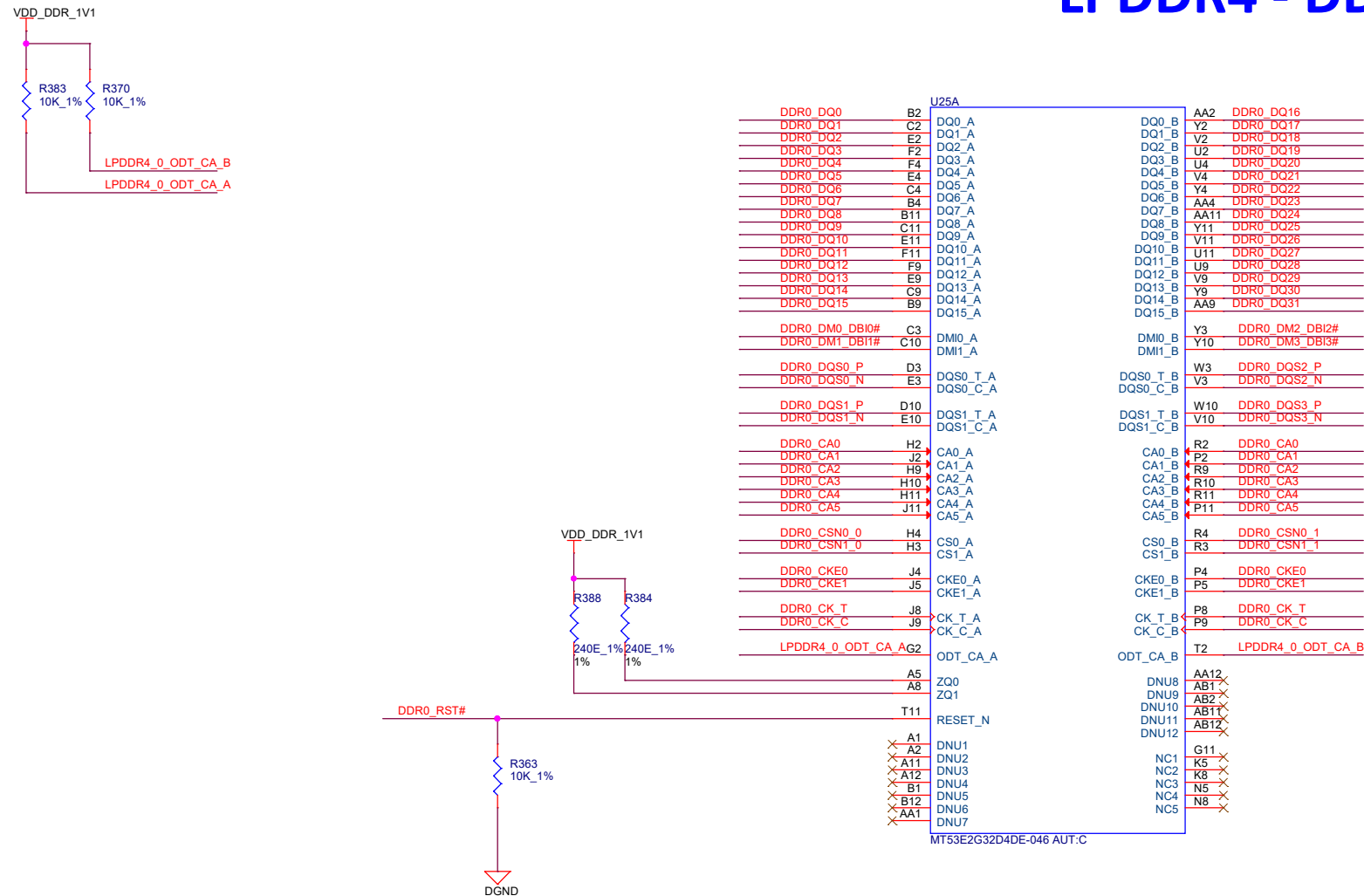
Project :
TDA4VM Edge AI Kit



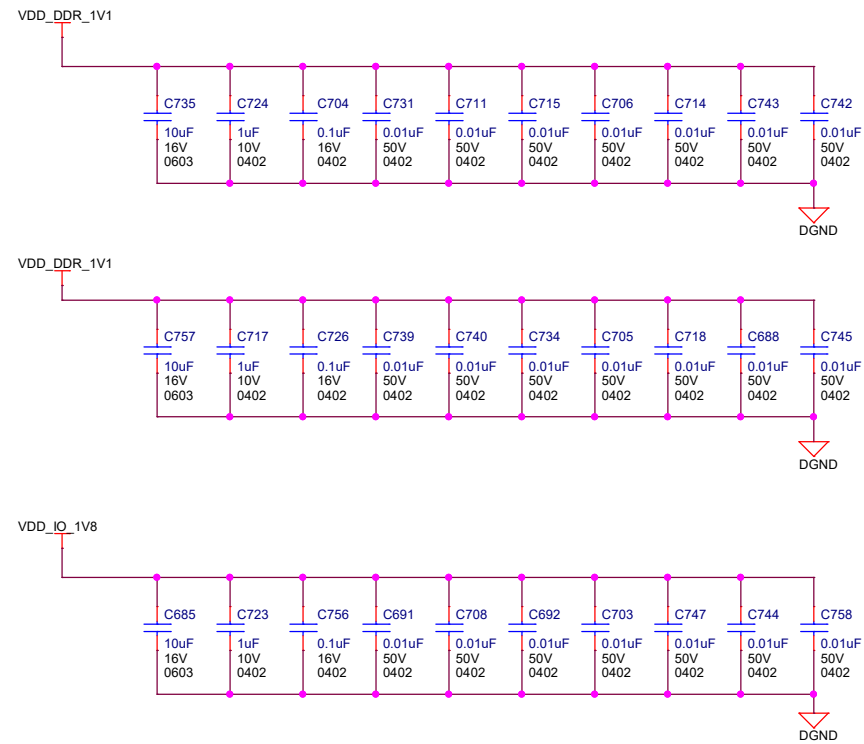
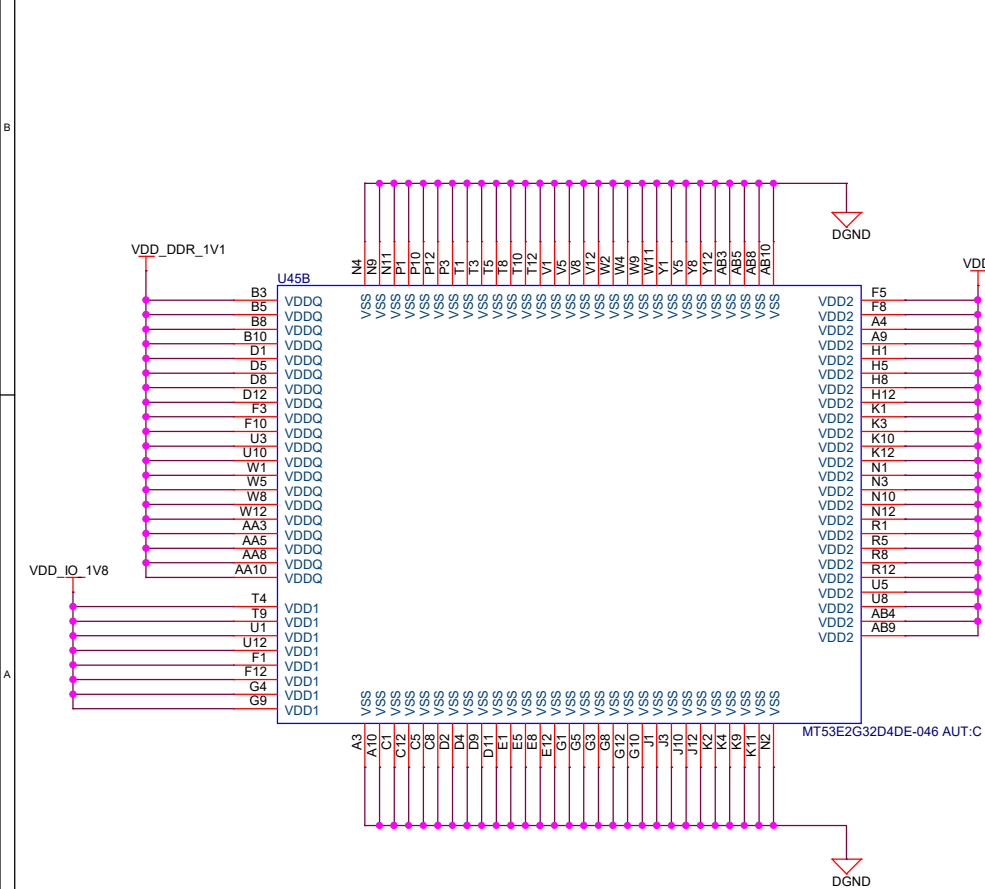
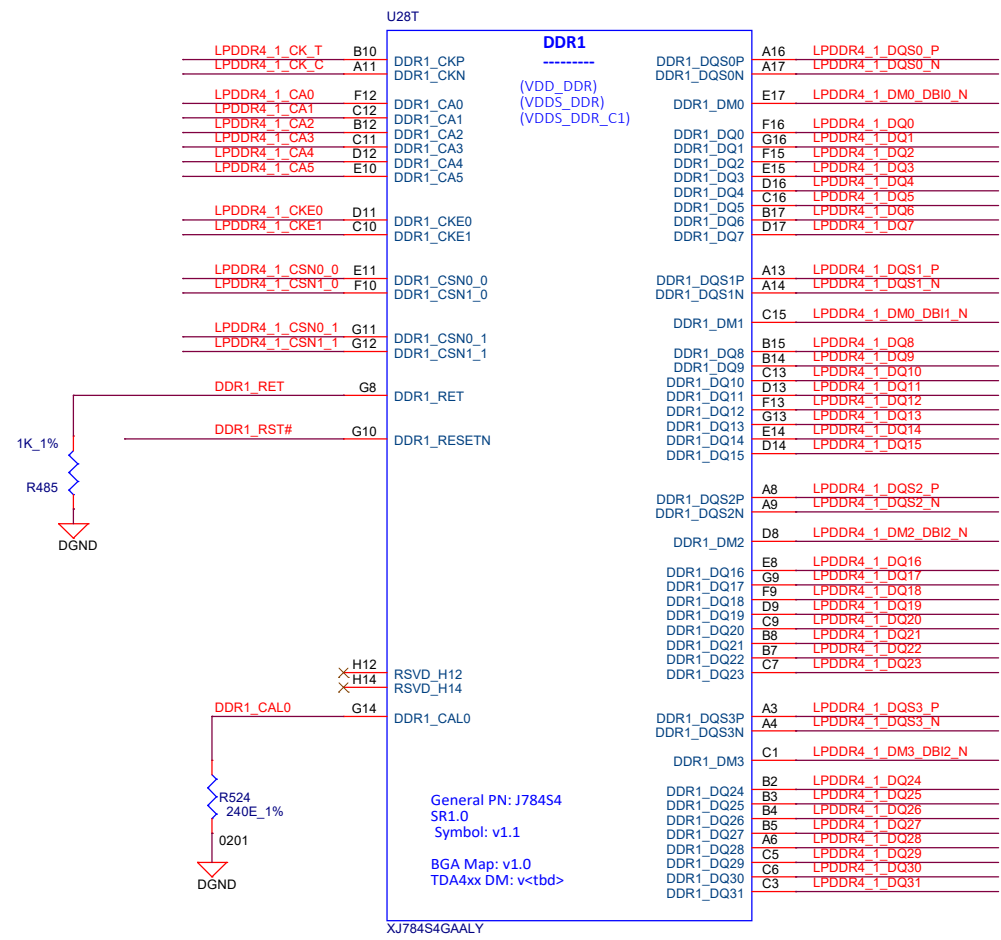
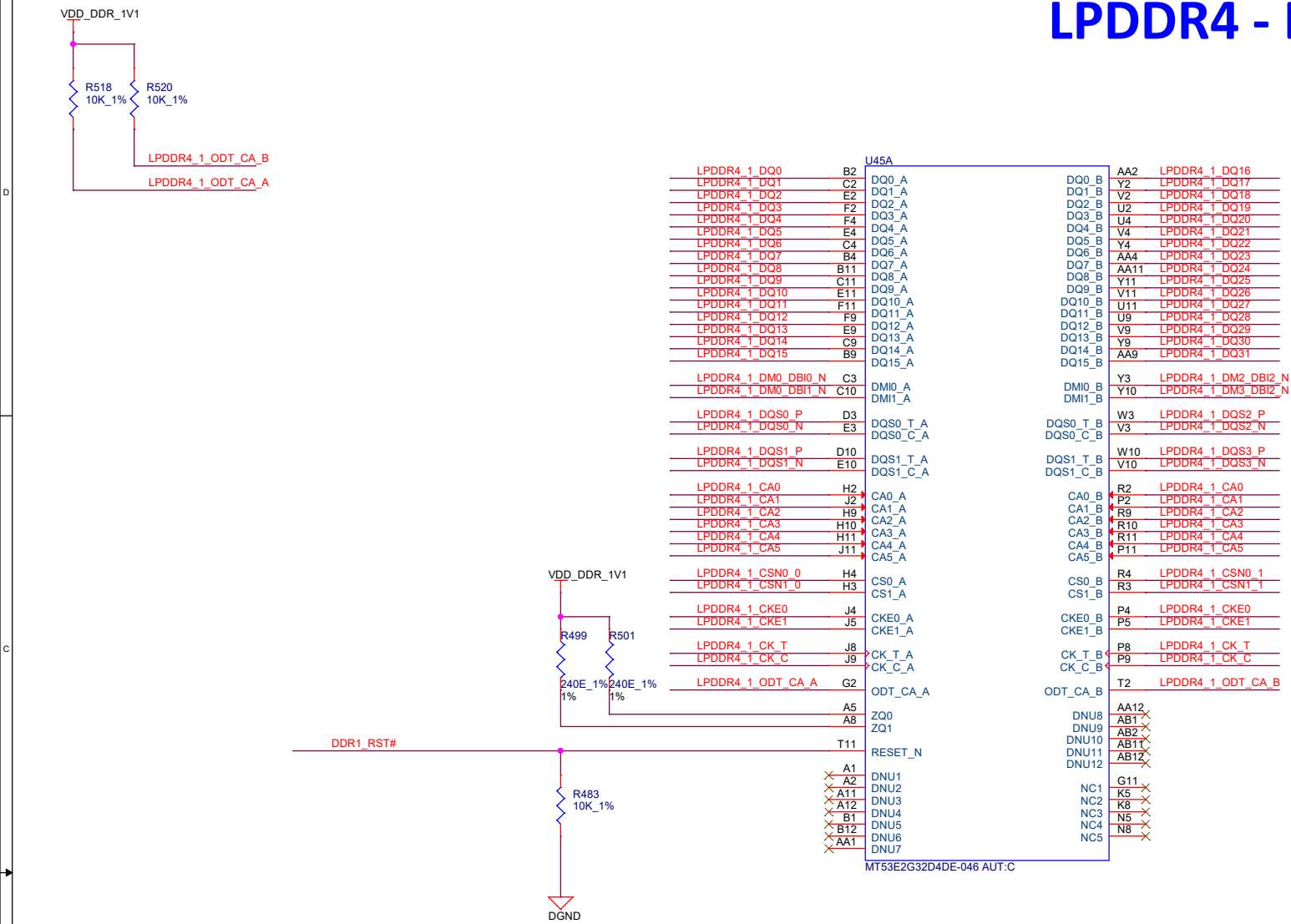
Title
SERDES INTERFACE

Size	Rev
C	E1
Date: Monday, October 17, 2022	
Sheet 11 of 62	

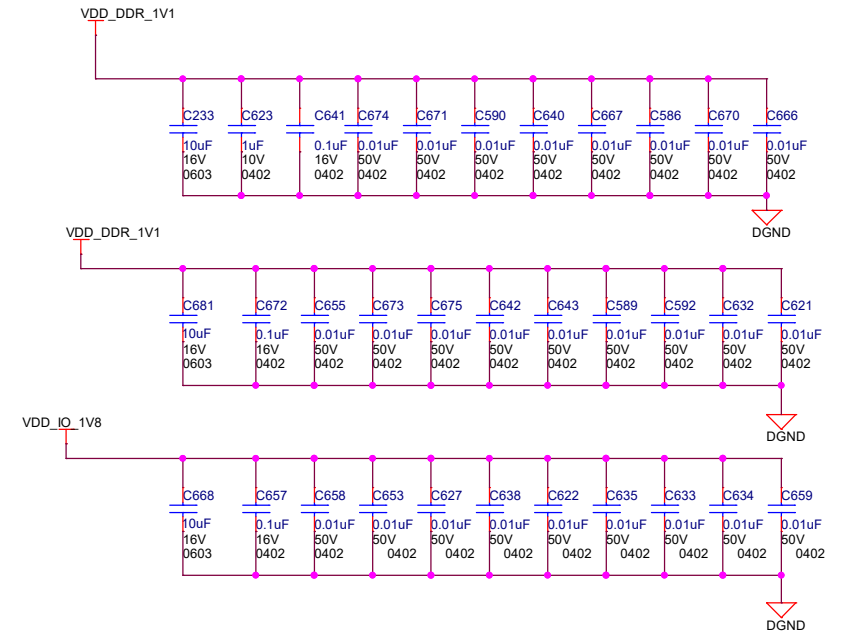
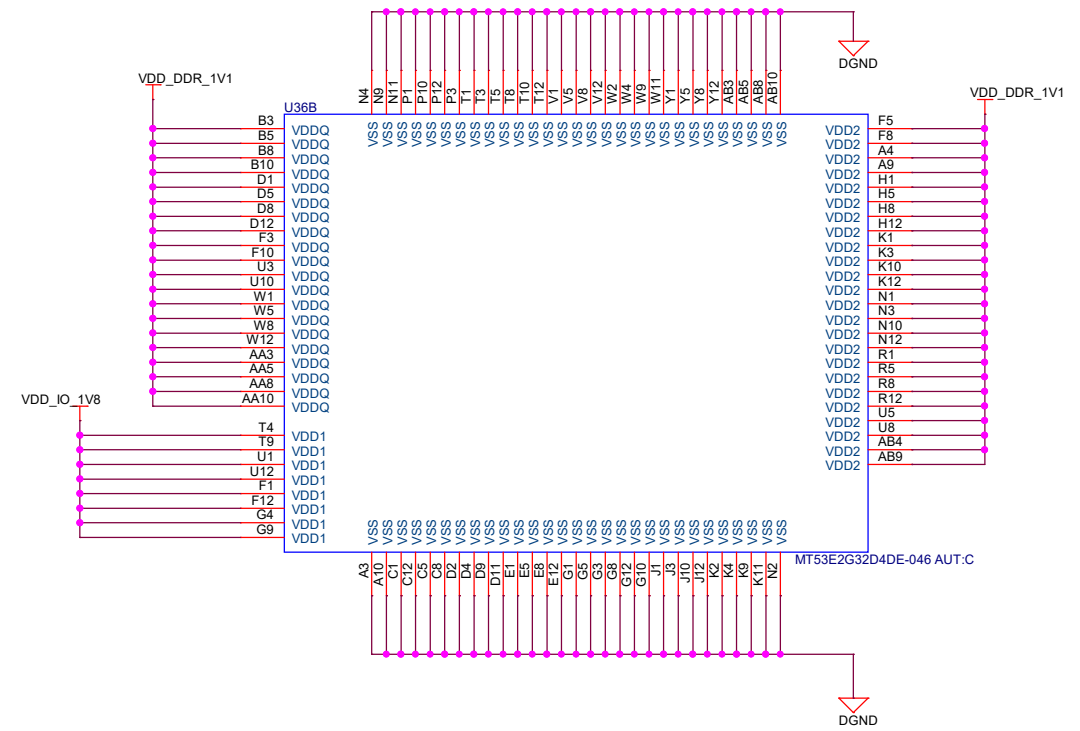
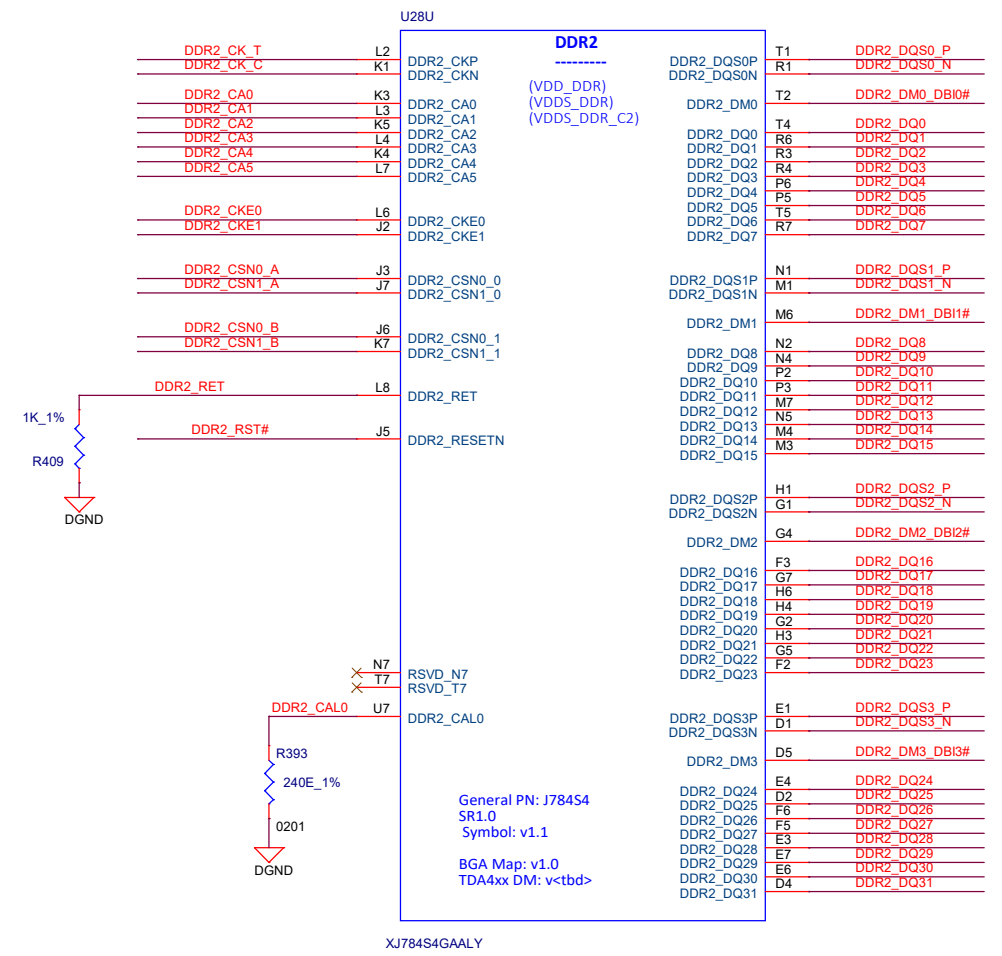
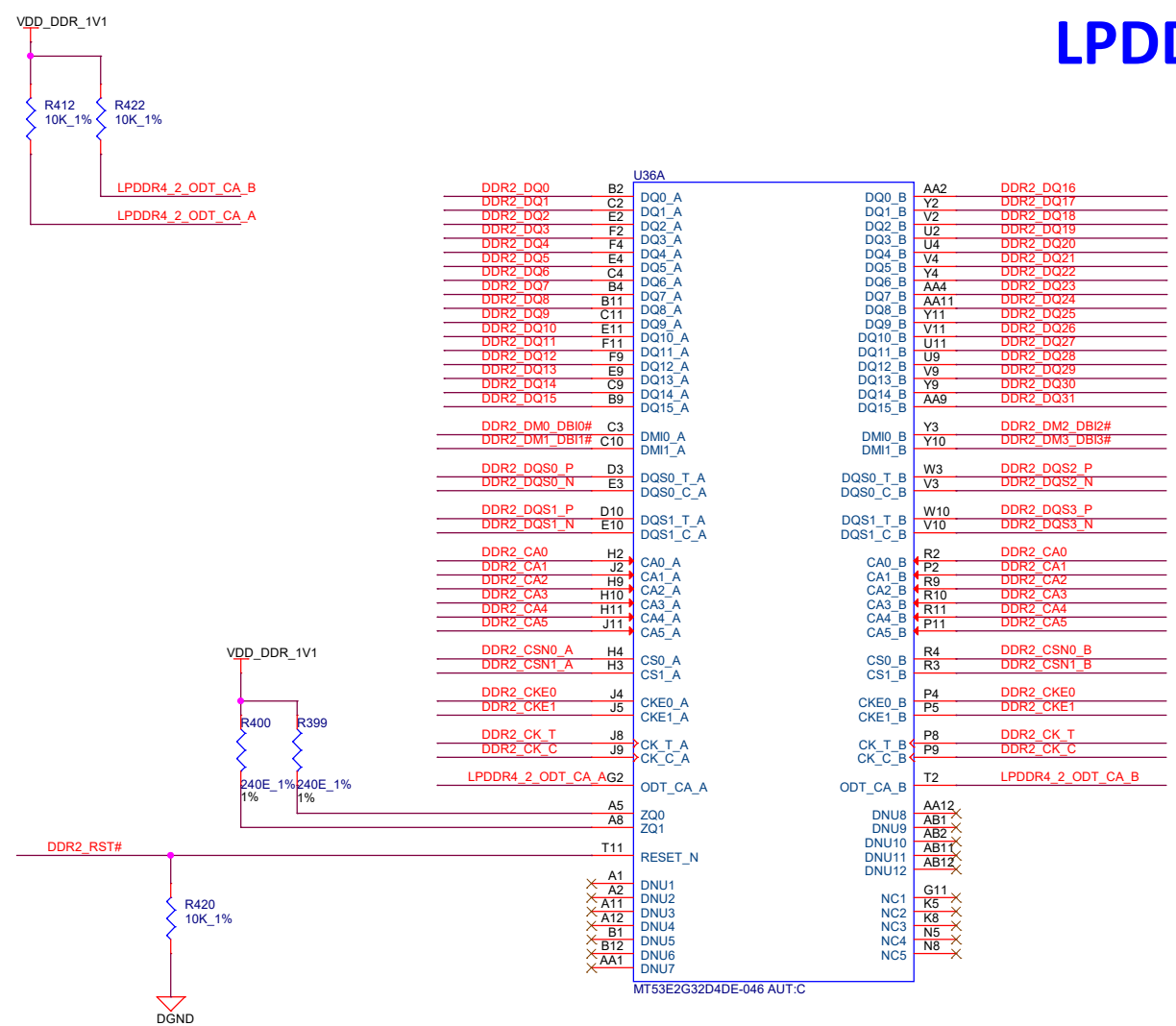
LPDDR4 - DDR0



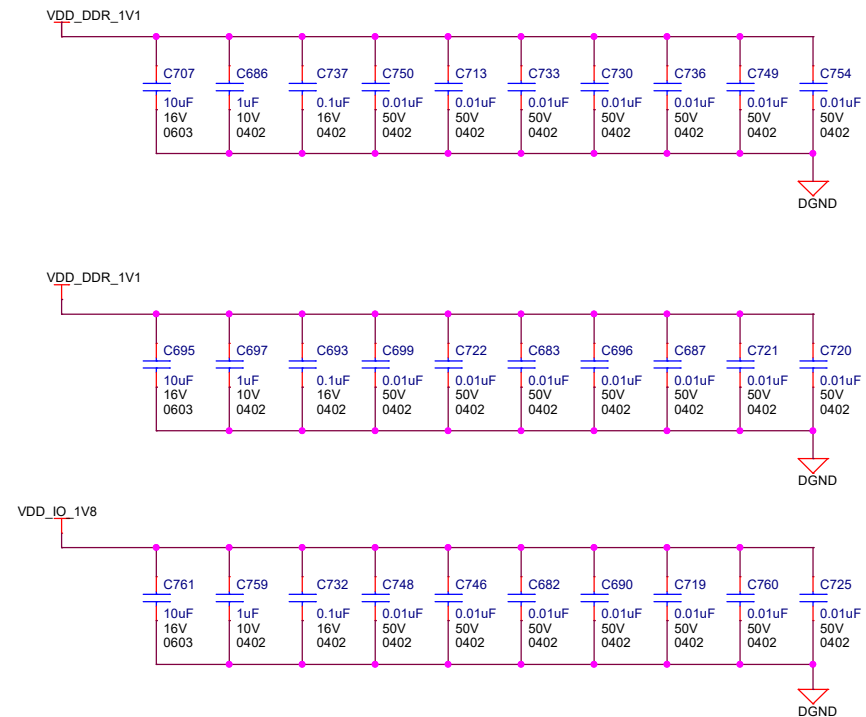
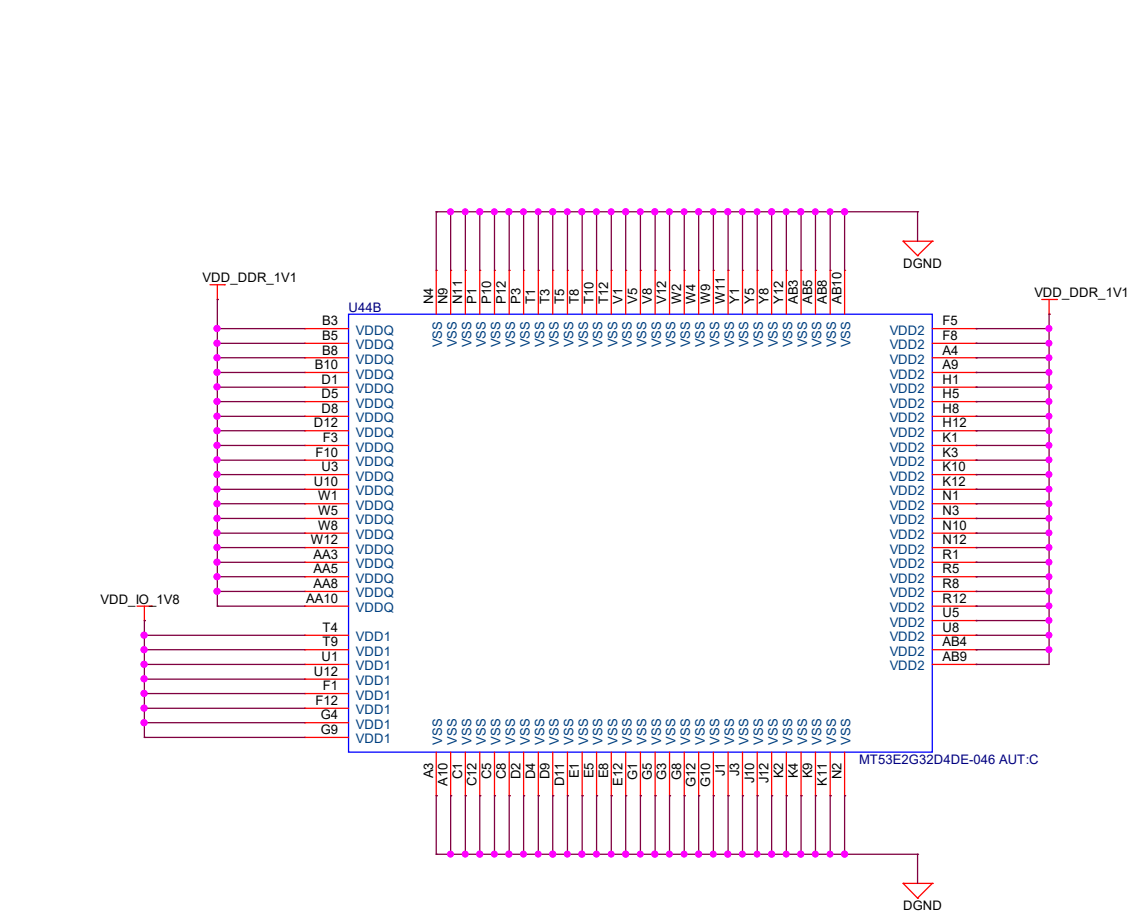
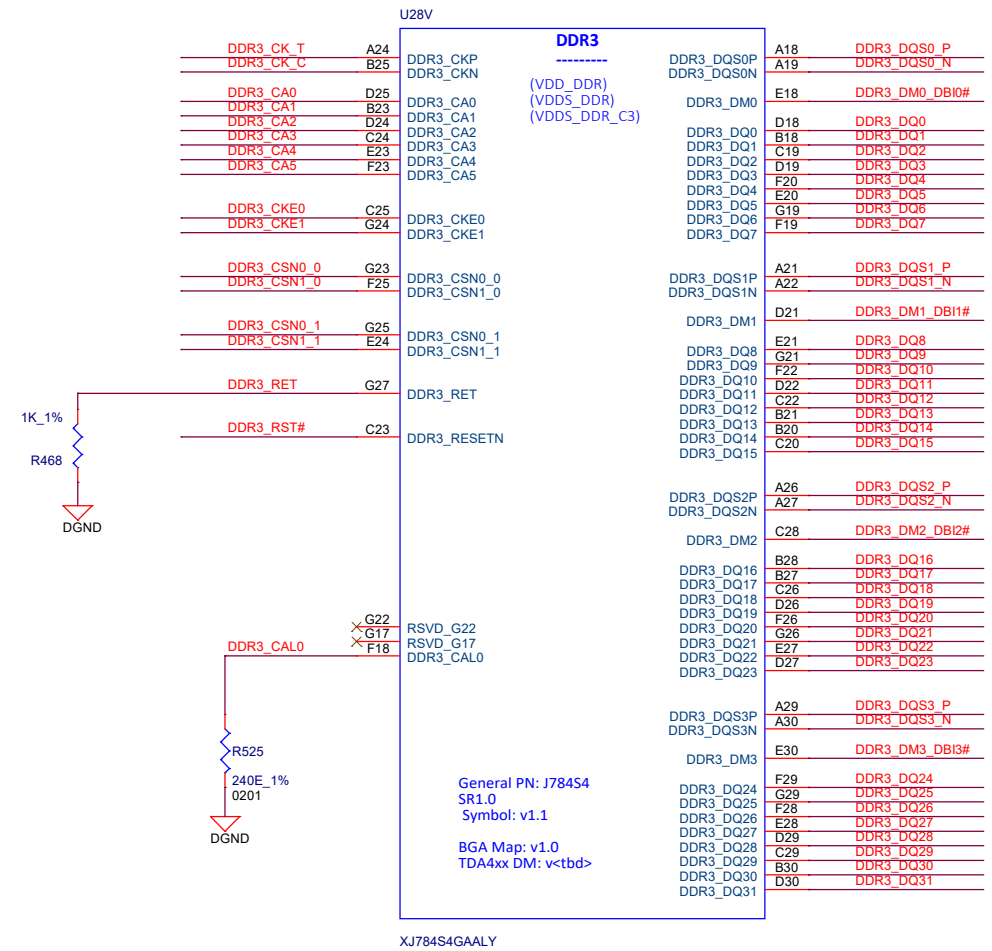
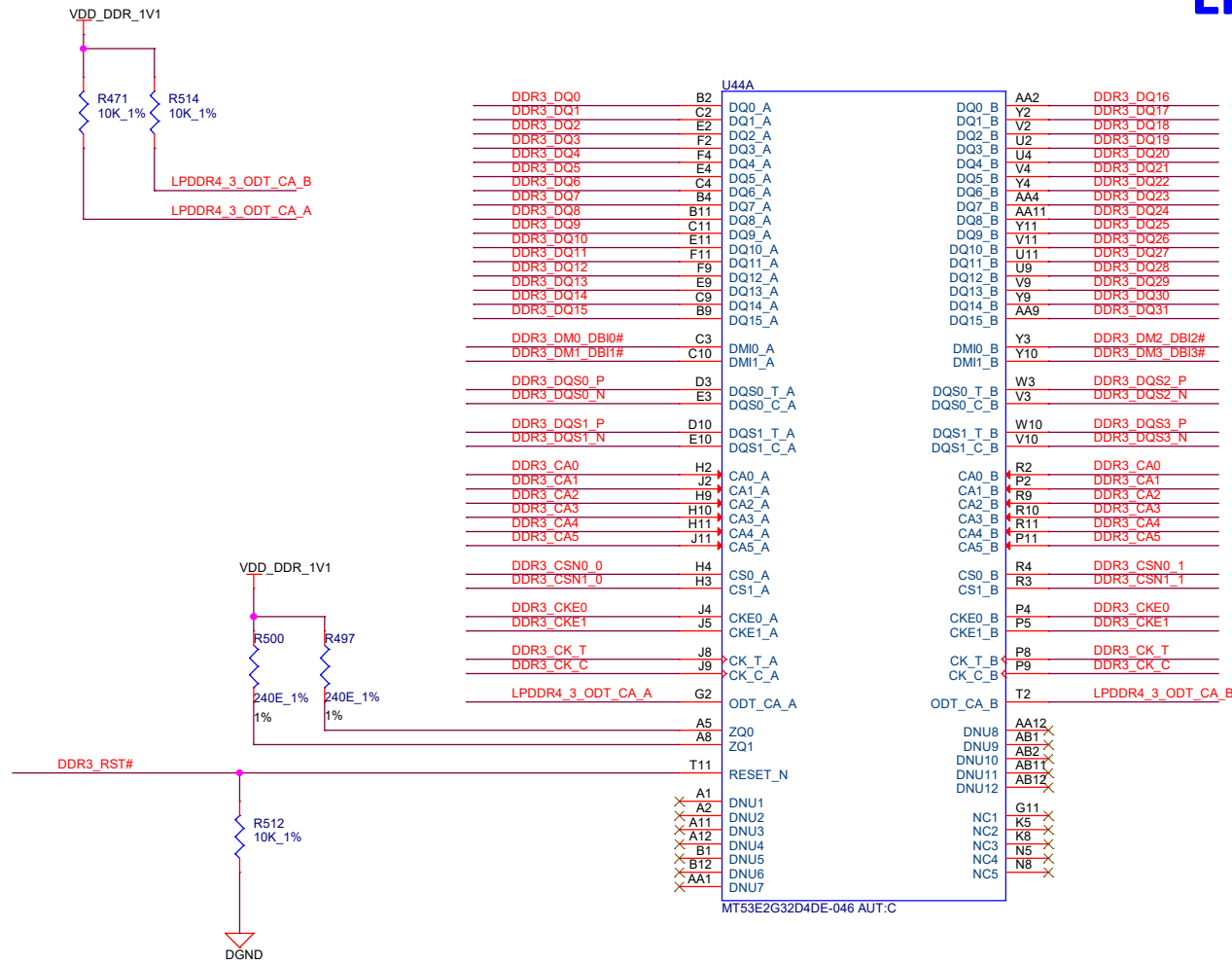
LPDDR4 - DDR1



LPDDR4 - DDR2

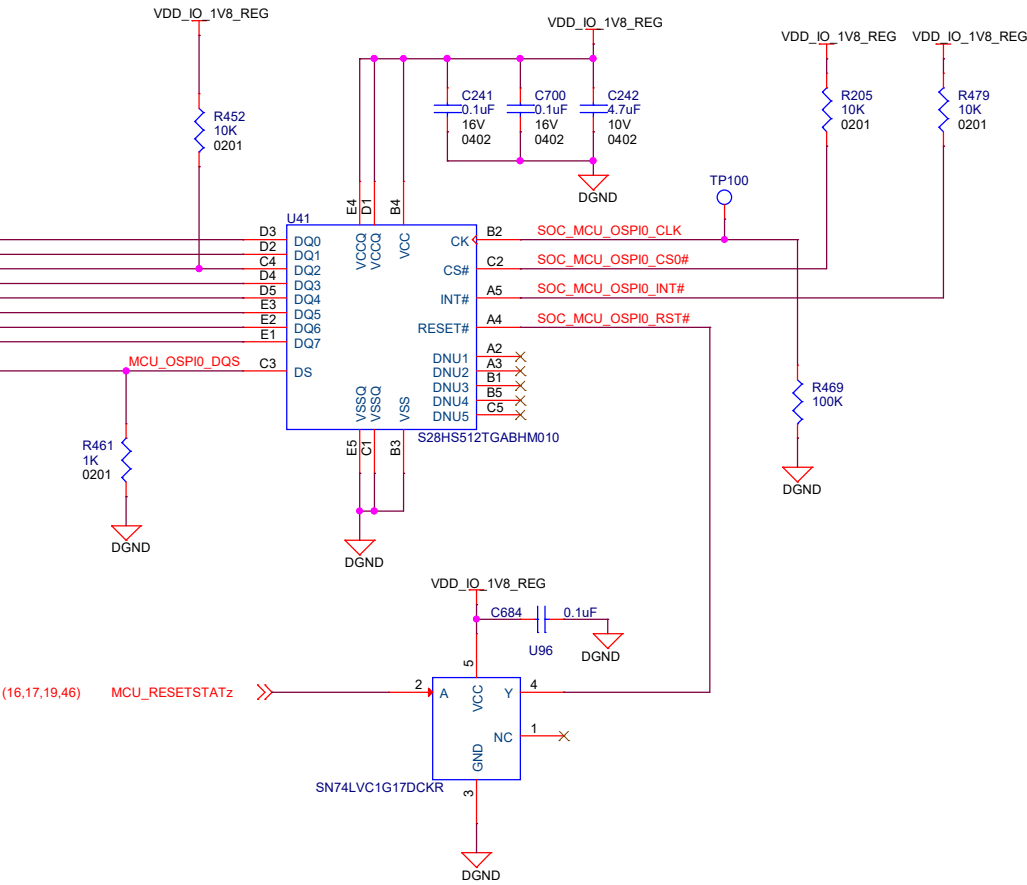
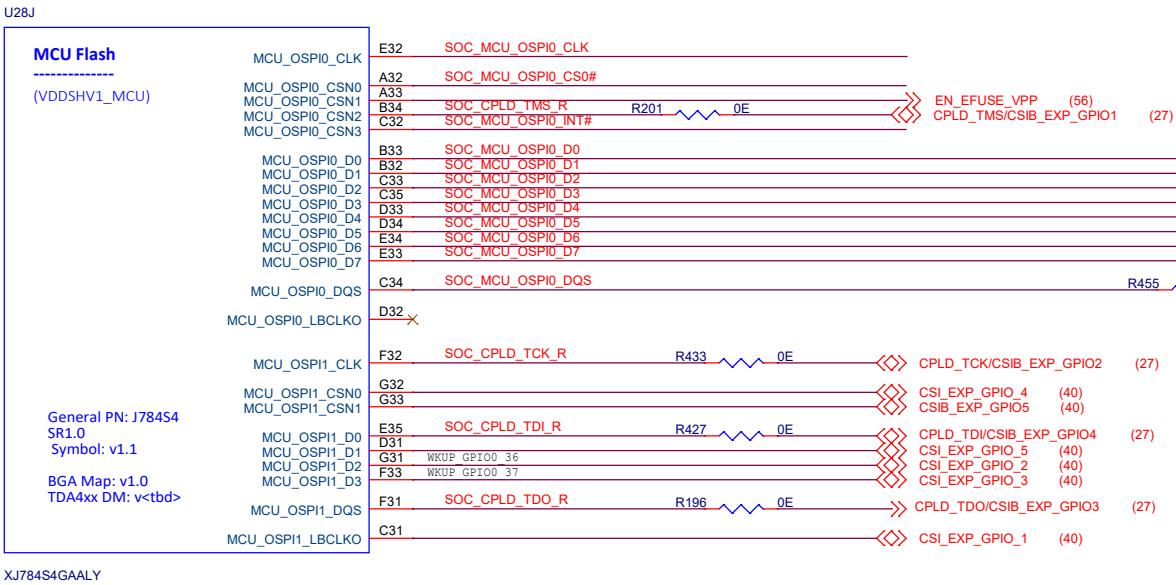


LPDDR4 - DDR3

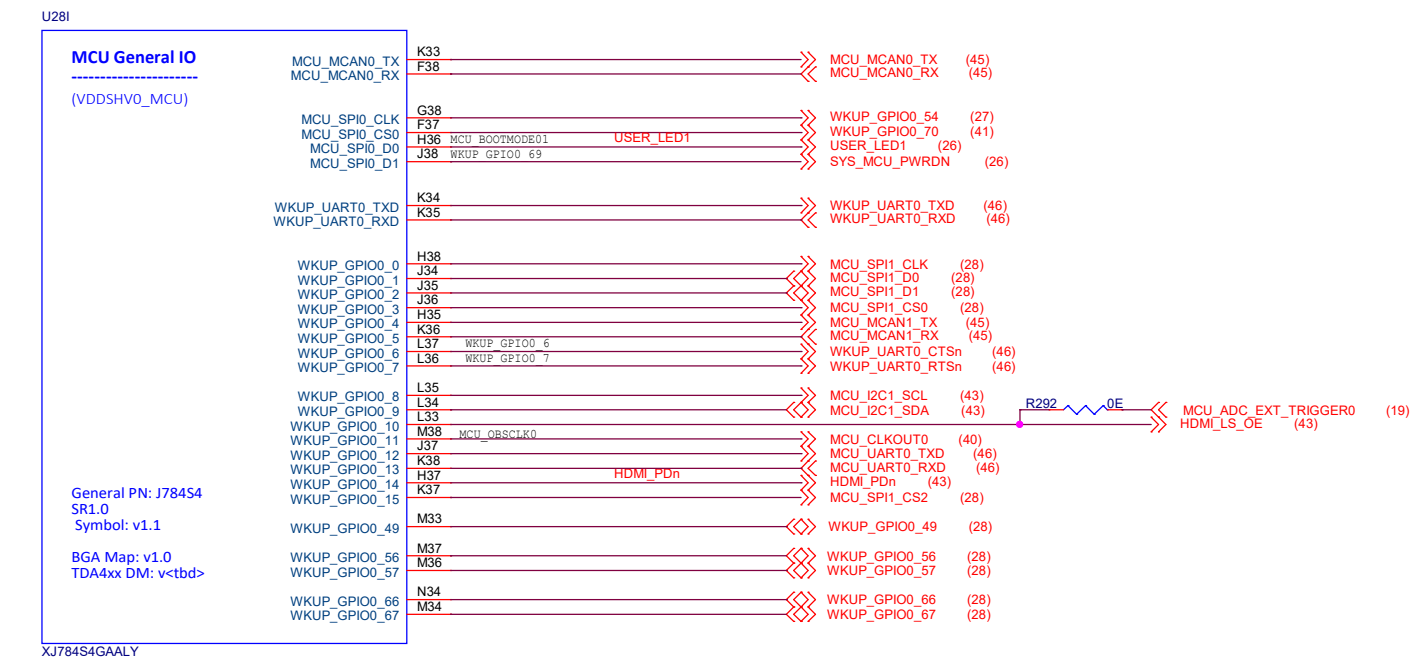


MCU FLASH

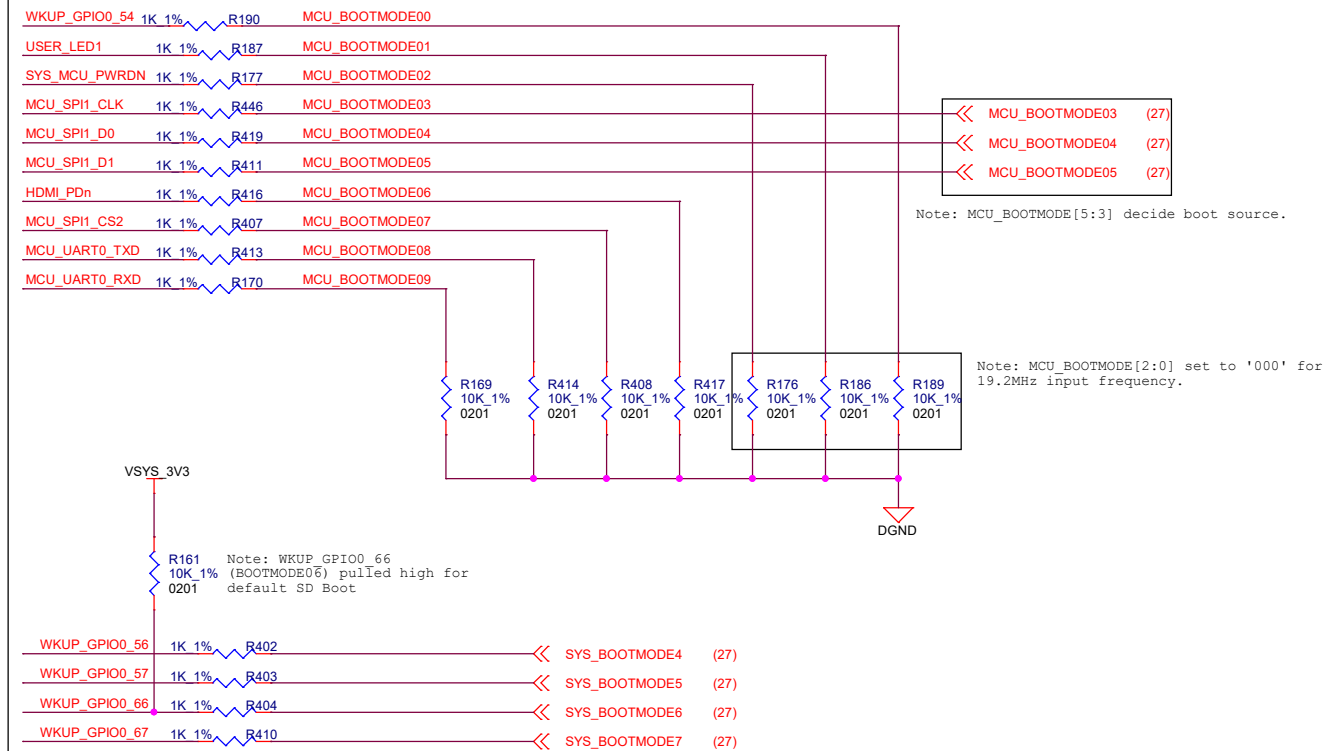
OSPI FLASH



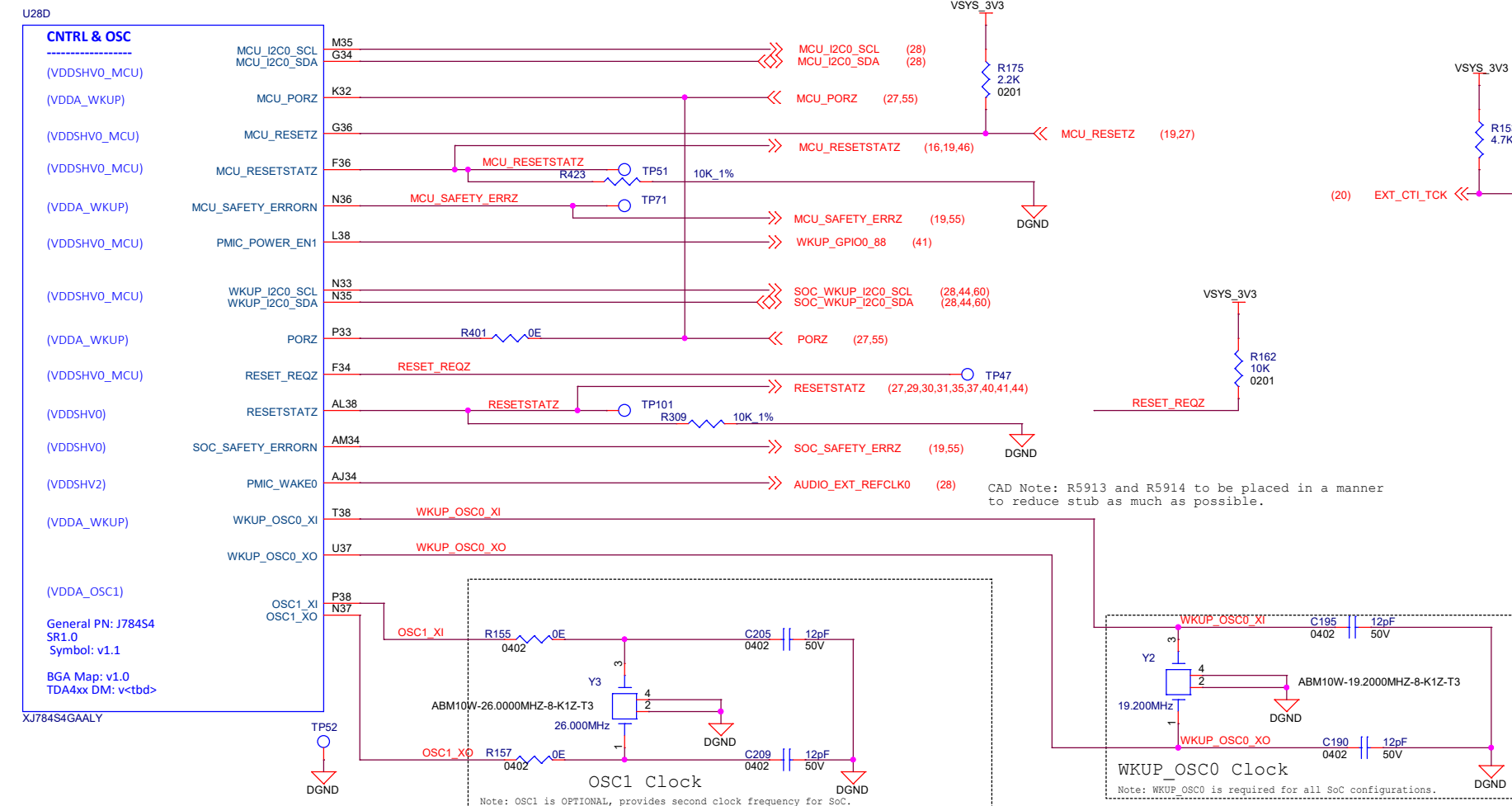
MCU & MAIN GENERAL IO, OSC CLKS



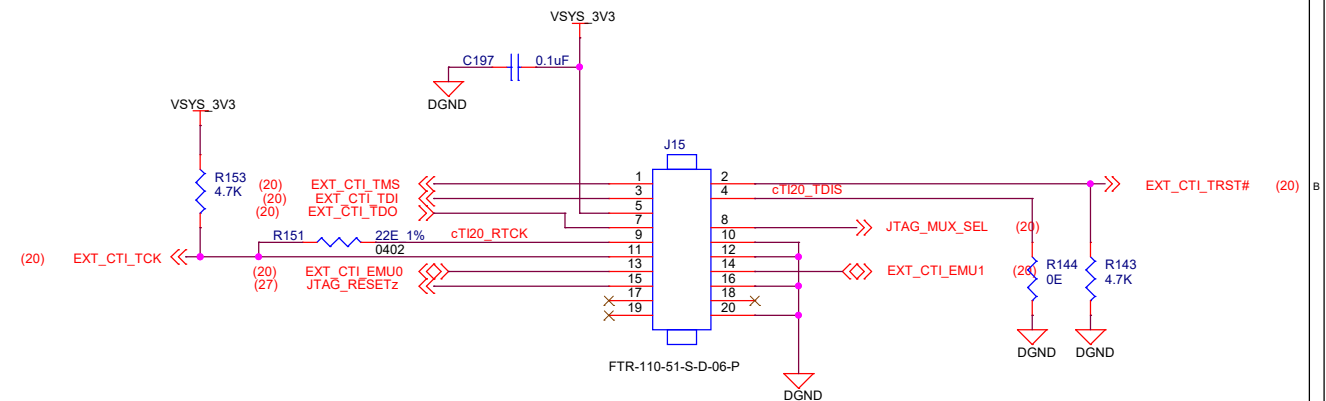
BOOTMODE



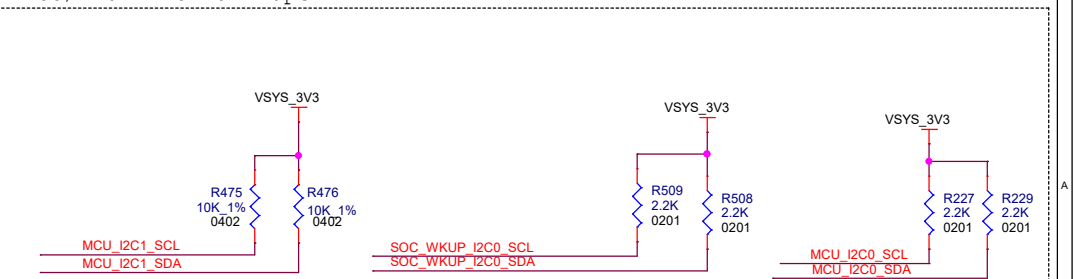
CONTROL & OSC



cTI 20PIN JTAG HEADER



MCU/WKUP I2C Pull-ups



GENERAL IO

U28A

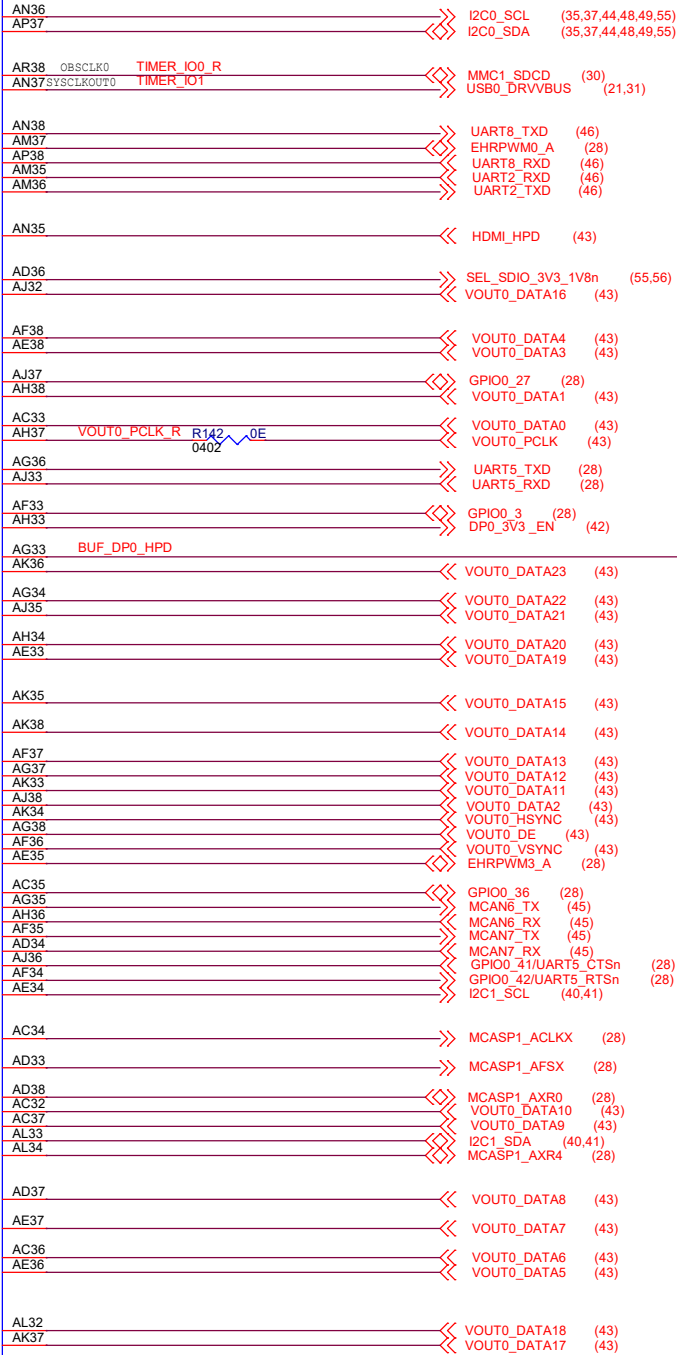
General IO

(VDDSHV0)

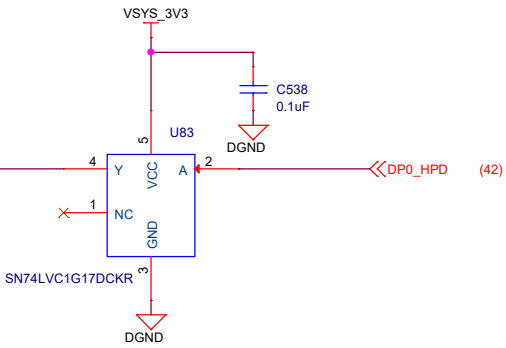
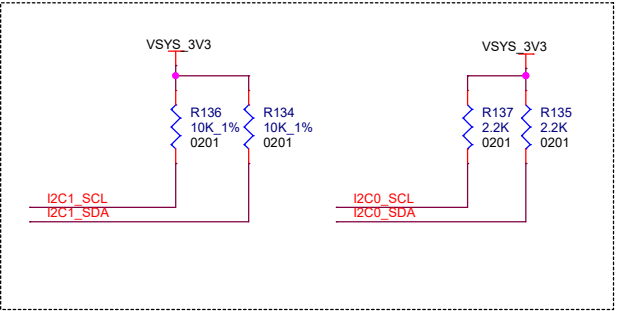
(VDDSHV2)

General PN: J784S4
SR1.0
Symbol: v1.1

BGA Map: v1.0
TDA4xx DM: <tbd>

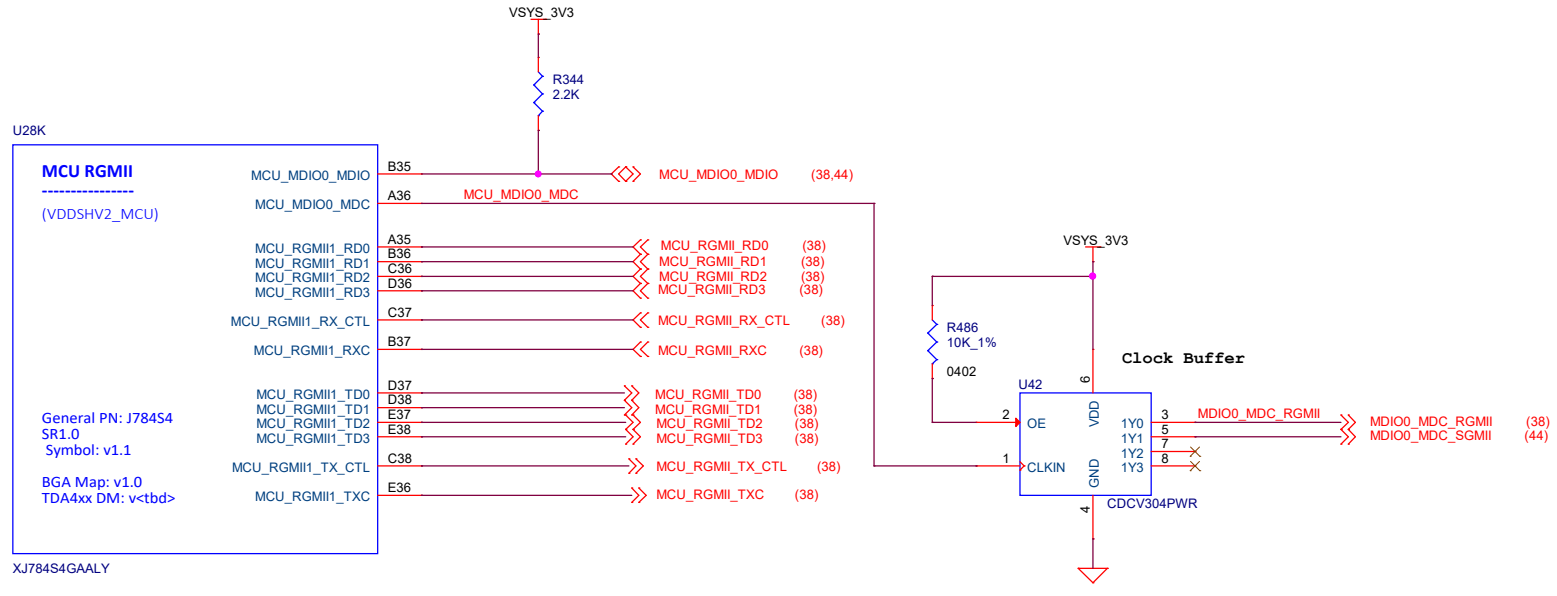


I2C Pull Ups

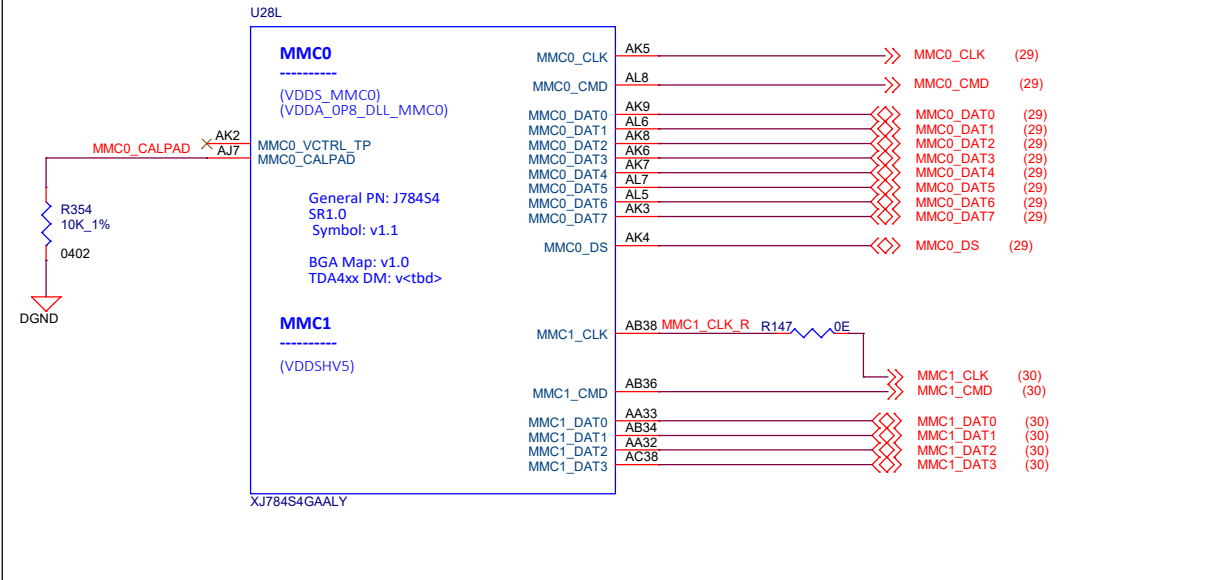


XJ784S4GAALY

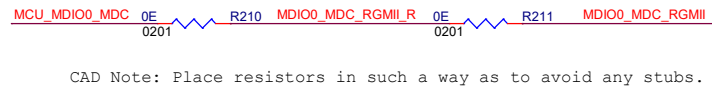
MCU_RGMII



MMC0 and MMC1

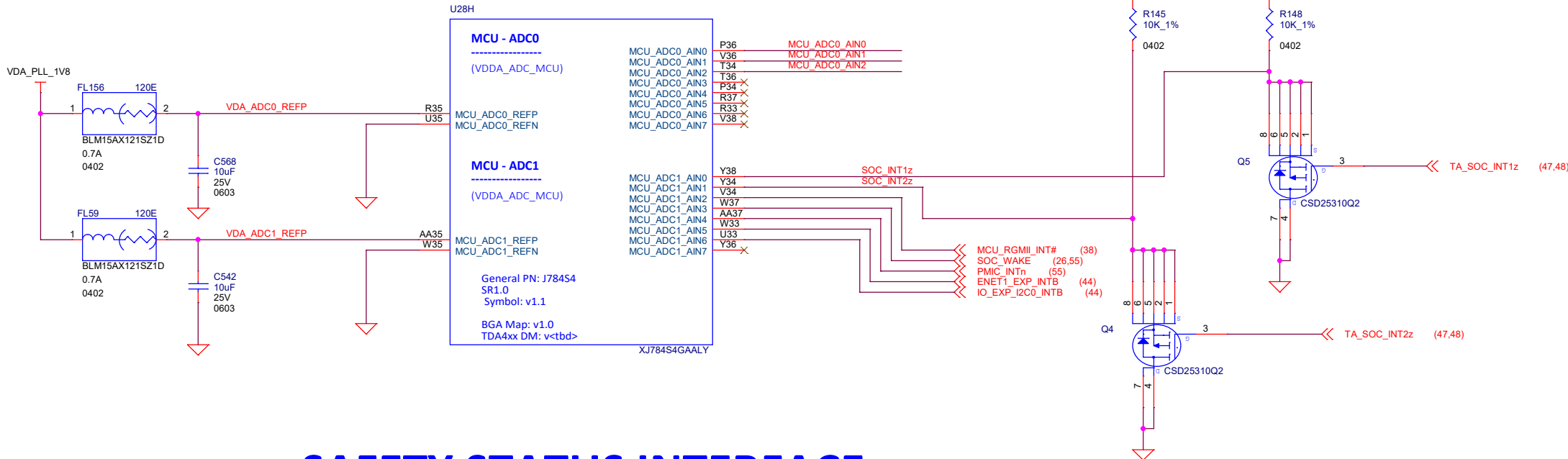


Resistor option to bypass clock buffer.

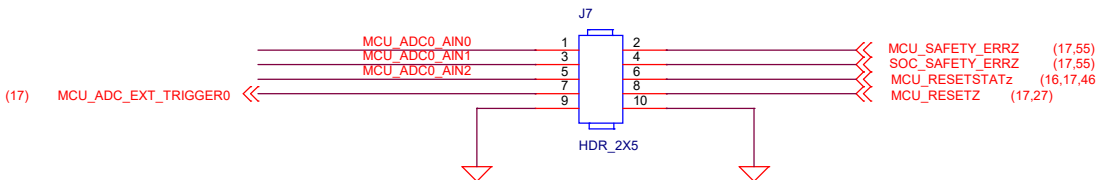


CAD Note: Place resistors in such a way as to avoid any stubs.

MCU_ADC



SAFETY STATUS INTERFACE



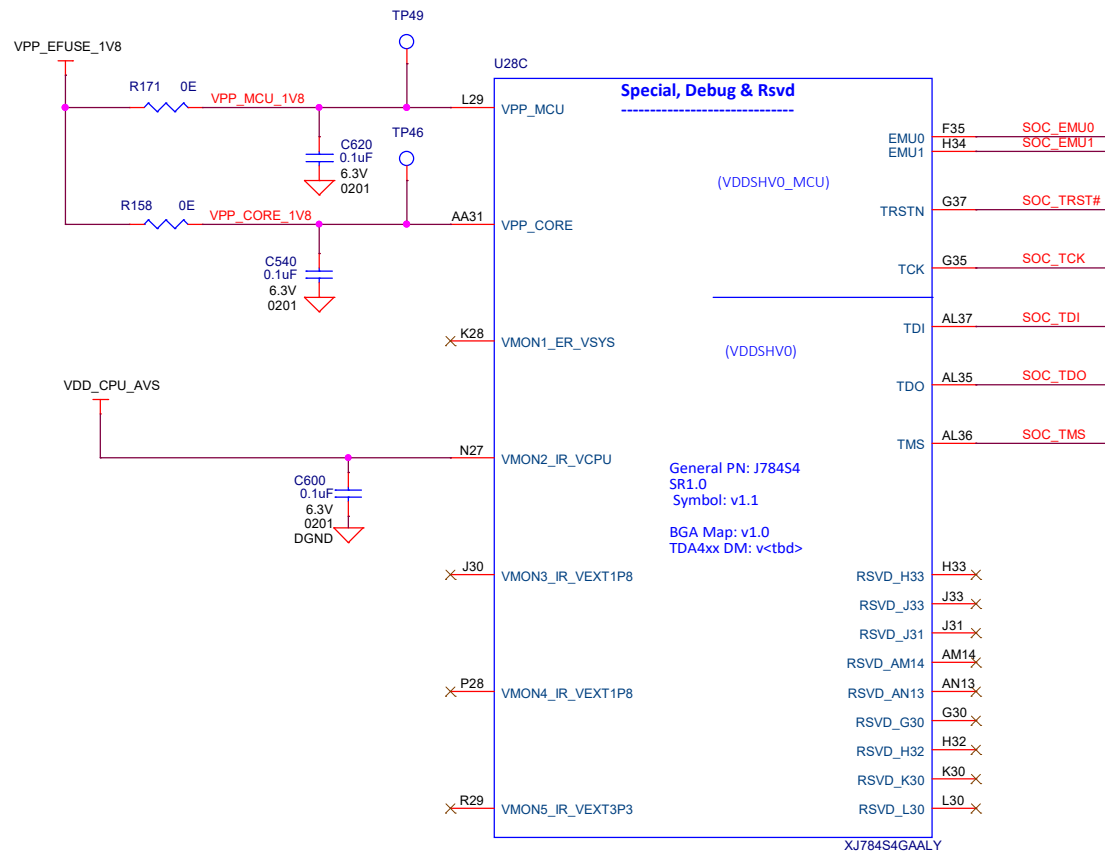
Project :
TDA4VM Edge AI Kit



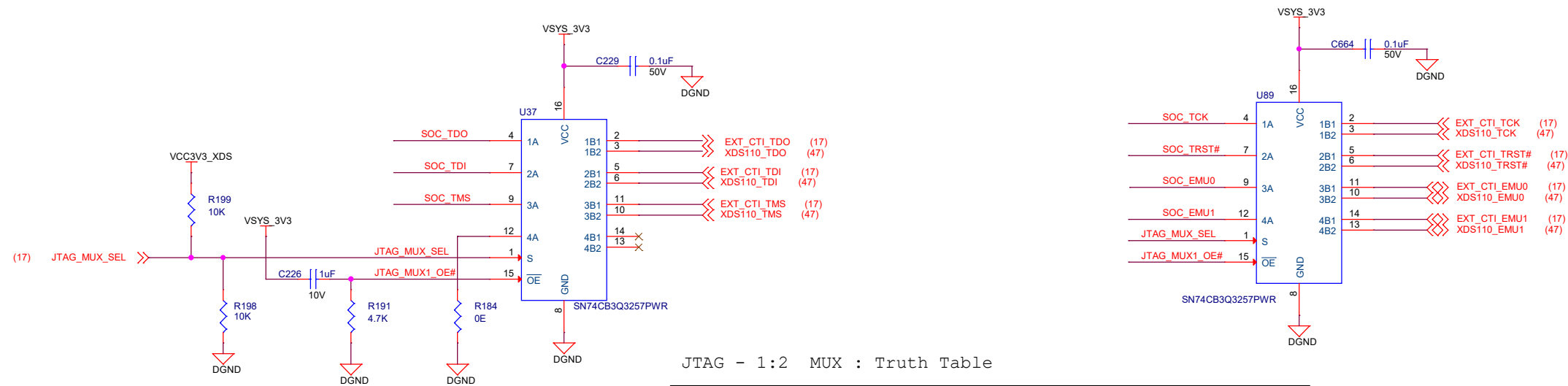
Title
SOC - MCU RGMII / MMC[0:1] / MCU ADC

Size	Rev
C	E1
Date:	Monday, October 17, 2022
Sheet	19 of 62

SPECIAL, DEBUG & RSVD



JTAG CONNECTOR AND XDS110 MUX



JTAG - 1:2 MUX : Truth Table

MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU]
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]

Project :
TDA4VM Edge AI Kit

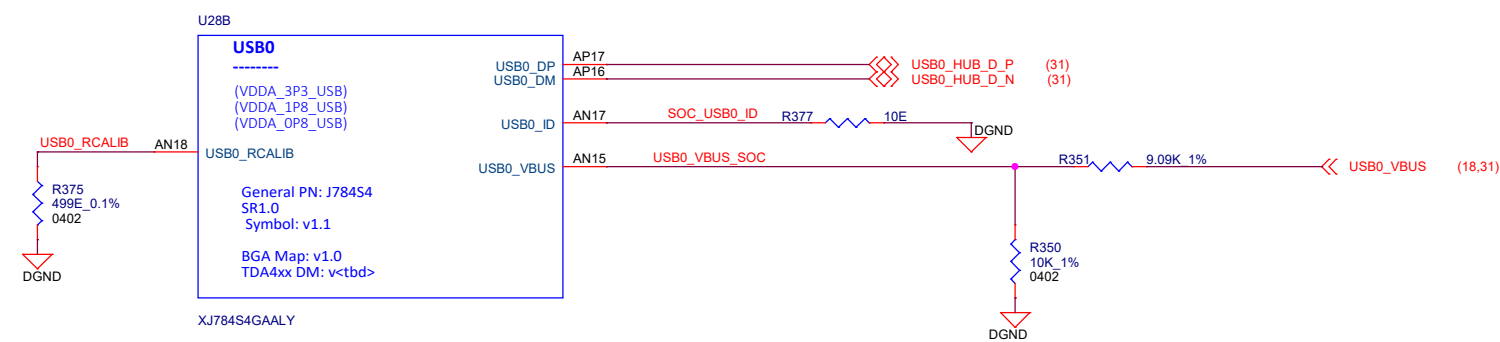


Title
SOC - DEBUG & VMON

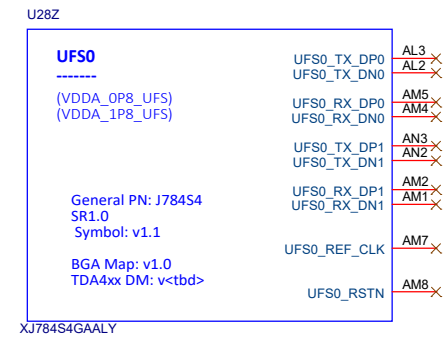
Size	Rev
C	E1
Date: Monday, October 17, 2022	Sheet 20 of 62

USB0 2.0

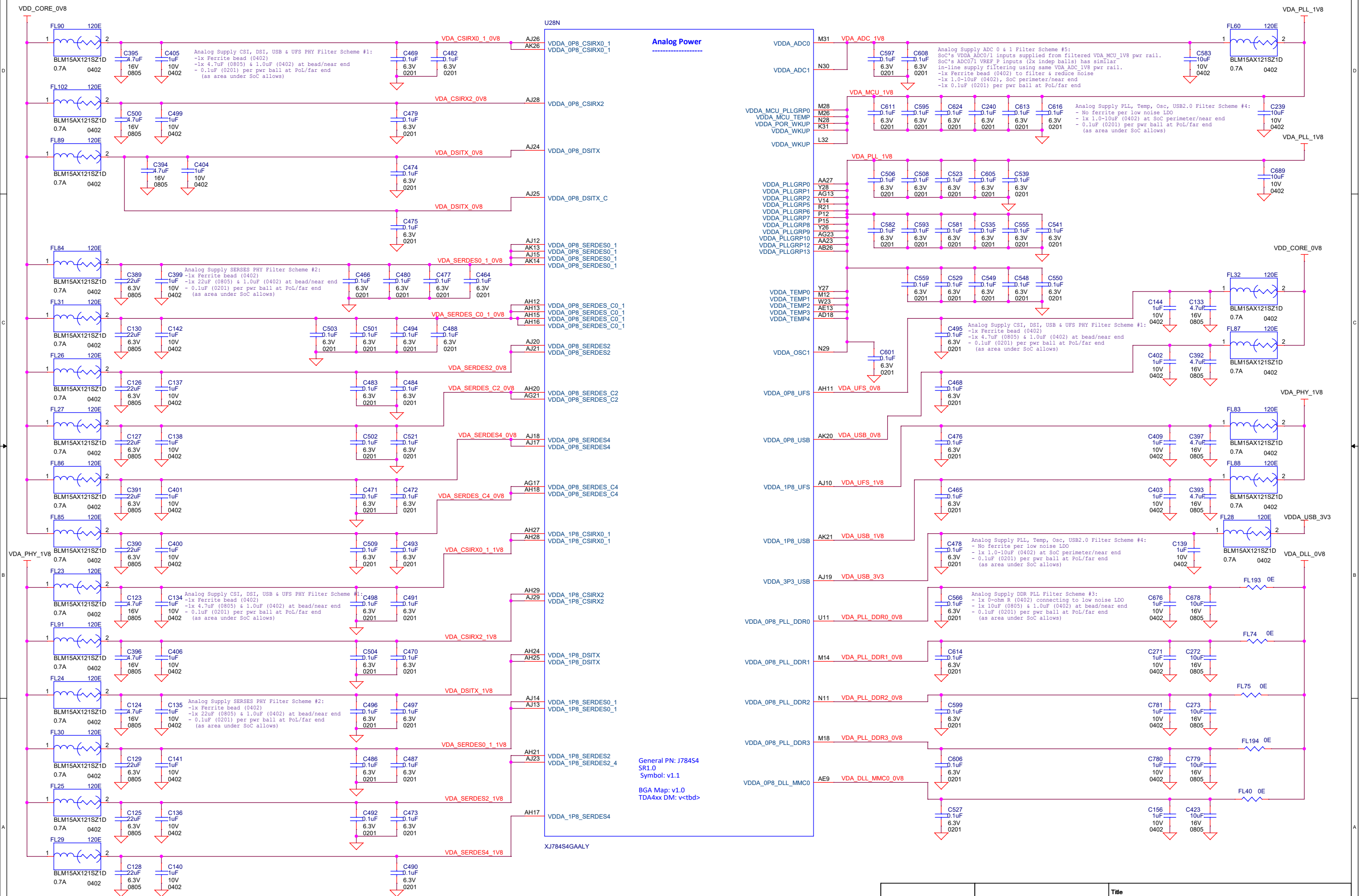
USB VBUS Resistor divider circuit



UFS FLASH



ANALOG POWER 1



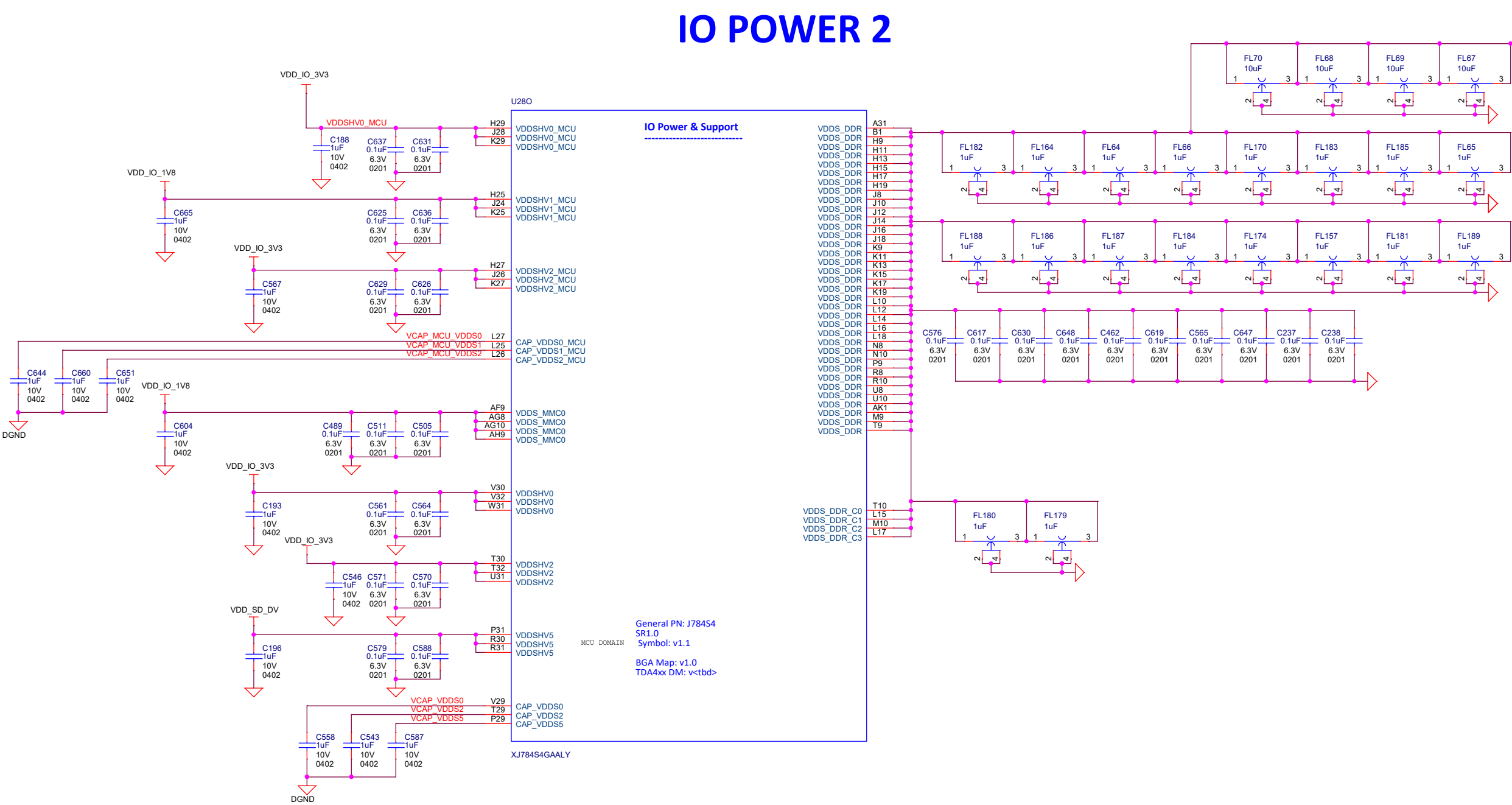
Project :
TDA4VM Edge AI Kit



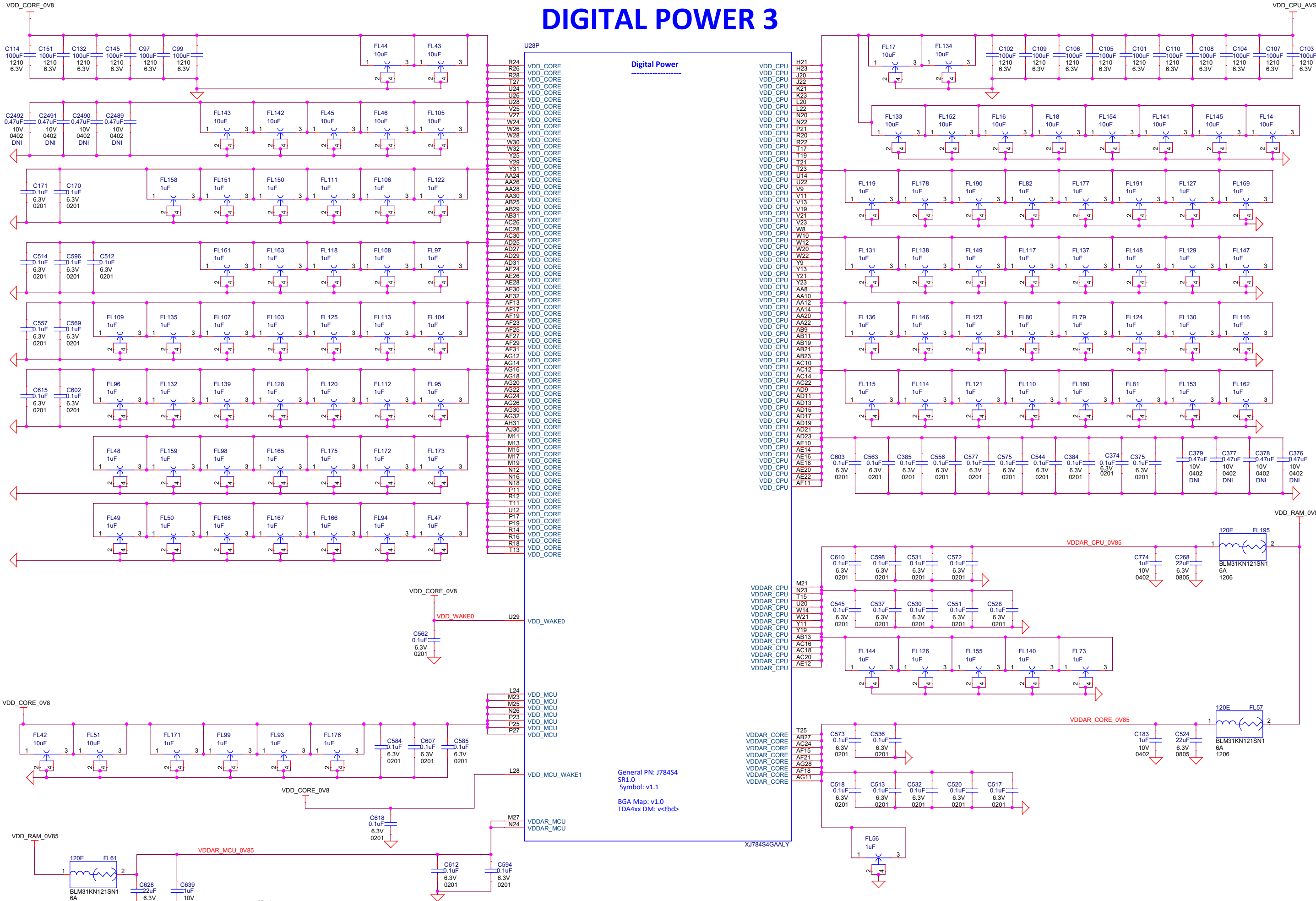
Title	SOC - ANALOG POWER 1
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Size	<Core Design>	Rev
C		E1
Date:	Monday, October 17, 2022	Sheet 22 of 62

IO POWER 2



DIGITAL POWER 3



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this SK PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project

TDA4VM Edge AI Ki

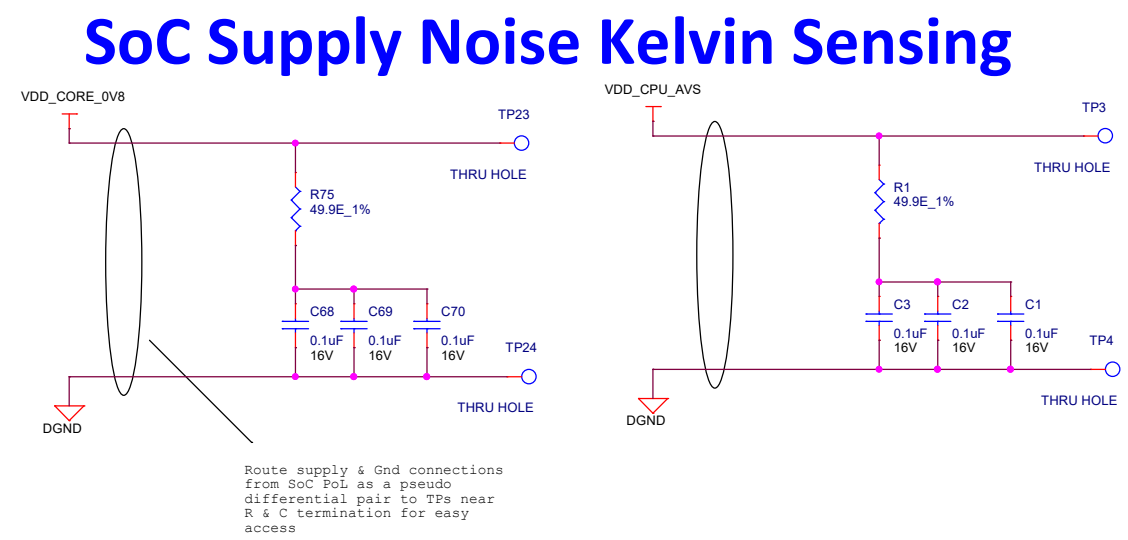
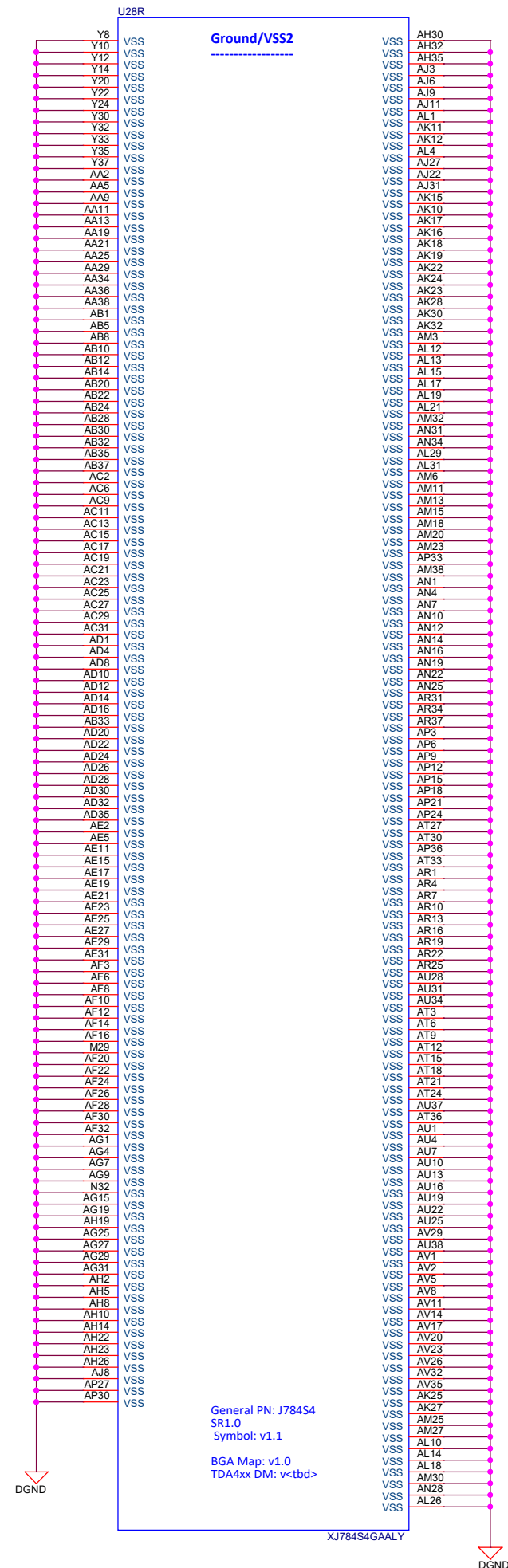
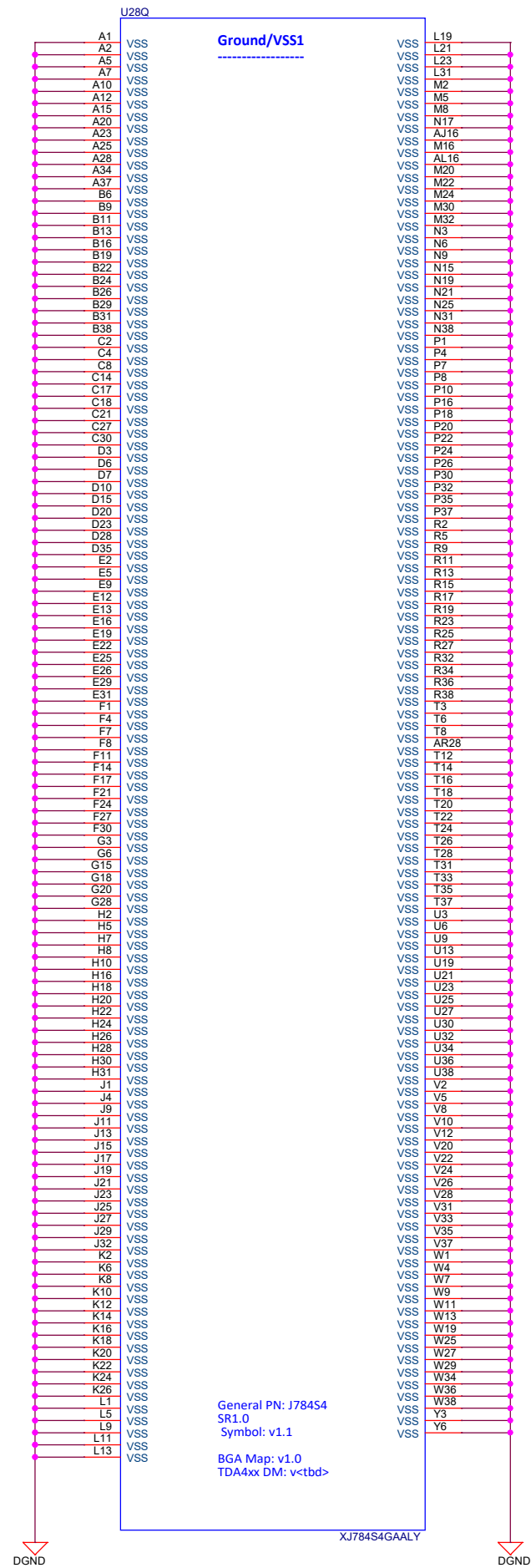


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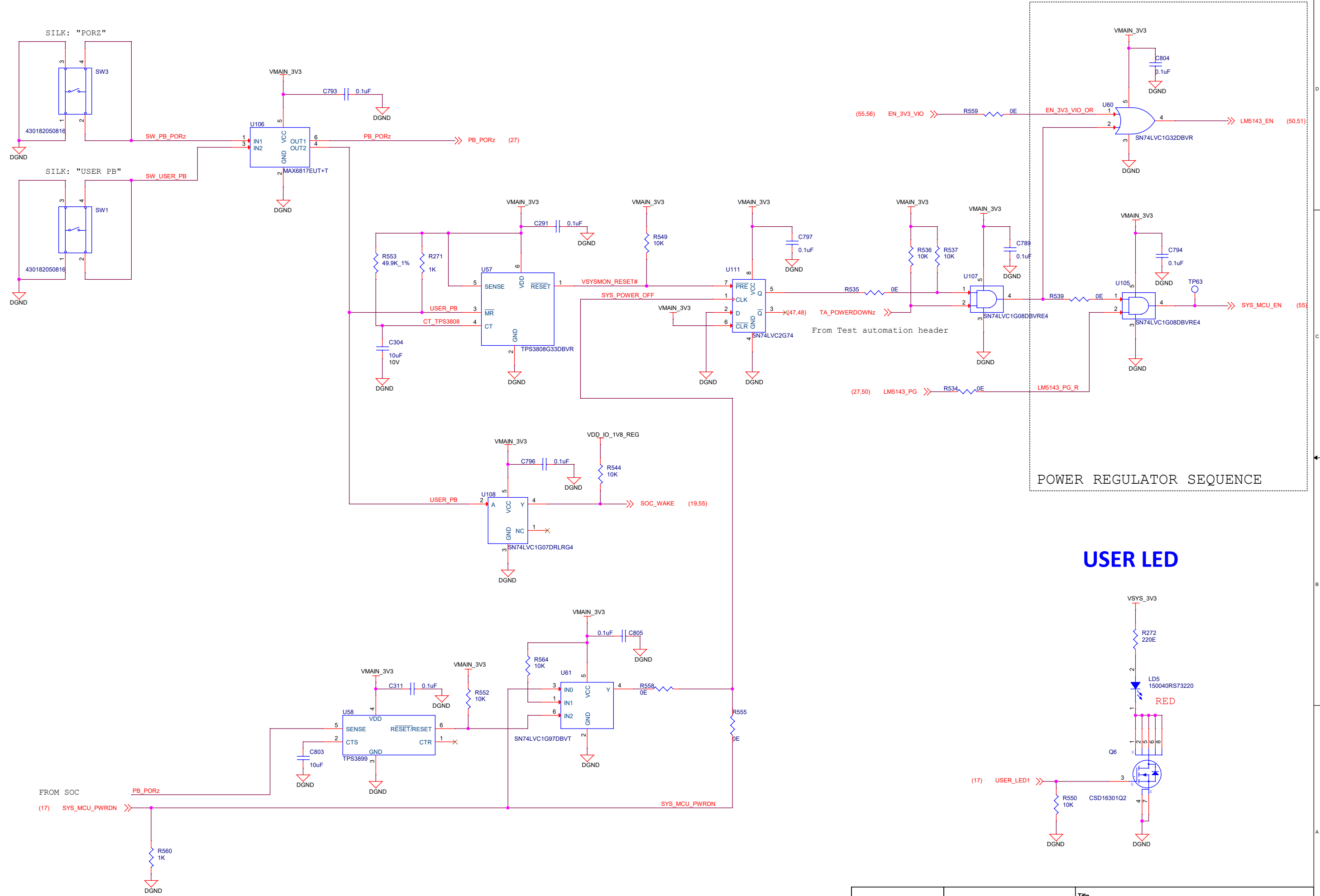
SOC - DIGITAL POWER

Size	<Core Design>	Rev
C		E1
Date: Monday, October 31, 2022	Sheet 24 of	62

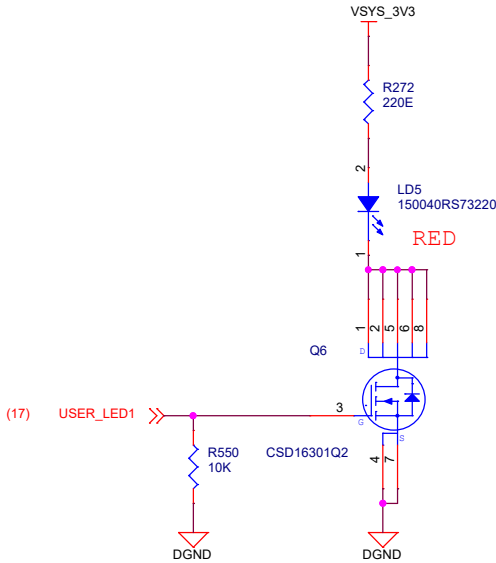
SOC GROUND



RESET BUTTONs

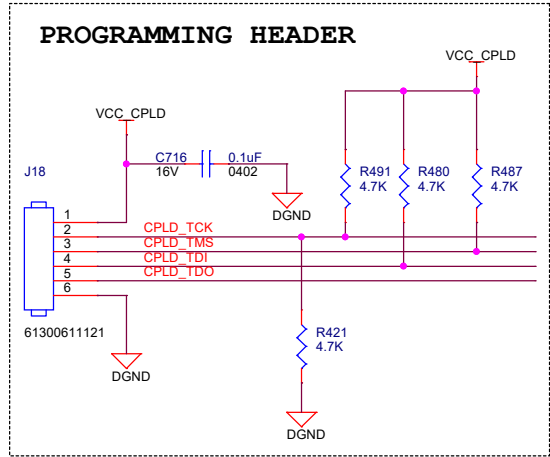


USER LED

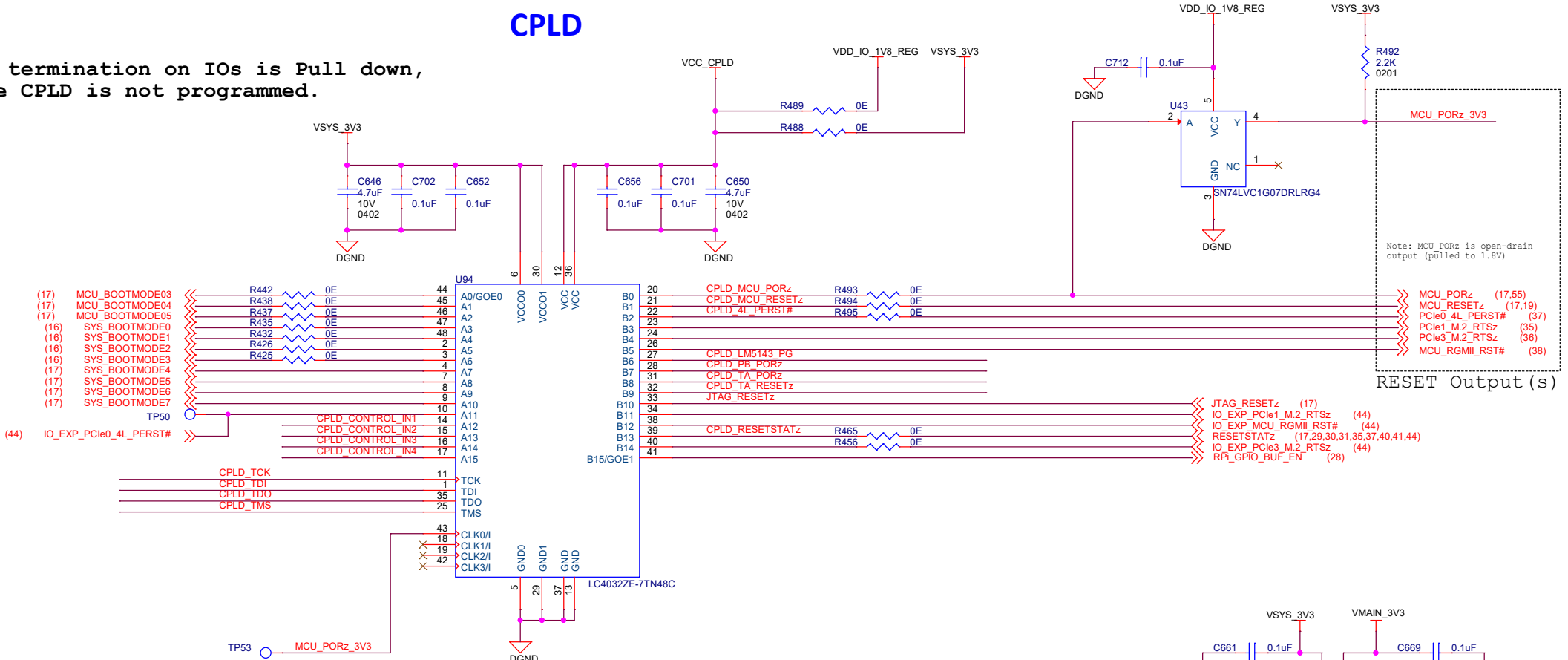


CPLD

Default termination on IOs is Pull down,
when the CPLD is not programmed.

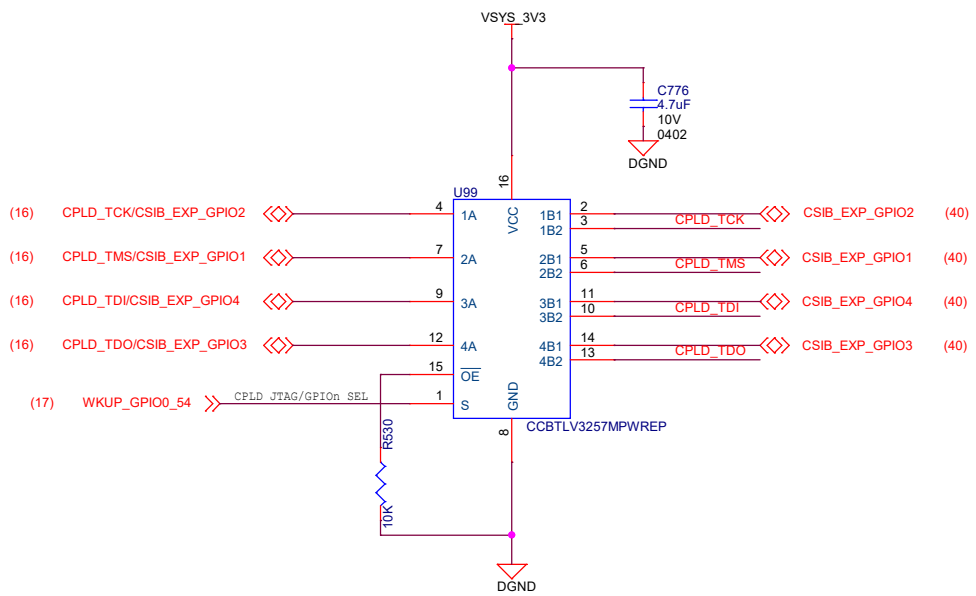


Silk Screen "CPLD JTAG"



Note: MCU PORz is open-drain output (pulled to 1.8V)

RESET Output(s)

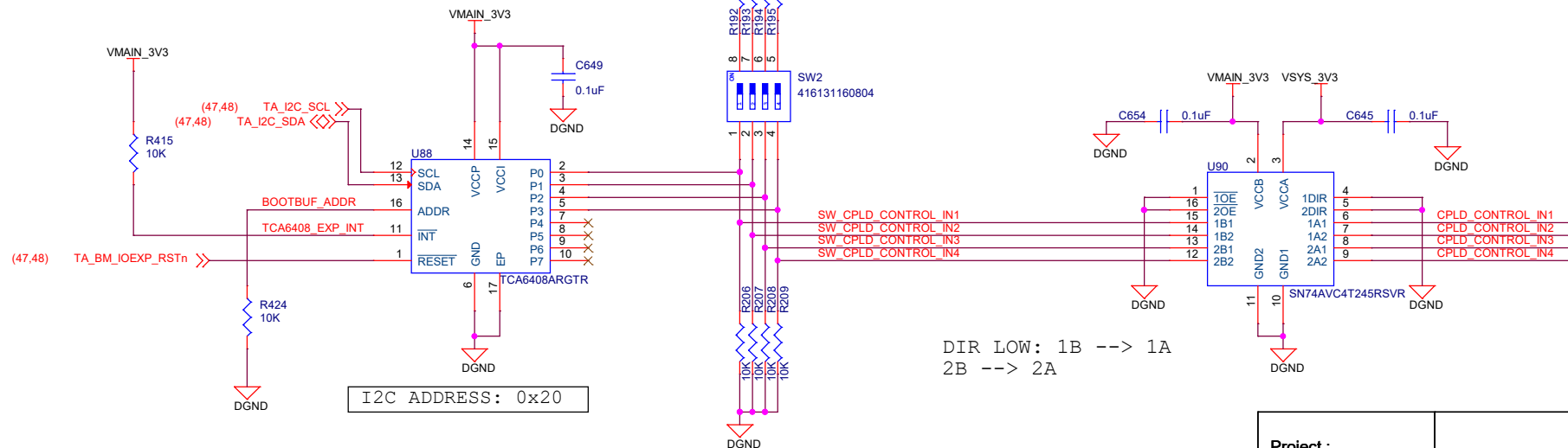


Test Automation BOOTMODE Logic

Note: Test Automation logic to set desired BOOTMODE.

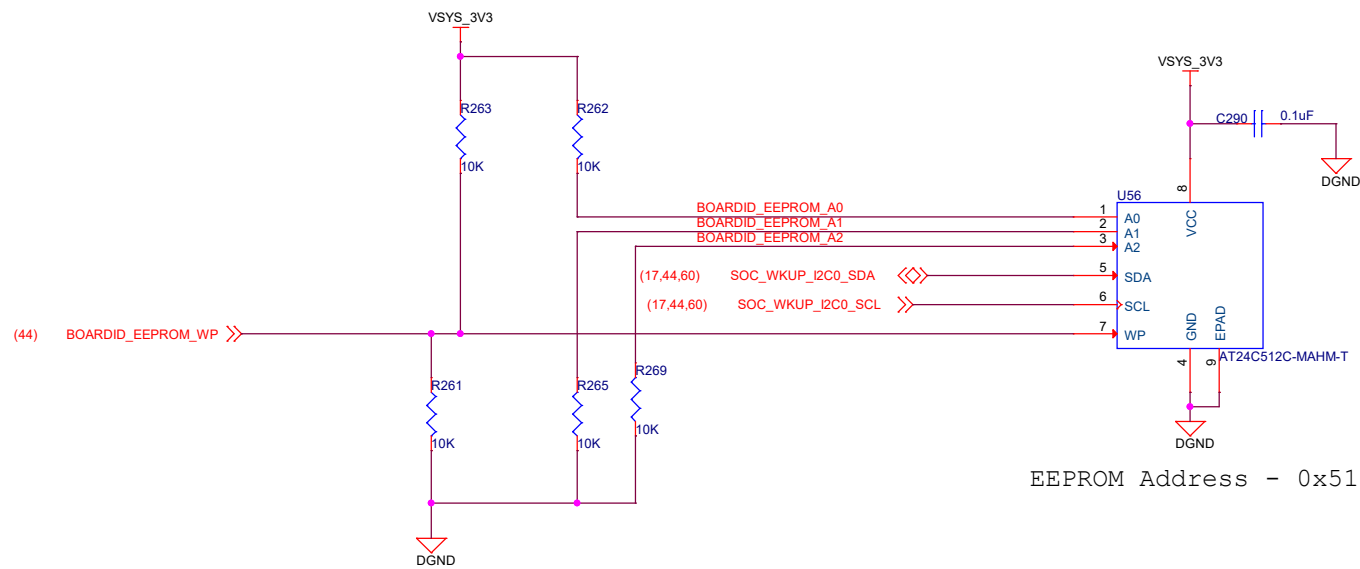
Bootmode Table

SW2.3	SW2.2	SW2.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	USB - 0 (DFU)
0	1	1	USB - 1 (DFU)
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	PCIe
1	1	1	xSPI SFDP



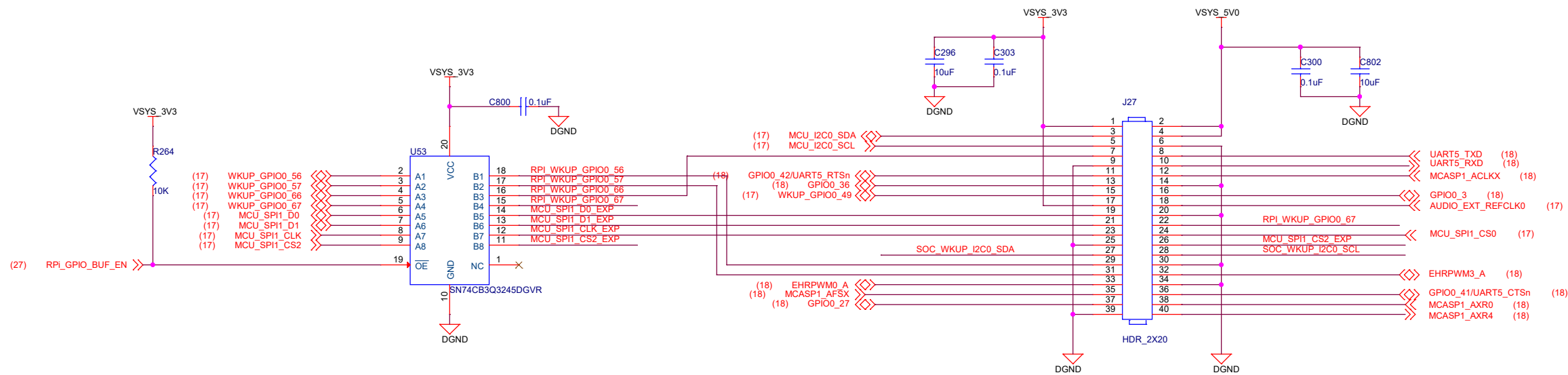
DIR LOW: 1B --> 1A
2B --> 2A

BOARD ID EEPROM



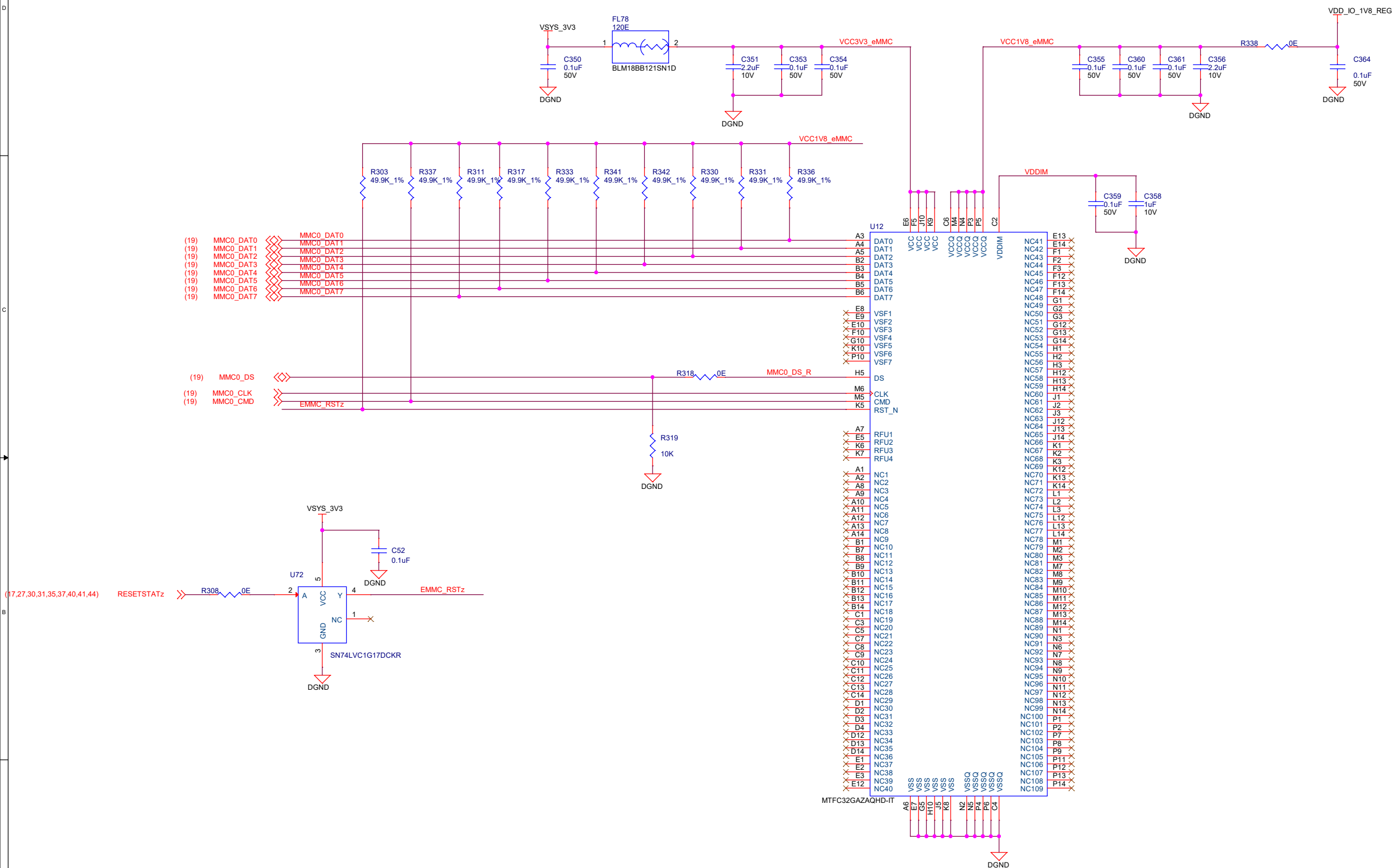
EEPROM Address - 0x51

40Pin Expansion Header

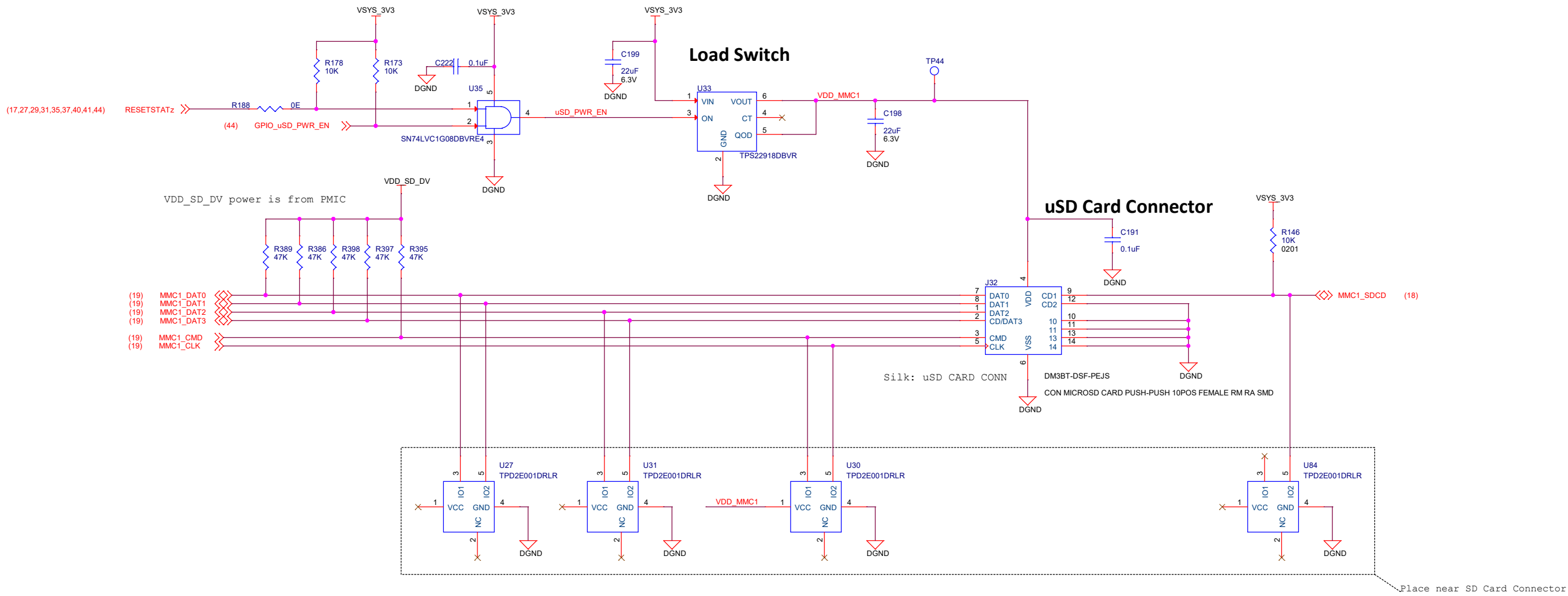


Silk Screen "40p EXP HDR"

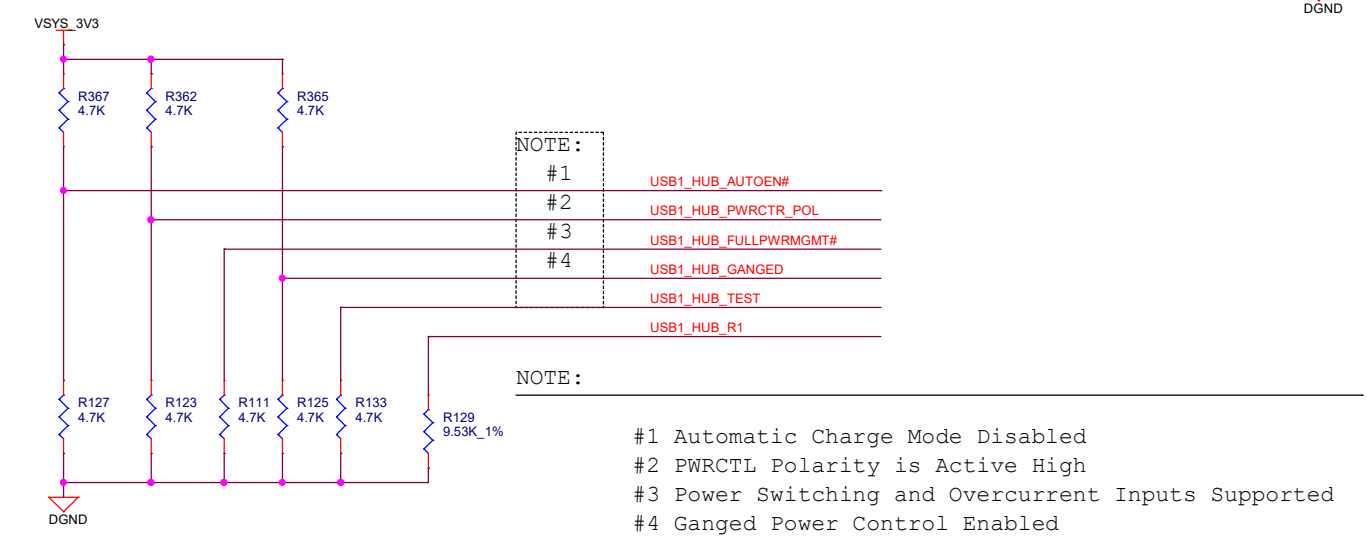
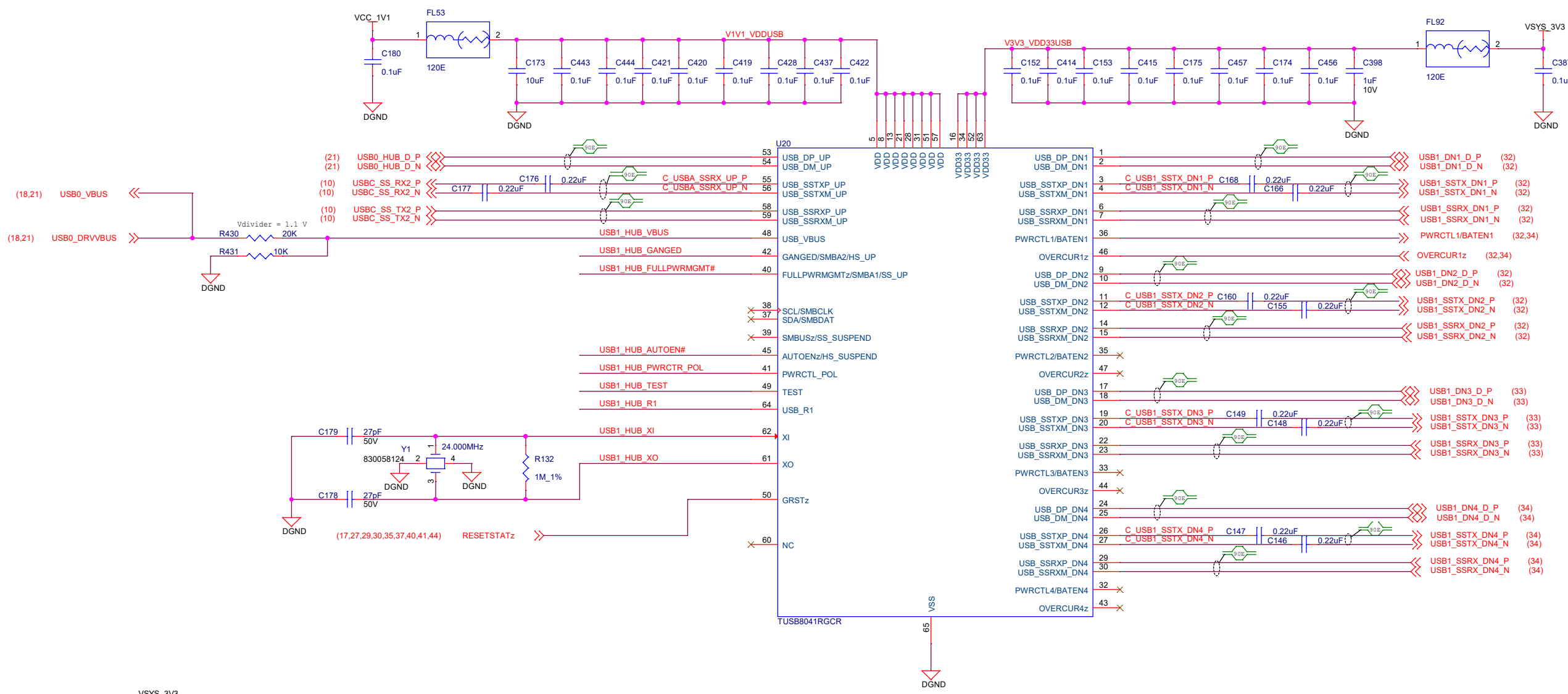
eMMC FLASH



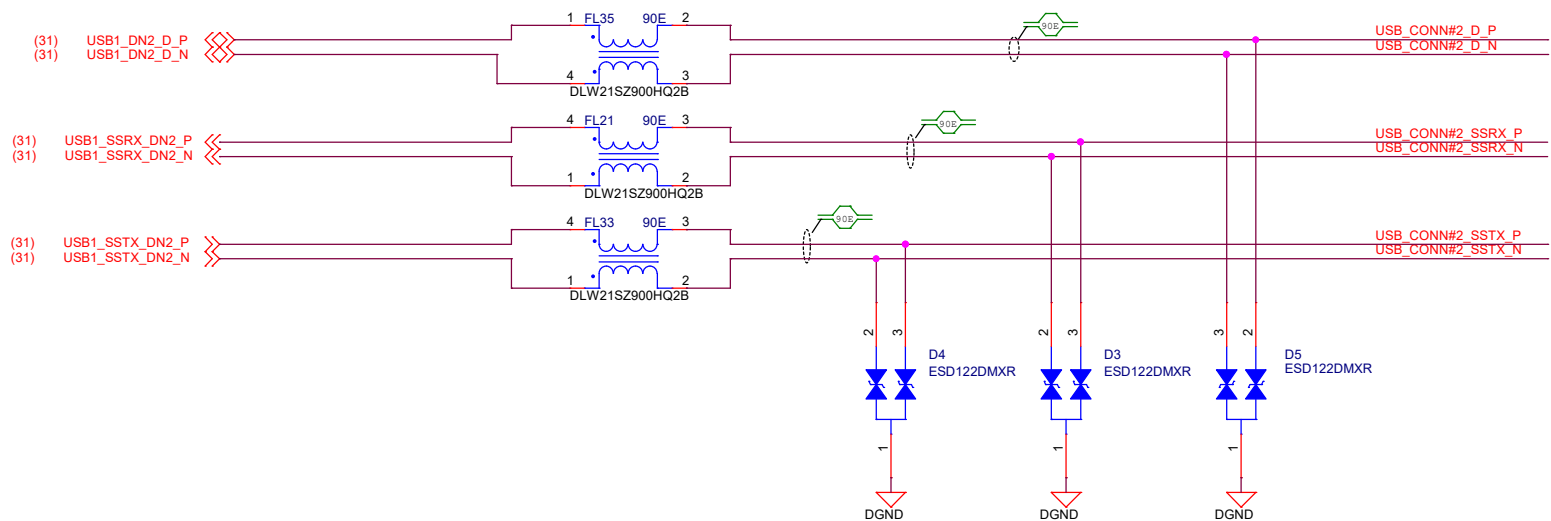
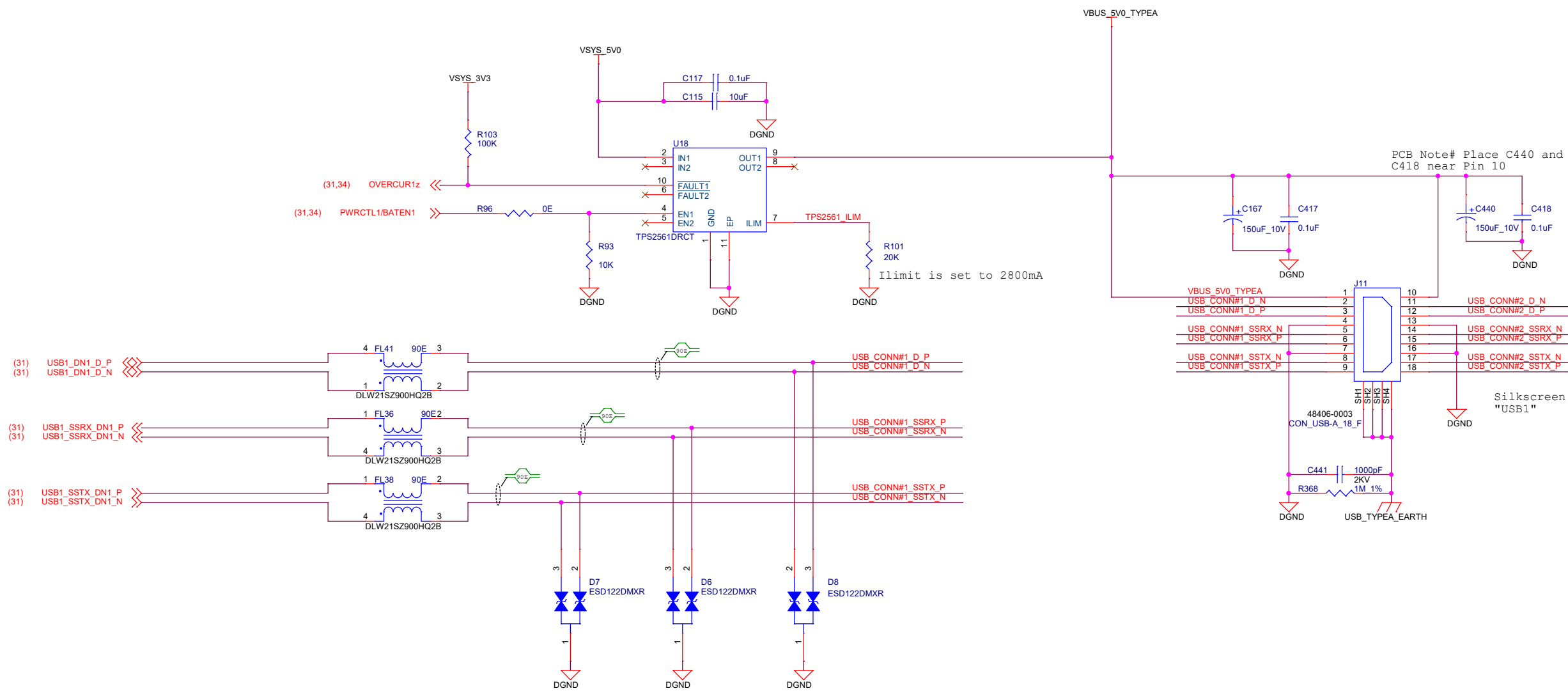
Micro SD CARD INTERFACE



USB3.0 HUB



USB 3.0 TYPE-A CONNECTORS - 1



Project :
TDA4VM Edge AI Kit



Title
USB 3.0 TYPE-A CONNECTORS - 1

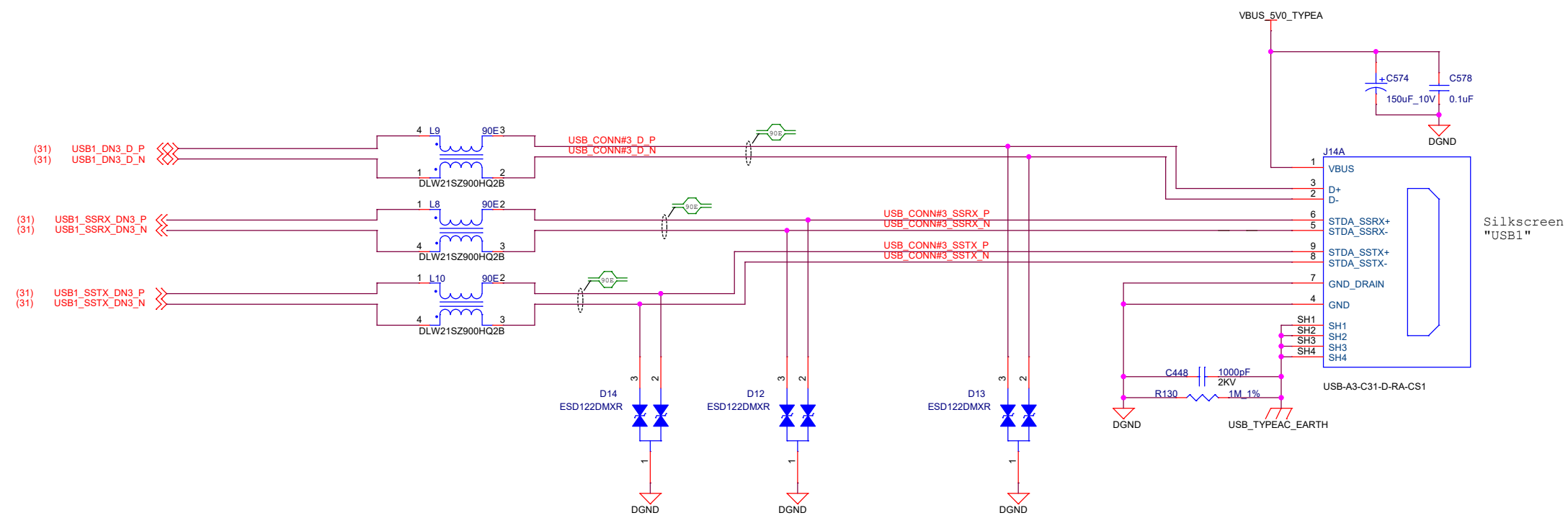
Size
C <Core Design>

Date: Monday, October 17, 2022

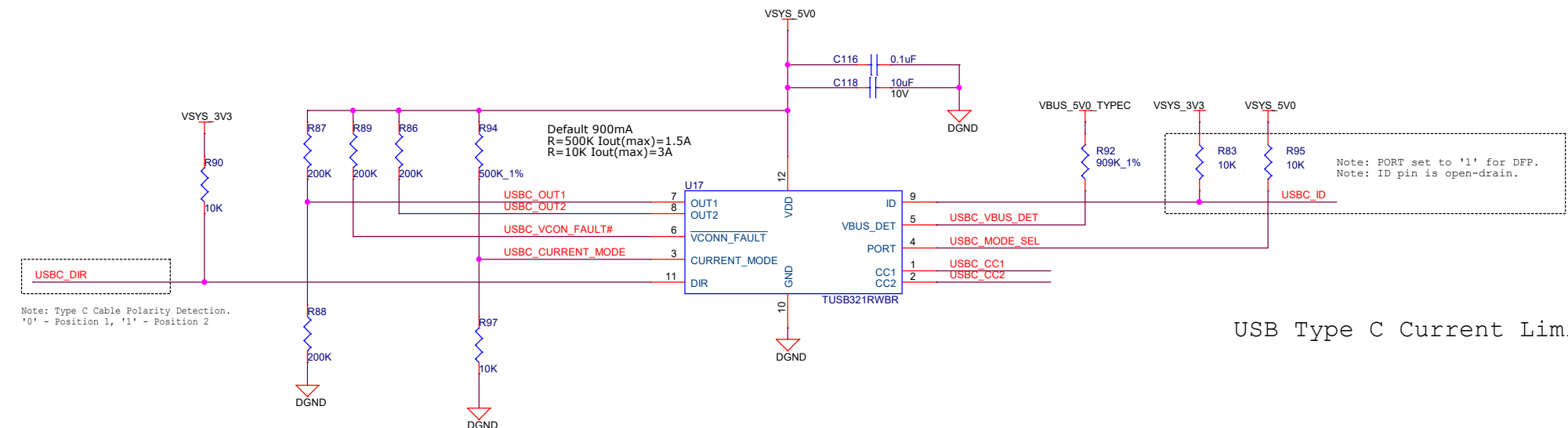
Sheet 32 of 62

Rev
E1

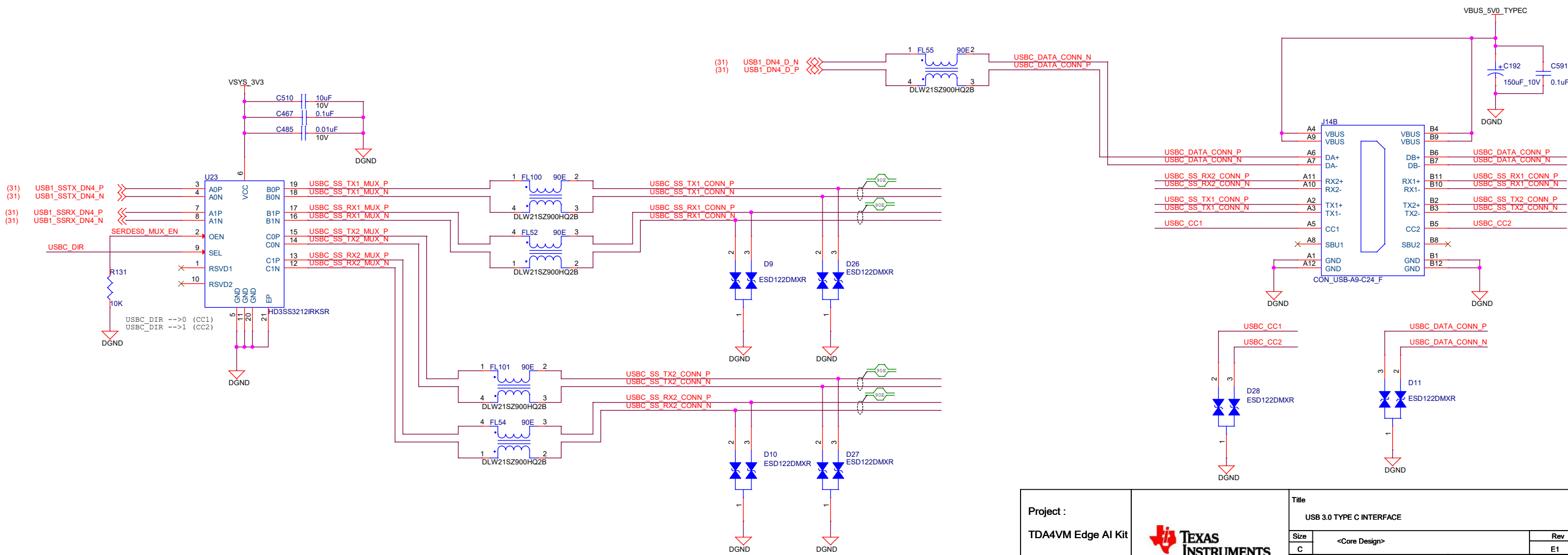
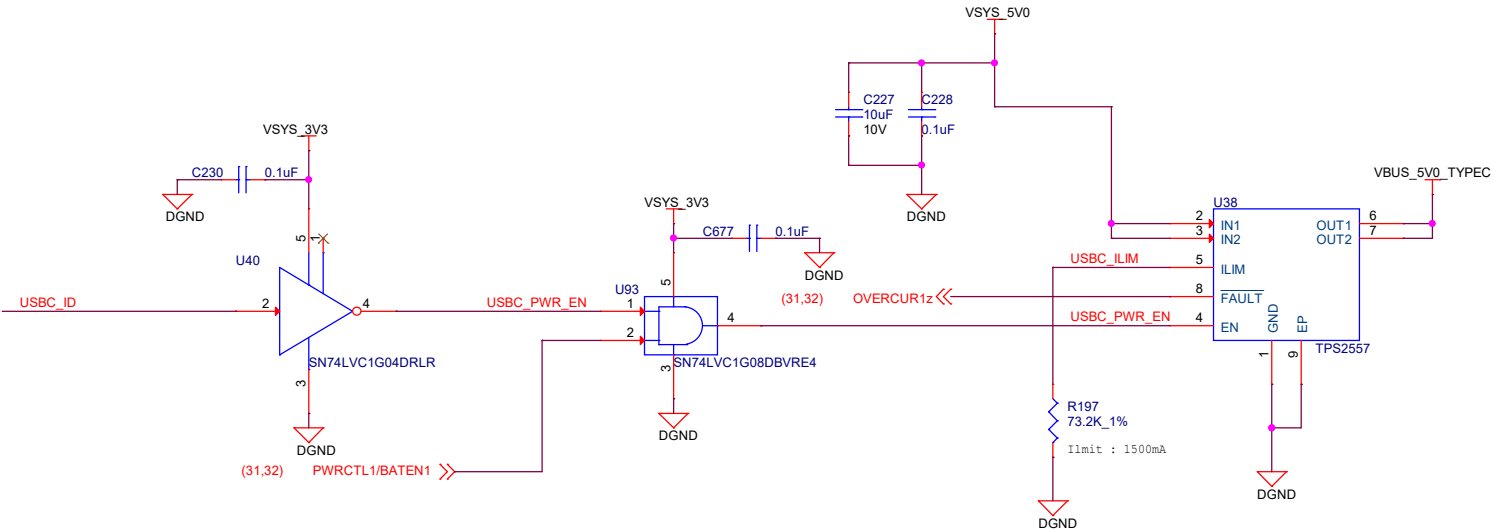
USB 3.0 TYPE-A CONNECTORS - 2



USB 3.0 TYPE C INTERFACE

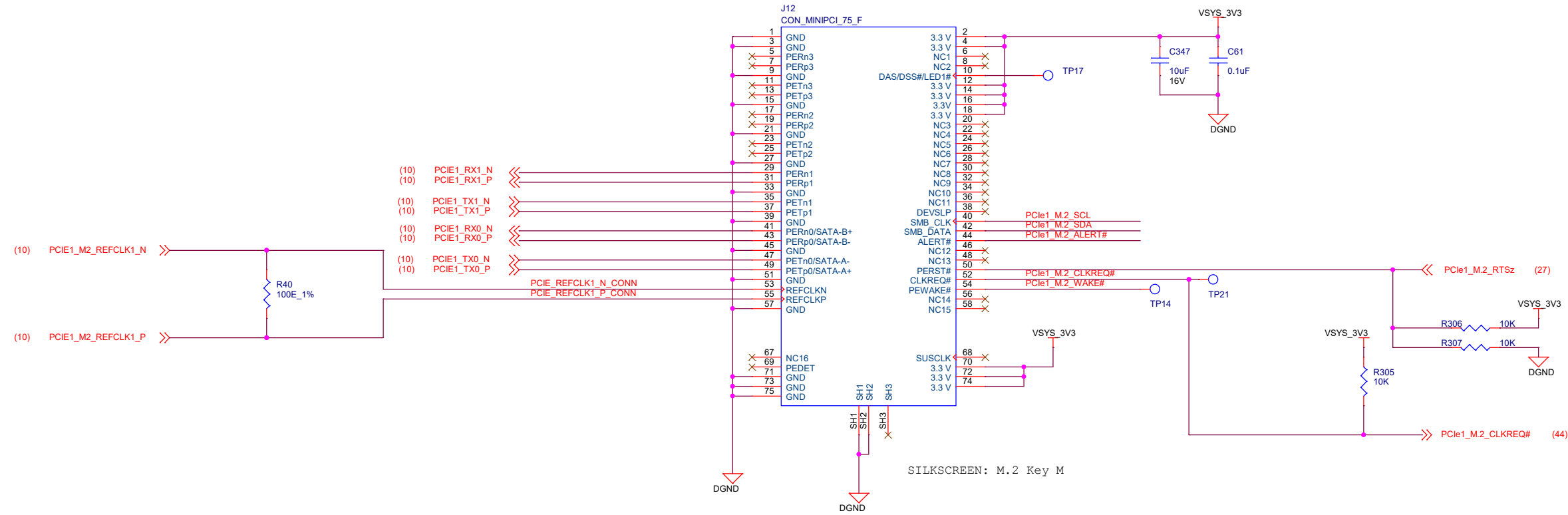


USB Type C Current Limit

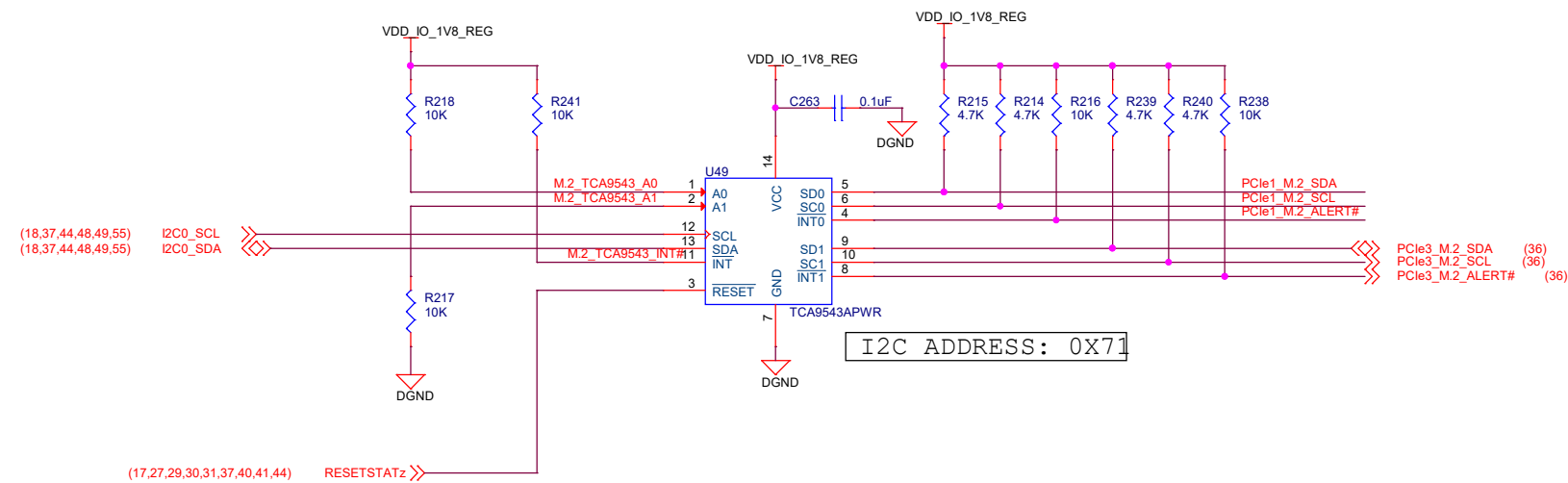


PCIe_M.2_INTERFACE SSD

M KEY



3.3V To 1V8 Level translator



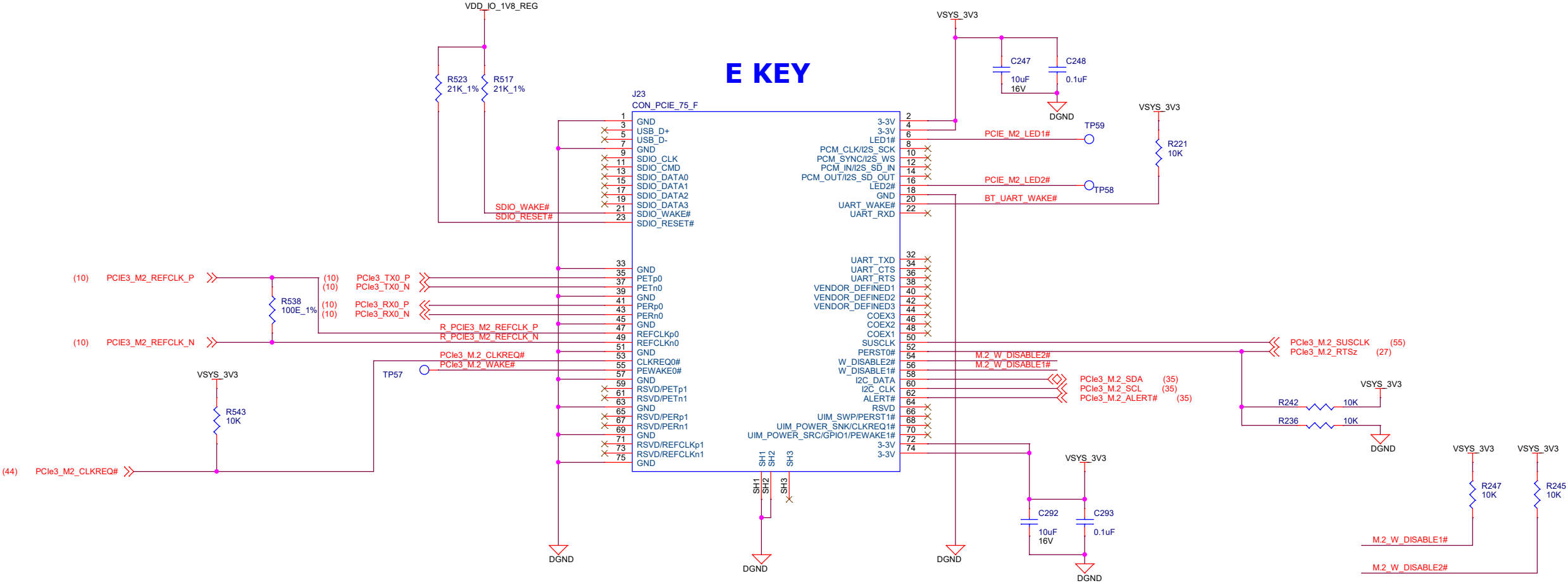
Project :
TDA4VM Edge AI Kit



Title	PCIe_M.2_INTERFACE (M Key)
-------	----------------------------

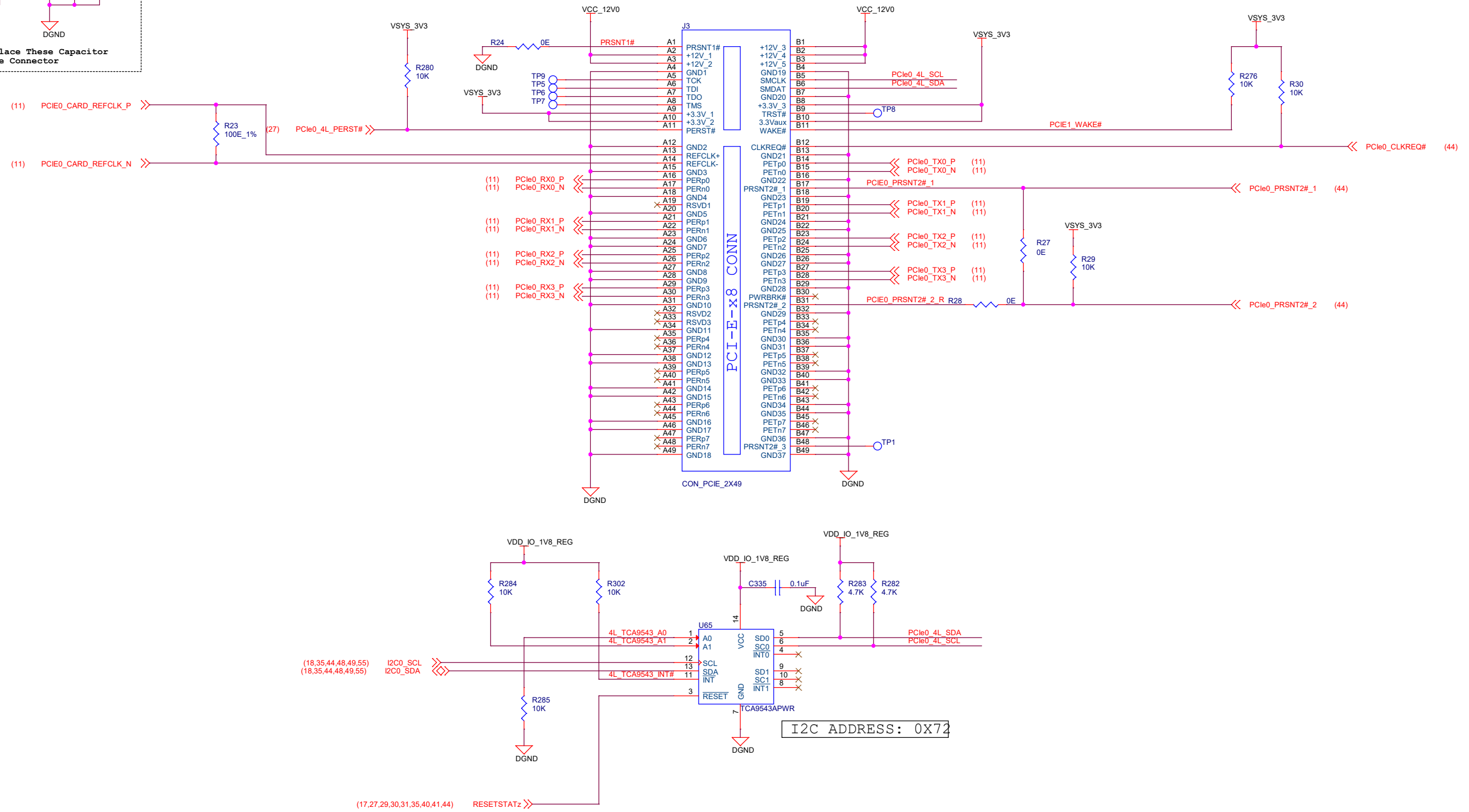
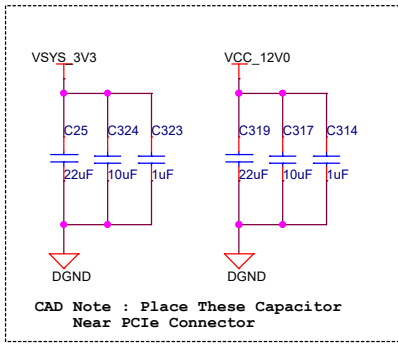
Size	<Core Design>	Rev	
C		E1	
Date:	Monday, October 17, 2022	Sheet	35 of 62

PCIE_M.2_INTERFACE - SDIO

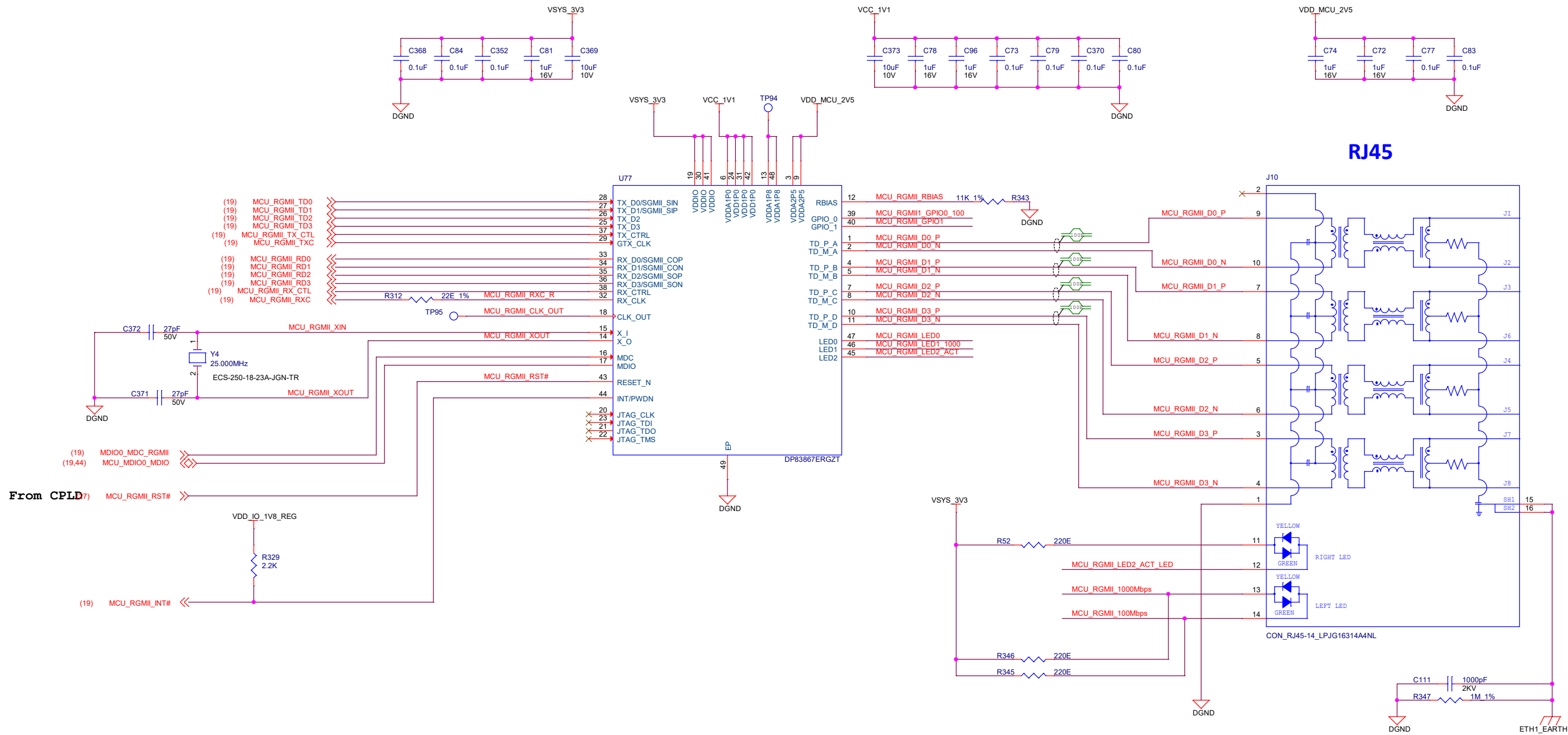


SILKSCREEN: M.2 Key E

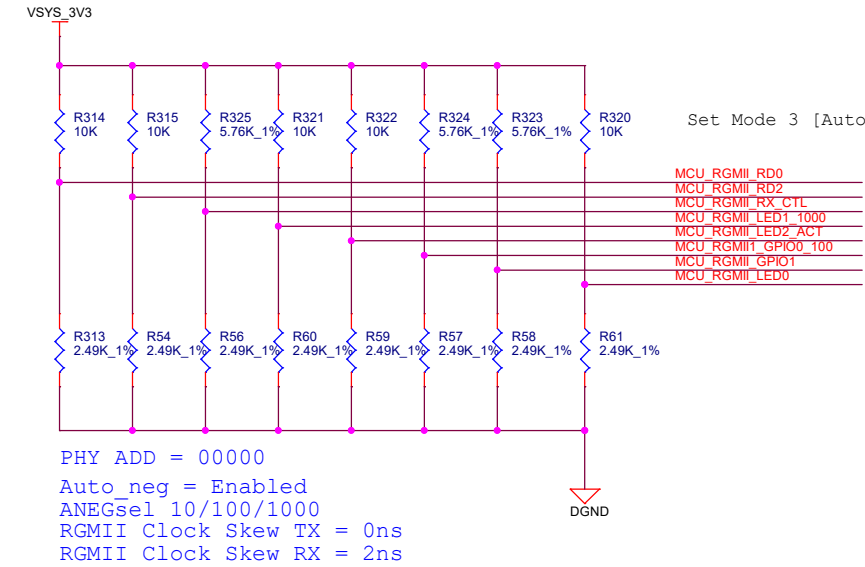
PCIe Card Slot



MCU GB ETHERNET



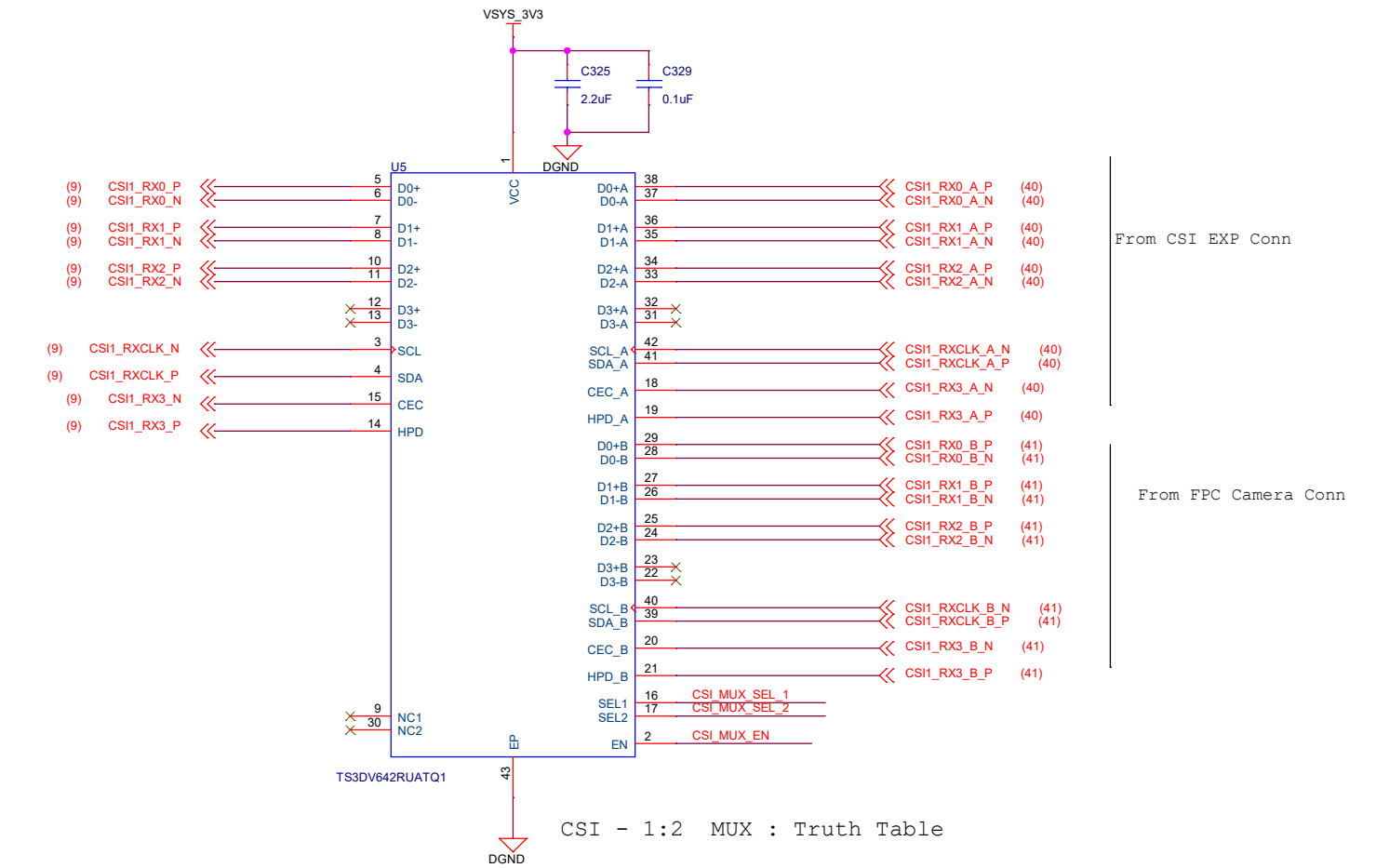
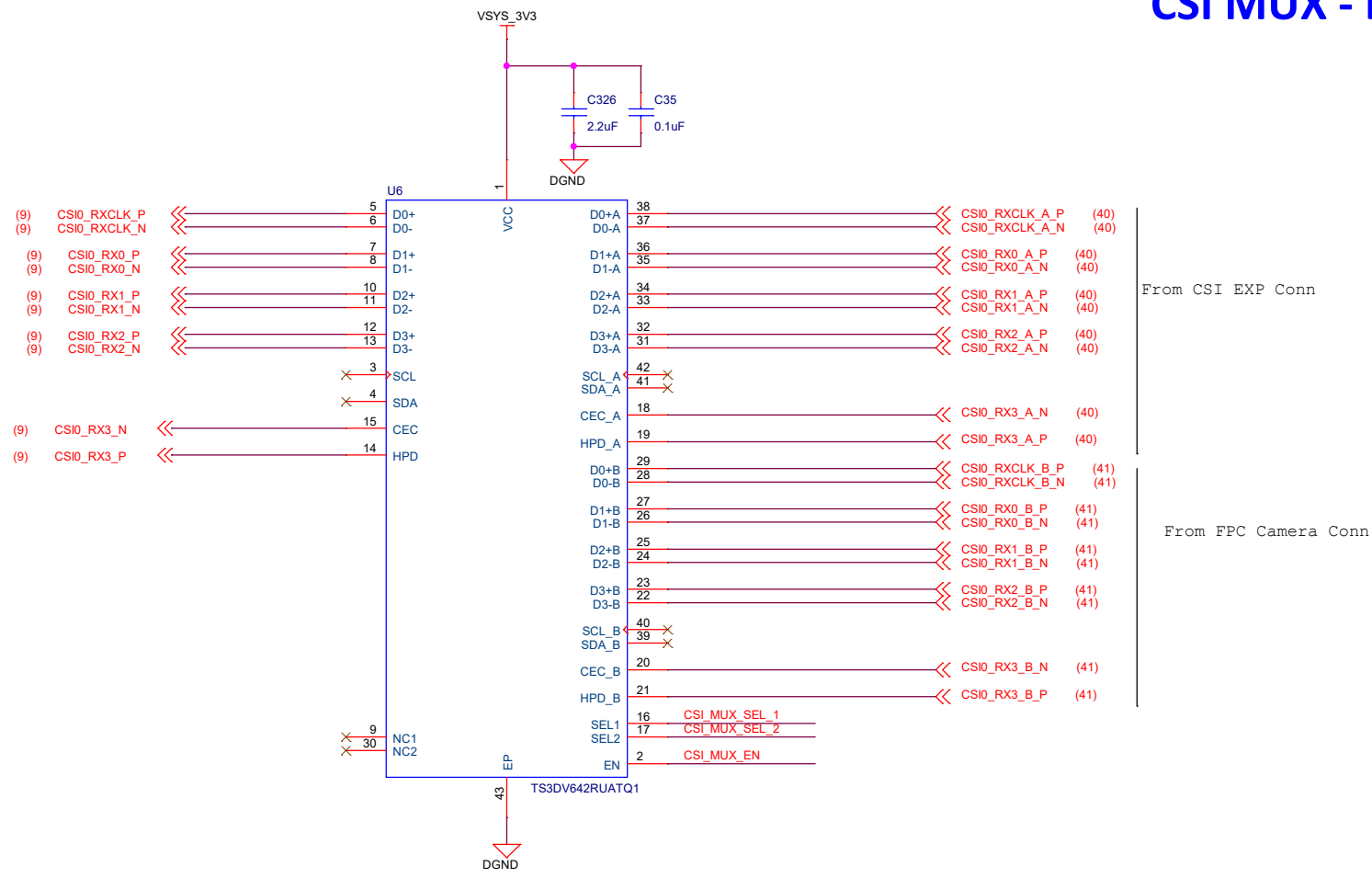
SPEED AND ACTIVITY LED DRIVERS



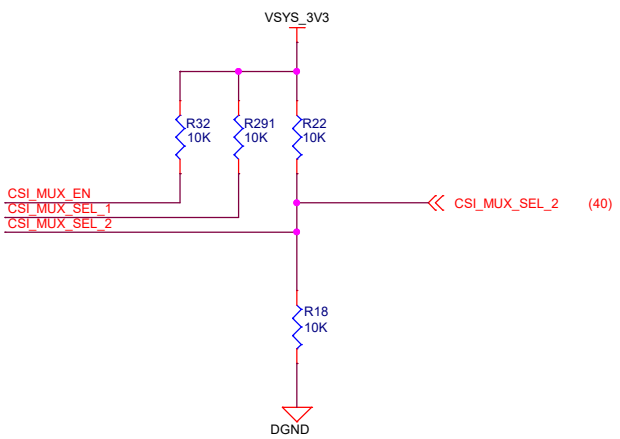
RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

LED_2-MODE1 & LED_1-MODE2-TX SKEW=0ns
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

CSI MUX - DATA

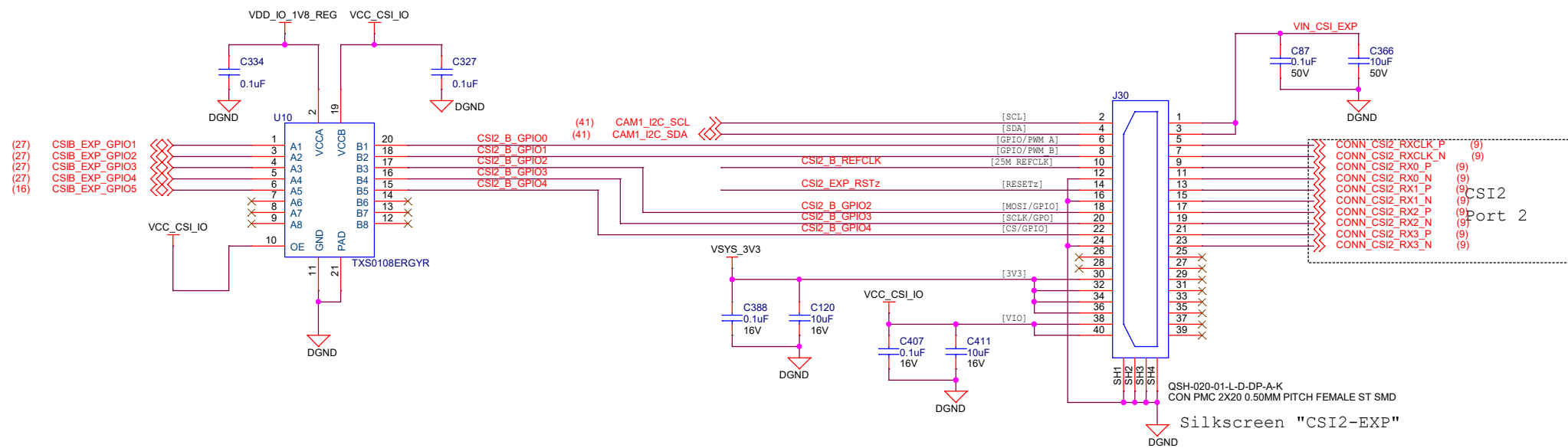
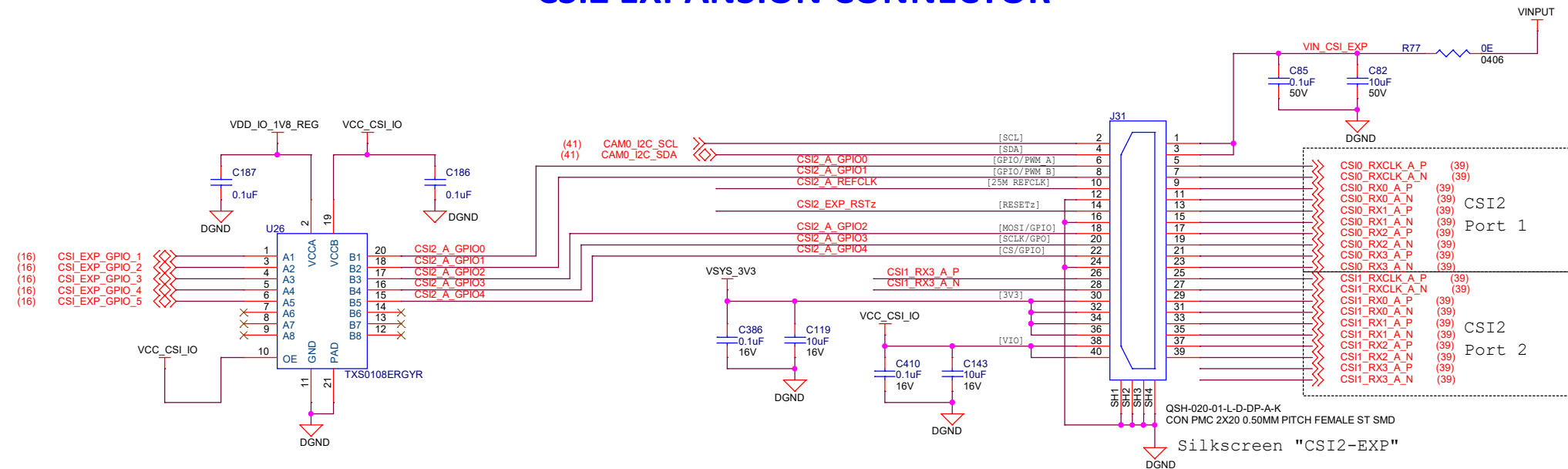


CSI - 1:2 MUX : Truth Table

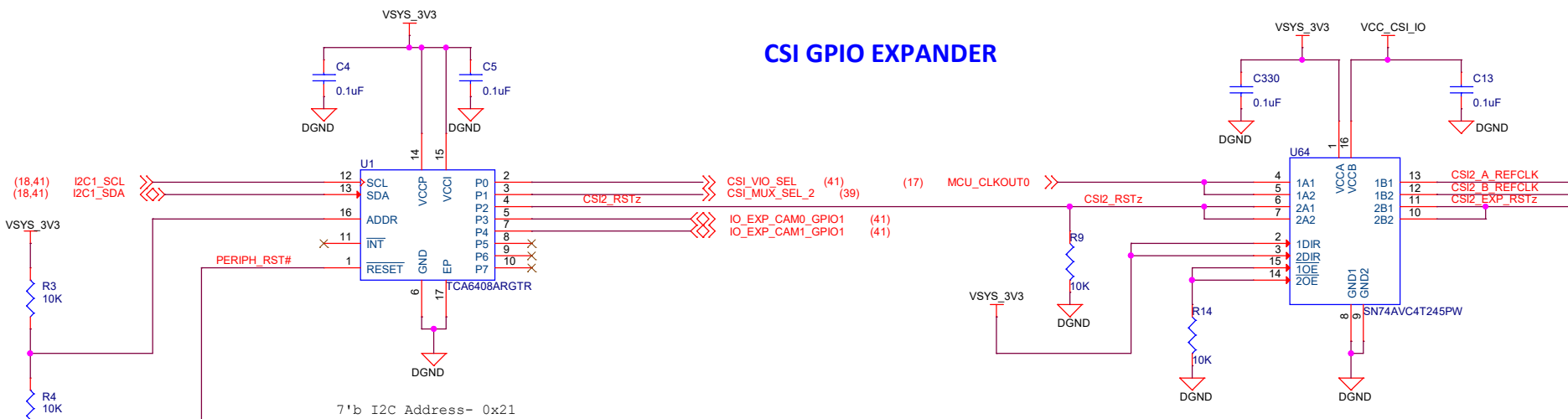


MUX_SEL_2	FUNCTION	
LOW	INPUT<-- A Port [CSI2 Connector]	(default)
HIGH	INPUT<--B port [FPC Camera Connector]	

CSI2 EXPANSION CONNECTOR

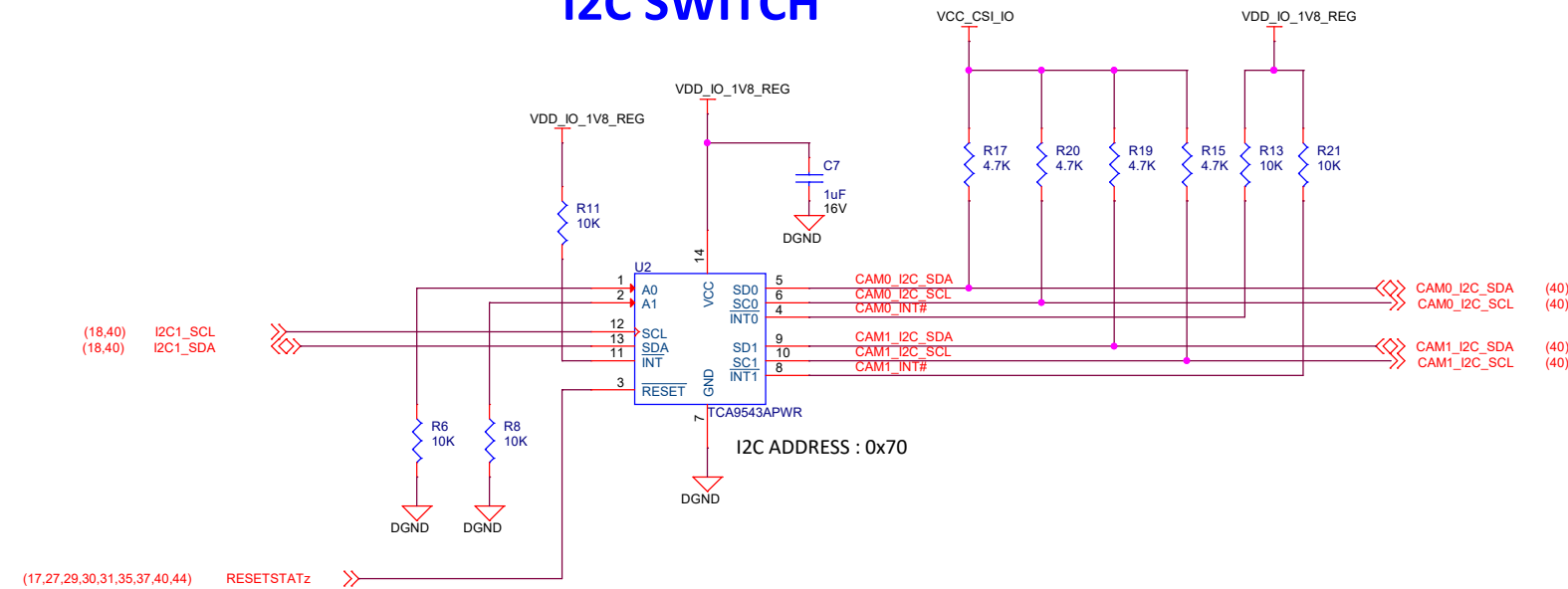


CSI GPIO EXPANDER

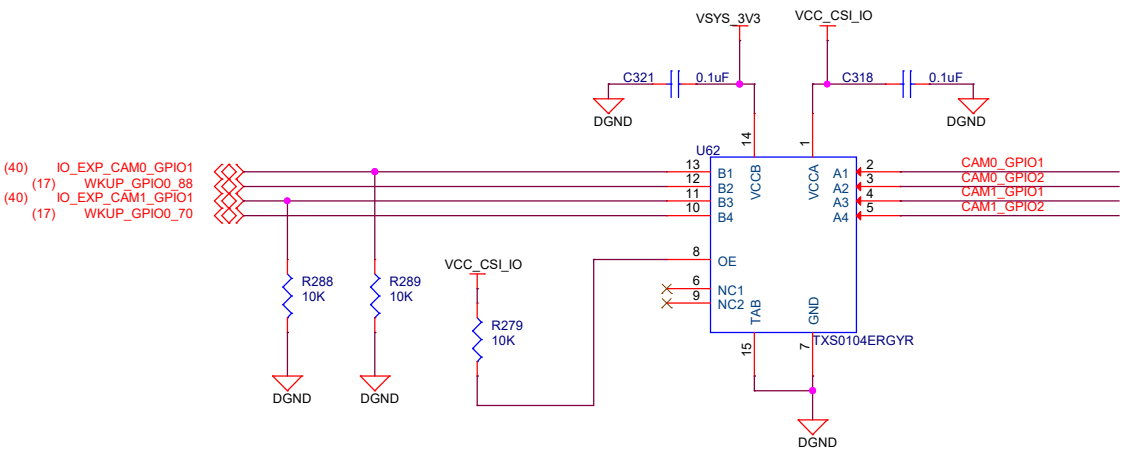


CSI FPC CAMERA CONNECTORS

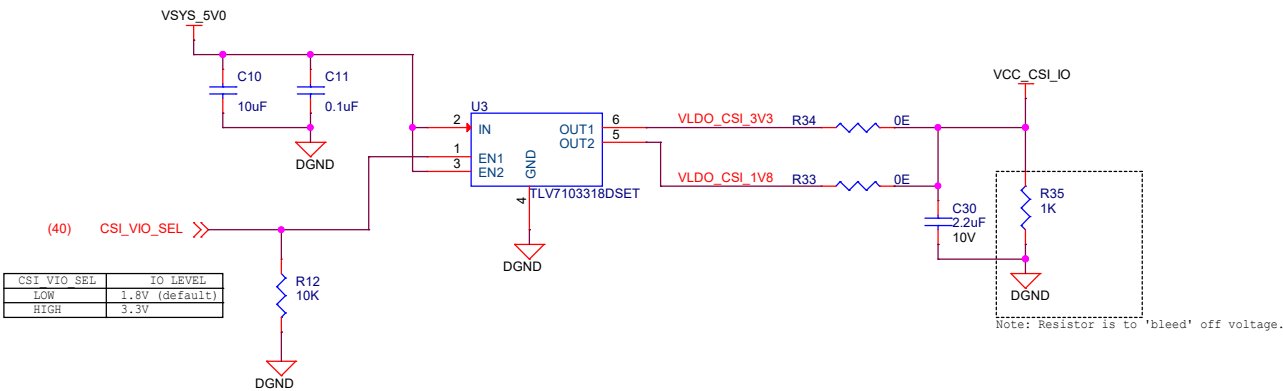
I2C SWITCH



GPIO LEVEL TRANSLATOR



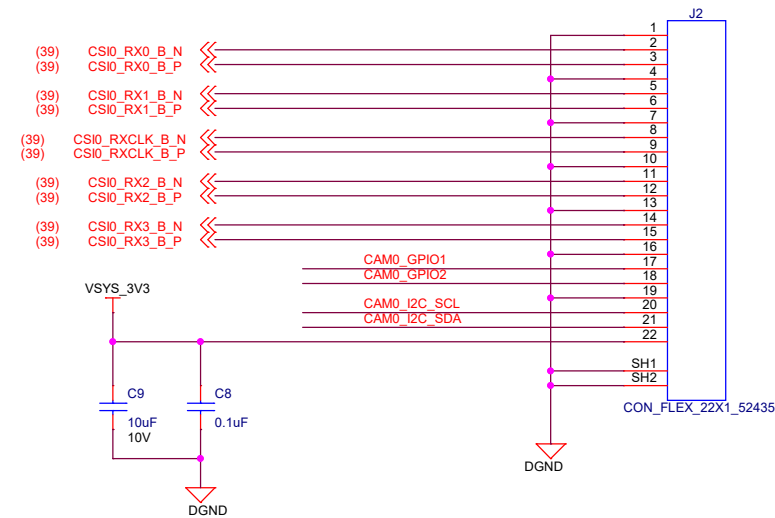
CAMERA IO SUPPLY



Silk Screen "CAM1"

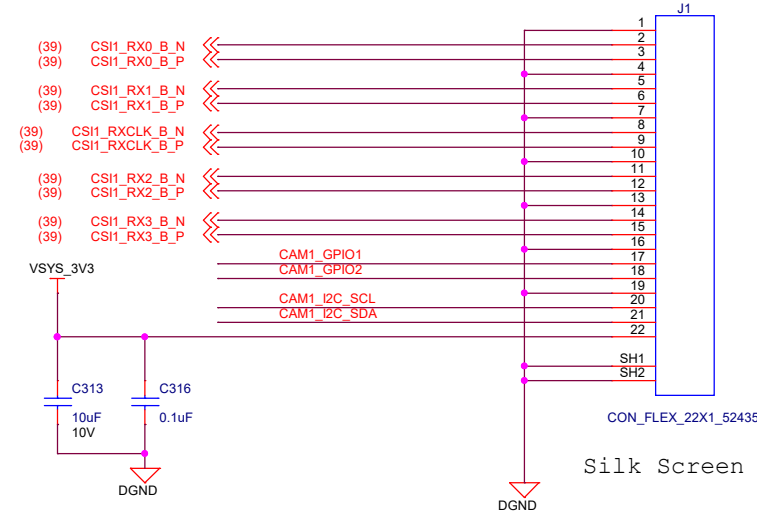
FPC Camera Connector -1

Pin out kept same as AM62A SK rev E1 !
Do we need to implement ECN as per AM62A SK

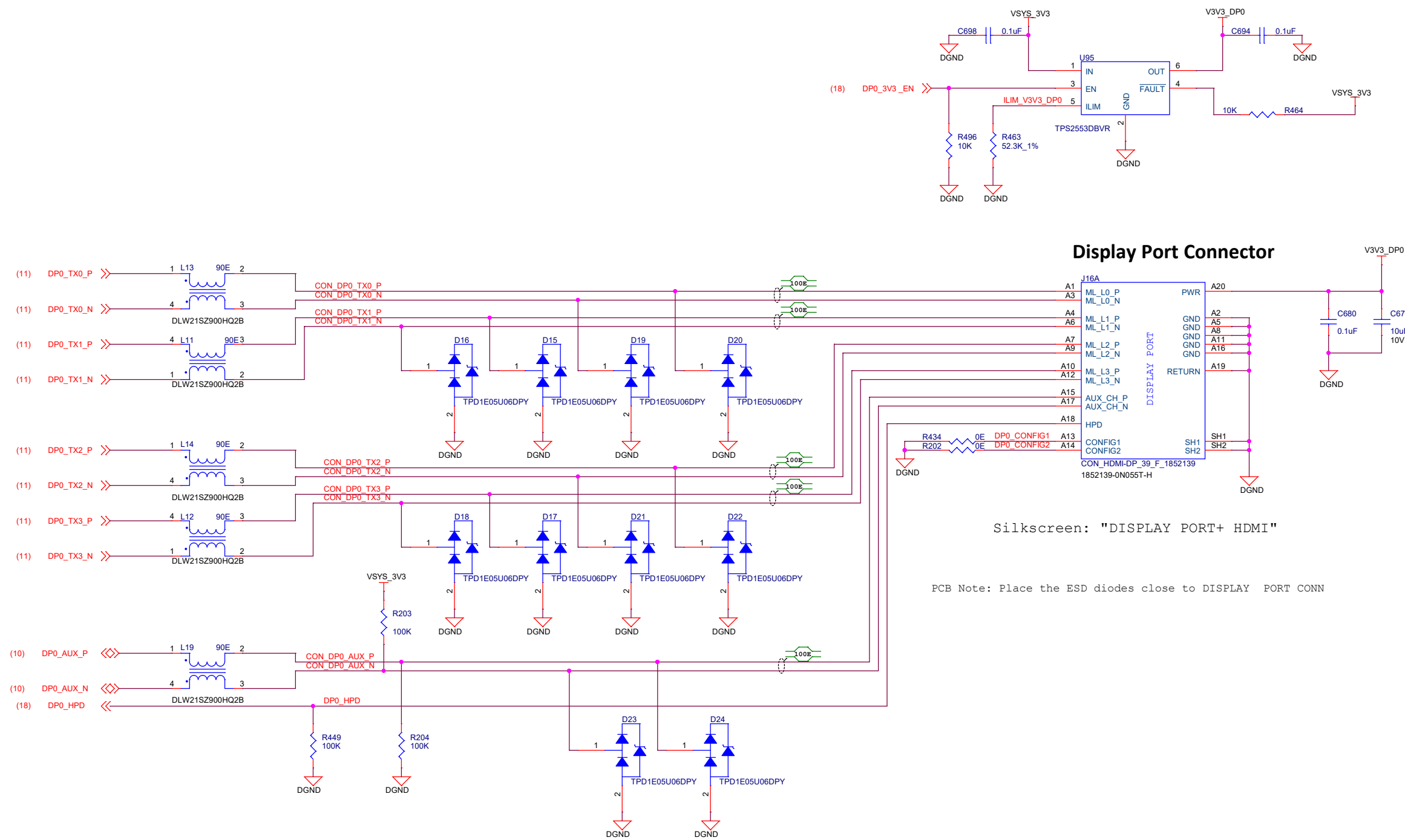


FPC Camera Connector -2

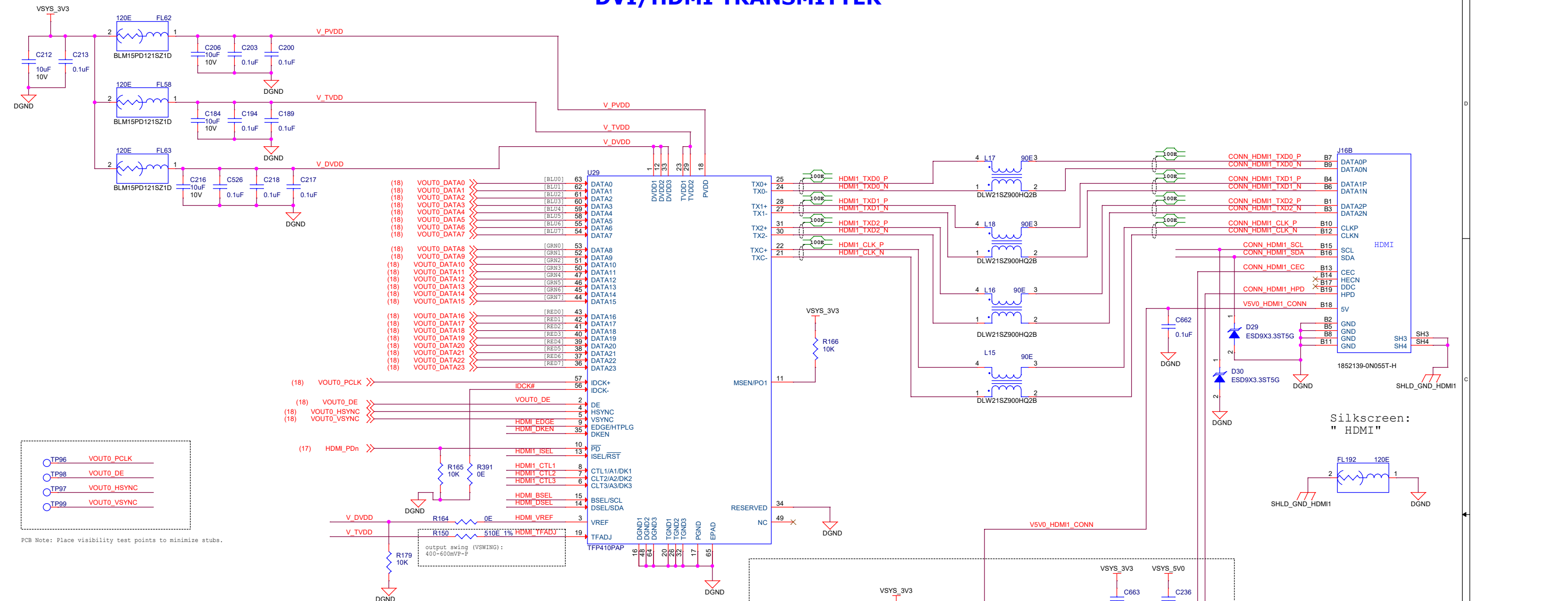
Pin out kept same as AM62A SK rev E1 !
Do we need to implement ECN as per AM62A SK



DISPLAY PORT INTERFACE



DVI/HDMI TRANSMITTER



DVI Configuration Settings

VSYS_3V3

R140 10K R183 10K R168 10K

HDMI_BSEL
HDMI_EDGE
HDMI_DKEN
HDMI_DSEL

R139 10K R182 10K R167 10K

DGND

VSYS_3V3

R163 10K

HDMI_CTL3
HDMI_CTL1
HDMI_CTL2

R181 10K R180 10K

DGND

VSYS_3V3

R174 10K

HDMI_ISEL

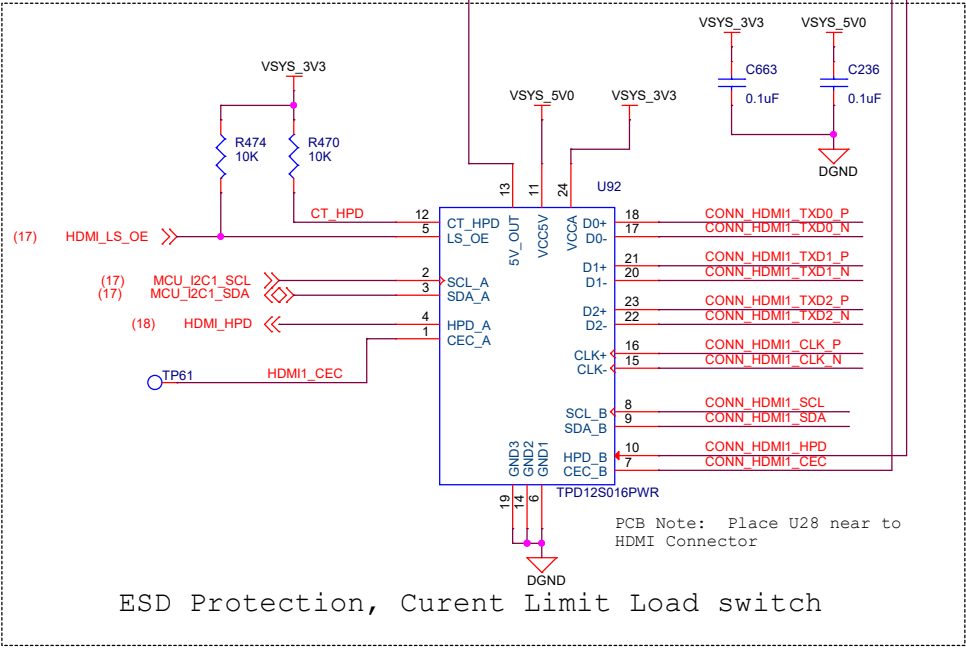
R185 10K C223 1uF

DGND

VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V-0.9V	1	0	0	24-bit	Single-ended	Falling	Single-ended
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended

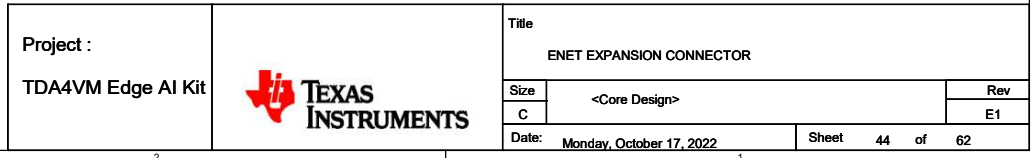
ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins

When ISEL: L, DSEL-H- enables de-skew function (default)

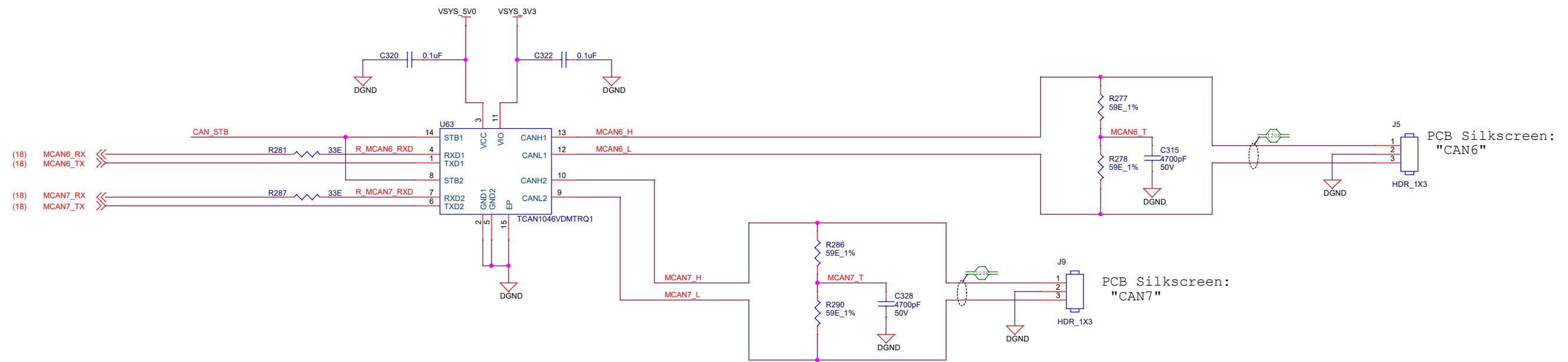
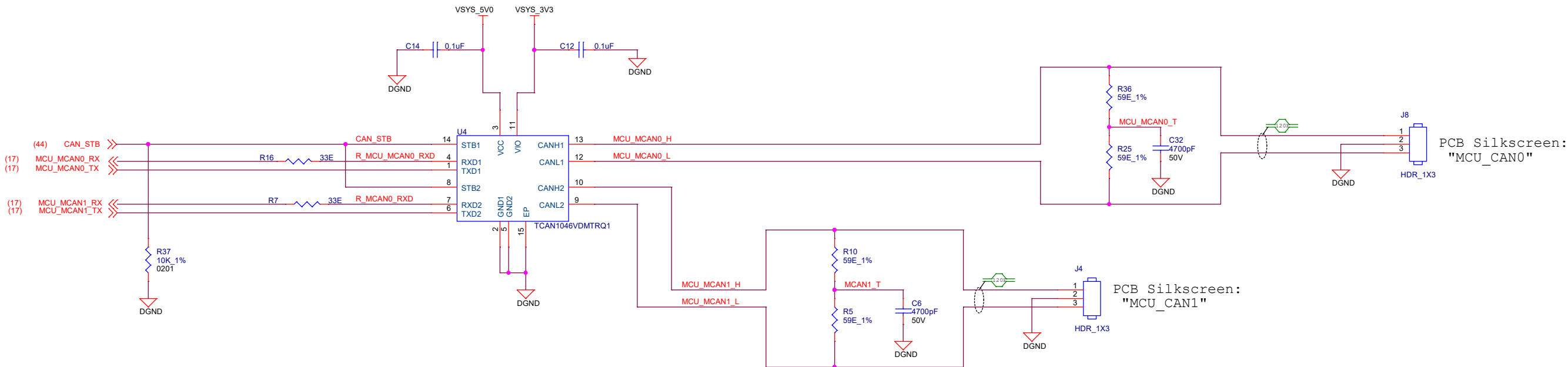


Silkscreen:
" HDMI"

```
Silkscreen  "ENET-EXP"
```

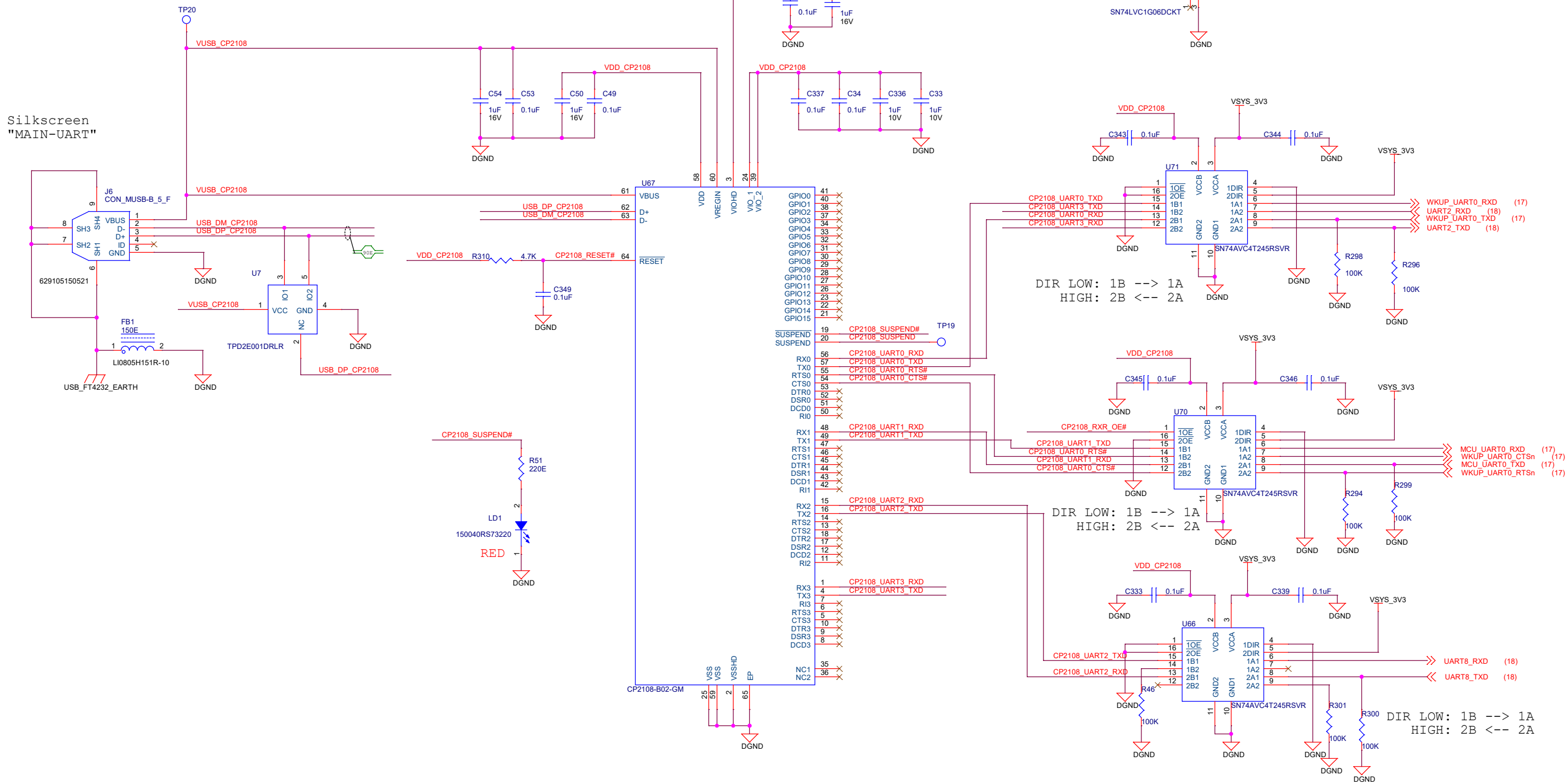


CAN TRANSCEIVERS



QUAD PORT CONSOLE

Silkscreen
"MAIN-UART"



Project :
TDA4VM Edge AI Kit

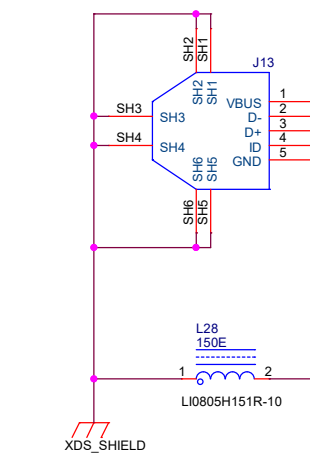


Title QUAD PORT UART	
Size C	<Core Design>
Date: Monday, October 17, 2022	Sheet 46 of 62
Rev E1	

XDS110 DEBUGGER

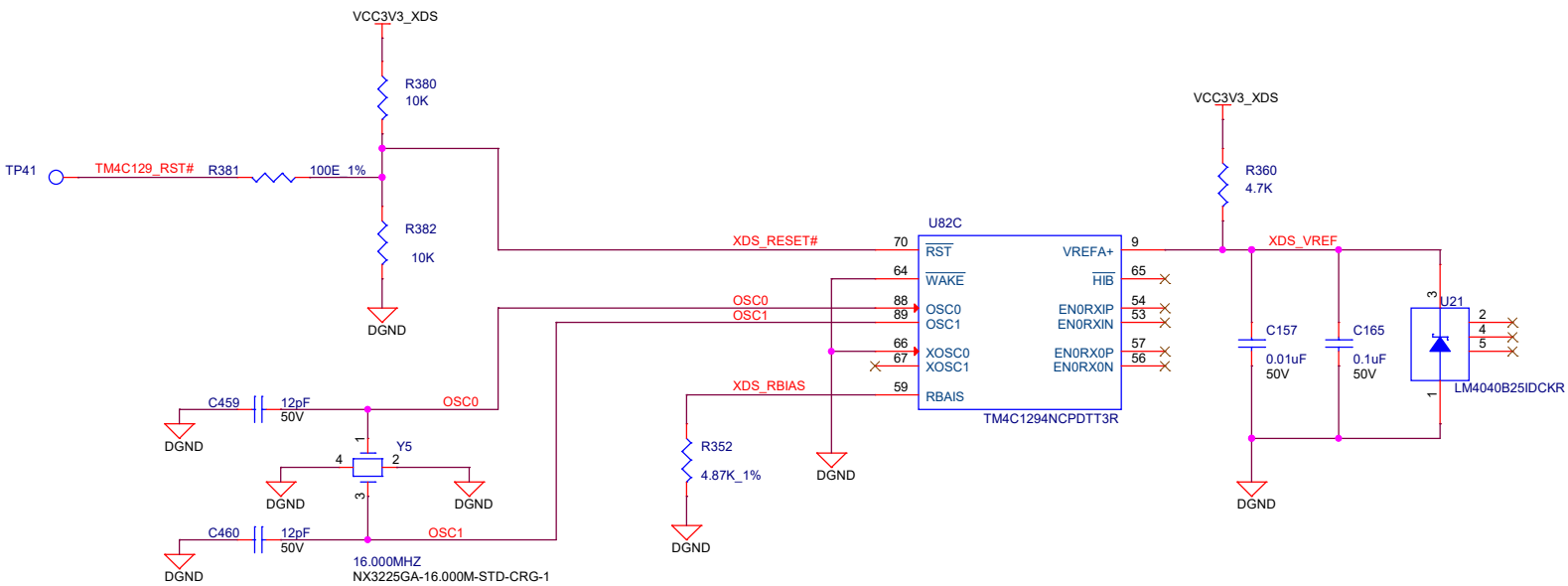
Silkscreen "XDS110"

1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD



(26,48)	TA_POWERDOWNz	<< 0E	R439	0201	XDS_TA_POWERDOWNz
(27,48)	TA_PORZ	<< 0E	R444	0201	XDS_TA_PORZn
(27,48)	TA_RESETz	<< 0E	R448	0201	XDS_TA_RESETz
(19,48)	TA_SOC_INT1z	<< 0E	R454	0201	XDS_TA_SOC_INT1z
(19,48)	TA_SOC_INT2z	<< 0E	R460	0201	XDS_TA_SOC_INT2z
(48)	TA_BOOTMODE_CNTRL#	<< 0E	R467	0201	XDS_TA_BOOTMODE_CNTRL#
(27,48)	TA_BM_IOEXP_RSTn	<< 0E	R473	0201	XDS_TA_BM_IOEXP_RSTn

Resistors to isolate Test Automation from XDS110



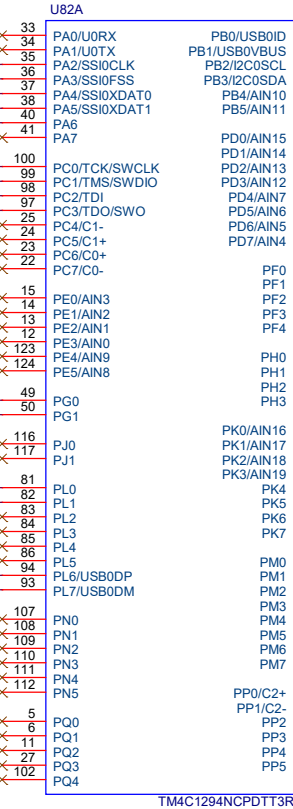
(20)	XDS110_TCK	<< 33	PA0/UORX
(20)	XDS110_TMS	<< 34	PA1/UOTX
(20)	XDS110_TDO	<< 36	PA2/SSI0CLK
(20)	XDS110_TDI	<< 37	PA3/SSI0FSS
(20)	XDS110_TRST#	<< 38	PA4/SSI0XDAT0

TP34	TM4C129_TCK	<< 100	PC0/TCK/SWCLK
TP35	TM4C129_TMS	<< 99	PC1/TMS/SWDIO
TP36	TM4C129_TDI	<< 98	PC2/TDI
TP38	TM4C129_TDO	<< 97	PC3/TDO/SWO

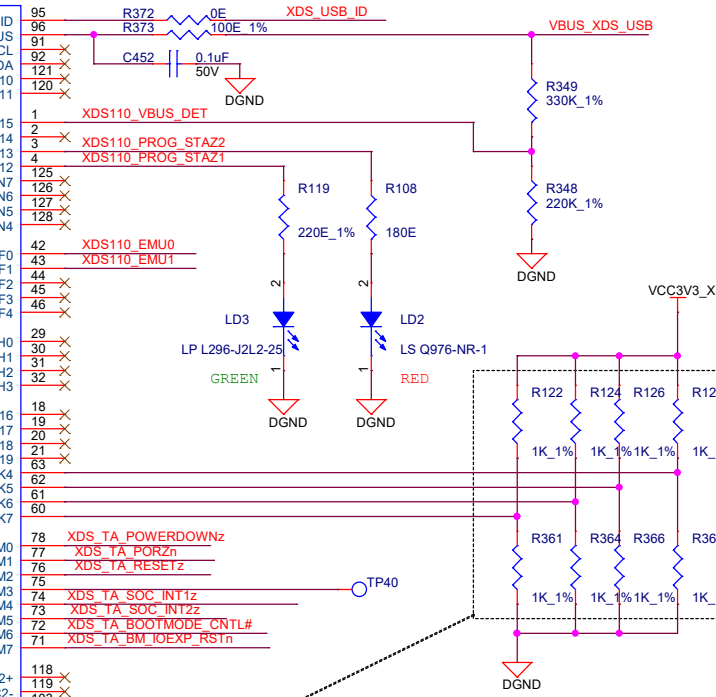
XDS_PM2_SCL	<< 49	PG0
XDS_PM2_SDA	<< 50	PG1

XDS_PM1_SDA	<< 81	PL0
XDS_PM1_SCL	<< 82	PL1

XDS_USB_D_P	<< 94	PL5
XDS_USB_D_N	<< 93	PL6/USB0DP



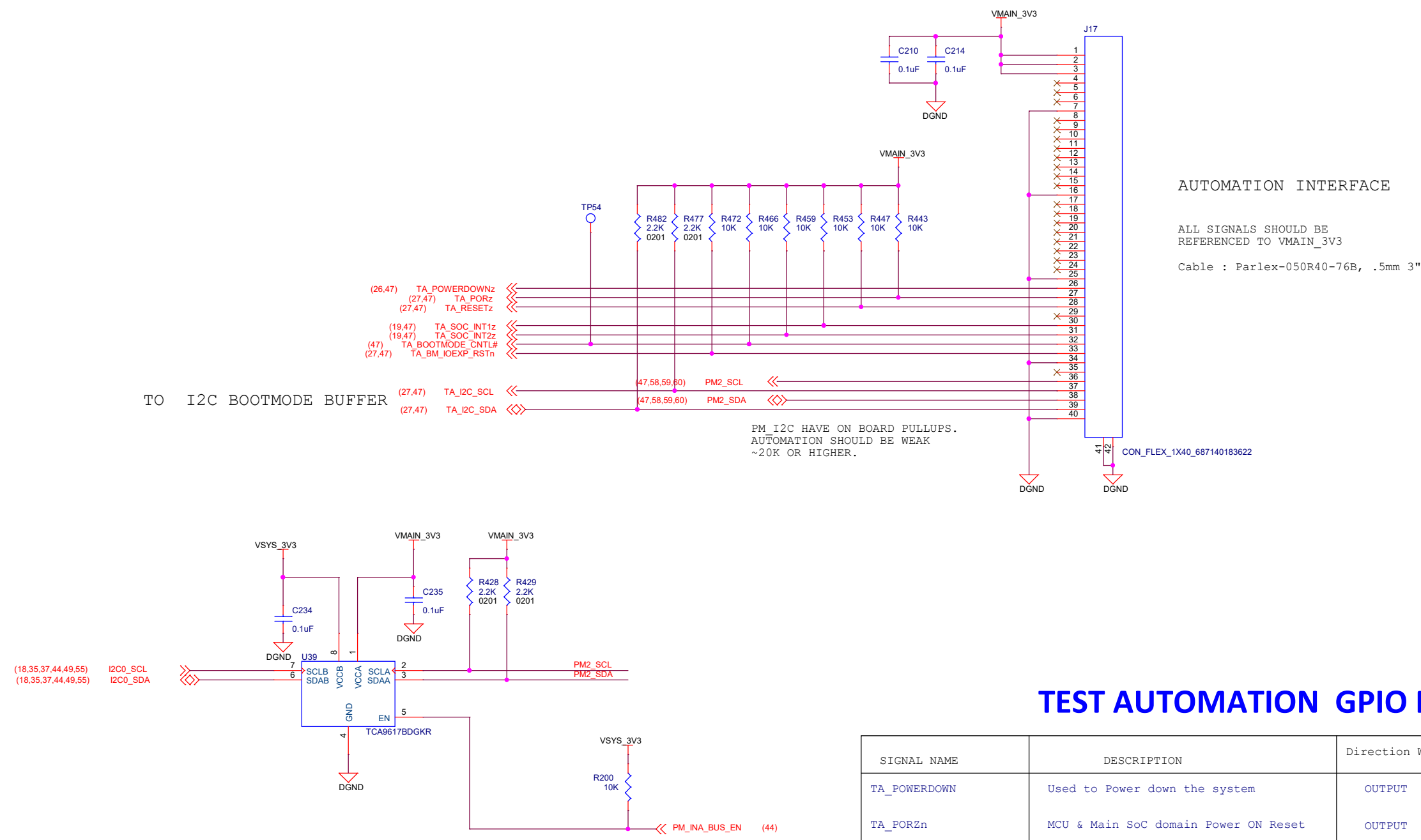
(48,58,59,60)	PM2_SCL	<< 0E	R478	0201	XDS_PM2_SCL
(48,58,59,60)	PM2_SDA	<< 0E	R484	0201	XDS_PM2_SDA
(27,48)	TA_I2C_SCL	<< 0E	R481	0201	XDS_PM1_SCL
(27,48)	TA_I2C_SDA	<< 0E	R490	0201	XDS_PM1_SDA



Set the unique ID
of the debugger

Project : TDA4VM Edge AI Kit		Title XDS110 DEBUGGER
		Size <Core Design>
		Rev E1
Date: Monday, October 17, 2022	Sheet 47 of 62	

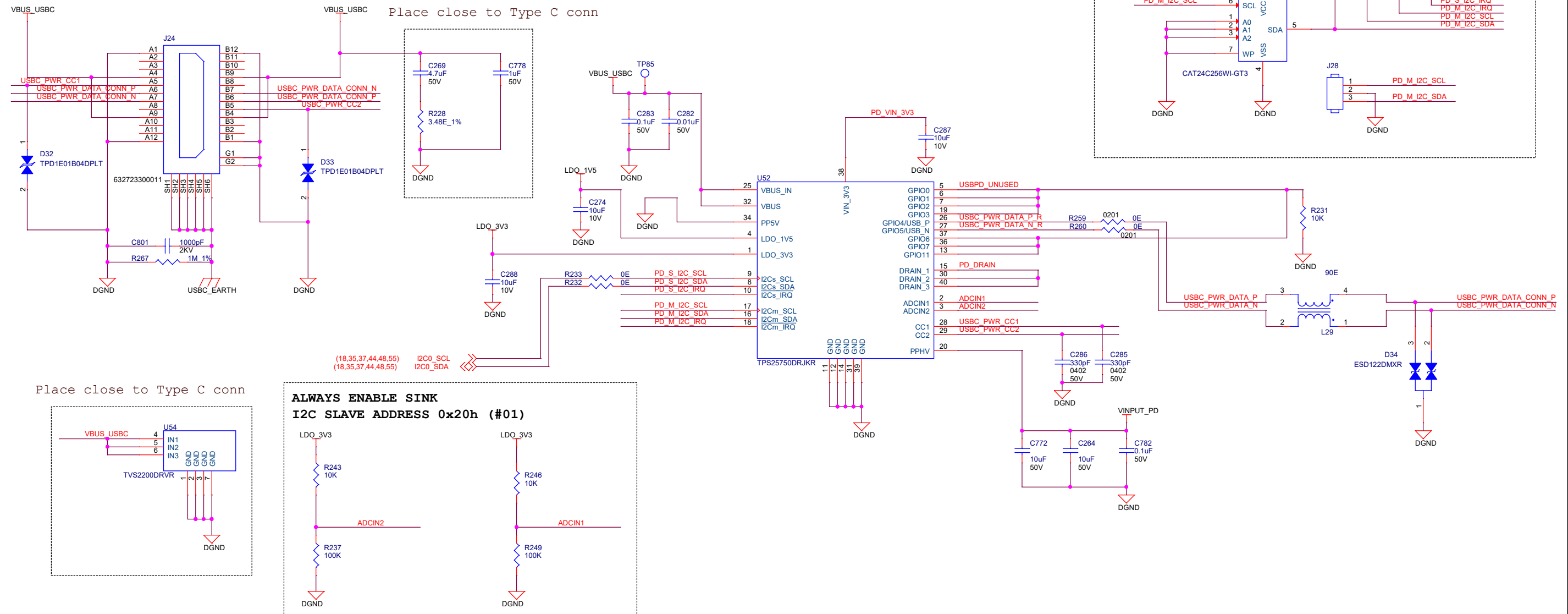
TEST AUTOMATION HEADER



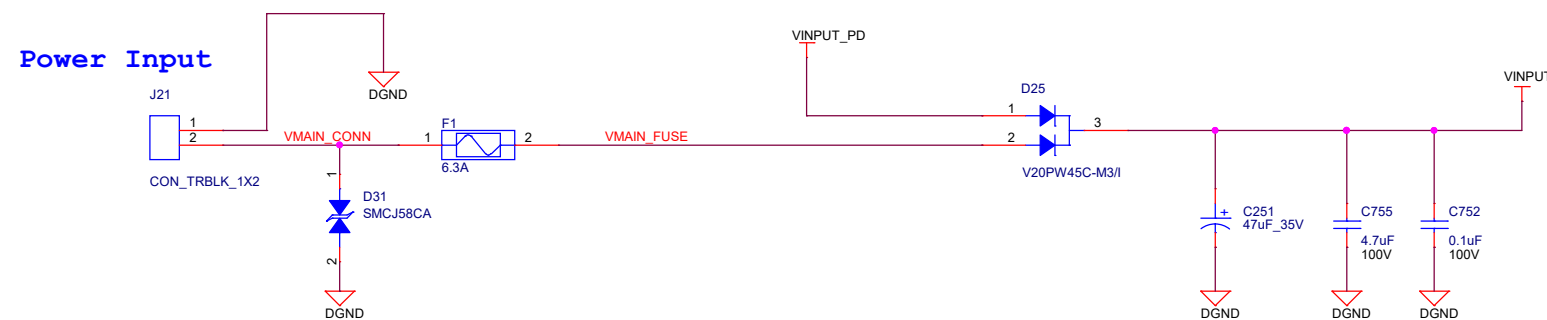
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

USB-C Power



OPTIONAL POWER INPUT



Normal operation Range for VININPUT 20V to 25V.

SILK: POWER IN

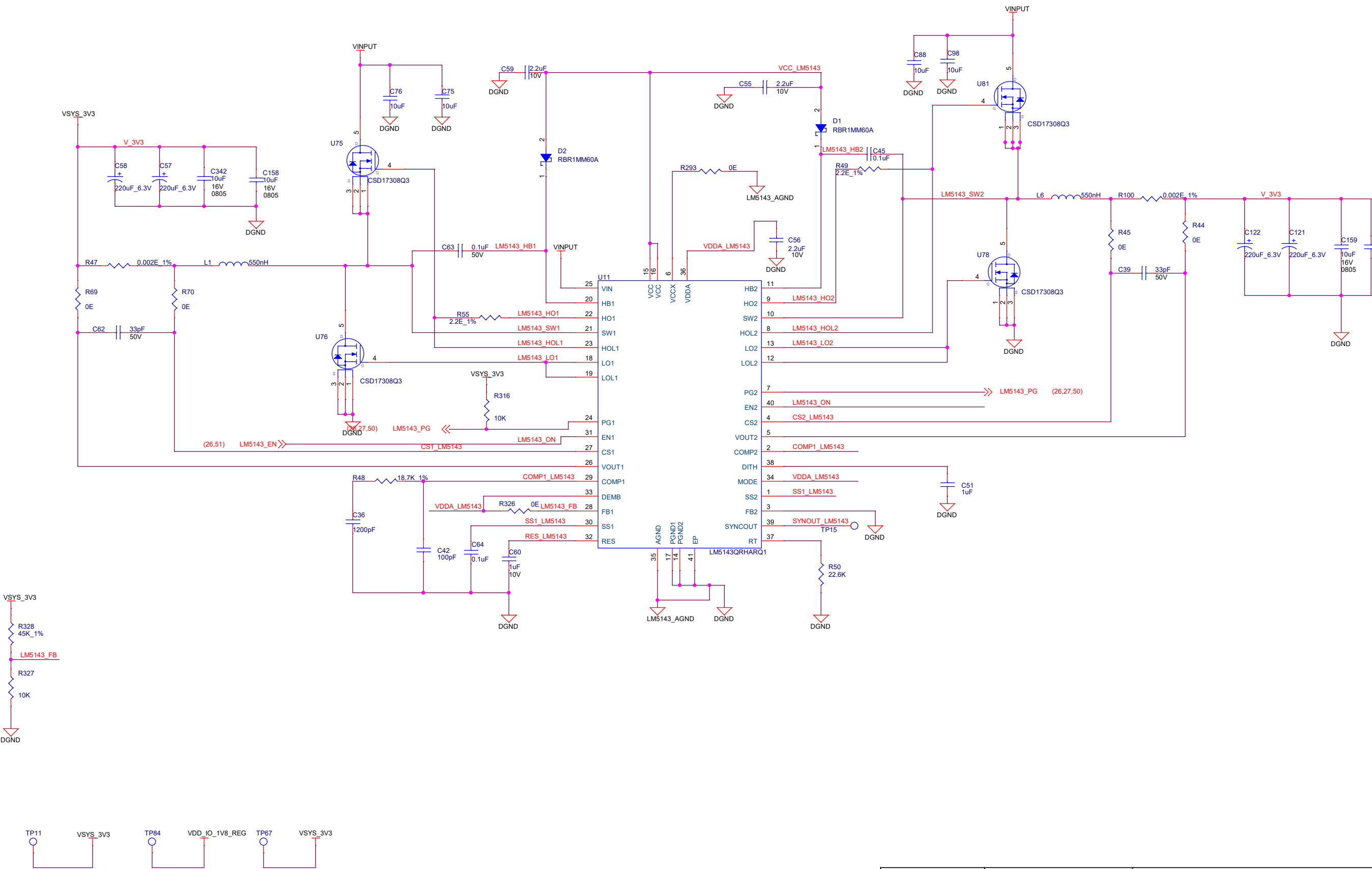
Project :
TDA4VM Edge AI Kit



Title		POWER INPUT	
Size	<Core Design>		Rev
C			E1
Date:	Monday, October 17, 2022	Sheet	49 of 62

POWER SUPPLY #1

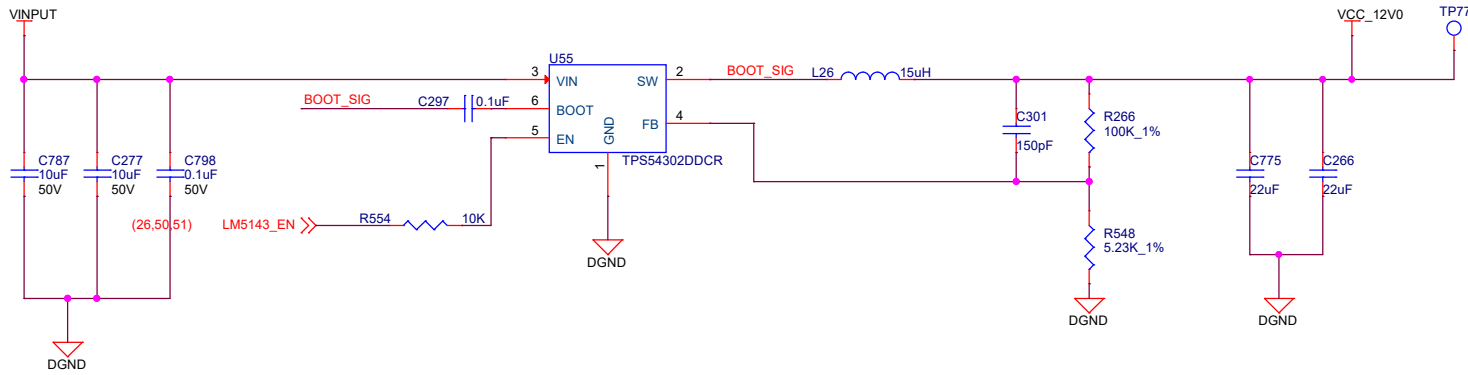
TI WEBENCH Simulation Inputs:
Vin (min) = 24V Vin (max) = 48V
Vout = 3.3V@30A
Ta = 25 deg



POWER SUPPLY #2

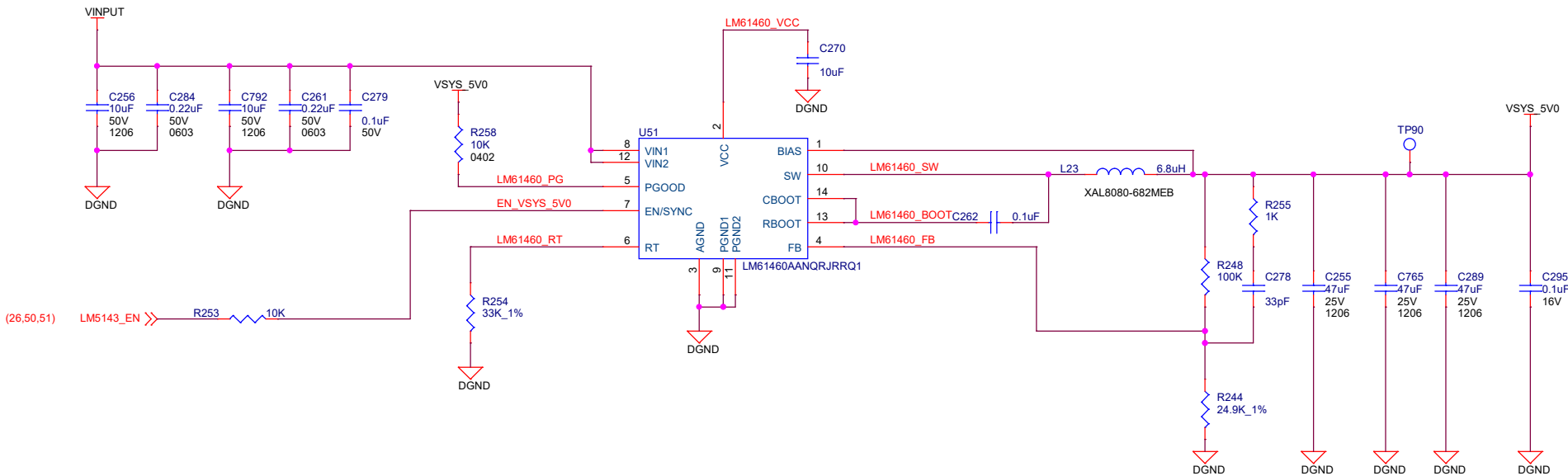
TI WEBENCH Simulation Inputs:
Vin (min) = 15V Vin (max) = 25V
Vout = 12V@3A
Ta = 25 deg

12V GENERATION



LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 25V
Vout = 5.0V
Iout = 6A

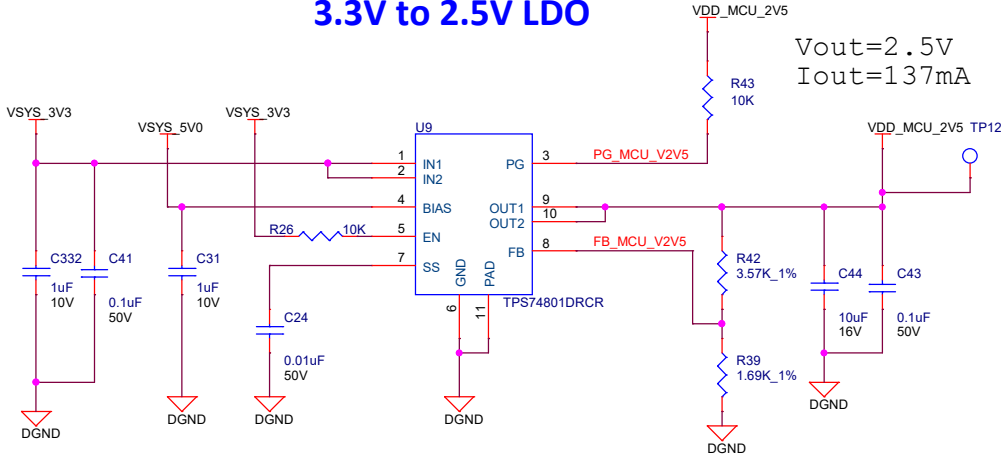
5V GENERATION



POWER SUPPLY #3

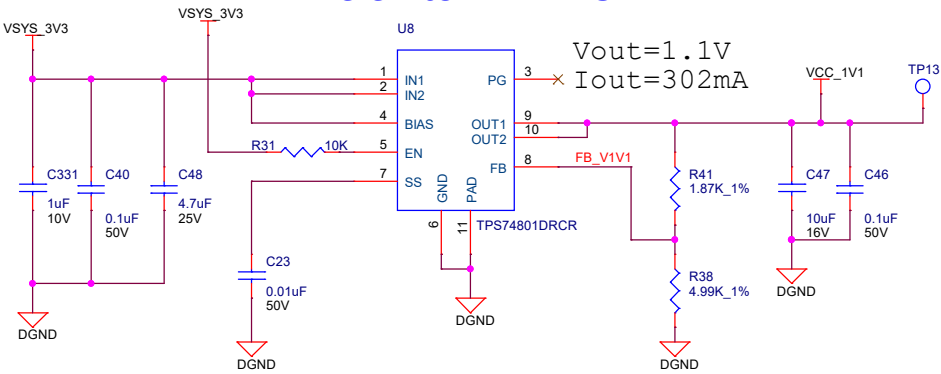
ETHERNET POWER- MCU RGMII

3.3V to 2.5V LDO



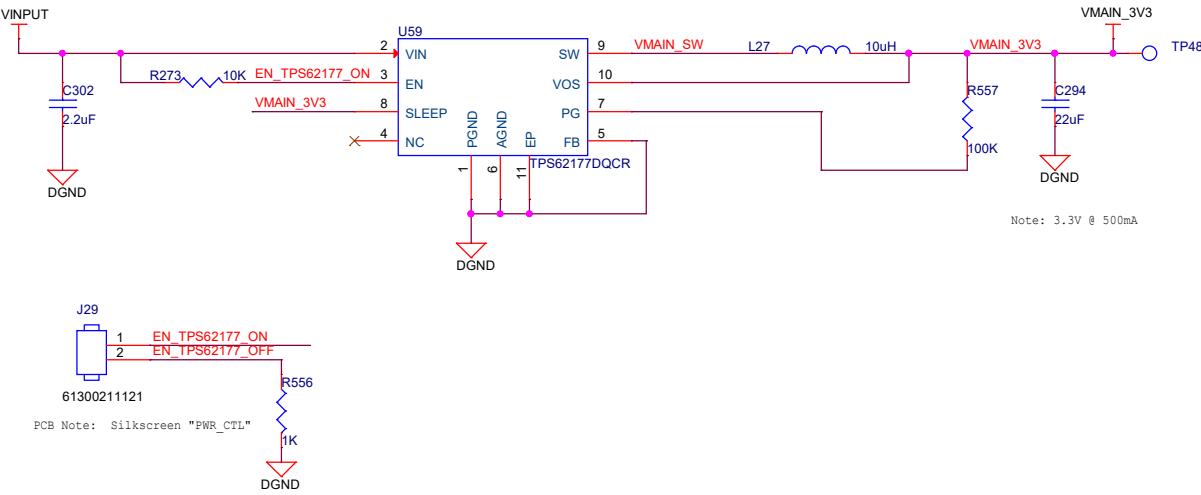
USB HUB POWER & ETHERNET POWER - RGMII1

3.3V to 1.1V LDO

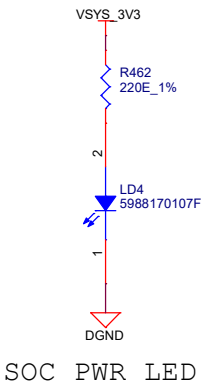


PCB NOTE:Keep 4.7uF capacitor close to BIAS pin

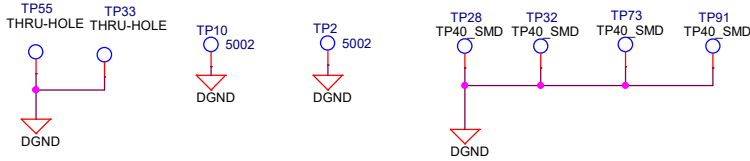
SYSTEM MANAGEMENT 3.3V REGULATOR



POWER INDICATION LED's

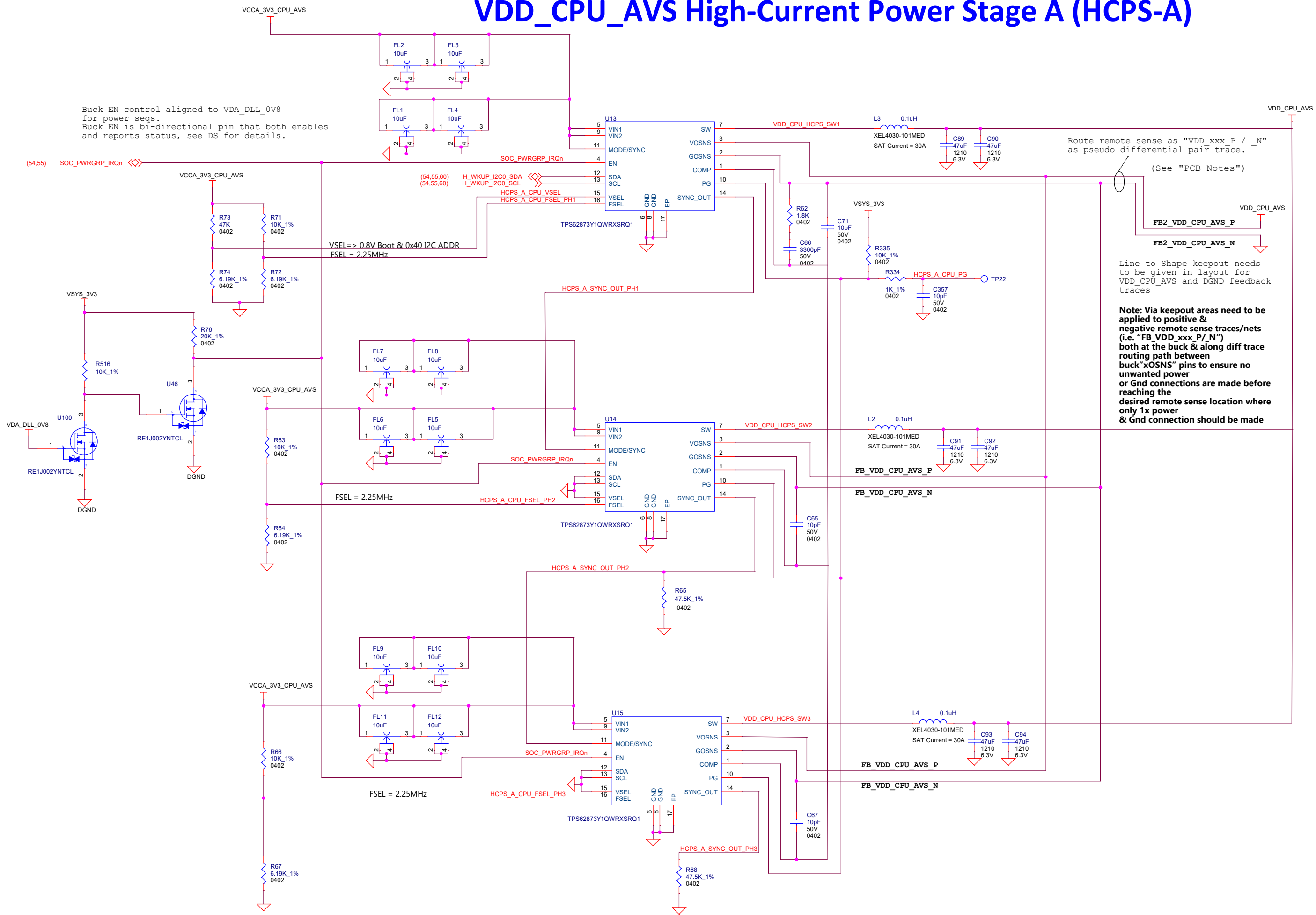


GROUND TEST POINTS



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

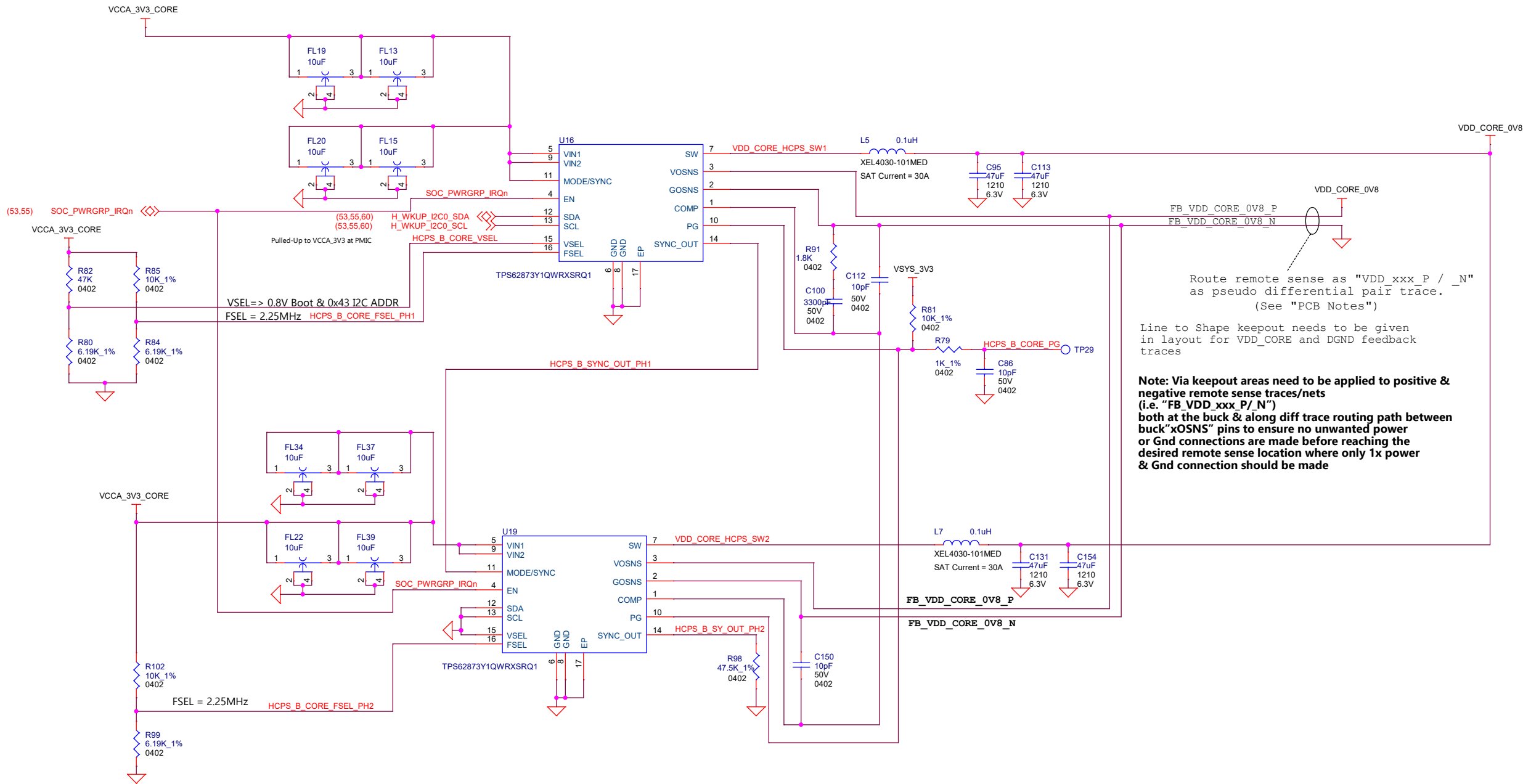


Buck EN control aligned to VDA_DLL_0V8 for power segs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.

Route remote sense as "VDD xxx_P / _N" as pseudo differential pair trace.
(See "PCB Notes")

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "FB_VDD_XXX_P/_N") both at the buck & along diff trace routing path between buck "xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)



Route remote sense as "VDD xxx_P / _N" as pseudo differential pair trace. (See "PCB Notes")

Line to Shape keepout needs to be given in layout for VDD_CORE and DGND feedback traces

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "FB_VDD xxx_P / _N") both at the buck & along diff trace routing path between buck"xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

PMIC

"PCB Notes":

For multi-phase Buck converter configs, route remote sense feedback as follows:

1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs, route remote sense feedback as follows:

1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.

Route as Pseudo diff pair traces
(See "PCB Notes")

Note: Keepout needs to be provided for the VDD_DDR_1V1 and Gnd vias of the feedback pins connecting to the PMIC.

Line to Shape keepout needs to be given in layout for VDD_DDR_1V1 and DGND feedback traces

PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

Project :

TDA4VM Edge AI Kit



Title
PMIC

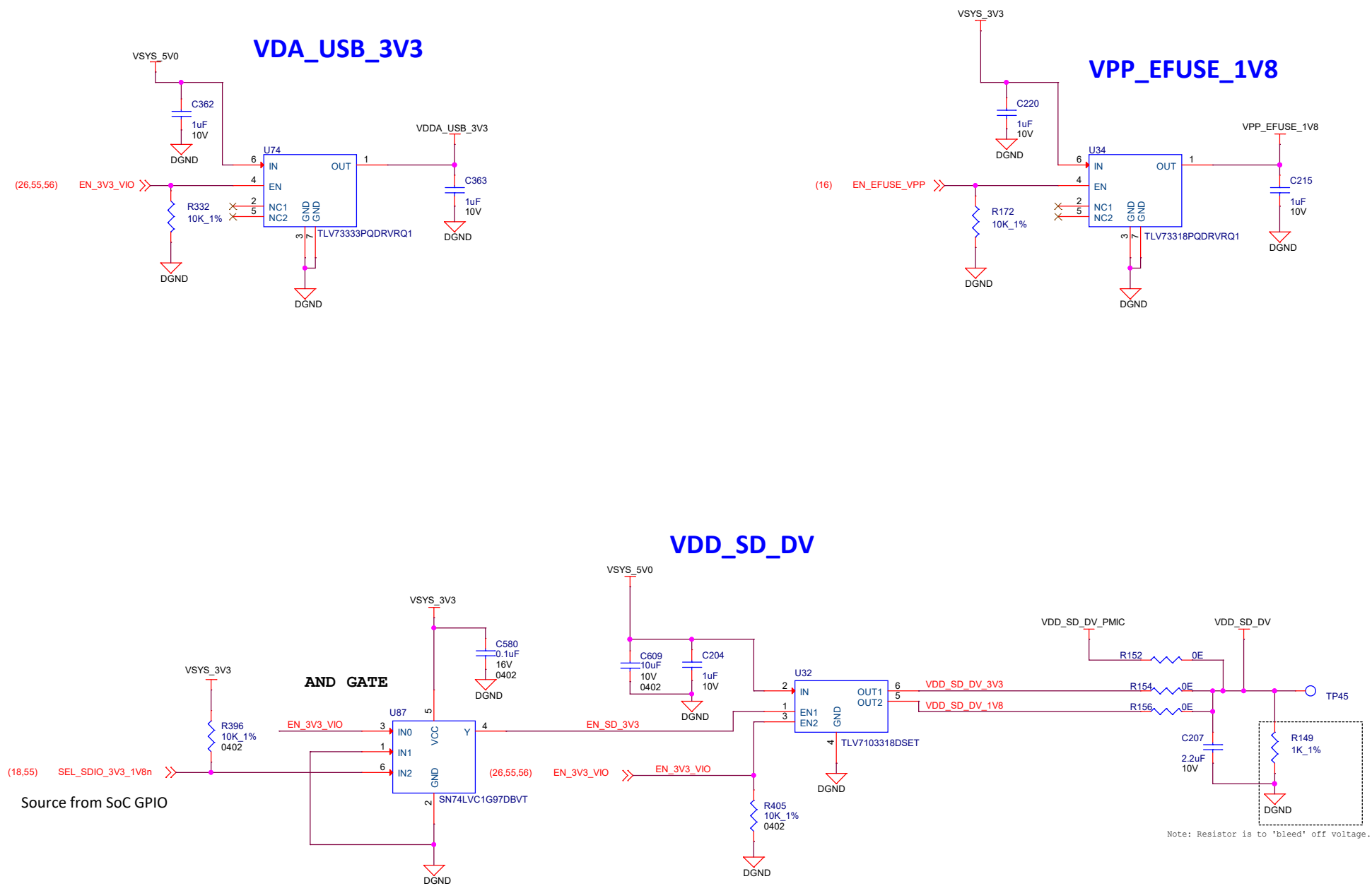
Size
C <Core Design>

Date: Monday, October 17, 2022

Sheet 55 of 62

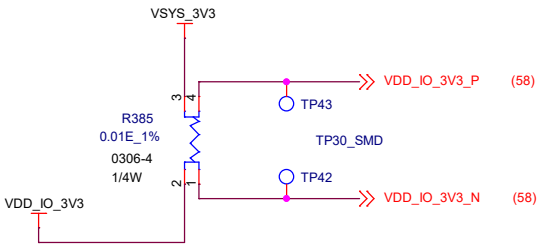
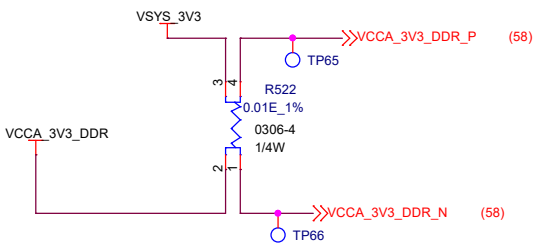
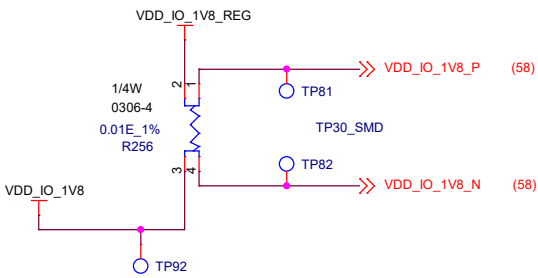
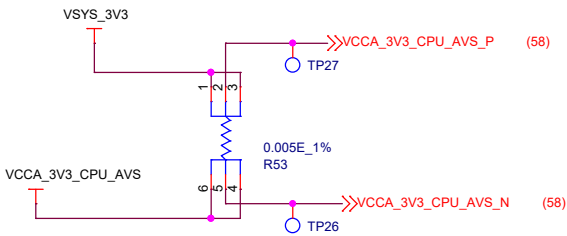
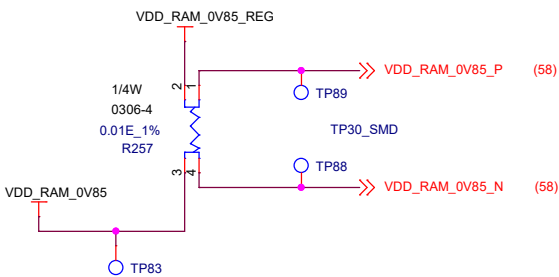
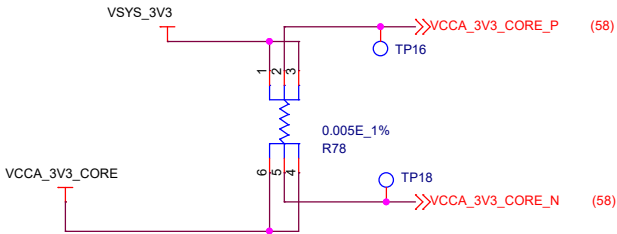
Rev
E1

LDOs

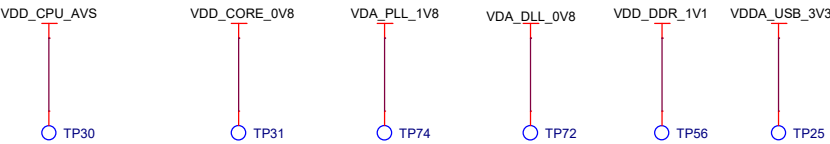


SOC Current Sense Resistors

CORE, AVS and DDR input supply sense resistors

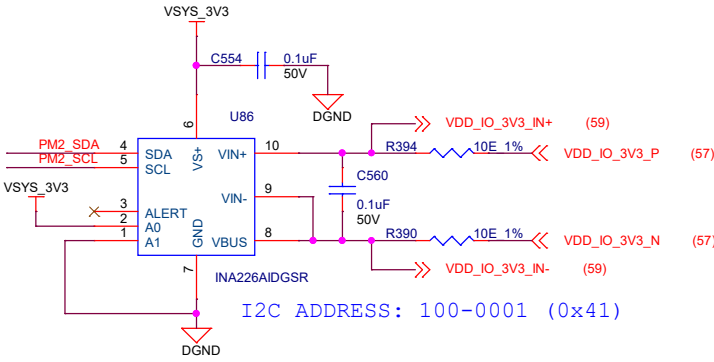
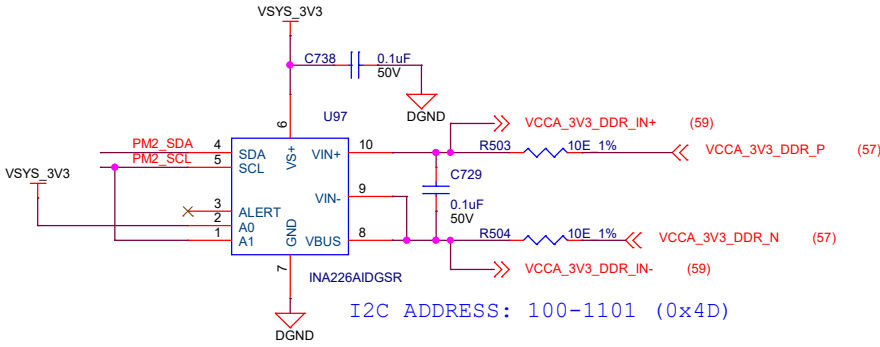
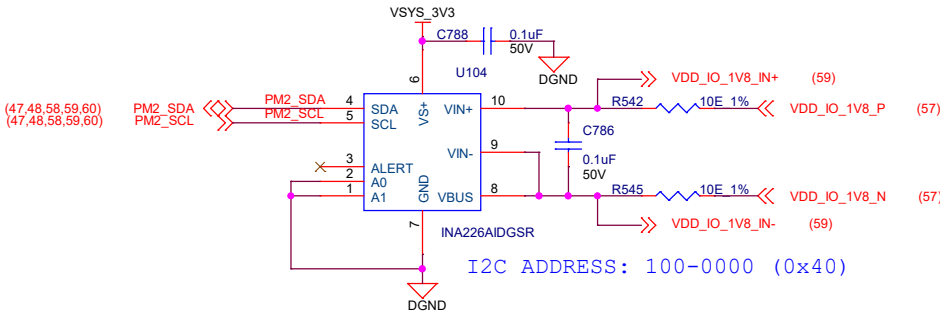
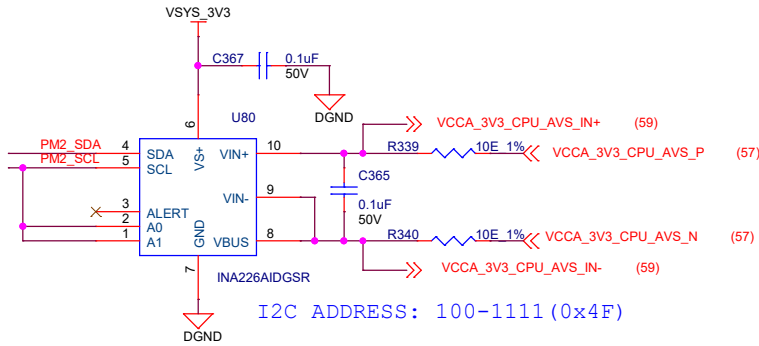
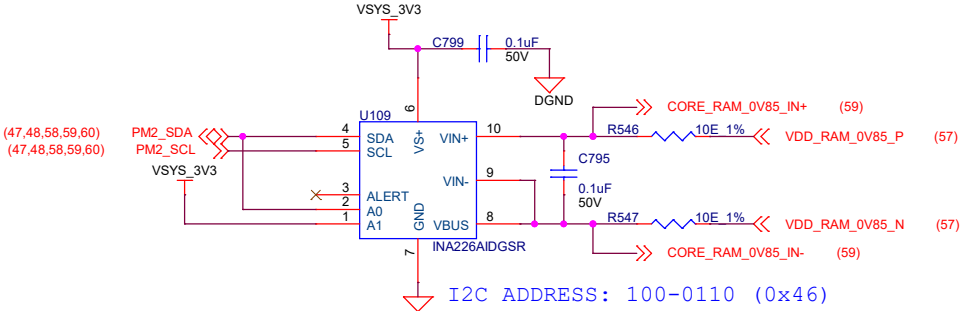
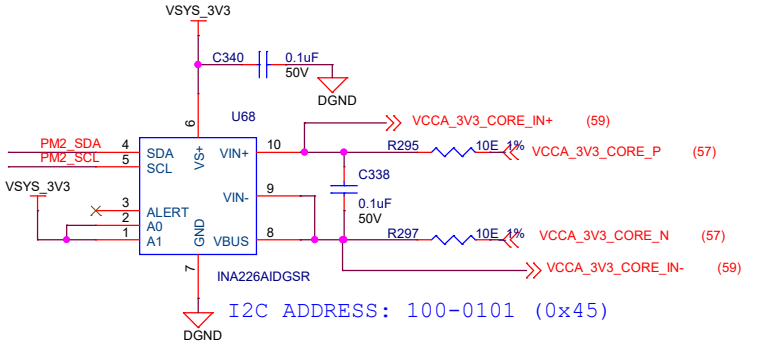


PCB Note: Place all SMT TPs on PCB top-side & on top of via at Bd-to-Bd connector



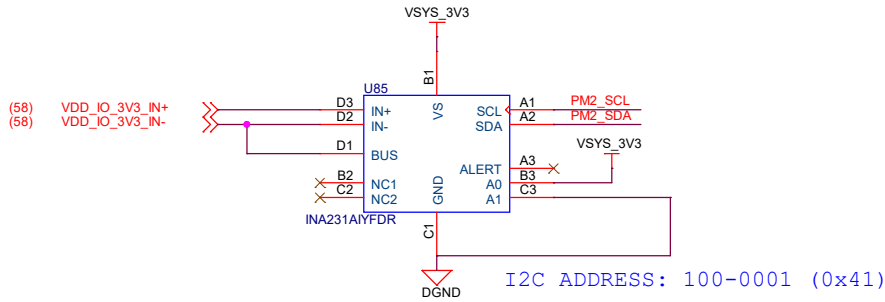
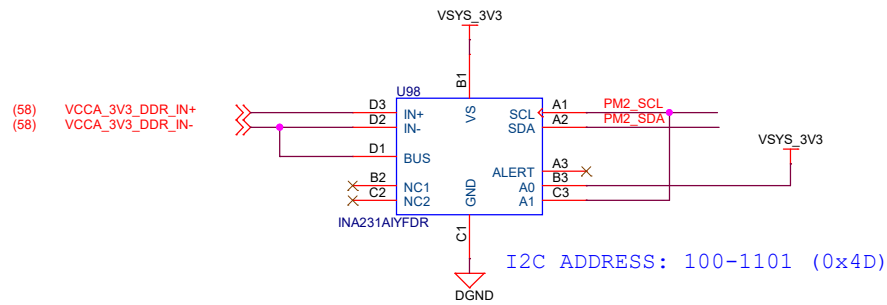
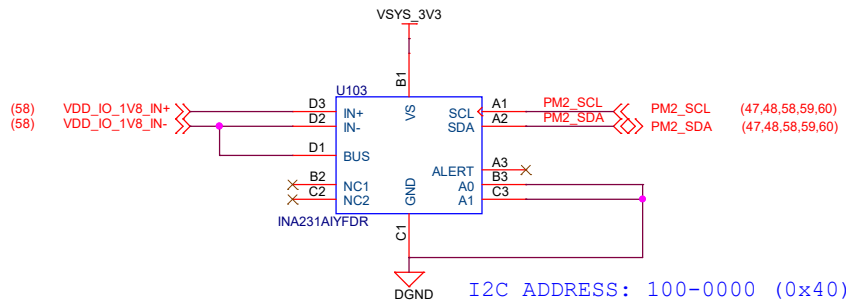
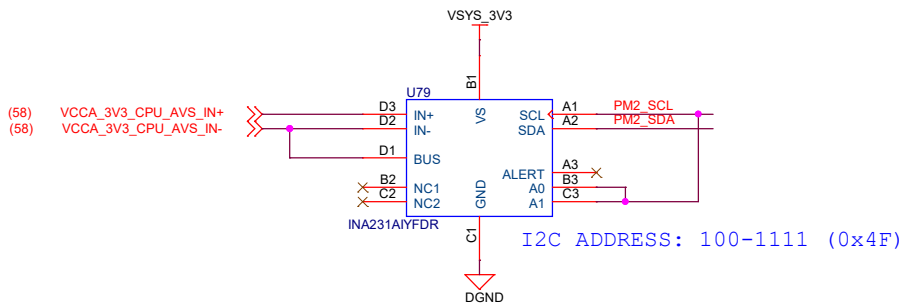
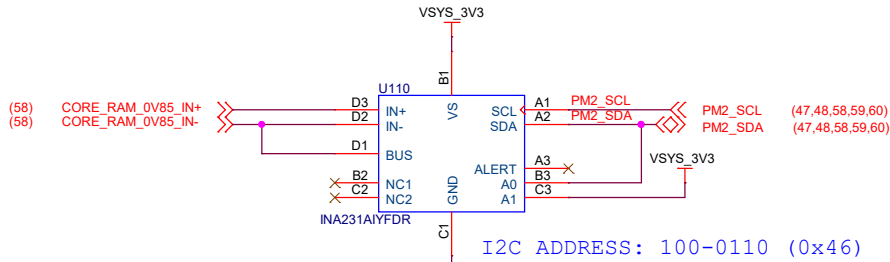
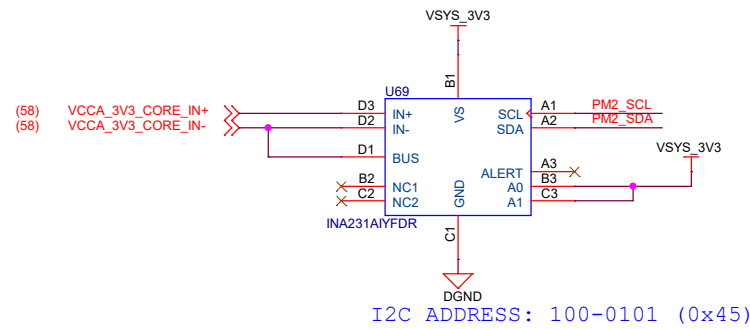
Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA226

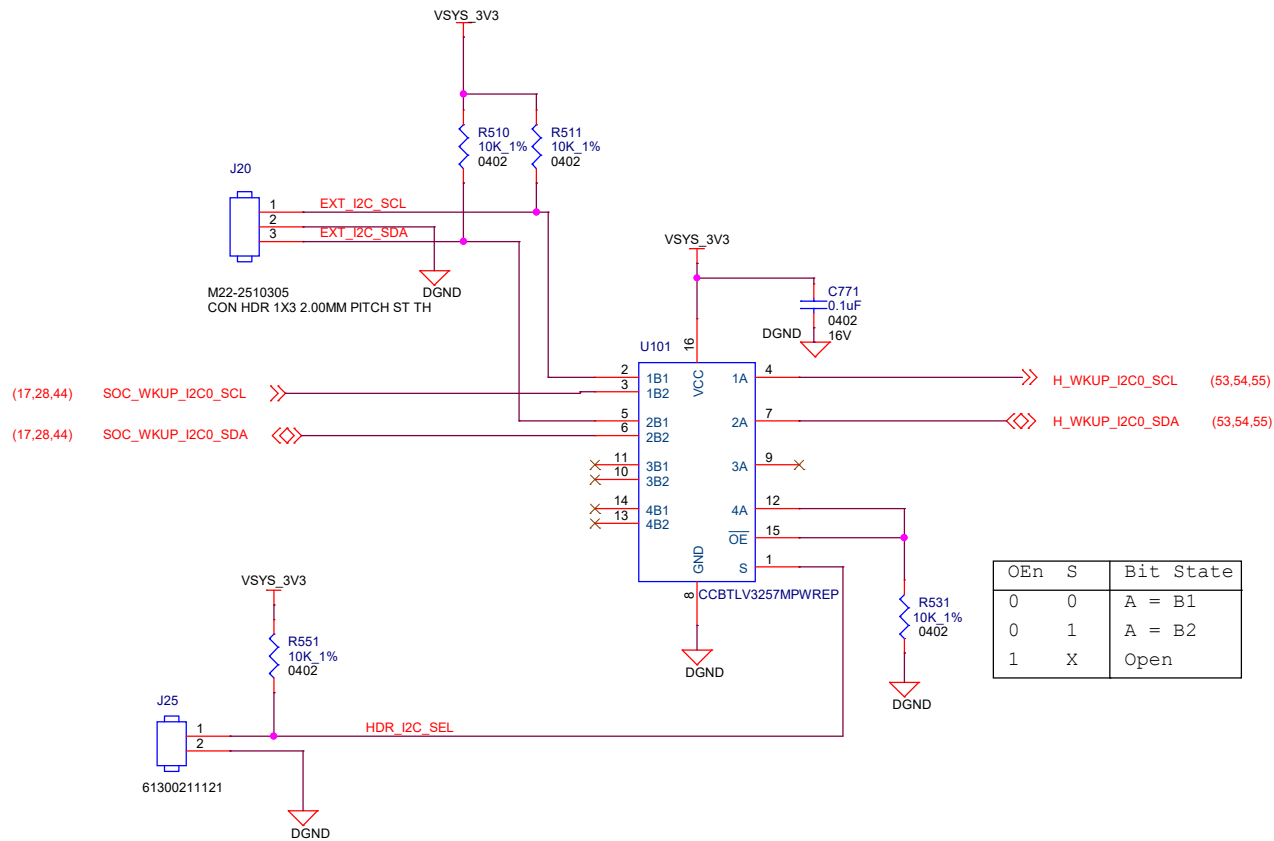


Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

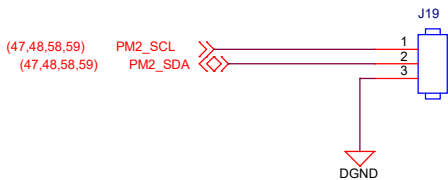
CURRENT MONITORS - INA231




PMIC Support Circuit



EXT POWER MEASUREMENT



RESERVED

Project : TDA4VM Edge AI Kit		Title			
		RESERVED			
		Size	<Core Design>		Rev
		C			E1
		Date:	Monday, October 17, 2022	Sheet	61

NOTES, HW & LABELS

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABELS

Board Serial No.



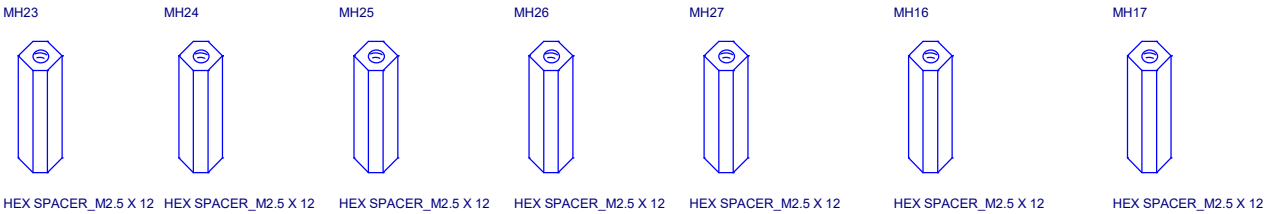
Assembly Revision.



SCREWS



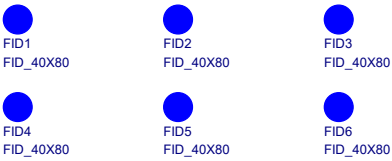
STANDOFFs



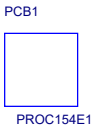
WASHER



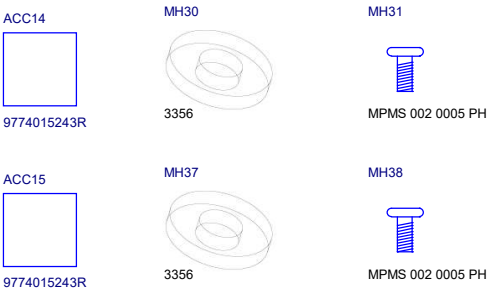
FIDUCIALS



BARE PCB

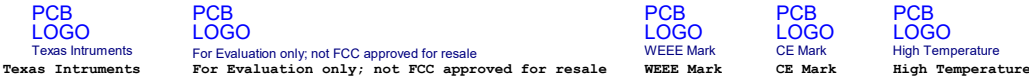


SCREW & WASHER FOR PCIe M.2



ENET EXP ACCESSORY

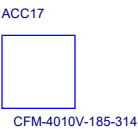
LOGOs



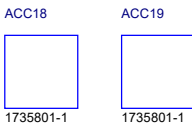
HEAT SINK



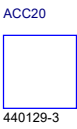
FAN



CRIMP PIN



CONN HOUSING



SCREW FOR FAN ASSEMBLY

