

AM62P STARTER KIT EVM

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BOARD REVISION	E1-1
SCHEMATIC VERSION	2.1

D-Note:-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note:-

- * Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build.(Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprada9/sprada9.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/sprad66a/sprad66a.pdf
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

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REVISION HISTORY

E1	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
	0.01	20 FEB 2023	Initial Draft derived from AM62A SK - PROC135E3 schematics	Mistral Design Team		
	0.02	23 FEB 2023	Updated power section & PMIC part as per PDN	Mistral Design Team		
	0.03	24 FEB 2023	1. Added pullups on XDS110 side for Test Automation signals 2. Added 5V0 sourcing caps to meet USB Specifications	Mistral Design Team	Nishant	
	0.04	27 FEB 2023	Replaced parts : LPDDR4 (8 GB), eMMC (32 GB with HS400 support), OSPI (512 Mb NOR Flash)	Mistral Design Team		
	0.06	01 MAR 2023	Replaced parts : LPDDR4 (8 GB), eMMC (32 GB with HS400 support), OSPI (512 Mb NOR Flash) Added DSI, OLDI, GPMC (x8) connectors & updated respective net connections	Mistral Design Team	Nishant	
	0.07	03 MAR 2023	Updated PMIC local caps, GPIO connections & assembly variants	Mistral Design Team		
	0.08	08 MAR 2023	1. Updated INA section to include INA228 as default with footprint support for INA231 2. INA Kelvin sense resisitors moved to PMIC sheet as per modular design requirement	Mistral Design Team	Nishant	
	0.09	15 MAR 2023	1. Updated TI review comments 2. Updated PMIC connections as per PDN v1.5	Mistral Design Team	Nishant	
	0.10	16 MAR 2023	Added separate dual LDO for VDDSHV_SDIO, 5V0 headers for OLDI & DSI daughter cards	Mistral Design Team		
	0.11	20 MAR 2023	1. Updated PMIC Enable & GPIO connections 2. Modified RC shield connections for RGMII1, RGMII2 & USB Type A connectors	Mistral Design Team		
	0.12	22 MAR 2023	1. Updated TI review comments on PD Controller 2. Replaced HDMI EXT_SWING resistor with 7.5K_5% ohms	Mistral Design Team	Nishant	
	0.13	28 MAR 2023	Added extra local caps to PMIC Switching outputs as recommended in datasheet	Mistral Design Team		
	0.14	04 APR 2023	Modified SoC decaps & added RC circuit for I2C	Mistral Design Team		
	0.15	07 APR 2023	1. Added series resistors for RGMII TX signals 2. Swapped DDR DQ & DMI bits	Mistral Design Team		
	0.16	13 APR 2023	Implemented review comments from TI	Mistral Design Team	Nishant	Ajit
	0.17	18 APR 2023	1. Updated Internal and review comments from TI 2. Replaced Oscillator with new LMK6CE series (BAW), OLDI and DSI Connector.	Mistral Design Team	Nishant	Ajit
	0.18	03 MAY 2023	Modified the 3T decaps as 4 pin IC's and updated a few review comments from TI	Mistral Design Team	Nishant	
	0.19	10 MAY 2023	Modified the 2T current sense resistor parts to 4T sense similar to AM62A SK	Mistral Design Team	Nishant	
	0.20	16 MAY 2023	1. Replaced USB Type A load switch (with OC) & ESD protection device 2. Added capacitor to CT pin of VCC_3V3_SYS & VDD_MMC1 load switches	Mistral Design Team	Nishant	Ajit
	0.21	24 MAY 2023	1. VMON connection modified for PMIC to meet threshold of 3.3V 2. Part References Back annotated from PCB file	Mistral Design Team		
	0.22	16 JUNE 2023	1. Updated OPN's for SoC and PMIC 2. Removed dip switch for VDD_CORE voltage configuration. 3. Replaced HDMI connector part	Mistral Design Team	Nishant	
	0.23	21 JUNE 2023	1. Removed shorting jumper for VCC_CORE rail 2. Added dip switch control for EMU0 & EMU1 signals	Mistral Design Team	Nishant	
	0.24	23 JUNE 2023	1.Modified decaps for VDD_CORE 2.Replaced 3T SoC decaps with correct symbol & footprints	Mistral Design Team	Nishant	
	0.25	21 AUG 2023	1. Corrected power architecture & sequencing diagrams 2. Baselined	Mistral Design Team	Nishant	Ajit
E1-1	1.1	03 OCT 2023	1. Modified WD_DISABLE pull to VCC_3V3_MAIN 2. Modified PMIC_RSTOUT pull to VCC_3V3_SYS 3. Changed Assembly instruction for R280 to Mount 4. Changed the PMIC VSENSE voltage from VMAIN to VBUS_TYPEC1 and VBUS_TYPEC2 (dual input) and implemented ORing diode.	Mistral Design Team	Nishant	Ajit MB
	1.2	05 OCT 2023	Few circuits marked DNI as captured in change list document	Mistral Design Team	Nishant	Ajit MB
	2.0	21 NOV 2023	Baselined	Mistral Design Team	Nishant	Ajit MB
	2.1	05 JUNE 2024	1. Enabled Voltage ratings for all the capacitors and added Design Review notes 2. R133,R643 - 0E changed to 22E; R91,R127 - 3.4K_1% changed to 3.48K_1%. 3. C273 - 4.7uF changed to 1uF ; C275 - 0.1uF changed to 4.7uF ; C276,C178,C180 - 1uF changed to 0.1uF ; C40,C43 - 12pF changed to 18pF ; C177,C175 - 2.2uF changed to 1uF.	Mistral Design Team		

LINKS TO KEY FAQs

(10) [FAQ] AM62P / AM62P-Q1 Custom board hardware design - Collaterals to Get started - Processors forum - Processors - TI E2E support forums
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-am62px-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1340906/faq-am62p-am62p-q1---custom-board-hardware-design---Design-and-review-notes-for-reuse-of-sk-am62p-lp-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1306030/faq-am62p-am62p-q1-custom-board-hardware-design--faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit

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Title REVISION HISTORY

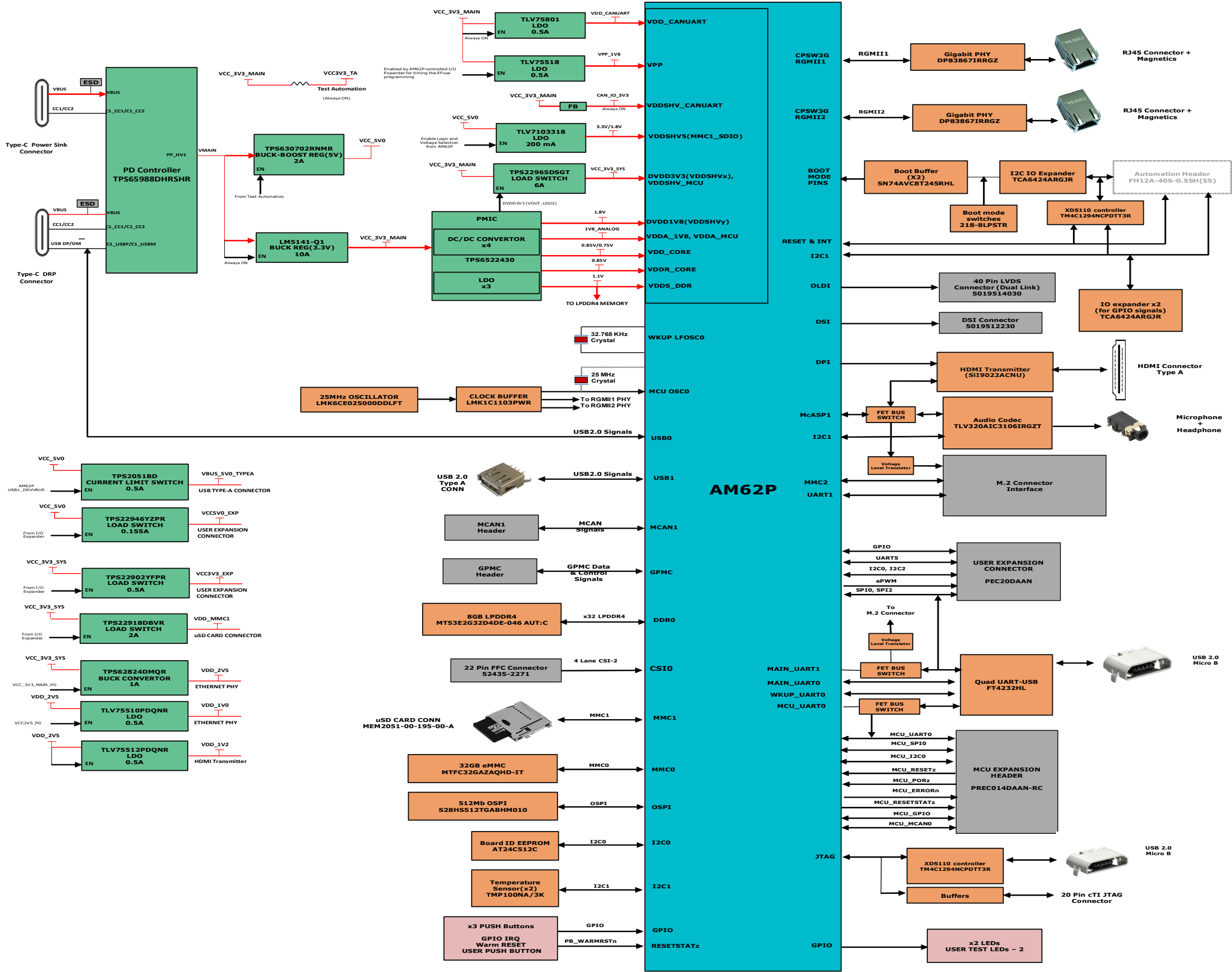
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BLOCK DIAGRAM - AM62P SKEVM

D-Note :-
Pins (OBSCLK) AA25 and B25 of the SoC are main domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible
Pin (MCU_OBSCLK) E10 of the SOC are MCU Domain Observation clock output for test and debug purposes only.
Add a TP near to the SoC and provision to isolate the signal for testing whenever possible

D-Note :-
Drive strength configuration is currently not supported. The drive strength must remain in the default state since this is the only condition used during timing closure of the Peripherals. The devices are set to maximum drive strength. Please reference to the IBIS model to find the drive strength of the IOs.

D-Note :-
Refer Device Comparison section of the processor data sheet for supported cores, peripherals and memory size



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Title BLOCK DIAGRAM AM62A_ SKEVM

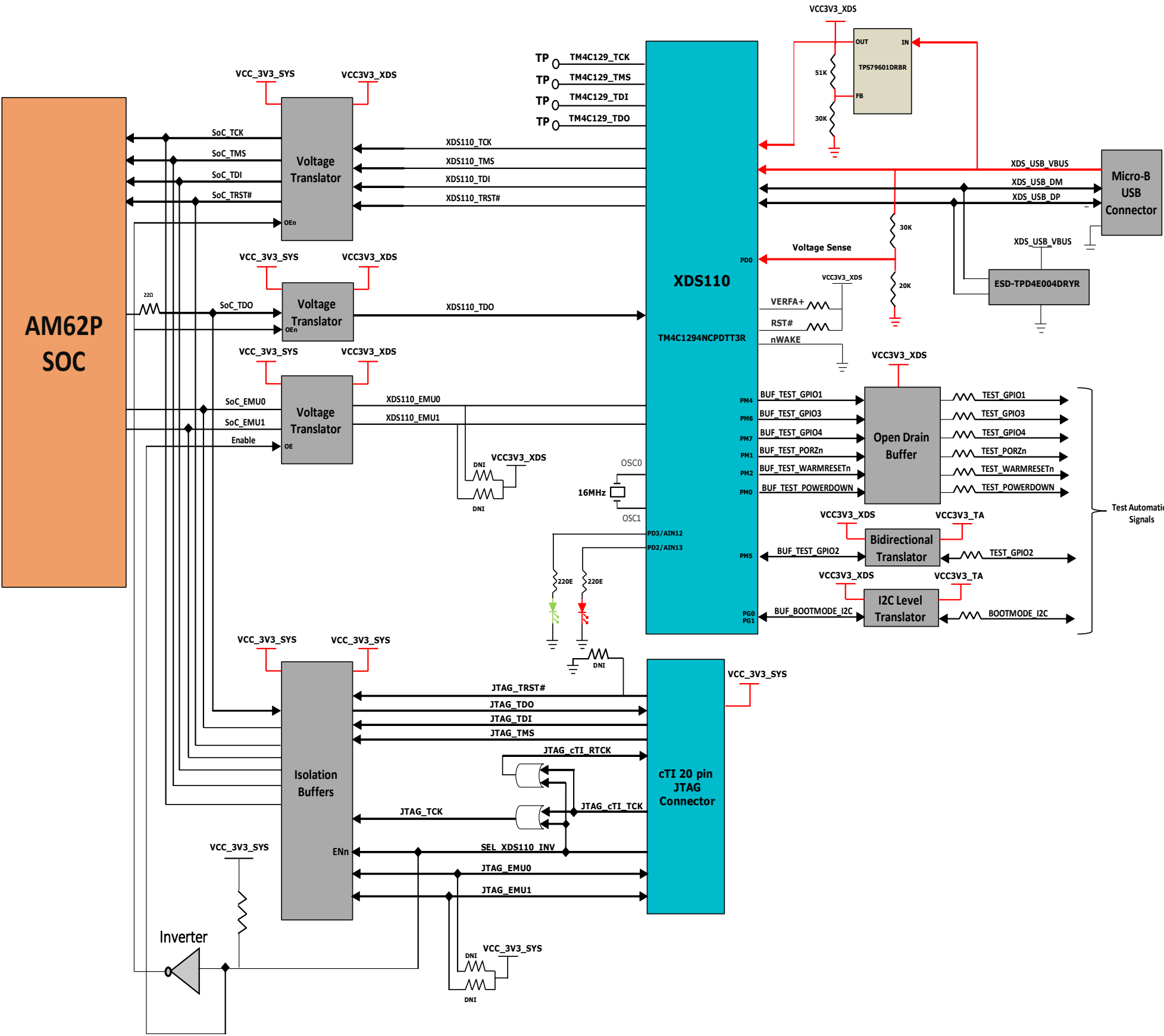
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BLOCK DIAGRAM - XDS110



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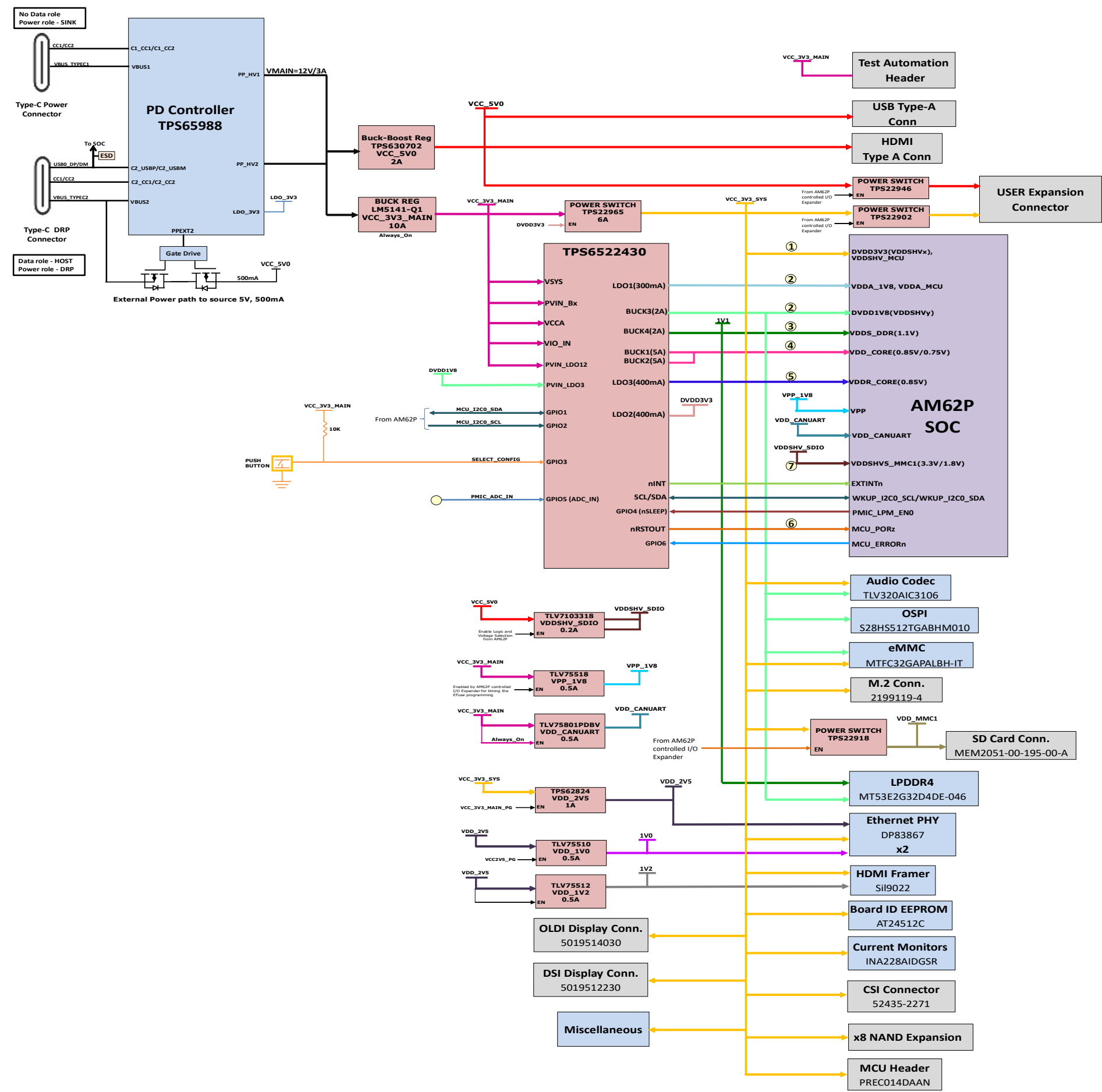
Title BLOCK DIAGRAM_XDS110

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POWER ARCHITECTURE BLOCK DIAGRAM



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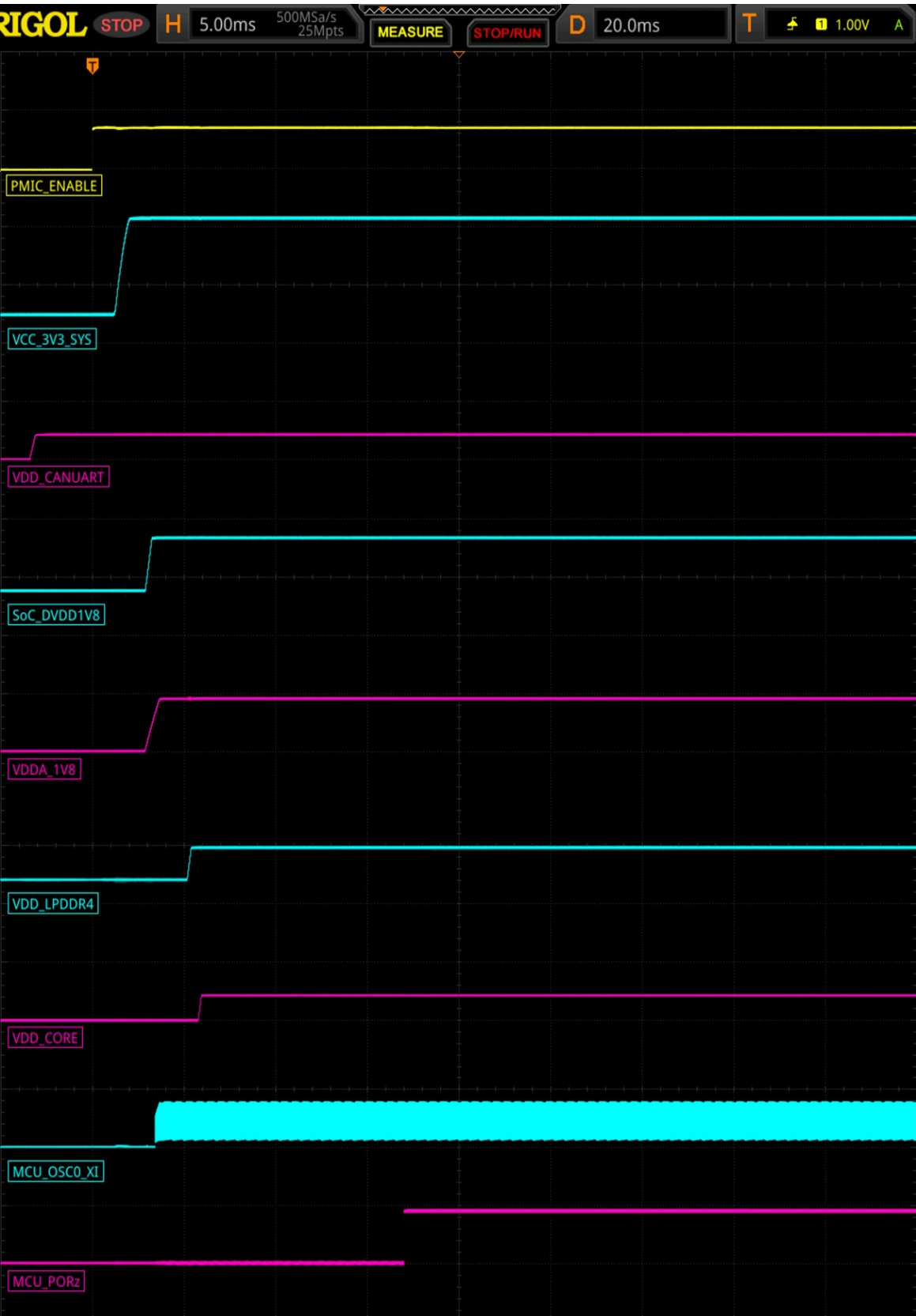
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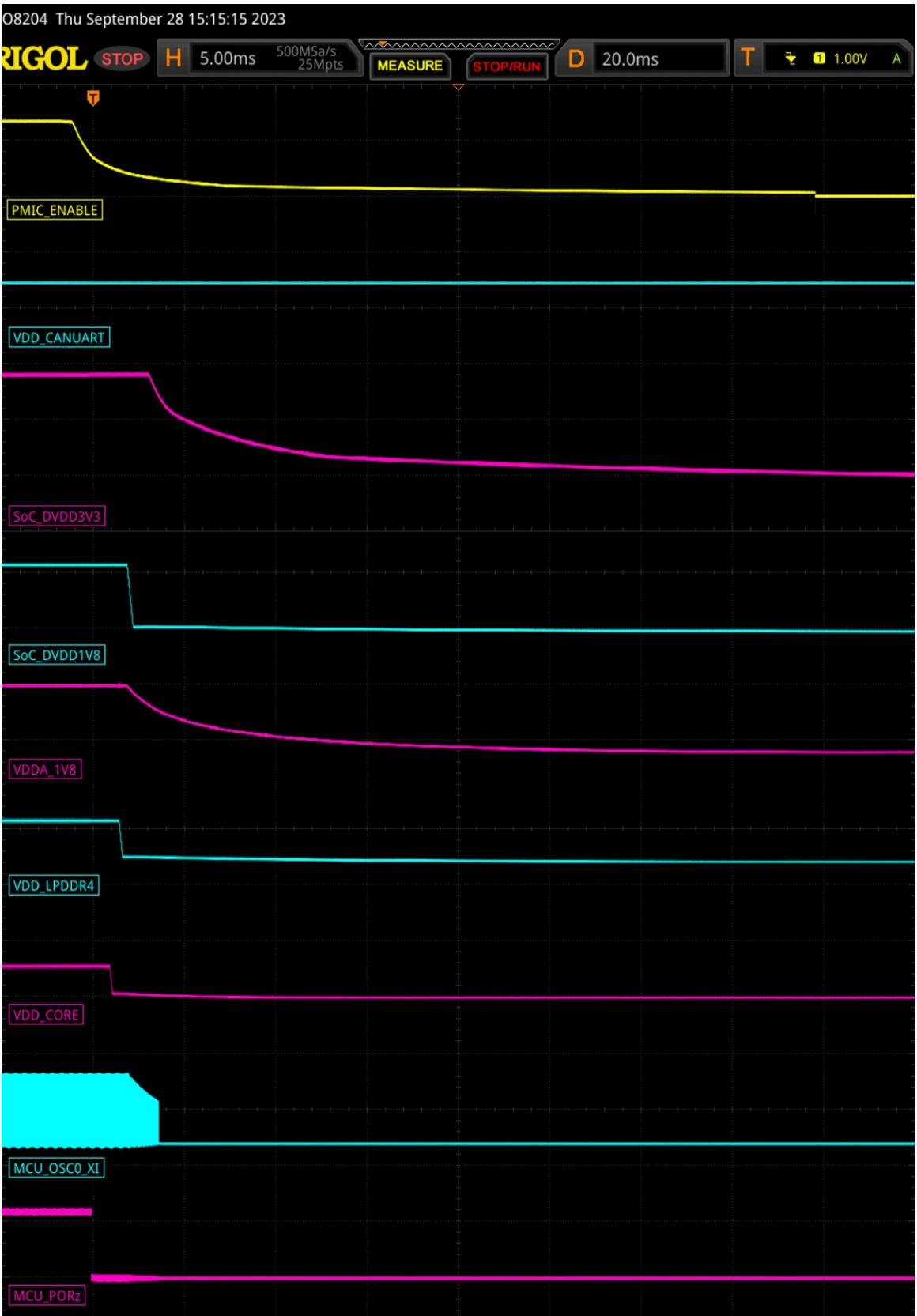
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POWER UP SEQUENCE



POWER DOWN SEQUENCE



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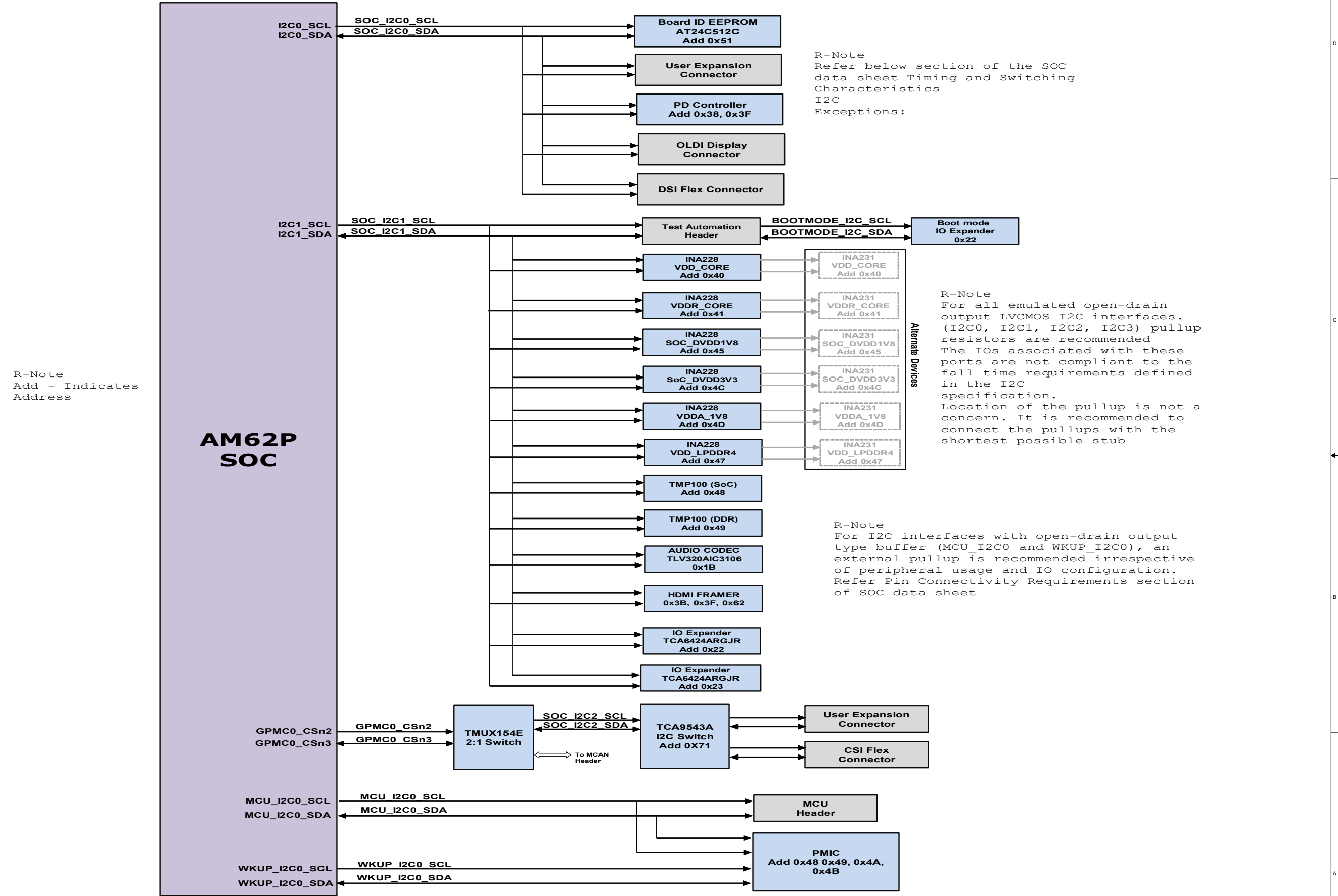
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I2C TREE



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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_0	MCU_SPI0_CS0	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
9	PMIC Interrupt	PMIC_INTn	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
11	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
12	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	User Interrupt									
15	Low power mode enable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
16	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_31	GPMC0_CLK	OUTPUT	NA	NA	VDDSHV2	SoC_DVDD3V3
IO EXPANDER – 01										
1	Interrupt from OLDI display	OLDI_INT#	INTERRUPT	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	x8 NAND Card Presence Detect	x8_NAND_DETECT	DETECTION	IO EXPANDER-P01		INPUT	HIGH	LOW		VCC_3V3_SYS
3	MCASP1 Enable and Direction Control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
10	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
11	OLDI to HDMI Card Device ID interrupt	OLDI_EDID	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSIO GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSIO GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P01		OUTPUT	LOW	HIGH		VCC_3V3_SYS
3	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SoC I2C2 & MCAN MUX Selection	SoC_I2C2_MCAN_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	HIGH	-		VCC_3V3_SYS
5	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	OLDI display Reset control GPIO	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

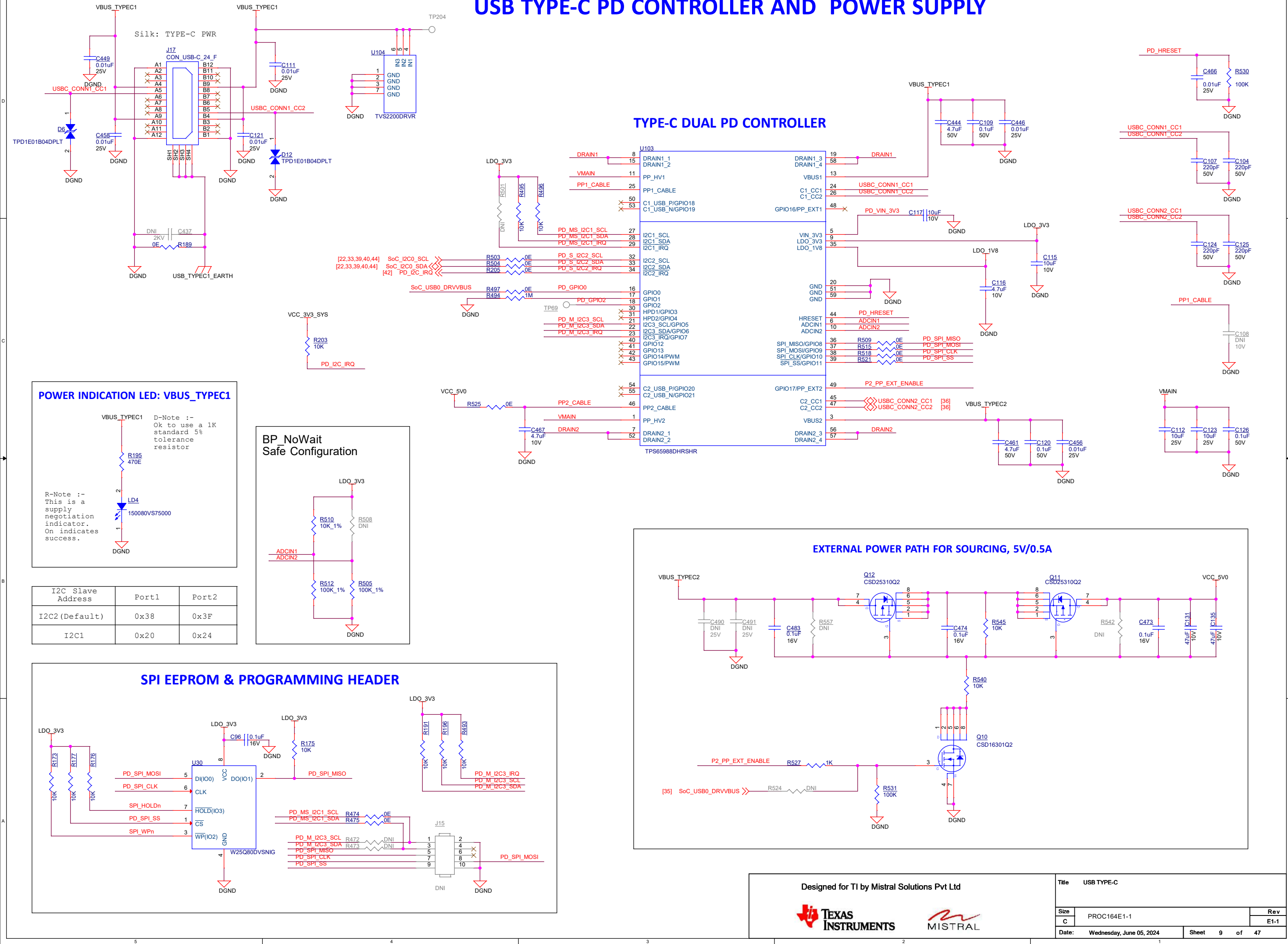
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Title GPIO MAPPING TABLE

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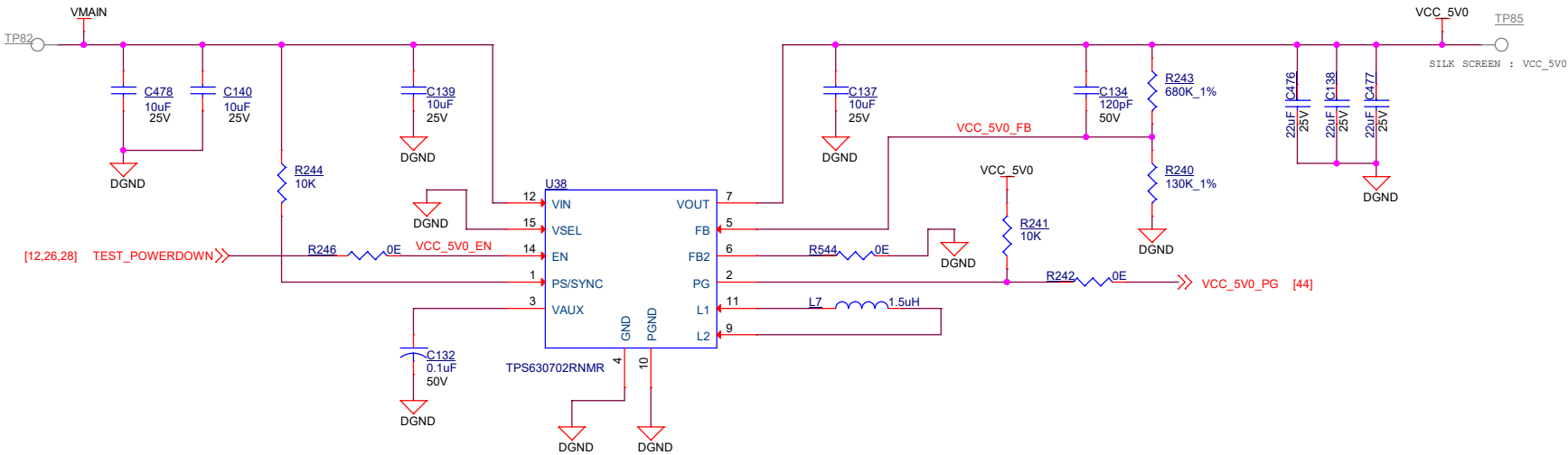
USB TYPE-C PD CONTROLLER AND POWER SUPPLY



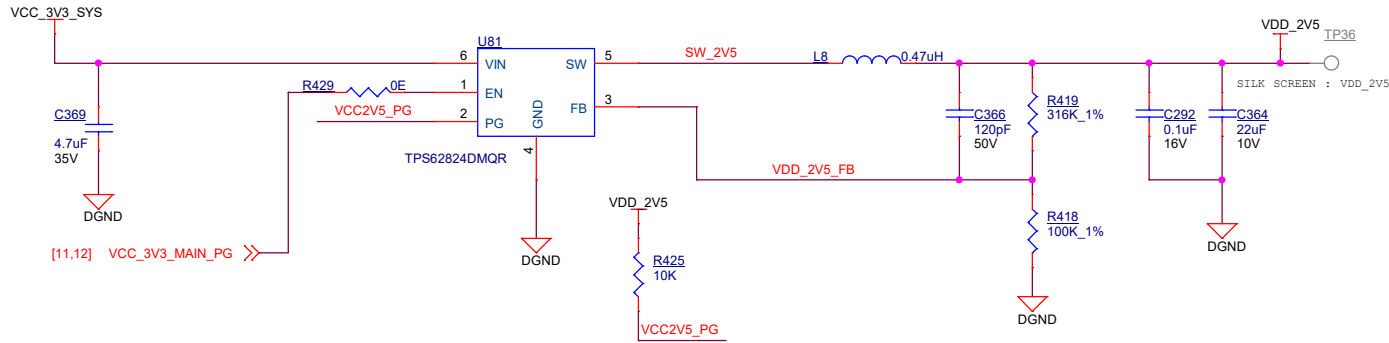
PERIPHERAL POWER SUPPLY-1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A

D-Note :-
Add a Jumper or OR for isolation or Current measurement
for preproduction board

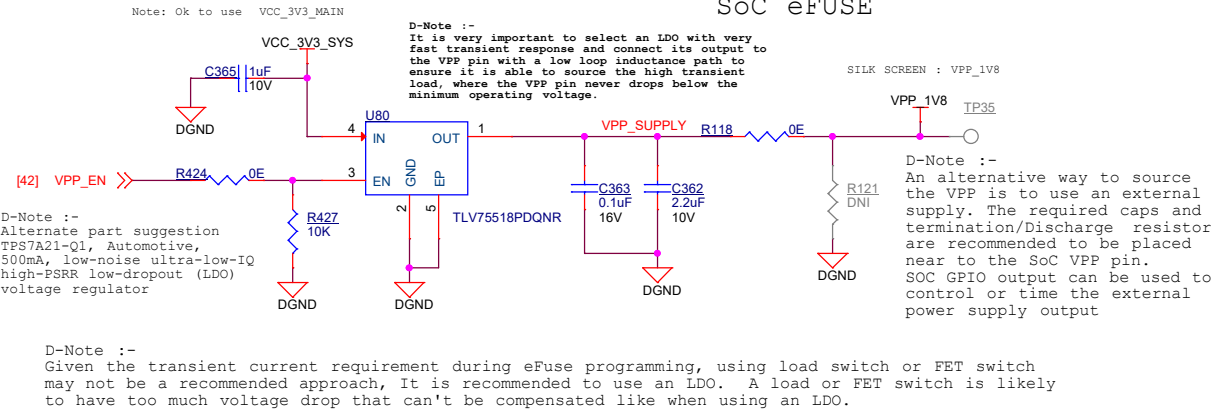


2.5V (ETHERNET PHY), 1.0AMPS SUPPLY

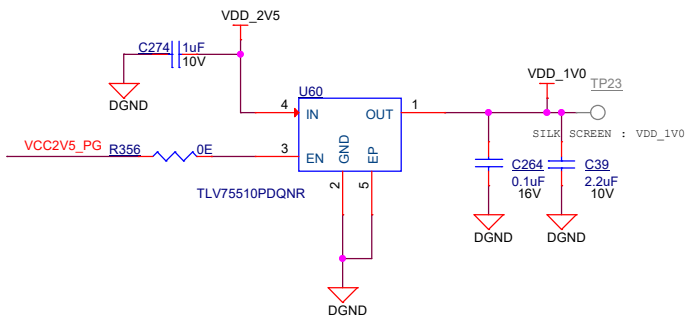


1.8V VPP (eFUSE), 0.5AMPS SUPPLY

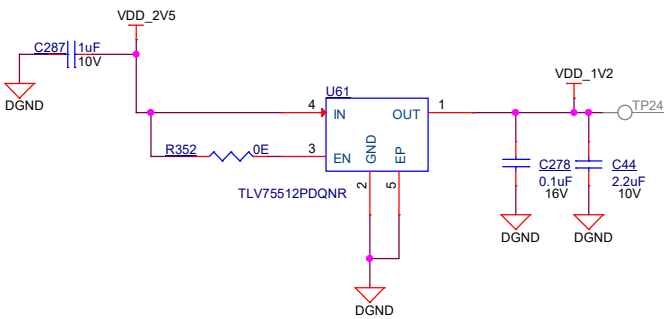
SoC eFUSE



1.0V (ETHERNET PHY), 0.5AMPS SUPPLY

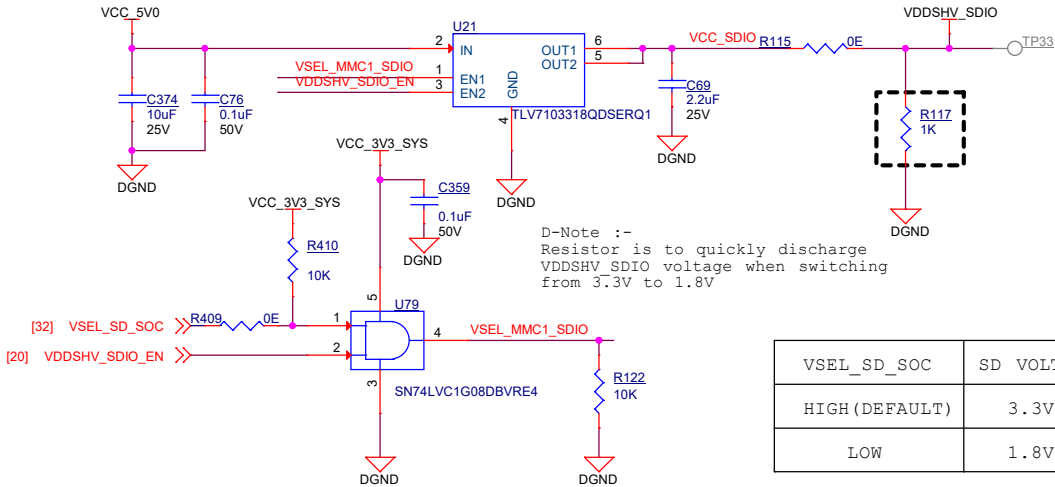


1.2V (HDMI), 0.5AMPS SUPPLY



3.3V/1.8V SD CARD IO SUPPLY

R-Note :-
SD card interface IO supply voltage switching (3.3V/1.8V) is required to support higher speed data rates. Refer SOC data sheet for supported rates and IO voltage levels



VSEL_SD_SOC	SD VOLTAGE
HIGH (DEFAULT)	3.3V
LOW	1.8V

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Title PERIPHERAL POWER SUPPLY -1

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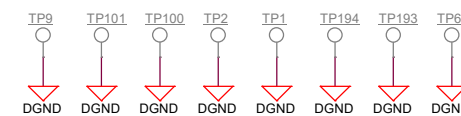
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3.3V, 10.0 AMPS SUPPLY

[34] ETH_CAN_INH_PREREG >> DN R75 EN_LM5141_ON

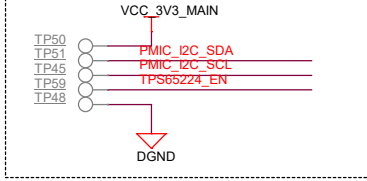


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PMIC Config option

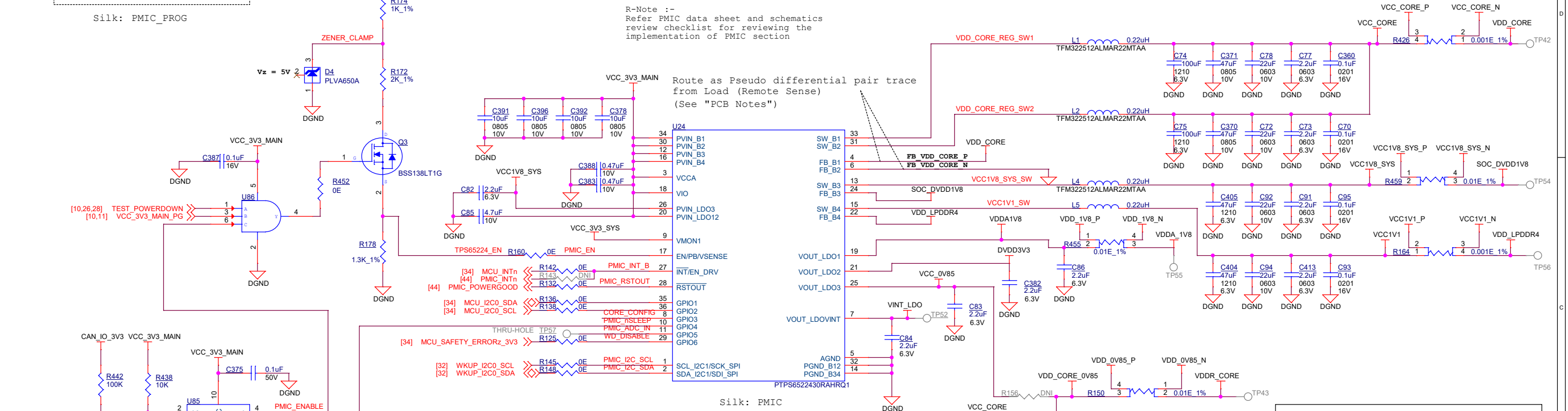


Silk: PMIC_PROG

SOC POWER SUPPLY PMIC

R-Note :-
Refer PMIC data sheet and schematics
review checklist for reviewing the
implementation of PMIC section

CAD Note :-
Follow Kelvin connection for Current
Sensing when using 2 terminal resistors



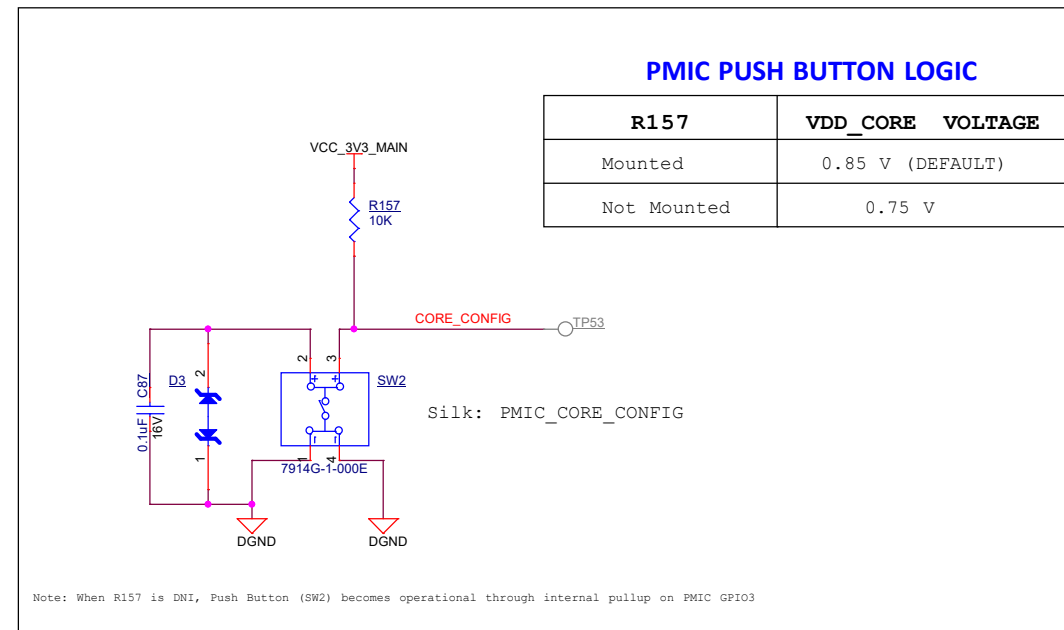
Route as Pseudo differential pair trace
from Load (Remote Sense)
(See "PCB Notes")

Silk: PMIC

PMIC uses default I2C1 ADDR: 0x48, 0x49, 0x4A, 0x4B

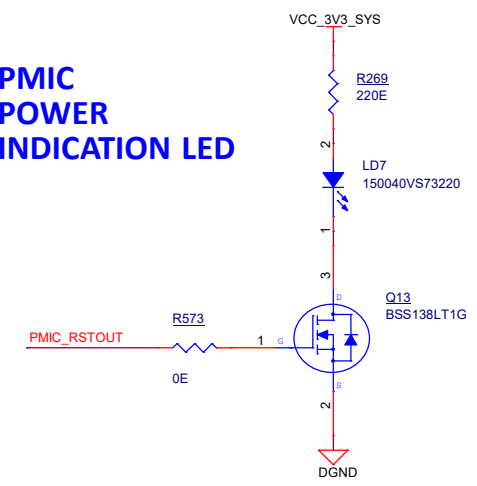
PMIC PUSH BUTTON LOGIC

R157	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

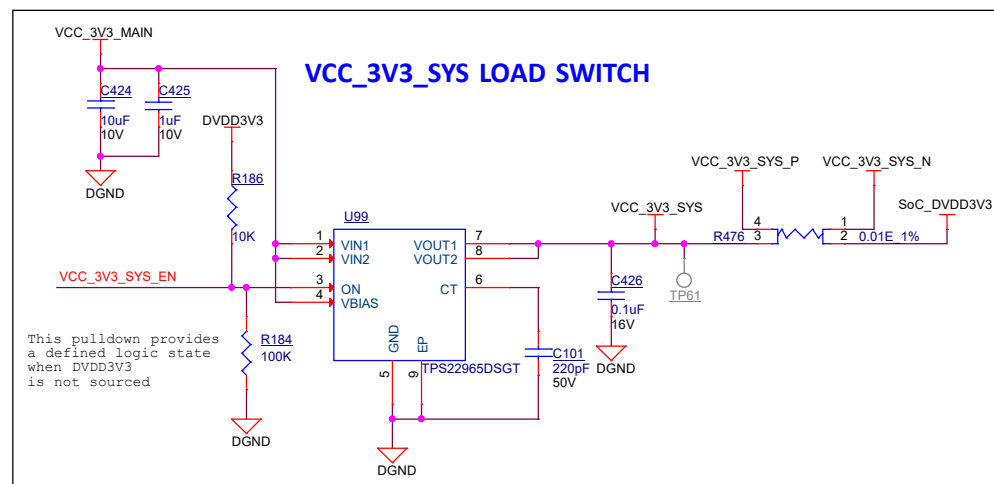


Note: When R157 is DNI, Push Button (SW2) becomes operational through internal pullup on PMIC GPIO3

PMIC POWER INDICATION LED



VCC_3V3_SYS LOAD SWITCH



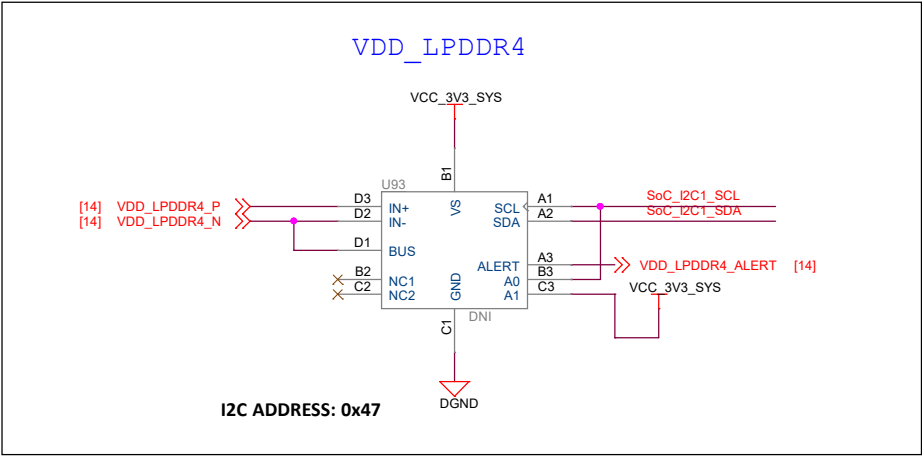
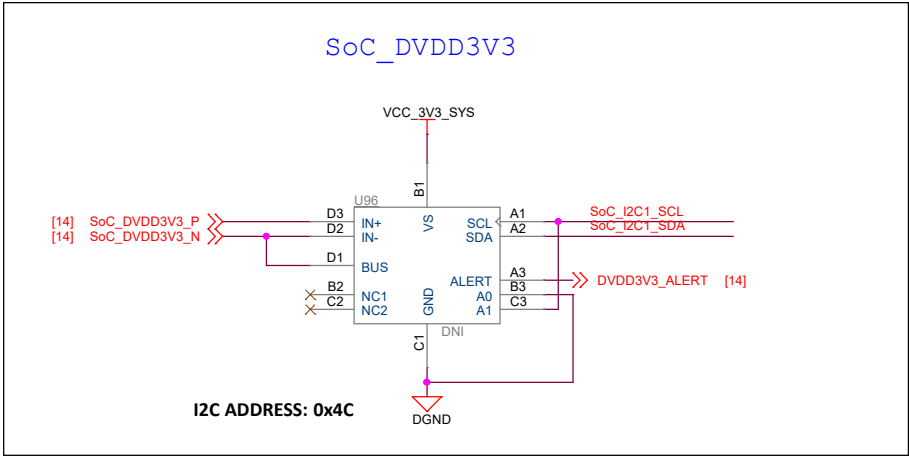
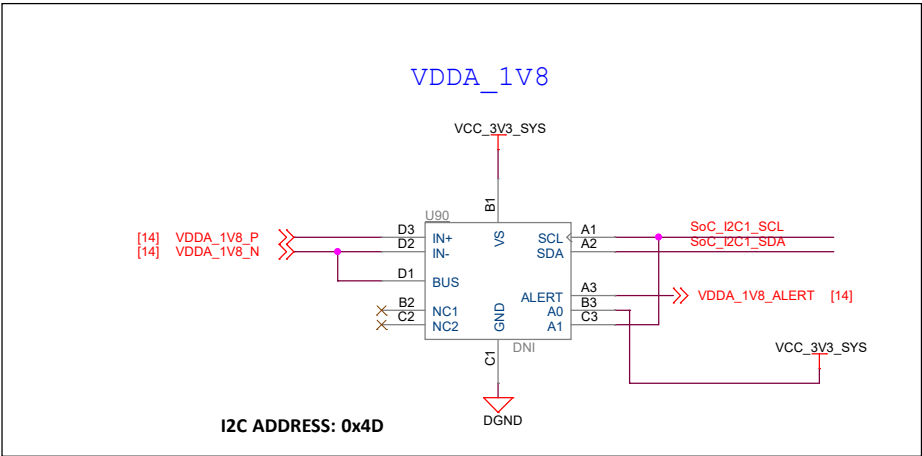
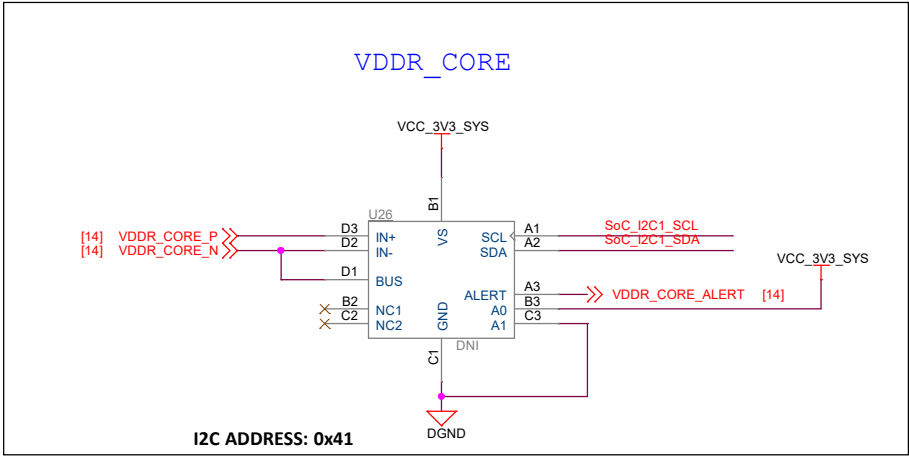
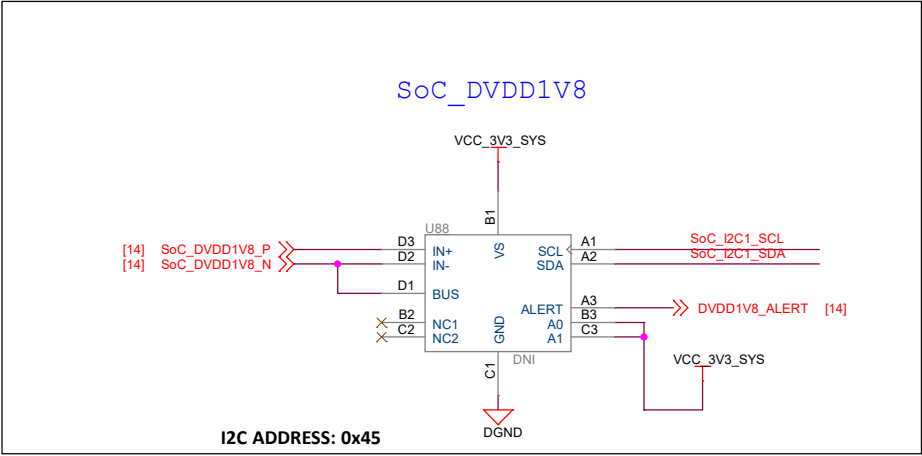
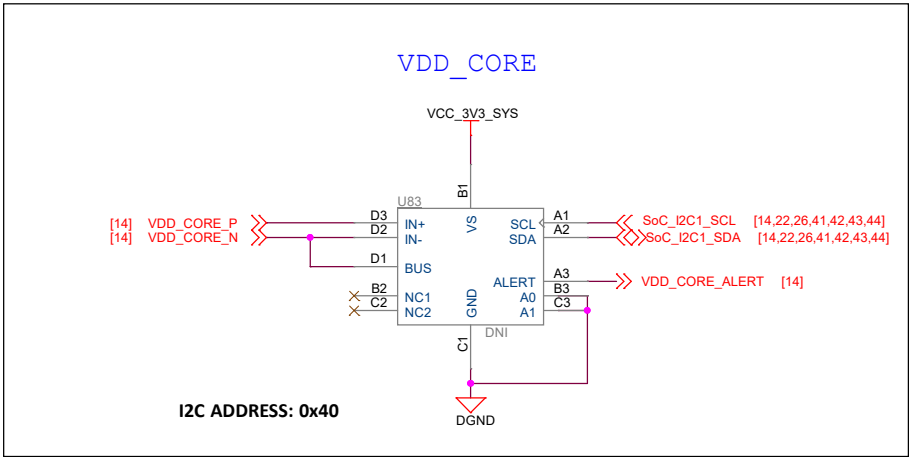
This pulldown provides
a defined logic state
when DVDD3V3
is not sourced

Designed for TI by Mistral Solutions Pvt Ltd



Title		SOC POWER SUPPLY PMIC	
Size	PROC164E1-1	Rev	E1-1
C			
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CURRENT MONITORING DEVICES - 1



Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

Designed for TI by Mistral Solutions Pvt Ltd



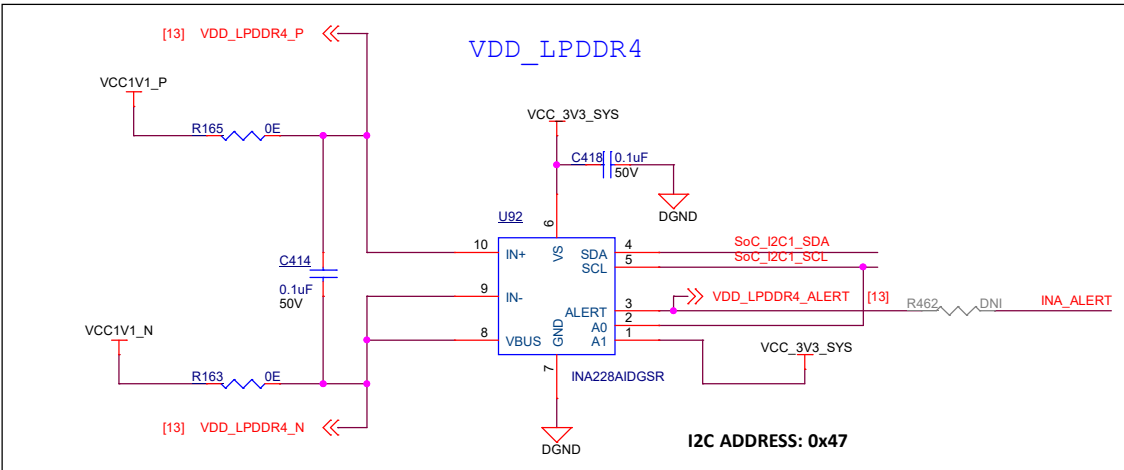
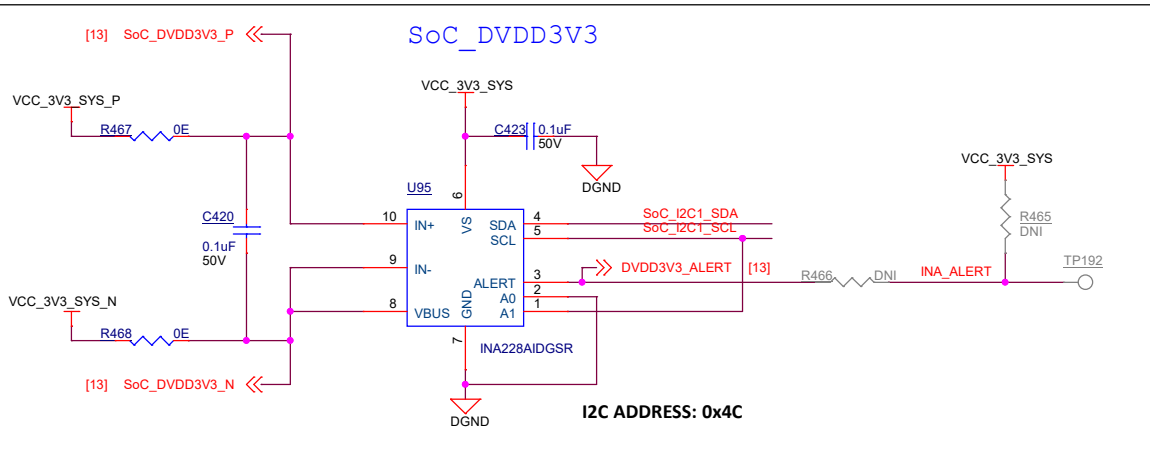
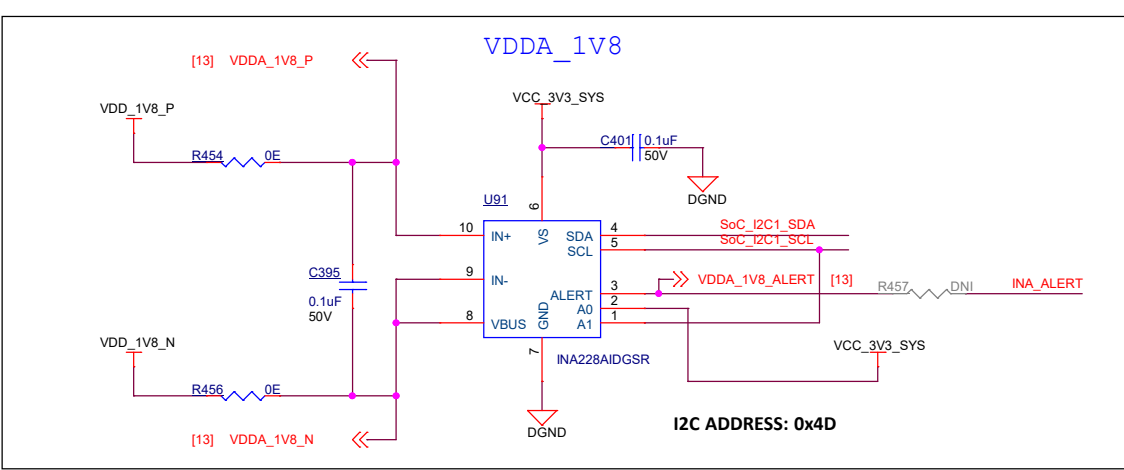
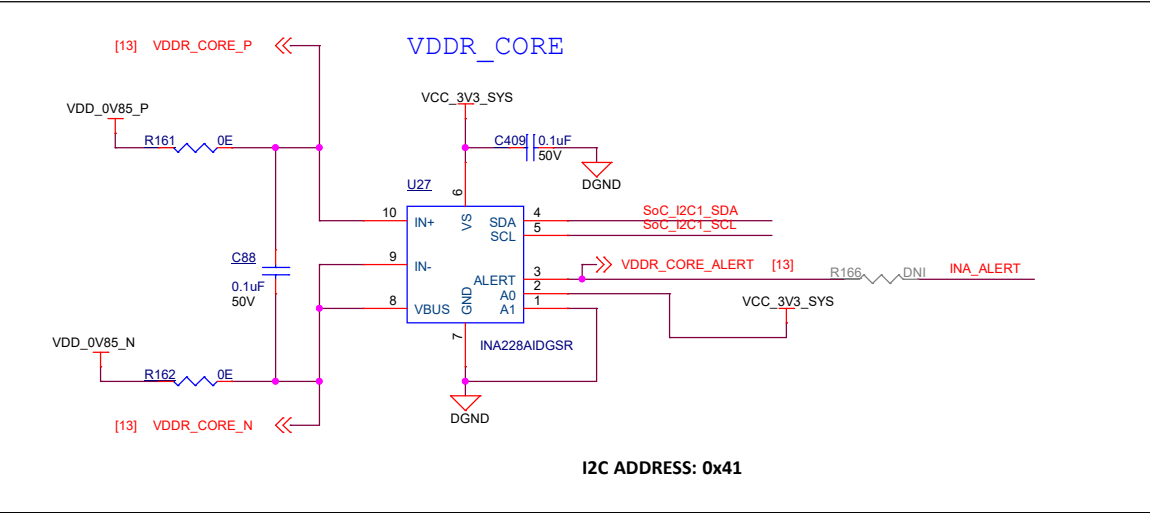
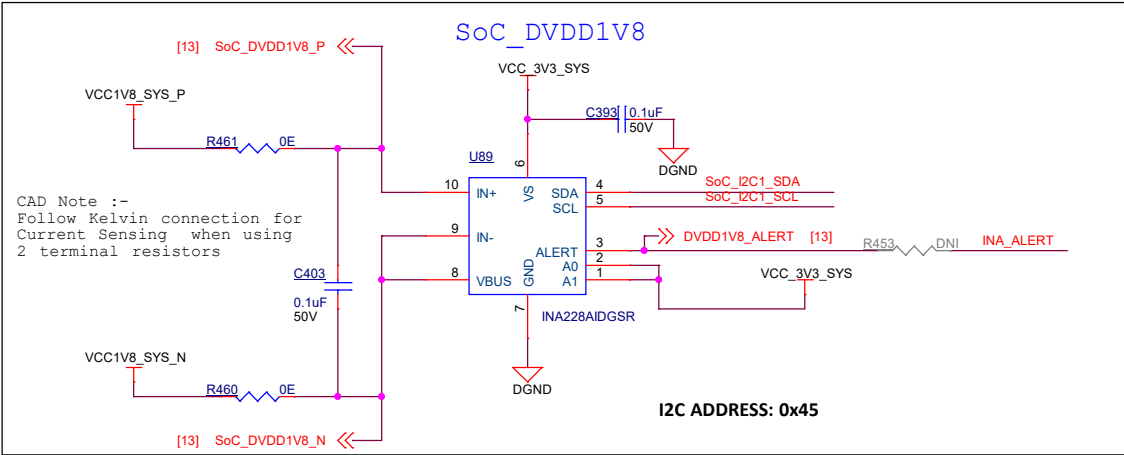
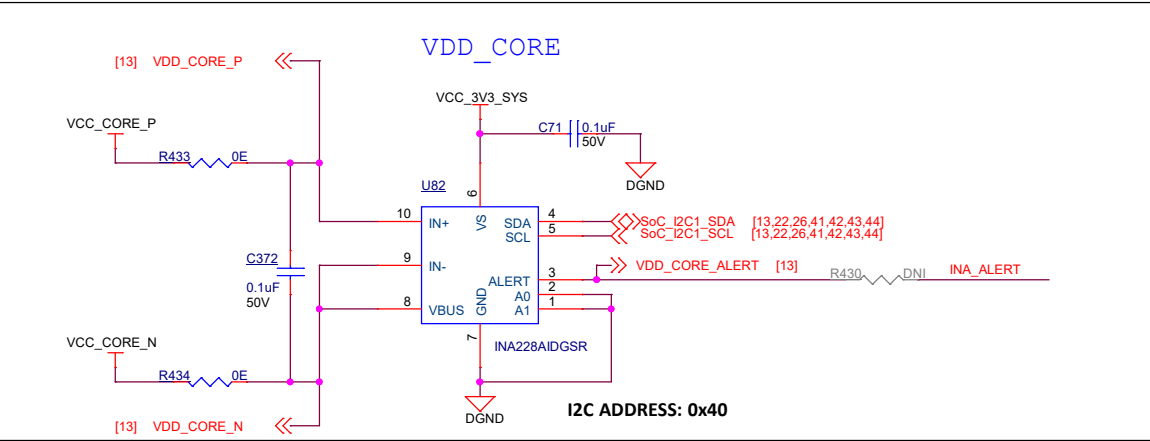
Title CURRENT MONITORING DEVICES - 1

Size C
PROC164E1-1

Rev E1-1

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CURRENT MONITORING DEVICES - 2



Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

Designed for TI by Mistral Solutions Pvt Ltd



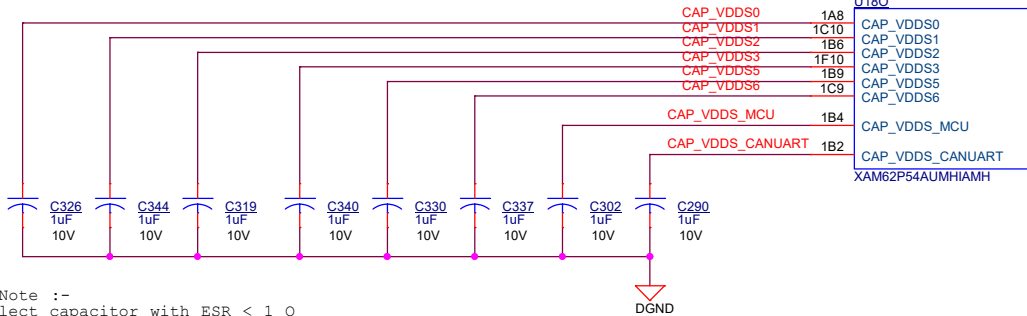
Title CURRENT MONITORING DEVICES - 2

Size PROC164E1-1

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Rev E1-1

SOC POWER



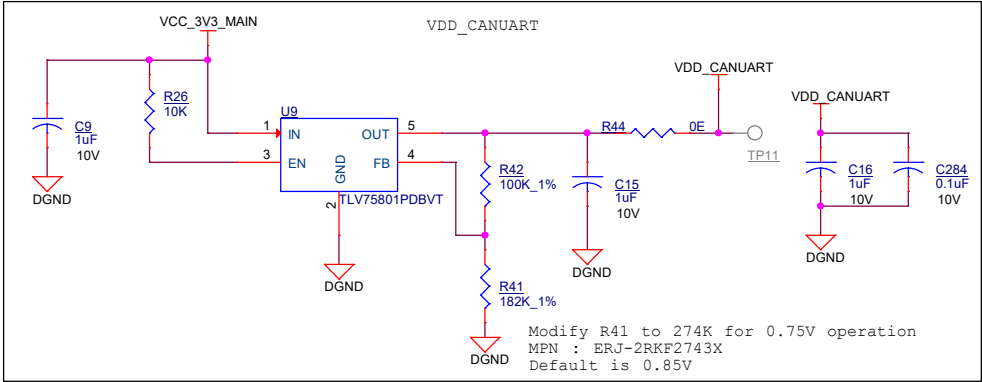
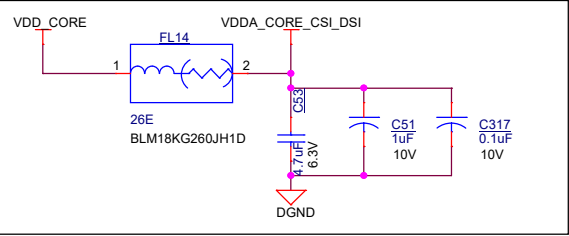
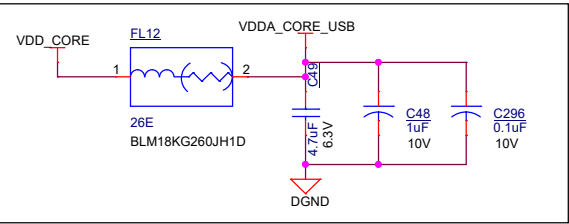
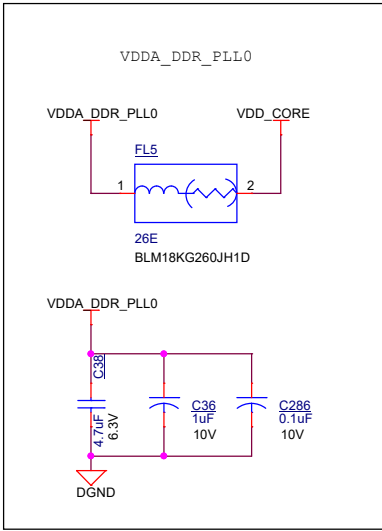
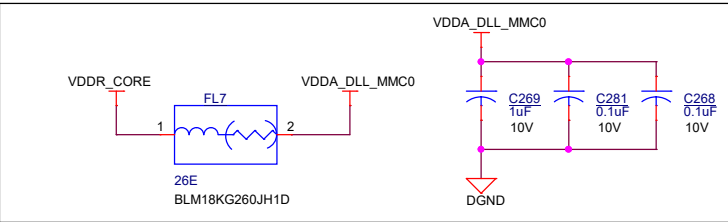
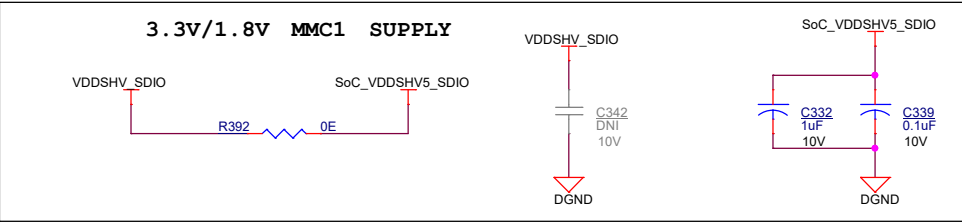
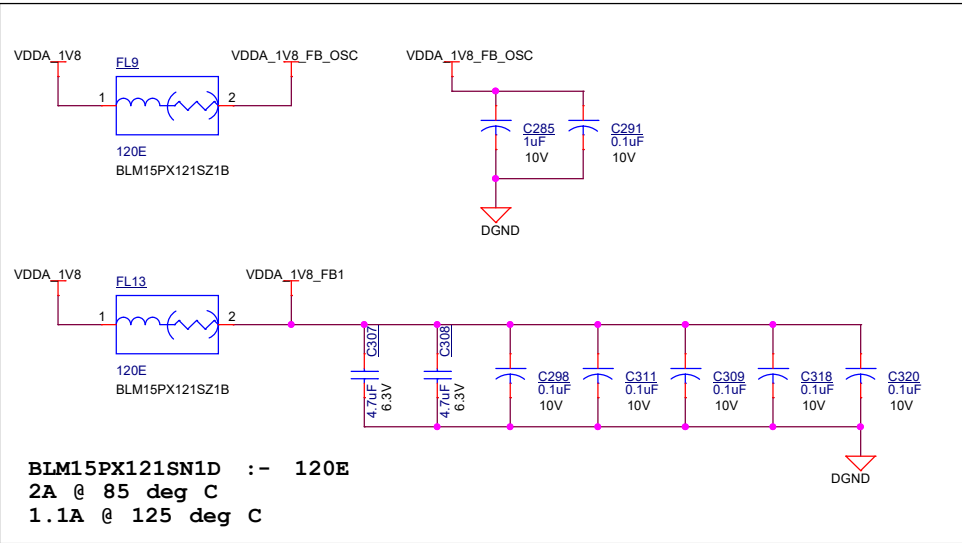
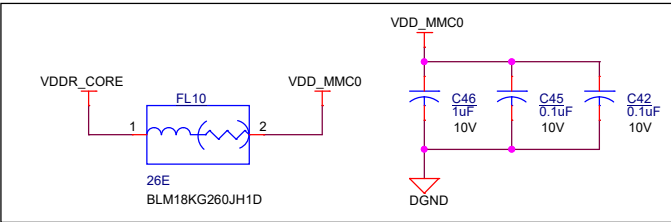
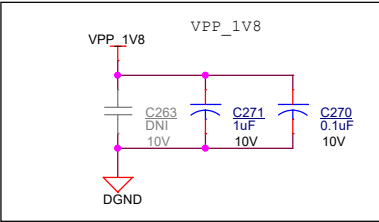
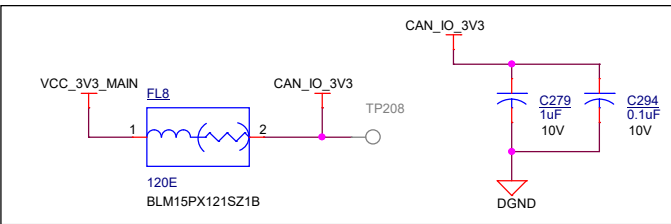
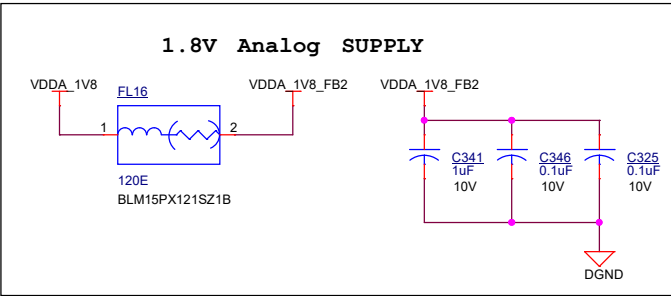
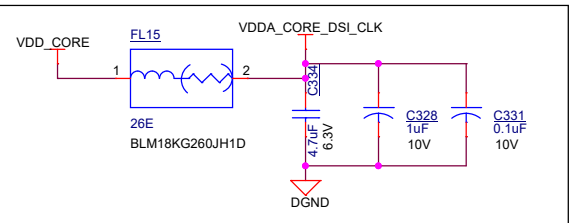
D-Note :- A Trace connected to SOC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest at the highest impedance end of the signal. By placing a pull-up or pull-down near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

```

-DNote :-
Common SOC LVCMOS IO interface guidelines
1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slow rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being
driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull.
When adding pull is not feasible, ensure the traces are routed away from noisy signals

```

CORE SUPPLY

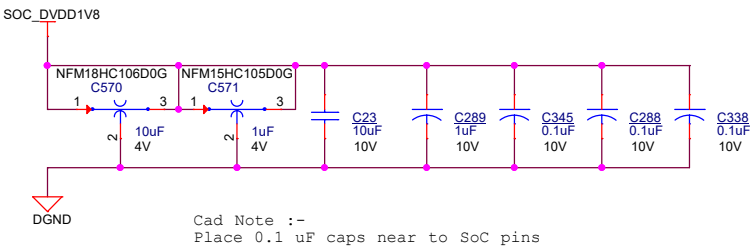
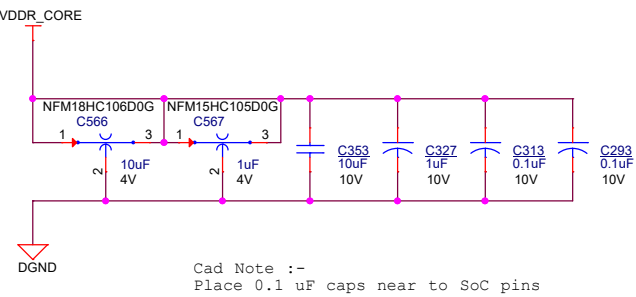
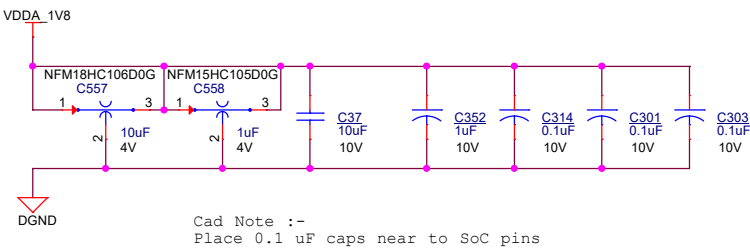
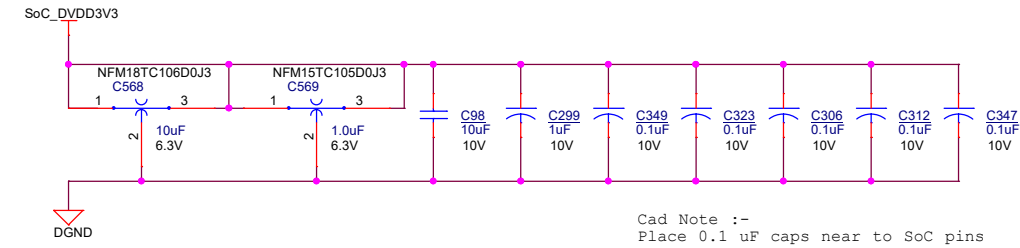
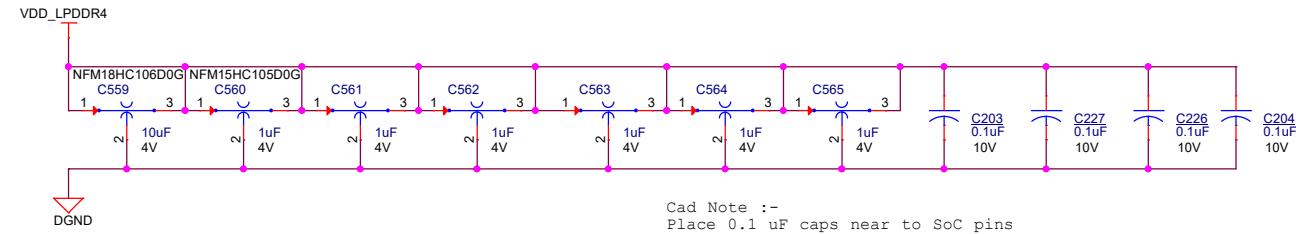
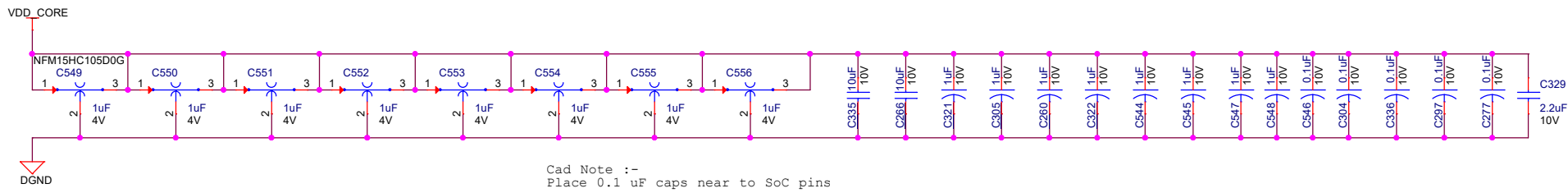


Title SOC POWER



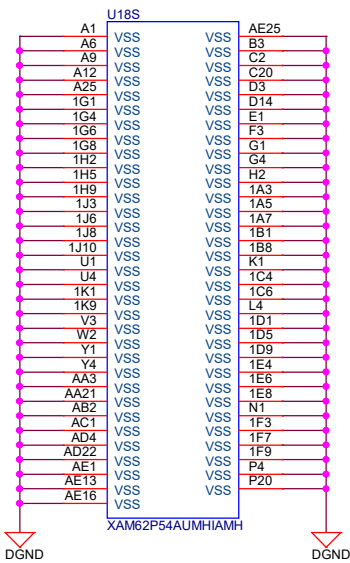
Size	PROC164E1-1	Rev
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SOC POWER DECAPS

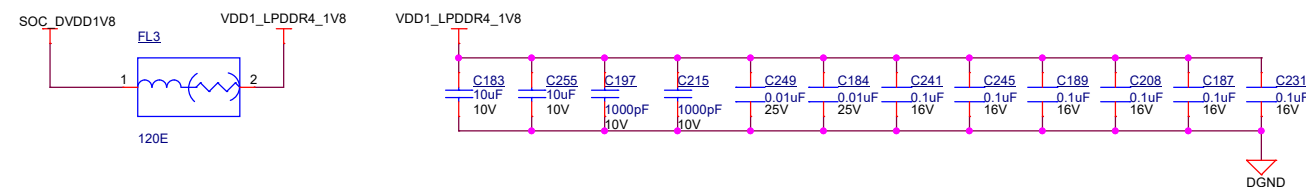
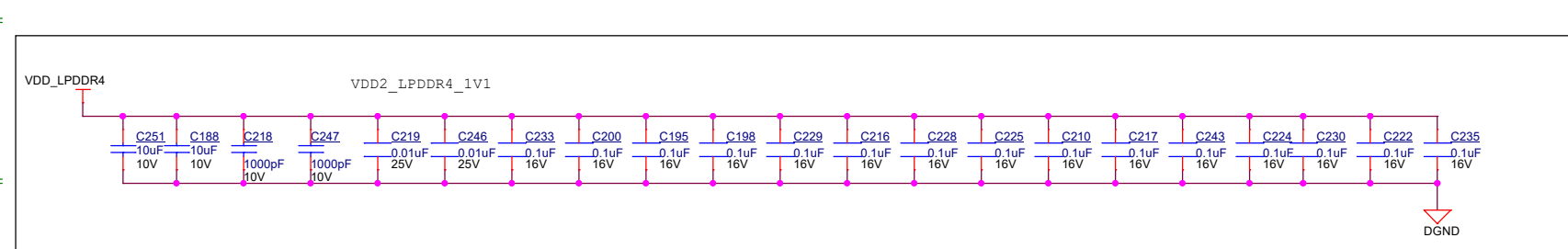


R-Note :-
Use of 3 terminal caps optimizes use of
bulk caps and minimizes the PCB inductance

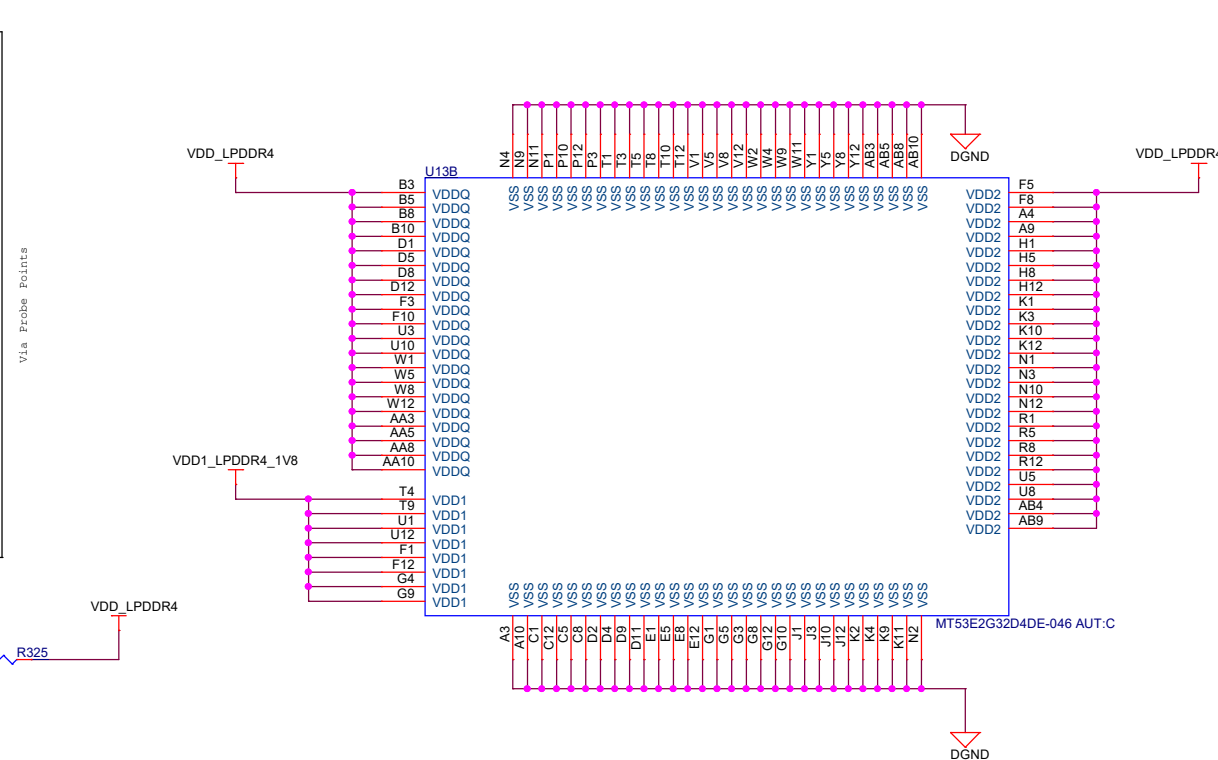
SOC VSS



LPDDR4 POWER DECAPS



Silk: LPDDR4



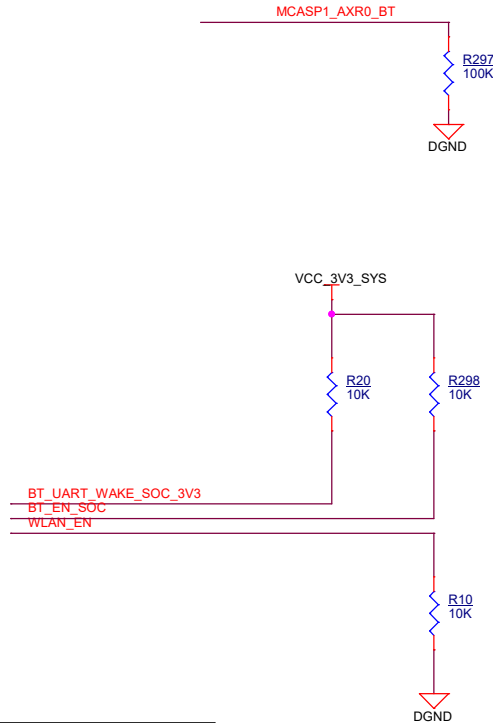
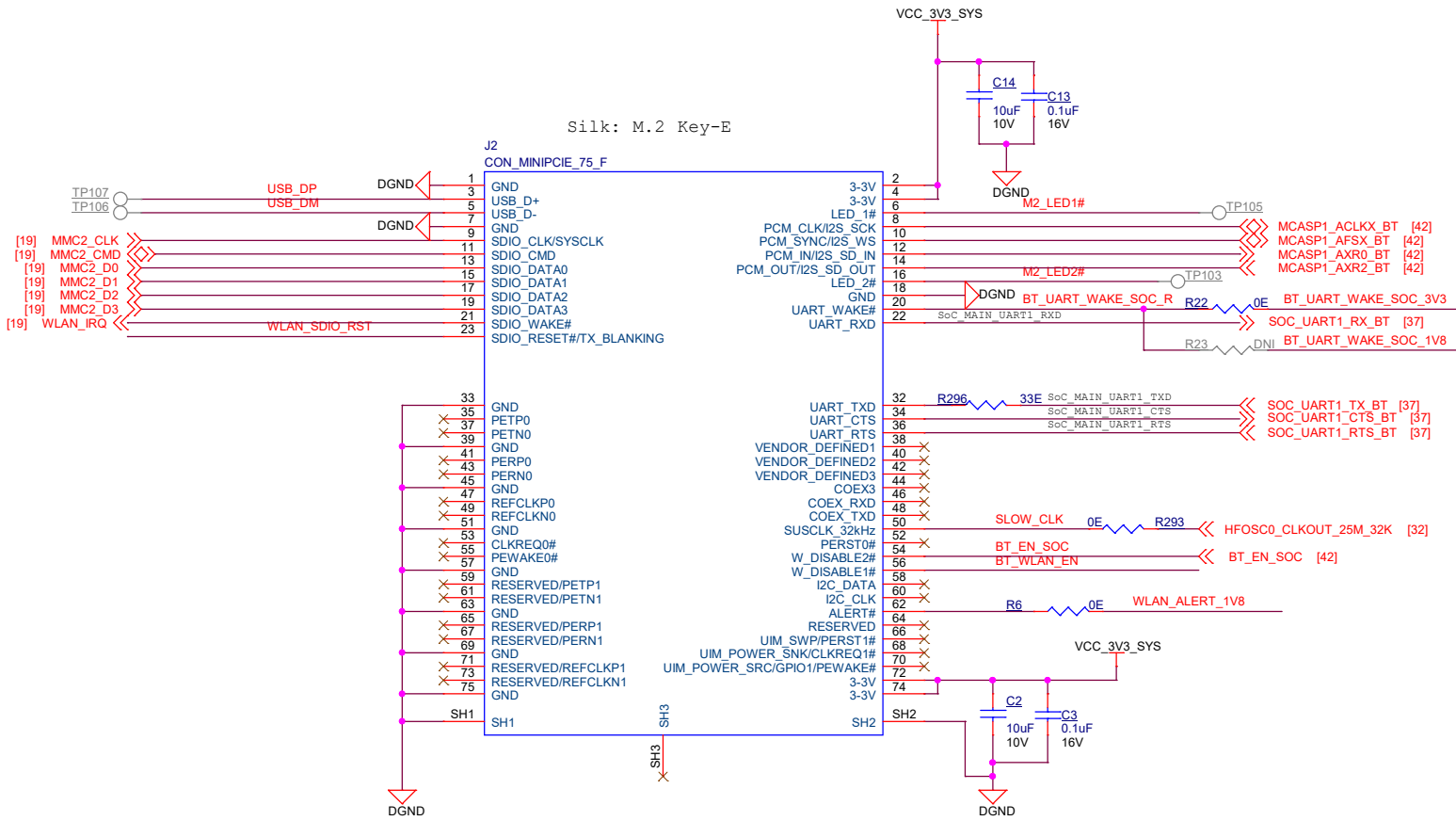
D-Note :-
10 K pulldown is recommended
Refer Processor specific DDR design guide



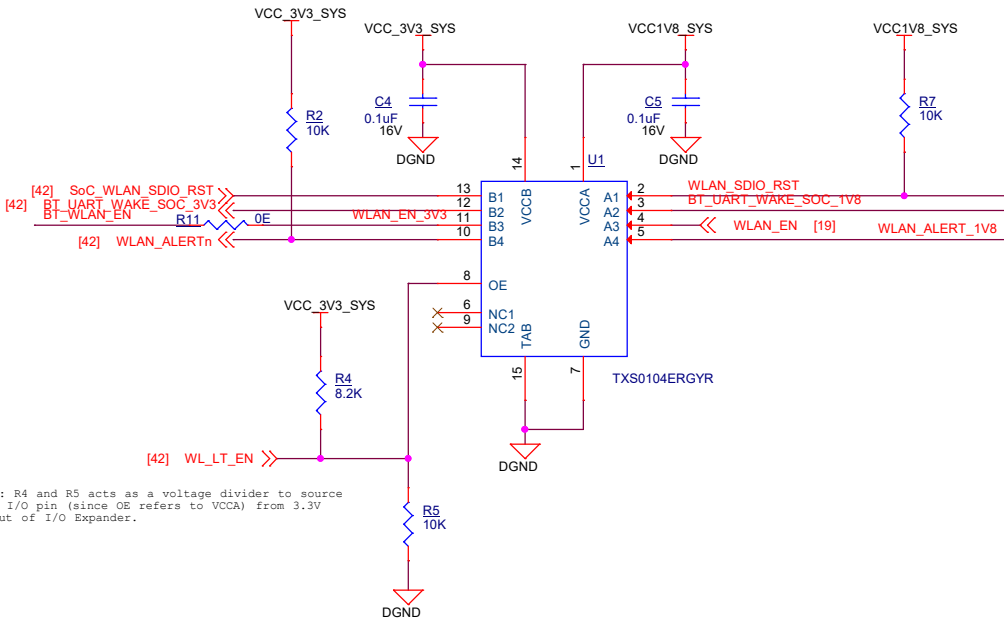
MISTRA

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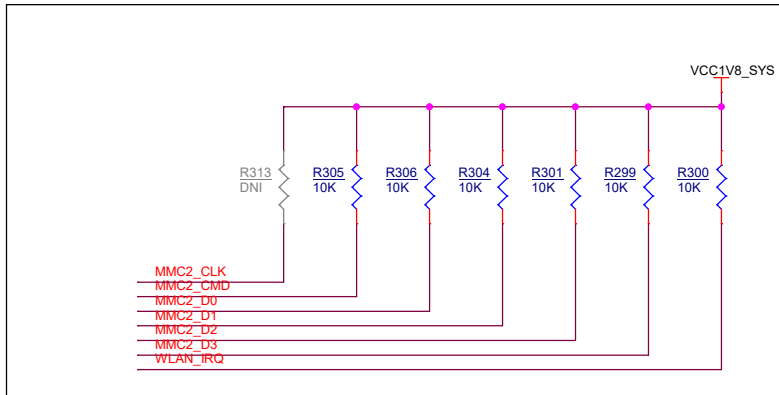
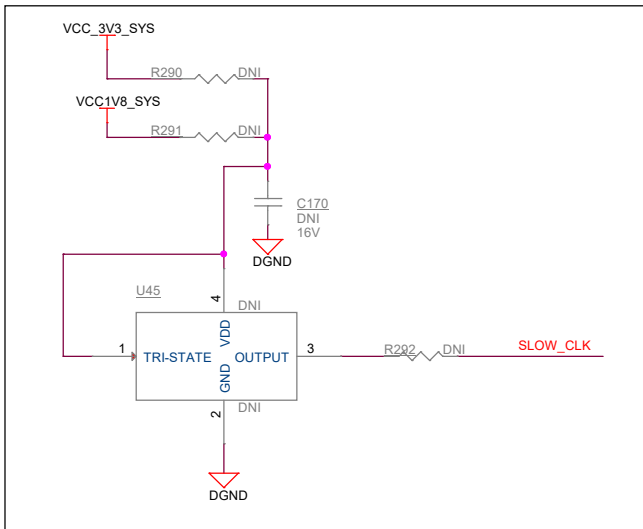
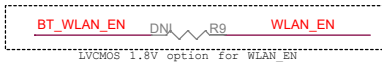
M.2 INTERFACE - SDIO



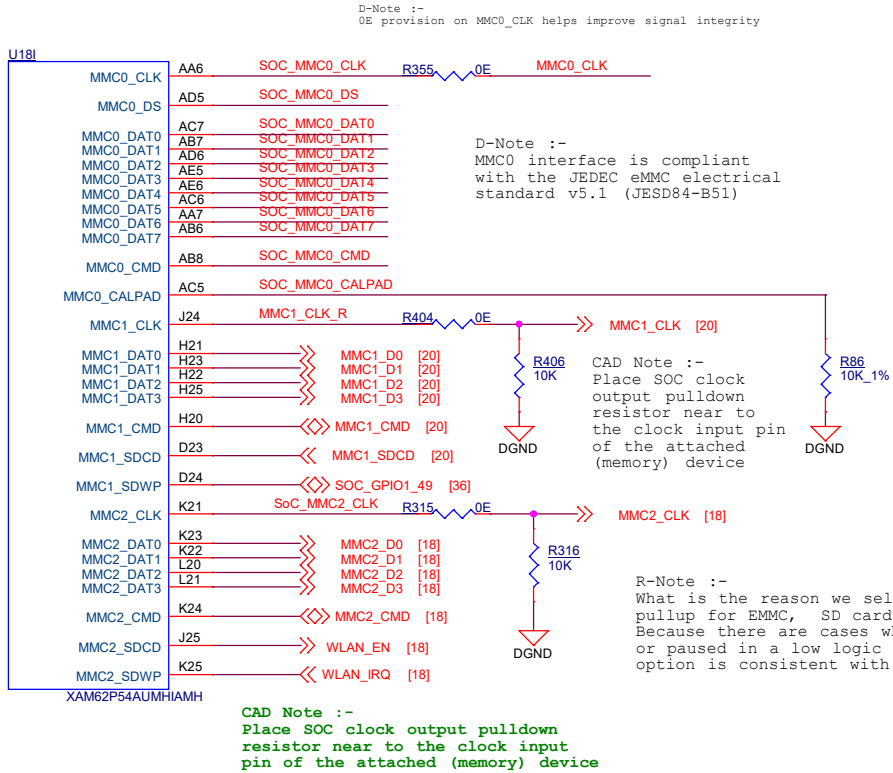
M.2 LEVEL TRANSLATOR



Note: R4 and R5 acts as a voltage divider to source 1.8V I/O pin (since OE refers to VCCA) from 3.3V output of I/O Expander.



SOC - MMC Interface



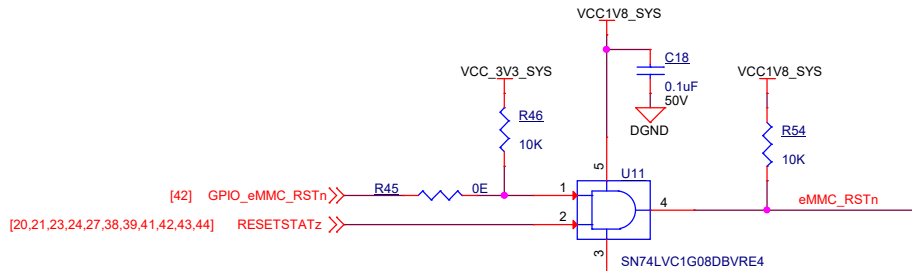
D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDI or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

D-Note :-
You could eliminate the GPIO option and only use the reset output (Warm or Cold), where software forces a warm reset if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.

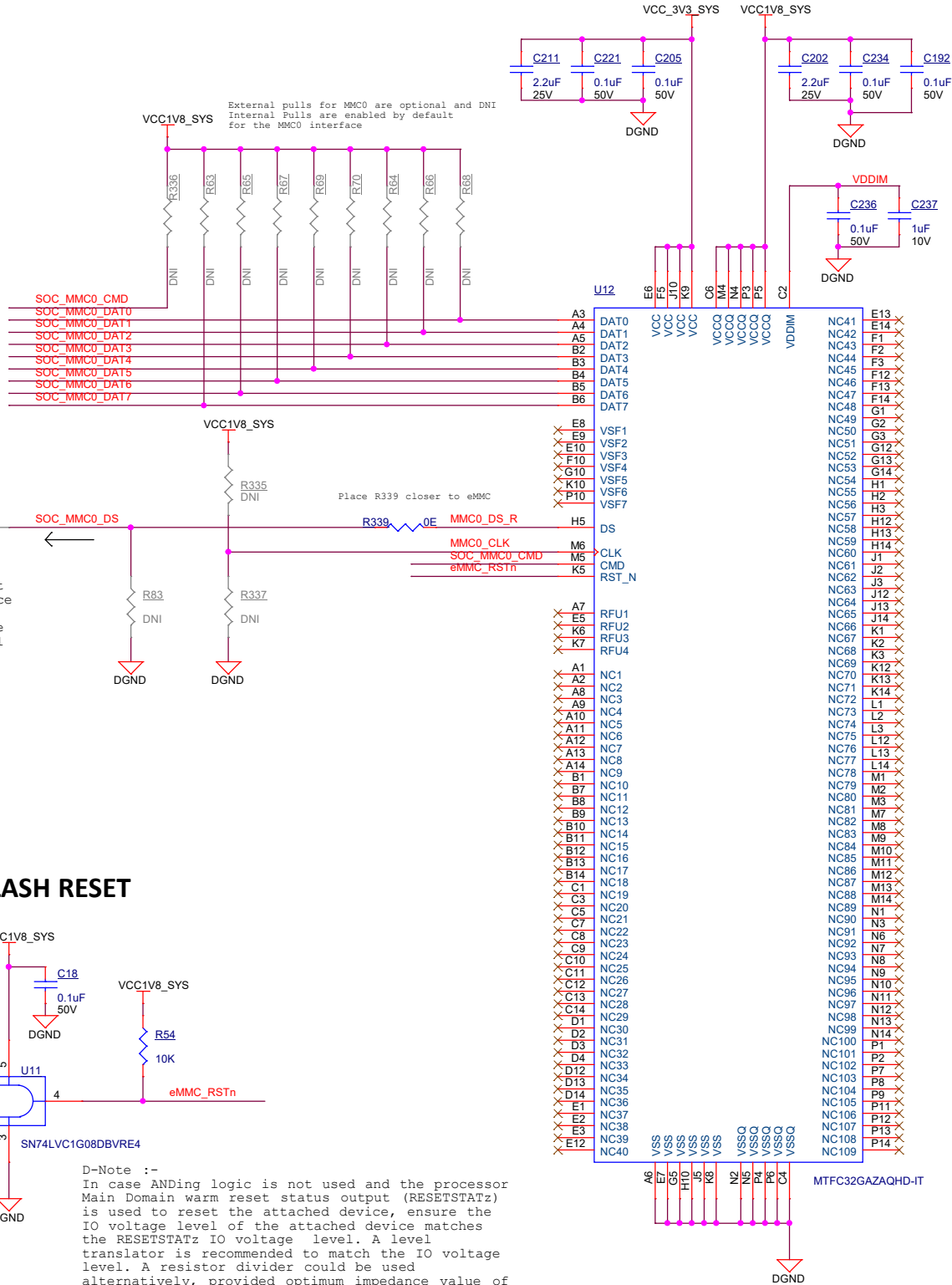
D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level
compatibility before optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and affect SOC operation

D-Note :-
In case ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be slow and introduce too much delay. If too low it will cause the AM62x to source too much steady-state current during normal operation.

eMMC FLASH RESET



eMMC FLASH



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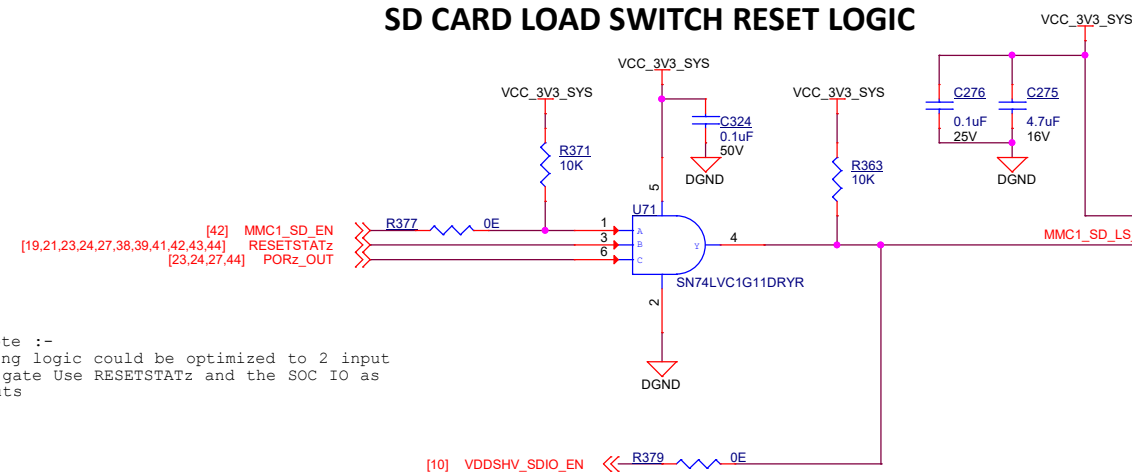


Title eMMC FLASH INTERFACE

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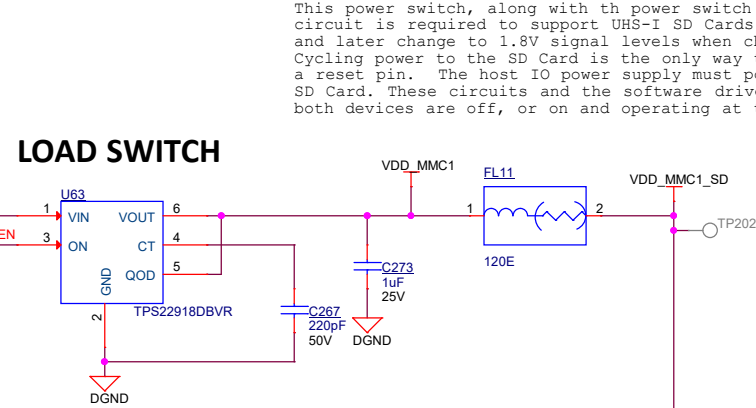
SD CARD INTERFACE

SD CARD LOAD SWITCH RESET LOGIC



D-Note :-
ANDing logic could be optimized to 2 input
AND gate Use RESETSTATz and the SOC IO as
inputs

LOAD SWITCH

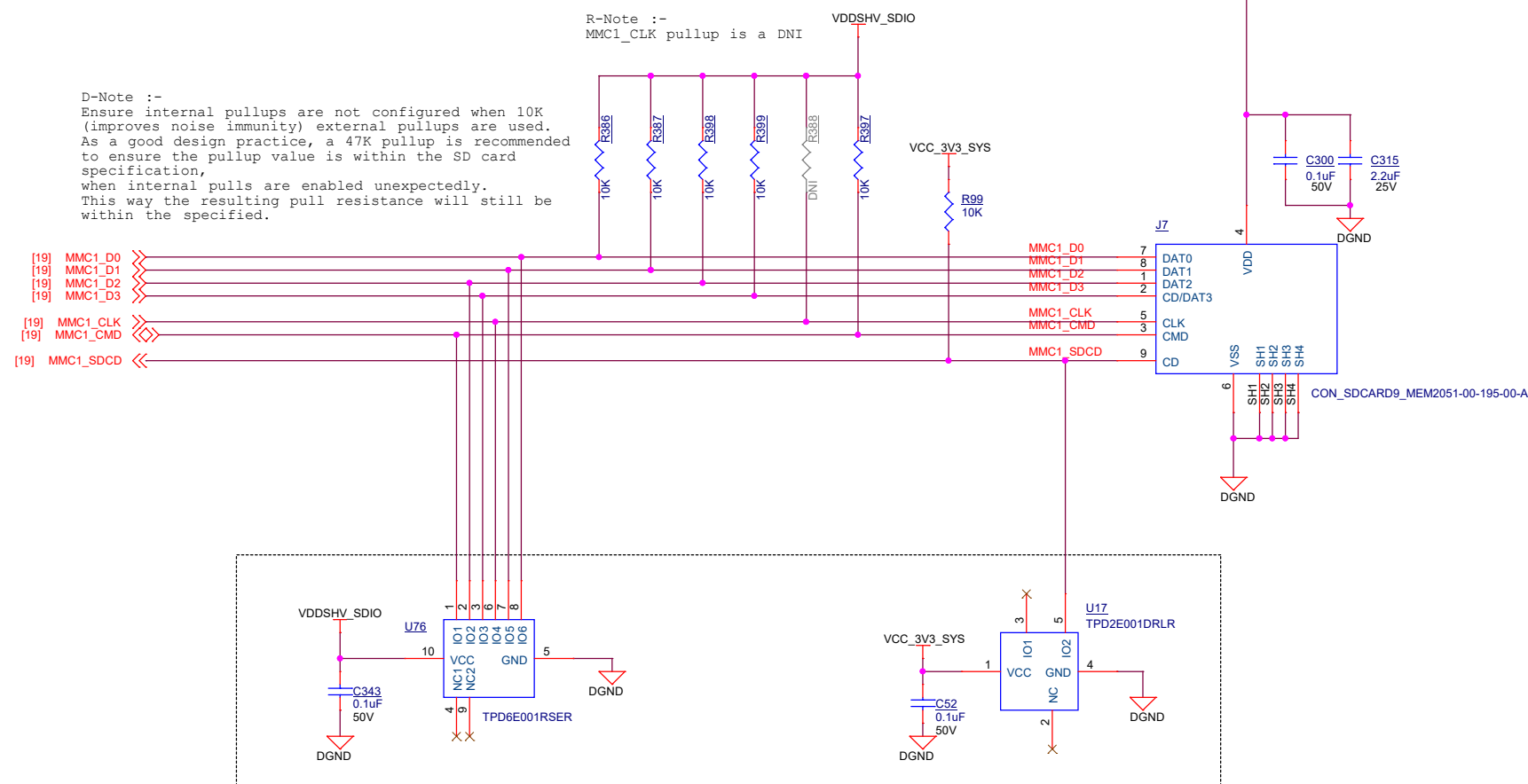


D-Note :-
This power switch, along with the power switch supply reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begin communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds. Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

D-Note :-
For UHS-I operation, the pullups
are recommended to be connected to
the 3.3V/1.8V switched LDO output

R-Note :-
MMC1_CLK pullup is a DNI

D-Note :-
Ensure internal pullups are not configured when 10K (improves noise immunity) external pullups are used. As a good design practice, a 47K pullup is recommended to ensure the pullup value is within the SD card specification, when internal pulls are enabled unexpectedly. This way the resulting pull resistance will still be within the specified.



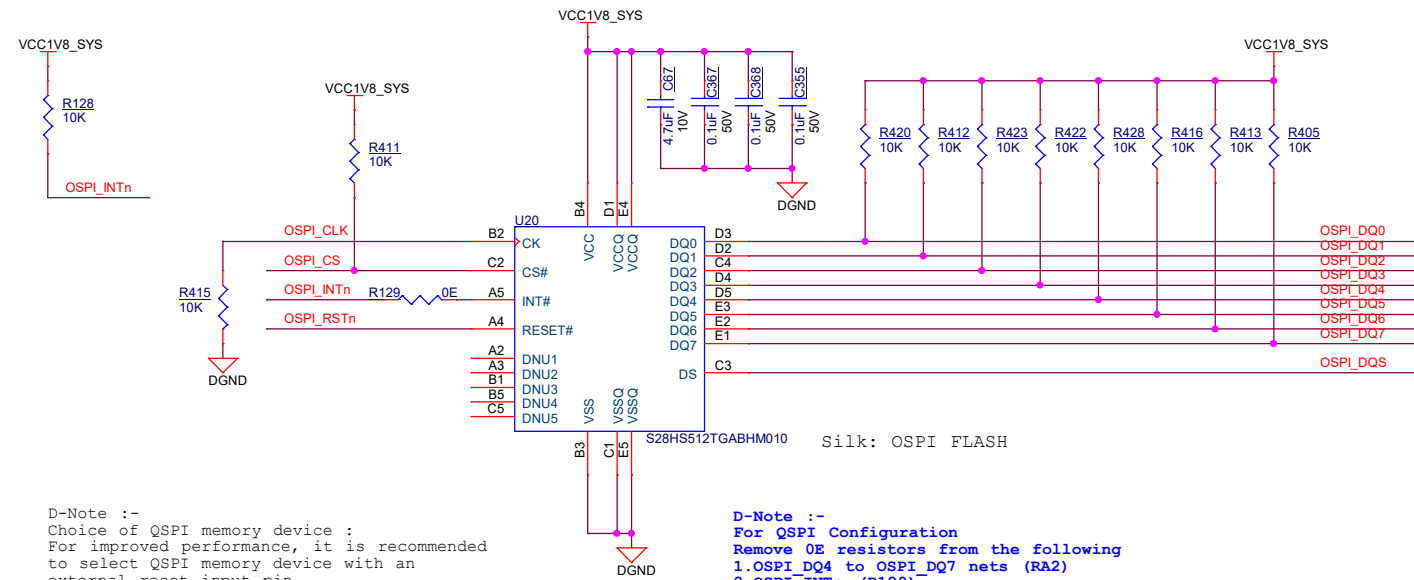
D-Note :-
Place near to SD Card Connector



R-Note :-
These 0 0 resistors are used for configuring QSPI and OSPI
This is optional during custom board design

R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state.
Use of Pullups are attached device dependent

OSPI FLASH



D-Note :-
Choice of QSPI memory device :
For improved performance, it is recommended to select QSPI memory device with an external reset input pin
The reset pin is recommended to be controlled using SOC reset status output or an ANDING logic as implemented in the starter kit

D-Note :-
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA2)
2.OSPI_INTN (R129)
OSPI NOR Flash can be replaced with the Footprint
compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

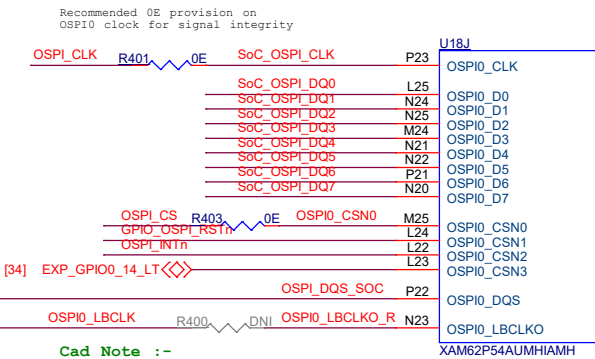
Place RA3 & RA2 closer to Memory



These series resistors are for enabling OSPI and QSPI
These are specific to SK and optional if the interface is fixed

D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported

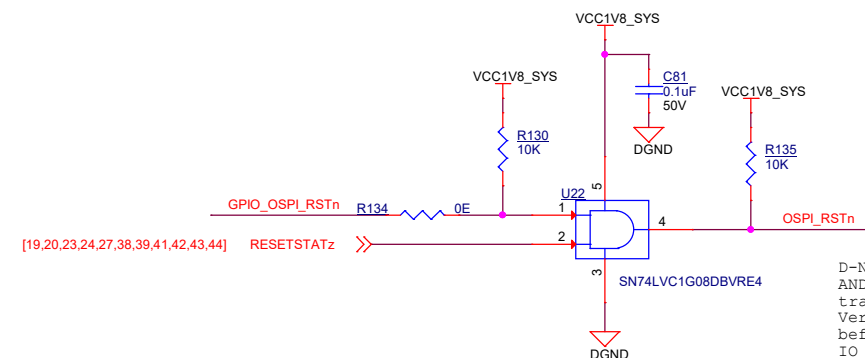
SOC OSPI INTERFACE



Cad Note :-
Place R400 close to the SOC Ball
with as little trace as possible

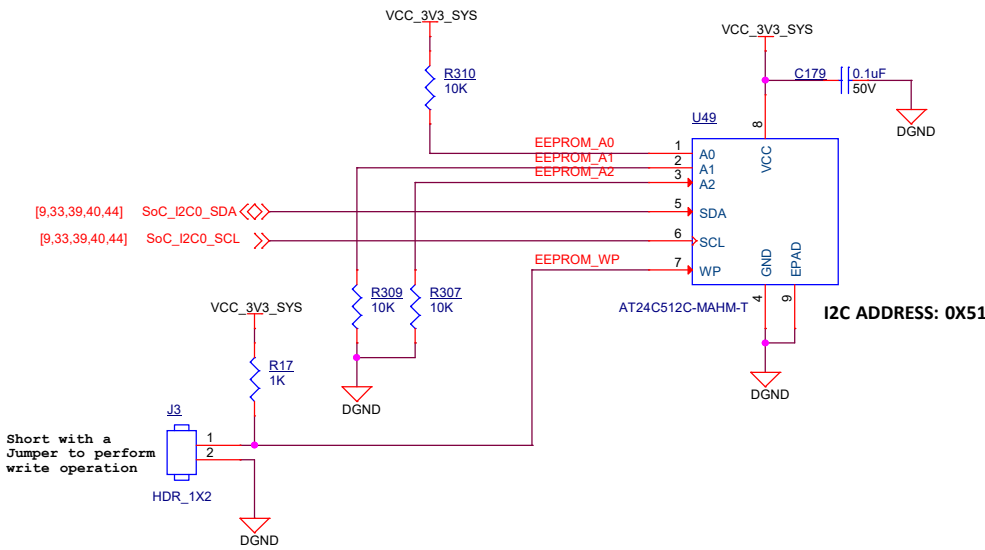
D-Note :-
External loopback clock OSPI0_LBCLK series resistors
(R400 and R421) are DNI when _DQS is connected

OSPI FLASH RESET

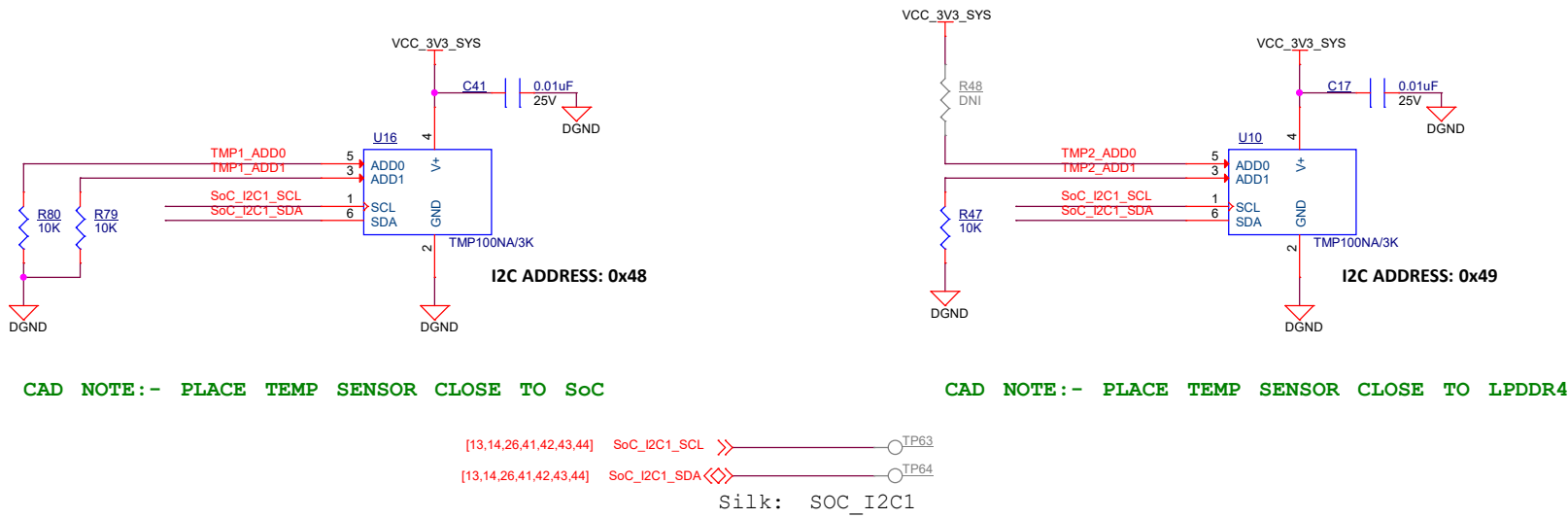


D-Note :-
ANDING logic additionally performs level translation
Verify the Reset IO level compatibility
before optimizing the reset ANDING logic.
IO level mismatch could cause supply
leakage and affect SOC operation

BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



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Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size C PROC164E1-1

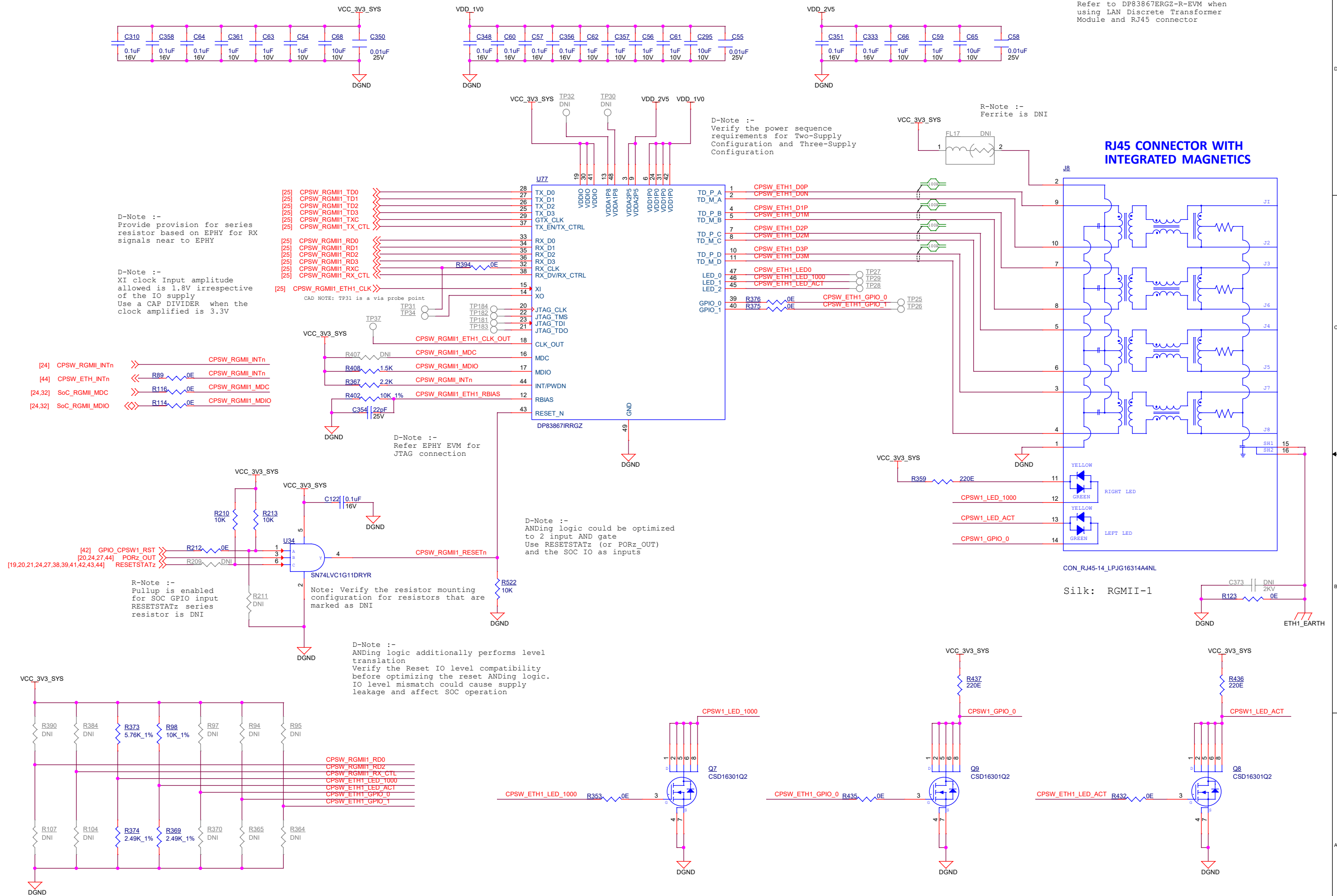
Rev E1-1

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D-Note :-
The caps and values used are as per the EPHY data sheet recommendations.

CPSW3G RGMII 1 - PHY

D-Note :-
Refer to DP83867ERG2-R-EVM when
using LAN Discrete Transformer
Module and RJ45 connector



PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

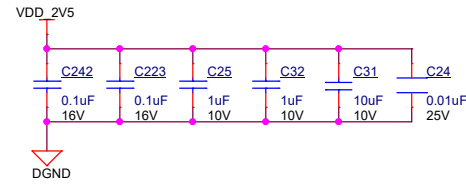
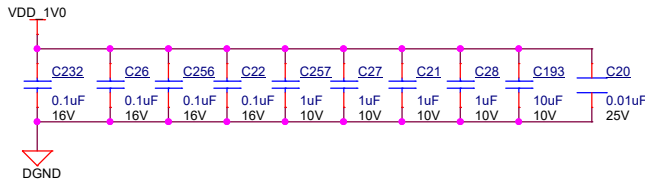
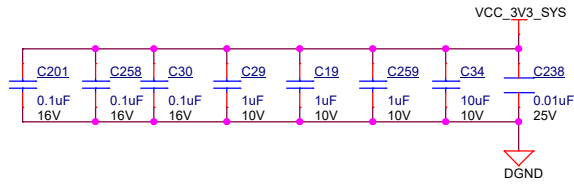
Designed for TI by Mistral Solutions Pvt Ltd



Title					CPSW3G RGMII 1 - PHY					
Size		PROC164E1-1				Rev				
C						E1-1				
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CPSW3G RGMII 2 - PHY

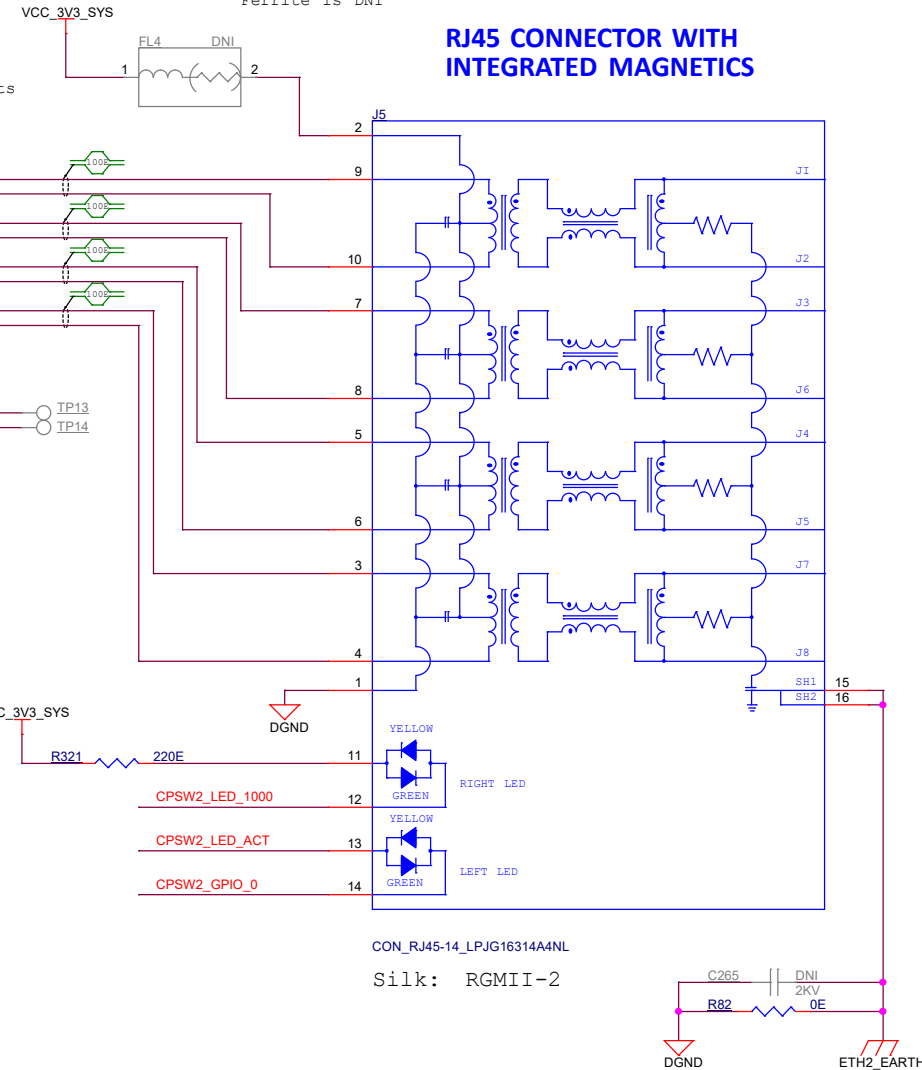
D-Note :-
The caps and values used are
as per the EPHY data sheet
recommendations.



D-Note :-
Refer to DP83867ERGZ-R-EVM when
using LAN Discrete Transformer
Module and RJ45 connector

R-Note :-
Ferrite is DNI

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS



D-Note :-
Provide provision for series
resistor based on EPHY for RX
signals near to EPHY

D-Note :-
XI clock Input amplitude
allowed is 1.8V irrespective
of the IO supply
Use a CAP DIVIDER when the
clock amplified is 3.3V

- [25] CPSW_RGMII2_TD0
- [25] CPSW_RGMII2_TD1
- [25] CPSW_RGMII2_TD2
- [25] CPSW_RGMII2_TD3
- [25] CPSW_RGMII2_TXC
- [25] CPSW_RGMII2_TX_CTL
- [25] CPSW_RGMII2_RD0
- [25] CPSW_RGMII2_RD1
- [25] CPSW_RGMII2_RD2
- [25] CPSW_RGMII2_RD3
- [25] CPSW_RGMII2_RXC
- [25] CPSW_RGMII2_RX_CTL
- [25] CPSW_RGMII2_ETH2_CLK

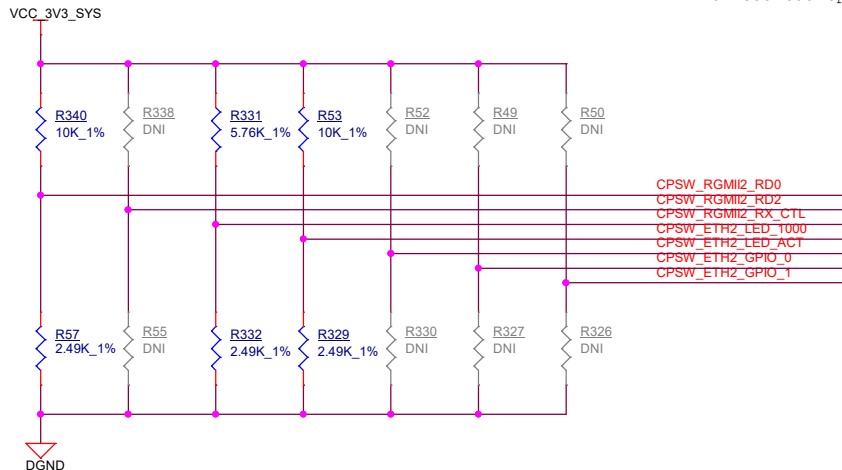
CAD NOTE: TP19 is a via probe point

D-Note :-
Refer EPHY EVM
for JTAG
connection

D-Note :-
ANDing logic could be optimized
to 2 input AND gate
Use RESETSTATz (or PORz OUT)
and the SOC IO as inputs

R-Note :-
Pullup is enabled
for SOC GPIO input
RESETSTATz series
resistor is DNI

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic.
IO level mismatch could cause supply leakage and
affect SOC operation



- CPSW_RGMII2_RD0
- CPSW_RGMII2_RD2
- CPSW_RGMII2_RX_CTL
- CPSW_ETH2_LED1000
- CPSW_ETH2_LED_ACT
- CPSW_ETH2_GPIO_0
- CPSW_ETH2_GPIO_1

PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

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Title CPSW3G RGMII 2 - PHY

Size PROC164E1-1

Date: Wednesday, June 05, 2024

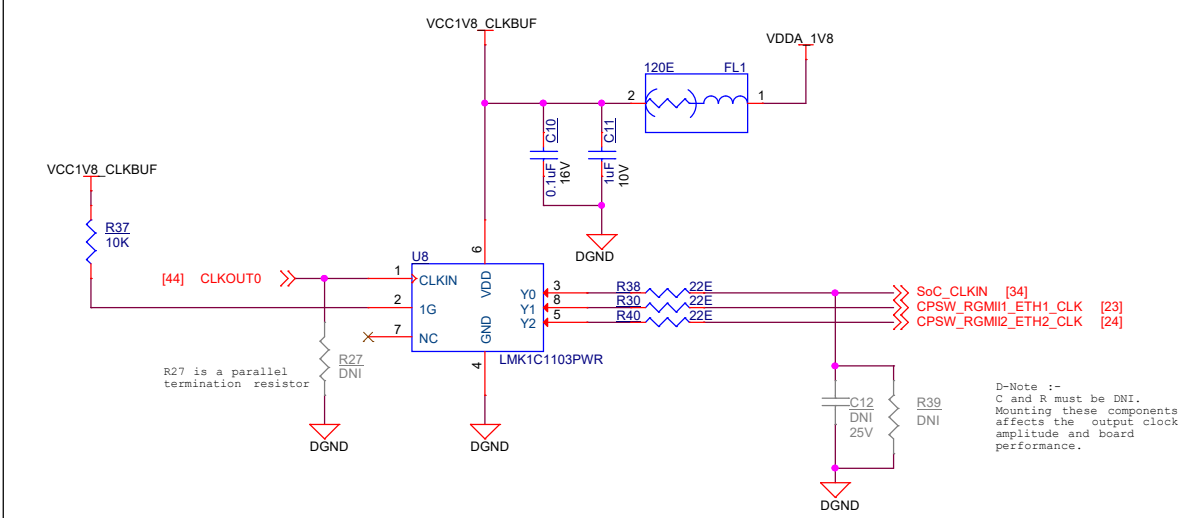
Sheet 24 of 47

Rev E1-1

SOC CPSW3G ETHERNET INTERFACE



SOC & ETHERNET PHY CLOCK BUFFER

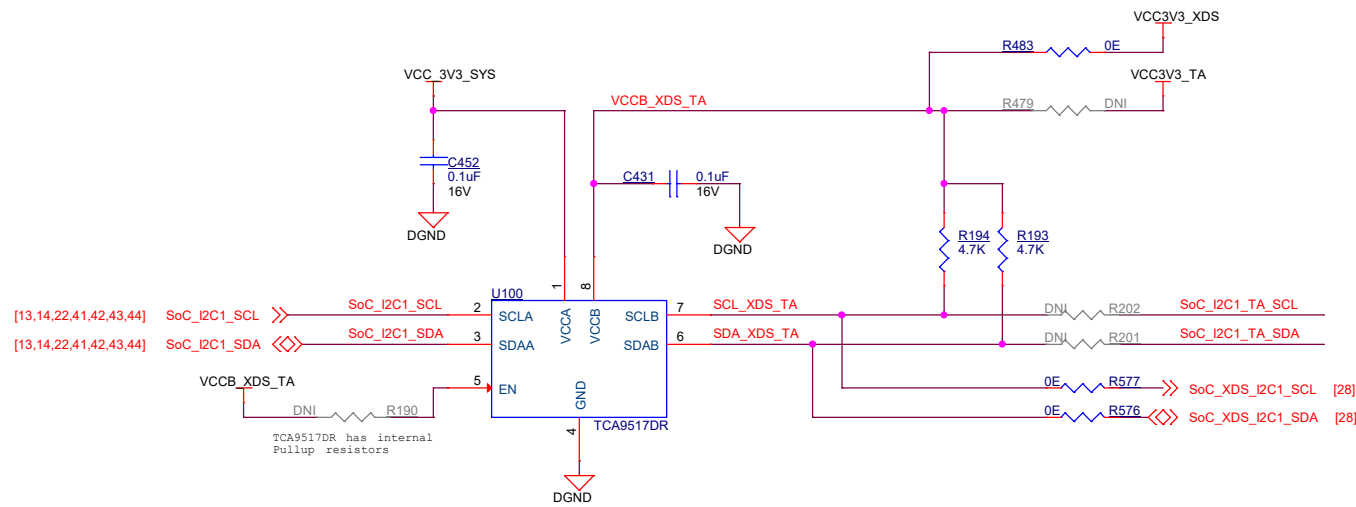


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Title		ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size	PROC164E1-1		Rev
C			E1-1
Date:	Wednesday, June 05, 2024	Sheet	25 of 47

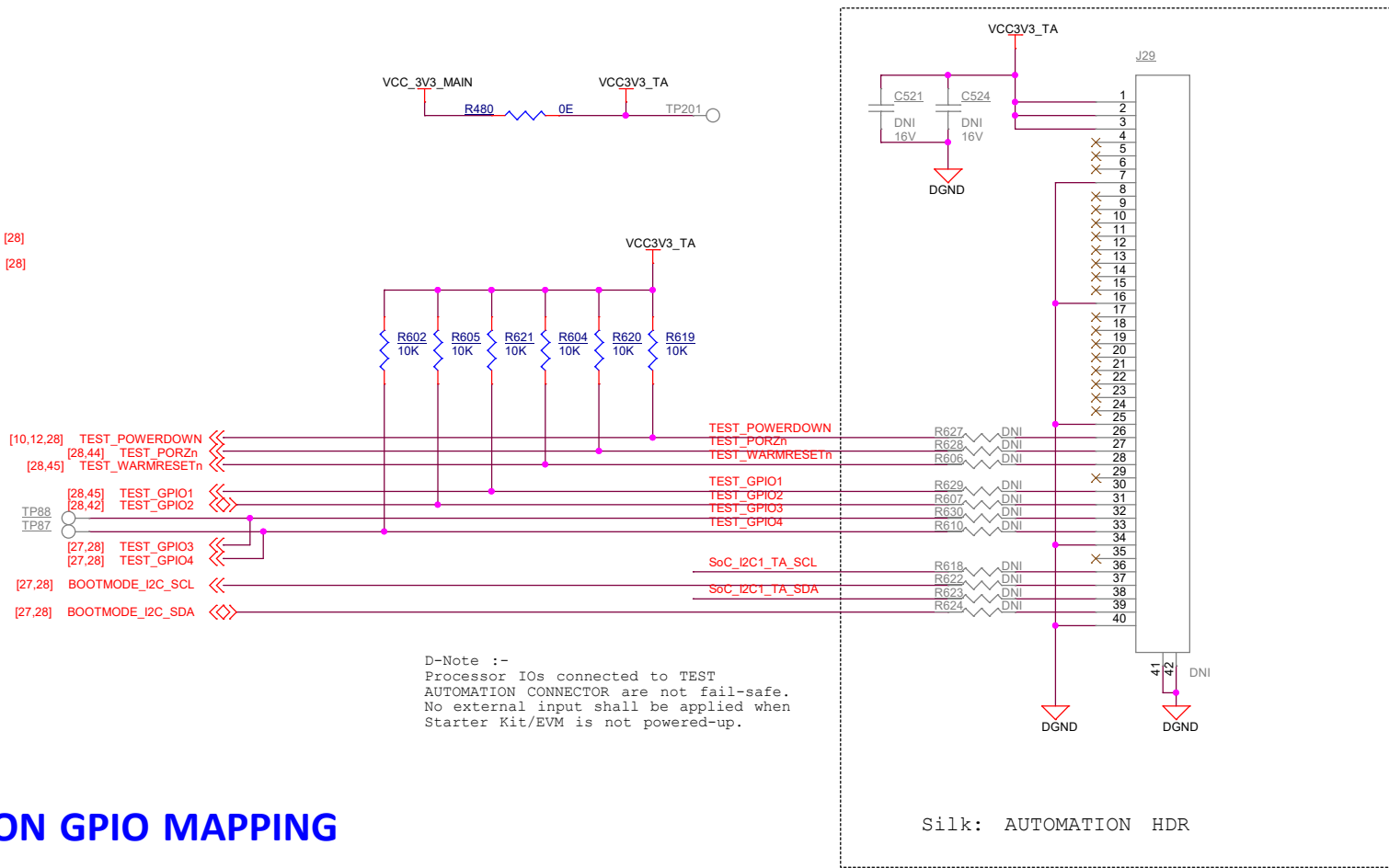
I2C BUS BUFFER



TA Header Configuration

Mount : R201, R202, R479
Demount: R483, R576, R577

40-PIN TEST AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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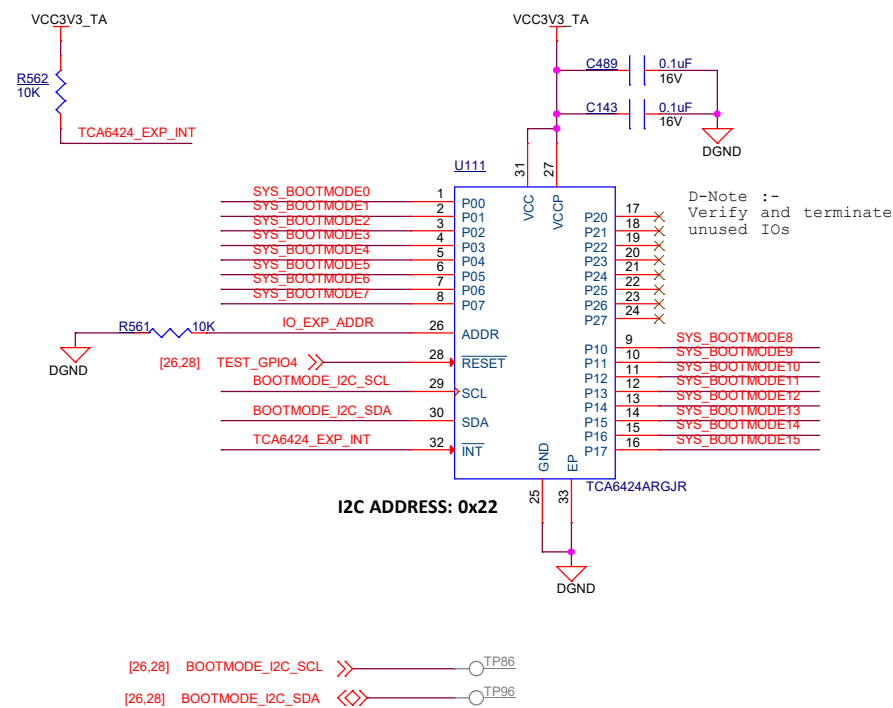
Title TEST AUTOMATION

Size PROC164E1-1

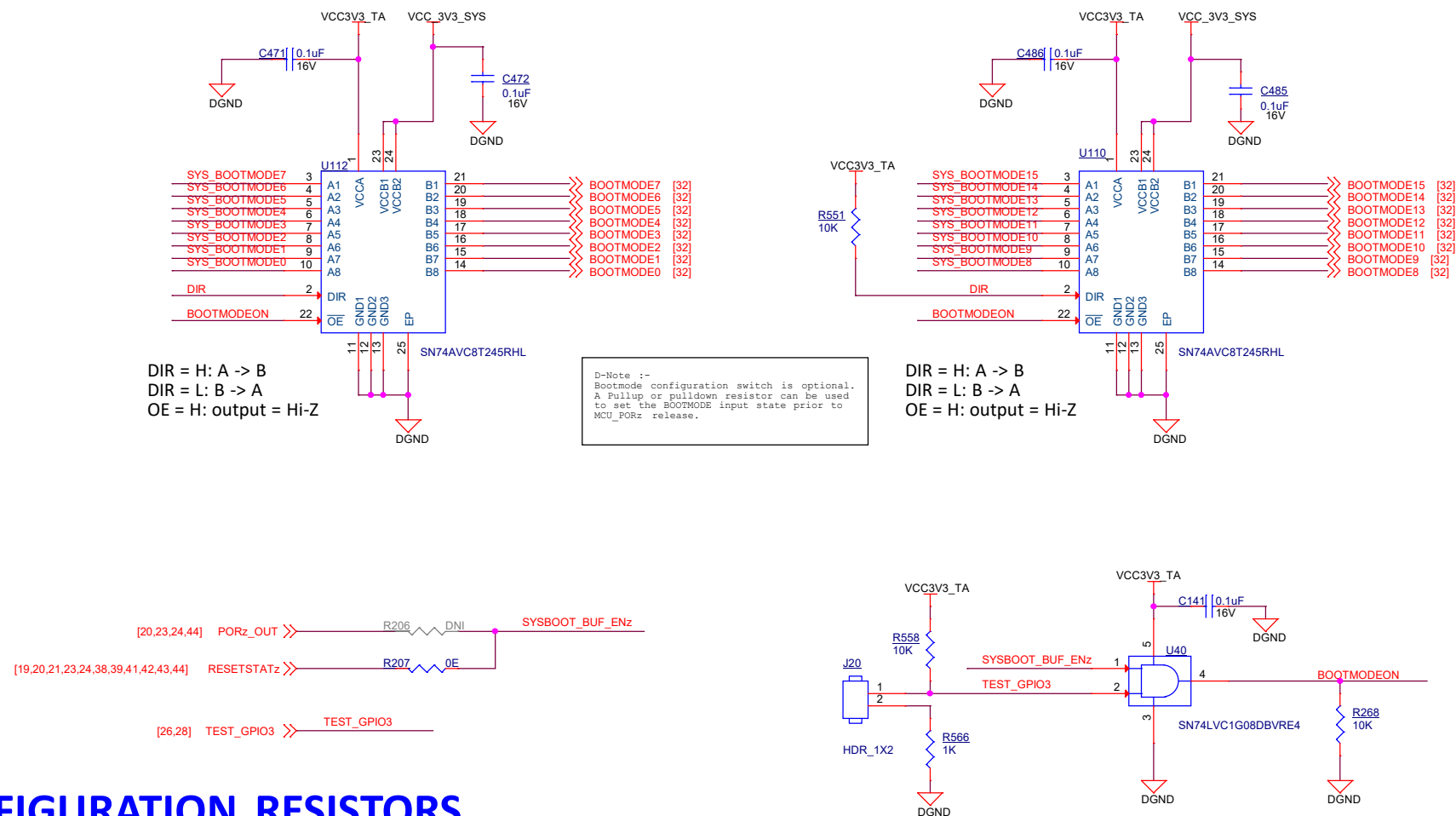
Date: Wednesday, June 05, 2024 Sheet 26 of 47

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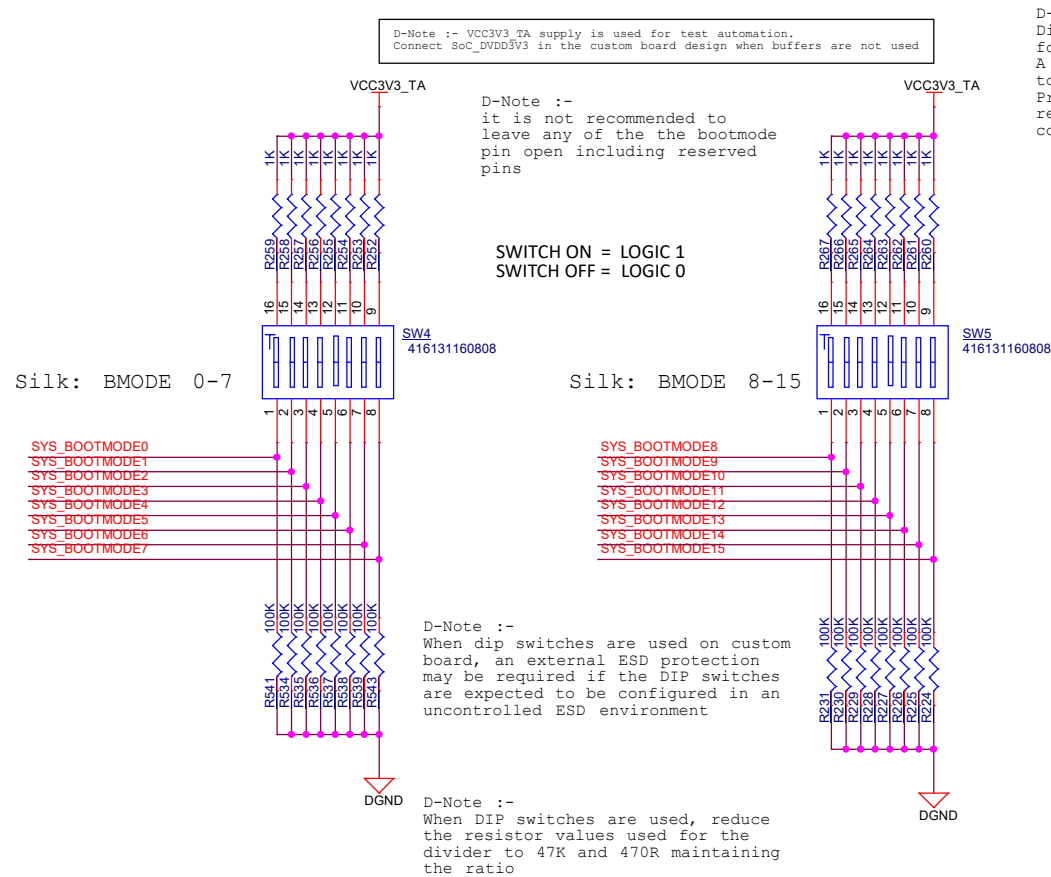
BOOTMODE IO EXPANDER



BOOT MODE BUFFERS



BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

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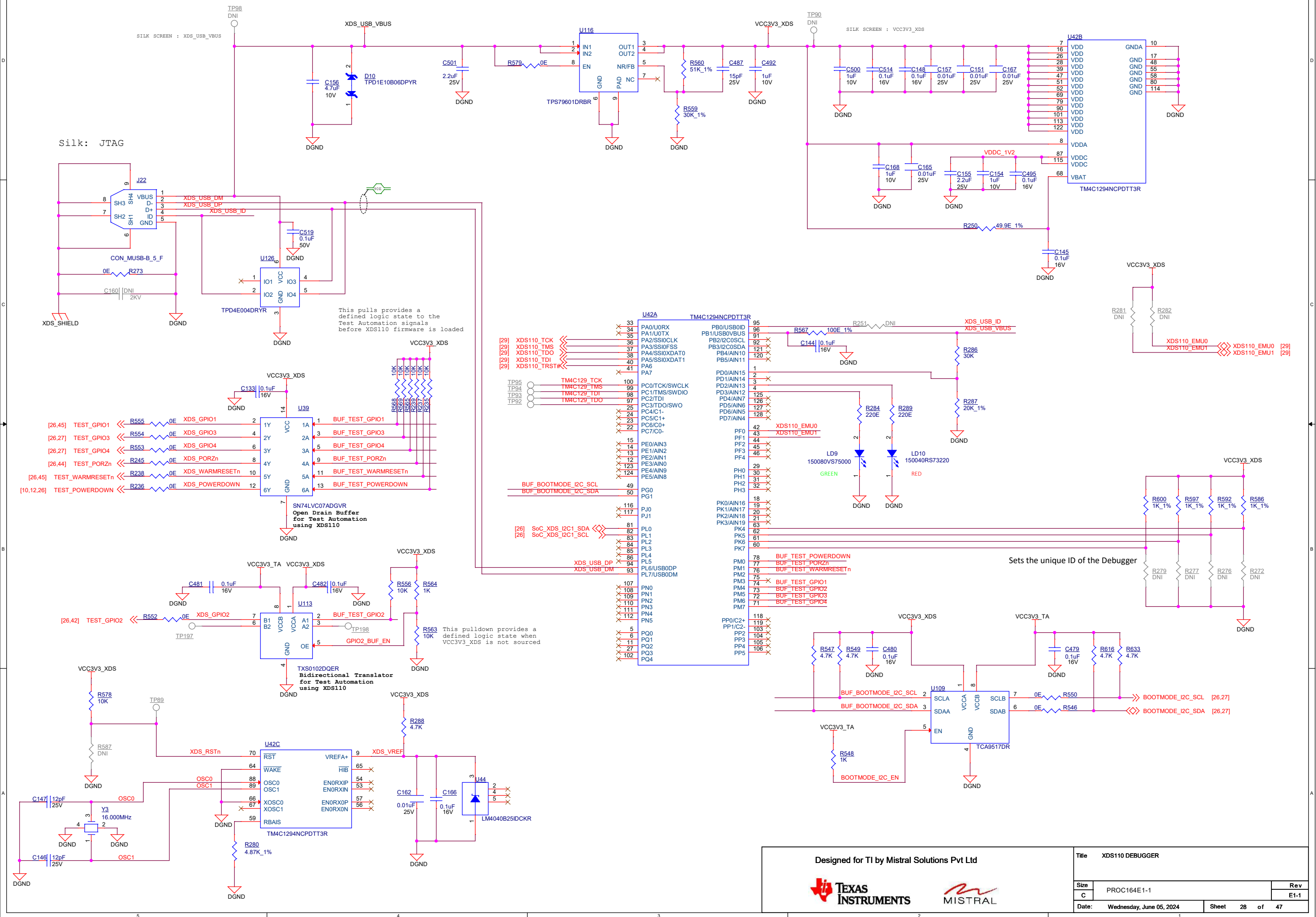
Title BOOT MODE BUFFER & SWITCHES

Size
C PROC164E1-1

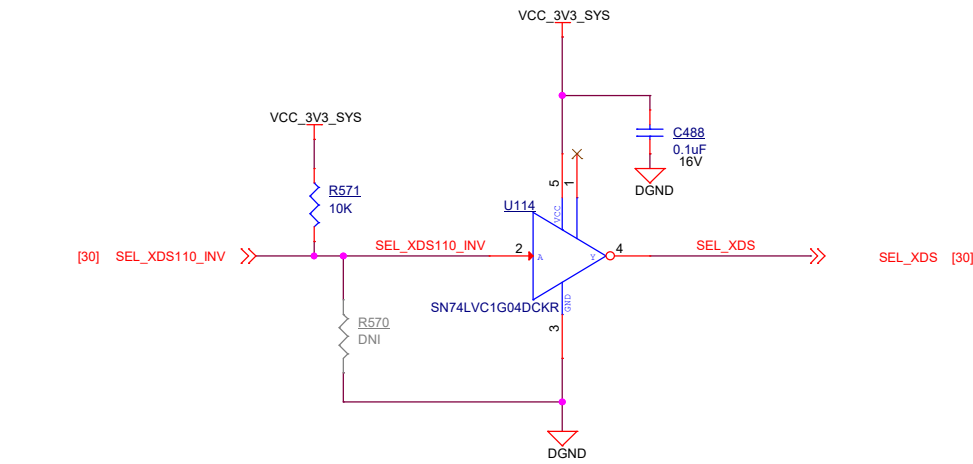
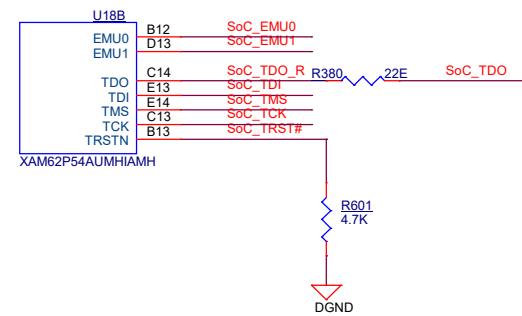
Date: Wednesday, June 05, 2024 Sheet 27 of 47

Rev
E1-1

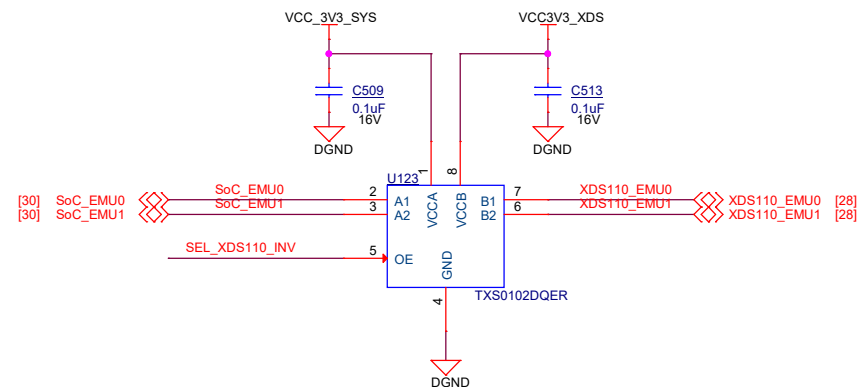
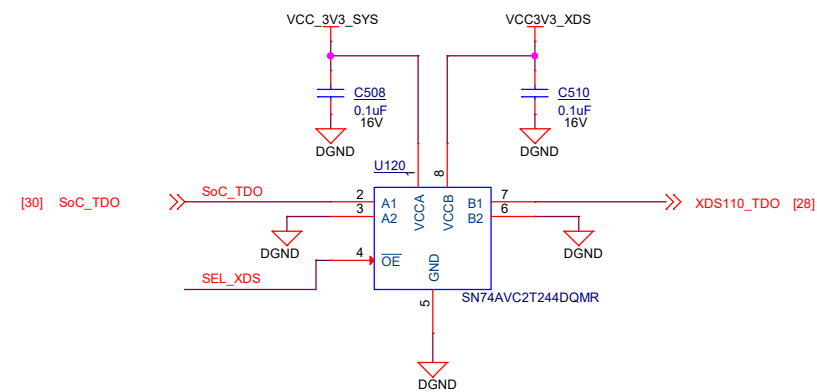
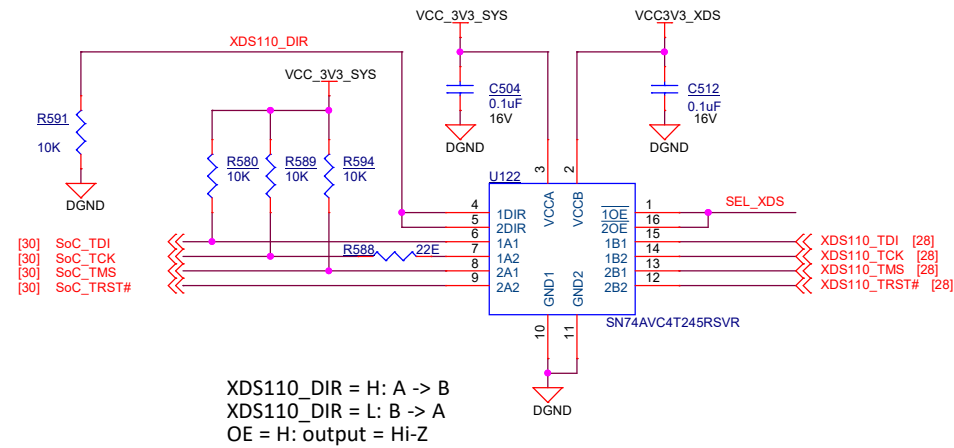
XDS110 DEBUGGER



JTAG SOC SECTION



BUFFER XDS110



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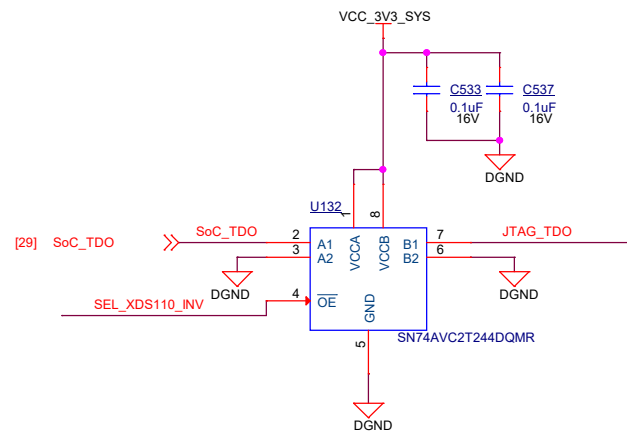
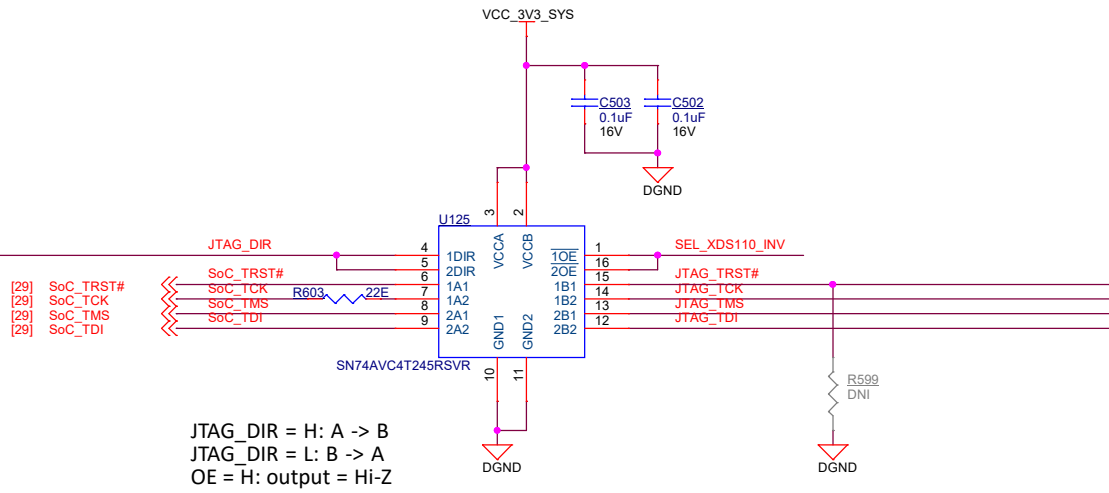
Title JTAG BUFFER

Size PROC164E1-1
C

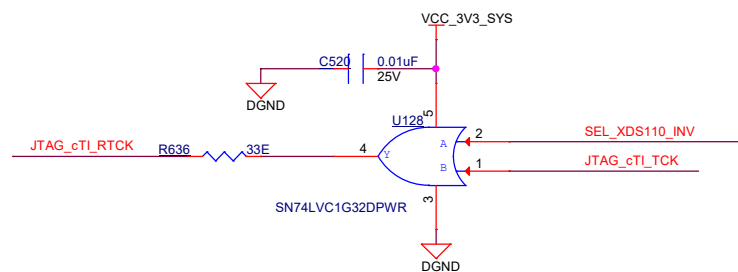
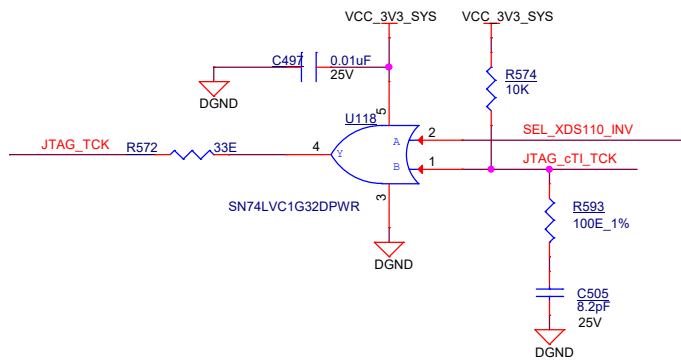
Date: Wednesday, June 05, 2024 Sheet 29 of 47

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cTI20 JTAG BUFFERS

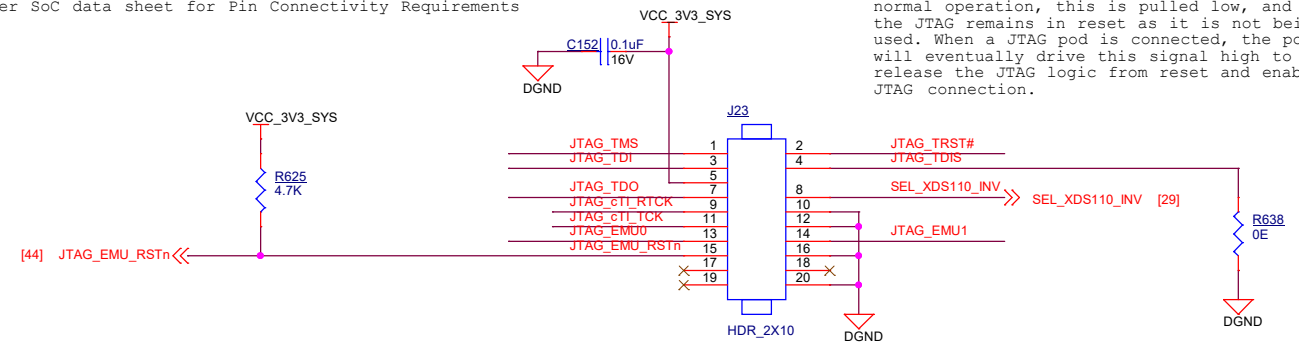


JTAG CLOCK BUFFER



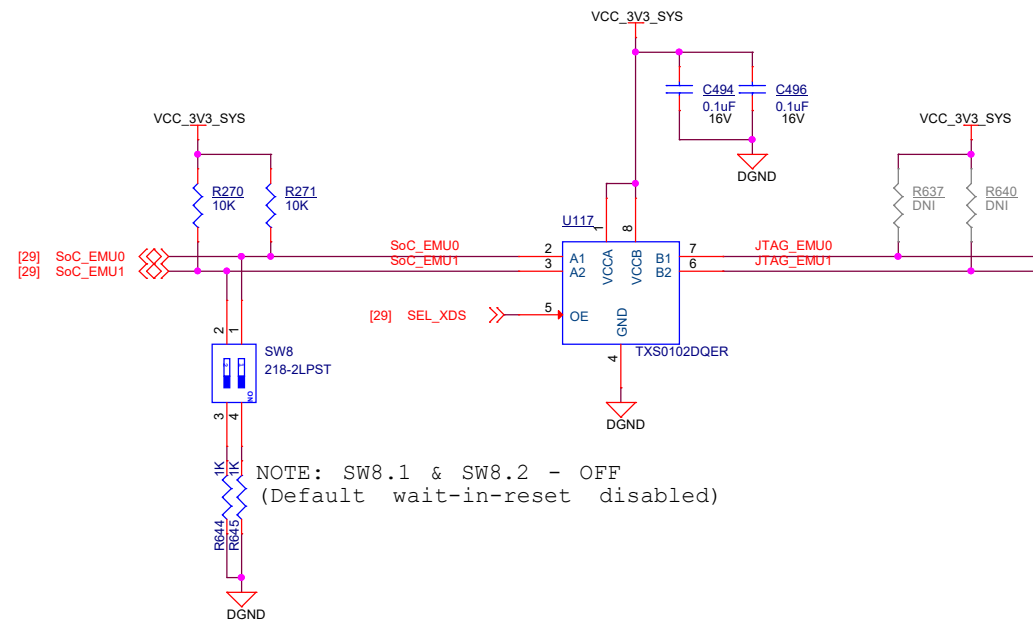
JTAG 20 PIN cTI CONNECTOR

D-Note :-
Place pulls on the JTAG signals near to the SoC
Refer SoC data sheet for Pin Connectivity Requirements



Silk: cTI

```
D-Note :-
Add an external ESD protection to provide
system level ESD protection when external connector is
used for debug. Follow the connectivity table for connecting
the required pulls for the SOC JTAG interface
Add Test points, and external ESD protection when JTAG
connector is not used
```



NOTE: SW8.1 & SW8.2 - OFF
(Default wait-in-reset disabled)

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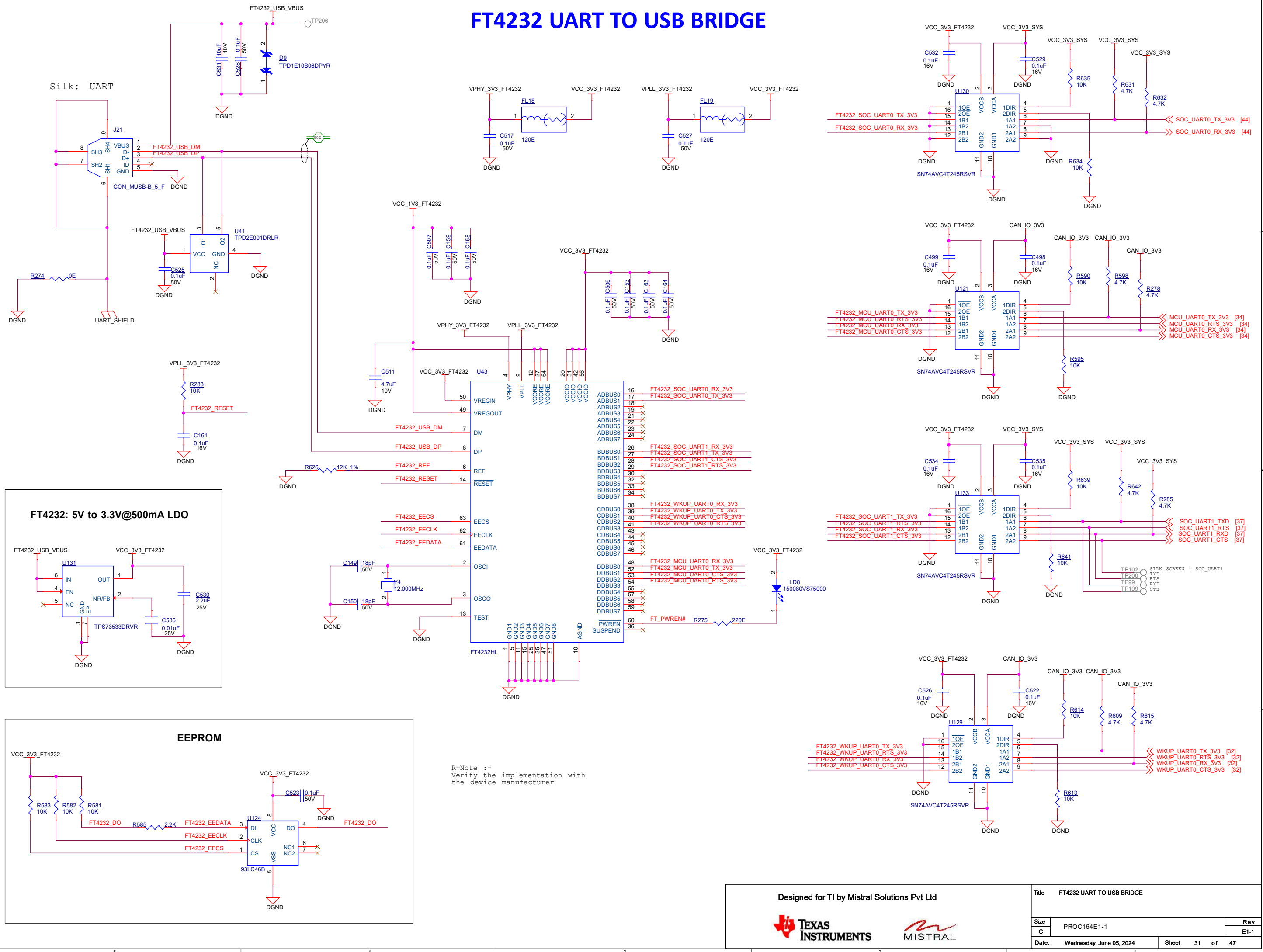
Title	JTAG 20 PIN cTI CONNECTOR
-------	---------------------------

Size	PROC164E1-1
C	

Date:	Wednesday, June 05, 2024	Sheet	30	of	47
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Rev
E1.1

FT4232 UART TO USB BRIDGE



R-Note :-
Verify the implementation with
the device manufacturer

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Title FT4232 UART TO USB BRIDGE

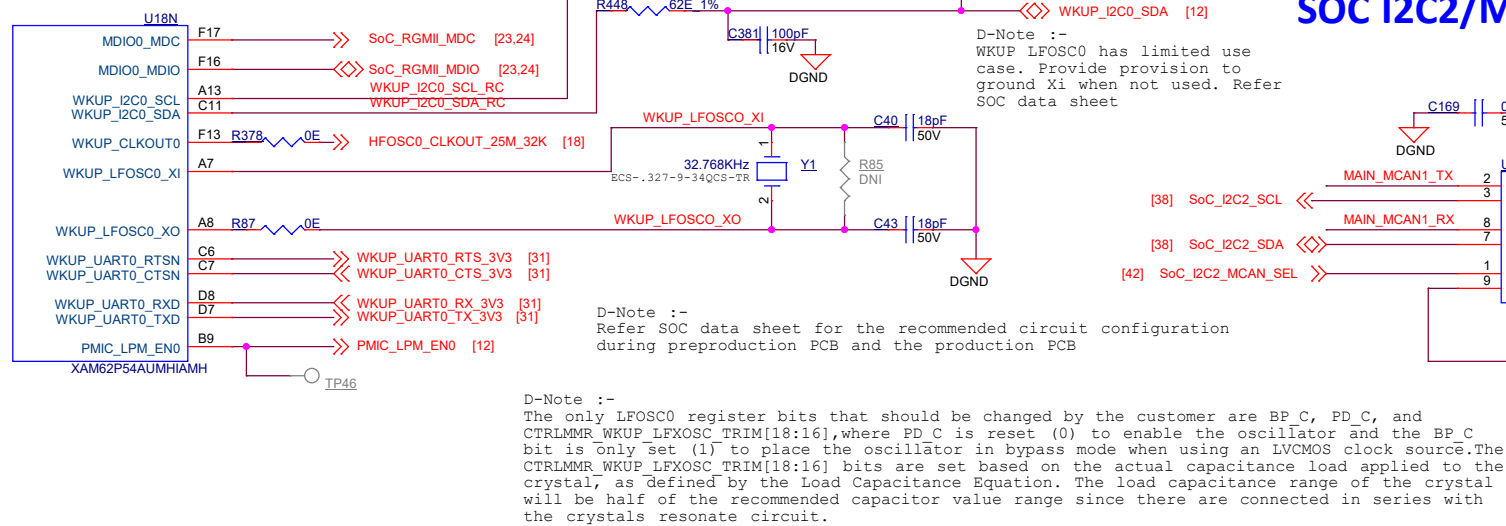
Size PROC164E1-1

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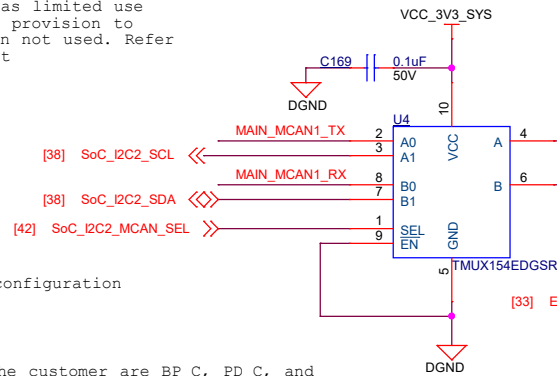
Rev E1-1

SOC GPMC INTERFACE

SOC WKUP DOMAIN

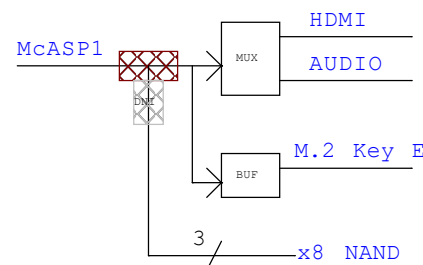
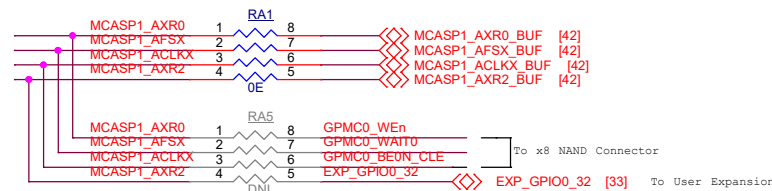
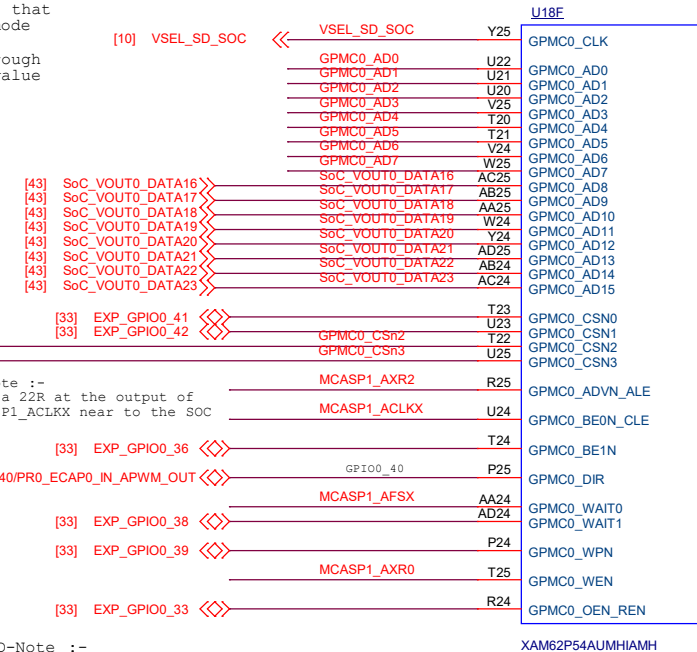


SOC I2C2/MCAN1 MUX

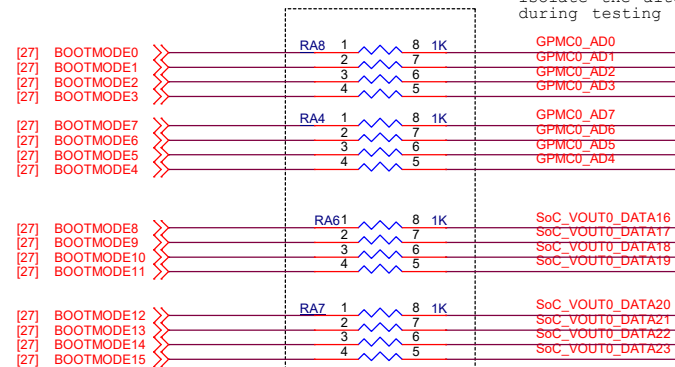


D-Note :-

Add a series resistor 0R when used as GPMC0_Clk



BOOTMODE PINS



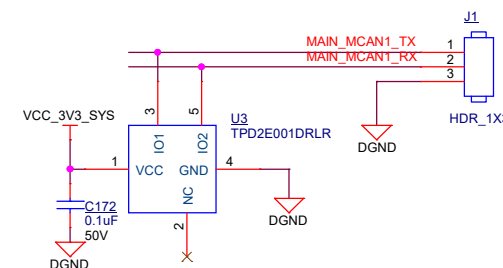
D-Note :-

Resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions

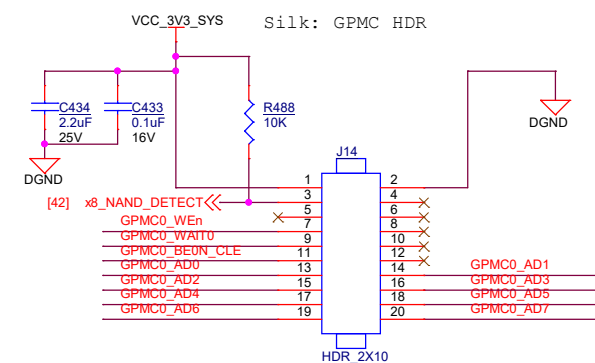
D-Note :-

When bootmode Isolation buffers are not used, connect the bootmode configuration resistors directly to the SOC bootmode input pins. Connect the SOC bootmode signal used for alternate function to the attached device through 0R for isolation or testing.

MCAN1 HEADER



GPMC HEADER



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Title SOC WKUP & GPMC

Size PROC164E1-1

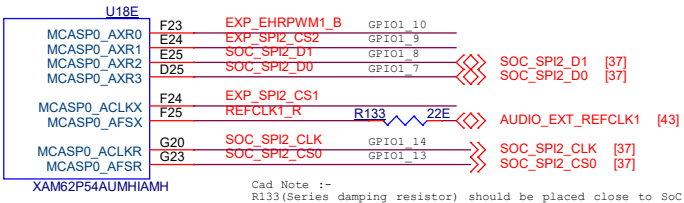
Date: Wednesday, June 05, 2024

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D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

USER EXPANSION CONNECTOR



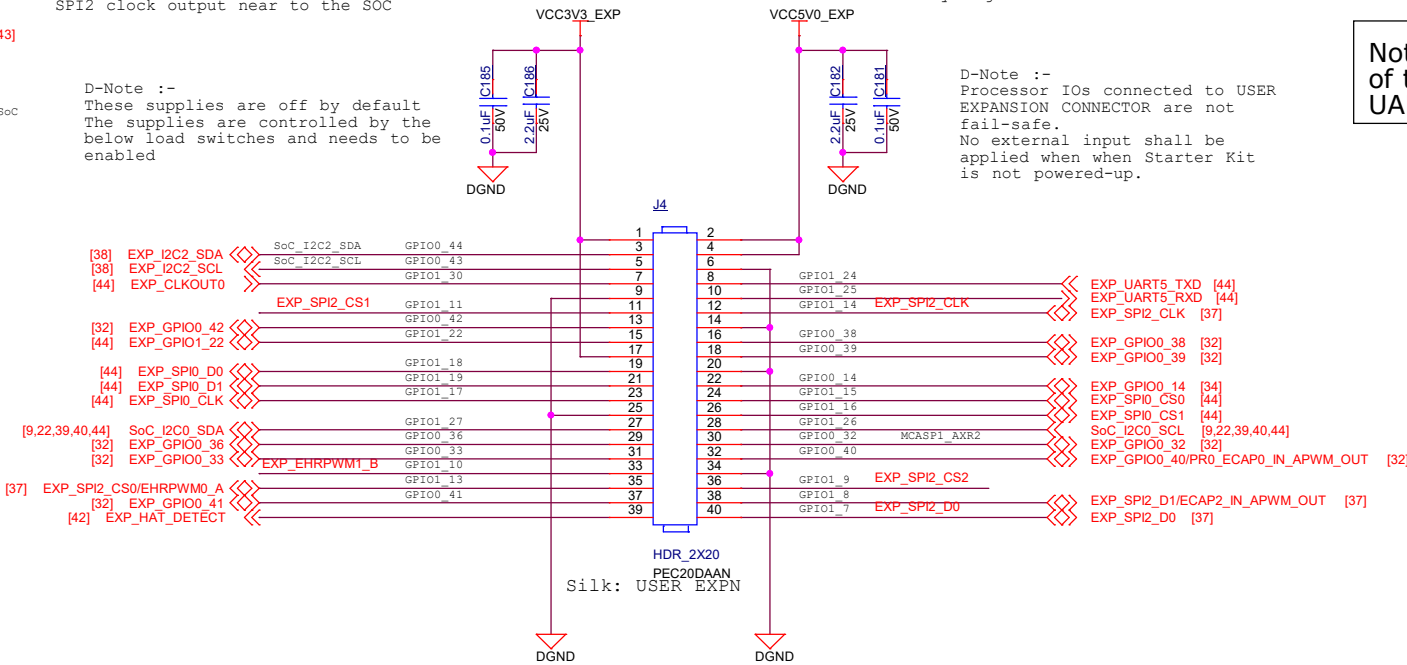
D-Note :-
Add a series resistor 22 0 for the SPI2 clock output near to the SOC

D-Note :-
These supplies are off by default
The supplies are controlled by the below load switches and needs to be enabled

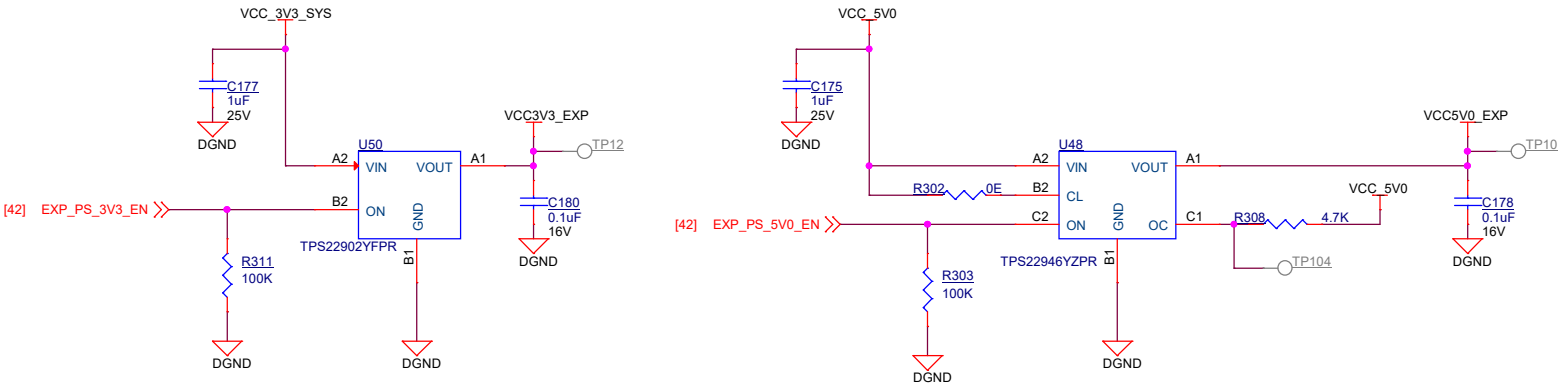
D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull.
When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note :-
Processor IOs connected to USER EXPANSION CONNECTOR are not fail-safe.
No external input shall be applied when Starter Kit is not powered-up.

Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



D-Note :-

AM62P Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62P Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

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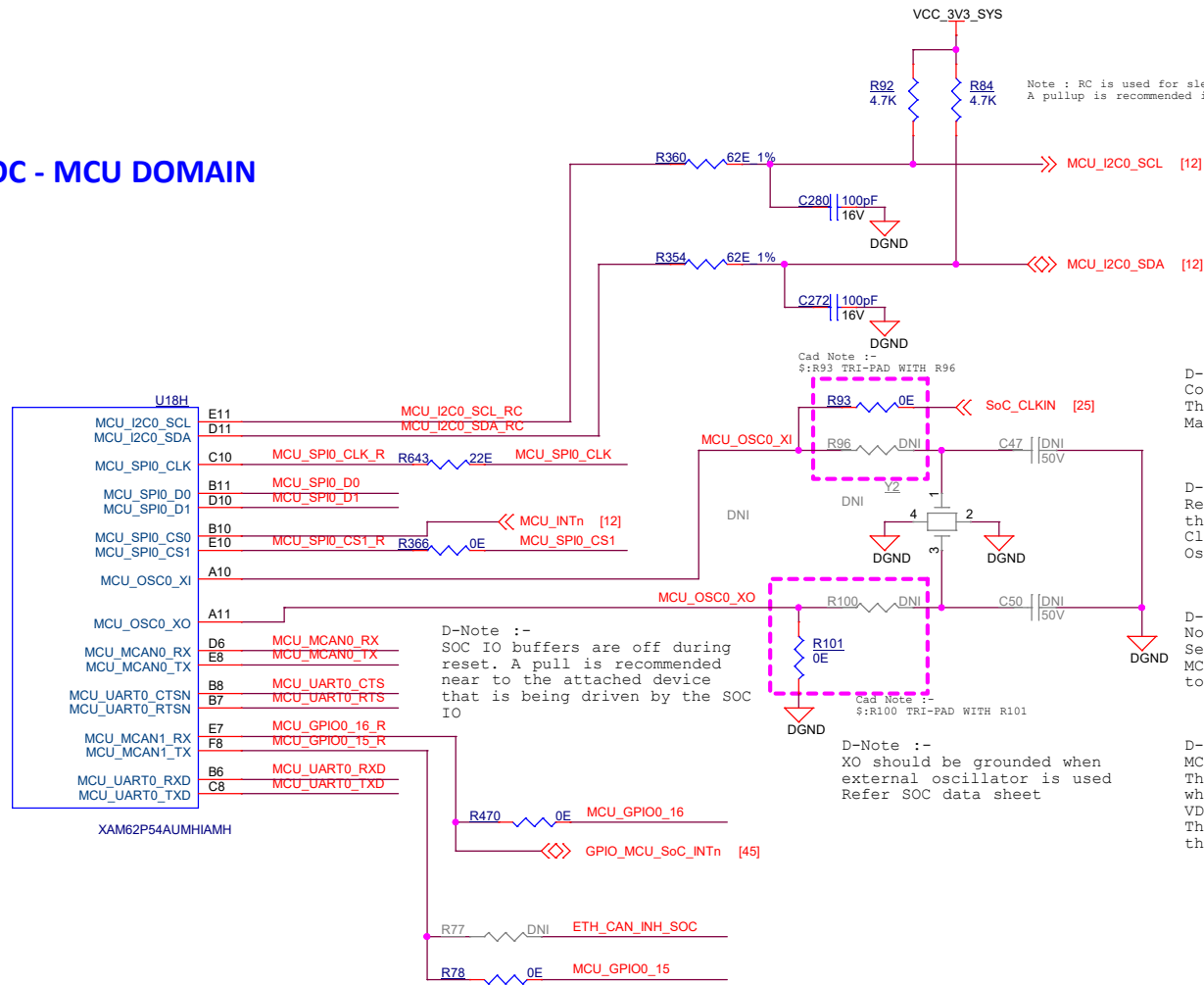
Title USER EXPANSION CONNECTOR

Size C PROC164E1-1

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SOC - MCU DOMAIN



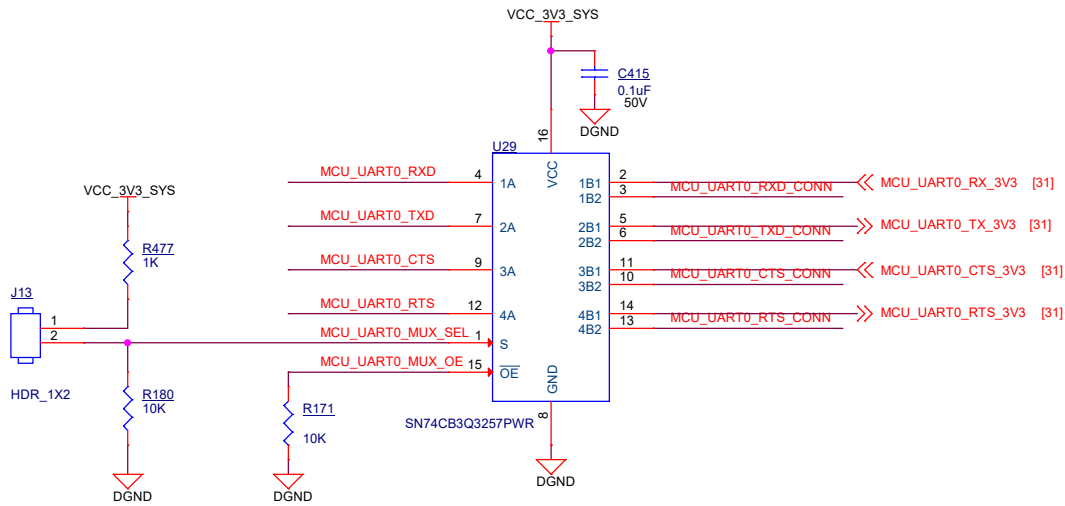
D-Note :-
Connect the 25 Mhz crystal directly to the SOC Xi and Xo pins (No Series or parallel resistors are recommended).
The internal oscillator implements AGC (Automatic Gain Control) for amplitude control
Match the SOC and the EPHY crystal specs

D-Note :-
Refer Applications, Implementation, and Layout section of the data sheet for clock routing guidelines as below:
Clock Routing Guidelines
Oscillator Routing

D-Note :-
No HFOSCO registers are required to be changed. These registers should remain in their default state.
Select the appropriate crystal circuit components that are compliant to the values defined in the MCU_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

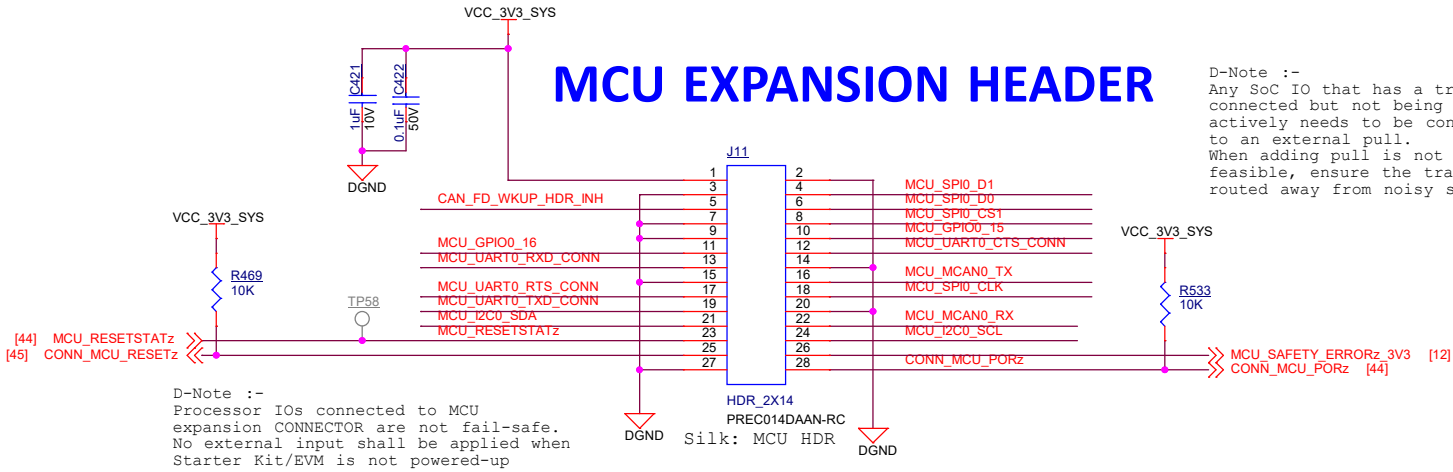
D-Note :-
MCU_OSC0 has been validated only with a 25 Mhz clock source, so that is the only frequency supported.
The datasheet shows MCU_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD CORE is valid. In most cases it will start as early as VDD8 OSC0, but this may not always be the case.
This diagram in the datasheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

SoC MCU UART0 FET BUS SWITCH

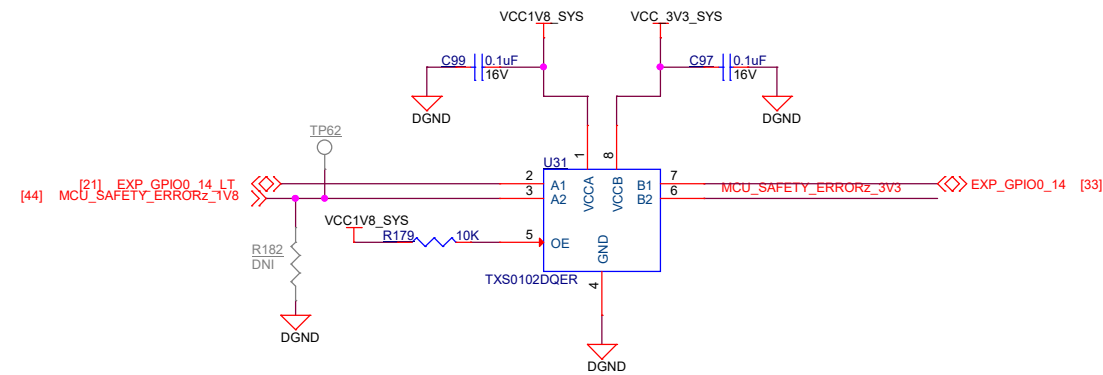


OEn	SEL	INPUT/OUTPUT	
		An=nB1	An
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

MCU EXPANSION HEADER



D-Note :-
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull.
When adding pull is not feasible, ensure the traces are routed away from noisy signals



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Title MCU HEADER

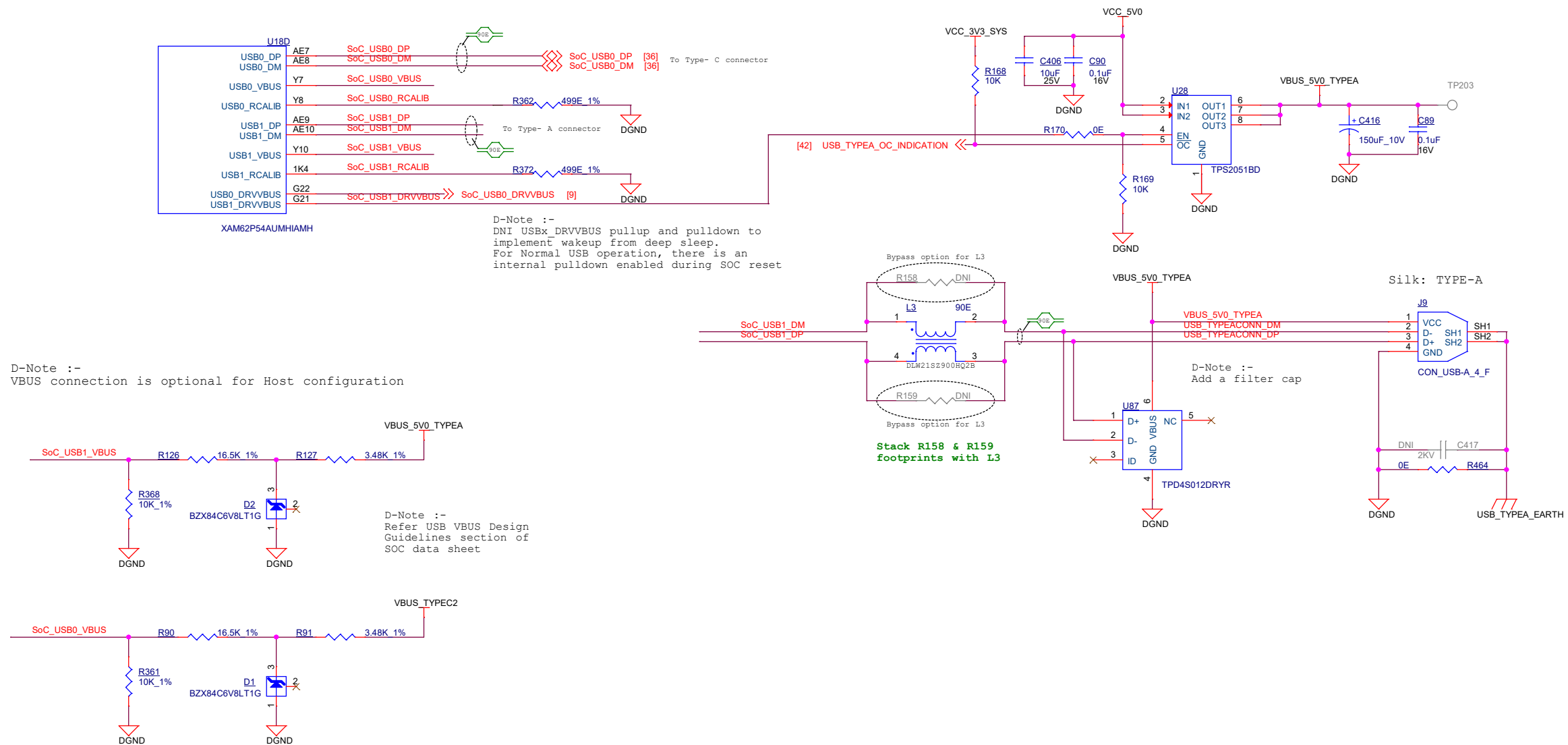
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Date: Wednesday, June 05, 2024

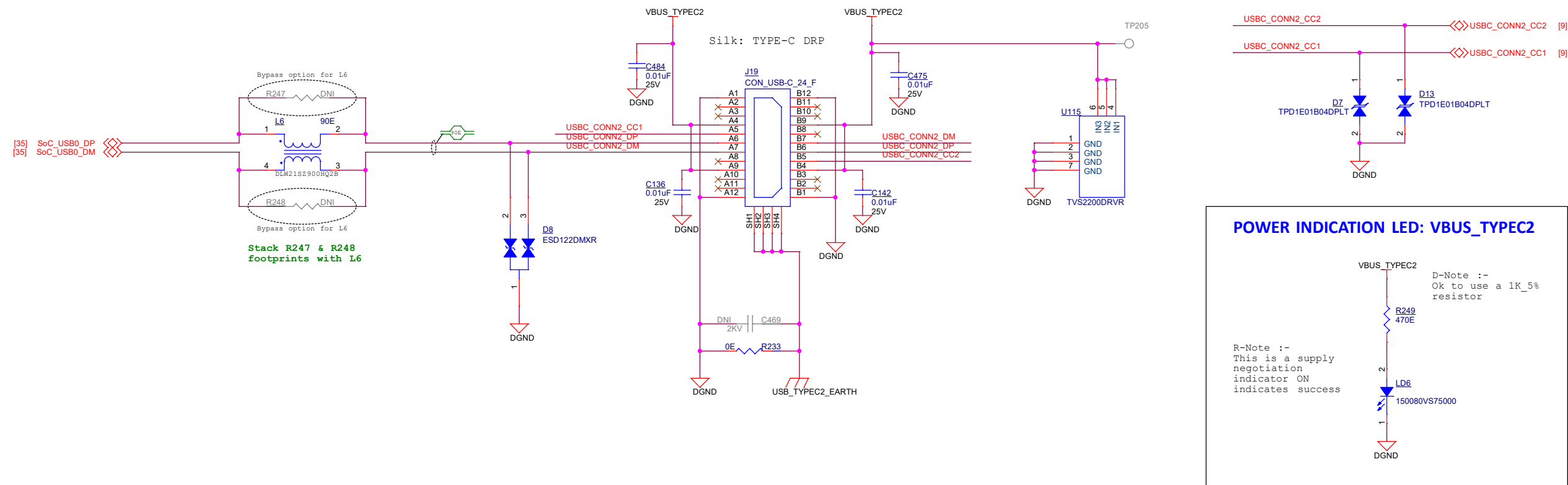
Sheet 34 of 47

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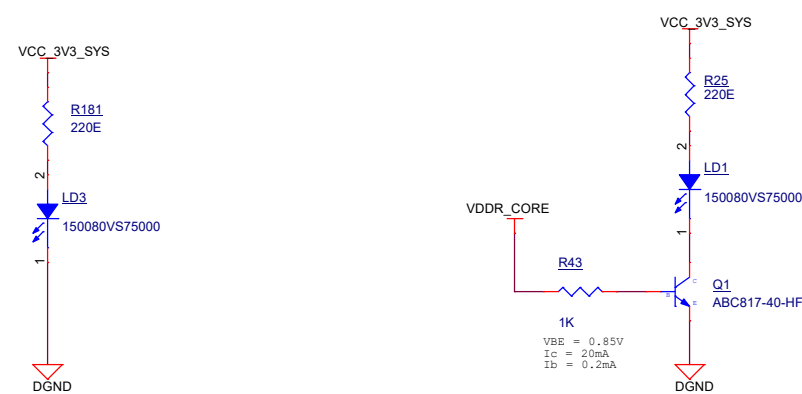
USB1 TYPE-A



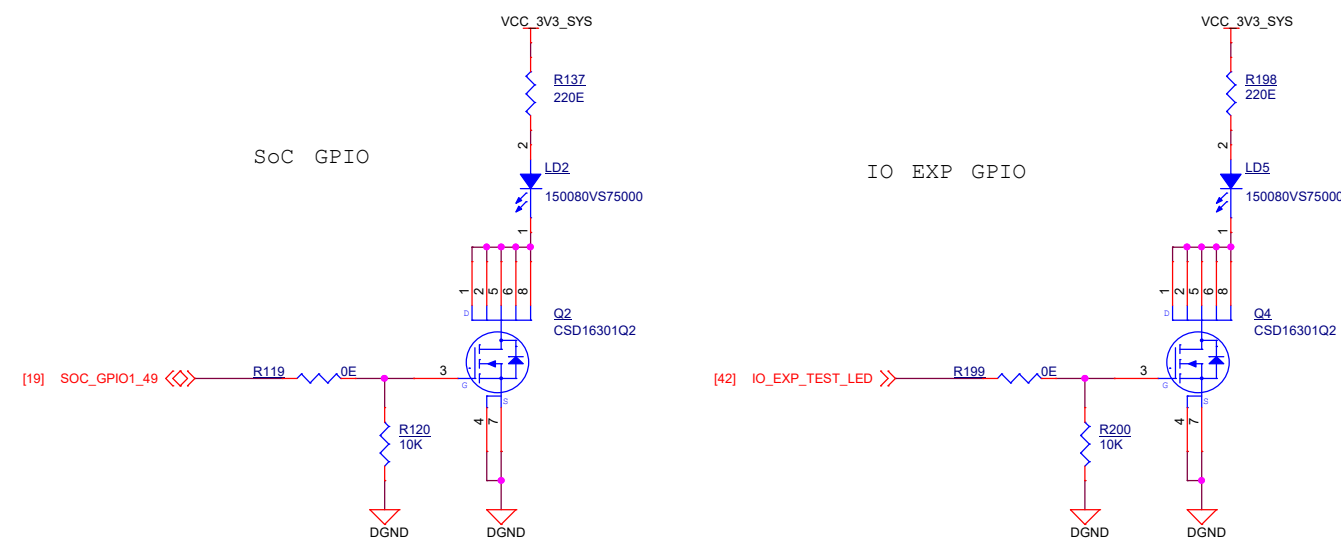
USB0 TYPE-C DRP



POWER RAIL LEDS



USER TEST LEDS



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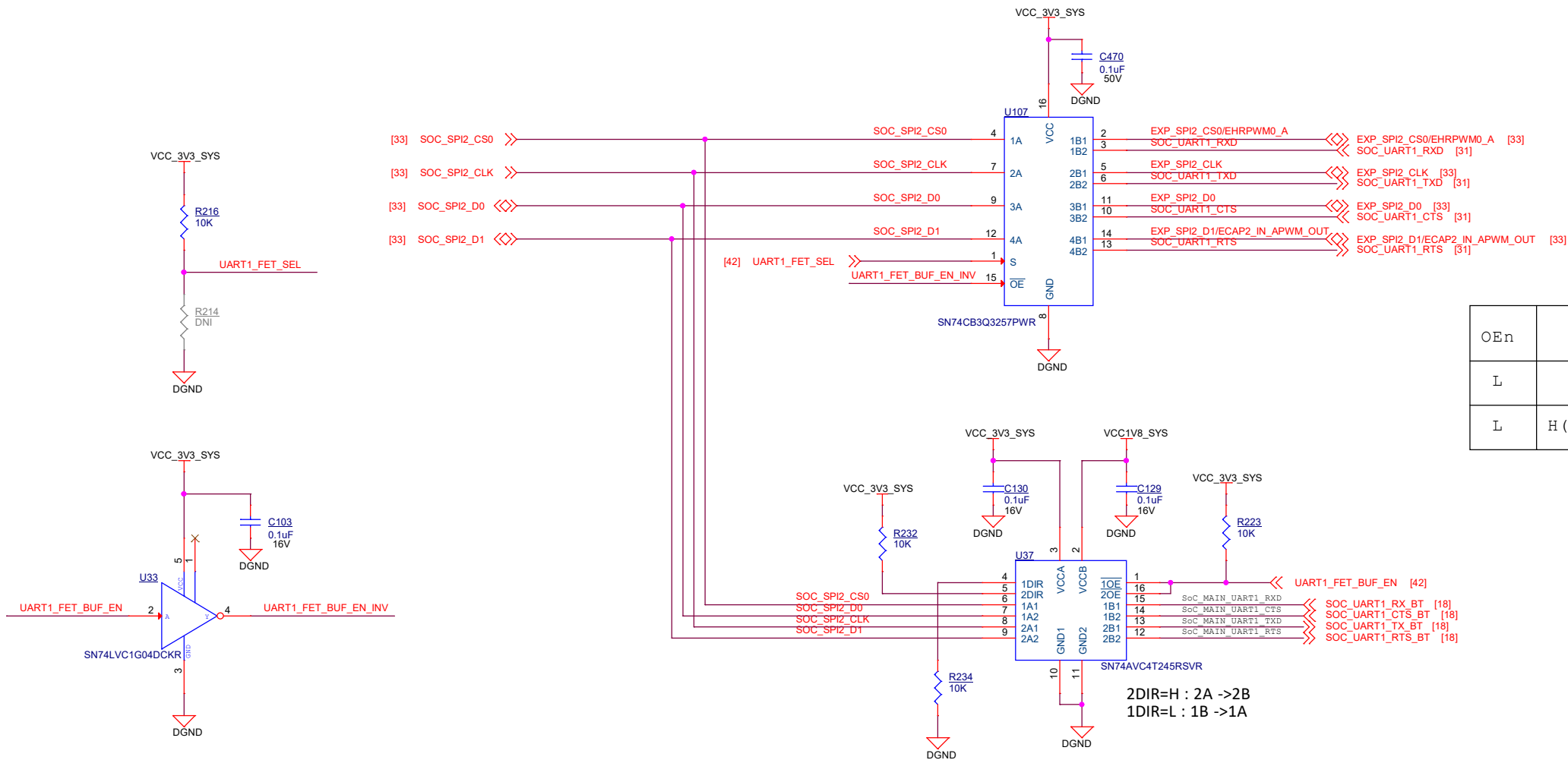
Title USB0 TYPE-C DRP & USER TEST LED

Size PROC164E1-1

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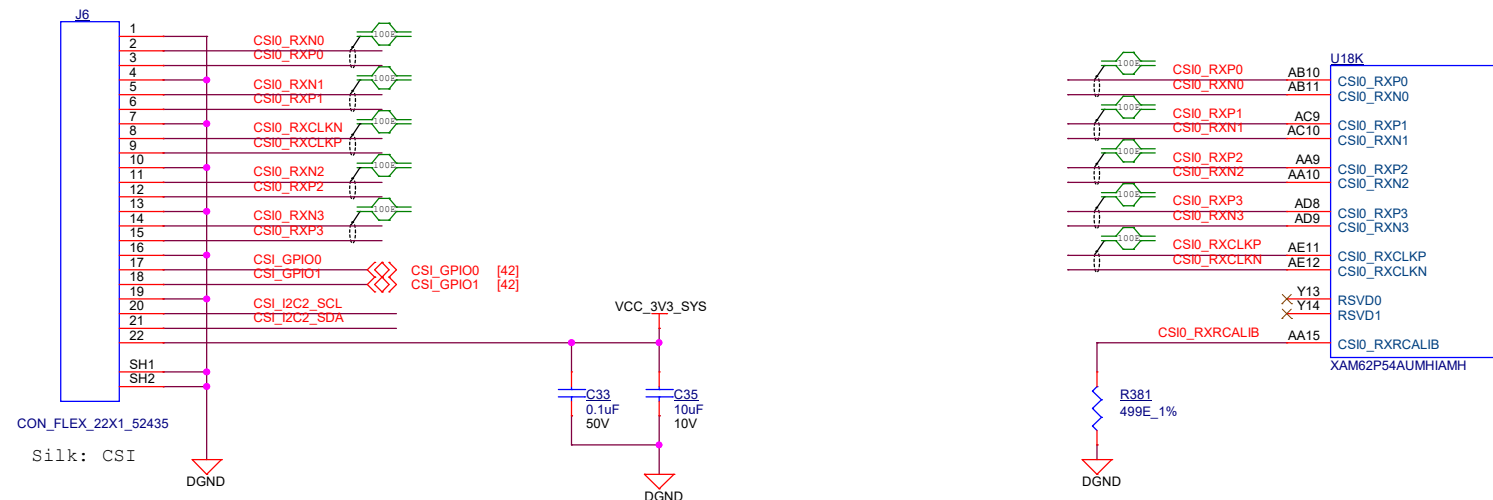
SoC MAIN UART1 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR



OEn	SEL	INPUT/OUTPUT	
		An	
L	L	An=nB1	SOC - EXP CONN
L	H (DEFAULT)	An=nB2	SOC - FT4232

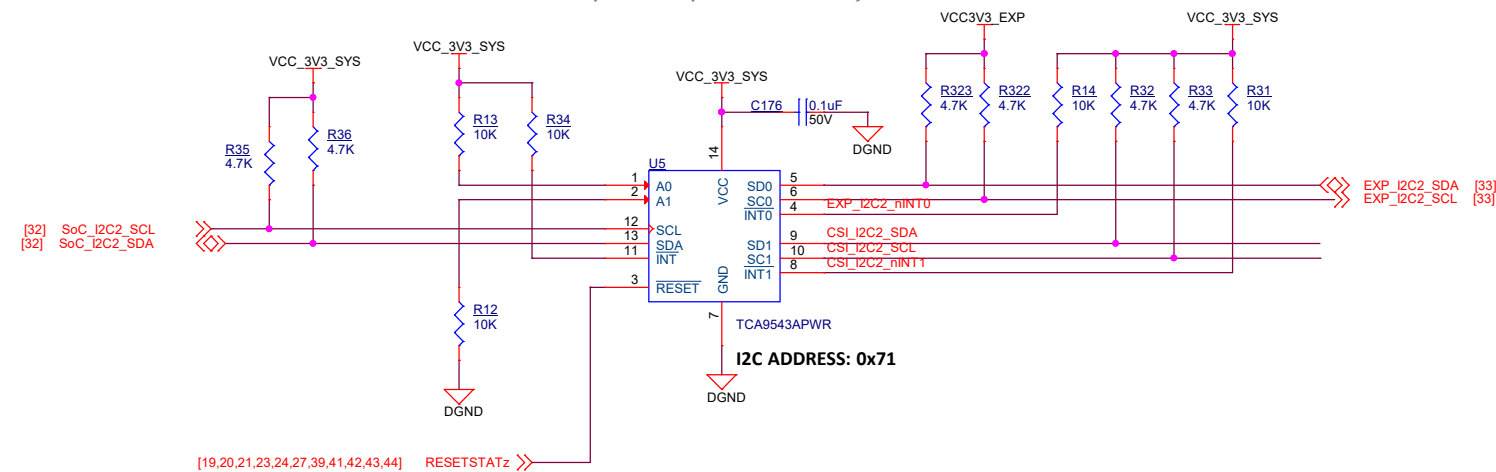
2DIR=H : 2A ->2B
1DIR=L : 1B ->1A

SOC CSI INTERFACE

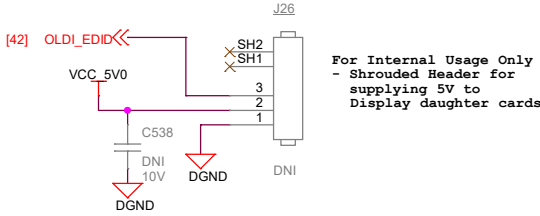
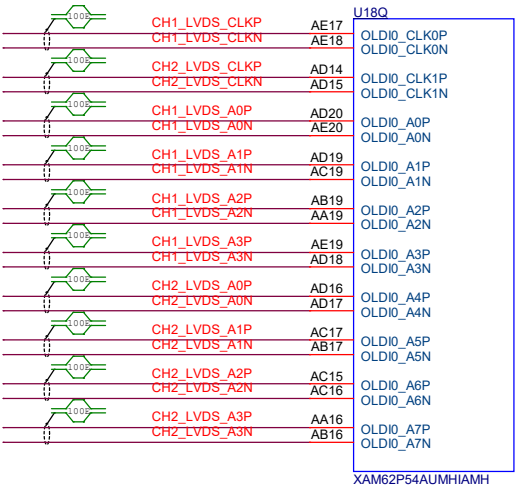
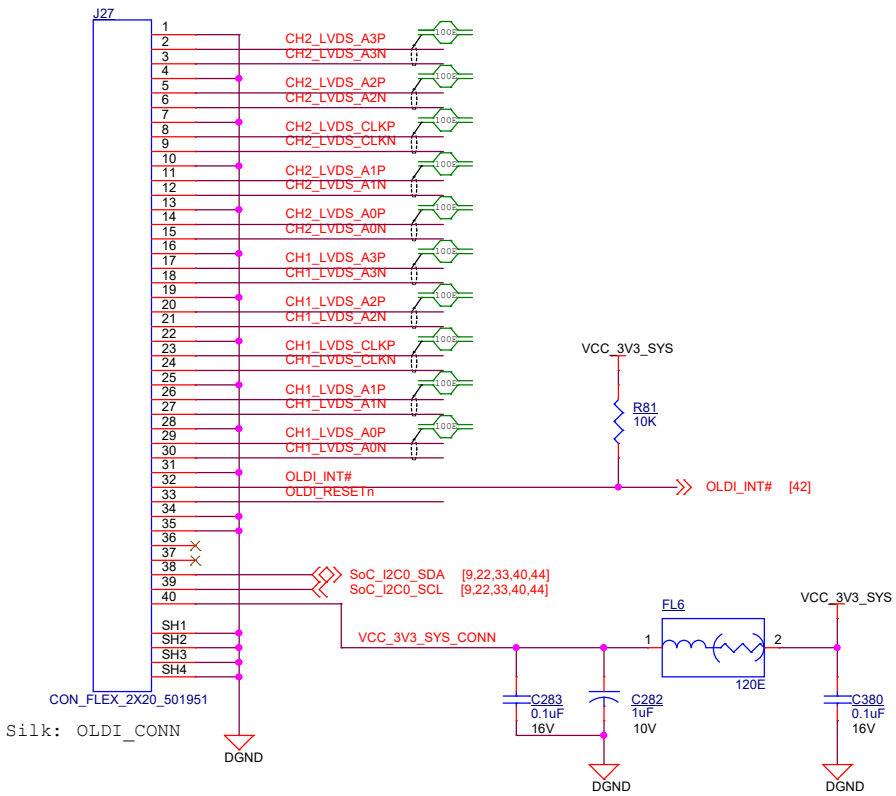


I2C SWITCH FOR SoC MAIN I2C2

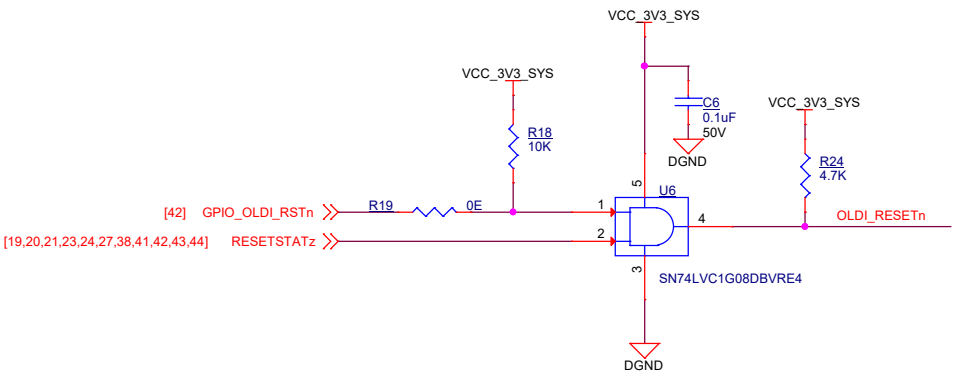
D-Note :-
Both the I2C outputs are off during power-up
The required I2C output needs to be configured



SOC OLDI INTERFACE



OLDI RESET

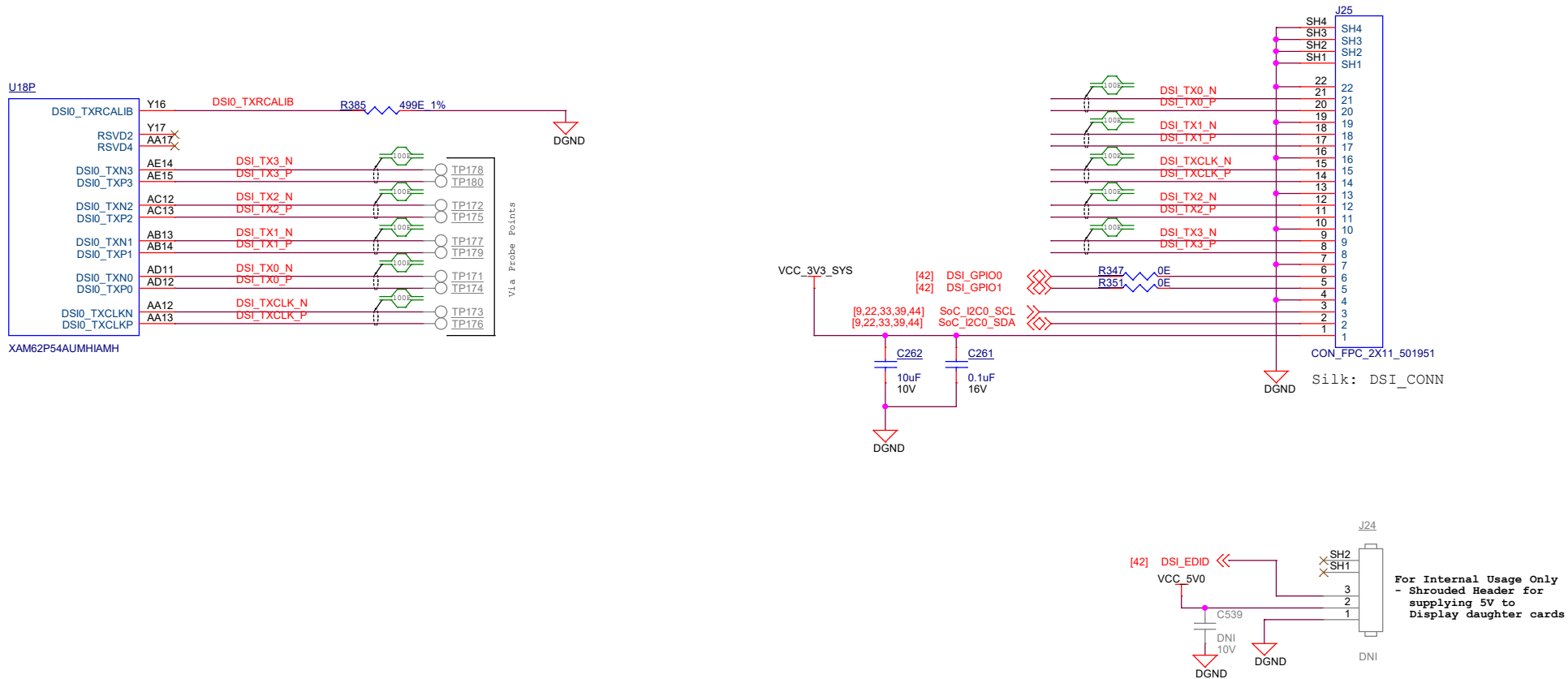


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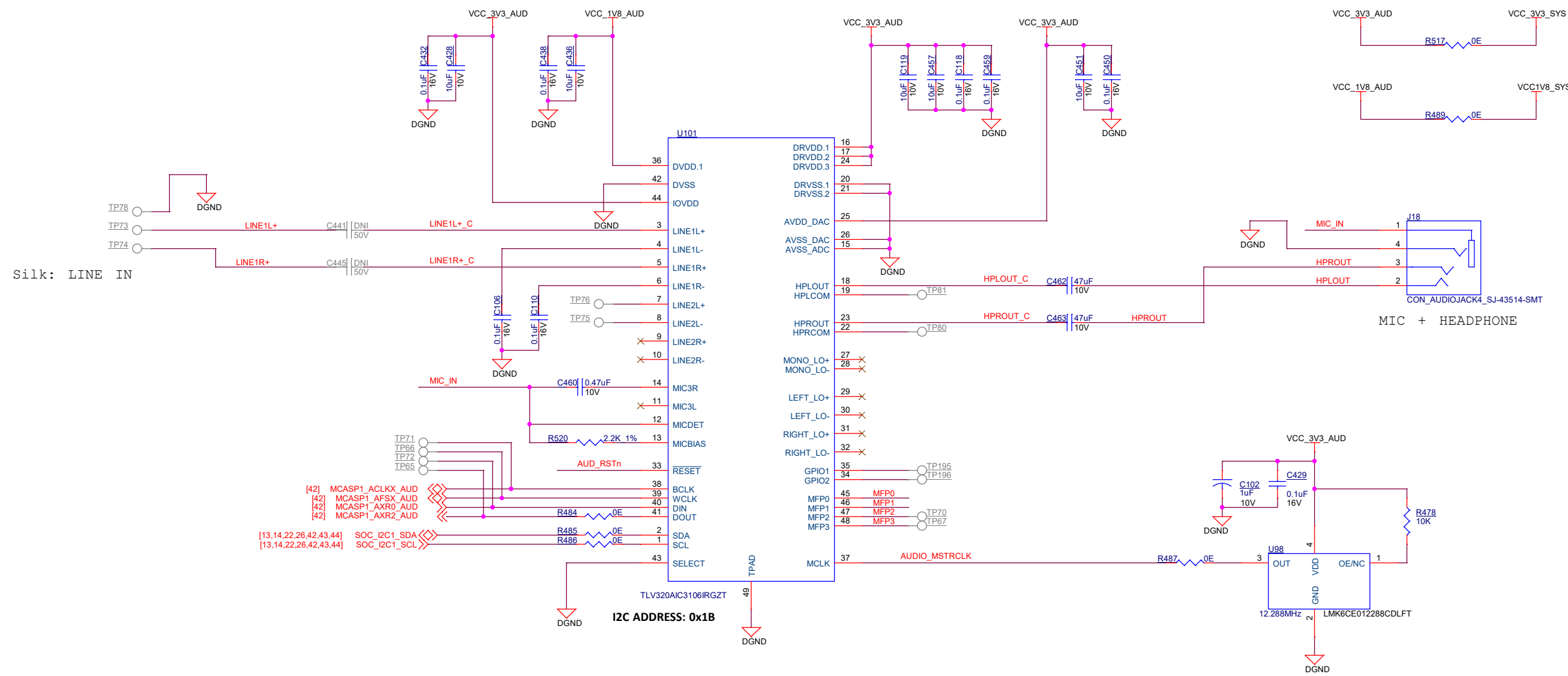


Title			SOC OLDI INTERFACE	
Size	C		PROC164E1-1	Rev
				E1-1
Date:		Wednesday, June 05, 2024	Sheet	39 of 47

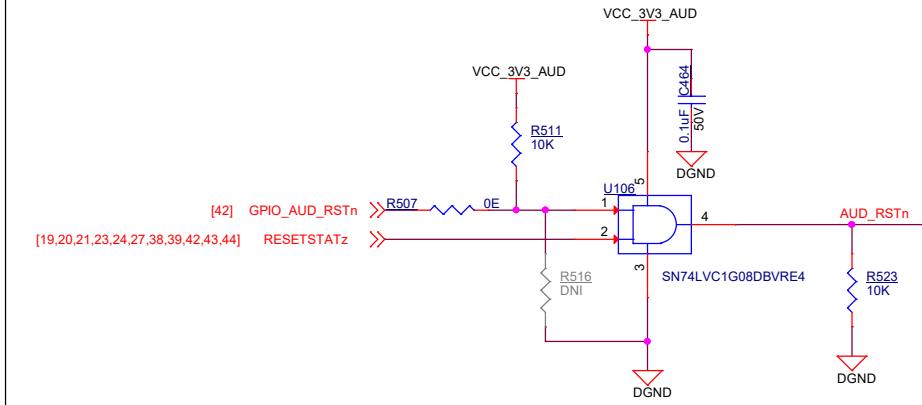
SOC DSI INTERFACE



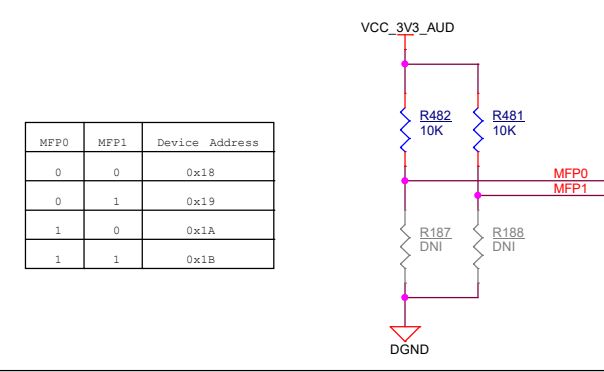
AUDIO CODEC



AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

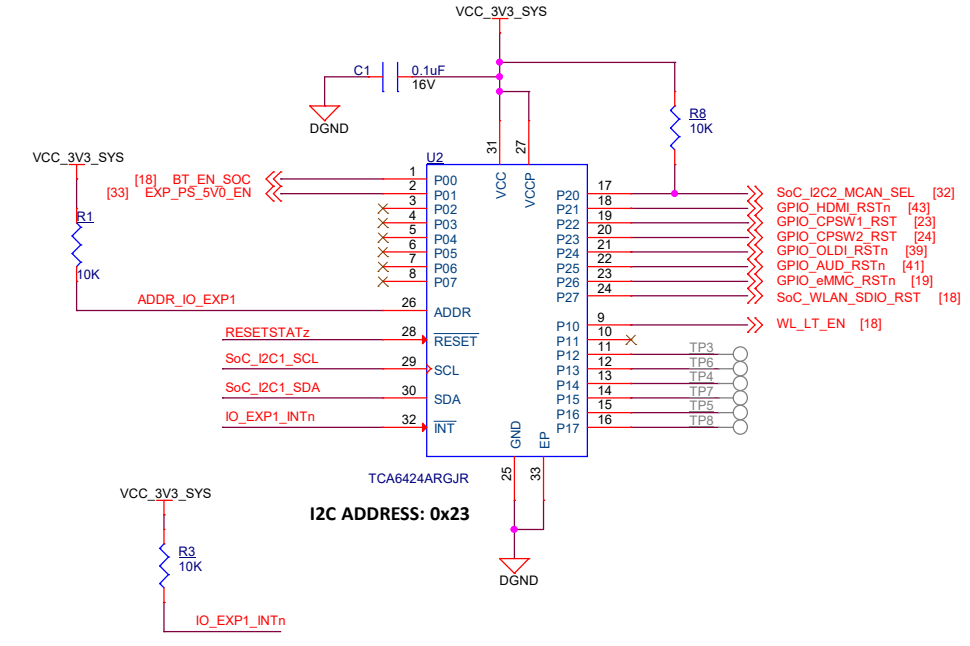
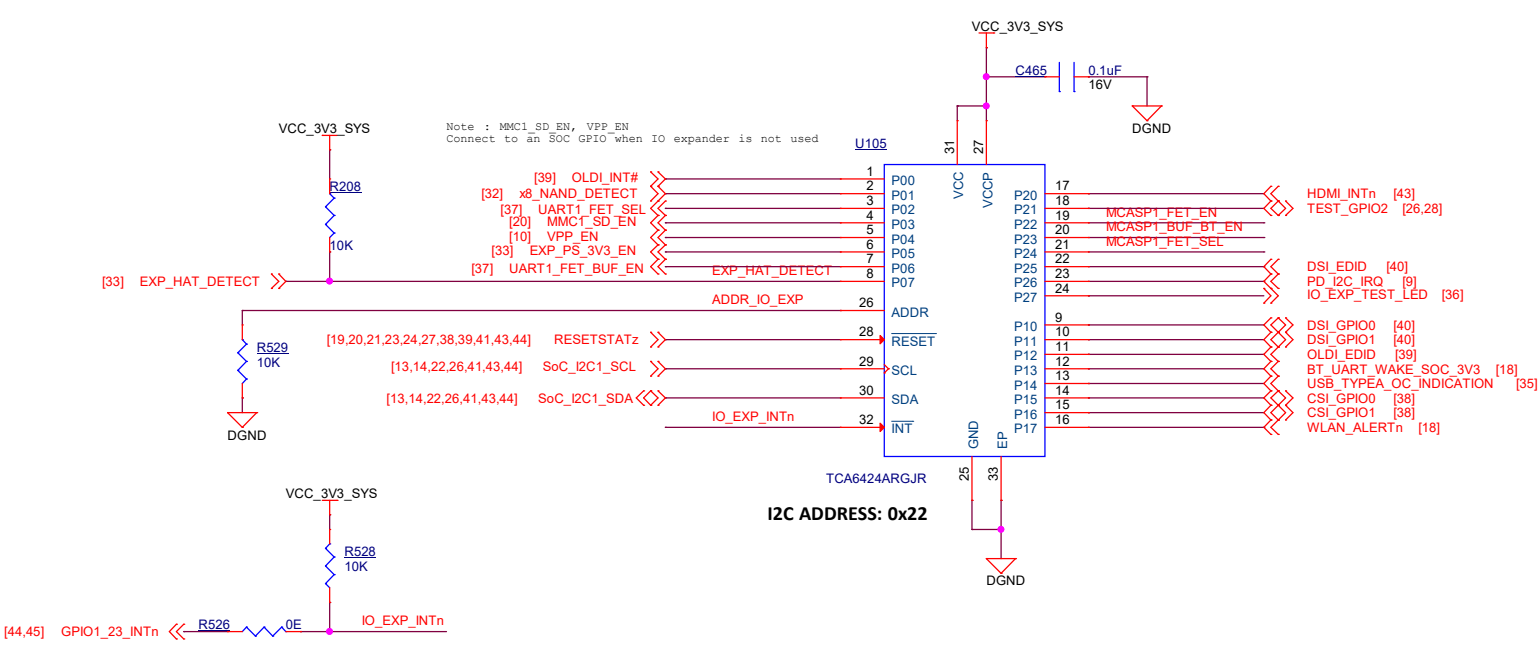


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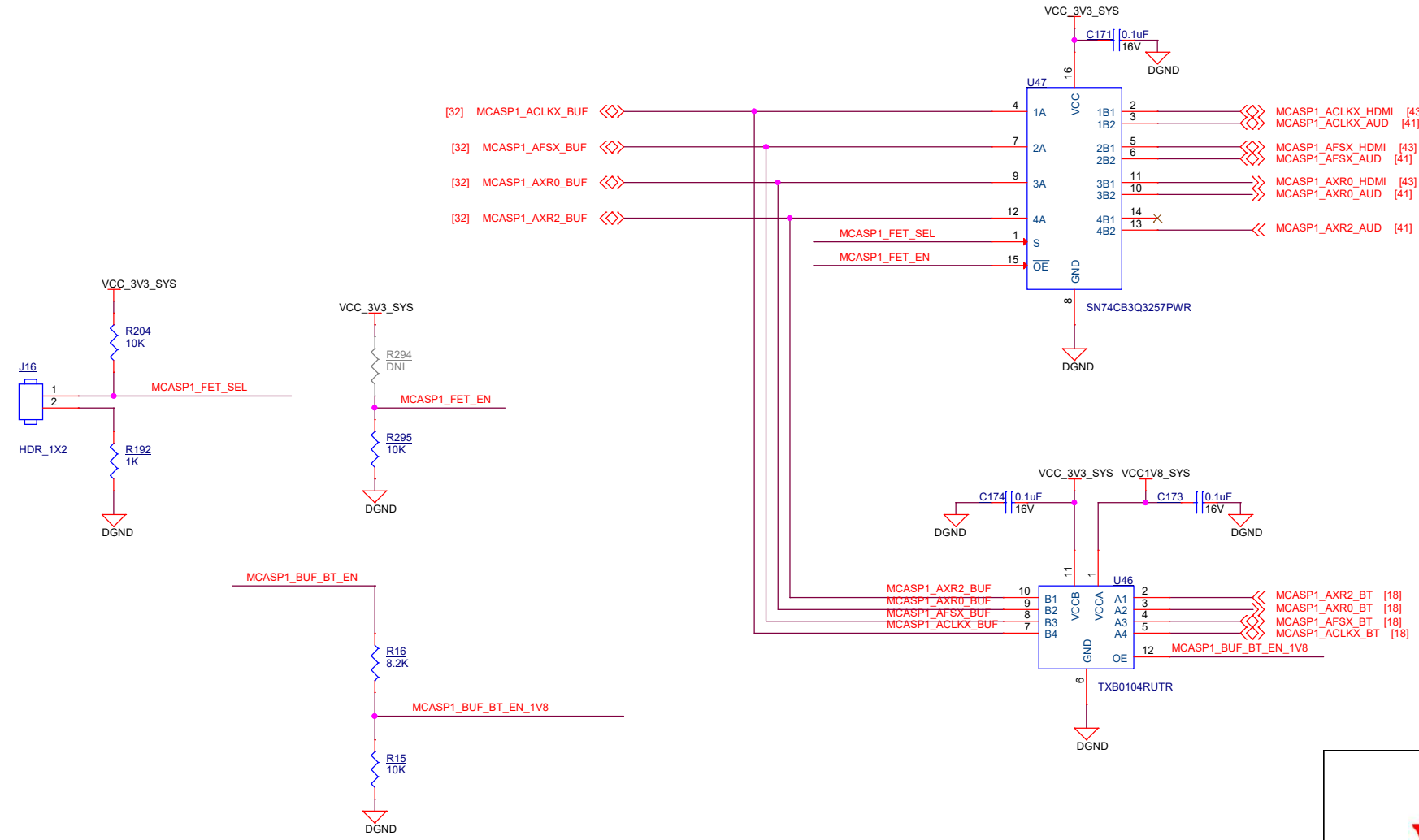


Title		AUDIO CODEC	
Size	PROC164E1-1	Rev	
C		E1-1	
Date:	Wednesday, June 05, 2024	Sheet	41 of 47

IO EXPANDER



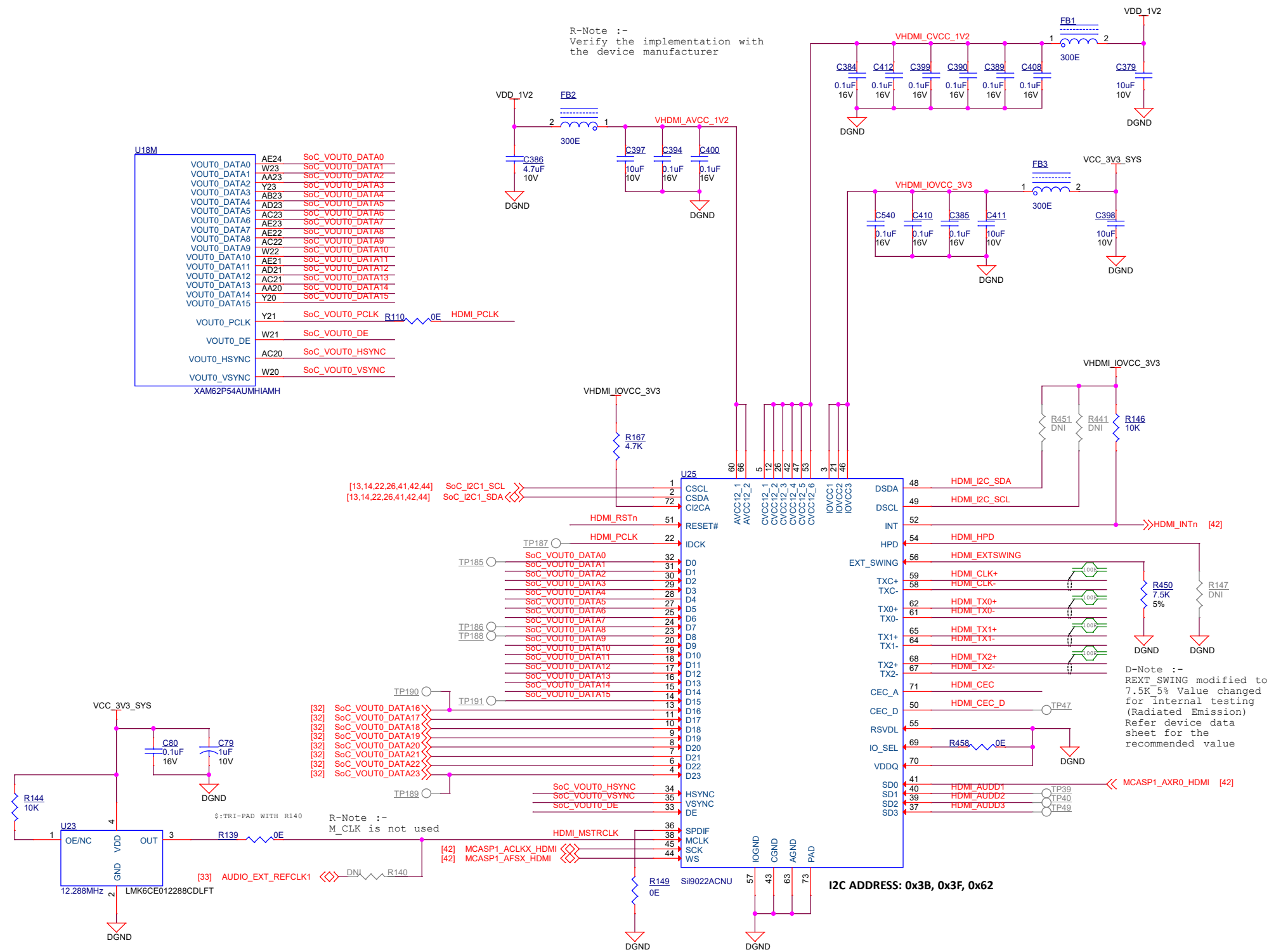
SOC MAIN McASP1 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR



OEn	SEL	INPUT/OUTPUT	
		An	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

HDMI INTERFACE

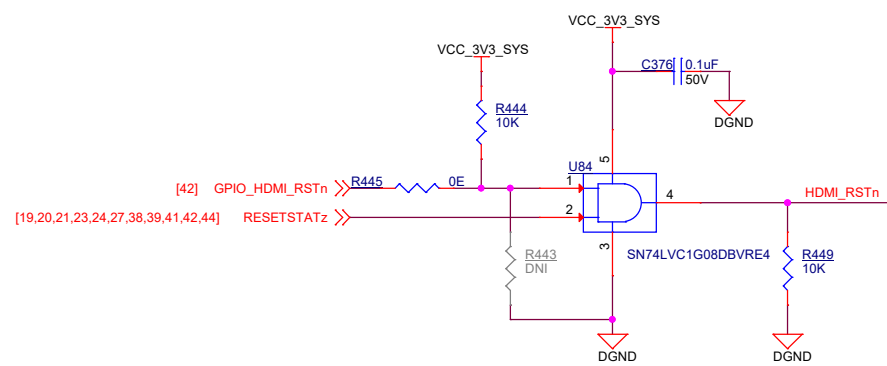
R-Note :-
Verify the implementation with
the device manufacturer



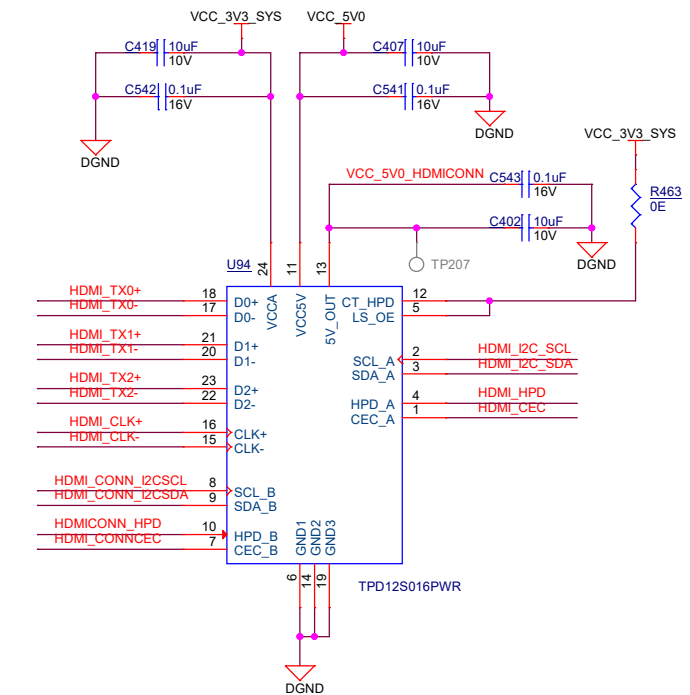
D-Note :-
REXT SWING modified to
7.5K 5% Value changed
for internal testing
(Radiated Emission)
Refer device data
sheet for the
recommended value

I2C ADDRESS: 0x3B, 0x3F, 0x62

HDMI RESET

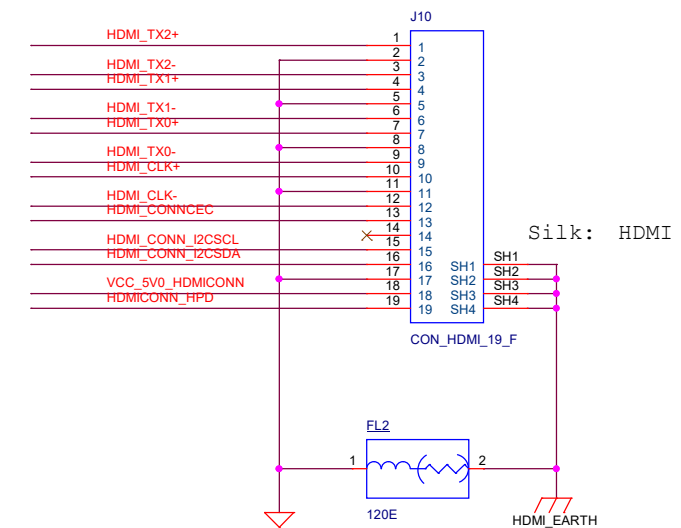


HDMI ESD DEVICE



D-Note :-
TPD12S016PWR has integrated pullup or pulldown resistors on the
I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR



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Title HDMI INTERFACE

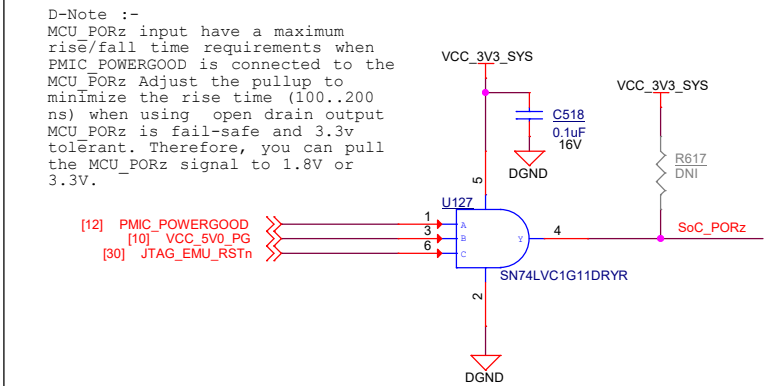
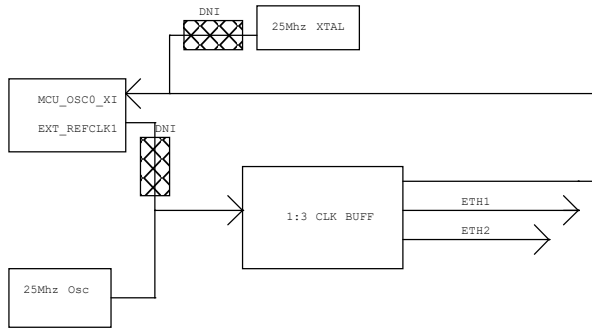
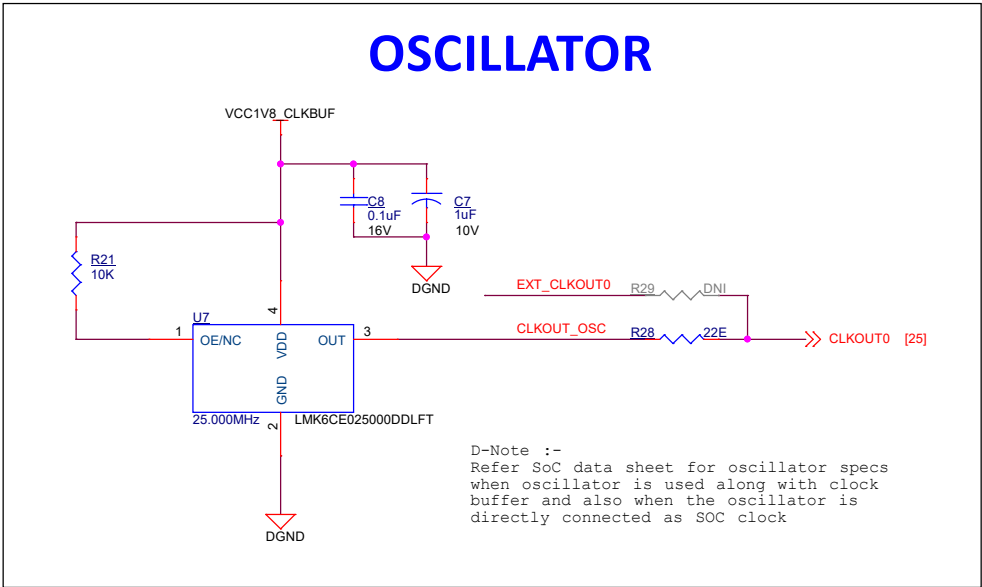
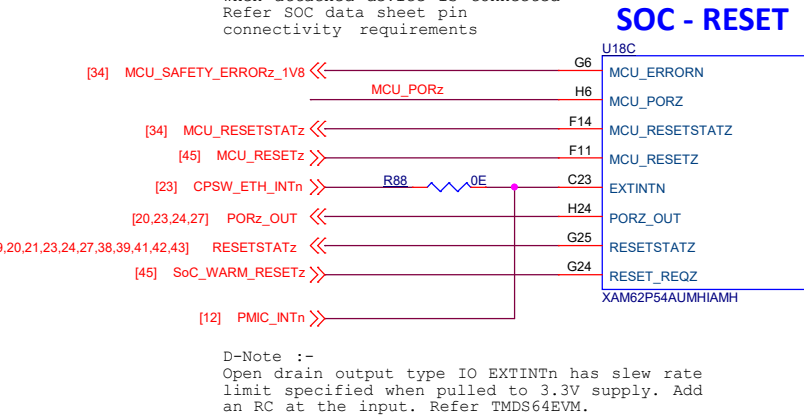
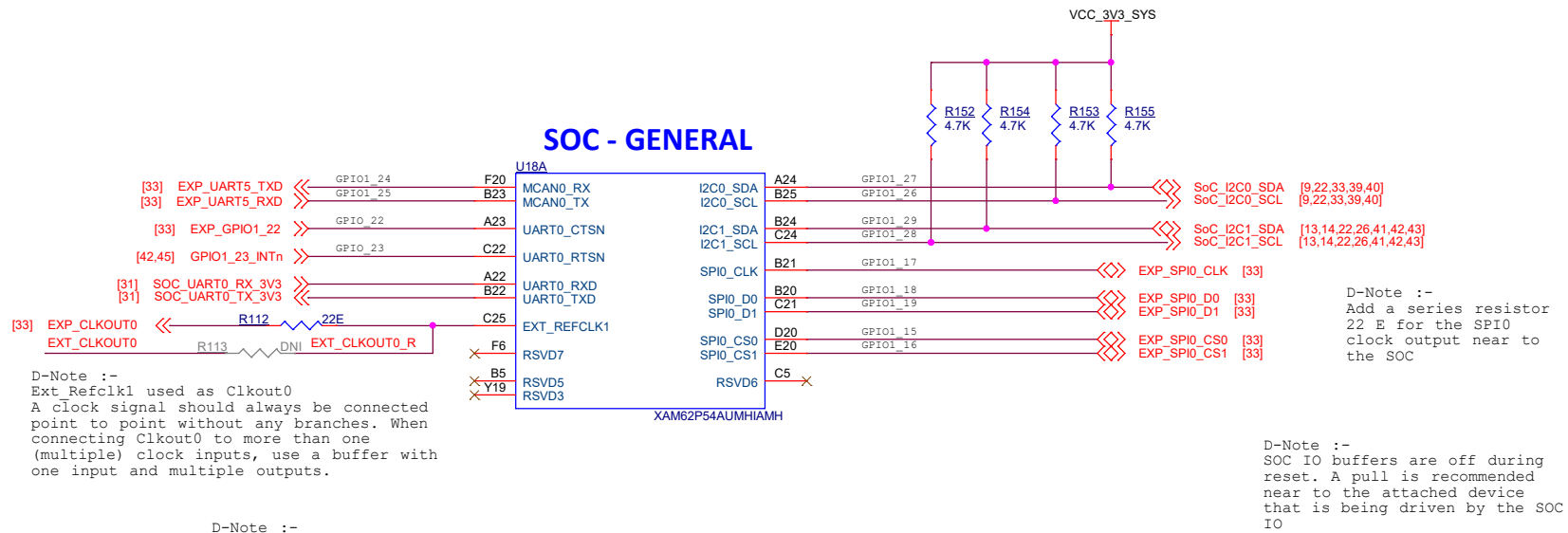
Size PROC164E1-1

C

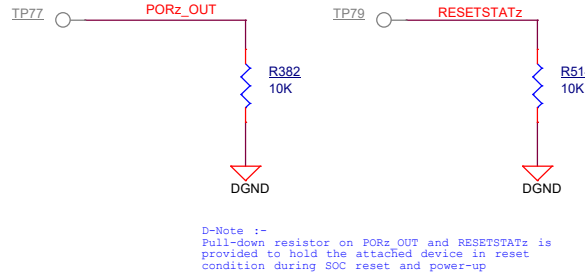
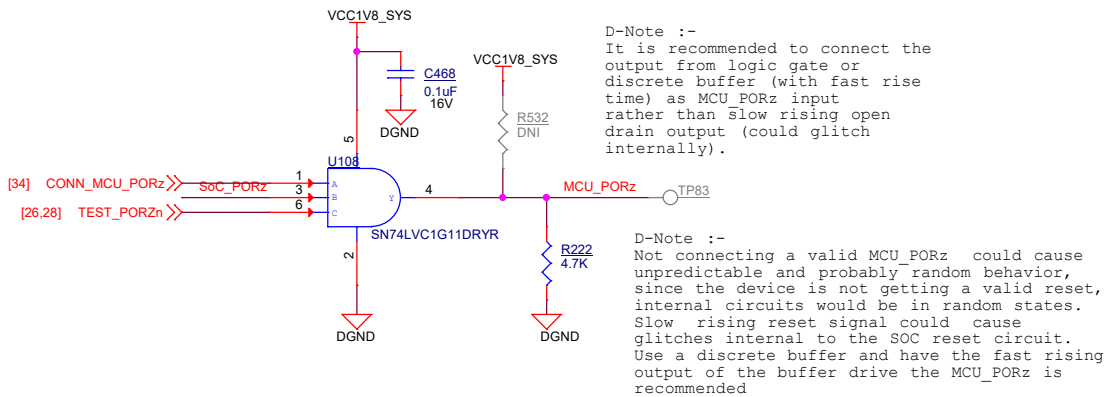
Date: Wednesday, June 05, 2024

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MCU POWER ON RESET



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Title OSCILLATOR

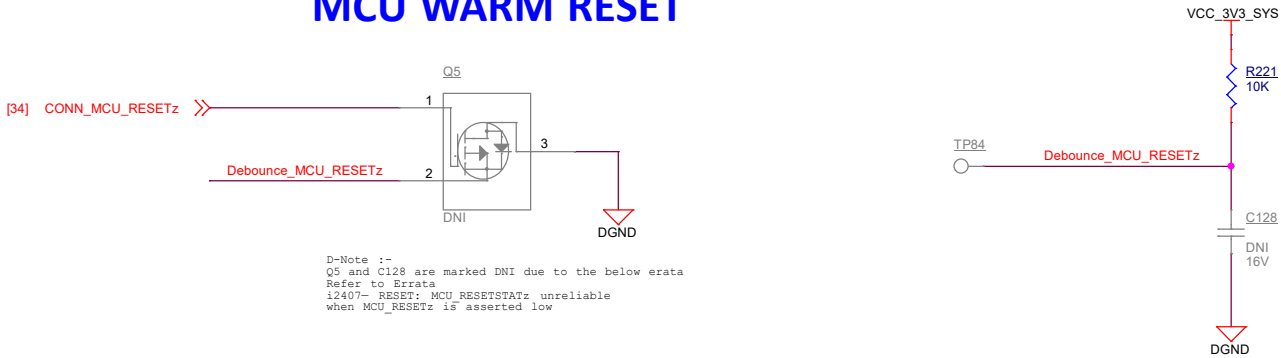
Size C
PROC164E1-1

Rev E1-1

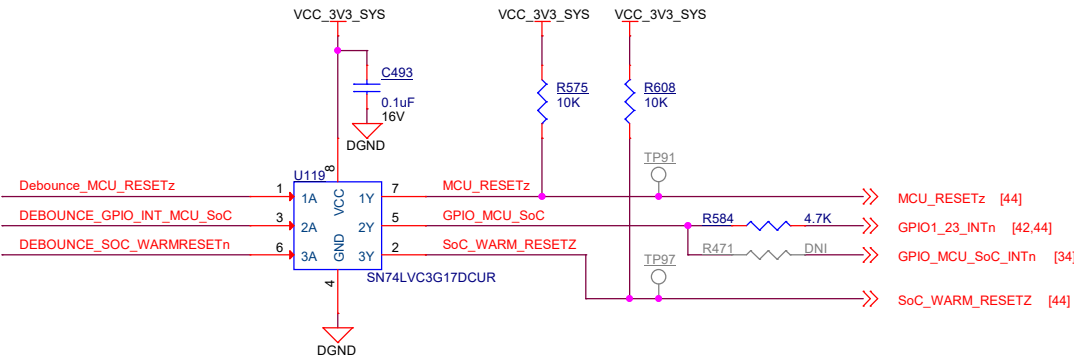
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SOC RESET

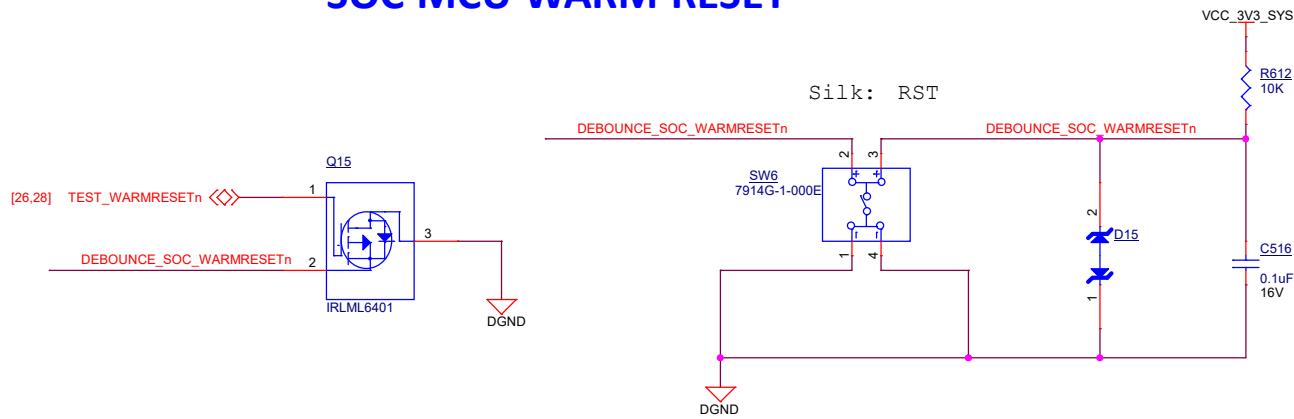
MCU WARM RESET



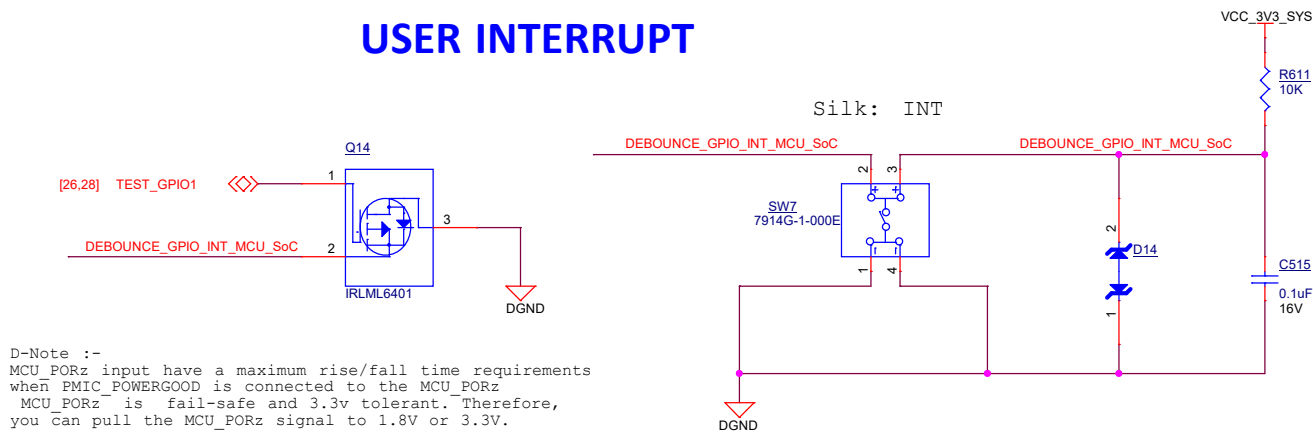
RESET & INT DEBOUNCE CIRCUIT



SOC MCU WARM RESET



USER INTERRUPT



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Title RESET

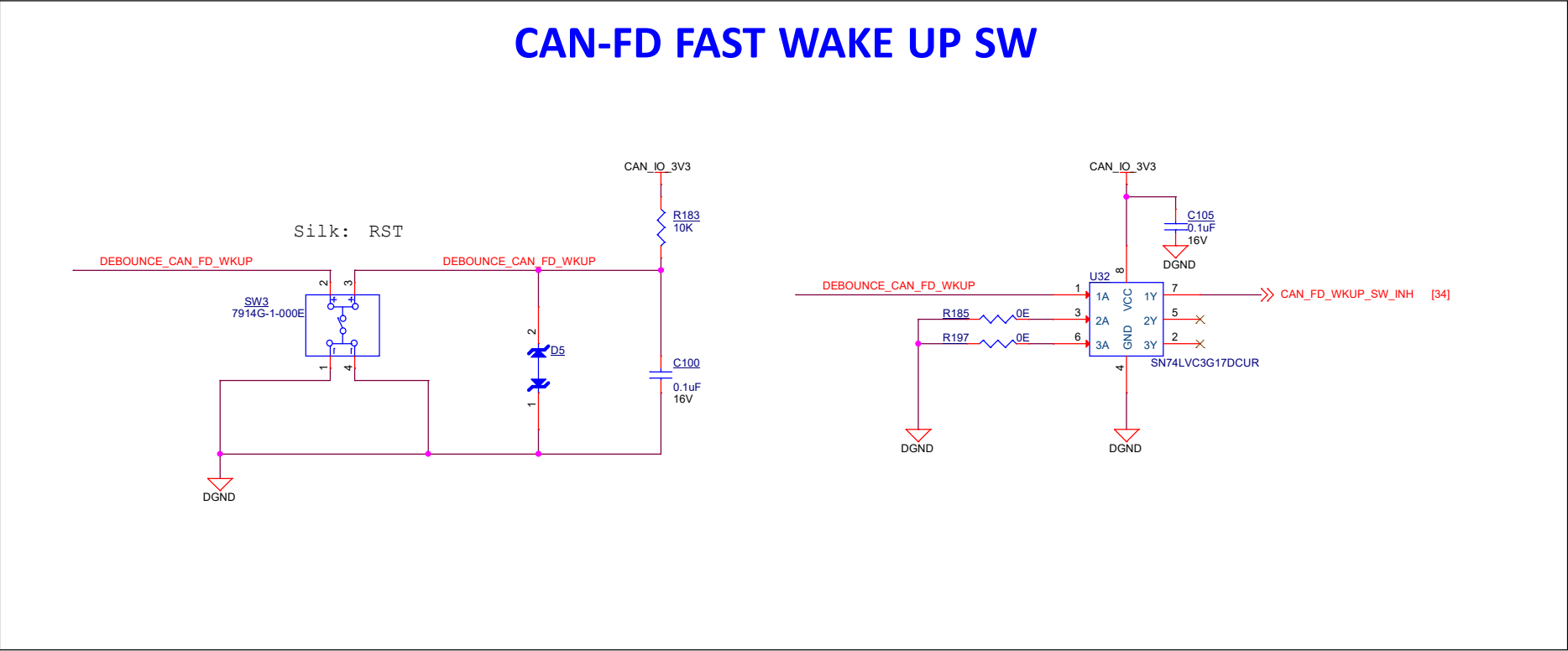
Size C PROC164E1-1

Rev E1-1

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CAN-FD FAST WAKE UP SW

The left diagram illustrates a mechanical switch-based wake-up circuit. A signal labeled "Silk: RST" controls a switch SW3 (7914G-1-000E). The switch is connected to a 3V3 supply through a 10K resistor (R183) and a 0.1uF capacitor (C100). A diode D5 is connected in parallel with the switch. The right diagram shows a MOSFET-based solution using an SN74LVC3G17DCUR (U32) buffer. The input is DEBOUNCE_CAN_FD_WKUP, which is pulled up to 3V3 by R185. The output of the buffer is connected to the CAN_FDWKUP pin (pin 7) and is also pulled up to 3V3 by R197. A 0.1uF capacitor (C105) is connected between the 3V3 supply and ground.



<p>Designed for TI by Mistral Solutions Pvt Ltd</p> <div>   </div>	Title		CAN FD WKUP SW	
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<p>Designed for TI by Mistral Solutions Pvt Ltd</p> <div>   </div>	Title		CAN FD WKUP SW	
	Size	PROC164E1-1		Rev
	C			E1-1
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<p>Designed for TI by Mistral Solutions Pvt Ltd</p> <div>   </div>	Title		CAN FD WKUP SW	
	Size	PROC164E1-1		Rev
	C			E1-1
	Date:	Wednesday, June 05, 2024	Sheet	46

<p>Designed for TI by Mistral Solutions Pvt Ltd</p> <div>   </div>	Title		CAN FD WKUP SW	
	Size	PROC164E1-1		Rev
	C			E1-1
	Date:	Wednesday, June 05, 2024	Sheet	46

<p>Designed for TI by Mistral Solutions Pvt Ltd</p> <div>   </div>	Title		CAN FD WKUP SW	
	Size	PROC164E1-1		Rev
	C			E1-1
	Date:	Wednesday, June 05, 2024	Sheet	46

<p>Designed for TI by Mistral Solutions Pvt Ltd</p> <div>   </div>	Title		CAN FD WKUP SW	
	Size	PROC164E1-1		Rev
	C			E1-1
	Date:	Wednesday, June 05, 2024	Sheet	46

<p>Designed for TI by Mistral Solutions Pvt Ltd</p> <div>   </div>	Title		CAN FD WKUP SW	
	Size	PROC164E1-1		Rev
	C			E1-1
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MOUNTING HARDWARE

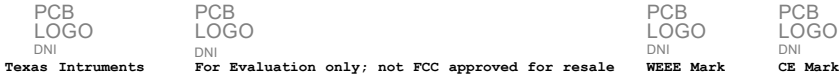
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



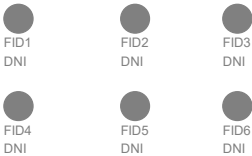
AM62P SOCKET



JUMPERS



FIDUCIALS



LABELS

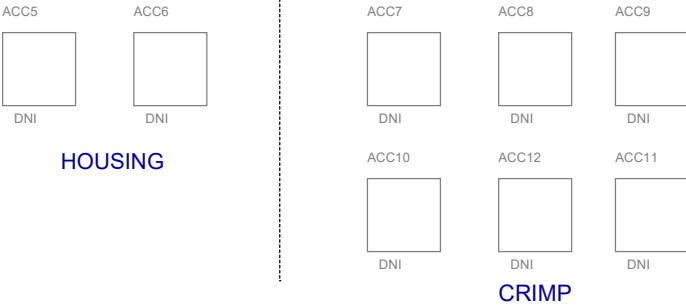


SCREW & WASHER FOR PCIe M.2



D-Note :-
Refer STRAP CONFIGURATION OF ETHERNET PHYS page from
SK-AM64B schematics

HOUSING & CRIMP FOR DSI AND OLDI HEADER



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Title HARDWARE SCHEMATICS

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