

REVISION HISTORY (REV E2)

SL no.	DESCRIPTION OF CHANGES	AUTHOR
1	Drafted from REV E1 Schematics. Net names updated wrt SOC symbol (U1) pin naming conventions	Mistral Design Team
2	Added MDIO/MDC Mux (U81) FOR MDIO0_MDIO and MDIO0_MDC signals. Changed the IO expander part (U60) from TCA6416ARTWR to TCA6424ARGJR and it's I2C slave address changed to 0x22	Mistral Design Team
3	Added Circuit for SoC Safety_error (Q20), Removed C3746 cap, C82 Cap changed to 6.8nF, DNI'd termination caps on ADC lines (C318 to C324). Added green LEDs for PMIC LDO rails	Mistral Design Team
4	Added layer of MUXing to allow MII0 OR MII1 to be inputs for either Ethernet interface - on-board PHY or Add-on board connector	Mistral Design Team
5	Added 1x2 header (J22) with jumper on INH/PMIC_WKUP2 net	Mistral Design Team
6	Added resistor mux across ICSSM Ethernet/HSEC lines	Mistral Design Team
7	Resistor muxes across ICSSM Ethernet/HSEC lines value changed from 0E to 33E	Mistral Design Team
8	SW15 - for ICSSM MII0/MII1 signals selection has been removed. SW14 will control all six ICSSM muxes	Mistral Design Team
9	Rearrangement is done wrt ICSSM signals, as resistor mux should now be at PHY end of the scheme. Rearranged signals on ADC Muxes (U70,U72,U73). DNI'd R205, Populated R204 for FSI activation. OSPI_LBCLK connection rearranged.	Mistral Design Team
10	Changed resistor arrays to individual 0201 0-ohm resistors on ICSSM lines. Added MDC/MDIO mux (U90) for Add on connector. DNI'd R3865, Populated R190 with default set to HSEC_EPWM11_A.	Mistral Design Team
11	Ethernet/HSEC muxes SEL lines changed to independently controllable SEL lines.(SW16 added for ICSSM1_MUX_SEL) Changed R474 to pull-up resistor to select CPSW for on-board PHY MDIO/MDC lines. Populated all ADC caps - 330 Pf. Populated resistors on MDC lines across U90 and U91). Changed ICSSM -> ICSS in all schematic titles	Mistral Design Team
12	Added shunt jumpers to the schematic for J20,J21,J22	Mistral Design Team