AM275 EVM

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BOARD REVISION	A
SCHEMATIC VERSION	1.0

Note:
Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of design before board assembly

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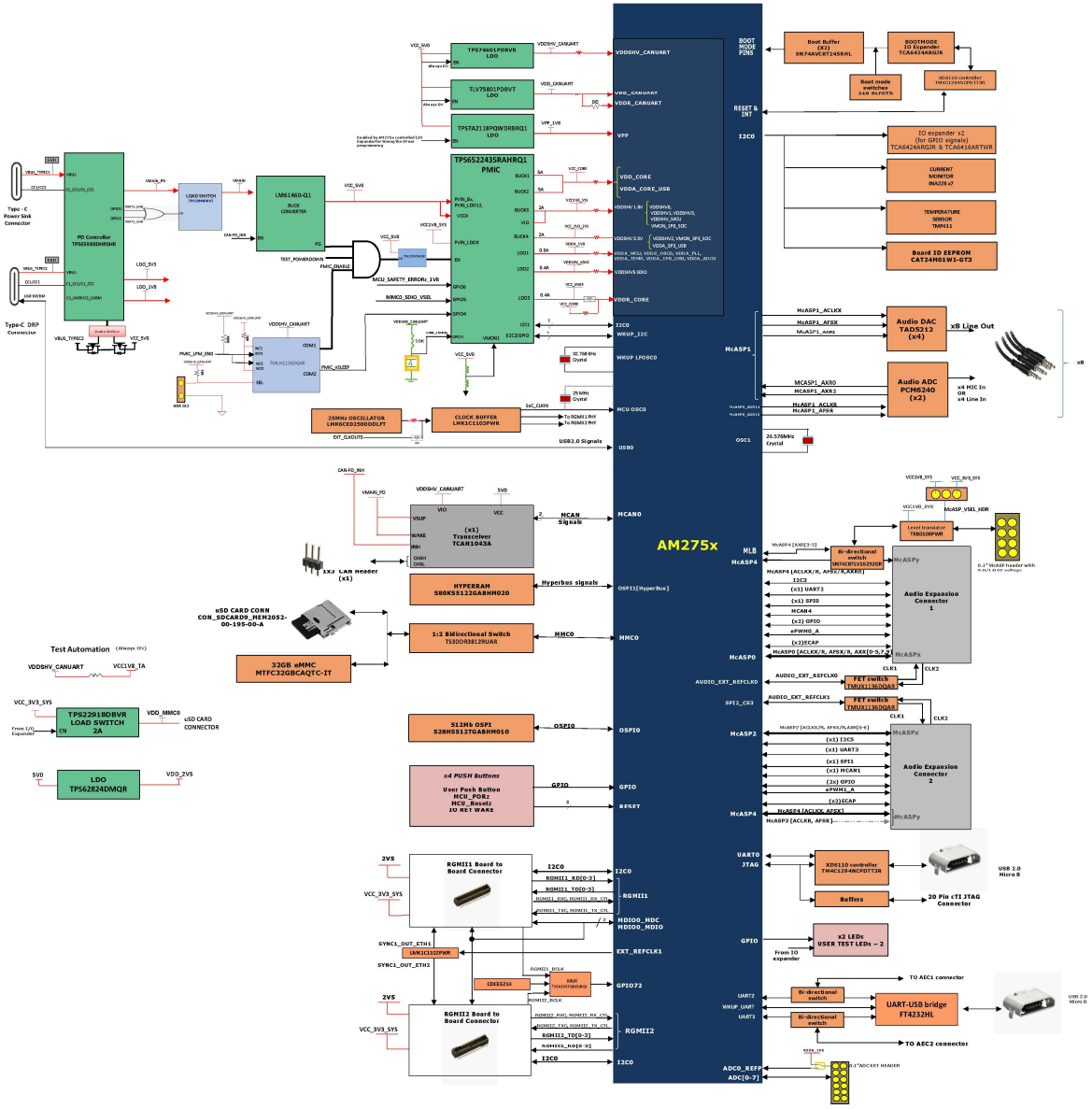
REVISION HISTORY

A	0.1	28-02-2025	Drafted from Rev_E2, Ver 0.2 schematics. Updated the U134 part from LM61460AASQRJRRQ1 to LM61460AFSQRJRRQ1 as requested by TI.	Mistral Design Team	Pandiyarajan	Ajit MB
	0.2	12-03-2025	Reverted the MPN of U134 from LM61460AFSQRJRRQ1 to LM61460AASQRJRRQ1, same as in Rev_E2, as requested by TI.	Mistral Design Team	Pandiyarajan	Ajit MB
	1.0	14-03-2025	Schematic Baselined	Mistral Design Team	Pandiyarajan	Ajit MB

LINK TO DESIGN COLLATERALS

FAQs

BLOCK DIAGRAM AM275x EVM



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Title	BLOCK DIAGRAM AM62D_ SKEVM		
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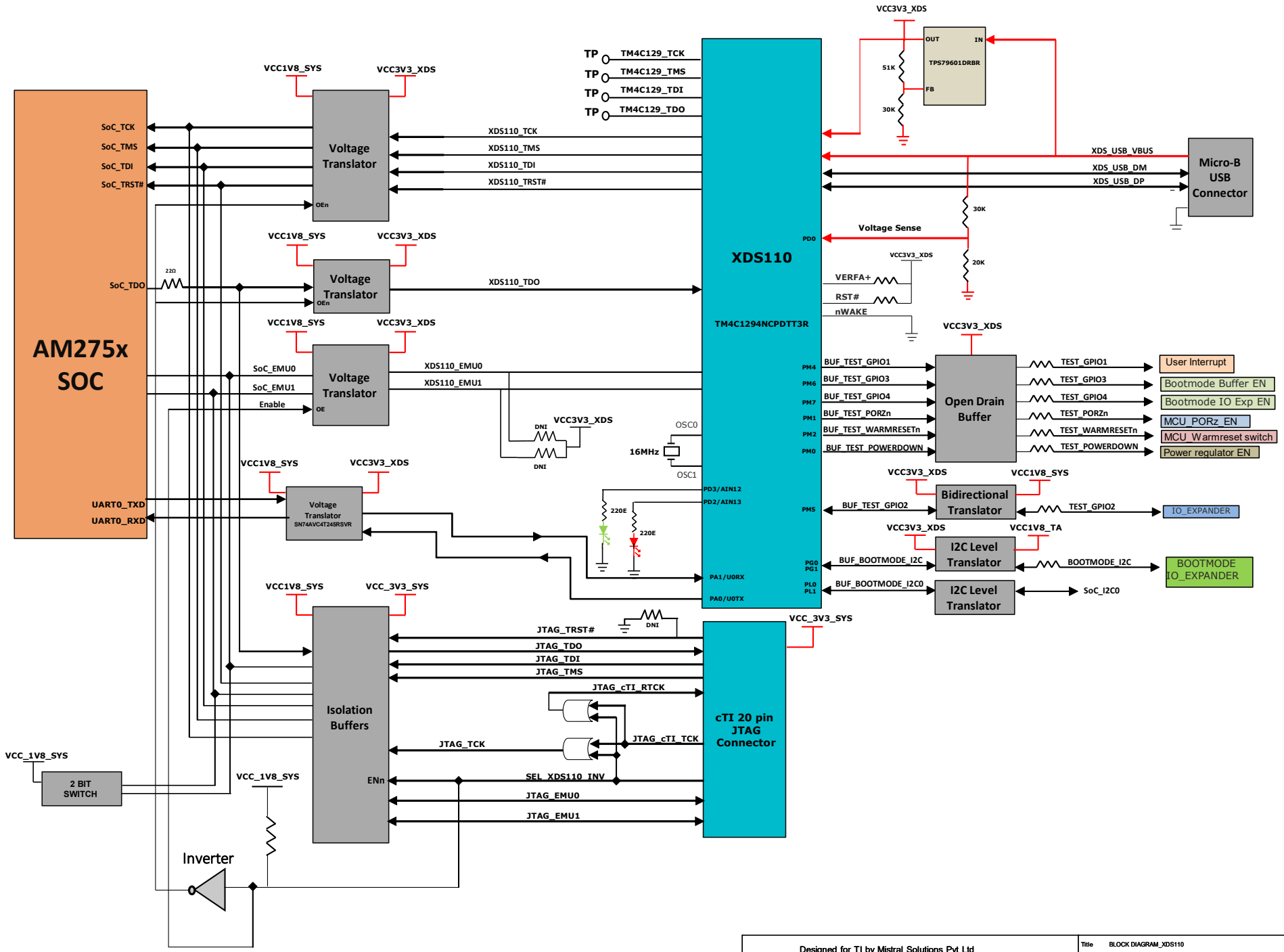
BLOCK DIAGRAM_XDS110



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Texas Instruments — MISTRAL

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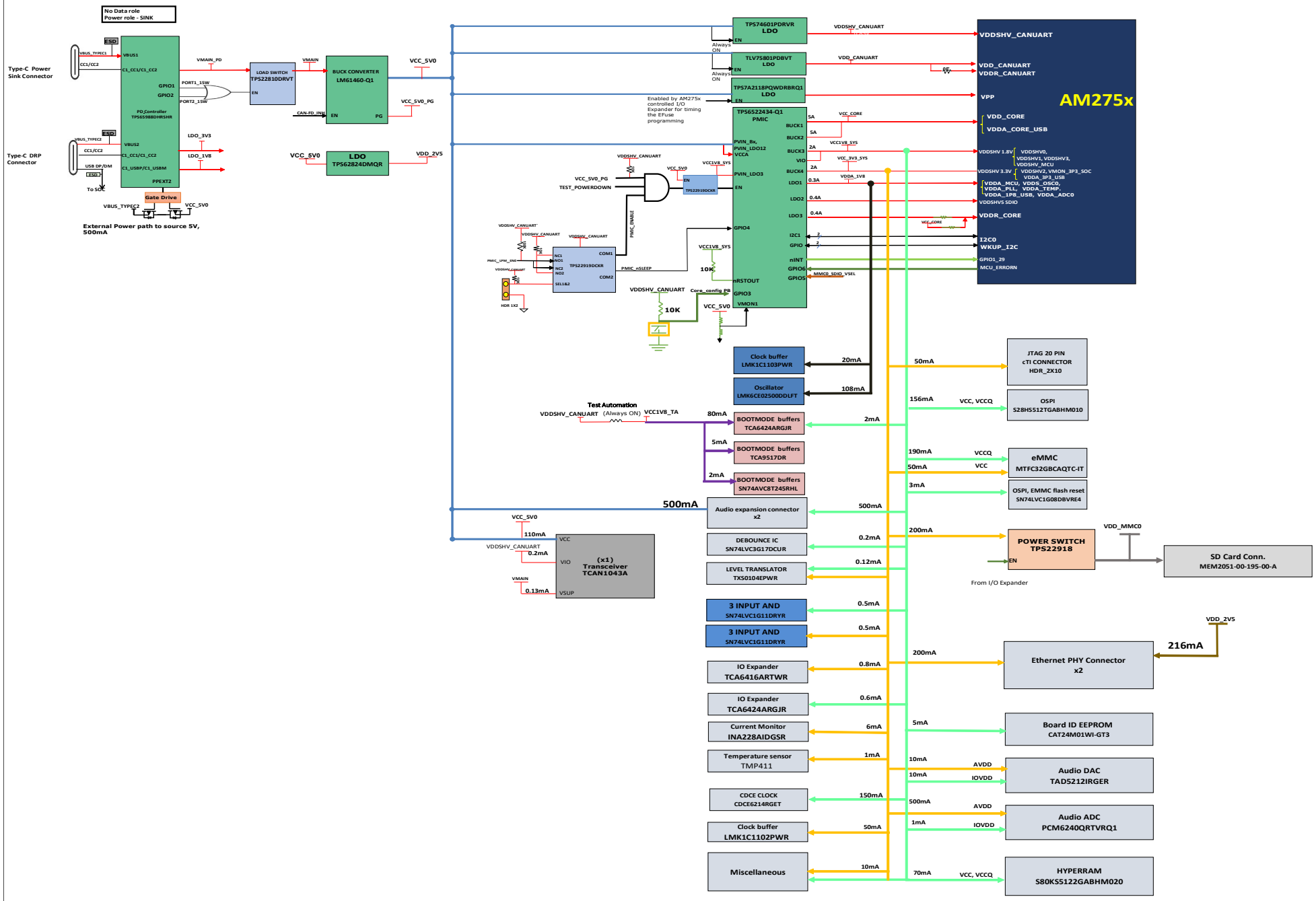
POWER ARCHITECTURE BLOCK DIAGRAM



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Title	POWER ARCHITECTURE BLOCK DIAGRAM		
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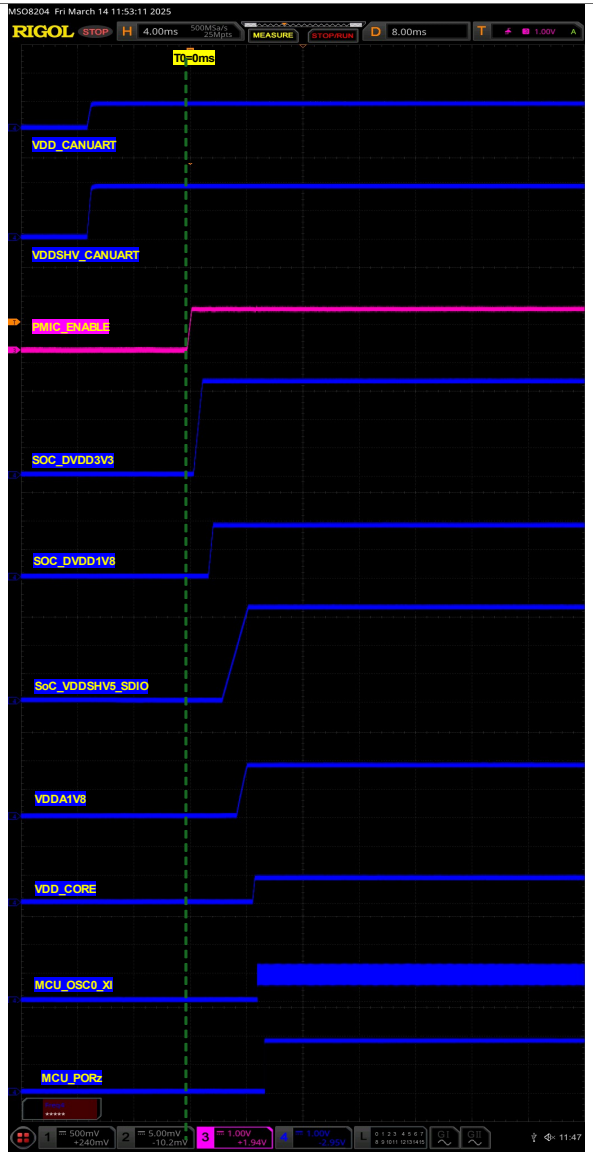
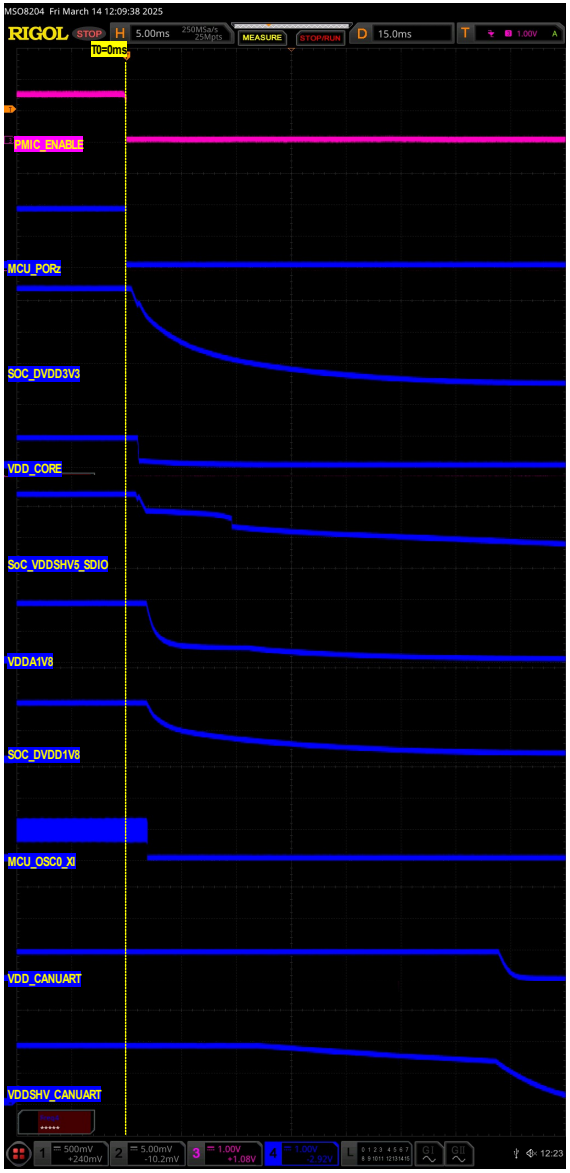
POWER UP SEQUENCE



POWER DOWN SEQUENCE



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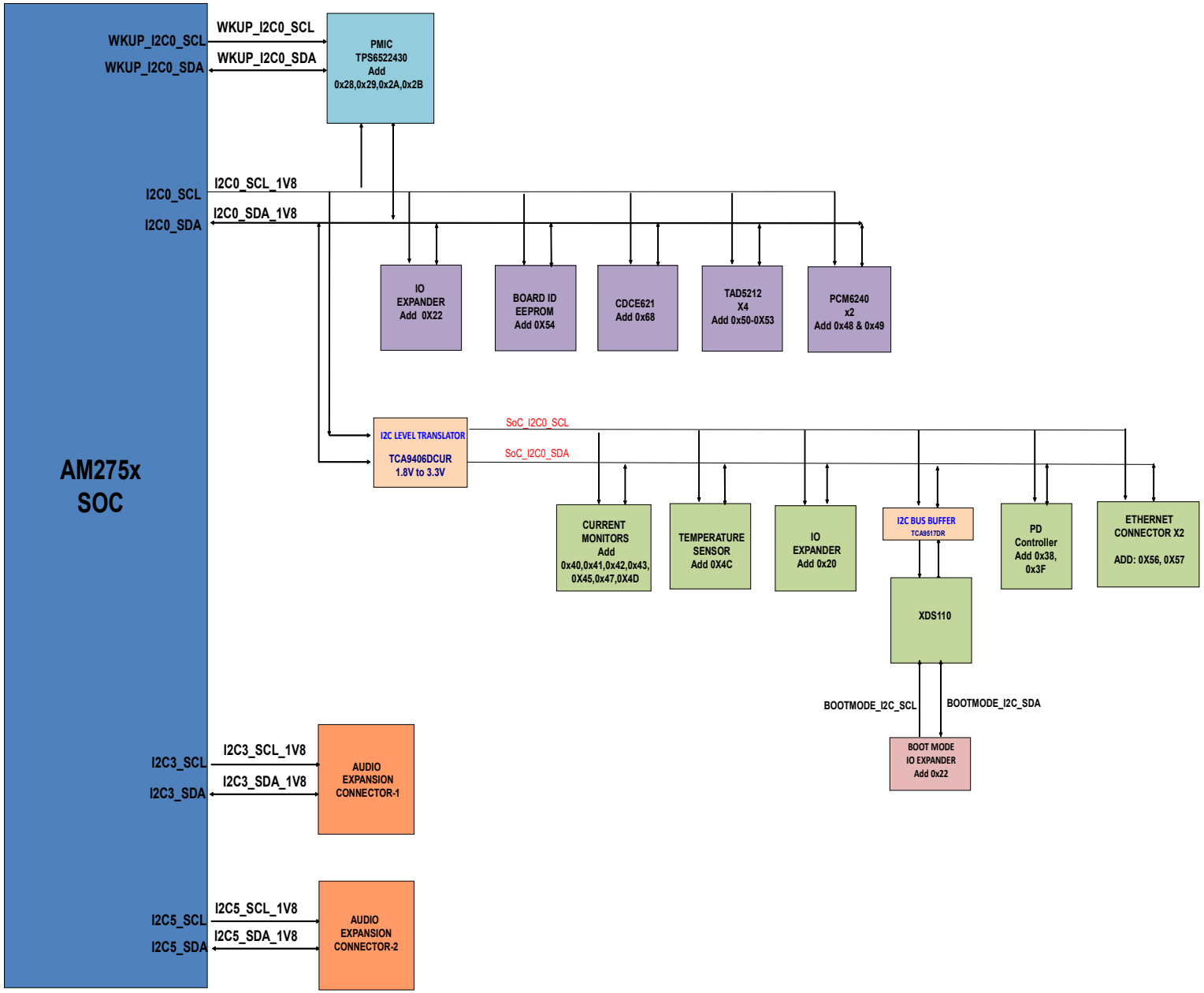
I2C TREE



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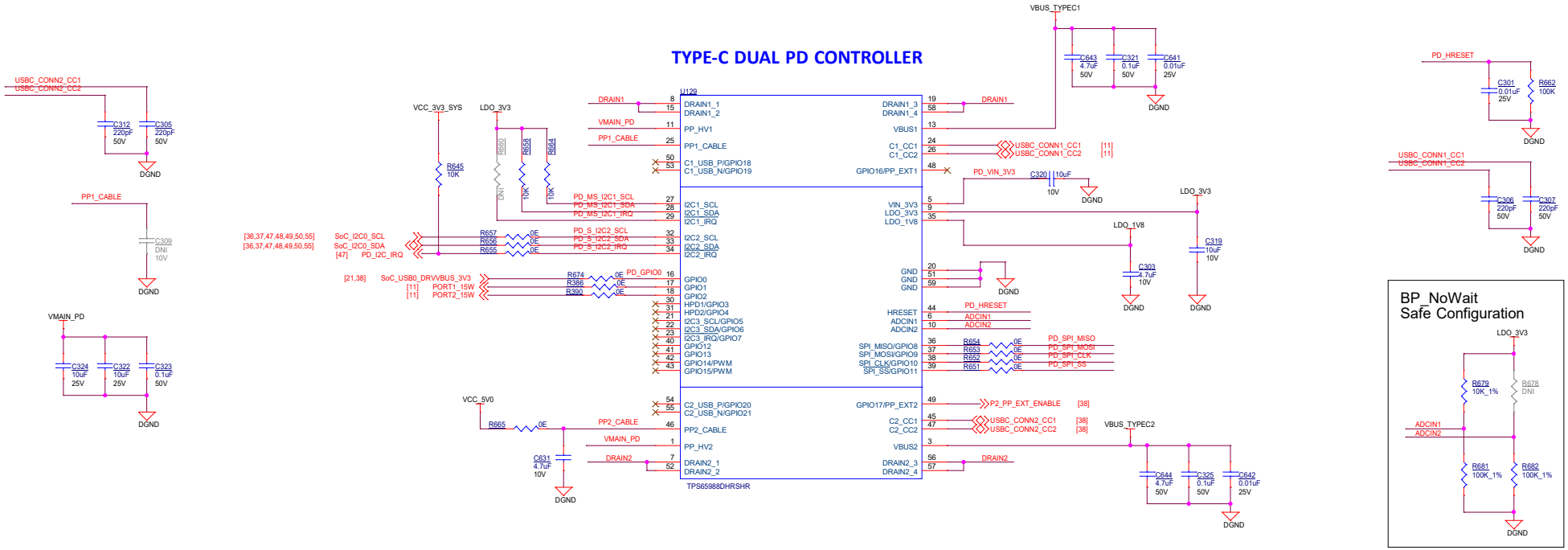
GPIO MAPPING TABLE

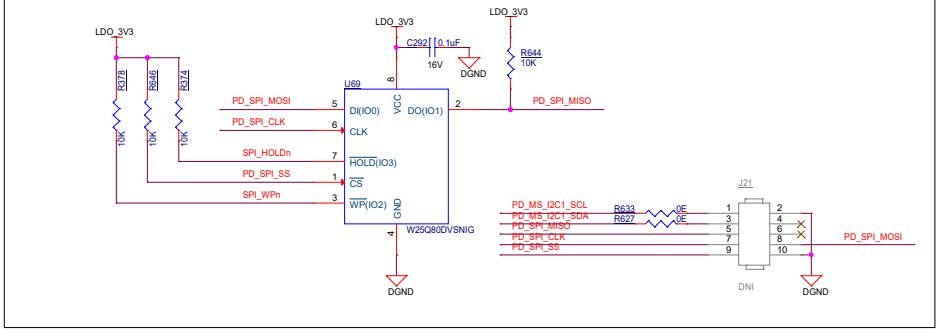
SL.No	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN	VOLTAGE RAIL CONNECTED
									ON SOC SIDE	ON SKEVM
1	User_Test_LED_1	SOC_GPIO0_38	GPIO	GPIO0_38	MCASP1_AXR3	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD1V8
2	User_interrupt	GPIO_MCU_SoC_INTn	GPIO	MCU_GPIO0_2	MCU_GPIO0_2	INPUT	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
3	PMIC SD/DDR voltage select, and EMMC/SD FET path select	VSEL_SD_SOC	VOLTAGE SELECTION	MCU_GPIO0_0	WKUP_TIMER_IO0	OUTPUT	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
4	Push button IORET WAKE	IORET_WAKE	GPIO	MCU_GPIO0_16	MCU_GPIO0_16	INPUT	HIGH	LOW	VDDSHV_CANUART	SOC_VDDSHV_CANUART
5	AEC conn 1 GPIO_0	AEC1_GPIO0_0	GPIO	MCU_GPIO0_15	MCU_GPIO0_15	NA	NA	NA	VDDSHV_CANUART	SOC_VDDSHV_CANUART
6	AEC conn 1 GPIO_1	AEC1_GPIO0_1	GPIO	GPIO0_12	OSPI0_CSn1	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
7	For PMIC interrupt	MCU_INTn	Interrupt	GPIO1_29	I2C1_SDA	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD1V8
9	User Interrupt IO Expander Interrupt	MCU_GPIO0_1_INTn	INTERRUPT	MCU_GPIO0_1	WKUP_TIMER_IO1	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD1V8
9	AEC conn 2 GPIO_0	AEC2_GPIO0_0	GPIO	MCU_GPIO0_4	MCU_GPIO0_4	NA	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
10	AEC conn 2 GPIO_1	AEC2_GPIO0_1	GPIO	MCU_GPIO0_3	MCU_GPIO0_3	NA	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
IO EXPANDER – 01										
1	RGMII2_RST	GPIO_CPSW2_RST	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	RGMII1_RST	GPIO_CPSW1_RST	ENABLE	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	MMC0 FET selection	MMC0_FET_EN	Peripheral selection	IO EXPANDER-P02		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	McASP4 FET selection	McASP4_FET_SEL	Peripheral selection	IO EXPANDER-P03		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	ENABLE	IO EXPANDER-P05		INPUT	HIGH	LOW		VCC_3V3_SYS
6	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P12		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	PCM1 RESET	GPIO_PCM1_RST	ENABLE	IO EXPANDER-P20		OUTPUT	HIGH	LOW		VCC1V8_SYS
2	PCM2 RESET	GPIO_PCM2_RST	ENABLE	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC1V8_SYS
3	Test GPIO from the XDS IC	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC1V8_TA
4	Audio ext refclk2 selection	AUDIO_EXT_REFCLK2_S0	Clock selection	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC1V8_SYS
5	Audio ext refclk2 selection	AUDIO_EXT_REFCLK2_S1	Clock selection	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC1V8_SYS
6	AEC 1 & 2 connector refclk selection	AEC1_REFCLK_SEL	Clock selection	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC1V8_SYS
7	AEC 1 & 2 connector refclk selection	AEC2_REFCLK_SEL	Clock selection	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC1V8_SYS
8	eMMC flash reset	GPIO_eMMC_RSTn	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC1V8_SYS
9	TCAN1043A enable	IO_MCAN0_EN	ENABLE	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VDDSHV_CANUART
10	TCAN1043A STB control	IO_MCAN0_STB#	MODE SELECTION	IO EXPANDER-P13		OUTPUT	HIGH	LOW		VDDSHV_CANUART
11	UART2 FET selection	UART2_FET_SEL	Peripheral selection	IO EXPANDER-P14		OUTPUT	LOW	HIGH		VCC1V8_SYS
12	UART3 FET selection	UART3_FET_SEL	Peripheral selection	IO EXPANDER-P15		OUTPUT	LOW	HIGH		VCC1V8_SYS
13	PCM6240_INT	PCM1_INT_1V8	INTERRUPT	IO EXPANDER-P16		INPUT	NA	HIGH		VCC1V8_SYS
14	PCM6240_INT	PCM2_INT_1V8	INTERRUPT	IO EXPANDER-P17		INPUT	NA	HIGH		VCC1V8_SYS
15	uSD interface voltage enable	MMC0_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC1V8_SYS
16	VPP supply enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC1V8_SYS

USB TYPE-C POWER



I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

SPI EEPROM & PROGRAMMING HEADER



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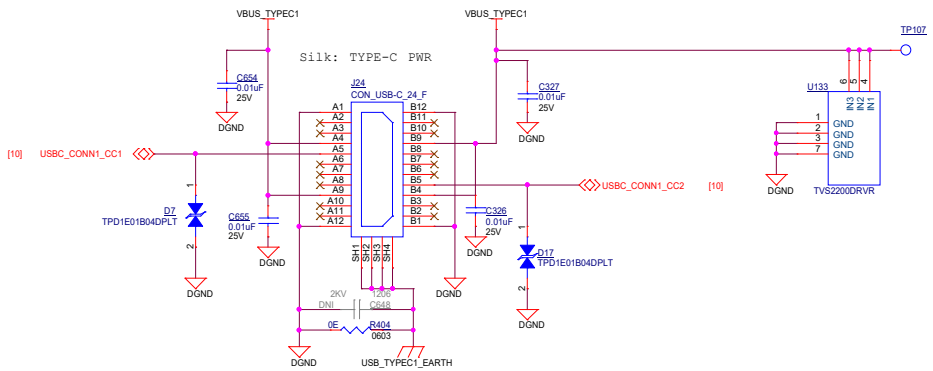
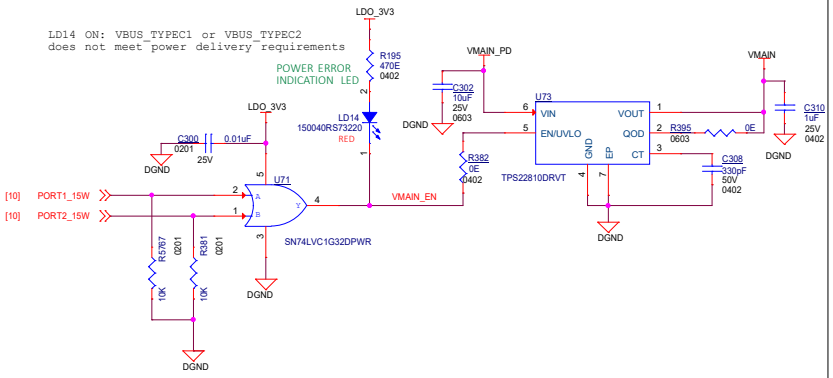
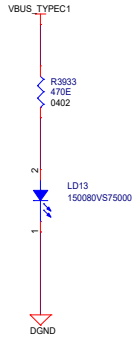
USB TYPE-C POWER CONNECTOR



LOAD SWITCH FOR VMAIN



POWER INDICATION LED: VBUS_TYPEC1



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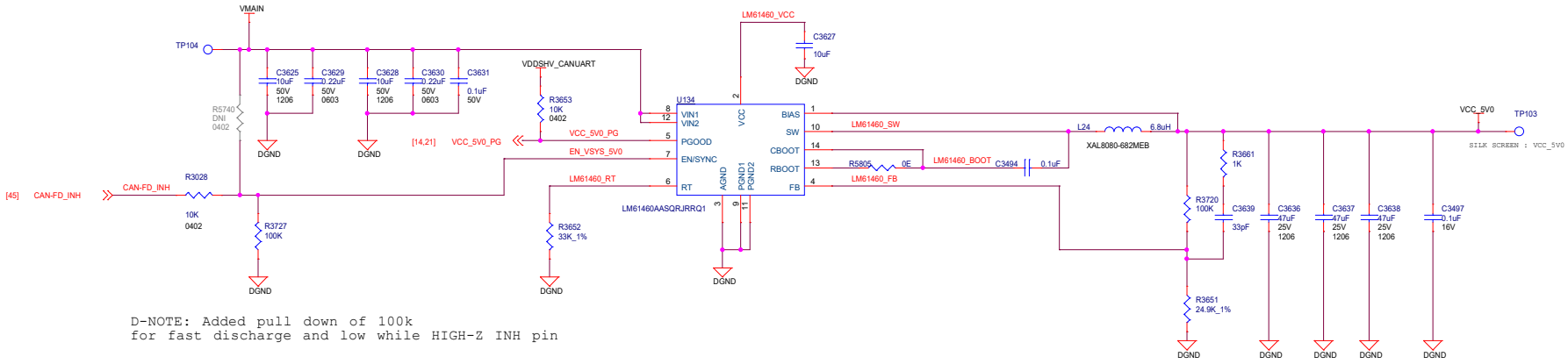
PERIPHERAL POWER SUPPLY - 1

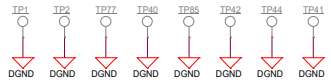
5V, 6.0 AMPS SUPPLY

LM61460-Q1 5V BUCK REGULATOR
VinMin = 5V
VinMax = 15V
Vout = 5V
Iout = 6A



D-NOTE: Added pull down of 100k
for fast discharge and low while HIGH-Z INH pin

GND TEST POINTS



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Title	PERIPHERAL POWER SUPPLY		
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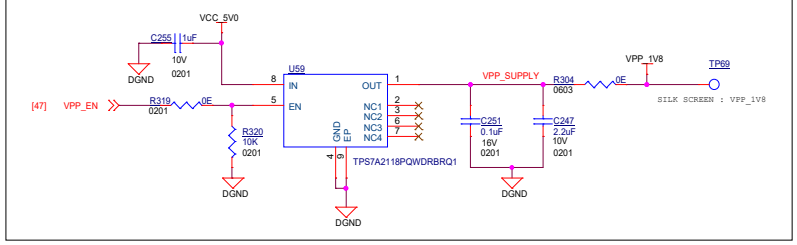
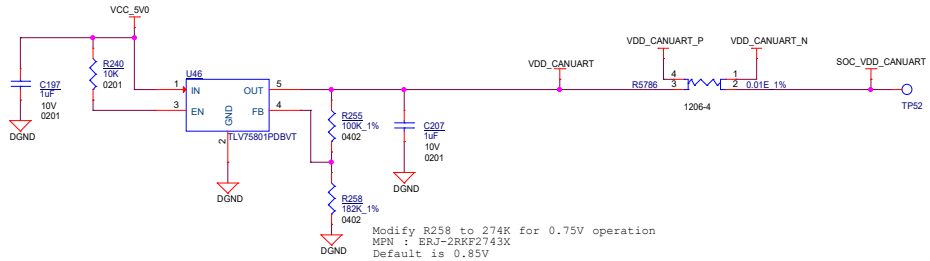
PRE REGULATOR SUPPLY - LDOs

1.8V VPP (eFUSE), 0.5AMPS SUPPLY

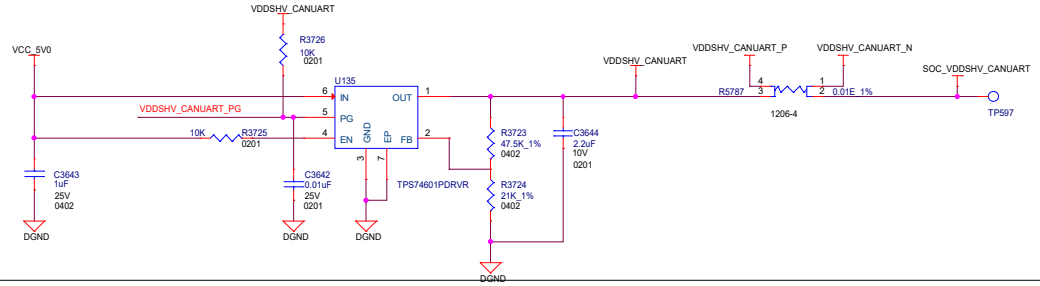


D-NOTE:U59 only needed for eFUSE ROM programming. If no OTP operation, VPP can be left unconnected.

VDD_CANUART(0.85V),0.5 AMPS SUPPLY



VDDSHV_CANUART(1.8V),1 AMPS SUPPLY



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Title	SOC POWER SUPPLIES - LDOs & VCC_3V3_SYS LOAD SWITCH		
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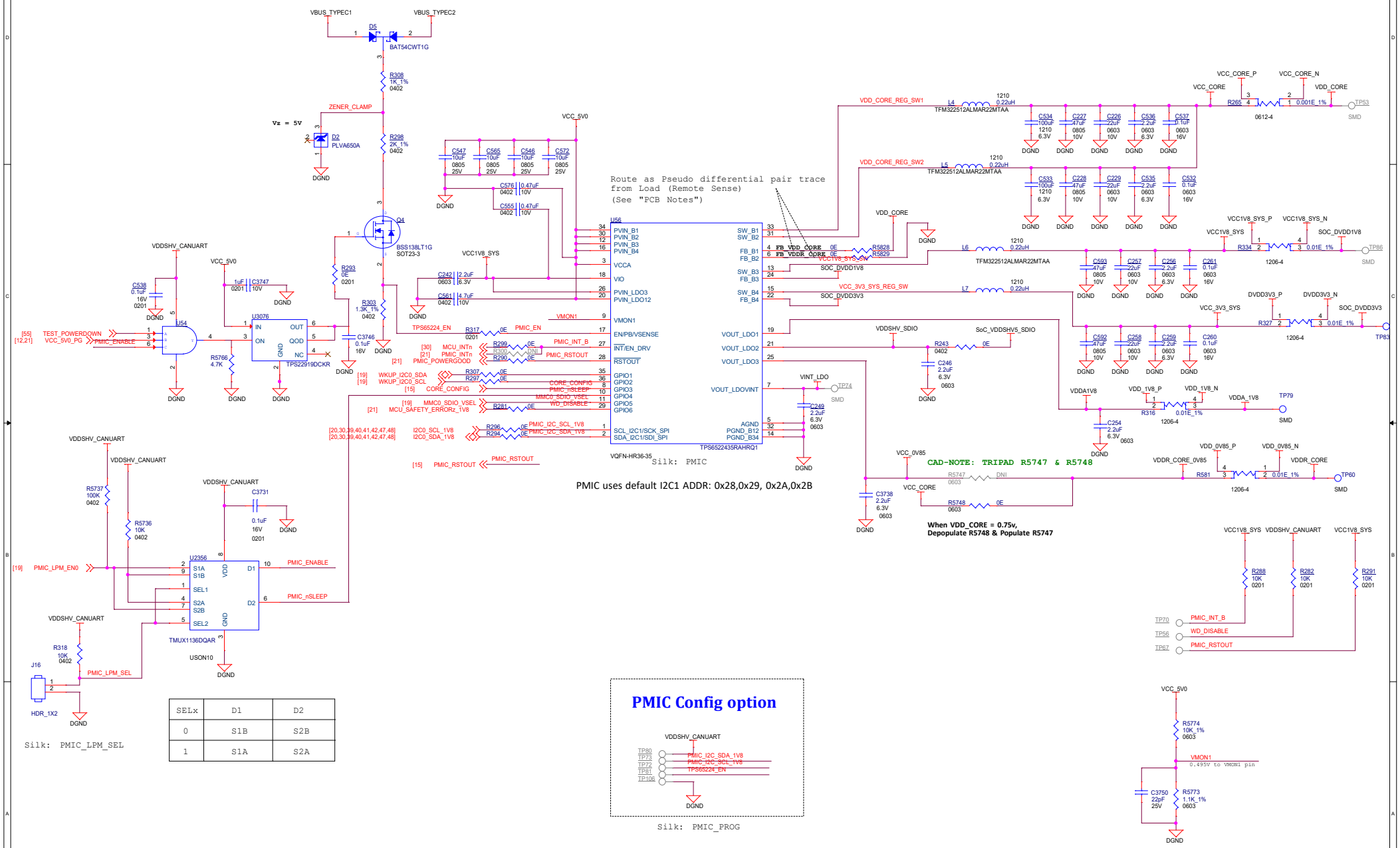
SOC POWER SUPPLY PMIC - 1



SELx	D1	D2
0	S1B	S2B
1	S1A	S2A

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Title	SOC POWER SUPPLY PMIC - 1	
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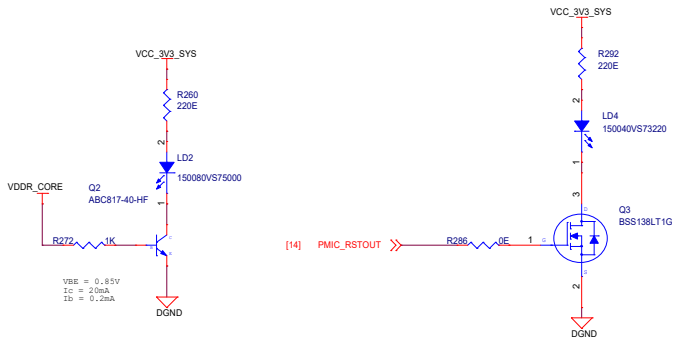
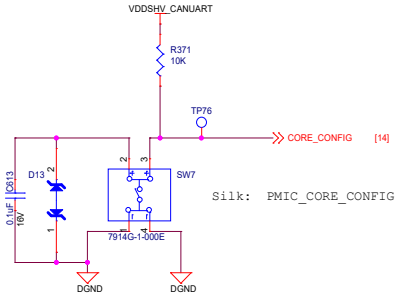
SOC POWER SUPPLY PMIC - 2

PMIC POWER INDICATION LED



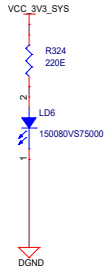
PMIC PUSH BUTTON LOGIC



Note: When R371 is DNI, Push Button (SW7) becomes operational through internal pullup on PMIC GPIO5

R371	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

POWER INDICATION LED: VCC_3V3_SYS



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Title	SOC POWER SUPPLY PMIC - 2		
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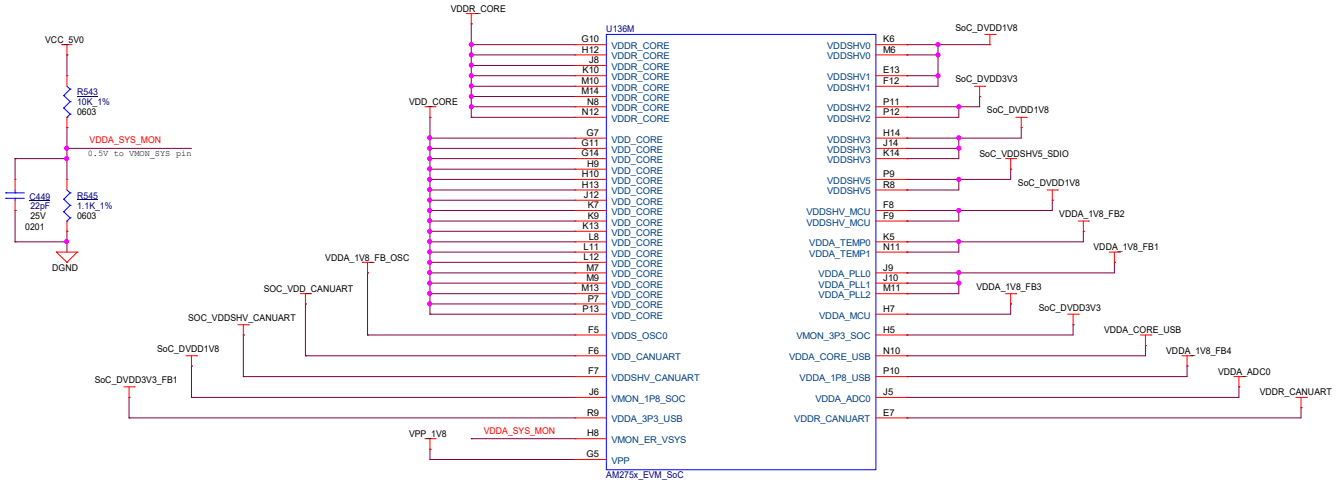
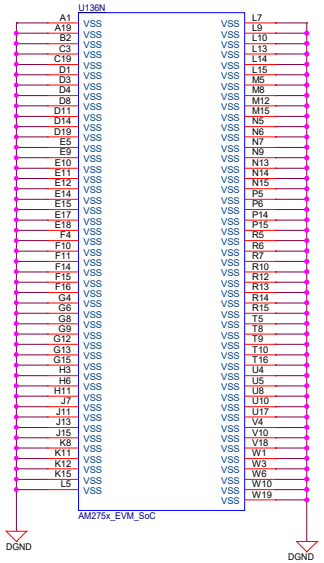
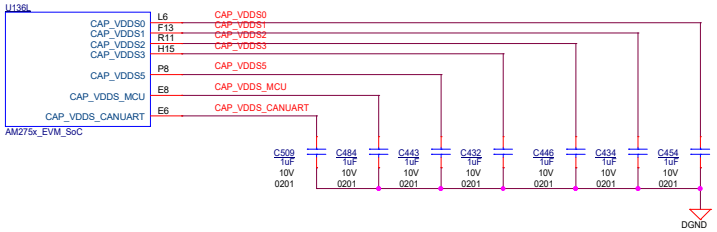
SOC POWER SUPPLIES AND SUPPLY RAILS



SOC VSS





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Title	SOC POWER SUPPLIES, SUPPLY RAILS AND SOC GROUND VSS		
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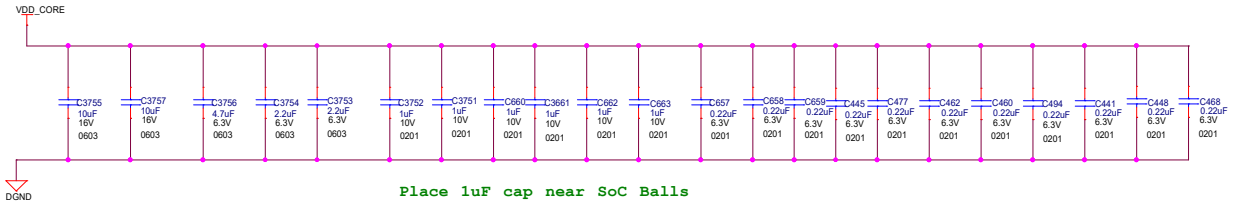
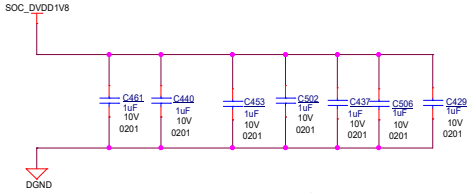
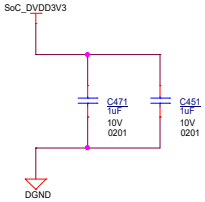
SOC POWER SUPPLIES - DECAPS 1



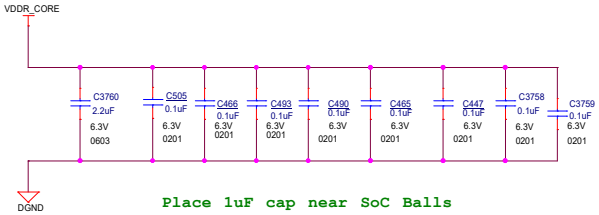
Place 1uF cap near SoC Balls



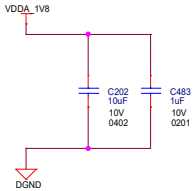
Place 1uF cap near SoC Balls



Place 1uF cap near SoC Balls



Place 1uF cap near SoC Balls



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Title	SOC POWER SUPPLIES - DECAPS 1		
Size C	PROC190A		Rev
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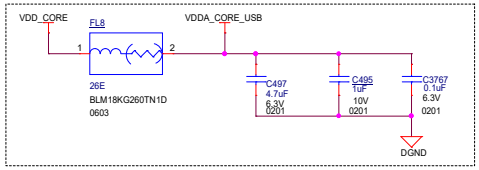
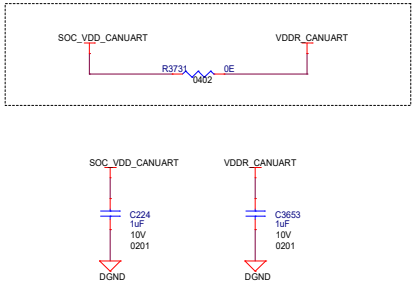
SOC POWER SUPPLIES - DECAPS 2

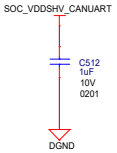
Peripherals - Core SUPPLY



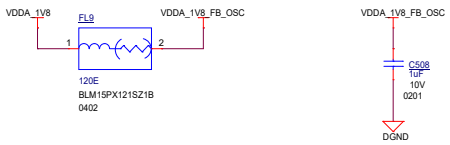
VDDR_CANUART SUPPLY

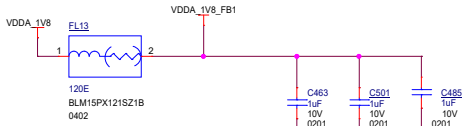


VDDSHV_CANUART SUPPLY

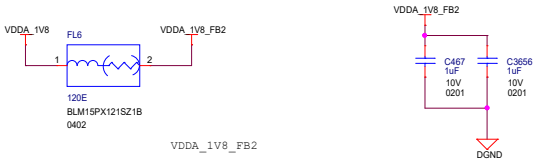


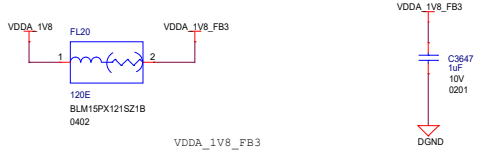
Peripherals - 1.8V Analog SUPPLY

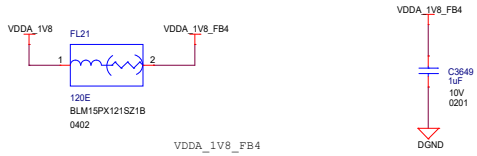


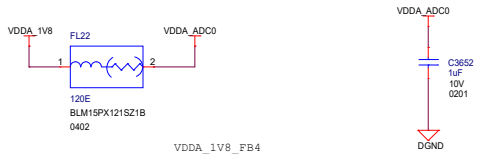


BLM15PX121SN1D :- 120E
2A @ 85 deg C
1.1A @ 125 deg C



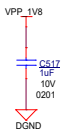




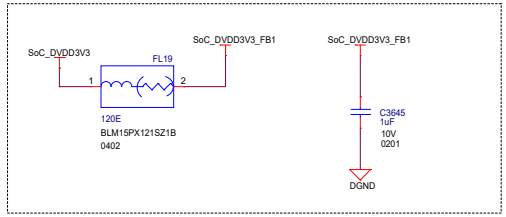


3.3V/1.8V MMC0 SUPPLY

VPP_1V8



Peripherals - 3.3V Analog SUPPLY



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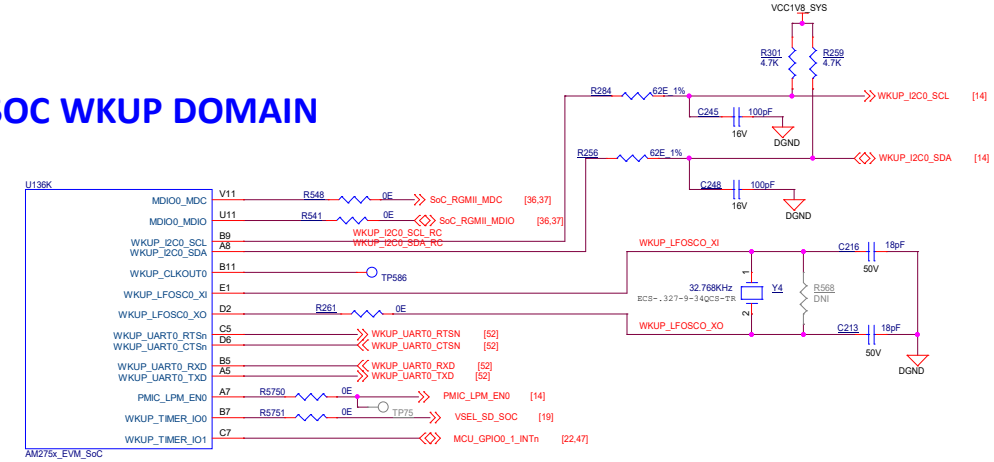
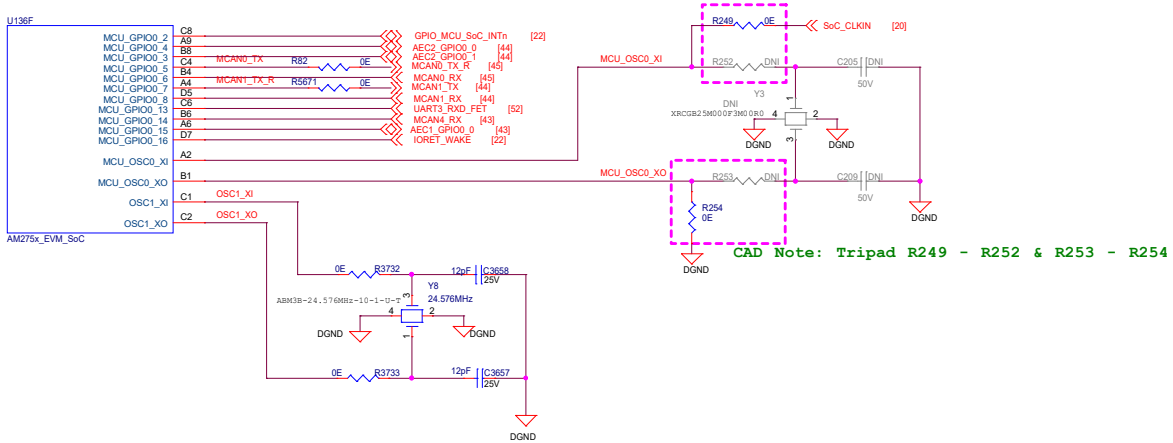
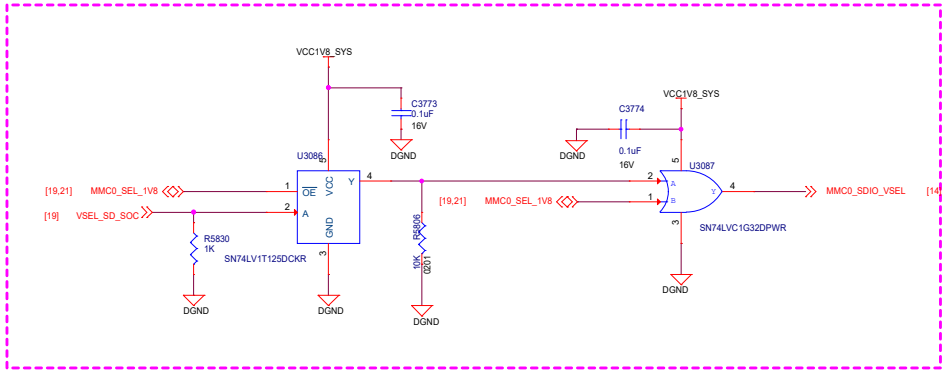
SOC WKUP DOMAIN



SOC GPIO





MMC0_SEL_1V8	VSEL_SD_SOC	MMC0_SDIO_VSEL	VDDSHV_SDIO	
0	0	0	3V3	3V3 IO routed to uSD
0	1	1	1V8	1V8 IO routed to uSD
1 (DEFAULT)	X	1	1V8	1V8 IO routed to EMMC

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Texas Instruments MISTRAL

Title	SOC WKUP & CLOCK	
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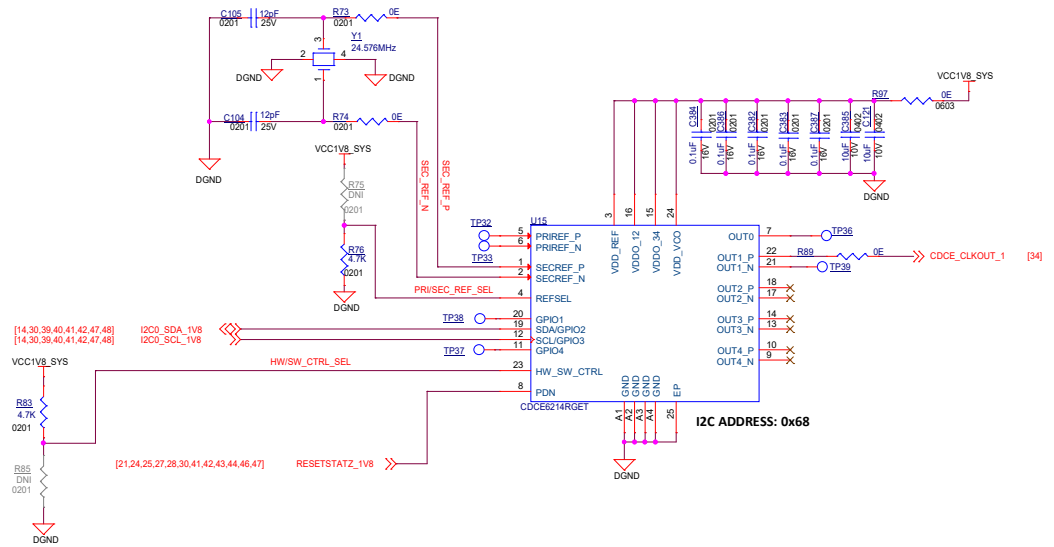
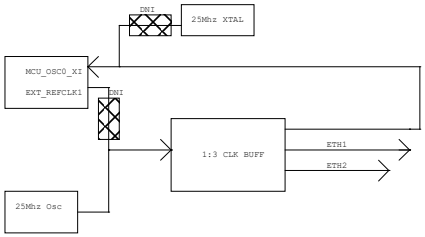
CDCE CLOCK GENERATION

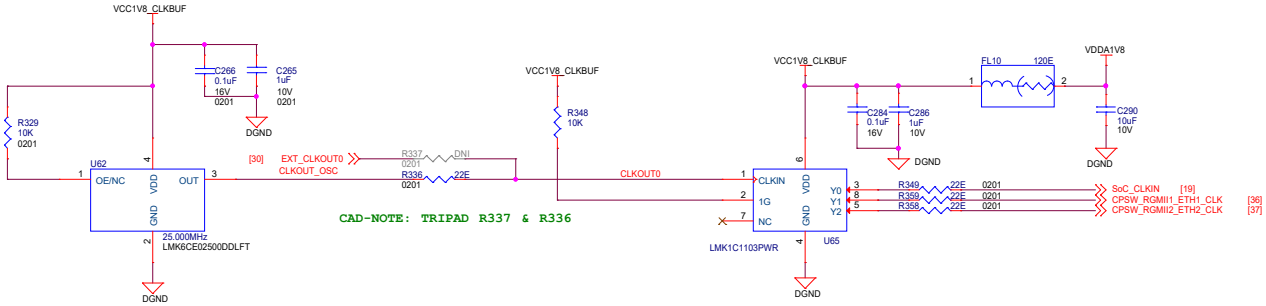


HW/SW CTRL SEL / PRI/SEC_REF_SEL	PAGE_SELECT	CLOCK_SOURCE
LOW	PAGE 0	SEC_REF
HIGH	PAGE 1	PRI_REF

OSCILLATOR



SOC & ETHERNET PHY CLOCK BUFFER



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Title	CDCE CLOCK GENERATION	
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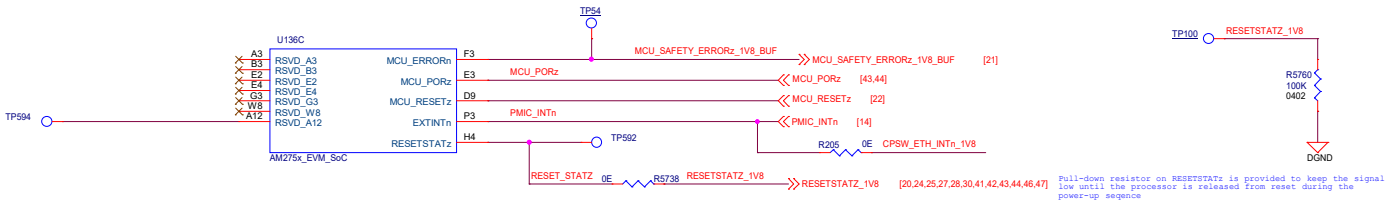
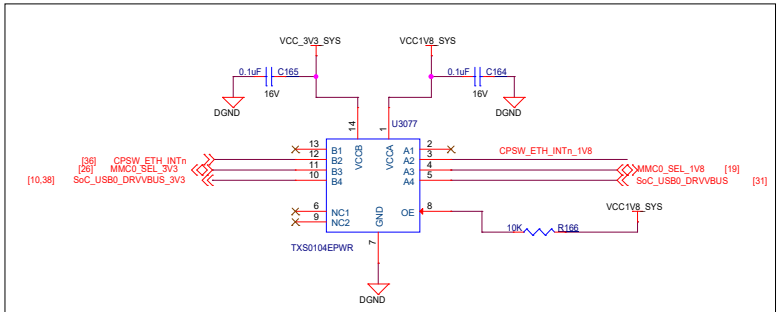
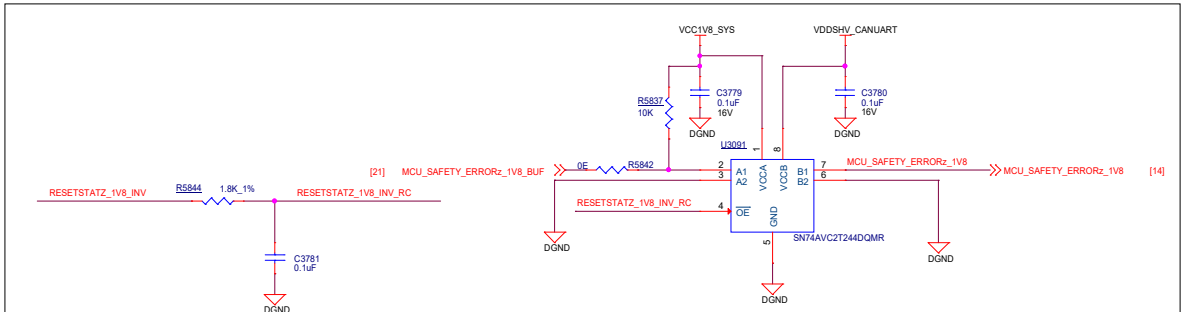
SOC RESET - 1

SOC - RESET

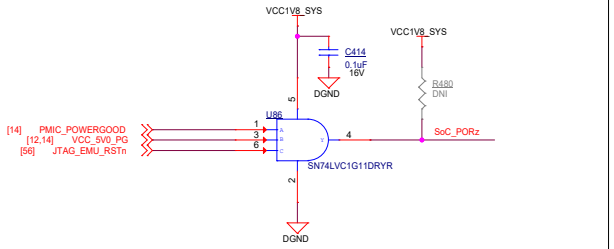




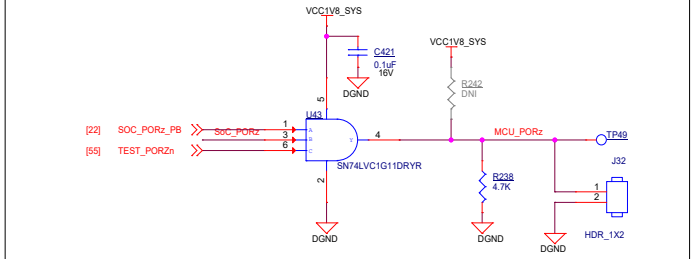
LEVEL TRANSLATOR

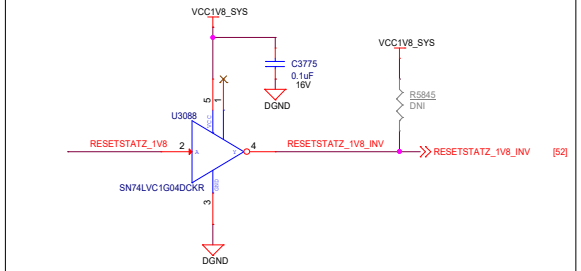


SOC POWER ON RESET



MCU POWER ON RESET





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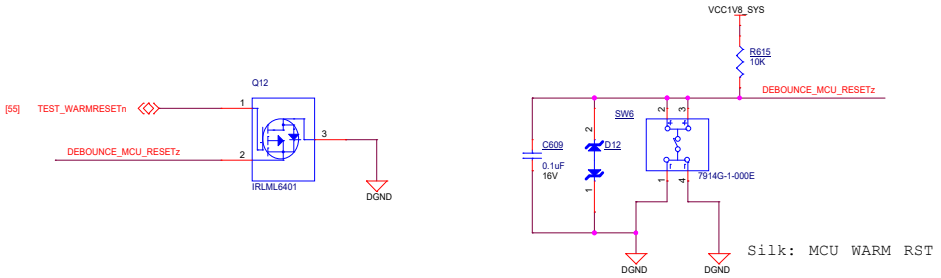
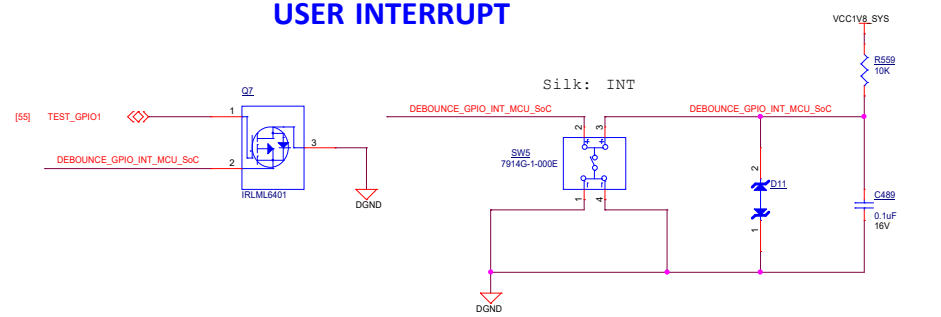
SOC RESET - 2

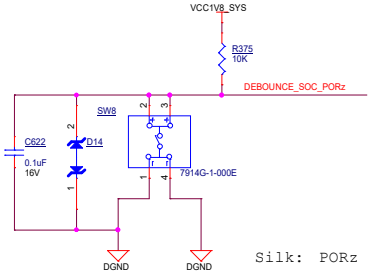
MCU WARM RESET



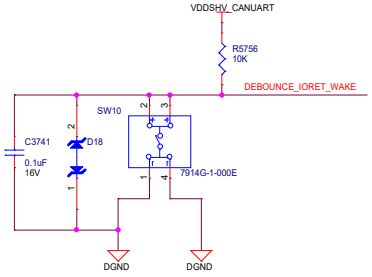
USER INTERRUPT



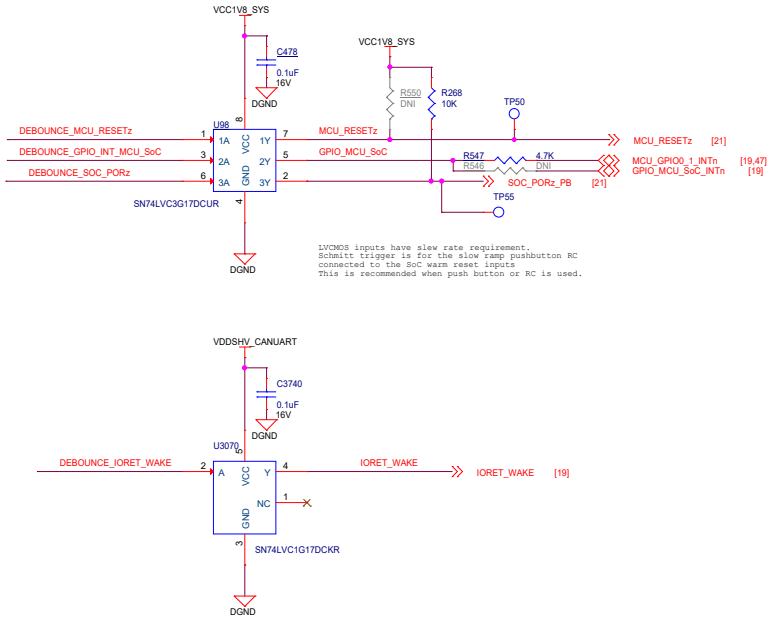
SOC PORZ



IO RET WAKE



RESET & INT DEBOUNCE CIRCUIT



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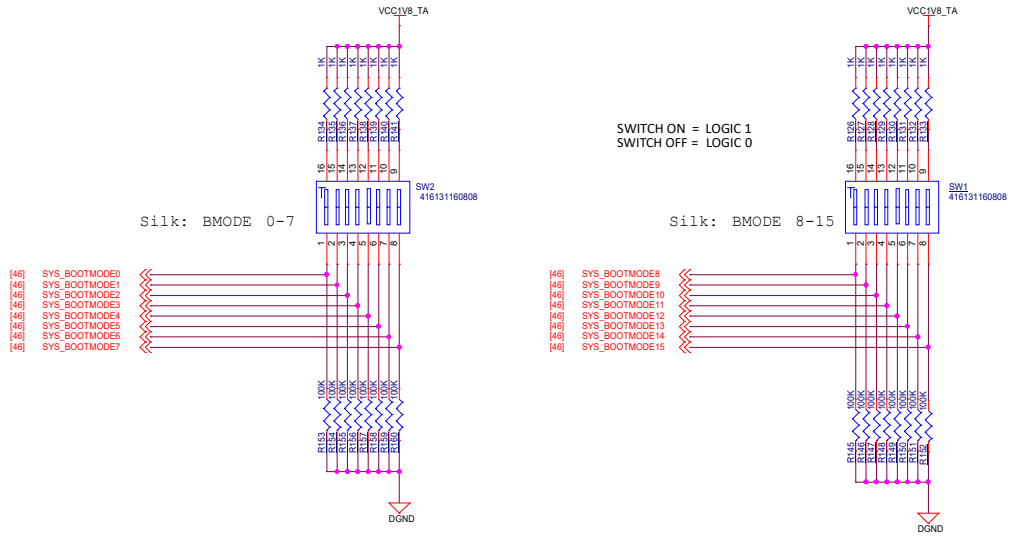
BOOT MODE SWITCHES

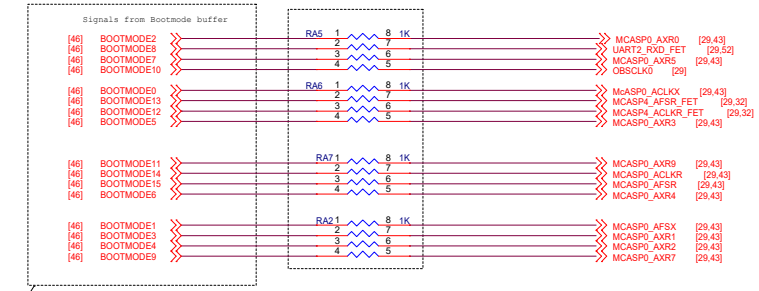
D-Note: VCC1V8_TA supply is used for test automation.
Connect SoC_DVDD1V8in the custom board design when buffers are not used



BOOT MODES SUPPORTED

1. OSPI
2. MMC0 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

BOOTMODE PINS



D-Note :
Connect SYS_BOOTMODE signals when bootmode buffers are not used

D-NOTE:
1. 1K Resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions
2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

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Title	BOOT MODE SWITCHES		
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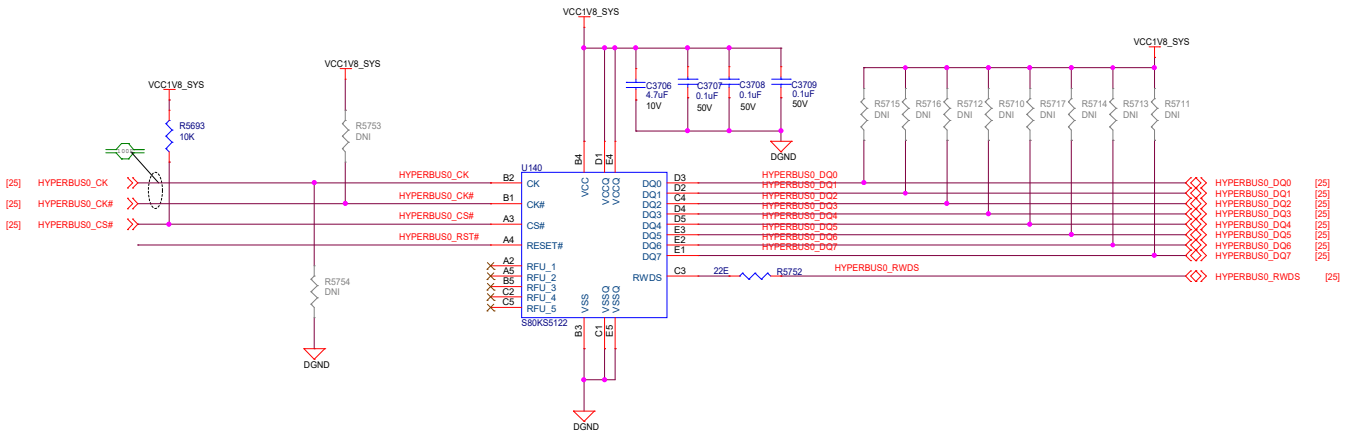
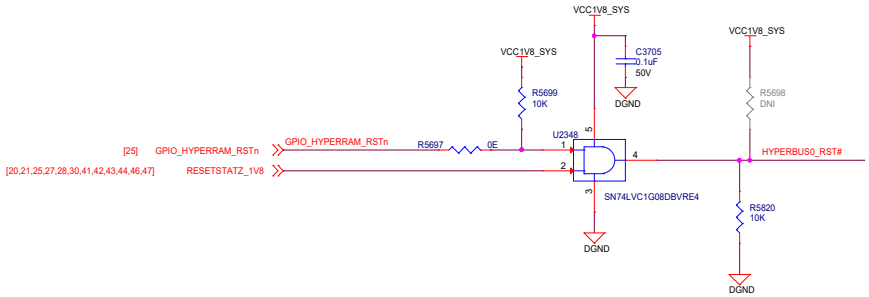
HYPERRAM DEVICE



HYPERRAM RESET



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Title	HYPERRAM INTERFACE		
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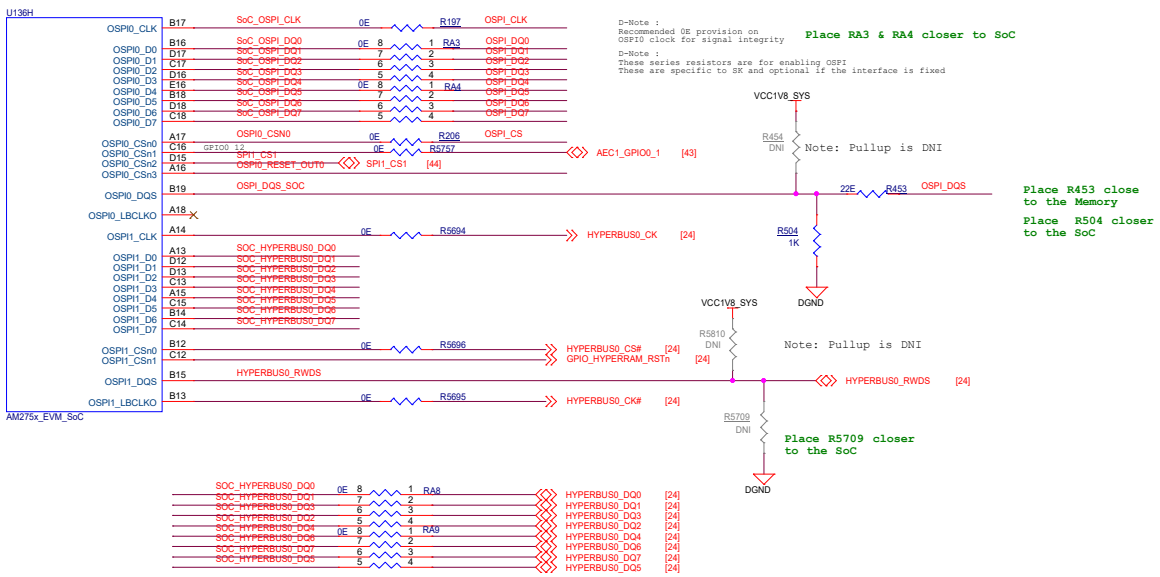
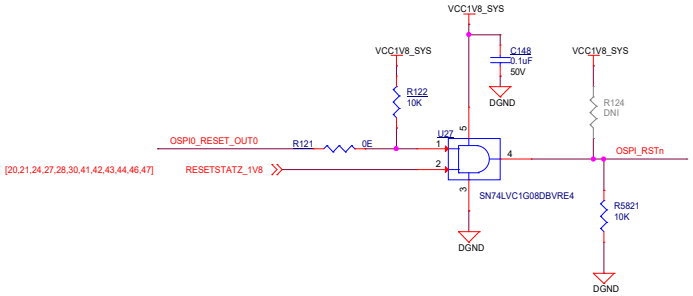
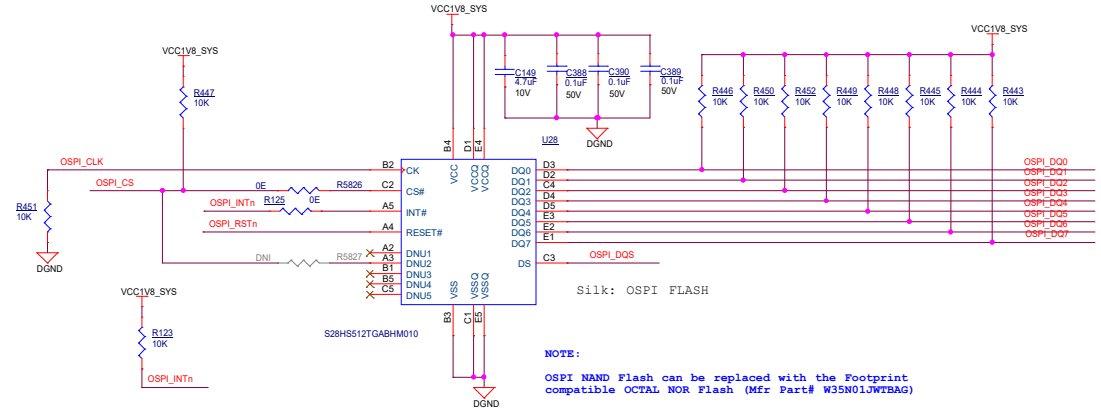
OSPI INTERFACE



OSPI FLASH RESET



OSPI FLASH



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Title	OSPI INTERFACE	
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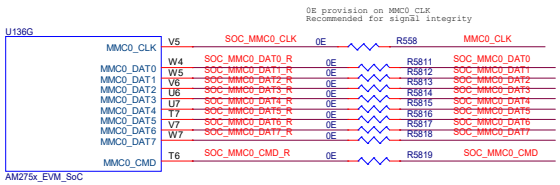
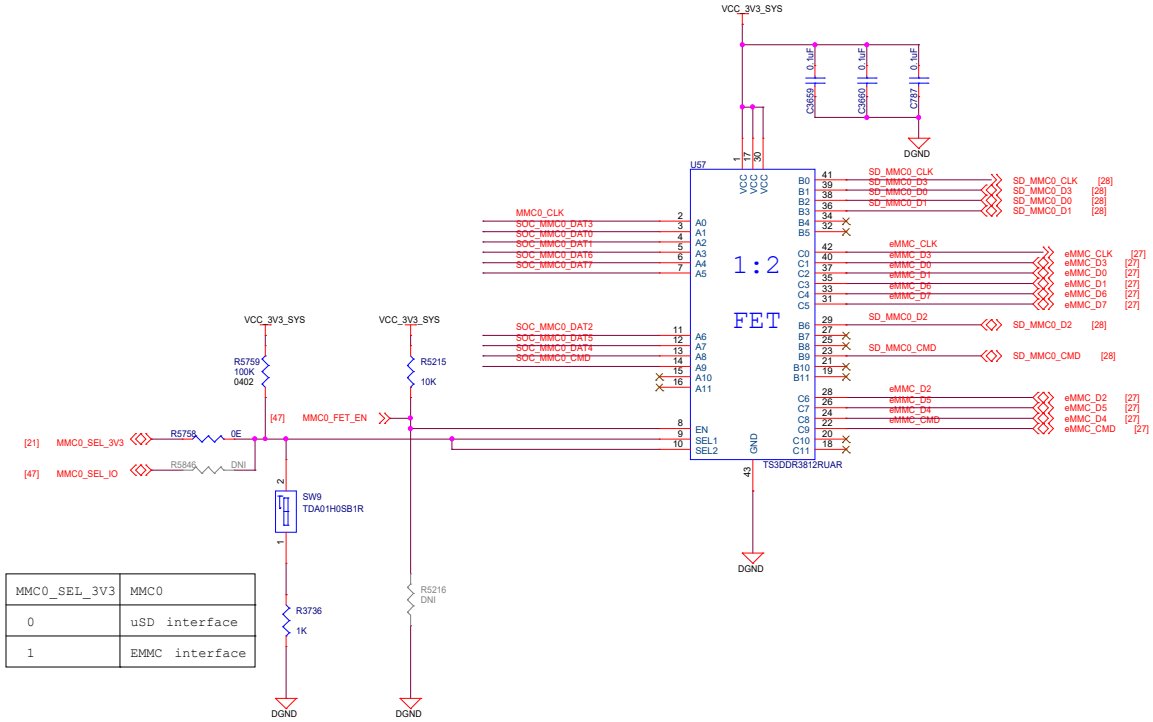
MMC0 INTERFACE



MMC0 INTERFACE FET SELECTION



MMC0_SEL_3V3	MMC0
0	uSD interface
1	EMMC interface

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Title	MMC0 INTERFACE		
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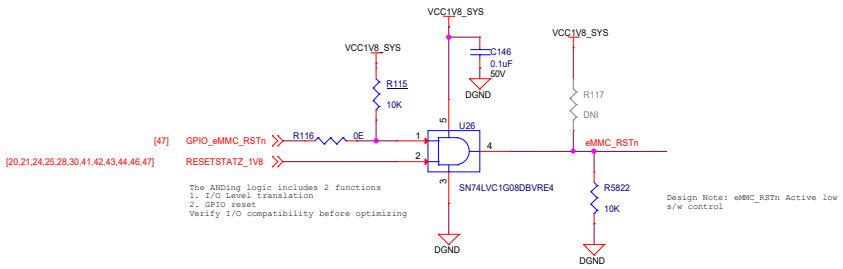
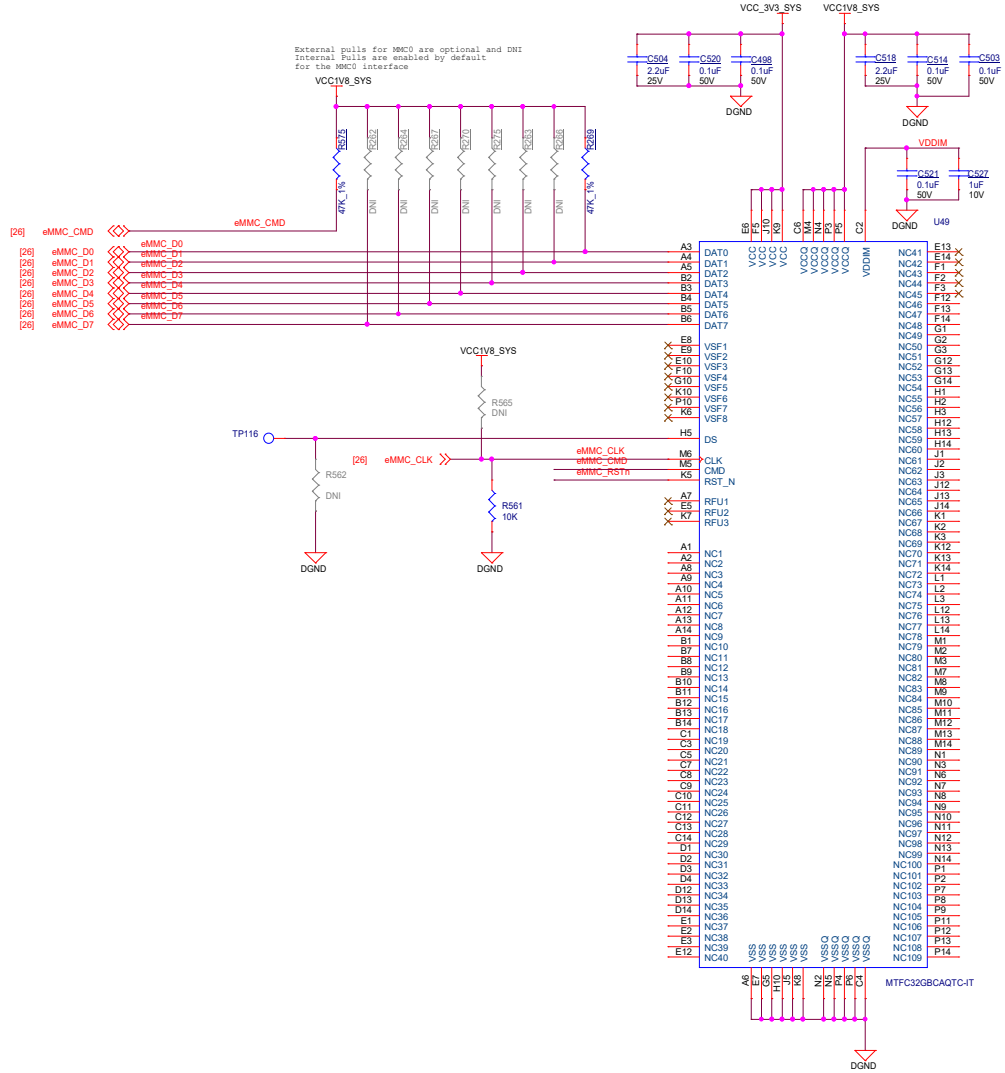
eMMC FLASH

eMMC FLASH RESET





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Title	eMMC FLASH AND RESET	
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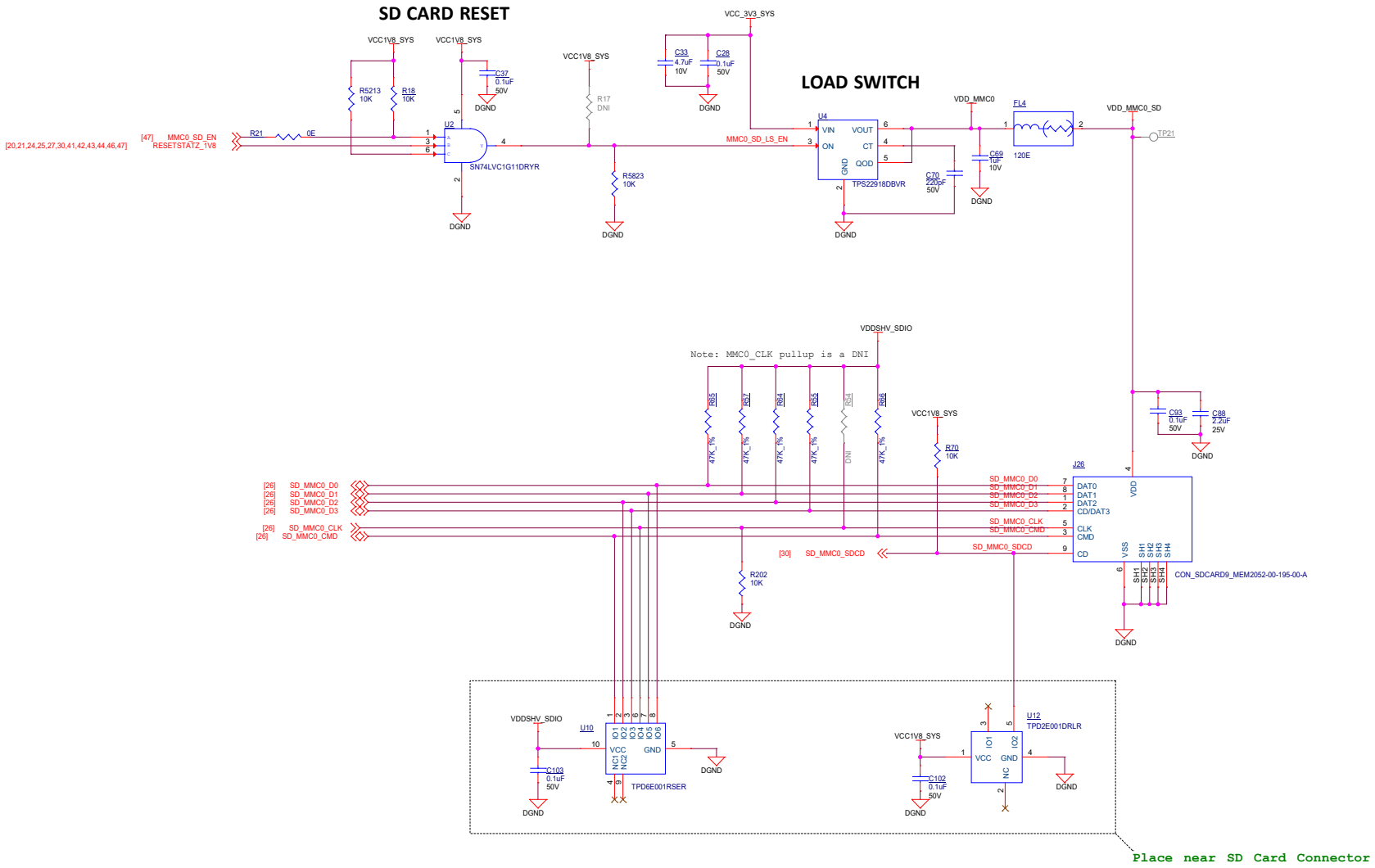
SD CARD INTERFACE



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Title	SD CARD INTERFACE	
Size C	PROC190A	Rev A
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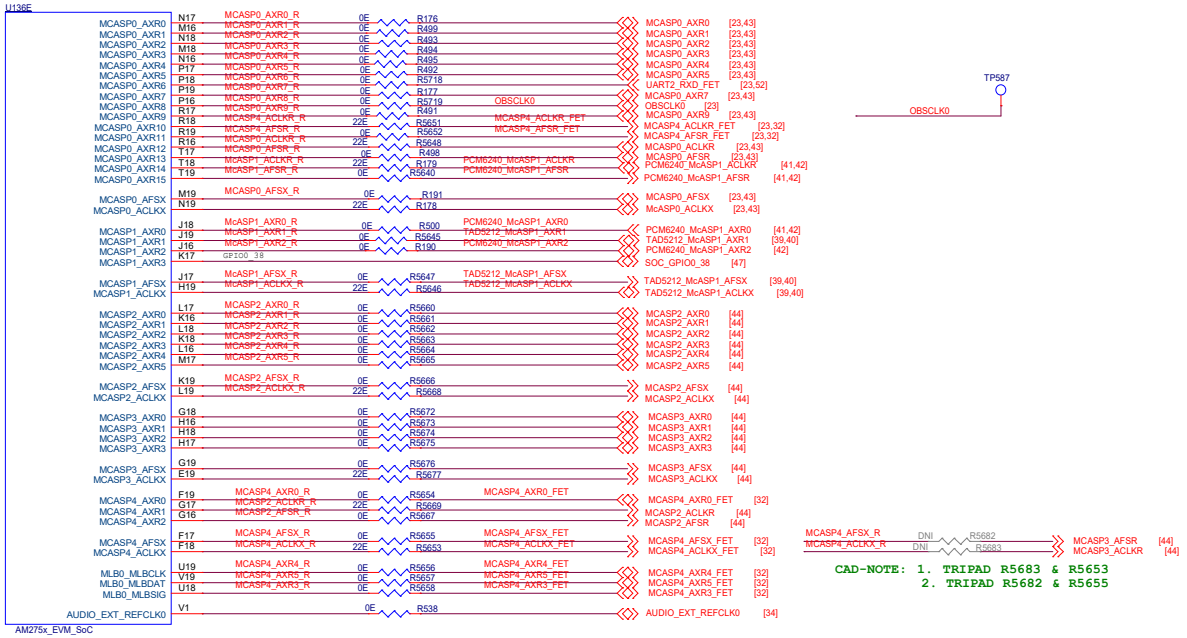
SOC McASP



CAD-NOTE: 1. TRIPAD R5683 & R5653
2. TRIPAD R5682 & R5655

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Title	SOC PERIPHERALS 1		
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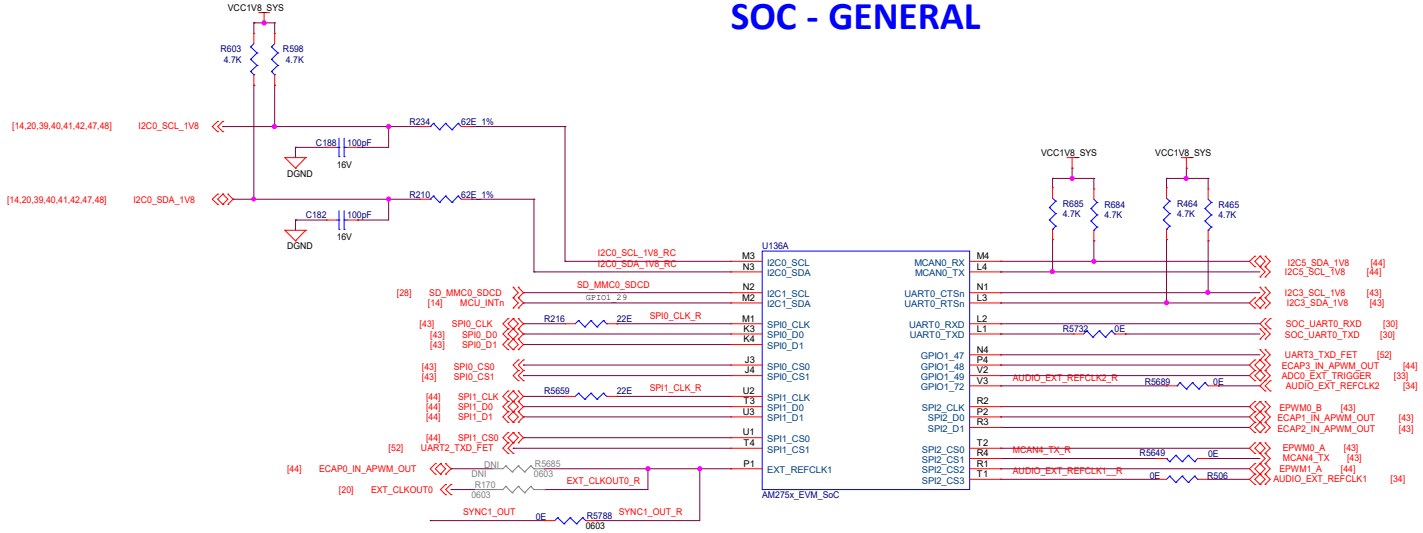
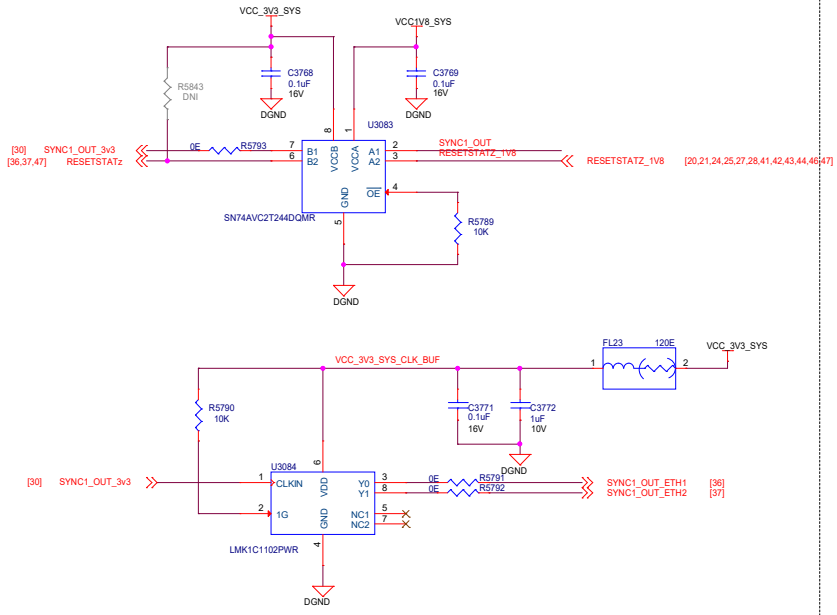
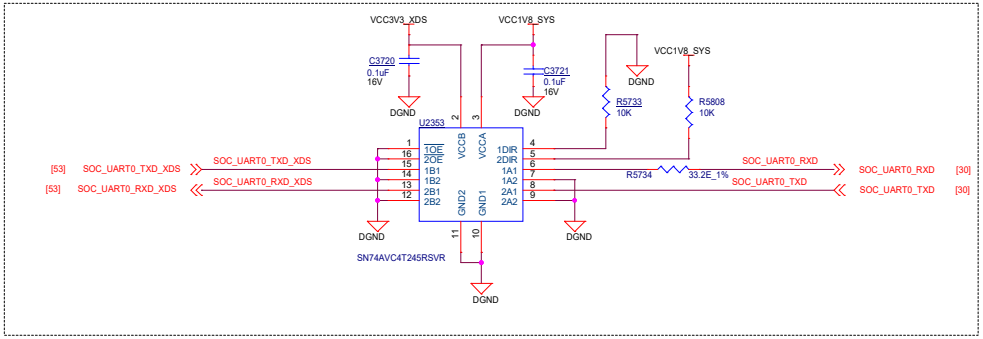
SOC - GENERAL



CAD-NOTE: TRIPAD R5685, R170 & R5788





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Title	SOC PERIPHERALS 2		
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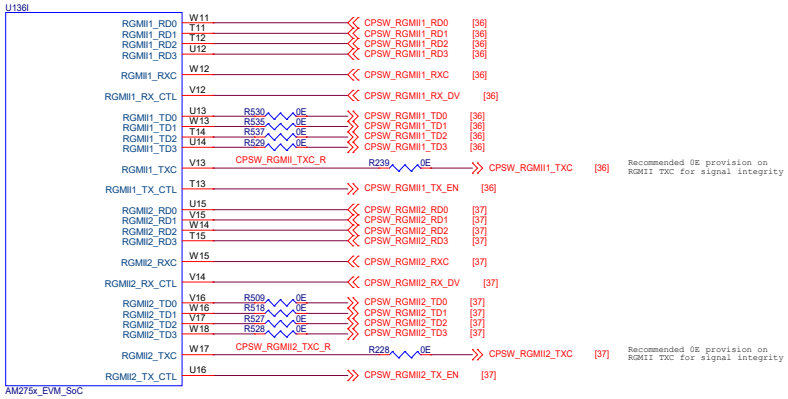
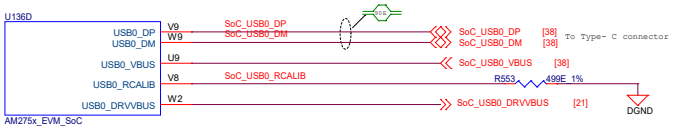
SOC CPSW3G ETHERNET INTERFACE



SOC - USB



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Title	SOC PERIPHERALS 3		
Size C	PROC190A		Rev A
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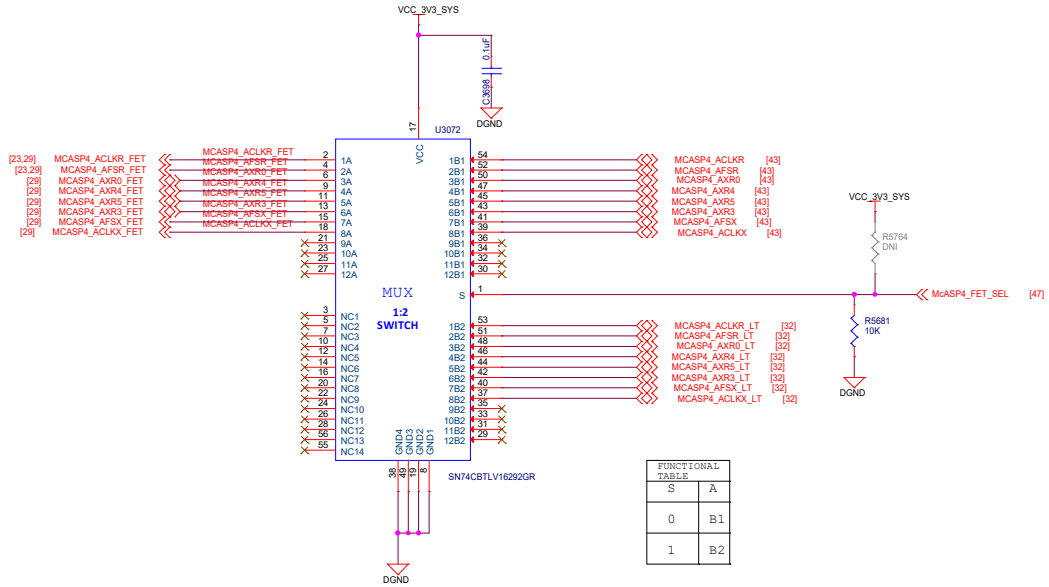
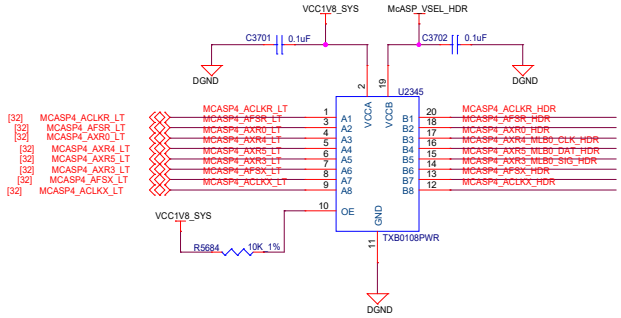
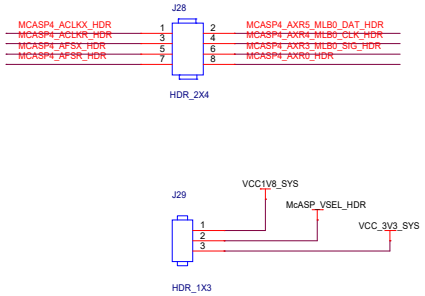
McASP4 FET SELECTION



FUNCTIONAL TABLE	
S	A
0	B1
1	B2





McASP HEADER 3.3/1.8 VOLTAGE SELECTION

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Title	McASP4 FET SELECTION & MLB HEADER	
Size C	PROC190A	Rev A
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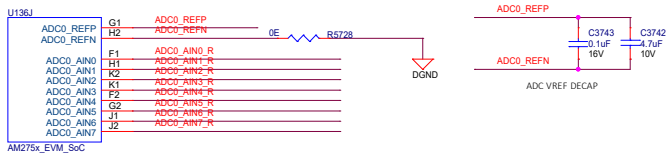
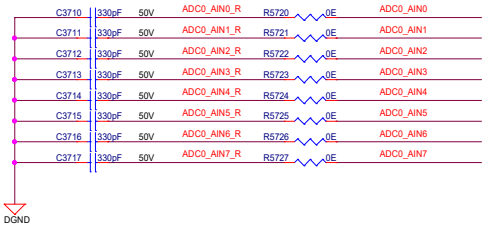
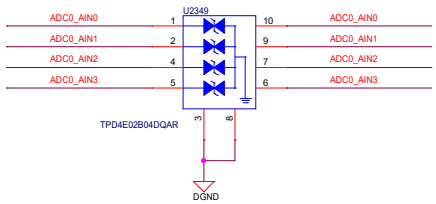
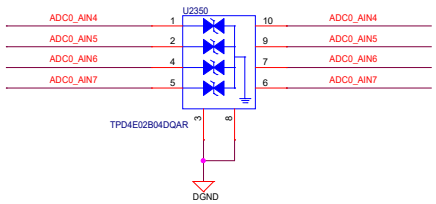
SOC ADC

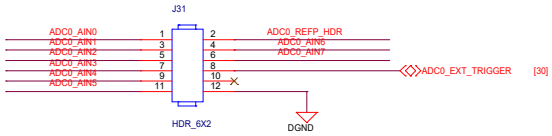


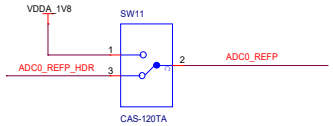


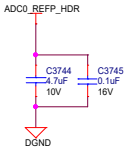




ADC EXT HEADER







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Title	SoC ADC0 INTERFACE AND HEADER		
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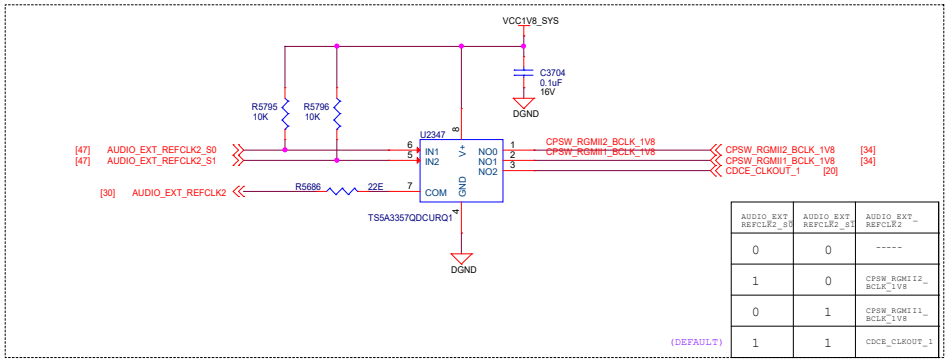
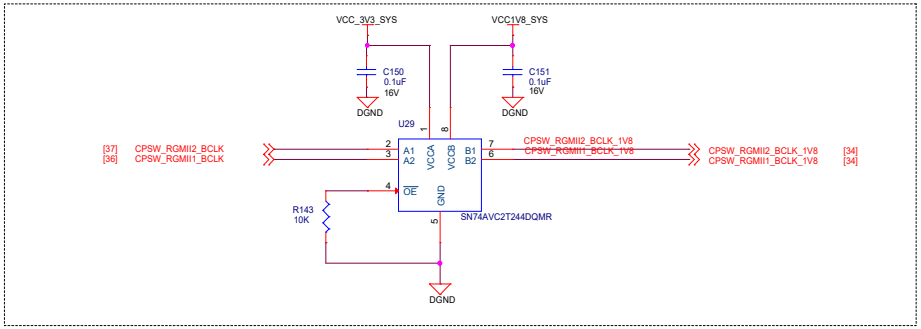
AUDIO_EXT_REFCLK2_SELECTION

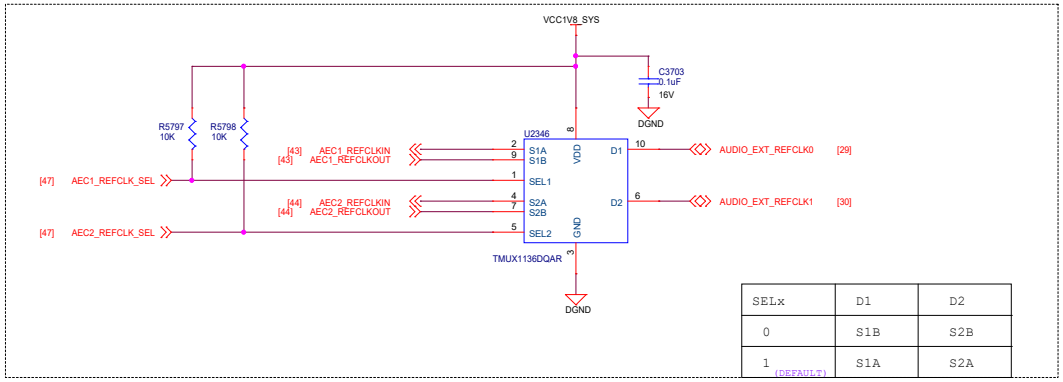


AUDIO_EXT_REFCLK2_S0	AUDIO_EXT_REFCLK2_S1	AUDIO_EXT_REFCLK2
0	0	-----
1	0	CPSW_RGMII2_BCLK_1V8
0	1	CPSW_RGMII1_BCLK_1V8
1 (DEFAULT)	1	CDCE_CLKOUT_1

ETHERNET_BCLK LEVEL TRANSLATOR



AUDIO EXPANSION REFCLK



SELx	D1	D2
0	S1B	S2B
1 (DEFAULT)	S1A	S2A

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Title	AUDIO REFERENCE CLOCK	
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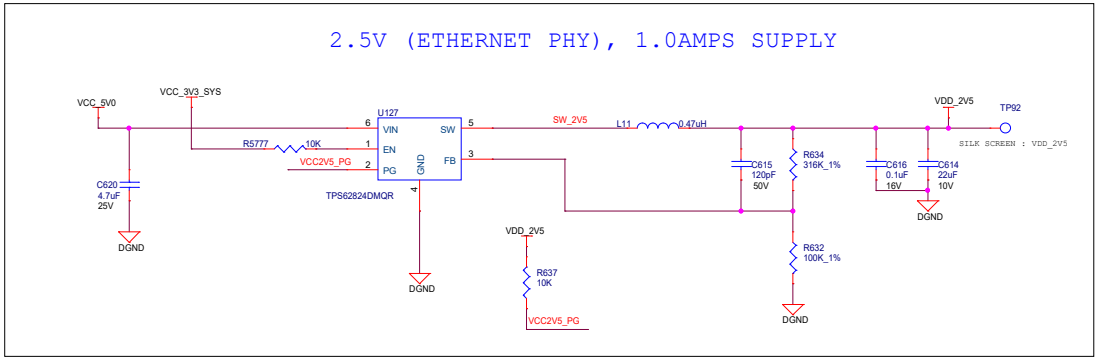
POWER SUPPLY (CORE) FOR ETHERNET PHY



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Title	ETHERNET PHY POWER SUPPLY		
Size C	PROC190A		Rev A
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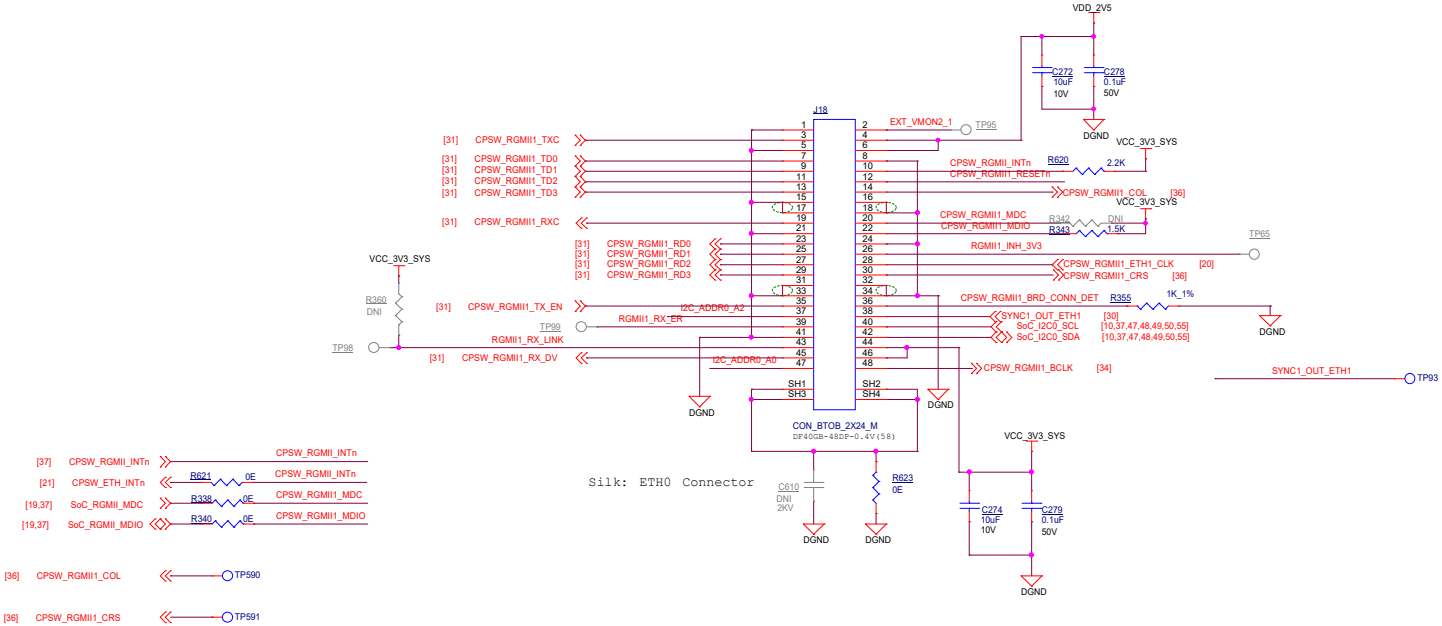
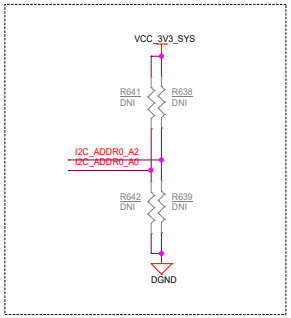
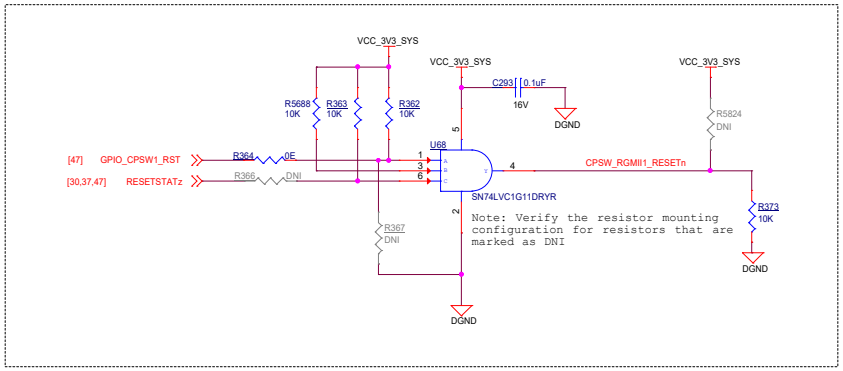
ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 1



I2C Address Strap



CPSW3G RGMII 1 RESET



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Title	ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 1		
Size C	PROC190A		Rev A
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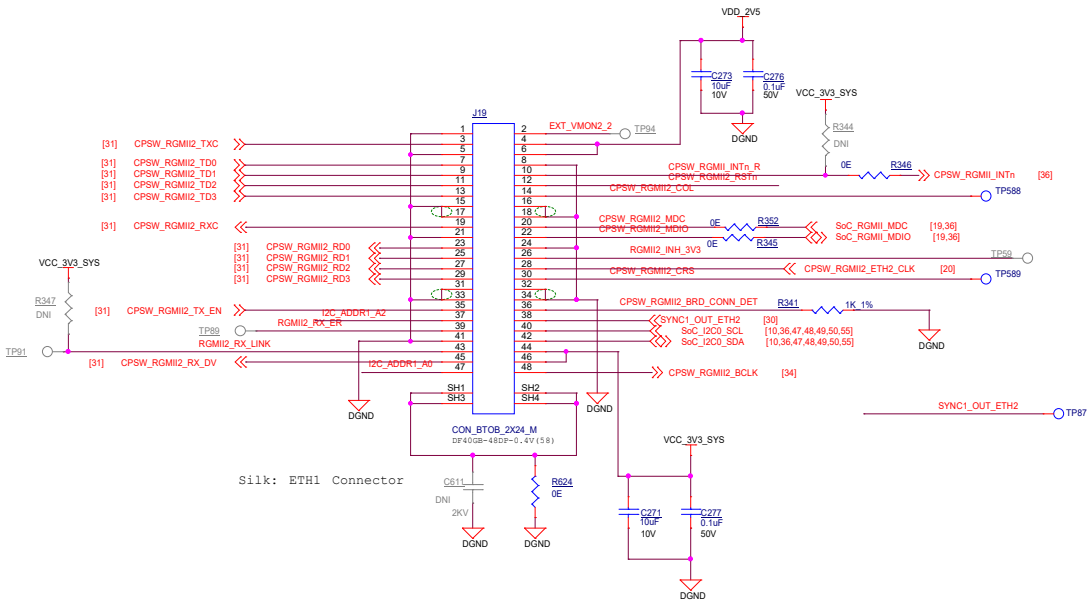
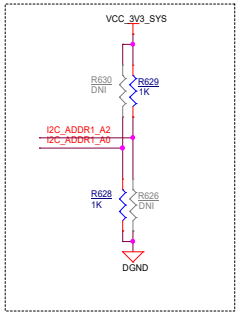
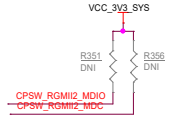
ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2

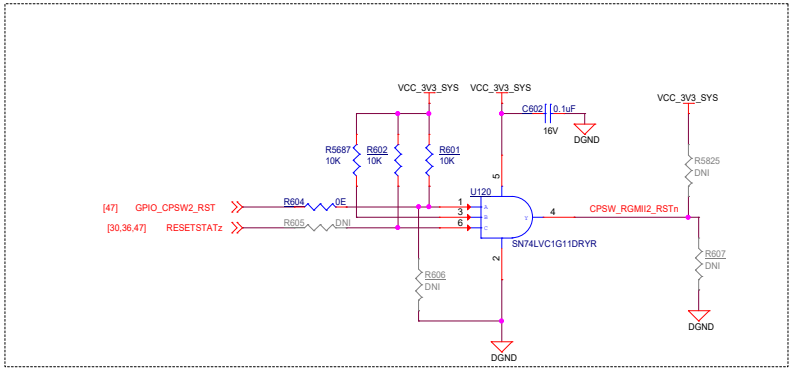


I2C Address Strap

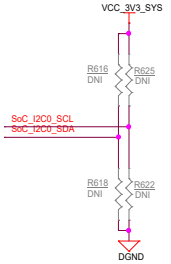




CPSW3G RGMII 2 RESET



Note: Verify the resistor mounting configuration for resistors that are marked as DNI



CAD Note: Thevnin's termination should be placed at the J19 Connector

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Title	ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2	
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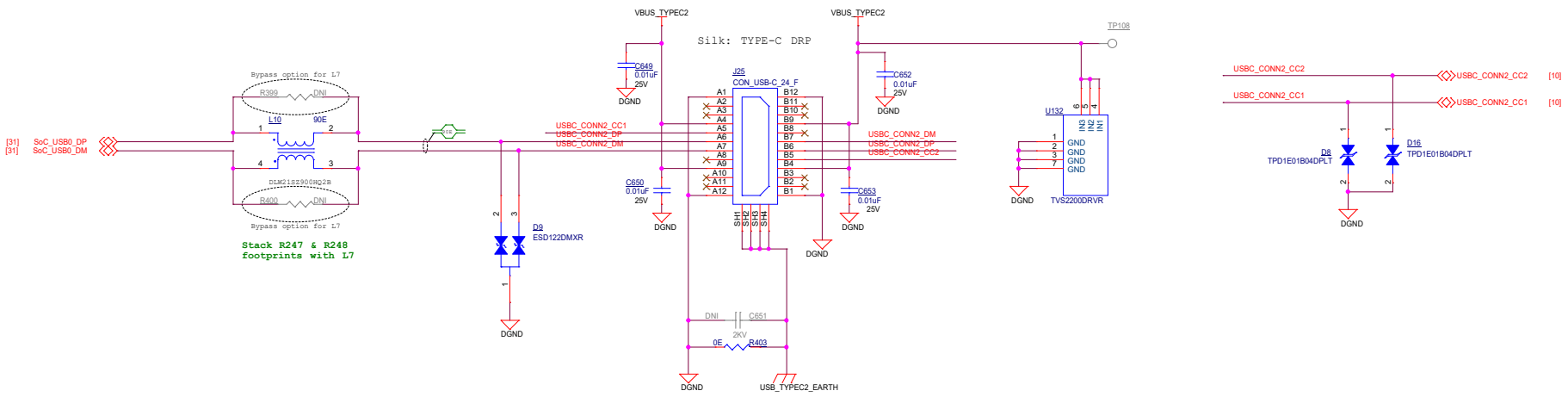
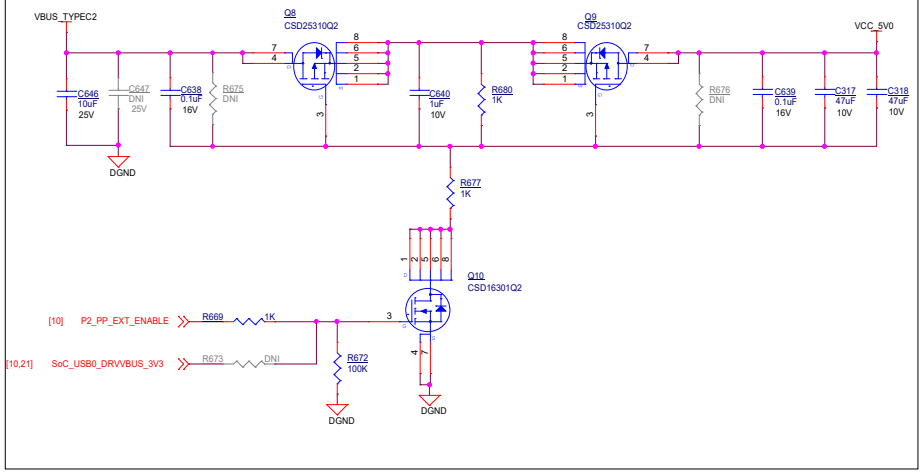
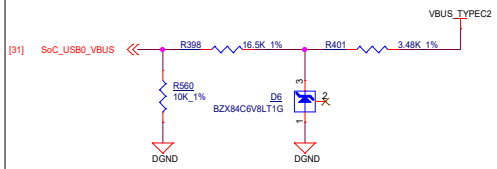
USB0 TYPE-C DRP



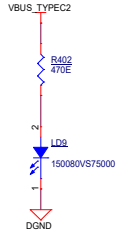
EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



Note: Refer data sheet USB VBUS Design Guidelines section.



POWER INDICATION LED: VBUS_TYPEC2



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Title	USB0 TYPE-C DRP		
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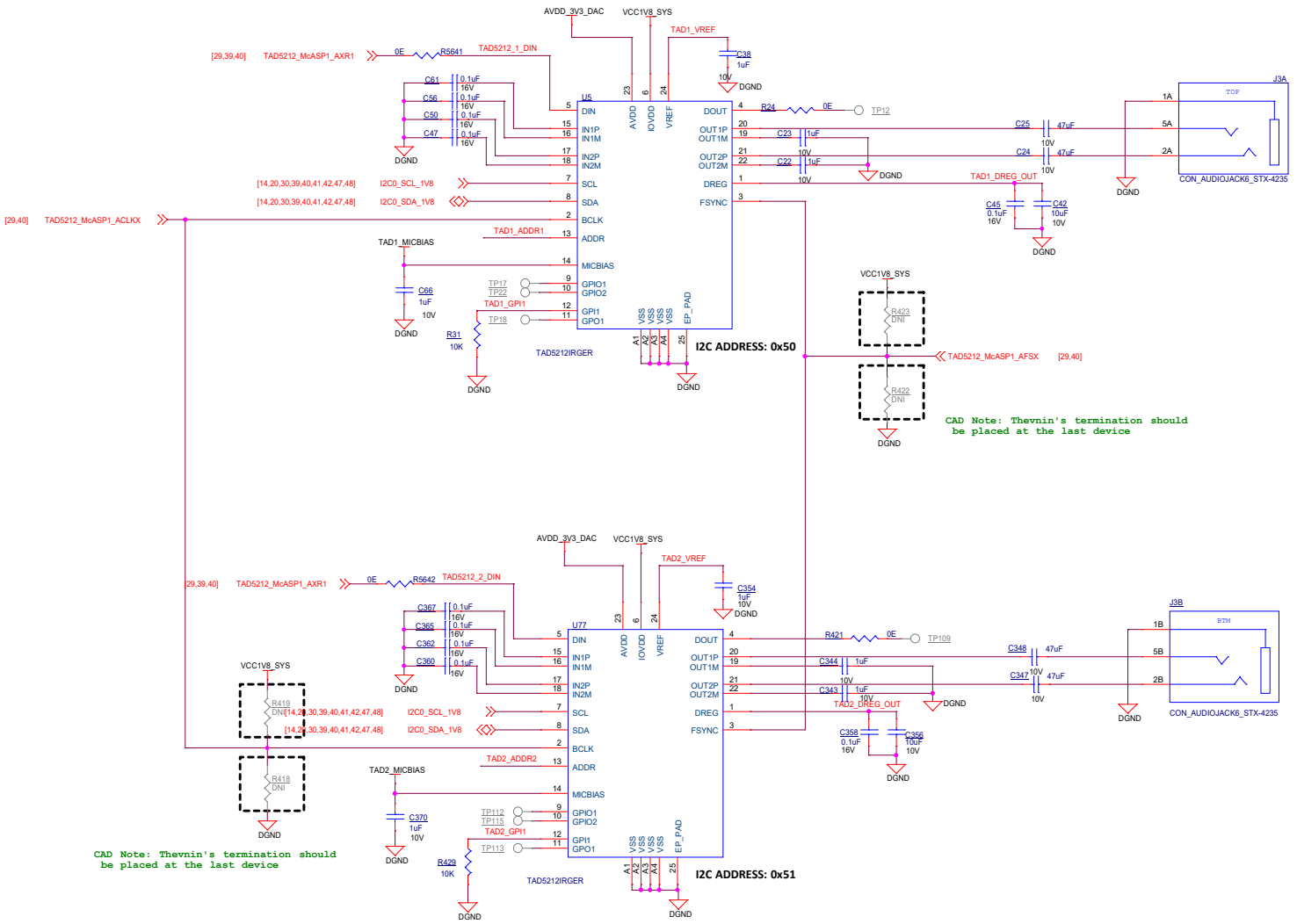
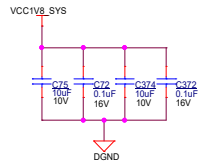
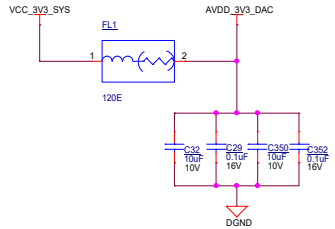
AUDIO - STEREO LINEOUT - 1



DAC Supply & Decaps

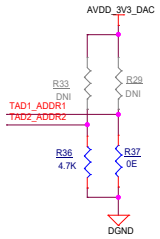


CAD Note: Place these decaps near the DVDD supply pin of DAC's



CAD Note: Place these decaps near the AVDD supply pin of DAC's

DAC I2C Address Straps



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO - STEREO LINEOUT - 1		
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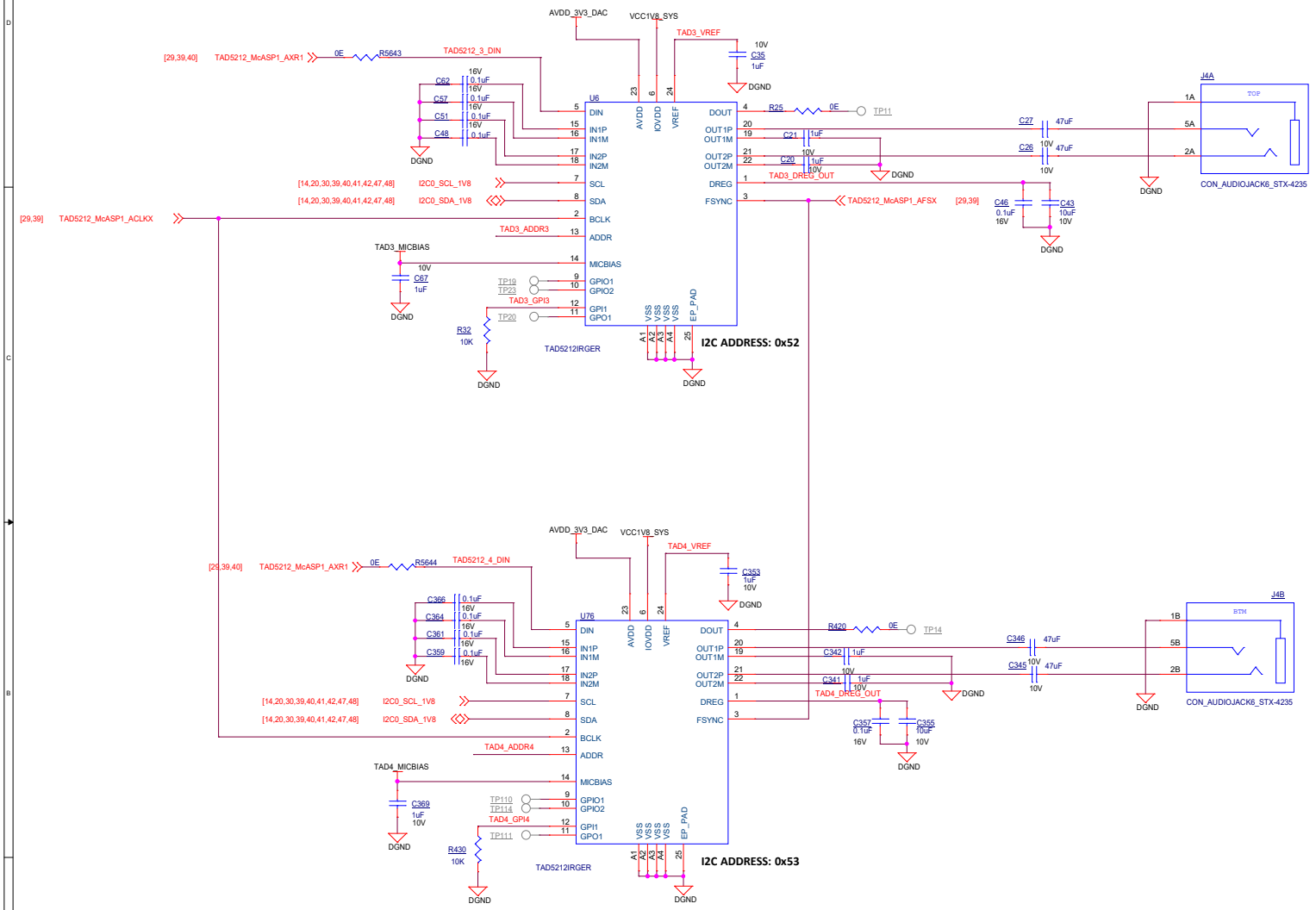
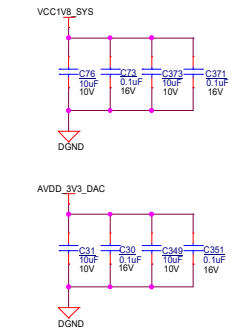
AUDIO - STEREO LINEOUT - 2

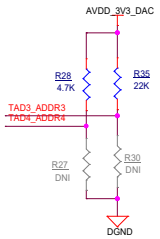


DAC Supply & Decaps



CAD Note: Place these decaps near the DVDD supply pin of DAC's

Device Straps



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO - STEREO LINEOUT - 2		
Size C	PROC190A		Rev A
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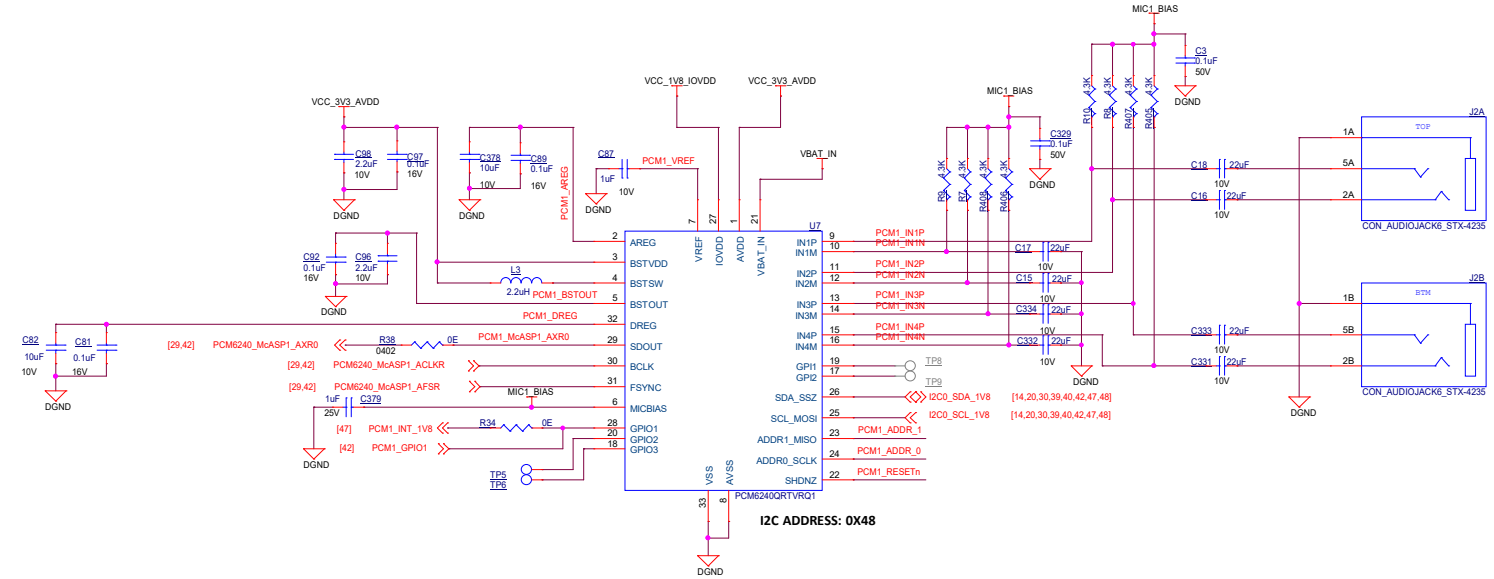
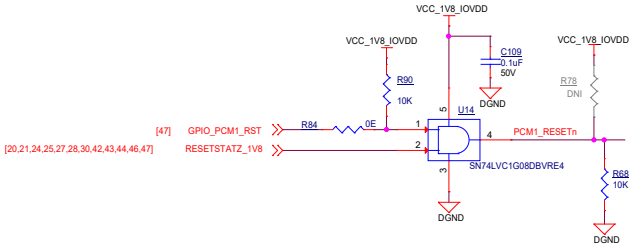
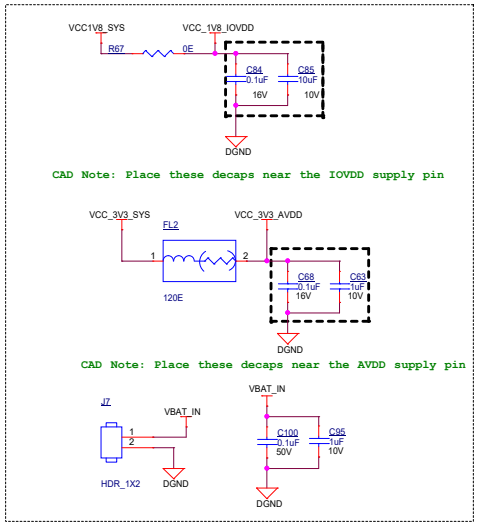
AUDIO - MICROPHONE/LINE IN 1

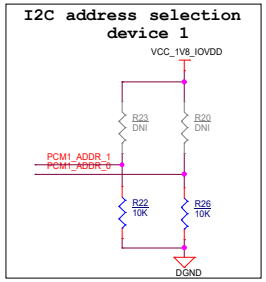


PCM1 RESET



ADC Supply & Decaps





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Title	AUDIO - MICROPHONE/LINE IN 1		
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C			A
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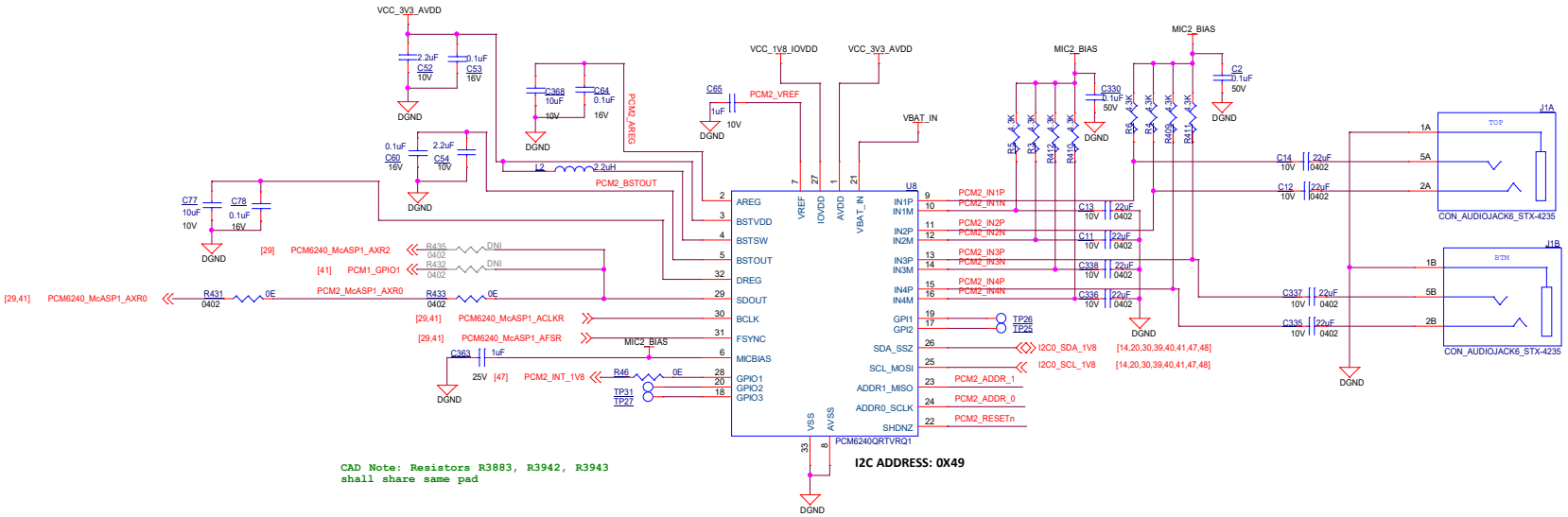
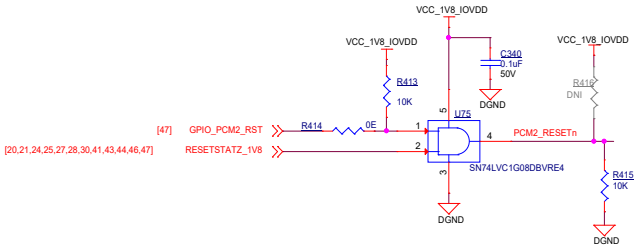
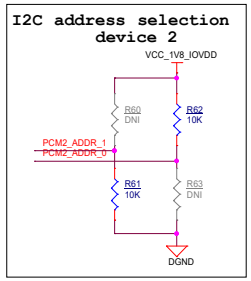
AUDIO - MICROPHONE/LINE IN 2

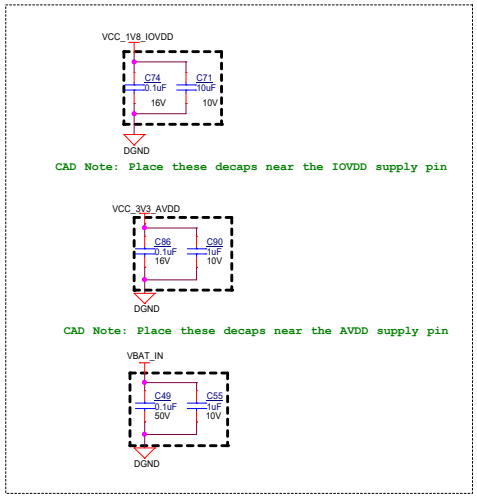


PCM2 RESET





ADC Supply & Decaps



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Title	AUDIO - MICROPHONE/LINE IN 2		
Size C	PROC190A		Rev A
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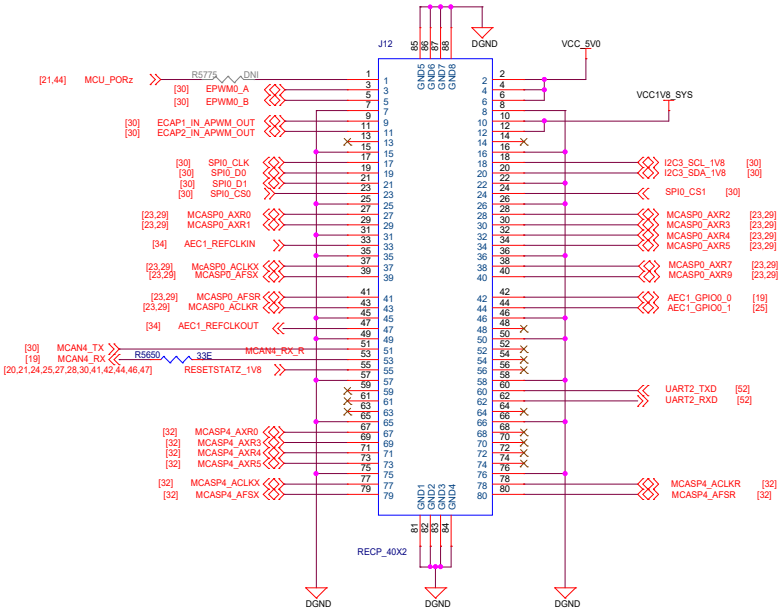
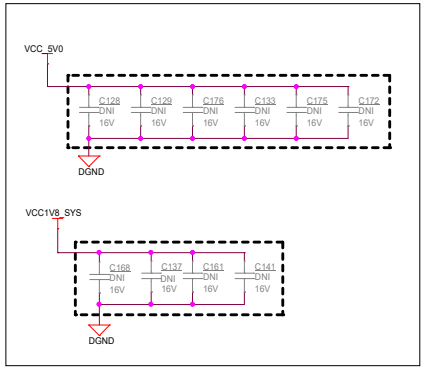
AUDIO EXPANSION CONNECTOR #1



AUDIO EXPANSION DECAPS



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO EXPANSION CONNECTOR #1		
Size C	PROC190A		Rev A
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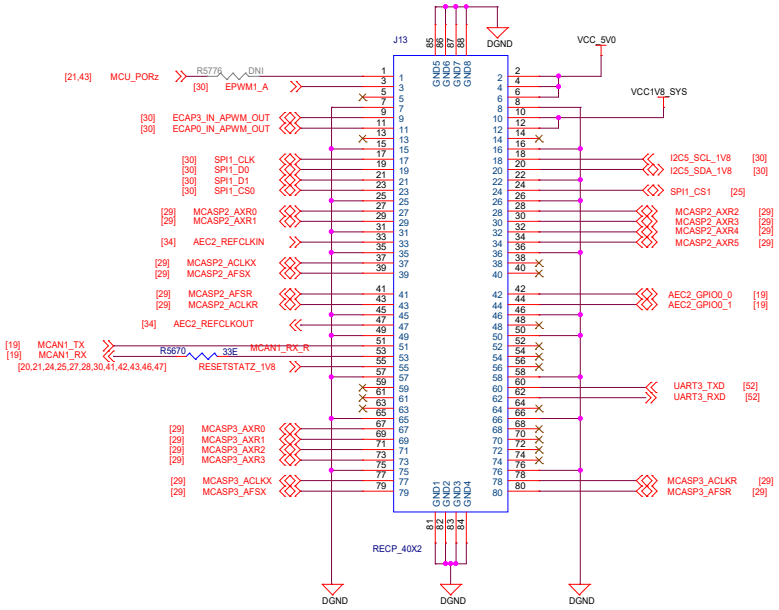
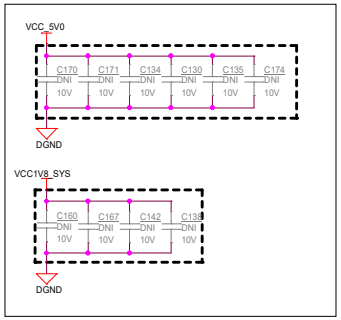
AUDIO EXPANSION CONNECTOR #2



AUDIO EXPANSION DECAPS



Designed for TI by Mistral Solutions Pvt Ltd

Title	AUDIO EXPANSION CONNECTOR #2	
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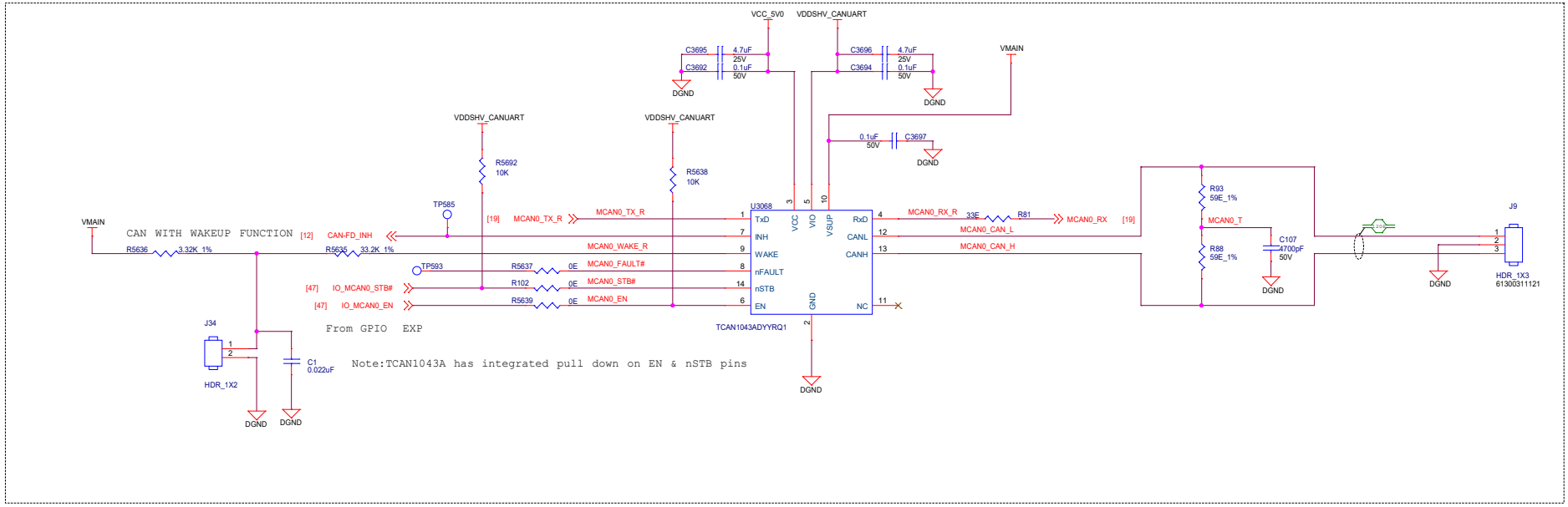
CAN TRANSCEIVER

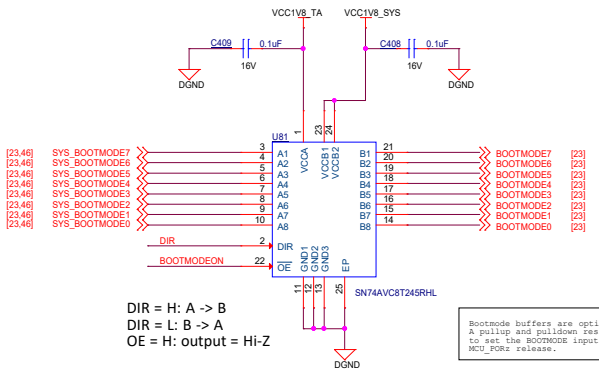


Designed for TI by Mistral Solutions Pvt Ltd

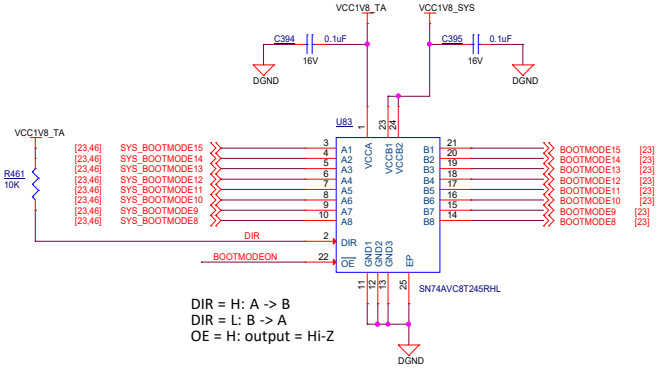
Title	CAN TRANSCEIVER		
Size C	PROC190A		Rev A
Date:	Thursday, March 13, 2025	Sheet 45 of 57	

BOOTMODE BUFFERS AND IO EXPANDERS

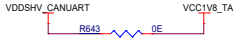
BOOT MODE BUFFERS

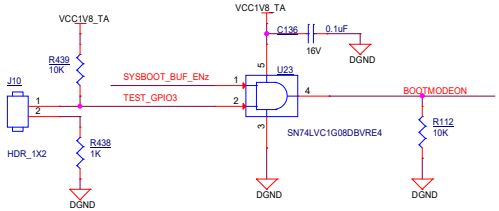


Bootmode buffers are optional.
A pullup and pulldown resistor can be used to set the BOOTMODE input state prior to MCU_PORz release.

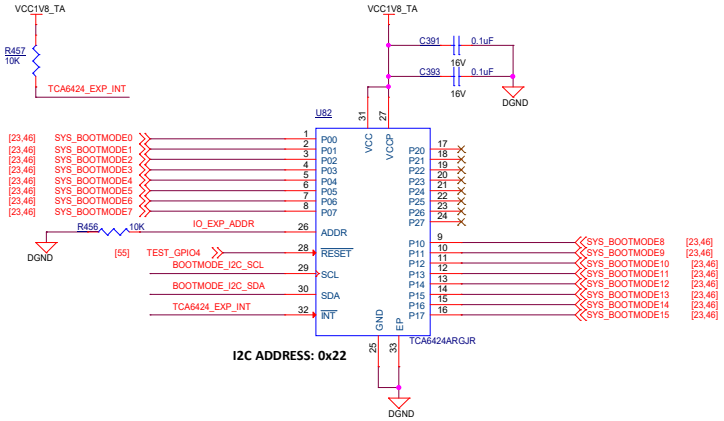


TEST AUTOMATION SUPPLY

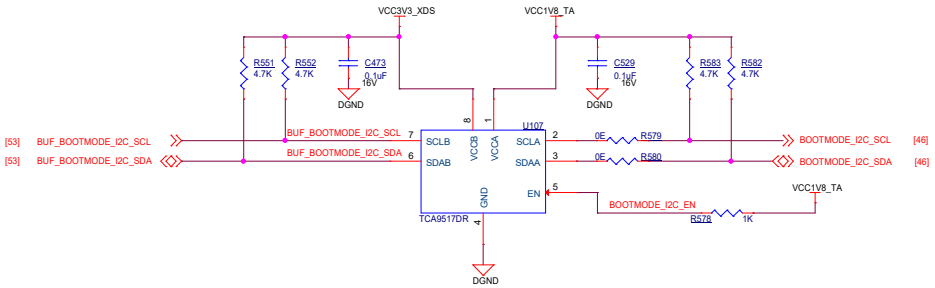




BOOTMODE IO EXPANDER



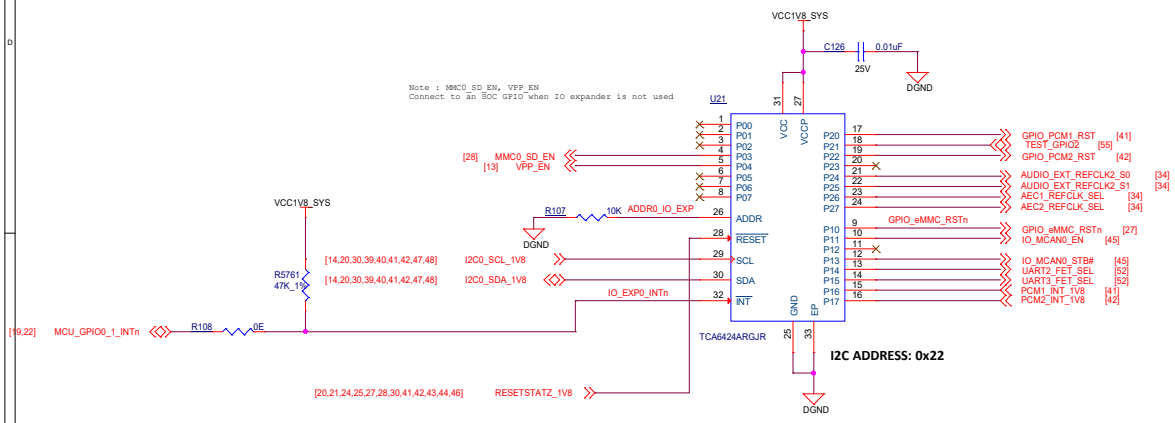
BOOTMODE I2C BUS BUFFER

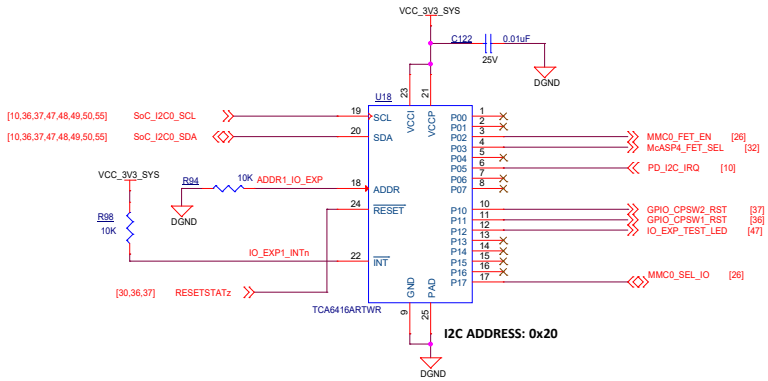


Designed for TI by Mistral Solutions Pvt Ltd

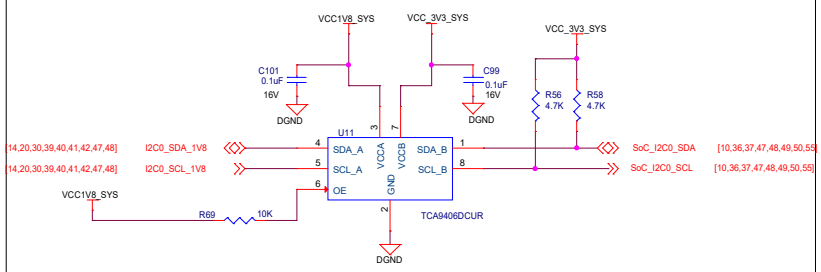
Title	BOOT MODE BUFFER & IO EXPANDERS		
Size C	PROC190A		Rev A
Date: Thursday, March 13, 2025		Sheet 46 of 57	

IO EXPANDER

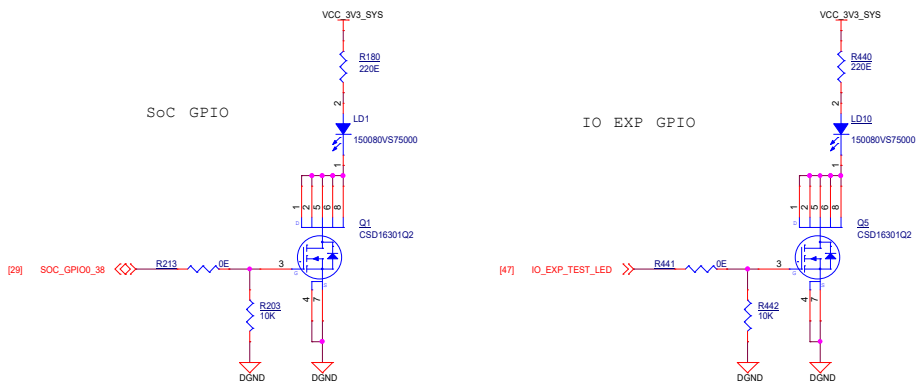




I2C LEVEL TRANSLATOR



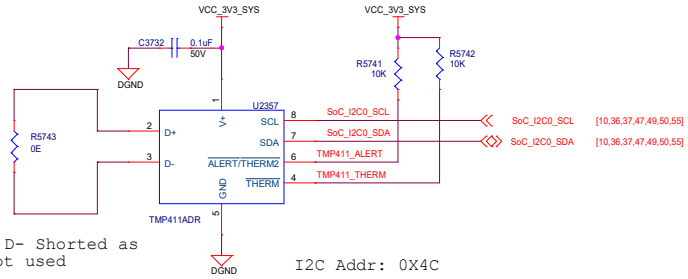
USER TEST LEDS



Designed for TI by Mistral Solutions Pvt Ltd

Title	IO EXPANDER & USER TEST LEDS	
Size C	PROC190A	Rev A
Date: Thursday, March 13, 2025	Sheet 47 of 57	

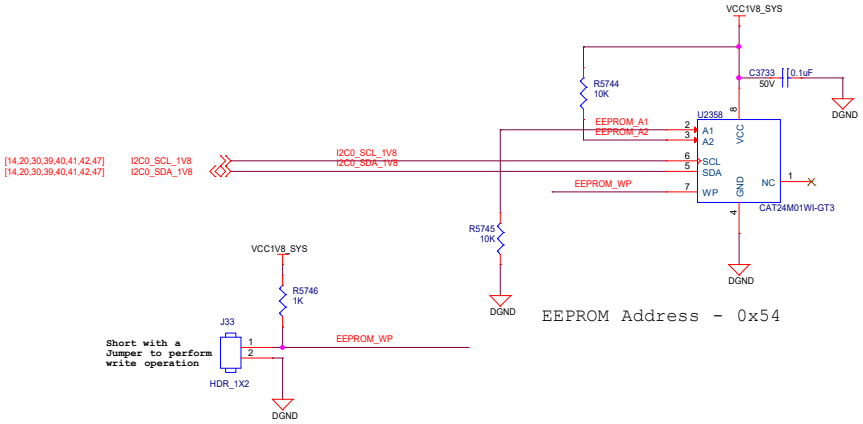
TEMPERATURE SENSORS



Note: D+ and D- Shorted as TEMPCAL is not used

I2C Addr: 0X4C
CAD Note: Place Close To SOC

BOARD ID EEPROM



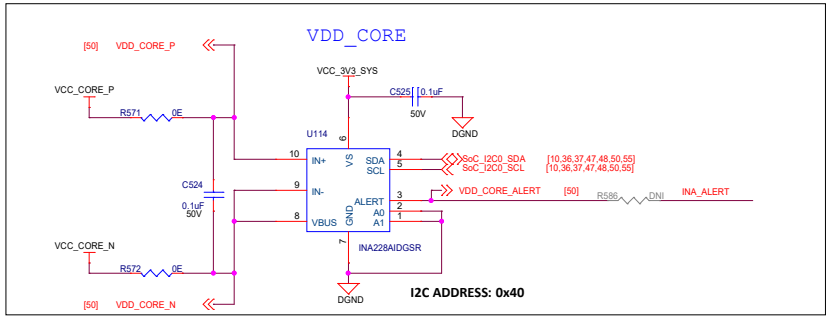
EEPROM Address - 0x54

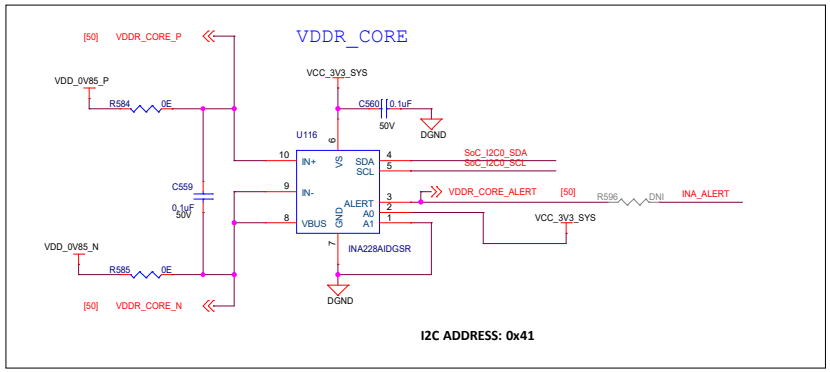
PROC190A

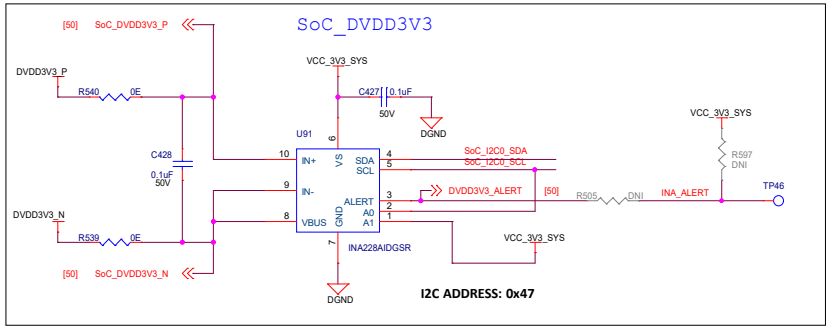
Designed for TI by Mistral Solutions Pvt Ltd

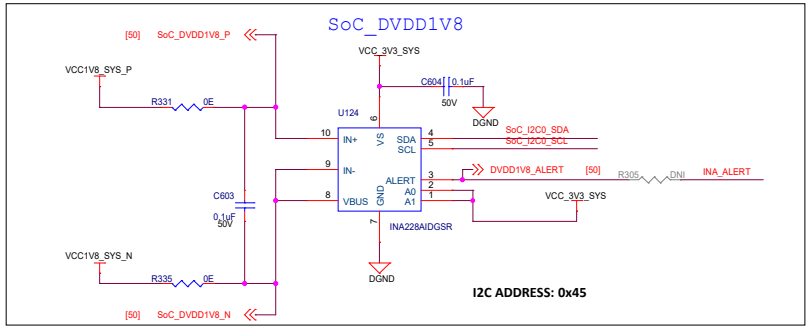
Title	TEMPERATURE SENSORS & BOARD ID EEPROM		
Size	PROC180E1		Rev
C			A
Date:	Thursday, March 13, 2025	Sheet 48 of 57	

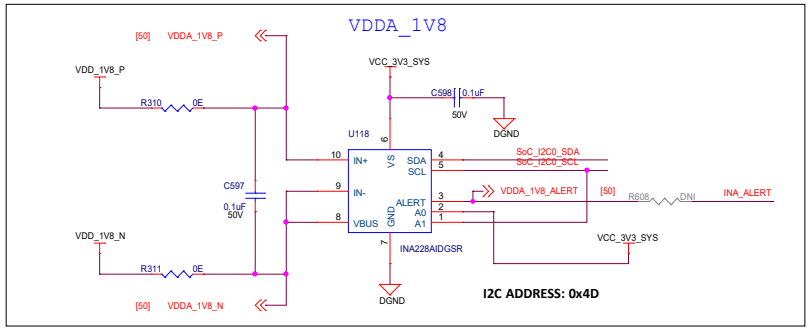
CURRENT MONITORING DEVICES - 1

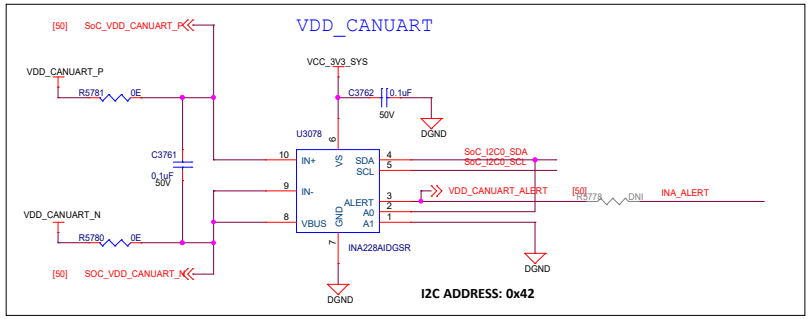


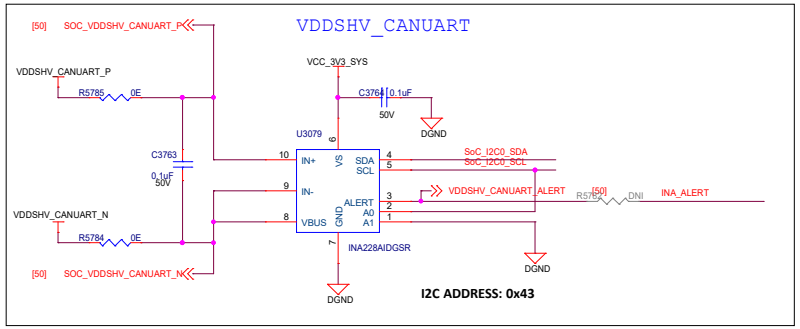












INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	47
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VDD_CANUART	SOC_VDD_CANUART	42
VDDSHV_CANUART	SOC_VDDSHV_CANUART	43

Note: The design supports current/voltage measurements using either INA228 or INA231.
INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

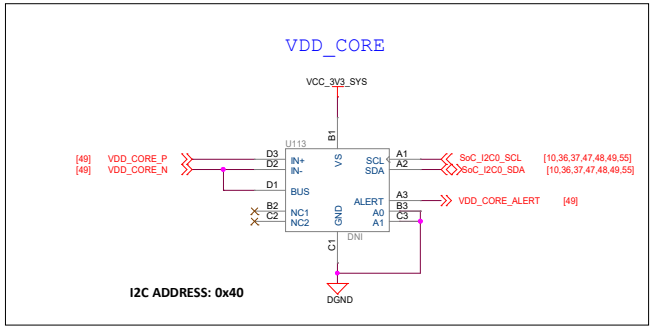
PROC190A

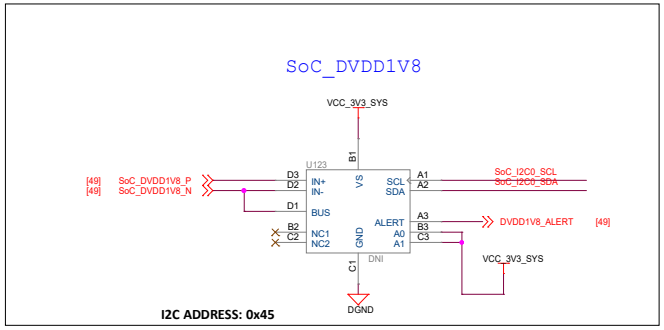
Designed for TI by Mistral Solutions Pvt Ltd

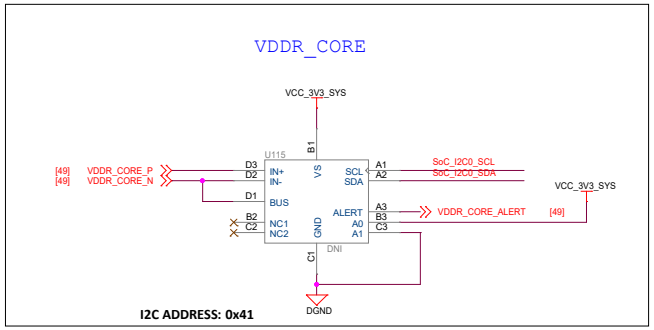
Texas Instruments MISTRAL

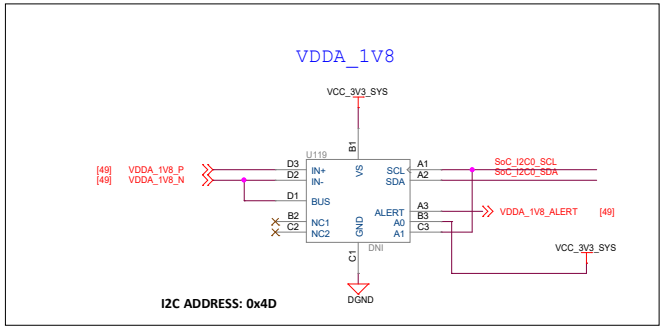
Title	CURRENT MONITORING DEVICES - 1	
Size C	PROC180E1	Rev A
Date: Thursday, March 13, 2025	Sheet 49 of 57	

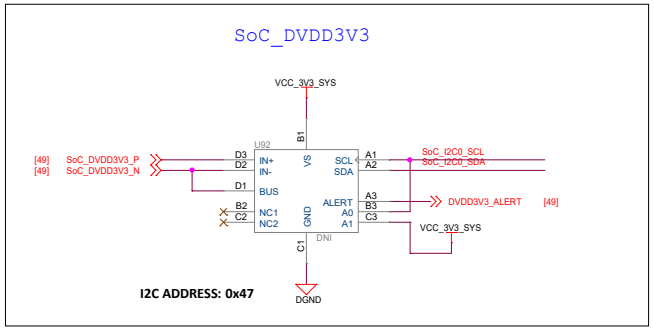
CURRENT MONITORING DEVICES - 2

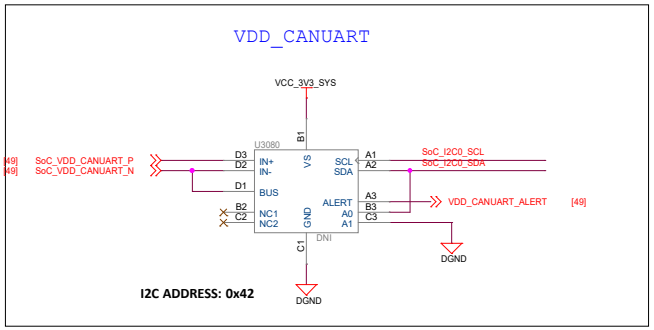


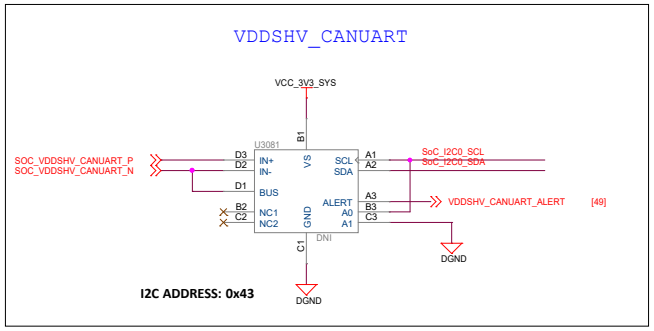












INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	47
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VDD_CANUART	SOC_VDD_CANUART	42
VDDSHV_CANUART	SOC_VDDSHV_CANUART	43

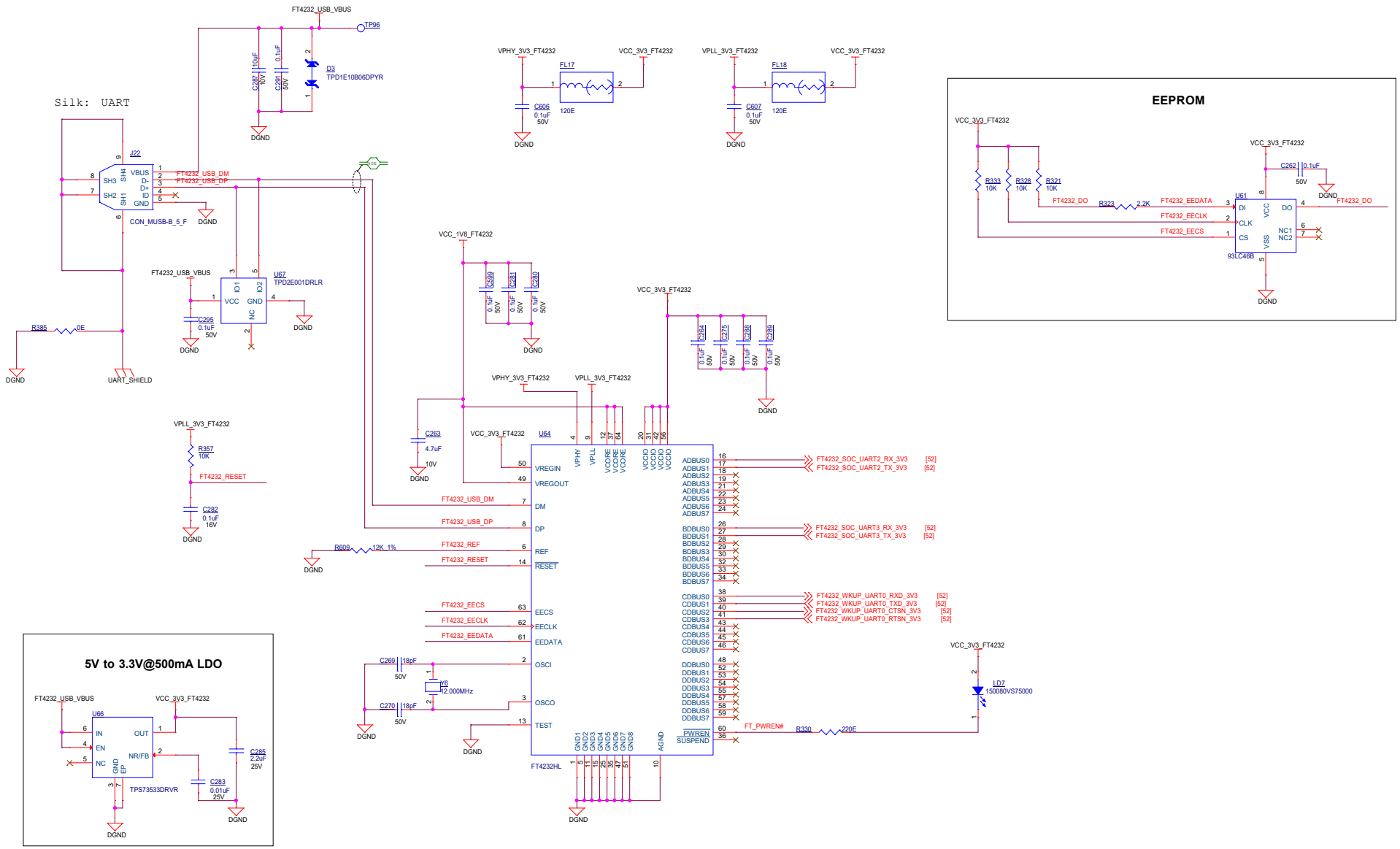
Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

PROC190A

Designed for TI by Mistral Solutions Pvt Ltd

Title	CURRENT MONITORING DEVICES - 2	
Size C	PROC180E1	Rev A
Date: Thursday, March 13, 2025	Sheet 50 of 57	

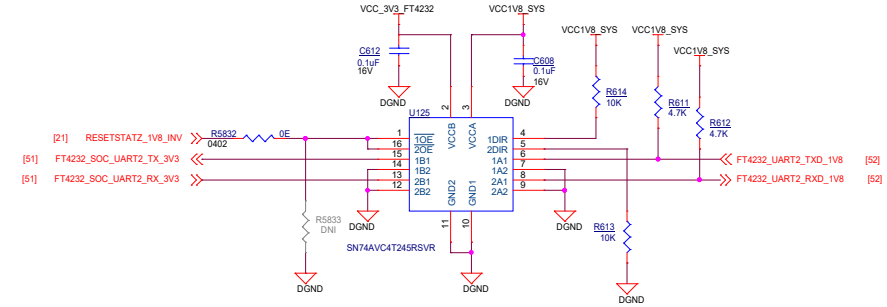
USB TO UART BRIDGE

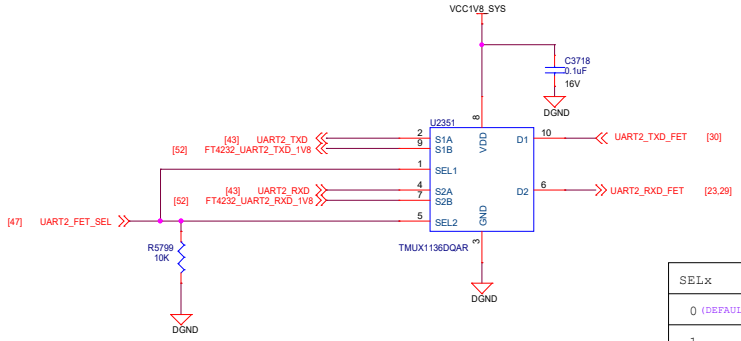


Designed for TI by Mistral Solutions Pvt Ltd

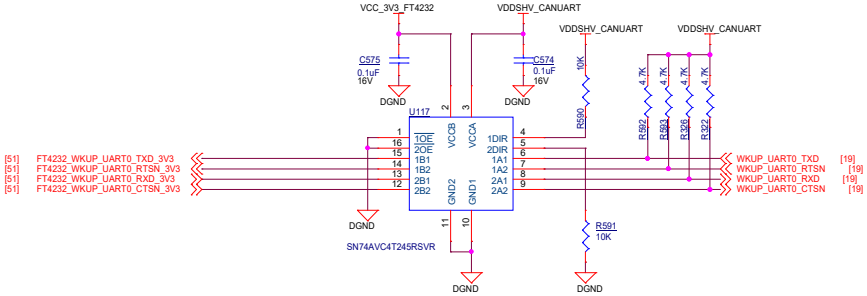
Title	FT4232 UART TO USB BRIDGE		
Size C	PROC190A		Rev A
Date: Thursday, March 13, 2025		Sheet 51 of 57	

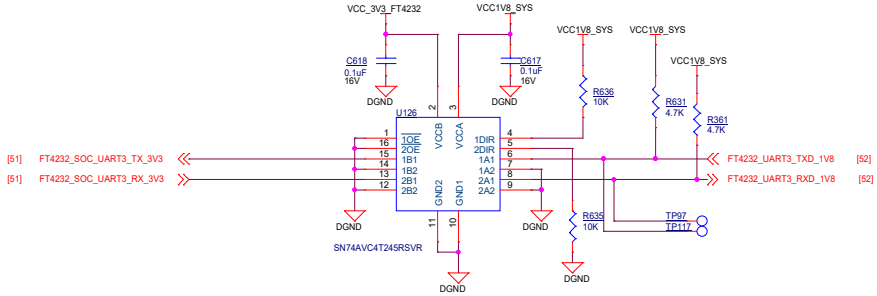
FT4232 UART BUFFERS

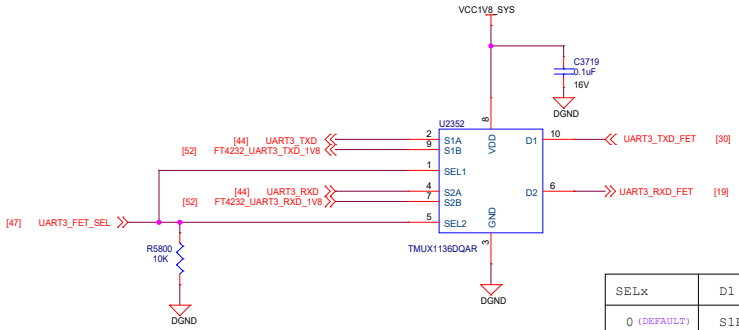




SELx	D1	D2
0 (DEFAULT)	S1B	S2B
1	S1A	S2A







SELx	D1	D2
0 (DEFAULT)	S1B	S2B
1	S1A	S2A

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Title	FT4232 UART BUFFERS	
Size C	PROC190A	Rev A
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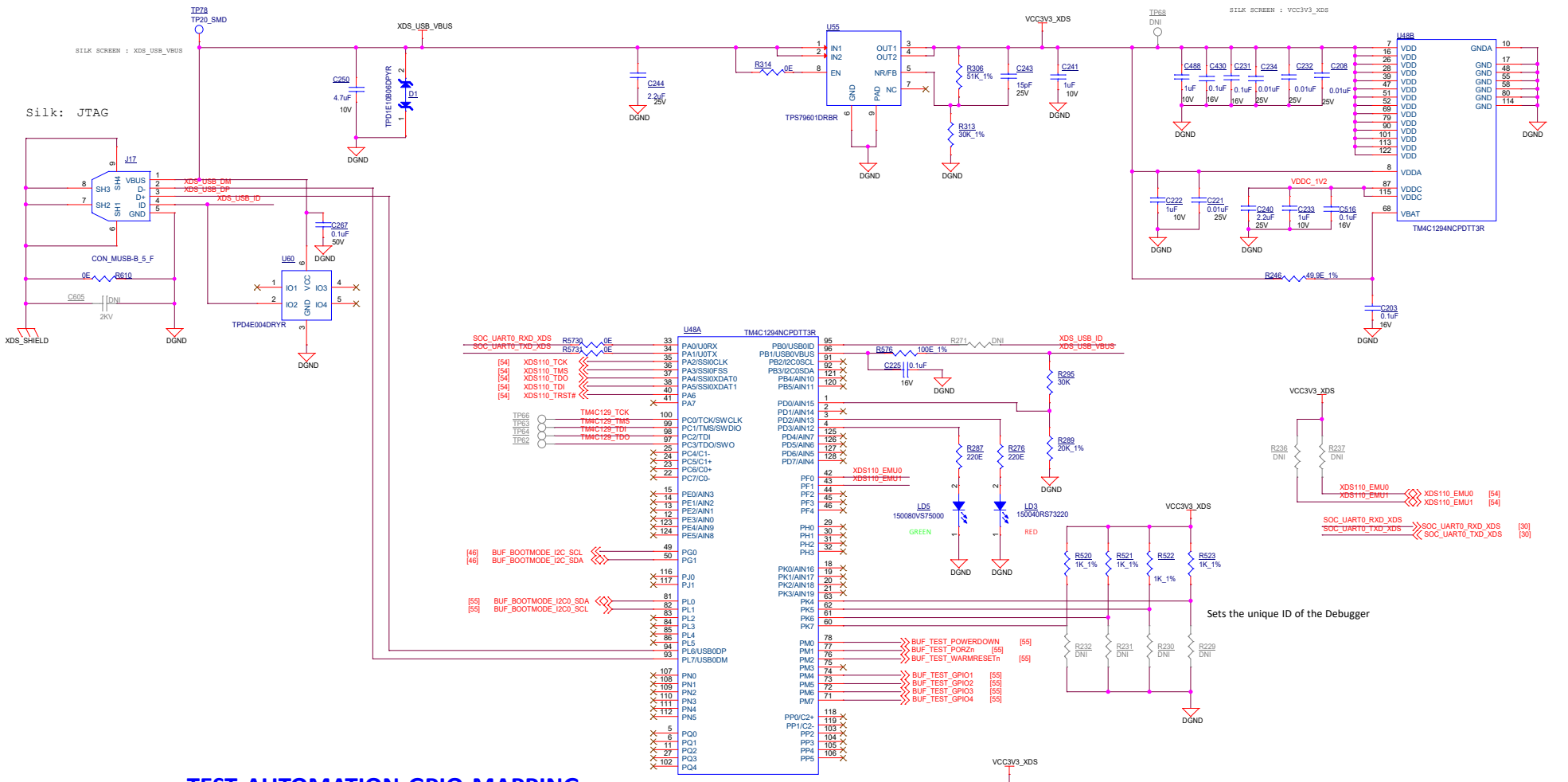
XDS110 DEBUGGER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO0_90 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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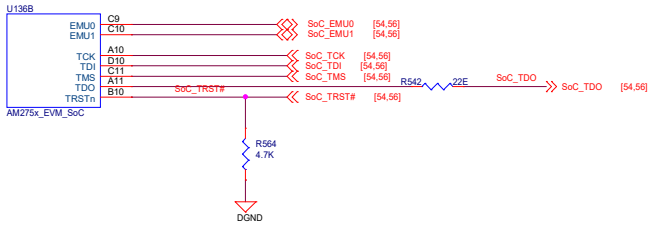
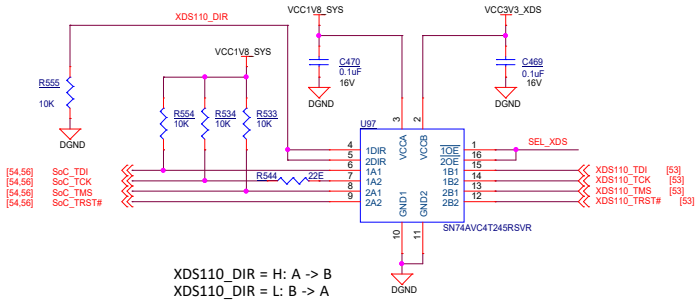
Texas Instruments MISTRAL

Title	XDS110 DEBUGGER		
Size C	PROC190A		Rev A
Date: Thursday, March 13, 2025		Sheet 53 of 57	

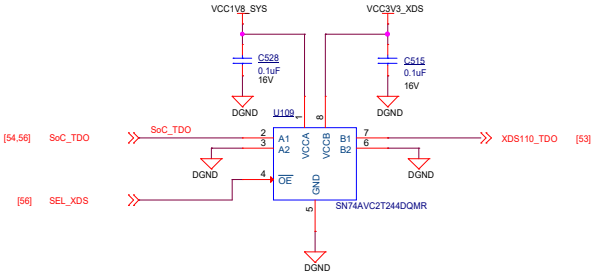
SOC - JTAG

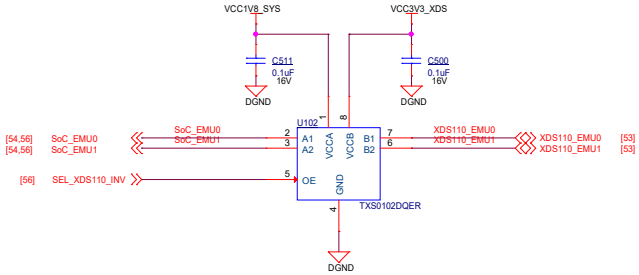


XDS110 JTAG BUFFER



XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z

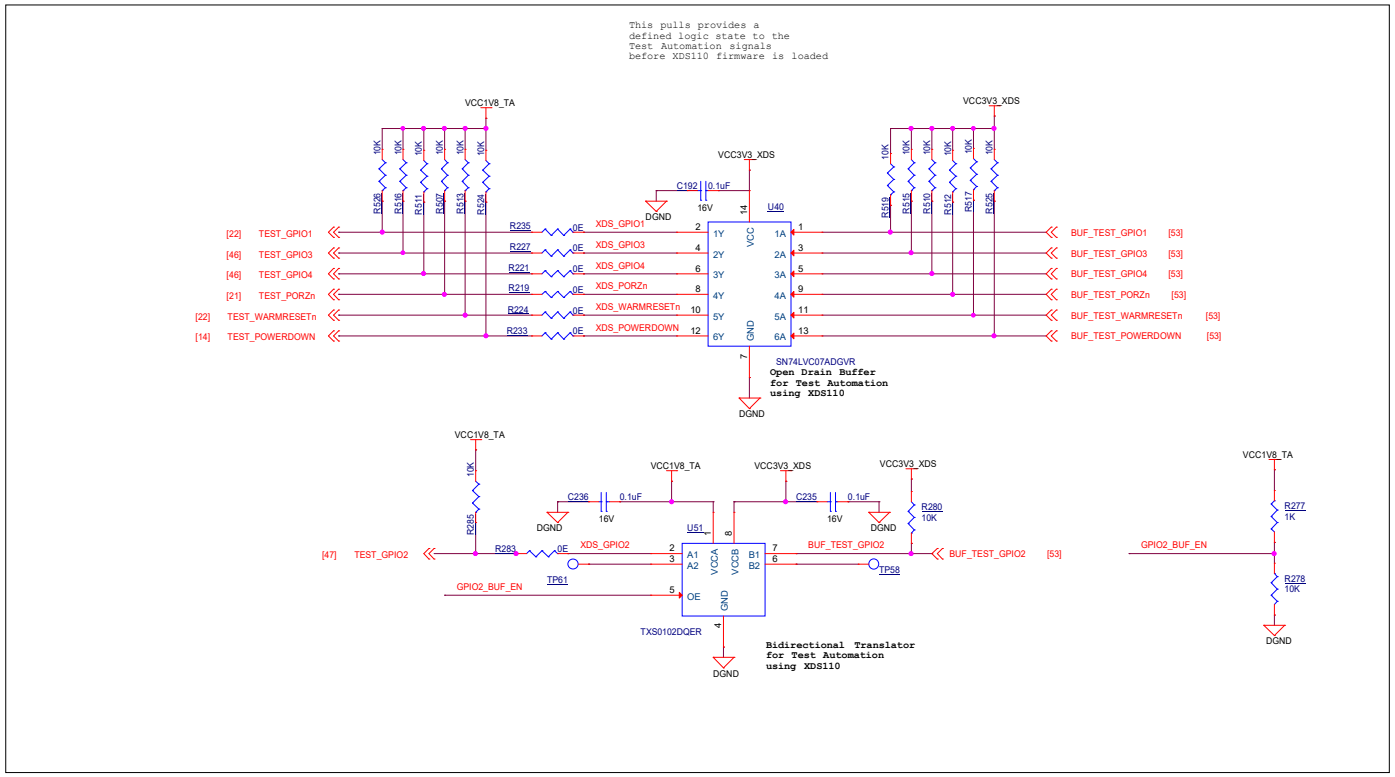




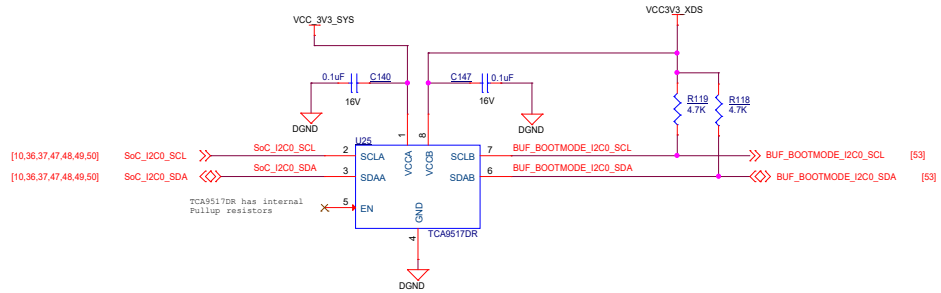
Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 JTAG BUFFER		
Size C	PROC190A		Rev A
Date: Thursday, March 13, 2025		Sheet 54 of 57	

XDS110 TEST AUTOMATION BUFFERS



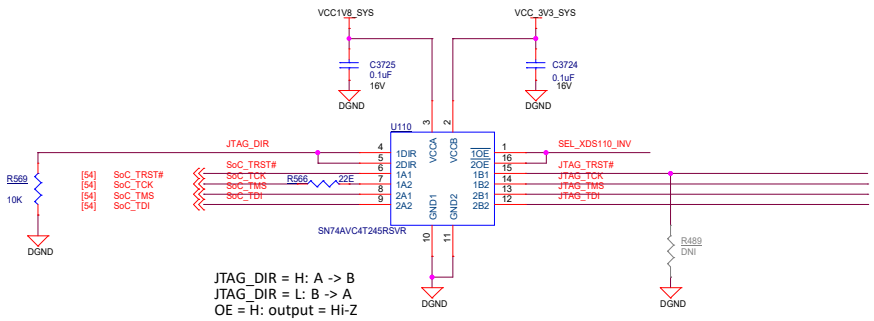
SOC I2C BUS BUFFER



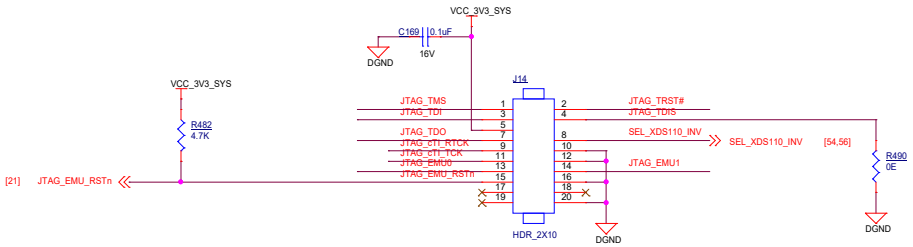
Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 TEST AUTOMATION BUFFERS		
Size C	PROC190A		Rev A
Date: Thursday, March 13, 2025		Sheet 55 of 57	

JTAG BUFFERS

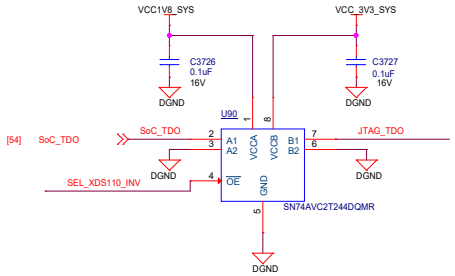


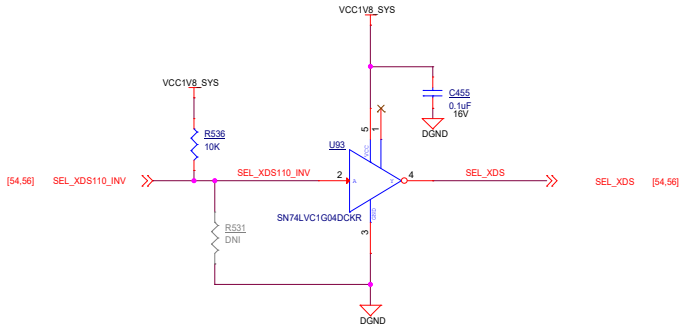
cTI20 JTAG CONNECTOR



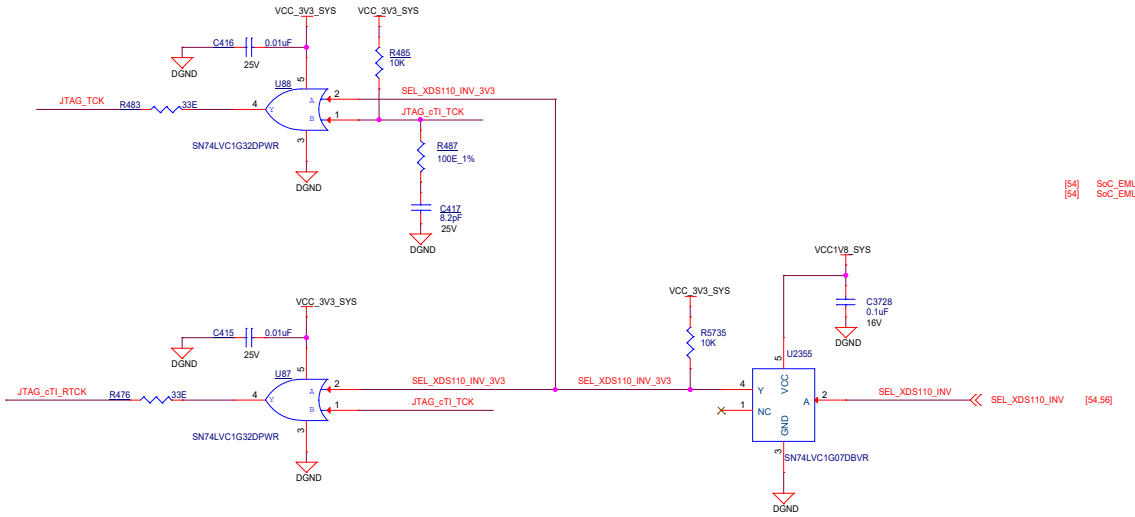
Silk: cTI

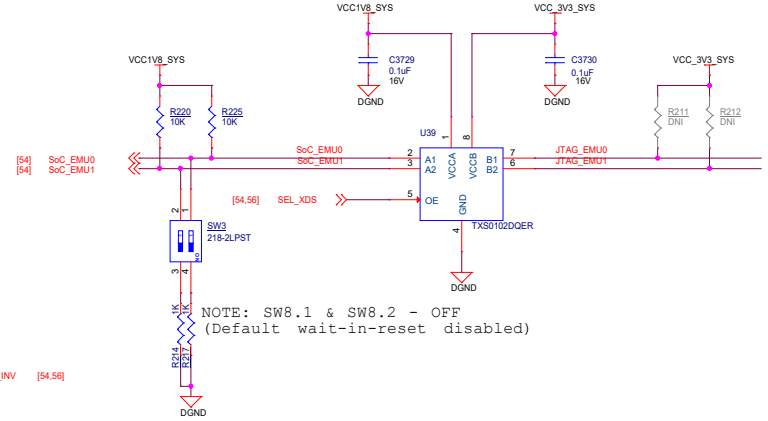
Add an external ESD protection to provide system level ESD protection





JTAG CLOCK BUFFER





Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG 20 PIN cTI CONNECTOR		
Size C	PROC190A		Rev A
Date: Thursday, March 13, 2025		Sheet 56 of 57	

MOUNTING HARDWARE

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

JUMPERS

ACC2 DNI
ACC3 DNI

LOGOs

PCB LOGO DNI Texas Intruments
PCB LOGO DNI For Evaluation only; not FCC approved for resale
PCB LOGO DNI WEEE Mark
PCB LOGO DNI CE Mark

LABELS

Board Serial No.

LBL1 PCB LABEL DNI

Assembly Revision

LBL2 PCB LABEL DNI

EVM Orderable No.

LBL3 PCB LABEL DNI

Orderable Part Numbers	
Variant	**Label Text**
001	AUDIO-AM275-EVM

BARE PCB

PROC190A
PROC190A

SCREWS

MH1 PAN HEAD_M3 X 6
MH2 PAN HEAD_M3 X 6
MH3 PAN HEAD_M3 X 6
MH4 PAN HEAD_M3 X 6

STANDOFFs

ACC9 970100327
ACC14 970100327
ACC15 970100327
ACC16 970100327

WASHER

ACC10 PLAIN WASHER_M3
ACC11 PLAIN WASHER_M3
ACC12 PLAIN WASHER_M3
ACC13 PLAIN WASHER_M3

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Title	MOUNTING HARDWARE		
Size C	PROC190A		Rev A
Date: Friday, March 14, 2025		Sheet 57 of 57	