

1

2

3

4

5

6

A

B

C

D

1

2

3

4

5

6

Cannot open file D:\Sol-Def\CC31XX\R2\Boards\CC3220-LAUNCHXL\Rev-Ax\Docs\CC3220LP_Block_Diagram.png

Cannot open file D:\Sol-Def\CC31XX\R2\Boards\CC3220-LAUNCHXL\Rev-Ax\Docs\CC3220LP_Block_Diagram.png

Revision History

Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

Orderable: CC3220SF-LAUNCHXL

Designed for: TI CONFIDENTIAL

Mod. Date: 8/17/2016

TID #: N/A

Project Title: WCS002A

Number: WCS002

Rev: A

Sheet Title: Cover Sheet

SVN Rev: Version control disabled

Assembly Variant: 001

Sheet: 1 of 6

Drawn By:

File: WCS002A_CoverSheet_SchDoc

Size: C

Engineer: Prajay Madhavan

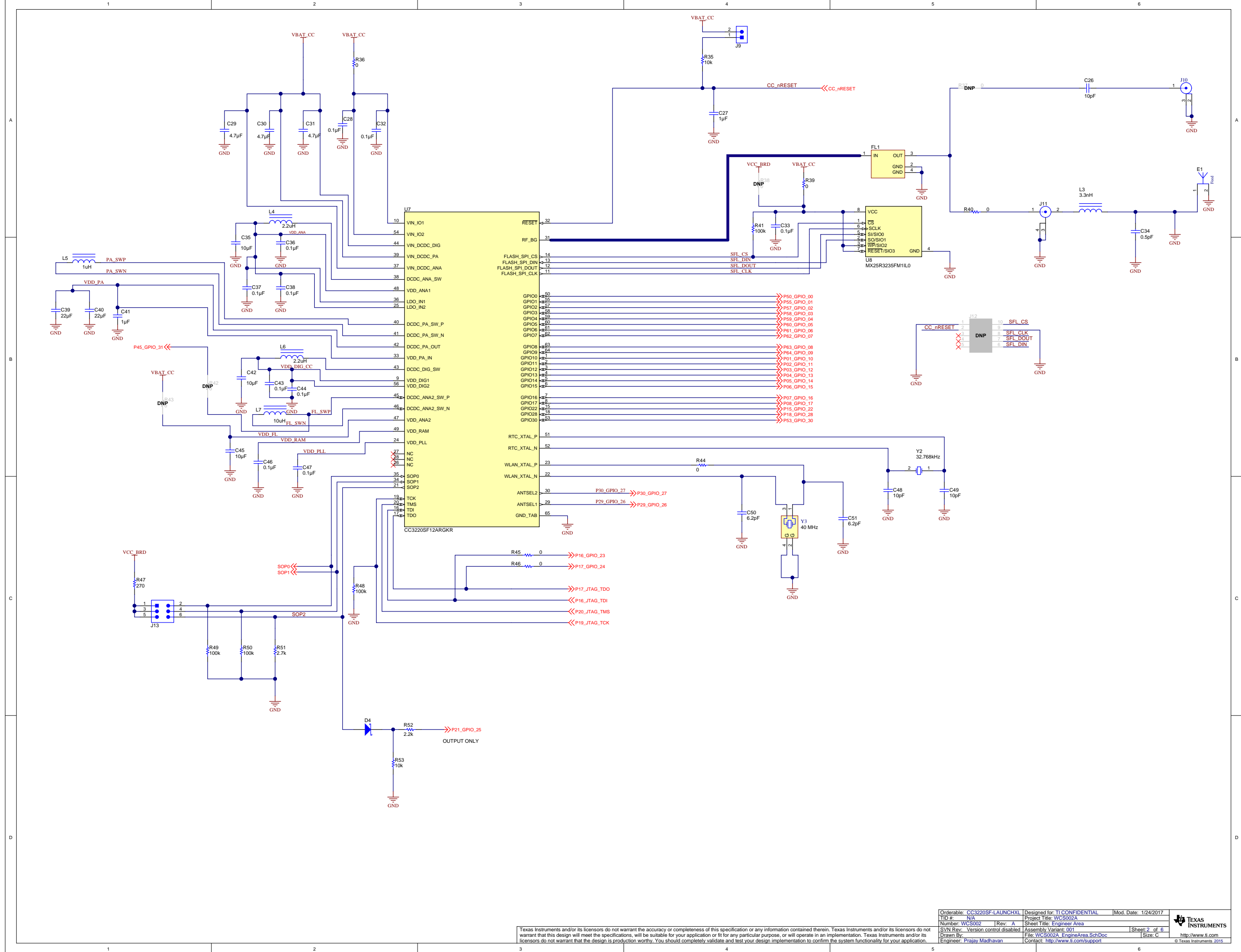
Contact: <http://www.ti.com/support>

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

 TEXAS INSTRUMENTS

© Texas Instruments 2015

<http://www.ti.com>



The diagram illustrates the pin connections for the P1 and P3 headers of the Pico board. The connections are as follows:

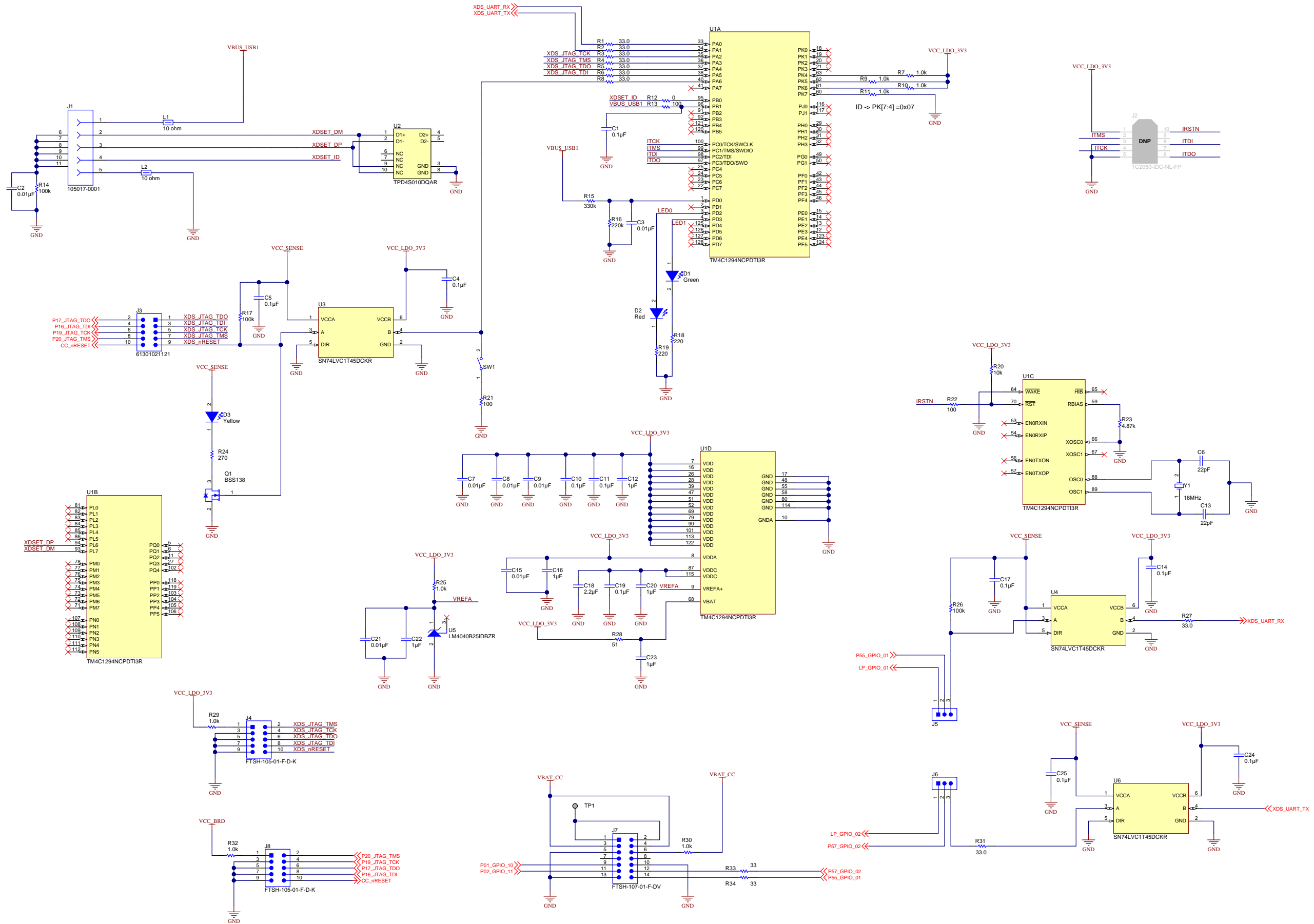
- VCC_BRD** is connected to **P1_1** (PWR) and **P3_1** (PWR).
- VBAT_CC** is connected to **P1_2** (ANA_IN) and **P3_2** (GND).
- R56** (0) is connected to **P1_3** (TX) and **P3_3** (ANA_IN).
- R57** (0) is connected to **P1_4** (RX) and **P3_4** (ANA_IN).
- DNP** is connected to **P1_5** (GPIO) and **P3_5** (ANA_IN).
- PWR** is connected to **P1_6** (GPIO) and **P3_6** (ANA_IN).
- ANA_IN** is connected to **P1_7** (SPI_CLK) and **P3_7** (I2S_SYNC).
- TX** is connected to **P1_8** (GPIO) and **P3_8** (I2S_CLK).
- RX** is connected to **P1_9** (SCL) and **P3_9** (I2S_DOUT).
- GPIO** is connected to **P1_10** (SDA) and **P3_10** (I2S_DIN).
- SPI_CLK** is connected to **P1_11** (SCL) and **P3_11** (I2S_DIN).
- SCL** is connected to **P1_12** (SDA) and **P3_12** (I2S_DIN).
- SDA** is connected to **P1_13** (SCL) and **P3_13** (I2S_DIN).
- I2S_CLK** is connected to **P1_14** (SCL) and **P3_14** (I2S_DIN).
- I2S_DOUT** is connected to **P1_15** (SCL) and **P3_15** (I2S_DIN).
- I2S_DIN** is connected to **P1_16** (SCL) and **P3_16** (I2S_DIN).
- GND** is connected to **P1_17** (SCL) and **P3_17** (I2S_DIN).

The diagram also shows connections for the P04, P03, P61, P05, P62, P01, P02, P16, P17, P63, P64, and P50 GPIO pins.

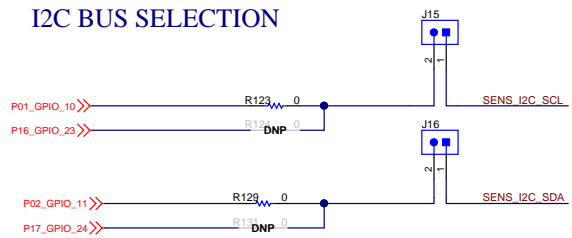
[illegible]

The internal structure of the ADC driver is detailed in four circuit diagrams. Each diagram shows an OPA4342EA/250 op-amp configured as a voltage follower (buffer). The op-amp's non-inverting input (+) is connected to an analog input (ANA_IN1, ANA_IN4, ANA_IN2, or ANA_IN3) through a resistor (R104, R103, R112, or R113, all 576k). The inverting input (-) is connected to the output (pin 7, 8, 1, or 14) and also to a feedback network consisting of a resistor (R107, R106, R114, or R115, all 422k) to ground and a capacitor (C52, C54, C55, or C56, all 0.01μF) to VCC_QFAMP. The output of each buffer is connected to a specific GPIO pin (LP_GPIO_02, P60_GPIO_05, P58_GPIO_03, or P59_GPIO_04) through a resistor (R105, R102, R110, or R111, all 470k). A pull-up resistor (R101, R100, R108, or R109, all 0Ω) is connected to the output line. The op-amp is powered by VCC_QFAMP and has its input offset null pins (pins 9 and 10) connected to ground. A J14 connector is shown at the top, connecting VCC_BRD and VCC_QFAMP.

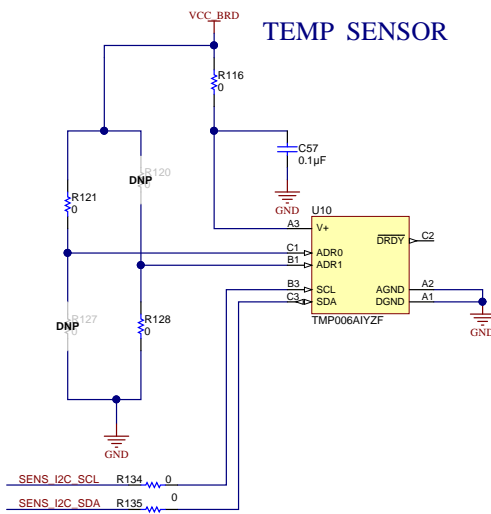
EMULATION CIRCUIT



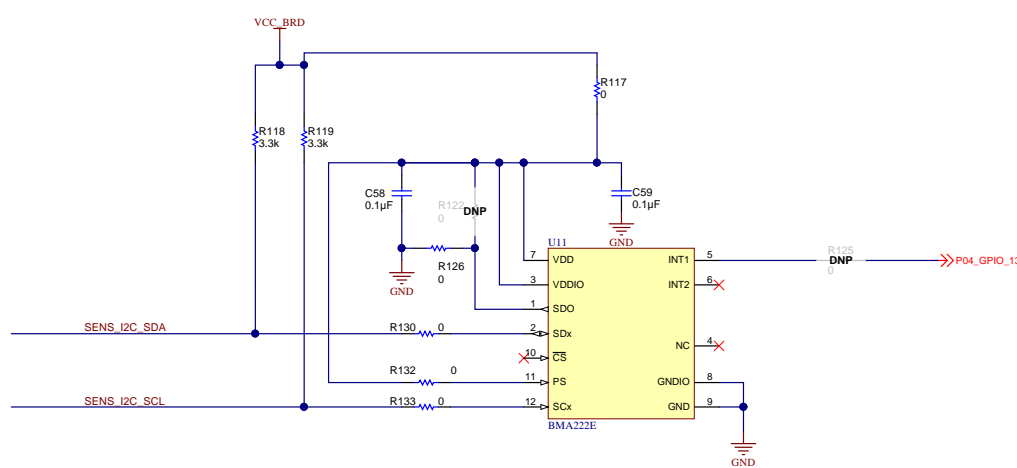
I2C BUS SELECTION



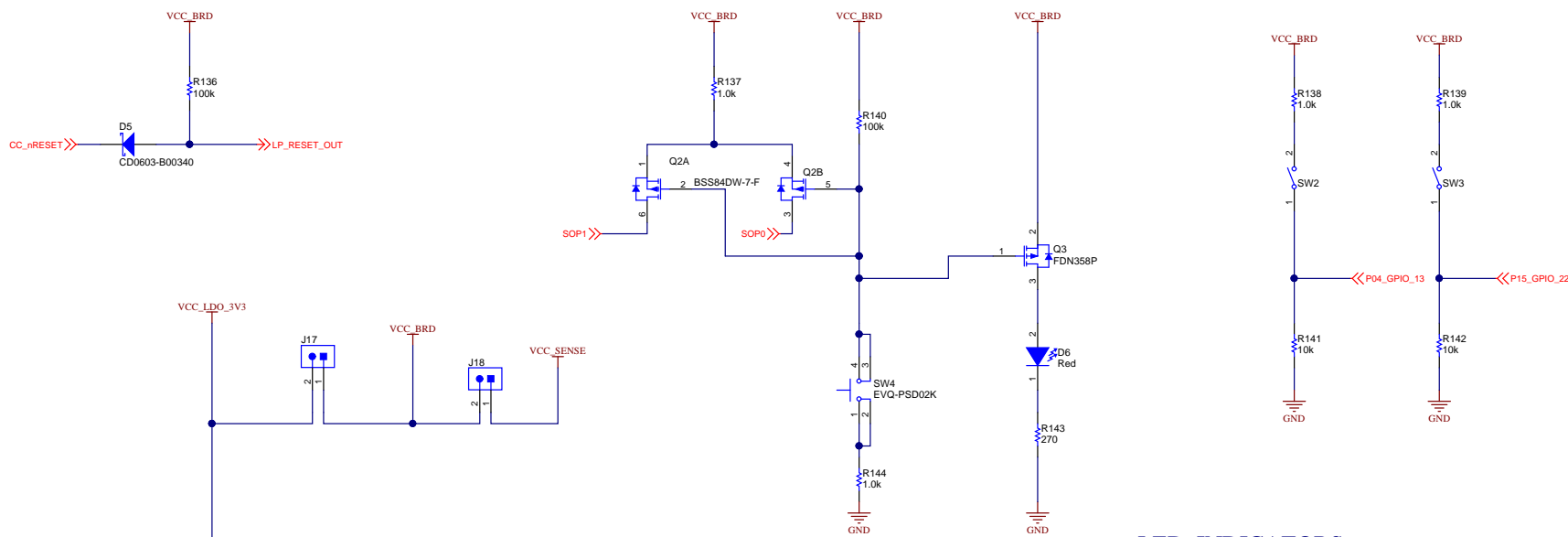
TEMP SENSOR



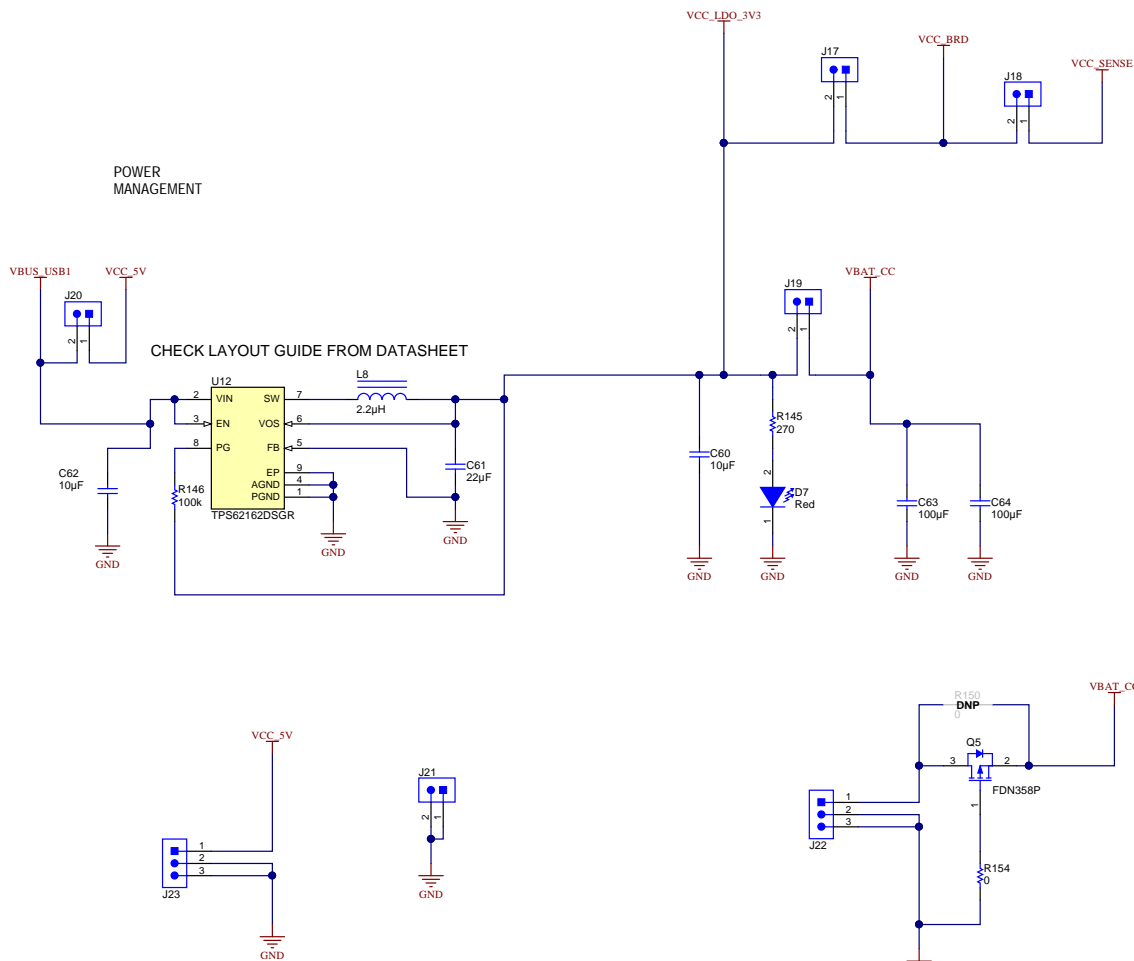
ACCELEROMETER



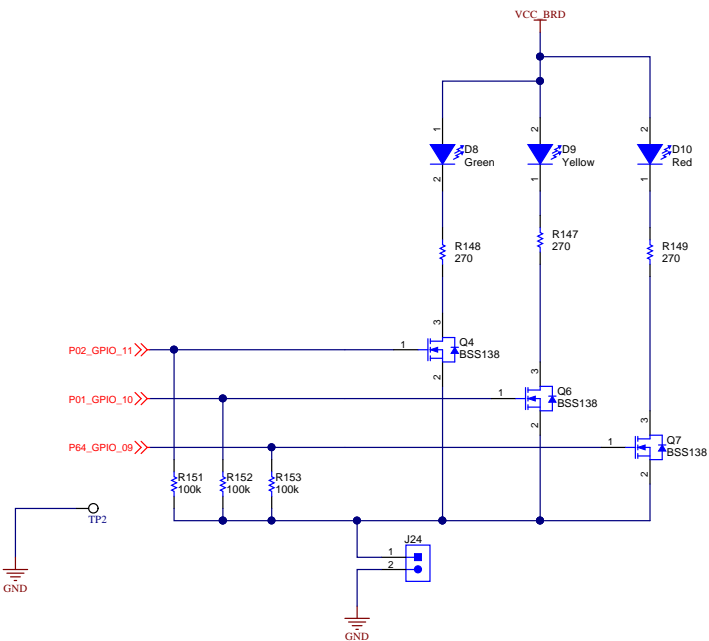
SWITCHES & RESET



POWER MANAGEMENT

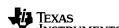


LED INDICATORS



Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: CC3220SF-LAUNCHXL	Designed for: TI CONFIDENTIAL	Mod. Date: 11/1/2016
TID #: N/A	Project Title: WCS002A	
Number: WCS002	Rev: A	Sheet Title: Power LEDs Switch Sensor
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 5 of 6
Drawn By:	File: WCS002A_PowerLedsSwitchSensors.SchDoc	Size: C
Engineer: Prajay Madhavan	Contact: http://www.ti.com/support	http://www.ti.com



© Texas Instruments 2015

