Dual-Supply, Discrete, Programmable Gain Amplifier Circuit



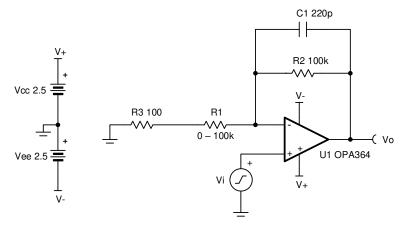
Design Goals

Input		Output		Supply	
V _{iMin}	V _{iMax}	V _{oMin}	V_{oMax}	V _{cc}	V _{ee}
–1.25 V	+1.25 V	–2.4 V	+2.4 V	+2.5 V	–2.5 V

Gain	Cutoff Frequency	
6 dB (2 V/V) to 60 dB (1000 V/V)	7 kHz	

Design Description

This circuit provides programmable, non-inverting gains ranging from 6 dB (2 V/V) to 60 dB (1000 V/V) using a variable input resistance. The design maintains the same cutoff frequency over the gain range.



Design Notes

- 1. Choose a digital potentiometer, such as TPL0102 for R₁ to design a low-cost digital programmable gain amplifier.
- 2. R_3 sets the maximum gain when R_1 approaches 0 Ω .
- 3. A feedback capacitor limits the bandwidth and prevent stability issues.
- 4. Stability should be evaluated across the selected gain range. The minimum gain setting will likely be most sensitive to stability issues.
- 5. Some digital potentiometers can vary in absolute value by as much as ±20% so gain calibration may be necessary.

Design Steps

1. Choose R₂ and R₃, to set the maximum gain when R₁ approaches 0:

$$\begin{split} G_{max} &= 1 + \frac{R_2}{R_3} \\ G_{max} - 1 &= \frac{R_2}{R_3} \rightarrow R_2 = \left(G_{max} - 1\right) \times R_3 \\ \text{Set} \quad R_3 &= 100 \ \Omega \\ R_2 &= \left(1000 \ \frac{V}{V} - 1\right) \times 100 = 99 \ \text{k}\Omega \rightarrow R_2 = 100 \ \text{k}\Omega \quad \left(\text{Standard value}\right) \end{split}$$

2. Choose the potentiometer maximum value to set the minimum gain:

$$\begin{split} G_{min} &= 1 + \frac{R_2}{R_{1,\,max} + R_3} \\ G_{min} - 1 &= \frac{R_2}{R_{1,\,max} + R_3} \\ R_{1,\,max} + R_3 &= \frac{R_2}{G_{min} - 1} \\ R_{1,\,max} &= \frac{R_2}{G_{min} - 1} - R_3 = \frac{100 k\Omega}{2 - 1} - 100\Omega = 99.9 k\Omega \rightarrow R_{1,\,max} = 100 k\Omega \quad \left(\text{Standard value} \right) \\ R_{1,\,min} &= 0\Omega \quad \left(\text{Wiper resistance, typically } 25\Omega, \text{ will introduce some error} \right) \end{split}$$

3. Choose the bandwidth with a feedback capacitor:

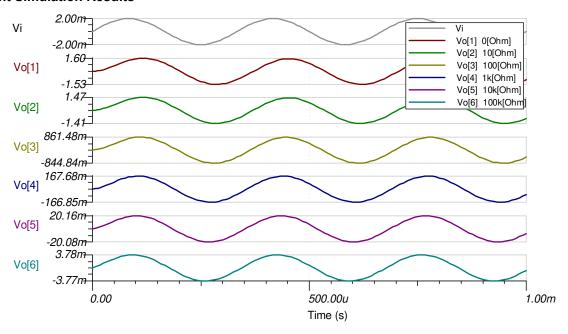
$$\begin{split} f_c &= \frac{GBW}{G_{max}} = \frac{7MHz}{1000\frac{V}{V}} = 7kHz \\ f_c &= 7kHz \rightarrow C_1 = \frac{1}{2\pi \times R_2 \times f_c} = 227pF \quad \rightarrow C_1 = 220pF \quad \left(\text{Standard Value} \right) \end{split}$$

4. Check for stability at minimum gain (2V/V), which is when R_1 =100 k Ω . To satisfy the requirement f_c (circuit bandwidth) must be less than f_{zero} (zero created by the resistive feedback network and the differential and common-mode input capacitances).

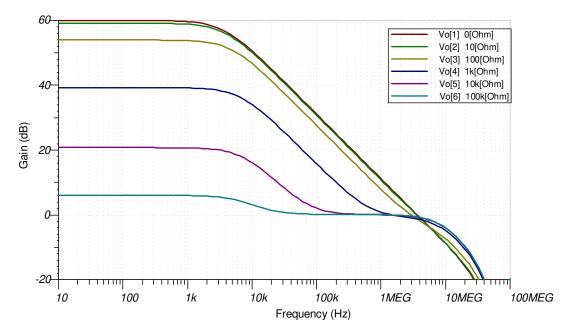
$$\begin{split} f_{c} &= \frac{1}{2\pi \times C_{1} \times R_{2}} = 7 \text{ kHz} \\ f_{zero} &= \frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_{2} \parallel R_{1})} = \frac{1}{2 \times \pi \times \left(3 \text{ pF} + 2 \text{ pF}\right) \times \left(\frac{100 \text{ k}\Omega \times 100 \text{ k}\Omega}{100 \text{ k}\Omega + 100 \text{ k}\Omega}\right)} \\ f_{zero} &= 637 \text{ kHz} \\ 7 \text{ kHz} &< 637 \text{ kHz} \rightarrow f_{c} < f_{zero} \end{split}$$

Design Simulations

Transient Simulation Results



AC Simulation Results



References:

- 1. Analog Engineer's Circuit Cookbooks
- 2. SPICE Simulation File SBOC521
- 3. TI Precision Designs TIPD204
- 4. TI Precision Labs

Design Featured Op Amp

OPA364				
V _{ss}	1.8 V to 5.5 V			
V _{inCM}	Rail-to-rail			
V _{out}	Rail-to-rail			
V _{os}	1 mV			
Iq	1.1 mA			
I _b	1 pA			
UGBW	7 MHz			
SR	5 V/μs			
#Channels	1, 2, and 4			
OPA364				

Design Alternate Op Amp

OPA376				
V _{ss}	2.2 V to 5.5 V			
V _{inCM}	Rail-to-rail			
V _{out}	Rail-to-rail			
V _{os}	5 μV			
Iq	760 µA			
I _b	0.2 pA			
UGBW	5.5 MHz			
SR	2 V/µs			
#Channels	1, 2, and 4			
OPA376				

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