Texas Instruments

Ultra-High Efficiency Buck Converter Using TPS40000/1 Controller Keeps Power System Costs Low, (PR073)

Reference Design

Ultra-High Efficiency Buck Converter using TPS40000/1 Controller Keeps Power System Costs Low, (PR073)

Mark Dennis *Power Supply Control Products*

1 Introduction

The TPS40000 and the TPS40001 are voltage-mode, synchronous buck PWM controllers that utilize TI's proprietary Predictive Gate Drive™ technology to wring maximum efficiency from step-down converters. This controller family provides a bootstrap circuit to allow the use of an N-channel MOSFET as the topside buck switch to reduce conduction losses and increase silicon device utilization. Predictive Gate Drive™ technology controls the delay from main switch turn-off to synchronous rectifier turn-on and also the delay from rectifier turn-off to main switch turn-on. This allows minimization of the losses in the MOSFET body diodes, both conduction and reverse recovery. This design note provides details on a buck converter that converts 3.3 V down to a 2.5-V level utilizing either the TPS40000 or TPS40001 controller.

A schematic for the board is shown in Figure 1. The list of material is provided in a later section of this reference design.

The specification for this board is as follows:

- V_{IN} = 3.0 V to 5 V
- V_{OUT} = 2.5 V
- I_{OUT} = 0– 10 Amps
- Efficiency = >95% with V_{IN} = 3.3 V, load 3 A
- Output voltage ripple < 2% V_{OUT}
- Power semiconductor devices: each MOSFET is a single SO-8 package

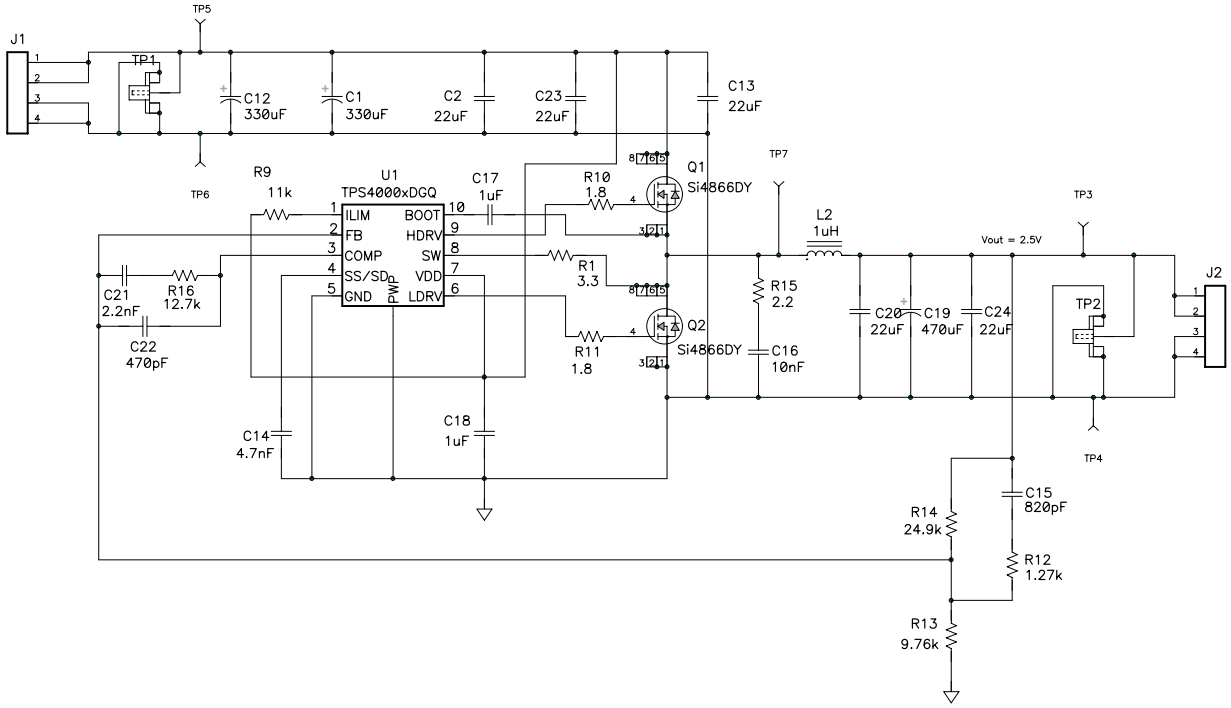

Figure 1. Application Diagram for the TPS40000/1

2 Design Procedure

2.1 TPS4000X Family Device Selection

The TPS4000X family of devices offers four selections to encompass the frequency and output current mode choices. The TPS4000/1 are selected for this high current application because the 300-kHz switching frequency improves efficiency. The TPS40002/3 are available for applications needing 600-kHz operation. The TPS4000X family also allows the user to select discontinuous current mode (DCM) operation or continuous current mode (CCM) operation at lighter loads. In this reference design the TPS40001 is selected to maintain continuous mode operation down to zero load. If desired, the TPS40000 can be installed to turn the synchronous MOSFET OFF when the controller senses the inductor current reaching zero, indicating the circuit is entering the DCM of operation.

2.2 Inductance Value

The output inductor value is selected to set the ripple current to a value most suited to overall circuit functionality. An inductor selection that is too small leads to larger ripple current that increases RMS current losses in the inductor and MOSFETs, also leads to more ripple voltage on the output. The inductor value is calculated by (1)

$$L_{MIN} = \frac{V_{OUT}}{f \times I_{RIPPLE}} \left(1 - \frac{V_{OUT}}{V_{IN(max)}} \right) \quad (1)$$

in which I_{RIPPLE} is chosen to be 25% of I_{OUT}, or 2.5 A. At V_{IN} = 5 V this equation calls for 1.2 μH. When considering standard inductor values in a fixed size, the smaller inductor values generally has less resistance because reduced turns equates to more room for copper in the winding area. Since this design is aimed for high efficiency, a standard value of 1 μH is selected, and the resistance is only 3.5 mΩ. At full load the power loss is only 0.35 W, which is only 1.4% of the 25-W output power.

2.3 Input Capacitor Selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this standalone supply, onboard capacitance is added to handle input voltage ripple and RMS current considerations. For this power level, input voltage ripple of 150 mV is reasonable, and the minimum capacitance is calculated in equation (2).

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{10\ A \times 2.5\ \mu s}{0.15\ V} = 167\ \mu F \quad (2)$$

In addition to this minimum capacitance requirement, the RMS current stresses must be considered. In this converter, the large duty cycle causes the input RMS current to be nearly as large as the output current, as shown in equation (3), which is a simplified formula for the RMS current for a trapazoidal current waveform.

$$I_{RMS} = I \times \sqrt{D} \quad (3)$$

Additional terms for the ripple component of the current add only a few percent to the total RMS current, so the ripple contribution can be negglected. With V_{IN} = 3.3 V and I_{OUT} = 10 A the input RMS current is 8.7 A. To meet this initial requirement with small size and cost, a combination of capacitors is considered. To carry the high frequency ripple current, three 22-μF, X5R ceramic capacitors are placed close to the power circuitry. Although these capacitors have an extremely small resistance the datasheet indicates that the part undergoes a 30°C temperature rise with 2 A_{RMS} current at 500 kHz and therefore more current capability is needed. Two 330-μF POSCAPs with an RMS current capability of 4.4 A each is selected. In typical embedded converters, these POSCAPs is not required if the upstream converter feeding this buck has sufficient capacitance to handle the ripple current.

2.4 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. A variety of solutions is possible. First, the minimum allowable output capacitance should be determined by the amount of inductor ripple current and the allowable output ripple, as given in equation (4).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} \quad (4)$$

In this design, $C_{OUT(min)}$ is 42 μF with V_{RIPPLE} = 25 mV. However, this only affects the capacitive component of the ripple voltage. In addition, the voltage component due to the capacitor ESR must be considered, as shown in equation (5).

$$C_{ESR} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (5)$$

To minimize capacitor size and cost, a 470-μF OSCON in paralleled with two 22-μF ceramic capacitors.

2.5 MOSFET Selection

One constraint in this design is the use of one SO-8 MOSFET in the upper switch device and one SO-8 in the lower synchronous rectifier location in the buck converter power stage. The upper device loss is usually dominated by switching loss, so a device with lower gate charge and switching times was selected. With the high output voltage, the upper device runs at a high duty cycle and needs to have a low $R_{DS(on)}$ to keep conduction losses low, and an 8-mΩ device with a maximum gate charge of 30 nC is selected. The same device is fitted in the bottom switch location to achieve high efficiency.

2.6 Short Circuit Protection

The TPS40003 implements short circuit protection by comparing the voltage across the topside MOSFET while it is ON to a voltage dropped from VDD by R_{LIM} due to an internal current source of 15 μA inside pin 1. Due to tolerances in the current source and variations in the power MOSFET ON-voltage versus temperature, the short circuit level can protect against gross overcurrent conditions only, and should be set much higher than rated load. In this particular case, R_{LIM} is selected as shown in equation (6).

$$R_{LIM} = R1 = \frac{2 \times \left(I_{OUT}\right) \times R_{DS(on)}}{15\ \mu A} \quad (6)$$

For this design, R_{LIM} = 11 kΩ, and the factor of 2 in the equation accounts for the variations in component tolerances and output current ripple. The high currents that are switched under short circuit conditions may cause SW pin 8 to be driven below ground several volts, possibly injecting substrate current which can cause improper operation of the device. A 3.3-Ω resistor has been placed in series with this pin to limit its excursion to safe levels.

2.7 Compensation Design

The TPS40000 uses voltage mode control in conjunction with a high frequency error amplifier. The power circuit L-C double pole corner frequency f_C is situated at 7 kHz, and the output capacitor ESR zero is near 33 kHz. The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed at the origin to improve dc regulation.

The first zero is placed just below f_C at 5.7 kHz,

$$f_{z1} = \frac{1}{2 \times \pi \times R_{16} \times C_{21}} \tag{7}$$

The second zero is selected at f_C,

$$f_{z2} = \frac{1}{2 \times \pi \times \left(R_{12} + R_{14}\right) \times C_{C15}} \tag{8}$$

The first poles is placed near the ESR zero frequency,

$$f_{p1} = \frac{1}{2 \times \pi \times R_{16} \times \left(\frac{C_{21} \times C_{22}}{C_{21} + C_{22}}\right)} \tag{9}$$

and the second pole is placed at one-half the switching frequency,

$$f_{p2} = \frac{1}{2 \times \pi \times R_{12} \times C_{15}} \tag{10}$$

2.8 Snubber Component selection

The switch node where Q1 and L1 come together is very noisy. An R-C network fitted between this node and ground can help reduce ringing and voltage overshoot on Q2. This ringing noise should be minimized to prevent it from confusing the control circuitry which is monitoring this node for current limit, Predictive Gate Drive™, and DCM control functions.

As a starting point, the snubber capacitor, C16, is generally chosen to be 5 to 8 times larger than the parasitic capacitance at the node, which is primarily C_{OS} of Q2. Since C_{OS} is around 1600 pF for Q2 at 5 V, C8 is chosen to be 10 nF. R2 is empirically determined to be 2.2 Ω, which minimizes the ringing and overshoot at the switch node. With the relatively low input voltage of 5 V, the power loss, ½ CV^2f , is relatively small at 37 mW.

3 PowerPAD Packaging

The TPS4000X family is available in the DGQ version of TI's PowerPAD™ thermally enhanced package. In the PowerPAD™, the integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The leadframe die pad is exposed on the bottom side of the package, and can be soldered to the PCB using standard solder flow techniques. This construction technique provides extremely low thermal resistance from the junction to the PCB ambient temperature.

The PowerPAD™ package helps to keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

To effectively remove heat from the PowerPAD™ package, a thermal land should be provided directly underneath the package. This thermal land usually has vias that help to spread heat to internal copper layers and/or the opposite side of the PCB. The vias should not have thermal reliefs that are often used on ground planes, because this reduces the copper area to transfer heat. Additionally, the vias should be small enough so that the holes are effectively plugged when plated. This prevents the solder from wicking away from the connection between the PCB surface and the bottom of the part. A typical footprint pattern is shown in Figure 2, but does not include the additional copper plane which would include the vias above and below the device.

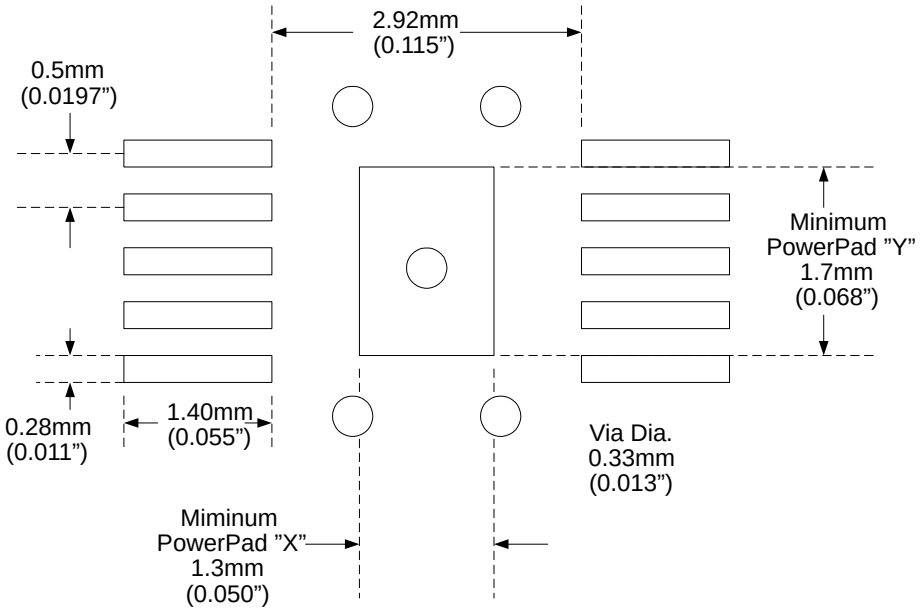

Figure 2. PowerPAD Land

The Texas Instrument document, *PowerPAD Thermally Enhanced Package Application Report* (Ti Literature number SLMA002) should be consulted for more information on the PowerPAD™ package. This report offers in-depth information on the package, assembly and rework techniques, and illustrative examples of the thermal performance of the PowerPAD™ package.

4 Test Results/Performance Data

Typical efficiency curves are shown in Figure 3 for a nominal 3.3-V input.

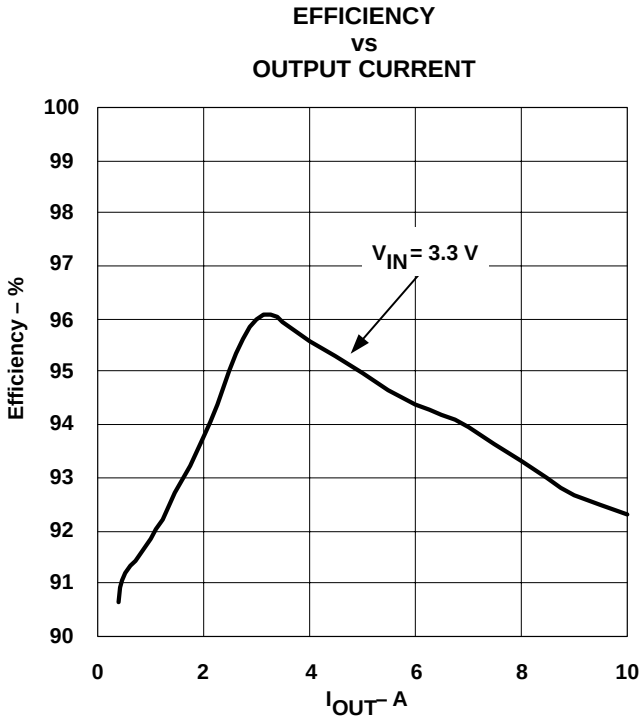

Figure 3.

Figure 4 shows the switch node at V_{IN} = 3.3 V and I_{OUT} = 10 A.

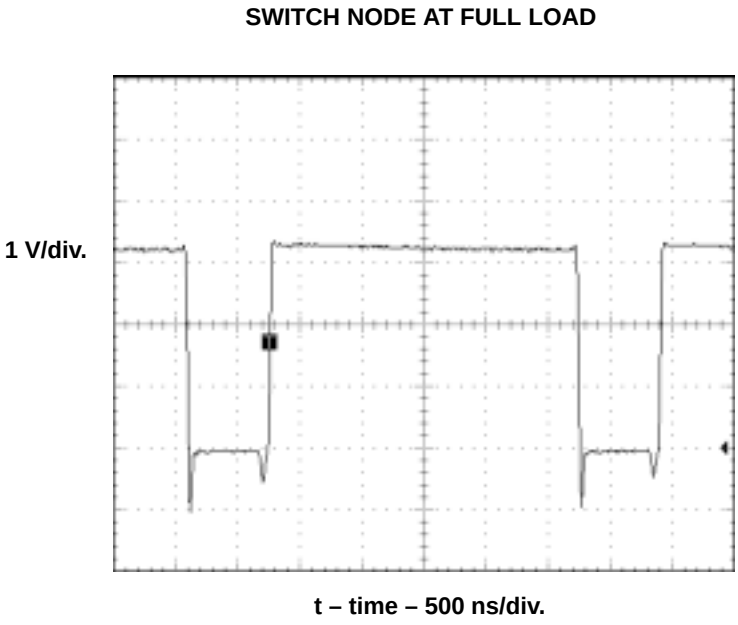

Figure 4.

Figure 5 shows the output voltage ripple with the selected components.

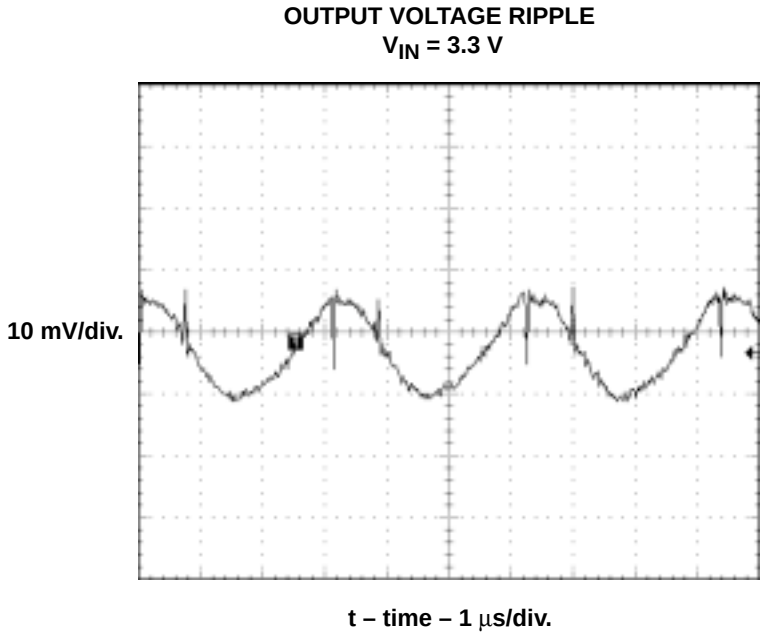

Figure 5.

5 PCB layout

PCB layout details are available in both Gerber and PCAD format.

6 List of Material

	Qty	Reference	Description	Manufacturer	Part Number
Capacitor	2	C1, C12	POSCAP, 330 µF, 6.3 V, 10 mΩ, 20%, 7343 (D)	Sanyo	6TPD330M
	1	C14	Ceramic, 0.0047 µF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y472KXAAT
	1	C15	Ceramic, 820 pF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y821KXAAT
	1	C16	Ceramic, 0.01 µF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y103KXAAT
	2	C17, C18	Ceramic, 1 µF, 10 V, X5R, 10%, 805	Panasonic	ECJ–2YB1A105K
	1	C19	POSCAP, 470 µF, 4 V, 10 mΩ, 20%, 7343 (D)	Sanyo	4TPD470M
	5	C2, C13, C20, C23, C24	Ceramic, 22 µF, 6.3 V, X5R, 20%, 1210	Panasonic	ECJ–4YB0J226M
	1	C21	Ceramic, 0.0022 µF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y222KXAAT
	1	C22	Ceramic, 470 pF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y471KXAAT
Terminal Block	2	J1, J2	4-pin, 15 A, 5.1 mm, 291126	OST	ED2227
Inductor	1	L2	SMT, 1 µH, 15 A, 3.5 mΩ, 0.51 x 0.51	Vishay	IHLP–5050CE–01 1.0 µH 20%
MOSFET	2	Q1, Q2	N-channel, 12 V, 17 A, 5.5 mΩ, SO8	Siliconix	Si4866DY
Resistor	1	R1	Chip, 3.3 Ω, 1/10 W, 5%, 805	Std	Std
	2	R10, R11	1.8 Ω, 1/10 W, 5%, 805	Std	Std
	1	R12	Chip, 1.27 kΩ, 1/10 W, 1%, 805	Std	Std
	1	R13	Chip, 9.76 kΩ, 1/10 W, 1%, 805	Std	Std
	1	R14	Chip, 24.9 kΩ, 1/10 W, 1%, 805	Std	Std
	1	R15	Chip, 2.2 Ω, 1/10 W, 5%, 805	Std	Std
	1	R16	Chip, 12.7 kΩ, 1/10 W, 1%, 805	Std	Std
	1	R9	Chip, 11 kΩ, 1/10 W, 1%, 805	Std	Std
Adaptor	2	TP1, TP2	3.5-mm probe clip (or 131–5031–00), 72900	Tektronix	131–4244–00
Test Point	3	TP3, TP5, TP7	Red, 1 mm, 0.038”, 6400”	Farnell	240–345
	2	TP4, TP6	Black, 1 mm, 0.038”, 6400”	Farnell	240–333
Device	1	U1	Low Input Voltage Mode, Sync. Buck Controller, DGQ10	TI	TPS40001DGQ

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