

Gas Gauge IC with External Charge Control

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output operates an external charge controller such as the bq2004 Fast Charge IC
- Designed for battery pack integration
 - 120µA typical standby current
- Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- User-selectable end-of-discharge threshold
- Battery voltage, nominal available charge, temperature, etc. available over serial port
- 16-pin narrow SOIC

General Description

The bq2014 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The IC monitors the voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or “learned,” in the course of a discharge cycle from full to empty.

The bq2014 includes a charge control output that controls an external Fast Charge IC such as the bq2004.

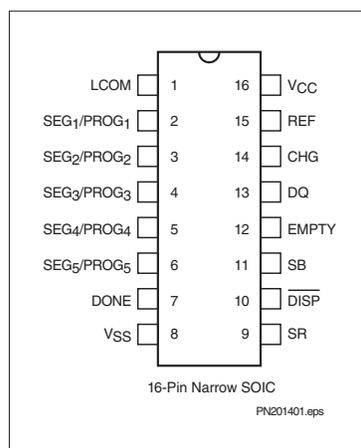
Nominal Available Charge (NAC) may be directly indicated using a five-segment LED display.

The bq2014 supports a simple single-line bidirectional serial link to an external processor (with a common ground). The bq2014 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, temperature, capacity, battery voltage, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2014 gas gauge data registers.

The bq2014 may operate directly from three or four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide VCC across a greater number of cells.

Pin Connections



Pin Names

LCOM	LED common output	REF	Voltage reference output
SEG ₁ /PROG ₁	LED segment 1/ program 1 input	CHG	Charge control output
SEG ₂ /PROG ₂	LED segment 2/ program 2 input	DQ	Serial communications input/output
SEG ₃ /PROG ₃	LED segment 3/ program 3 input	EMPTY	Empty battery indicator output
SEG ₄ /PROG ₄	LED segment 4/ program 4 input	SB	Battery sense input
SEG ₅ /PROG ₅	LED segment 5/ program 5 input	$\overline{\text{DISP}}$	Display control input
DONE	Fast charge complete	SR	Sense resistor input
		VCC	3.0–6.5V
		VSS	System ground

bq2014

Pin Descriptions

LCOM	LED common output Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down programming resistors. LCOM is also in a high impedance state when the display is off.
SEG₁–SEG₅	LED display segment outputs (dual function with PROG₁–PROG₅) Each output may activate an LED to sink the current sourced from LCOM.
PROG₁–PROG₅	Programmed full count selection inputs (dual function with SEG₁–SEG₅) These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.
PROG₃–PROG₄	Gas gauge rate selection inputs (dual function with SEG₃–SEG₄) These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.
PROG₅	Self-discharge rate selection (dual function with SEG₅) This three-level input pin defines the self-discharge compensation rate shown in Table 1.
CHG	Charge control output This open-drain output becomes active high when charging is allowed.
DONE	Fast charge complete This input is used to communicate the status of an external charge controller such as the bq2004 Fast Charge IC. Note: This pin must be pulled down to V_{SS} using a 200K Ω resistor.

SR	Sense resistor input The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop V_{SRO} , as seen by the bq2014, is $V_{SR} + V_{OS}$ (see Table 5).
DISP	Display control input \overline{DISP} high disables the LED display. \overline{DISP} tied to V_{CC} allows PROG _X to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. DISP floating allows the LED display to be active during a valid charge or during discharge if the NAC register is updated at a rate equivalent to $V_{SRO} \leq -4mV$. DISP low activates the display. See Table 1.
SB	Secondary battery input This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.
EMPTY	Battery empty output This open-drain output becomes high-impedance on detection of a valid final end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.
DQ	Serial I/O pin This is an open-drain bidirectional pin.
REF	Voltage reference output for regulator REF provides a voltage reference output for an optional micro-regulator.
VCC	Supply voltage input
VSS	Ground

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Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2014 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{R2}{R3} = N - 1$$

where N is the number of cells, R2 is connected to the positive battery terminal, and R3 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an “empty” state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2014 are programmable with the default values fixed at:

$$EDV1 \text{ (early warning)} = 1.05V$$

$$EDVF \text{ (empty)} = 0.95V$$

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB} , until the next valid charge (as defined in the section entitled “Gas Gauge Operation”). The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2014 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq -250mV$ typical and resumes $\frac{1}{2}$ second after $V_{SR} > -250mV$.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDVF}$ and remains latched until a valid charge occurs.

Reset

The bq2014 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V (V_{MCV}) resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2014 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate

compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2014 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C2 and C3) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC} .
- The sense resistor (R1, C1) should be placed as close as possible to the SR pin.
- The sense resistor (R16) should be as close as possible to the bq2014.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2014. The bq2014 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2014 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

Many actions in the bq2014 are triggered by detection of a “valid charge.” NAC is stored in an asynchronous, 2-byte counter; the lower byte is NACL and the upper byte is NACH. A valid charge has occurred anytime the

charge lasts long enough to cause an increment in NACH. Small increments of charging are not considered “valid” if they result in counts in NACL but do not generate a roll-over (carry) that increments NACH. NACL is reset anytime the counter direction changes from down to up, so the number of counts required to cause a roll-over and a valid charge is always 256. The counter may be incrementing by 2, 4, 8, or more counts per increment, however, depending on the scaling factors selected. Therefore, a valid charge may be constituted by a smaller number of counter increments.

1. Last Measured Discharge (LMD) or learned battery capacity:

LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), $LMD = PFC$. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using $PROG_1$ — $PROG_4$. The bq2014 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be

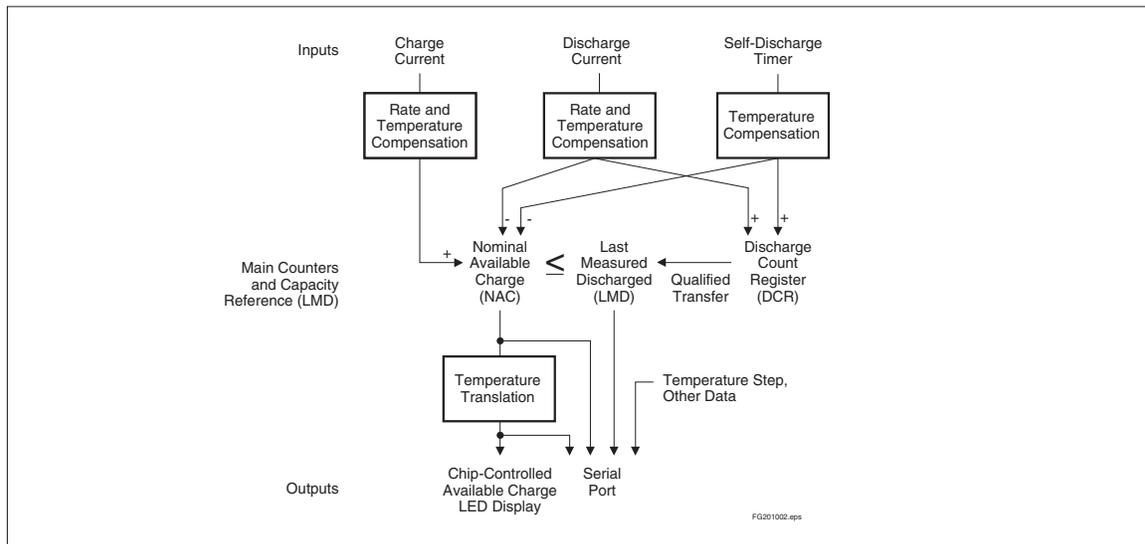


Figure 2. Operational Overview

bq2014

determined by multiplying the rated battery capacity in mAh by the sense resistor value:

$$\text{Battery capacity (mAh)} * \text{sense resistor } (\Omega) =$$

$$\text{PFC (mVh)}$$

Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

- Sense resistor = 0.1Ω
- Number of cells = 6
- Capacity = 2200mAh, NiCd battery
- Current range = 50mA to 2A

Relative display mode

Serial port only

Self-discharge = %₆₄

Voltage drop over sense resistor = 5mV to 400mV

Therefore:

$$2200\text{mAh} * 0.1\Omega = 220\text{mVh}$$

Select:

PFC = 33792 counts or 211mVh

PROG₁ = float

PROG₂ = float

PROG₃ = float

PROG₄ = low

PROG₅ = float

DONE = low

Table 1. bq2014 Programming

Pin Connection	PROG ₅ Self-Discharge Rate	DISP Display State
H	Disabled	LED disabled
Z	NAC/ ₆₄	LED enabled on discharge when V _{SRO} < -4mV or during a valid charge
L	NAC/ ₄₇	LED on

Table 2. bq2014 Programmed Full Count mVh Selections

PROG _x		Programmed Full Count (PFC)	PROG ₄ = L			PROG ₄ = Z			Units
1	2		PROG ₃ = H	PROG ₃ = Z	PROG ₃ = L	PROG ₃ = H	PROG ₃ = Z	PROG ₃ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/s (nom.)			90	45	22.5	11.25	5.6	2.8	mV

The initial full battery capacity is 211mVh (2110mAh) until the bq2014 “learns” a new capacity with a qualified discharge from full to EDV1.

3. Nominal Available Charge (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge after $EDV = 1$. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when $NAC = LMD$.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0 until $V_{SB} < EDV1$. Prior to $NAC = 0$ (empty battery), both discharge and self-discharge increment the DCR. After $NAC = 0$, only discharge increments the DCR. The DCR resets to 0 when $NAC = LMD$. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

- No valid charges have occurred during the period between $NAC = LMD$ and $EDV1$ detected.
- The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
- The temperature is $\geq 0^{\circ}\text{C}$ when the $EDV1$ level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. The bq2014 determines charge activity sustained at a continuous rate equivalent to V_{SRO} ($V_{SR} + V_{OS}$) $> V_{SRQ}$. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ} . V_{SRQ} is a programmable threshold (as described in the Digital Magnitude Filter section) and has a default value of $375\mu\text{V}$. If charge activity is detected, the bq2014 increments the NAC at a rate proportional to V_{SRO} . If enabled, the bq2014 then activates an LED display. Charge actions increment the NAC after compensation for charge rate and temperature.

Charge Control

Charge control is provided by the CHG output. This output is asserted continuously when $NAC > 0.94 * LMD$. CHG is also asserted when a valid charge is detected (CHGS in the FLGS1 register is also set). CHG is low when $NAC < 0.94 * LMD$ and there is no valid charge activity.

DONE Input

When the bq2014 detects a valid charge complete with an active-high signal on the DONE input, NAC is set to LMD for NAC_{64} (NiCd) self-discharge setting. NAC is set to 94% of LMD (if NAC is below 94%) for NAC_{47} (NiMH) self-discharge setting. VDQ is set along with DONE.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment if $EDV1 = 0$. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to $V_{SRO} < -4\text{mV}$ activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV . V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is $-300\mu\text{V}$.

Self-Discharge Estimation

The bq2014 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $\frac{1}{64} * NAC$ or $\frac{1}{47} * NAC$ per day or disabled as selected by $PROG5$. This is the rate for a battery whose temperature is between 20°C – 30°C . The NAC register cannot be decremented below 0.

Count Compensations

The bq2014 determines fast charge when the NAC updates at a rate of ≥ 2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec ($\geq 0.15\text{C}$ to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

bq2014

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
< 40°C	0.80	0.95
> 40°C	0.75	0.90

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR} .

The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
$V_{SR} > -150$ mV	1.00	100%
$V_{SR} < -150$ mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 * N)$$

Where N = number of 10°C steps below 10°C and $-150\text{mV} < V_{SR} < 0$.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $\frac{1}{64} * \text{NAC}$ per day, $\frac{1}{47} * \text{NAC}$ per day, or disabled. This is the rate for a battery within the 20°C–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	PROG ₅ = Z	PROG ₅ = L
< 10°C	NAC/ ₂₅₆	NAC/ ₁₈₈
10–20°C	NAC/ ₁₂₈	NAC/ ₉₄
20–30°C	NAC/ ₆₄	NAC/ ₄₇
30–40°C	NAC/ ₃₂	NAC/ _{23.5}
40–50°C	NAC/ ₁₆	NAC/ _{11.8}
50–60°C	NAC/ ₈	NAC/ _{5.88}
60–70°C	NAC/ ₄	NAC/ _{2.94}
> 70°C	NAC/ ₂	NAC/ _{1.47}

Digital Magnitude Filter

The bq2014 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ} . The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD} \text{ (mV)} = \frac{-45}{\text{DMF}}$$

$$V_{SRQ} \text{ (MV)} = -125 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR} . A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} ($V_{SR} + V_{OS}$) is between V_{SRQ} and V_{SRD} .

Communicating With the bq2014

The bq2014 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2014 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2014 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2014. The command directs the bq2014 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using

either polled or interrupt processing. Data input from the bq2014 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2014. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR} . The bq2014 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2014 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU} , after the negative edge used to start communication. The data should be held for a period, t_{DV} , to allow the host or bq2014 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU} , after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV} , to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2014 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2014 NAC register.

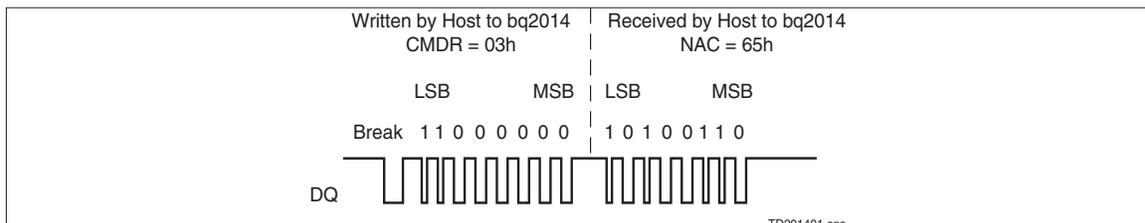


Figure 3. Typical Communication With the bq2014

bq2014

bq2014 Registers

The bq2014 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2014. The CMDR register contains two fields:

- $\overline{W/R}$ bit
- Command address

The $\overline{W/R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The $\overline{W/R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
$\overline{W/R}$	-	-	-	-	-	-	-

Where $\overline{W/R}$ is:

- 0 The bq2014 outputs the requested register contents specified by the address portion of CMDR.
- 1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2014 flags.

The **charge status** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

- 0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$
- 1 $V_{SRO} > V_{SRQ}$

The **battery replaced** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB} , falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2014 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

- 0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted
- 1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The **battery removed** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed. Because of signal filtering, 30 seconds may have to transpire for BRM to react to battery insertion or removal.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

- 0 $0.1V < V_{SB} < 2.25V$
- 1 $0.1V > V_{SB}$ or $V_{SB} > 2.25V$

The **capacity inaccurate** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2014 is reset. The flag is cleared after an LMD update.

Table 6. bq2014 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W \bar{R}	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVL
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0Ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
VSB	Battery voltage	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

bq2014

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

- 0 When LMD is updated with a valid full discharge
- 1 After the 64th valid charge action with no LMD updates or when the device is reset

The **valid discharge** flag (VDQ) is asserted when the bq2014 is discharged from NAC = LMD or DONE is valid. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

- 0 $SDCR \geq 4096$, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C
- 1 On first discharge after NAC = LMD or DONE is valid

The **first end-of-discharge warning** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG₁, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

- 0 Valid charge action detected, $V_{SB} \geq V_{TS}$
- 1 $V_{SB} < V_{TS}$ providing that OVLD=0 (see FLGS2 register description)

The **final end-of-discharge warning** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery. The EDVF threshold is set 100mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

- 0 Valid charge action detected, $V_{SB} \geq V_{TS} - 100\text{mV}$
- 1 $V_{SB} < V_{TS} - 100\text{mV}$ providing that OVLD=0 (see FLGS2 register description)

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address=0ch). The read/write VTS register sets the EDV1 trip point. EDVF is set 100mV below EDV1. The default value in the VTS register is 70h, representing EDV1 = 1.05V and EDVF = 0.95V. $EDV1 = 2.4V * (VTS/256)$.

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register is updated approximately once per second with the present value of the battery voltage.

$$V_{SB} = 2.4V * (VSB/256)$$

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2014 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

The bq2014 calculates the available charge as a function of NAC, temperature, and LMD. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Register (NACH/NACL)

The read/write NACH register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging registers for the bq2014. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

On reset, NACH and NACL are cleared to 0. When the bq2014 detects a charge, NACL resets to 0. NACH and NACL are reset to 0 on the first valid charge after $V_{SB} = EDV1$. Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2014 gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2014. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2014 uses as a measured full reference. The bq2014 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2014 updates the capacity of the battery. LMD is set to PFC during a bq2014 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2014 flags.

The **charge rate** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

bq2014

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

- 0 When charge rate falls below 2 counts/sec
- 1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The **discharge rate** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	-

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	$V_{SR} > -150\text{mV}$
0	0	1	$V_{SR} < -150\text{mV}$

The **overload** flag (OVLD) is asserted when a discharge overload is detected, $V_{SR} < -250\text{mV}$. OVLD remains asserted as long as the condition persists and is cleared after $V_{SR} > -150\text{mV}$. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination when excessive discharges occur.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS} . The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2014. The segment drivers, SEG_{1–5} and DONE, have corresponding PPD register locations, PPD_{1–6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG₁ and SEG₄ have

pull-down resistors, the contents of PPD are xx101001. (**Note:** DONE must be pulled down for proper operation.)

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2014. The segment drivers, SEG_{1–5} and DONE, have corresponding PPU register locations, PPU_{1–6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG₃ and DONE have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	PPU ₆	PPU ₅	PPU ₄	PPU ₃	PPU ₂	PPU ₁
-	-	PPD ₆	PPD ₅	PPD ₄	PPD ₃	PPD ₂	PPD ₁

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2014 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When $NAC > 0.94 * LMD$, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until $NAC < 0.94 * LMD$. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address=0Ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2014. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2014 reset is performed. *Setting any bit other than the most-significant bit of the RST register is **not allowed**, and results in improper operation of the bq2014.*

Resetting the bq2014 sets the following:

- LMD = PFC
- CPI, VDQ, NAC, and NACL = 0
- CI and BRP = 1

Note: Self-discharge is disabled when PROG₅ = H.

Display

The bq2014 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2014 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{\text{DISP}}$ is tied to V_{CC}, the SEG₁₋₅ outputs are inactive. **Note: $\overline{\text{DISP}}$ must be tied to V_{CC} if the LEDs are not used.** When $\overline{\text{DISP}}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to V_{SRO} < -4mV or charge current is detected, V_{SRO} > V_{SRQ}. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{\text{DISP}}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz, with each segment bank active for 30% of the period.

SEG₁ blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2014 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2014, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2014 can be inexpensively built using the FET and an external resistor; see Figure 1.

bq2014

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V _{CC}	Relative to V _{SS}	-0.3	7.0	V	
All other pins	Relative to V _{SS}	-0.3	7.0	V	
REF	Relative to V _{SS}	-0.3	8.5	V	Current limited by R1 (see Figure 1)
V _{SR}	Relative to V _{SS}	-0.3	7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2014 application note for details).
T _{OPR}	Operating temperature	0	70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (T_A = T_{OPR}; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V _{EDVF}	Final empty warning, default	0.92	0.95	0.98	V	SB
V _{EDV1}	First empty warning, default	1.02	1.05	1.08	V	SB
V _{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR
V _{SRO}	SR sense range	-300	-	2000	mV	SR
V _{OVLD}	Overload threshold	-220	-250	-280	mV	SR
V _{SRQ}	Valid charge	375	-	-	μV	V _{SR} + V _{OS} (see note 1)
V _{SRD}	Valid discharge	-	-	-300	μV	V _{SR} + V _{OS} (see note 1)
V _{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V _{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

- Notes:**
1. Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guide lines should be followed for optimal performance.
 2. To ensure correct threshold determination and proper operation, V_{CC} > V_{SB} + 1.5V

DC Electrical Characteristics (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V _{CC}	Supply voltage	3.0	4.25	6.5	V	V _{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V _{OS}	Offset referred to V _{SR}	-	±50	±150	μV	DISP = V _{CC}
V _{REF}	Reference at 25°C	5.7	6.0	6.3	V	I _{REF} = 5μA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I _{REF} = 5μA
R _{REF}	Reference input impedance	2.0	5.0	-	MΩ	V _{REF} = 3V
I _{CC}	Normal operation	-	90	135	μA	V _{CC} = 3.0V
		-	120	180	μA	V _{CC} = 4.25V
		-	170	250	μA	V _{CC} = 6.5V
V _{SB}	Battery input	-	-	2.4	V	
R _{SBmax}	SB input impedance	10	-	-	MΩ	0 < V _{SB} < V _{CC}
I _{DISP}	DISP input leakage	-	-	5	μA	V _{DISP} = V _{SS}
I _{LCOM}	LCOM input leakage	-0.2	-	0.2	μA	DISP = V _{CC}
R _{DQ}	Internal pulldown	500	-	-	KΩ	
V _{SR}	Sense resistor input	-0.3	-	2.0	V	V _{SR} < V _{SS} = discharge; V _{SR} > V _{SS} = charge
R _{SR}	SR input impedance	10	-	-	MΩ	-200mV < V _{SR} < V _{CC}
V _{IH}	Logic input high	V _{CC} - 0.2	-	-	V	PROG ₁ –PROG ₅
V _{IL}	Logic input low	-	-	V _{SS} + 0.2	V	PROG ₁ –PROG ₅ ; note 2
V _{IZ}	Logic input Z	float	-	float	V	PROG ₁ –PROG ₅
V _{OLSL}	SEG _X output low, low V _{CC}	-	0.1	-	V	V _{CC} = 3V, I _{OIS} ≤ 1.75mA SEG ₁ –SEG ₅
V _{OLSH}	SEG _X output low, high V _{CC}	-	0.4	-	V	V _{CC} = 6.5V, I _{OIS} ≤ 11.0mA SEG ₁ –SEG ₅
V _{OHLCL}	LCOM output high, low V _{CC}	V _{CC} - 0.3	-	-	V	V _{CC} = 3V, I _{OHLCOM} = -5.25mA
V _{OHLCH}	LCOM output high, high V _{CC}	V _{CC} - 0.6	-	-	V	V _{CC} = 6.5V, I _{OHLCOM} = -33.0mA
I _{IH}	PROG ₁₋₅ input high current	-	1.2	-	μA	V _{PROG} = V _{CC} /2
I _{IL}	PROG ₁₋₅ input low current	-	1.2	-	μA	V _{PROG} = V _{CC} /2
I _{OHLCOM}	LCOM source current	-33	-	-	mA	At V _{OHLCH} = V _{CC} - 0.6V
I _{OIS}	SEG _X sink current	-	-	11.0	mA	At V _{OLSH} = 0.4V
I _{OL}	Open-drain sink current	-	-	5.0	mA	At V _{OL} = V _{SS} + 0.3V DQ, EMPTY, CHG
V _{OL}	Open-drain output low	-	-	0.5	V	I _{OL} ≤ 5mA, DQ, EMPTY
V _{IHDQ}	DQ input high	2.5	-	-	V	DQ
V _{ILDQ}	DQ input low	-	-	0.8	V	DQ
R _{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	PROG ₁ –PROG ₅
R _{FLOAT}	Float state external impedance	-	5	-	MΩ	PROG ₁ –PROG ₅

- Notes:**
1. All voltages relative to V_{SS}.
 2. DONE must be pulled low for proper operation.

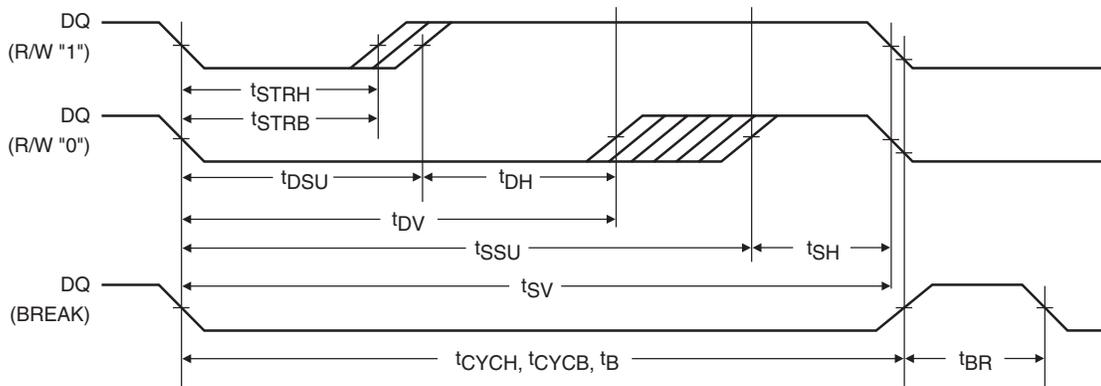
bq2014

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t _{CYCH}	Cycle time, host to bq2014	3	-	-	ms	See note
t _{CYCB}	Cycle time, bq2014 to host	3	-	6	ms	
t _{STRH}	Start hold, host to bq2014	5	-	-	ns	
t _{STRB}	Start hold, bq2014 to host	500	-	-	μs	
t _{DSU}	Data setup	-	-	750	μs	
t _{DH}	Data hold	750	-	-	μs	
t _{DV}	Data valid	1.50	-	-	ms	
t _{SSU}	Stop setup	-	-	2.25	ms	
t _{SH}	Stop hold	700	-	-	μs	
t _{SV}	Stop valid	2.95	-	-	ms	
t _B	Break	3	-	-	ms	
t _{BR}	Break recovery	1	-	-	ms	

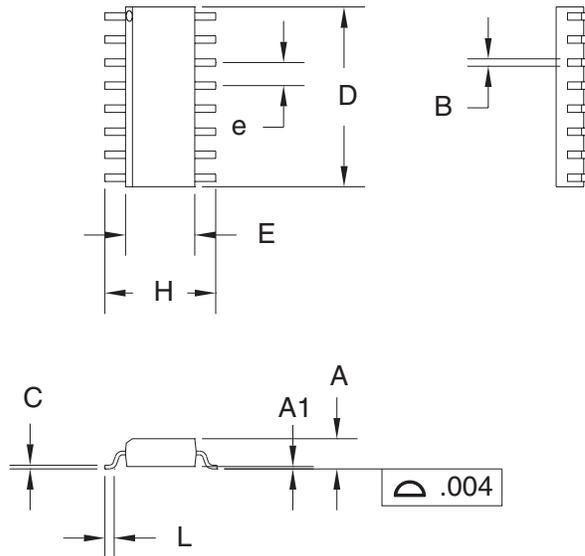
Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



TD201002.eps

16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.

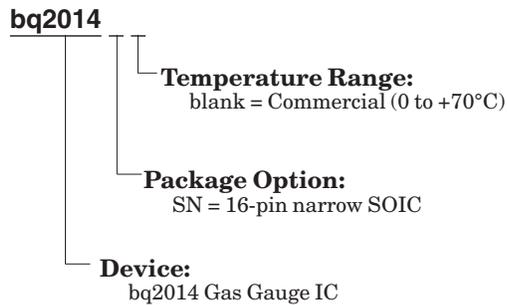
Data Sheet Revision History

ChangeNo.	Page No.	Description	Nature of Change
1	1, 3, 5, 6, 7, 13, 15	Changed display mode	Relative display mode only
1	1, 17	DONE pin	Removed PROG ₆
1	2, 17	DONE pin	Added: DONE pin must be pulled to V _{SS} with a 200KΩ resistor
1	6	Table 1	Removed PROG ₆
1	7	DONE input	Was: NAC is set to 90%... Is: NAC is set to 94%...
1	8, Table 3	PROG ₅ = Z	Was: PROG ₅ = Z or H Is: PROG ₅ = Z
2	8	Temperature Compensation table	Replaced
2	6	Table 2	Added V _{SR} definition
2	6	Valid charge definition	Added definition
2	14	Overload flag	Was: 0.5sec. after V _{SR} > -250mV Is: after V _{SR} = -150mV

Notes: Change 1 = Dec. 1994 B "Final" changes from Aug. 1994 A "Preliminary."
Change 2 = Dec. 1995 C from Dec. 1994 B.

bq2014

Ordering Information



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2014SN-D120	Last Time Buy	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2014 D120
BQ2014SN-D120.B	Last Time Buy	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2014 D120
BQ2014SN-D120TR	Last Time Buy	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2014 D120
BQ2014SN-D120TR.B	Last Time Buy	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2014 D120

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

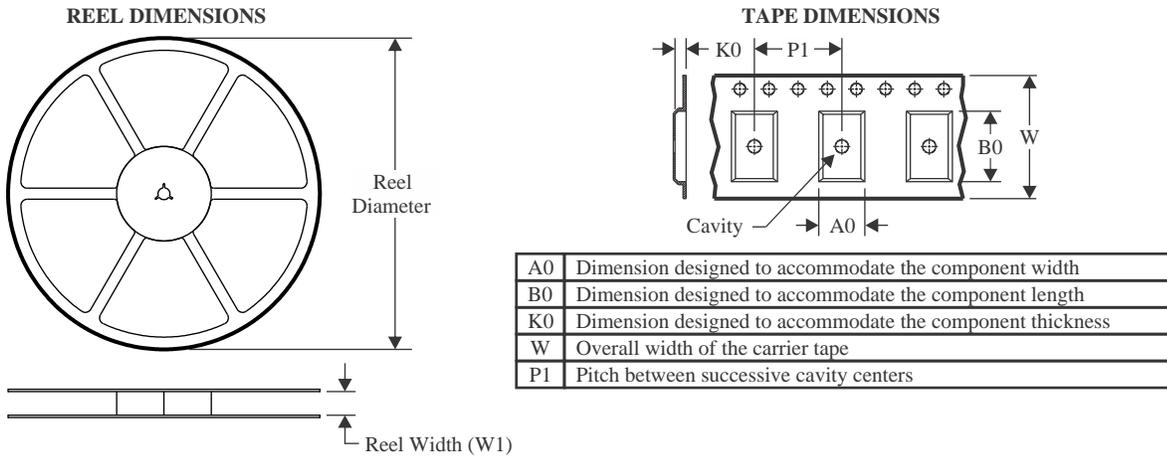
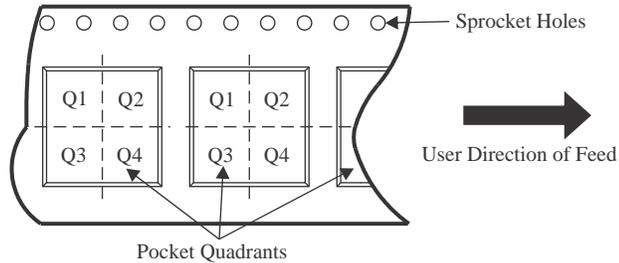
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


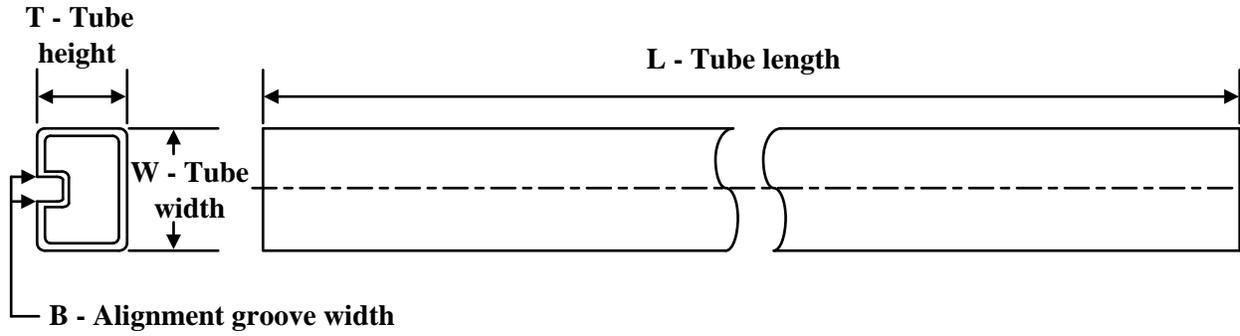
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2014SN-D120TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2014SN-D120TR	SOIC	D	16	2500	353.0	353.0	32.0

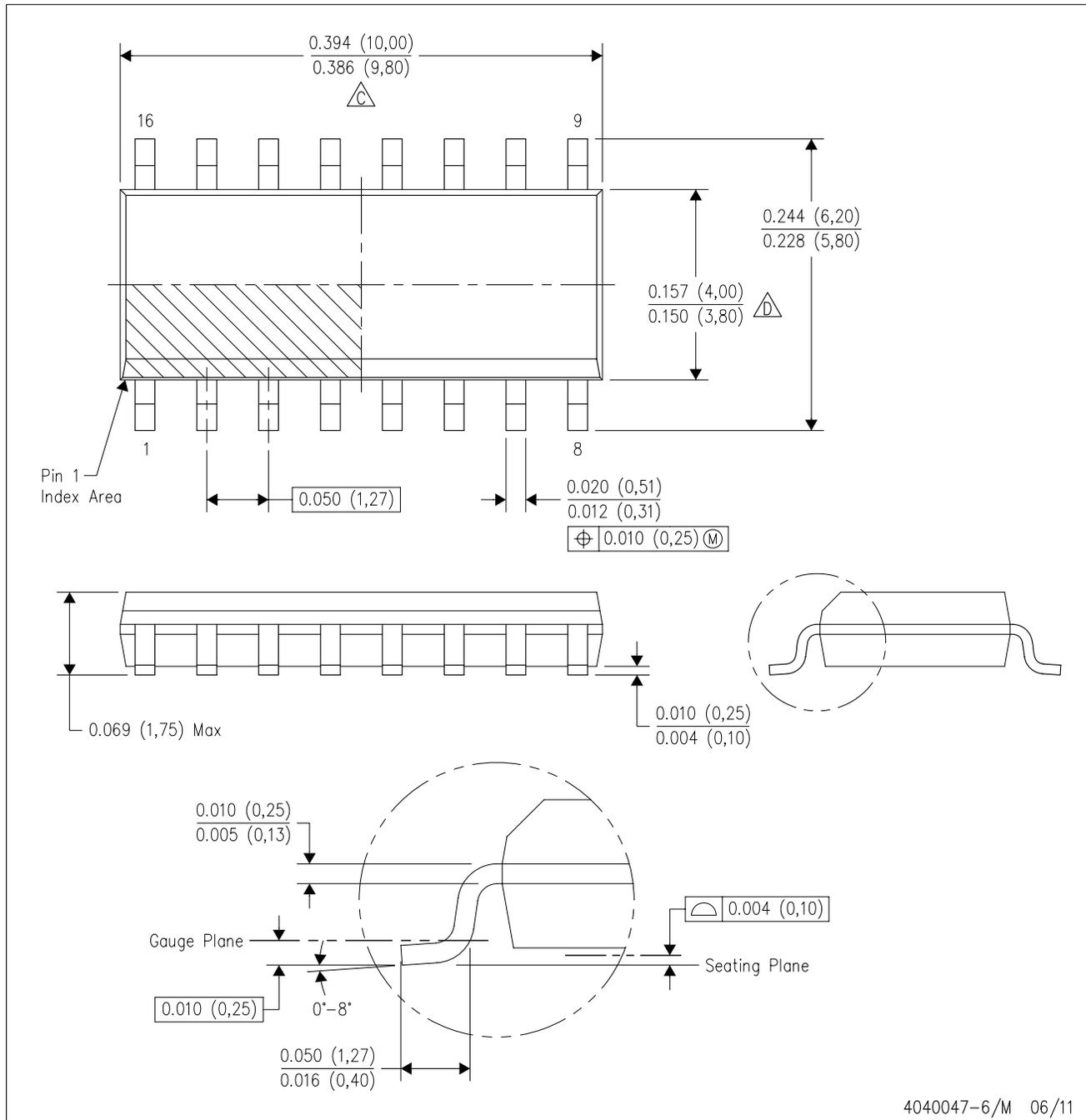
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
BQ2014SN-D120	D	SOIC	16	40	506.6	8	3940	4.32
BQ2014SN-D120.B	D	SOIC	16	40	506.6	8	3940	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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