BQ78709-Q1 2-Series to 7-Series High Accuracy Automotive Battery Monitor and Protector for Li-Ion, Li-Polymer, $LiFePO_4$ (LFP), and LTO Battery Packs and Supercaps

1 Features

- AEC-Q100 Qualified for automotive applications
- Functional Safety Compliant
  - Systematic Capability up to ASIL B / SIL 2
  - Hardware Capability up to ASIL B / SIL 2
- Battery and supercap monitoring capability for 2-series to 7-series cells
- Integrated low-side drivers for NFET protection with optional autonomous recovery
- Extensive protection suite including voltage, temperature, current, and internal diagnostics
- 16-bit delta-sigma voltage ADC
  - High accuracy cell voltage measurement of 1mV (typical)
- Dedicated 16- or 24-bit delta-sigma coulomb counter ADC
- – High-accuracy current measurement with low input offset error
  - Wide-range current applications (±200mV measurement range across sense resistor)
  - 48bit accumulated charge integrator with timer
- Host-controlled cell balancing
- Multiple power modes (typical battery pack operating range conditions)
  - NORMAL mode (with Coulomb counting): 32µA to 175µA
  - SLEEP mode (with protections active): 6µA
  - DEEPSLEEP mode: 2.7µA
  - SHUTDOWN mode: <1µA
- Supply voltage from 3V to 38.5V
- High-voltage tolerance of 45V on cell connect and select additional pins
- Support for temperature sensing using an internal sensor and an external thermistor
- Integrated one-time-programmable (OTP) memory for device settings, programmed by TI
- 400kHz I^2C serial communications with optional CRC support
- Programmable LDO for external system usage
- 20-pin QFN (RGR) package

2 Applications

- Door handle supercap module
- Automotive 12V auxiliary battery
- Automotive backup battery

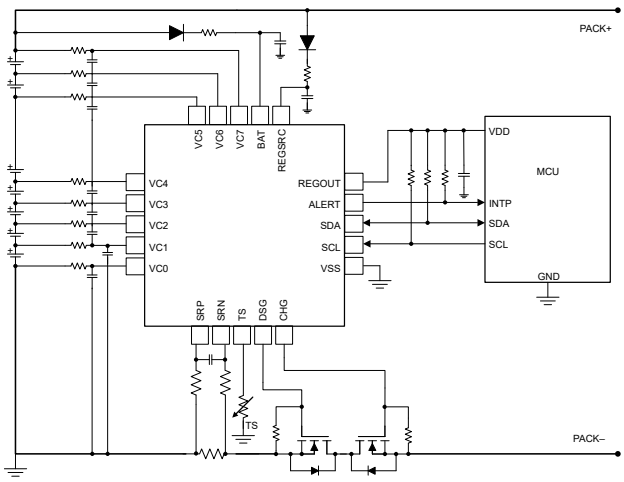
3 Description

The Texas Instruments BQ78709-Q1 provides a highly integrated, high-accuracy battery monitor and protector for 2-series to 7-series Li-ion, Li-polymer, $LiFePO_4$ (LFP), and LTO battery packs and supercaps. The device includes a high-accuracy monitoring system with a dedicated coulomb counter and accumulated charge integration, a highly configurable protection subsystem, and support for host-controlled cell balancing. Integration includes low-side protection NFET drivers, a programmable LDO for external system use, and an I^2C host communication interface supporting up to 400kHz operation with optional CRC. Continuous Coulomb counting is available in multiple power modes ranging down to 32µA. The BQ78709-Q1 operates over a supply voltage from 3V to 38.5V and is available in a 20-pin QFN package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)
BQ78709-Q1	RGR (20-pin)	3.5mm × 3.5mm × 0.9mm, 0.5mm pitch

(1) For more information, see the *Mechanical, Packaging, and Orderable information* sections.



Simplified Schematic

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4 Device Comparison Table

BQ78709-Q1 DEVICE FAMILY				
PART NUMBER	PACKAGE	SETTINGS PROGRAMMABLE	CELL COUNT SUPPORTED	REGOUT STATUS
BQ78709-Q1	QFN	Y	2 to 7	Enabled, 3.3V

5 Pin Configuration and Functions

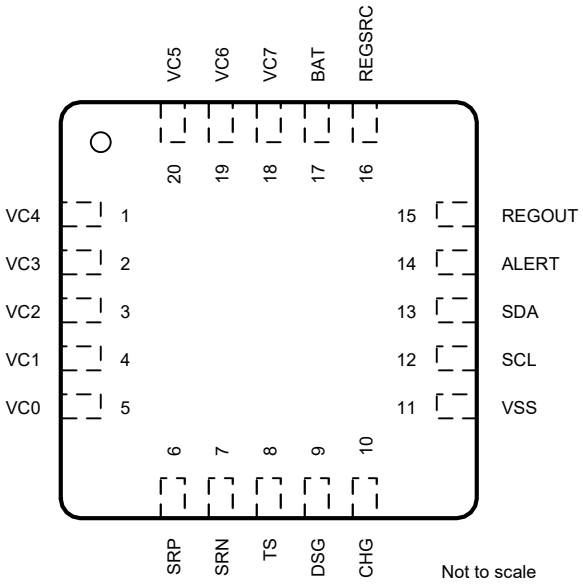


Figure 5-1. BQ78709-Q1 Pinout

Table 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	VC4	I	IA	Sense voltage input pin for the fourth cell from the bottom of the stack, balance current input for the fourth cell from the bottom of the stack, and return balance current for the fifth cell from the bottom of the stack
2	VC3	I	IA	Sense voltage input pin for third cell from the bottom of the stack, balance current input for third cell from the bottom of the stack, and return balance current for the fourth cell from the bottom of the stack
3	VC2	I	IA	Sense voltage input pin for second cell from the bottom of the stack, balance current input for second cell from the bottom of the stack, and return balance current for third cell from the bottom of the stack
4	VC1	I	IA	Sense voltage input pin for first cell from the bottom of the stack, balance current input for first cell from the bottom of the stack, and return balance current for second cell from the bottom of the stack
5	VC0	I	IA	Sense voltage input pin for negative terminal of the first cell from the bottom of the stack, and return balance current for first cell from the bottom of the stack
6	SRP	I	IA	Analog input pin connected to the internal Coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRP is the top of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
7	SRN	I	IA	Analog input pin connected to the internal Coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
8	TS	I/O	I/OA	Thermistor or general-purpose ADC input and functions as a wakeup from SHUTDOWN,
9	DSG	O	OA	NMOS Discharge FET drive output pin
10	CHG	O	OA	NMOS Charge FET drive output pin
11	VSS	—	P	Device ground
12	SCL	I/O	I/OD	I^2C serial communication bus clock
13	SDA	I/O	I/OD	I^2C serial communication bus data
14	ALERT	O	OD	Digital interrupt output pin
15	REGOUT	O	OA	LDO output, which can be programmed for 1.8V, 2.5V, 3.0V, 3.3V, or 5.0V.
16	REGSRC	I	IA	Input pin for REGOUT LDO, also functions as supply for the CHG and DSG FET drivers.
17	BAT	I	P	Primary power supply input pin
18	VC7	I	IA	Sense voltage input pin for the seventh cell from the bottom of the stack, balance current input for the seventh cell from the bottom of the stack, and top-of-stack measurement point
19	VC6	I	IA	Sense voltage input pin for the sixth cell from the bottom of the stack, balance current input for the sixth cell from the bottom of the stack, and return balance current for the seventh cell from the bottom of the stack
20	VC5	I	IA	Sense voltage input pin for the fifth cell from the bottom of the stack, balance current input for the fifth cell from the bottom of the stack, and return balance current for the sixth cell from the bottom of the stack

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

DESCRIPTION	PINS	MIN	MAX	UNIT
Supply voltage range, $V_{IN(DC)}$ (2)	BAT, REGSRC	VSS–0.3	VSS+40	V
Short duration input voltage range, $V_{IN(short)}$ (2)	VC1 - VC7, BAT, REGSRC, CHG		VSS+45	V
DC input voltage range, $V_{IN(DC)}$	ALERT, SCL, SDA	VSS–0.3	VSS+6	V
DC input voltage range, $V_{IN(DC)}$	TS	VSS–0.3	2.1	V
DC input voltage range, $V_{IN(DC)}$ (2)	SRP, SRN	VSS–0.3	2.1	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC7	Maximum of VSS–0.3 and VC6–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC6	Maximum of VSS–0.3 and VC5–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC5	Maximum of VSS–0.3 and VC4–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC4	Maximum of VSS–0.3 and VC3–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC3	Maximum of VSS–0.3 and VC2–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC2	Maximum of VSS–0.3 and VC1–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$ (2)	VC1	Maximum of VSS–0.3 and VC0–0.3	VSS+40	V
DC input voltage range, $V_{IN(DC)}$	VC0	VSS–0.3	VSS+6	V
DC input voltage range, $V_{IN(DC)}$ (2)	CHG	VSS–30	VSS+40	V
Output voltage range, V_O	DSG	VSS–0.3	VSS+20	V
Output voltage range, V_O	REGOUT	VSS–0.3	VSS+6	V
Maximum cell balancing current, each cell	VC0 – VC7		50	mA
Junction temperature, T_J		–65	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Stresses applied above $V_{IN(DC)}$ and below $V_{IN(SHORT)}$ must be limited to less than 100 hours over the lifetime of the device. These stresses may occur during brief transient events but DC voltages in this range should not be applied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	Supply voltage	Voltage on BAT pin (normal operation)	3		38.5	V
$V_{BAT(UVLO)}$	Under voltage lockout level	Falling voltage on BAT causing device reset		2.5		V
$V_{WAKEONTS}$	Wake on TS voltage	Voltage on BAT pin in valid range	0.65		1.2	V
$V_{WAKEONVC0}$	Wake on VC0 voltage	Voltage on BAT pin in valid range	0.65		1.2	V
V_{IN}	Input voltage range	ALERT, SCL, SDA	0		5.5	V
V_{IN}	Input voltage range (with ADC measurements)	TS	–0.2		1.8	V
V_{IN}	Input voltage range	SRP, SRN, SRP-SRN (while measuring current)	–0.2		0.2	V
V_{IN}	Input voltage range	SRP, SRN (without measuring current)	–0.2		1.8	V
V_{IN}	Input voltage range(3)	$V_{VC(0)}$	–0.2		3.0	V
V_{IN}	Input voltage range	$V_{VC(x)}$, 1 ≤ x ≤ 4	maximum of $V_{VC(x–1)}$ – 0.2 or VSS – 0.2		minimum of $V_{VC(x–1)}$+5.5 or VSS + 38.5	V
V_{IN}	Input voltage range	$V_{VC(x)}$, x ≥ 5	maximum of $V_{VC(x–1)}$ – 0.2 or VSS + 2.0		minimum of $V_{VC(x–1)}$ + 5.5 or VSS + 38.5	V
V_O	Output voltage range	CHG	–25		38.5	V
V_O	Output voltage range	DSG	–0.2		14	V
I_{CB}	Cell balancing current (internal, per cell)(3)		0		50	mA
R_C	External cell input resistance(2) (3)		10		1000	Ω
C_C	External cell input capacitance(2) (3)		0.1		10	µF
R_f	External supply filter resistance (BAT pin)(3)		50		1000	Ω
C_f	External supply filter capacitance (BAT pin)(3)		1		40	µF
R_{filt}	Sense resistor filter resistance(3)			100	200	Ω
C_{REGSRC}	REGSRC capacitance(3)		1			µF
R_{TS}	External thermistor nominal resistance (103-AT) at 25°C			10		kΩ

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{OPR}	Junction temperature during operation(1)		–40		125	°C

(1) Power dissipated within device must be limited to ensure junction temperature remains within specification during operation.
(2) External cell input resistance times external input capacitance must be limited to 200µs or below.
(3) Specified by design.

6.4 Thermal Information BQ78709-Q1

THERMAL METRIC(1)		BQ78709-Q1 RGR (QFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	8.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Supply Current

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{NORMAL}	Normal Mode	Regular measurements and protections active, REGOUT = 3.3V with no load, CHG = ON, DSG = ON, **Settings:Configuration:Power Config[IADCSPEED]** = 0x0, **Settings:Configuration:Power Config[CVADCSPEED]** = 0x0, no communication		146		µA
I_{SLEEP}	SLEEP Mode	Periodic protections and monitoring, no pack current, REGOUT = OFF, CHG = OFF, DSG = ON, no communication, **Power:Sleep:Voltage Time** = 5s		6.1		µA
$I_{DEEPSLEEP}$	DEEPSLEEP Mode	No monitoring or protections, REGOUT = 3.3V with no load, LFO = OFF, no communication		2.8		µA
$I_{SHUTDOWN}$	SHUTDOWN Mode	All blocks powered down, no monitoring or protections, no communication		1	2	µA

6.6 Digital I/O

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input	SCL, SDA	1.23		5.5	V
V_{IL}	Low-level input	SCL, SDA			0.53	V
V_{OL}	Output voltage low	ALERT, SCL, SDA, $V_{BAT} \geq$ 3V, I_{OL} = 5mA, 10pF load			0.4	V
C_{IN}	Input capacitance(1)	ALERT, SCL, SDA		2		pF

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LKG}	Input leakage current	ALERT, SCL, SDA, device in SHUTDOWN mode			1	µA

(1) Specified by design

6.7 REGOUT LDO

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REGOUT\_1.8\_LOW}$	Regulator voltage (nominal 1.8V setting)	V_{BAT}, V_{REGSRC} = 3.0V, I_{REGOUT} = 10mA	1.62	1.8	1.92	V
$V_{REGOUT\_1.8}$	Regulator voltage (nominal 1.8V setting) (1)	V_{BAT} ≥ 3.0V, V_{REGSRC} ≥ 3.8V, I_{REGOUT} = 0mA to 20mA	1.62	1.8	1.92	V
$V_{REGOUT\_2.5}$	Regulator voltage (nominal 2.5V setting) (1)	V_{BAT} ≥ 3.0V, V_{REGSRC} ≥ 3.8V, I_{REGOUT} = 0mA to 20mA	2.25	2.5	2.75	V
$V_{REGOUT\_3.0}$	Regulator voltage (nominal 3.0V setting) (1)	V_{BAT} ≥ 3.0V, V_{REGSRC} ≥ 3.8V, I_{REGOUT} = 0mA to 20mA	2.7	3.0	3.3	V
$V_{REGOUT\_3.3}$	Regulator voltage (nominal 3.3V setting) (1)	V_{BAT} ≥ 3.0V, V_{REGSRC} ≥ 4.2V, I_{REGOUT} = 0mA to 20mA	3	3.3	3.6	V
$V_{REGOUT\_5.0}$	Regulator voltage (nominal 5.0V setting) (1)	V_{BAT} ≥ 3.0V, V_{REGSRC} ≥ 5.5V, I_{REGOUT} = 0mA to 20mA	4.5	5.0	5.5	V
$\Delta V_{O(TEMP)}$	Regulator output over temperature	ΔV_{REGOUT} vs (V_{REGOUT} at 25°C, I_{REGOUT} = 20mA, V_{BAT} = 3.0V, V_{REGSRC} = 4.2V, V_{REGOUT} set to nominal 3.3V setting)		±0.015		% / °C
$\Delta V_{O(LINE)}$	Line regulation(1)	ΔV_{REGOUT} vs (V_{REGOUT} at 25°C, V_{BAT} = 3.0V, V_{REGSRC} = 4.2V, I_{REGOUT} = 5mA), as V_{REGSRC} varies from 4.2V to 38.5V, V_{REGOUT} set to nominal 3.3V setting	–1		1	%
I_{SC}	Regulator short-circuit current limit	V_{REGOUT} = 0V	23		50	mA
C_{EXT}	External capacitor REGOUT to VSS(2)		1			µF

(1) Specified by a combination of characterization and production test.
(2) Specified by design

6.8 Voltage References

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE 1						
$V_{(REF1)}$	Internal reference voltage (1)	T_A = 25°C	1.1955	1.1962	1.1969	V
$V_{(REF1DRIFT)}$	Internal reference voltage drift (1)	T_A = -40°C to 125°C	-31		31	PPM/°C
VOLTAGE REFERENCE 2						
$V_{(REF2)}$	Internal reference voltage (2)	T_A = 25°C	1.226	1.227	1.229	V
$V_{(REF2DRIFT)}$	Internal reference voltage drift(2)	T_A = -40°C to 125°C	-51		51	PPM/°C

(1) $V_{(REF1)}$ is used for the ADC reference. Its effective value is determined through indirect measurement using the ADC.
(2) $V_{(REF2)}$ is used for the Coulomb counter, LDOs, and comparator protection subsystem

6.9 Coulomb Counter

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(CC\_IN)}$	Input voltage range for measurements(3)	V_{SRP} - V_{SRN}	–0.2		0.2	V
$V_{(CC\_IN)}$	Input voltage range for measurements(3)	V_{SRP}, V_{SRN}	–0.2		0.2	V
$B_{(CM\_INL)}$	Integral nonlinearity(2)	16-bit, best fit straight line over input voltage range of -200mV to 200mV, using *CC1 Current()* command data with ***CC1 Gain*** = 32, such that 1-LSB ≈ 7.52µV, at 25°C			±4.3	LSB(1)
$B_{(CM\_INL)}$	Integral nonlinearity(2)	16-bit, best fit straight line over SRP-SRN input voltage range of -200mV to 100mV, using *CC1 Current()* command data with ***CC1 Gain*** = 32, such that 1-LSB ≈ 7.52µV, at 25°C			±1.2	LSB(1)
$V_{(CM\_OFF)}$	Offset error	16-bit, uncalibrated, using *Current()* command data with ***Curr Gain*** = 32, such that 1-LSB ≈ 7.52µV	-5		5	µV
$V_{(CM\_OFF\_DRIFT)}$	Offset error drift(2)	16-bit, uncalibrated, using *Current()* command data with ***Curr Gain*** = 32, such that 1-LSB ≈ 7.52µV		0.01		µV/°C
$B_{(CM\_GAIN)}$	Gain(2)	Using 16-bit data from *Current()* command, with ***Curr Gain*** = 32, V_{SRP} - V_{SRN} = ±0.15V	132344	132832	133911	LSB/V(1)
$B_{(CM\_GAIN)}$	Gain drift (2)	Using 16-bit data from *Current()* command, with ***Curr Gain*** = 32, V_{SRP} - V_{SRN} = ±0.15V	-12		15	LSB/V/°C(1)
$R_{(CM\_IN)}$	Effective input resistance(3) (4)		2			MΩ

(1) 1 LSB = V_{REF2} / (5 × 2^{N-1}) ≈ 1.227 / (5 × 2^{15}) = 7.49µV
(2) Specified by characterization
(3) Specified by design.
(4) Average effective differential input resistance with device operating in NORMAL mode, 0.1V differential input applied.

6.10 Coulomb Counter Digital Filter

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CC1 Charge Integration Digital Filter						
$t_{(CC1\_CONV)}$	Conversion-time	Single conversion		250		ms
$B_{(CC1\_RSL)}$	Effective resolution(1) (2)	Single conversion, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, at 25°C.	15.5			bits
$B_{(CC1\_RSL)}$	Effective resolution in low power mode(1) (2)	Single conversion, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, at 25°C.		15.7		bits
CC2 Current Measurement Digital Filter						
$t_{(CM\_CONV)}$	Conversion-time in slow mode	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x0		2.93		ms
$t_{(CM\_CONV\_MEDSLOW)}$	Conversion-time in medium slow mode	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x1		1.46		ms

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CM\_CONV\_MEDFAST)}$	Conversion-time in medium fast mode	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x2		732		µs
$t_{(CM\_CONV\_FAST)}$	Conversion-time in fast mode	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x3		366		µs
$B_{(CM\_RES)}$	Effective resolution in slow mode(1) (2)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x0 at 25°C.	13.4			bits
$B_{(CM\_RES\_MEDSLOW)}$	Effective resolution in medium slow mode(1)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x1 at 25°C.		14.4		bits
$B_{(CM\_RES\_MEDFAST)}$	Effective resolution in medium fast mode(1)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x2 at 25°C.		13.0		bits
$B_{(CM\_RES\_FAST)}$	Effective resolution in fast mode(1)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x3 at 25°C.		10.6		bits
$B_{(CM\_LP\_RES)}$	Effective resolution in slow mode and low power mode(1) (2)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x0, **Settings:Configuration:DA Config[CCMODE]** = 0x2 at 25°C.		15.0		bits
$B_{(CM\_LP\_RES\_MEDSLOW)}$	Effective resolution in medium slow mode and low power mode(1)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x1, **Settings:Configuration:DA Config[CCMODE]** = 0x2 at 25°C.		14.3		bits
$B_{(CM\_LP\_RES\_MEDFAST)}$	Effective resolution in medium fast mode and low power mode(1)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x2, **Settings:Configuration:DA Config[CCMODE]** = 0x2 at 25°C.		13.0		bits
$B_{(CM\_LP\_RES\_FAST)}$	Effective resolution in fast mode and low power mode(1)	Single conversion, in NORMAL mode, DC inputs from -200mV to +200mV across V_{SRP} - V_{SRN}, **Settings:Configuration:Power Config[IADCSPEED]** = 0x3, **Settings:Configuration:DA Config[CCMODE]** = 0x2 at 25°C.		10.5		bits

(1) Effective resolution is defined as the resolution such that the data exhibits 1-sigma variation within ±1-LSB.

(2) Specified by characterization.

6.11 Current Wake Detector

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 1, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	8	325	615	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 2, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	513	844	1140	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 3, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	1018	1367	1668	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 4, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	1285	1879	2423	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 5, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	1850	2389	2907	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 6, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	2375	2916	3425	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 7, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	2833	3417	4005	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 8, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	3184	3941	4698	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 9, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	3650	4470	5233	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 10, positive threshold (charging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	4136	4990	5799	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 1, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-739	-600	-461	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 2, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-1236	-1101	-949	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 3, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-1759	-1586	-1413	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 4, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-2273	-2074	-1871	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 5, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-2786	-2570	-2349	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 6, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-3324	-3067	-2793	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 7, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-3841	-3557	-3269	µV

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 8, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-4364	-4049	-3738	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 9, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-4901	-4543	-4192	µV
V_{WAKE_THR}	Wakeup voltage threshold (V_{SRP} – V_{SRN}), setting = 10, negative threshold (discharging current) (1)	T_A = -40°C to 125°C. Measured using averaged data to remove effects of noise.	-5419	-5038	-4643	µV
t_{WAKE}	Measurement interval			2.44		ms

(1) Specified by a combination of characterization and production test

6.12 Analog-to-Digital Converter

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(ADC\_IN\_CELLS)}$	Input voltage range (differential cell input mode) (2) (4)	Internal reference (Vref = V_{REF1})	–0.2		5.5	V
$V_{(ADC\_IN)}$	Input voltage range (ADCIN measurement mode)(2) (6)	Internal reference (Vref = V_{REF1}, **Settings:Configuration:DA Config[TSMODE]** = 1), applicable to ADCIN measurements using the TS pin	–0.2		1.8	V
$V_{(ADC\_IN\_TS)}$	Input voltage range (external thermistor measurement mode) (2) (5)	Regulator reference (Vref = V_{REG18}, **Settings:Configuration:DA Config[TSMODE]** = 0), applicable to external thermistor measurement using the TS pin	–0.2		1.8	V
$V_{(ADC\_IN\_DIV)}$	Input voltage range (divider measurement mode)(2) (7)	Internal reference (Vref = V_{REF1}), applicable to divider measurements using the VC7 pin relative to VSS.	2.0		38.5	V
$B_{(ADC\_OFF\_CELL)}$	Differential cell offset error	16-bit, uncalibrated, with VC7 - VC6 = 0V, VC6 = 24V, using raw ADC codes		-0.5		LSB (4)
$B_{(ADC\_OFF\_DRIFT\_CELL)}$	Differential cell offset error drift(3)	16-bit, uncalibrated, with VC7 - VC6 = 0V, VC6 = 4V, using raw ADC codes, over -40°C to +125°C	-0.27		0.24	LSB/°C (4)
$B_{(ADC\_OFF)}$	TS offset error (1)	16-bit, uncalibrated, using Vref = V_{REG18}	-33	4.2	44	LSB(6)
$B_{(ADC\_OFF\_DIV)}$	Divider offset error	16-bit, uncalibrated, using divider mode on VC7		-3.7		LSB(7)
$G_{(ADC\_TS\_REG18)}$	Gain of ADC TS pin measurement using Vref = V_{REG18} (9)	Reported digital code = $G_{(ADC\_TS\_REG18)}$ × V_{TS} / V_{REG18}. 16-bit, uncalibrated, using TS pin, V_{TS} = 1.5V.	19172	19416	19684	N/A (5)
$G_{(ADC\_TS\_ADCIN)}$	Gain of ADC TS pin measurement using Vref = V_{REF1} (9)	Reported digital code = $G_{(ADC\_TS\_ADCIN)}$ × V_{TS}. 16-bit, uncalibrated, using TS pin, V_{TS} = 1.5V.	15732	16020	16272	LSB/V (6)
$G_{(ADC\_CELL\_RAW)}$	Raw gain of ADC cell voltage measurement (9)	Gain measured 16-bit, using 2.0V and 4.0V differential cell input mode on VC7 - VC6, uncalibrated, using raw ADC codes.	5465	5477	5490	LSB/V (4)
$R_{(ADC\_IN\_CELL)}$	Effective input resistance(8)	Differential cell input mode on VC7 - VC6		4		MΩ
$R_{(ADC\_IN\_TOS)}$	Effective input resistance	Divider measurement on VC7 pin (only active while the pin is being measured)		600		kΩ

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(LEAKAGE)}$	Pin leakage current (3)	Input current per pin into VC1 ~ VC7, BAT, REGSRC, with no conversions, stack biased with 5V / cell, V_{BAT} = 30V, device in SHUTDOWN mode.			2	µA
$B_{(ADC\_RES\_SLOW)}$	Effective resolution with slow speed setting(1)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[SSADCSPEED]** = 0x0, using TS input in ADCIN mode.		15		bits
$B_{(ADC\_RES\_MEDSLOW)}$	Effective resolution with medium slow speed setting(1)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[SSADCSPEED]** = 0x1, using TS input in ADCIN mode.		14		bits
$B_{(ADC\_RES\_MEDFAST)}$	Effective resolution with medium fast speed setting(1)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[SSADCSPEED]** = 0x2, using TS input in ADCIN mode.		13		bits
$B_{(ADC\_RES\_FAST)}$	Effective resolution with fast speed setting(1)	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[SSADCSPEED]** = 0x3, using TS input in ADCIN mode.		11		bits
$t_{(ADC\_CONV\_SLOW)}$	Conversion-time	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[CVADCSPEED]** and **[SSADCSPEED]** = 0x0		2.93		ms
$t_{(ADC\_CONV\_MEDSLOW)}$	Conversion-time in medium slow mode	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[CVADCSPEED]** and **[SSADCSPEED]** = 0x1		1.46		ms
$t_{(ADC\_CONV\_MEDFAST)}$	Conversion-time in medium fast mode	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[CVADCSPEED]** and **[SSADCSPEED]** = 0x2		732		µs
$t_{(ADC\_CONV\_FAST)}$	Conversion-time in fast mode	Single conversion, in NORMAL mode, **Settings:Configuration:Power Config[CVADCSPEED]** and **[SSADCSPEED]** = 0x3		366		µs
$V_{STACK(ACC)}$	Stack voltage (V_{C7} - V_{VSS}) measurement accuracy (9)	3V ≤ V_{VC7} - V_{VSS} ≤ 38.5V, T_A = 25°C, specified using an input network of 20Ω and 220nF.	–37		28	mV
		3V ≤ V_{VC7} - V_{VSS} ≤ 38.5V, T_A = -20°C to 65°C, specified using an input network of 20Ω and 220nF.	–162		168	mV
		3V ≤ V_{VC7} - V_{VSS} ≤ 38.5V, T_A = -40°C to 125°C, specified using an input network of 20Ω and 220nF.	–380		215	mV

(1) Effective resolution is defined as the resolution such that the data exhibits 1-sigma variation within ±1-LSB.
(2) Specified by design
(3) Specified by characterization
(4) The 16-bit LSB size of the differential cell voltage raw codes measurement is given by 1 LSB = 1V / $G_{(ADC\_CELL\_RAW)}$ approximately 1V / 5479 LSB/V = 182.5µV
(5) Assuming a nominal value of V_{REG18} = 1.8V, the 16-bit LSB size of the TS pin voltage measurement in thermistor mode is given by 1 LSB = V_{REG18} / $G_{(ADC\_TS\_REG18)}$ ≈ 1.8V / 19405 = 93µV
(6) The 16-bit LSB size of the TS pin voltage measurement in ADCIN mode is given by 1 LSB = 1V / $G_{(ADC\_TS\_ADCIN)}$ approximately 1V / 16027 = 62µV
(7) The 16-bit LSB size of the divider voltage measurement is given by 1 LSB = 50 × V_{REF1} / 2^{N-1} approximately 50 × 1.1962V / 2^{15} = 1.825mV
(8) Average effective differential input resistance with device operating in NORMAL mode, cell balancing disabled, and a 5V differential voltage applied.

(9) Specified by a combination of characterization and production test

6.13 Cell Voltage Measurement Accuracy

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = –40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCELL(ACC)	Cell voltage measurement accuracy, $V_{VC(x)}$ - $V_{VC(x-1)}$ = 4.5V, 1 ≤ x ≤ 7(1)	T_A = 25°C	-3.6		3.6	mV
		–20°C ≤ T_A ≤ 65°C	-4.6		8.2	mV
		–40°C ≤ T_A ≤ 125°C	-6.2		10.8	mV
VCELL(ACC)	Cell voltage measurement accuracy, 2V < $V_{VC(x)}$ - $V_{VC(x-1)}$ = 5V, 1 ≤ x ≤ 7(1)	T_A = 25°C	-3.9		4.3	mV
		–20°C ≤ T_A ≤ 65°C	-4.8		8.2	mV
		–40°C ≤ T_A ≤ 125°C	-7.6		11.4	mV

(1) Specified by a combination of characterization and production test, using 7-series stack, input network series resistance = 20Ω, differential capacitance = 220nF, cell balancing inactive

6.14 Cell Balancing

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(CB)}$	Internal cell balancing resistance(1)	$R_{DS(ON)}$ for internal FET switch at $V_{VC(n)}$ - $V_{VC(n-1)}$ = 1.5V, 1 ≤ n ≤ 7	53	93	200	Ω

(1) Cell balancing must be controlled to limit the current based on the absolute maximum allowed current, and to avoid exceeding the recommended device operating temperature. This can be accomplished by appropriate sizing of the offchip cell input resistors and limiting the number of cells that can be balanced simultaneously.

6.15 Internal Temperature Sensor

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Internal temperature measurement error (1)		-7.8		9.0	°C
$V_{(TEMP)}$	Internal temperature sensor voltage drift	ΔV_{BE} measurement, using raw LSBs		6.76		LSB/°C

(1) Specified by characterization

6.16 Thermistor Measurement

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(TS\_PU)}$	Internal pullup resistance at 25°C(1)		19.75	20	20.25	kΩ
$R_{(TS\_PU\_DRIFT)}$	Internal pullup resistance change over temperature (1) (2)	Change over -20°C/+65°C vs value at 25°C	–23		28	Ω
$R_{(TS\_PU\_DRIFT)}$	Internal pullup resistance change over temperature (1) (2)	Change over -40°C/+125°C vs value at 25°C	–28		38	Ω

(1) The internal pullup resistance includes only the resistance between the REG18 internal LDO and the point where the voltage is sensed by the ADC.

(2) Specified by characterization

6.17 Hardware Overtemperature Detector

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OTSD)}$	Hardware overtemperature detector threshold(1)		118		132	°C

(1) Specified by design

6.18 Internal Oscillator

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-frequency Oscillator						
f_{LFO}	Operating frequency	Full speed setting, at 25°C	260.0	262.626	265.0	kHz
		Low speed setting, at 25°C	32.3	32.815	33.4	kHz
$f_{LFOF(ERR)}$	Frequency drift, full speed mode(1)	Change in frequency vs value at 25°C, T_A = –20°C to +65°C	–1.3		1	%
		Change in frequency vs value at 25°C, T_A = –40°C to +125°C.	–1.7		1.7	%
$f_{LFOS(ERR)}$	Frequency drift, low speed mode(1)	Change in frequency vs value at 25°C, T_A = –20°C to +65°C.	-1.0		1.0	%
$f_{LFOS(ERR)}$	Frequency drift, low speed mode(1)	Change in frequency vs value at 25°C, T_A = –40°C to +125°C.	-1.4		1.6	%
$f_{LFO(FAIL)}$	Failure detection frequency	Refers to the LFO frequency if in low speed mode, or the LFO frequency divided by 8 if in full speed mode. Detects oscillator failure if the frequency falls below this level.	11	15	20	kHz

(1) Specified by characterization

6.19 Charge and Discharge FET Drivers

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(FETON\_DSG)}$	DSG driver enabled	V_{REGSRC} ≥ 12V, C_L= 20nF	10.5	11.2	13	V
$V_{(FETON\_CHG)}$	CHG driver enabled	V_{REGSRC} ≥ 12V, C_L= 20nF	10	10.8	12	V
$V_{(FETON\_LOBAT\_DSG)}$	DSG driver enabled	V_{REGSRC} < 12V, C_L = 20nF	V_{REGSRC} – 1		V_{REGSRC}	V
$V_{(FETON\_LOBAT\_CHG)}$	CHG driver enabled	V_{REGSRC} < 12V, C_L = 20nF	V_{REGSRC} – 1.75		V_{REGSRC}	V
$t_{(CHG\_ON)}$	CHG FET driver rise time	CHG C_L = 20nF, R_{GATE} = 100Ω, V_{REGSRC} = 12V, 0.5V to 5V		50	85	µs
$t_{(DSG\_ON)}$	DSG FET driver rise time	DSG C_L = 20nF, R_{GATE} = 100Ω, V_{REGSRC} = 12V, 0.5V to 5V		35	55	µs
$t_{(CHG\_OFF)}$	CHG FET driver fall time	CHG C_L = 20nF, R_{GATE} = 100Ω, V_{REGSRC} = 12V, 80% to 20% of $V_{(FETON\_CHG)}$		24	35	µs
$t_{(DSG\_OFF)}$	DSG FET driver fall time	DSG C_L = 20nF, R_{GATE} = 100Ω, V_{REGSRC} = 12V, 80% to 20% of $V_{(FETON\_DSG)}$		2	3	µs
$I_{(CHG\_ON)}$	CHG FET driver output current	CHG enabled and pin held at 8V, V_{REGSRC} = 12V		1		mA

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(DSG\_ON)}$	DSG FET driver output current	DSG enabled and pin held at 8V, V_{REGSRC} = 12V		1.56		mA
$R_{(DSG\_OFF)}$	DSG FET driver off resistance	DSG off and pin held at 100mV		15	30	Ω
$V_{(CHG\_DETECT)}$	CHG detector threshold	CHG pin voltage rising	1.2		1.8	V
$V_{(CHG\_DET\_HYS)}$	CHG detector hysteresis			0.95		V

6.20 Comparator-Based Protection Subsystem

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCD)}$	Short circuit in discharge voltage threshold range	Nominal settings, threshold based on $V_{SRP} - V_{SRN}$		–10, –20, –40, –60, –80, –100, –125, –150, –175, –200, –250, –300, –350, –400, –450, –500		mV
$V_{(SCD\_ACC)}$	Short circuit in discharge voltage threshold detection accuracy (2)	–10mV setting	–43.3		39.8	% of nominal threshold
		–20mV setting	–22.6		19	% of nominal threshold
		–40mV setting	–14.2		9.7	% of nominal threshold
		Settings –60mV	–12.0		7.0	% of nominal threshold
		Settings –80mV	–9.6		5.8	% of nominal threshold
		Settings –100mV to -500mV	–9.1		5.4	% of nominal threshold

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCD\_DLY)}$	Short circuit in discharge detection delay(1)	Fastest setting (with 3mV overdrive)		8		µs
		Fastest setting (with 25mV overdrive)		0.6		µs
		Setting for 15µs (with 3mV overdrive)		20	28	µs
		Setting for 15µs (with 25mV overdrive)			20	µs
		Settings for 31µs (with 25mV overdrive)	14		35	µs
		Settings for 61µs (with 25mV overdrive)	42		66	µs
		Settings for 122µs (with 25mV overdrive)	102		130	µs
		Settings for 244µs (with 25mV overdrive)	218		258	µs
		Settings for 488µs (with 25mV overdrive)	452		510	µs
		Settings for 977µs (with 25mV overdrive)	920		1018	µs
		Settings for 1953µs (with 25mV overdrive)	1860		2034	µs
		Settings for 3906µs (with 25mV overdrive)	3735		4065	µs
		Setting for 7797µs (with 25mV overdrive)	7470		8112	µs
$V_{(OCC)}$	Overcurrent in charge (OCC) voltage threshold range	Nominal settings, threshold based on $V_{SRP} – V_{SRN}$		3mV to 19mV in 2mV steps, 22mV to 124mV in 2mV steps		mV
$V_{(OCC\_ACC)}$	Overcurrent in charge (OCC) voltage threshold accuracy (2)	Settings 3mV to 19mV	–1.45		1.81	mV
$V_{(OCC\_ACC)}$	Overcurrent in charge (OCC) voltage threshold accuracy (2)	Settings 22mV to 80mV	-3.02		2.95	mV
$V_{(OCC\_ACC)}$	Overcurrent in charge (OCC) voltage threshold accuracy (2)	Settings 82mV to 124mV	-4.05		5.26	mV
$V_{(OCD)}$	Overcurrent in discharge (OCD1, OCD2) voltage threshold ranges	Nominal settings, thresholds based on $V_{SRP} – V_{SRN}$		–4mV to –200mV in 2mV steps		mV
$V_{(OCD\_ACC)}$	Overcurrent (OCD1, OCD2) detection voltage threshold accuracy (2)	Settings -4mV	–1.76		1.4	mV
		Settings -6mV to -16mV	–1.45		1.0	mV
		Settings -18mV to -166mV	–3.34		3.27	mV
		Settings -168mV to -200mV	–3.98		4,38	mV

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OC\_DLY)}$	Overcurrent (OCC, OCD1, OCD2) detection delay (independent delay setting for each protection)	Fastest setting		0.46		ms
		Nominal settings, low range		1.22ms to 20.435ms in 0.305ms steps		ms
		Nominal settings, medium low range		22.875ms to 176.595 ms in 2.441ms steps		ms
		Nominal settings, medium high range		181.475 ms to 488.915 ms in 4.883ms steps		ms
		Nominal settings, high range		498.675 ms to 1103.795 ms in 9.766ms steps		ms
$V_{(OC\_DLY)}$	Overcurrent (OCC, OCD1, OCD2) detection delay accuracy(1)	Fastest setting	-0.35		0.35	ms
		Nominal settings, low range	-1.2		0.90	ms
		Nominal settings, medium low range	-7.5		7.2	ms
		Nominal settings, medium high range	-20		20	ms
		Nominal settings, high range	-45		45	ms

(1) Specified by design
(2) Specified by a combination of characterization and production test

6.21 Timing Requirements - I²C Interface, 100kHz Mode

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock operating frequency(1)	SCL duty cycle = 50%			100	kHz
$t_{HD:STA}$	START condition hold time(1)		4.0			µs
t_{LOW}	Low period of the SCL clock(1)		4.7			µs
t_{HIGH}	High period of the SCL clock(1)		4.0			µs
$t_{SU:STA}$	Setup repeated START(1)		4.7			µs
$t_{HD:DAT}$	Data hold time (SDA input)(1)		0			ns
$t_{SU:DAT}$	Data setup time (SDA input)(1)		250			ns
t_r	Clock rise time(1)	10% to 90%			1000	ns
t_f	Clock fall time(1)	90% to 10%			300	ns
$t_{SU:STO}$	Setup time STOP condition(1)		4.0			µs
t_{BUF}	Bus free time STOP to START(1)		4.7			µs
t_{RST}	I²C bus reset(1)	Bus interface is reset if SCL is detected low for this duration	1.9		2.1	s
R_{PULLUP}	Pullup resistor(1)	Pullup voltage rail ≤ 5V	1.1			kΩ

(1) Specified by design

6.22 Timing Requirements - I²C Interface, 400kHz Mode

Typical values stated where T_A = 25°C and V_{BAT} = 25.9V, min/max values stated where T_A = -40°C to 125°C and V_{BAT} = 3V to 38.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock operating frequency(1)	SCL duty cycle = 50%			400	kHz
$t_{HD:STA}$	START condition hold time(1)		0.6			µs
t_{LOW}	Low period of the SCL clock(1)		1.3			µs
t_{HIGH}	High period of the SCL clock(1)		600			ns
$t_{SU:STA}$	Setup repeated START(1)		600			ns
$t_{HD:DAT}$	Data hold time (SDA input)(1)		0			ns
$t_{SU:DAT}$	Data setup time (SDA input)(1)		100			ns
t_r	Clock rise time(1)	10% to 90%			300	ns
t_f	Clock fall time(1)	90% to 10%			300	ns
$t_{SU:STO}$	Setup time STOP condition(1)		0.6			µs
t_{BUF}	Bus free time STOP to START(1)		1.3			µs
t_{RST}	I²C bus reset(1)	Bus interface is reset if SCL is detected low for this duration	1.9		2.1	s
R_{PULLUP}	Pullup resistor(1)	Pullup voltage rail ≤ 5V	1.1			kΩ

(1) Specified by design

6.23 Timing Diagram

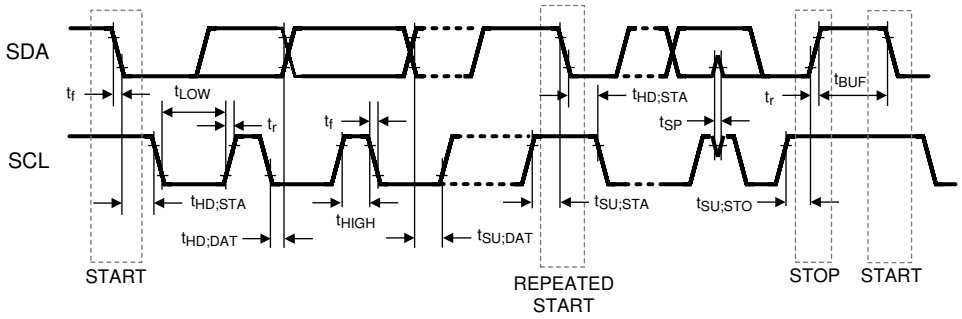


Figure 6-1. I²C Communications Interface Timing

6.24 Typical Characteristics

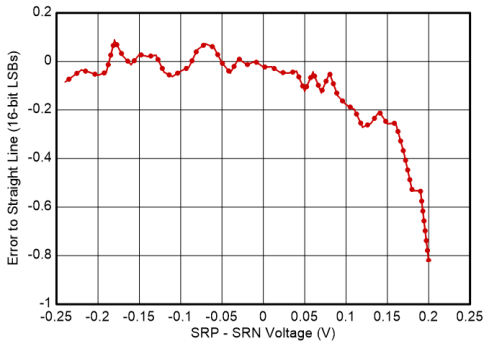


Figure 6-2. Current Linearity Error vs. Sense Resistor Voltage

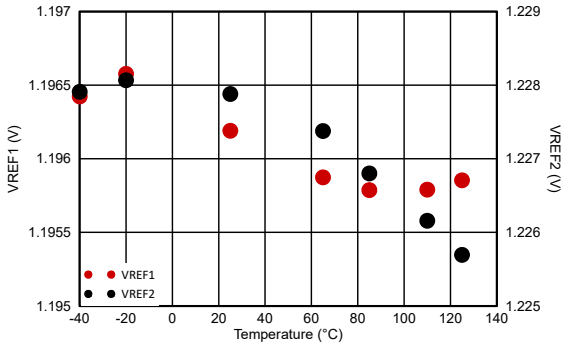


Figure 6-3. Internal Voltage References vs. Temperature (VREF1 and VREF2)

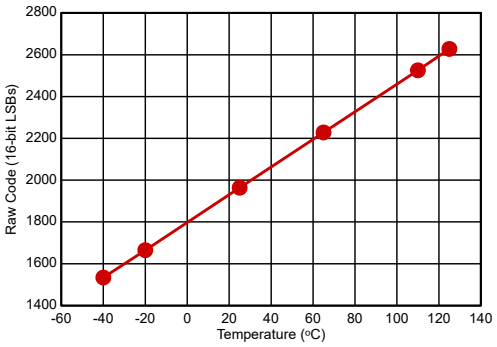


Figure 6-4. Internal Temperature Measurement Raw Codes vs. Temperature

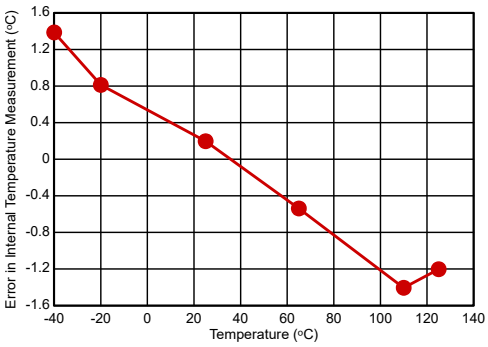


Figure 6-5. Internal Temperature Measurement Error vs. Temperature

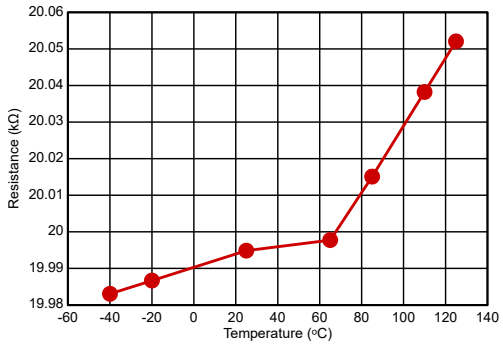
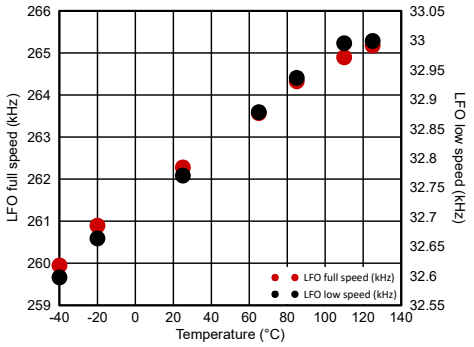


Figure 6-6. Thermistor Pullup Resistance vs. Temperature



LFO measured in full speed mode (262kHz) and low speed mode (32.77kHz)

Figure 6-7. Low Frequency Oscillator (LFO) Accuracy vs. Temperature

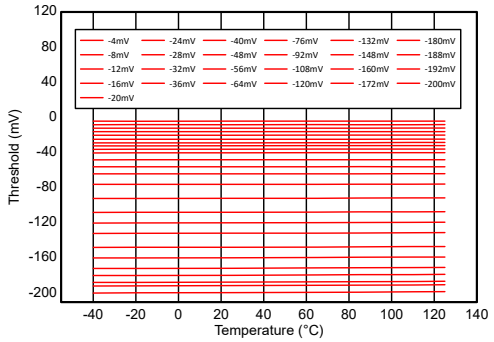


Figure 6-8. Overcurrent in Discharge Protection 1 (OCD1) Threshold vs. Temperature

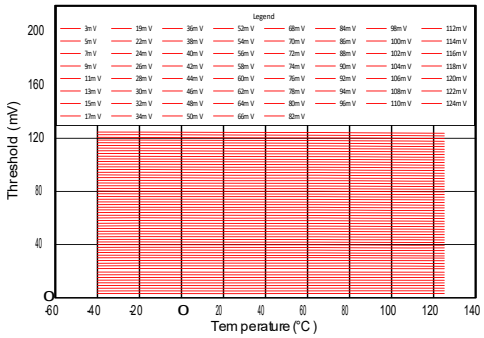


Figure 6-9. Overcurrent in Charge Protection (OCC) Threshold vs. Temperature

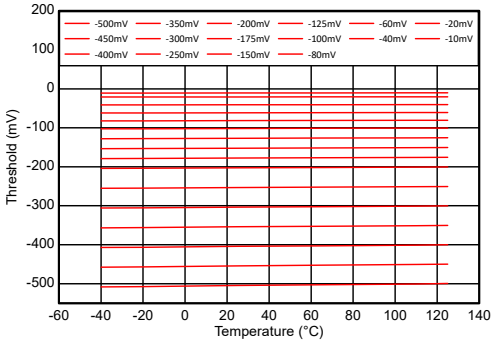
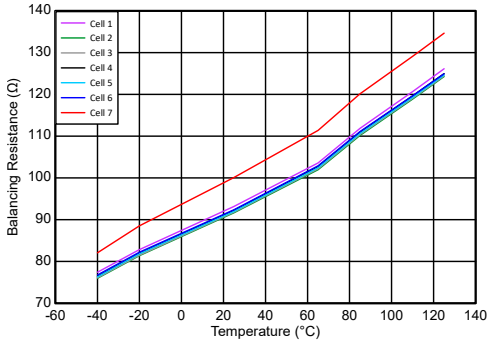


Figure 6-10. Short Circuit in Discharge Protection (SCD) Threshold vs. Temperature



Data is collected with a 1.5V differential input on cell.

Figure 6-11. Cell Balancing Resistance vs. Temperature

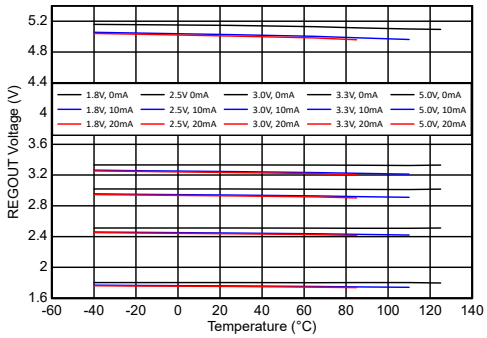


Figure 6-12. REGOUT Voltage vs. Temperature and Load

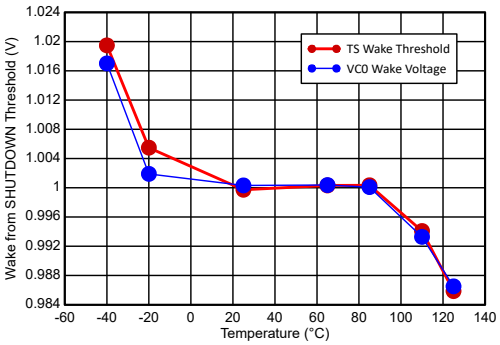
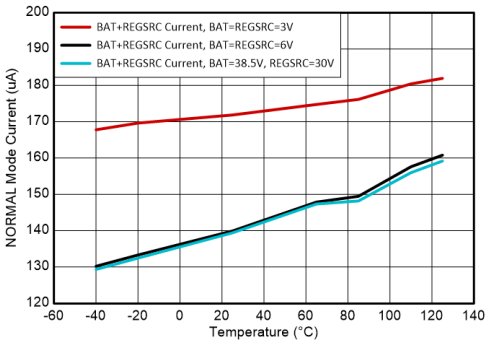
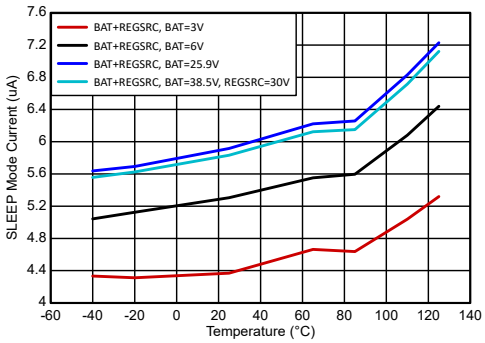


Figure 6-13. TS and VC0 Wake Voltage vs. Temperature



When REGSRC = 3V, REGSRC current increases as the device attempts to raise the REGOUT voltage to its target 3.3V.

Figure 6-14. Supply Current in NORMAL Mode vs. Temperature



No communications, REGOUT disabled

Figure 6-15. Supply Current in SLEEP Mode vs. Temperature

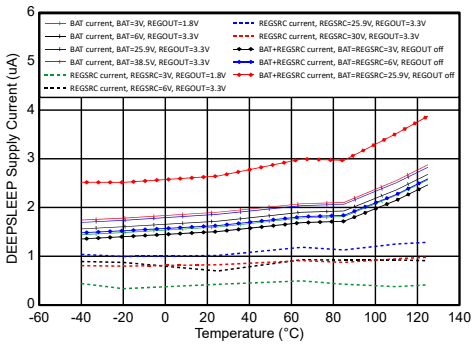


Figure 6-16. Supply Current in DEEPSLEEP Mode vs. Temperature

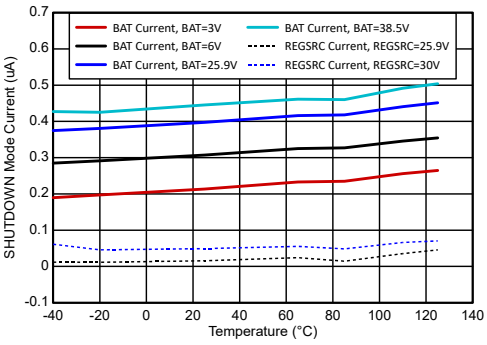


Figure 6-17. Supply Current in SHUTDOWN Mode vs. Temperature

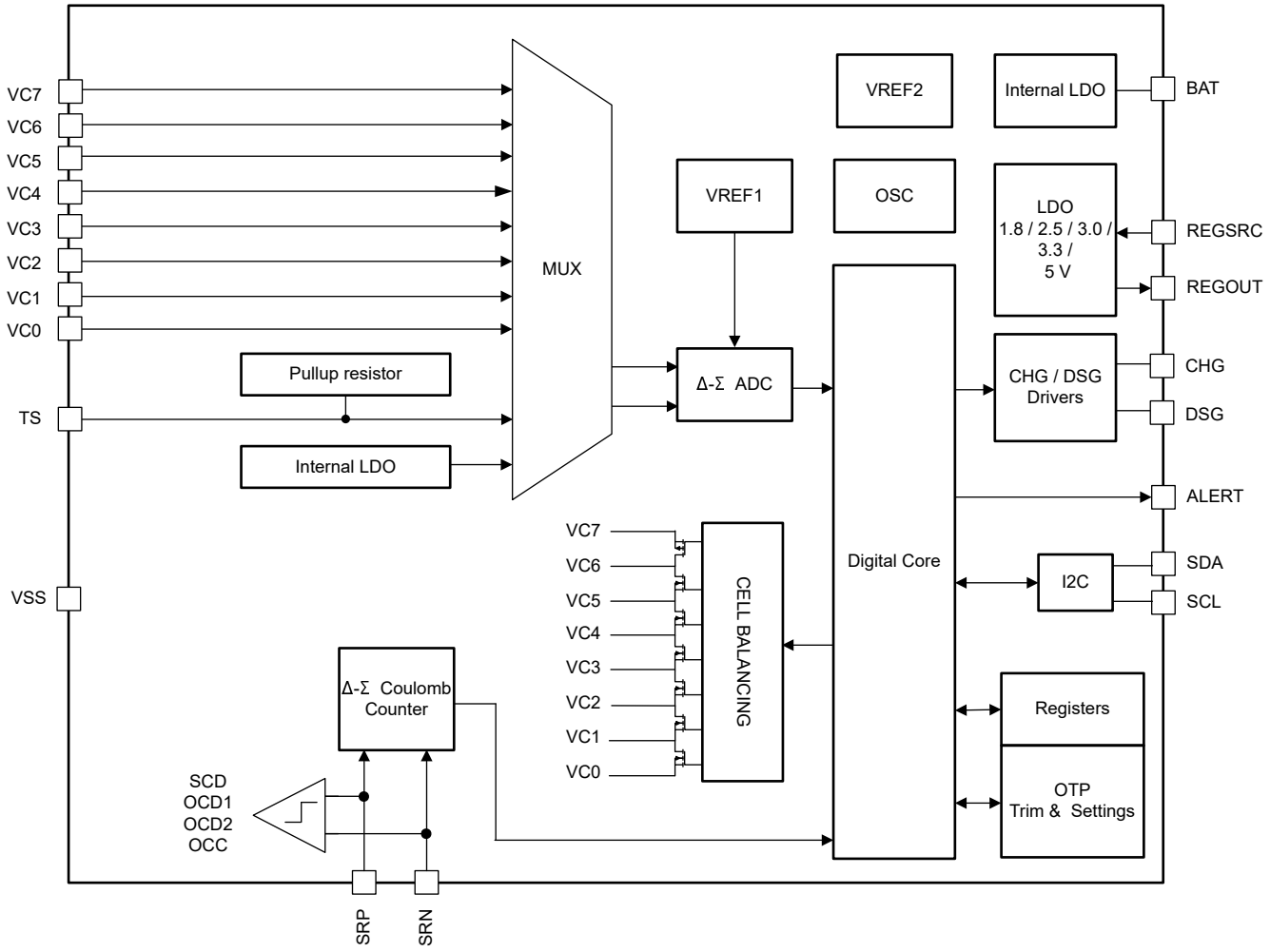
7 Detailed Description

7.1 Overview

The BQ78709-Q1 device is a highly integrated, accurate battery monitor and protector for 2-series to 7-series Li-ion, Li-polymer, $LiFePO_4$ (LFP), and LTO battery packs and supercaps. A high-accuracy voltage, current, and temperature measurement provides data for host-based algorithms and control. A feature-rich and highly configurable protection subsystem provides a wide set of protections, which can be triggered and recovered completely autonomously by the device or under full control of a host processor. Integrated FET drivers drive low-side charge and discharge protection NFETs. A programmable LDO is included for external system use, with voltage programmable to 1.8V, 2.5V, 3.0V, 3.3V, or 5.0V, capable of providing up to 20mA.

The BQ78709-Q1 device includes one-time-programmable (OTP) memory, which TI programs to configure default device operation settings, for systems where a host processor may not be available to configure the device. A 400kHz I^2C communication interface and ALERT interrupt output enable communication with a host processor. The device includes support for one external thermistor, as well as an internal die temperature measurement.

7.2 Functional Block Diagram



7.3 Device Configuration

7.3.1 Commands and Subcommands

The BQ78709-Q1 device includes support for direct commands and subcommands. The direct commands are accessed using a 7-bit command address that is sent from a host through the device serial communications interface and either triggers an action, or provides a data value to be written to the device, or instructs the device to report data back to the host. Subcommands are additional commands that are accessed indirectly using the 7-bit command address space and provide the capability for block data transfers. For more information on the commands and subcommands supported by the device, refer to *BQ76907 Technical Reference Manual*.

7.3.2 Configuration Using OTP or Registers

The BQ78709-Q1 device includes registers, with values stored in the RAM, and can be loaded automatically from one-time programmable (OTP) memory. At initial power-up, the device loads OTP settings into registers, which are used by the device during operation. The OTP settings are programmed into the device by TI during manufacturing. Register values are preserved while the device is in NORMAL, SLEEP, or DEEPSLEEP modes. If the device enters SHUTDOWN mode, all register memory is cleared, and the device reloads values from OTP when powered again.

7.3.3 Device Security

The BQ78709-Q1 device includes two security modes: SEALED and FULLACCESS, which can be used to limit the ability to view or change settings.

- In SEALED mode, most data and status can be read using commands and subcommands, but only selected settings can be changed. Data memory settings cannot be changed directly.
- FULLACCESS mode allows the capability to read and modify all device settings.

Selected settings in the device can be modified while the device is in operation through supported commands and subcommands, but in order to modify all settings, the device must enter CONFIG_UPDATE mode (see CONFIG_UPDATE Mode), which stops the device operation while settings are being updated. After the update is completed, the operation is restarted using the new settings. CONFIG_UPDATE mode is only available in FULLACCESS mode.

The BQ78709-Q1 device implements a key-access scheme to transition between SEALED and FULLACCESS modes. Changing from SEALED to FULLACCESS requires that a unique set of keys be sent to the device through subcommands. Refer to *BQ76907 Technical Reference Manual* for more details.

7.4 Device Hardware Features

7.4.1 Voltage ADC

The BQ78709-Q1 integrates a delta-sigma voltage ADC that is multiplexed between measurements of cell voltages, an internal temperature sensor, an external thermistor, as well as performs measurements of the voltage at the VC7 pin, the internal 1.8V LDO voltage, and the VSS rail (the latter two are for diagnostic purposes). The BQ78709-Q1 device supports measurements of individual differential cell voltages in a series configuration, ranging from 2-series cells to 7-series cells. Each cell voltage measurement is a differential measurement of the voltage between two adjacent cell input pins, such as VC1–VC0, VC2–VC1, and so forth. The cell voltage measurements are processed based on trim and calibration corrections and then reported in a 16-bit resolution using units of 1mV.

The ADC takes its input from the ADC multiplexer and generates a high-speed digital data stream which is digitally filtered to produce a 24-bit output. The ADC uses the 262.144kHz LFO clock as its sampling clock. The digital filter includes programmable decimation rates, which result in data generated at different intervals and with differing resolutions. The effective resolution (defined as the resolution such that the data exhibits 1-sigma variation with ±1 LSB) of the ADC conversions changes as the decimation rate changes, with effective resolution increasing as the output rate is reduced.

7.4.2 Coulomb Counter and Digital Filters

The BQ78709-Q1 device monitors pack current using a low-side sense resistor that connects to the SRP and SRN pins through an external RC filter, which must be connected such that a charging current will create a positive voltage on SRP relative to SRN. The differential voltage between SRP and SRN is digitized by an integrated delta-sigma coulomb counter ADC, which can digitize voltages over a ±200mV range and uses multiple digital filters to provide optimized measurement of the instantaneous, averaged, and integrated current. The device supports a wide range of sense resistor values, with a larger value providing better resolution for the digitized result. The maximum value of the sense resistor must be limited to ensure the differential voltage remains within the ±200mV range for system operation when the current measurement is desired. For example, a system with a maximum discharge current of 200A during normal operation (not a fault condition) should limit the sense resistor to 1mΩ or below.

Multiple digitized current values, as well as an accumulated charge integration, are available for readout over the serial communications interface, including two using separate hardware digital filters, CC1 and CC2. Further detail on the current measurements and charge integration results available are provided in Current Measurement and Charge Integration.

7.4.3 Protection FET Drivers

The BQ78709-Q1 integrates low-side CHG and DSG FET drivers, which can directly drive low-side protection NFET transistors. The device supports both series and parallel FET configurations, providing FET body diode protection when configured for a series FET configuration, if one FET driver is on, and the other FET driver is off. When body diode protection is enabled, the DSG driver may be turned on to prevent FET damage if the battery pack is charging while a discharge inhibit fault condition is present. Similarly, the CHG driver may be turned on if the pack is discharging while a charge inhibit fault condition is present. These decisions depend on the detection of a current with an absolute value over the programmable body diode threshold, which uses the coulomb counter current measurement for its decision.

The DSG pin is driven high when not blocked by command and when no related faults (such as UV, OTD, UTD, OCD1, OCD2, SCD, and select diagnostics), which are configured for autonomous control are present, or for body diode protection. The driver can be forced on by command, but the command will only take effect if configuration settings allow.

The DSG driver is designed to allow users to select an optimal resistance in series between the DSG pin and the DSG FET gate to achieve the desired FET rise and fall time per the application requirement and the choice of FET characteristics. When the DSG FET is turned off, the DSG pin drives low, and all overcurrent in discharge protections (OCD1, OCD2, SCD) are disabled to better conserve power. These resume operation when the DSG FET is turned on. Device configuration settings determine which protection will autonomously control the appropriate FET driver.

The CHG pin is driven high only when not blocked by command and when no related faults (OV, OTC, UTC, OCC, SCD, and select diagnostics) which are configured for autonomous control are present, or for body diode protection. The driver can be forced on by command, but the command will only take effect if configuration settings allow. Turning off the CHG pin does not influence the overcurrent protection circuitry. The CHG FET driver actively drives the CHG pin high when enabled, and actively drives the pin low to approximately 0.5V above the VSS voltage for about 100µs when disabled, then allows the pin to settle to the PACK- voltage through the external CHG FET gate-source resistor. If a charger is attached to the pack while the CHG FET is disabled, the CHG pin can fall to a voltage as low as 25V below the device VSS, per the device's electrical specifications. Due to the 100µs time interval during which CHG is actively pulled low, the time constant of the CHG drive circuit (made up of the driver effective resistance, any series resistance between the CHG pin and the CHG FET gate, and the FET gate capacitance) must be kept well below this level.

The BQ78709-Q1 includes PWM drive capability on the CHG and DSG FET drivers, which allows them to limit the average current flowing in a charge or discharge mode. The DSG FET driver actively drives the DSG pin high or low, based on the driver control, so can implement continual switching to turn on and off the DSG FET. If a charger is not attached, then the CHG driver can also implement continual switching in PWM mode. If a charger is attached with a voltage significantly above the pack voltage, then the CHG FET gate voltage will

generally be driven to approximately VSS + 0.5V quickly, then will settle to the lower PACK- voltage more slowly, depending on the system capacitance. See the *BQ76907 Technical Reference Manual* for more information.

7.4.4 Voltage References

The BQ78709-Q1 device includes two voltage references, VREF1 and VREF2, with VREF1 used by the voltage ADC for voltage measurements except the external thermistor. VREF2 is used by the coulomb counter, the integrated 1.8V LDO, and the internal oscillator. The value of VREF2 can be determined indirectly by the voltage ADC's measurement of the internal 1.8V LDO voltage while using VREF1. This measurement is available through a command for diagnostic purposes. If this measurement result exceeds an allowed range, a diagnostic alert or fault is triggered (if enabled by settings).

7.4.5 Multiplexer

The multiplexer connects various signals to the voltage ADC, including the individual differential cell voltage pins, the on-chip temperature sensor, the biased thermistor pin, the internal 1.8V LDO voltage, the top-of-stack voltage, and the VSS pin voltage. The multiplexer input circuitry is customized to support the range and level of voltage required for each particular input.

7.4.6 LDOs

The BQ78709-Q1 contains an integrated 1.8V LDO (REG18) that provides a regulated 1.8V supply voltage for the device's internal circuitry and digital logic. The supply current for this LDO is drawn from the BAT pin.

The device also integrates a programmable LDO (REGOUT) for external circuitry, such as a host processor or external transceiver circuitry. The REGOUT LDO's input is the REGSRC pin, which is generally expected to be connected to the top-of-the-stack, or the REGSRC voltage can be generated by a separate DC/DC converter in the system. The REGOUT LDO can provide an output current of up to 20mA if thermal conditions permit.

The REGOUT LDO can be programmed to either remain disabled or power up automatically whenever the device exits SHUTDOWN mode, depending on OTP configuration. The LDO output voltage can be programmed to 1.8V, 2.5V, 3.0V, 3.3V, or 5.0V by modifying configuration settings. When the REGOUT LDO is disabled and the device is in NORMAL, SLEEP, or DEEPSLEEP modes, the output is pulled to VSS with an internal resistance of approximately 2.5kΩ. If the LDO is configured based on OTP settings to be powered, then at each later power-up the device autonomously loads the OTP settings and enables the LDO as configured, without requiring communications first.

The BQ78709-Q1 is designed to operate properly with a die temperature of up to 125°C, therefore the system design must avoid drawing excessive current from the REGOUT LDO if this results in the die temperature exceeding this level. For example, with a stack voltage of 31.5V, and REGOUT programmed to an output voltage of 2.5V, the device dissipates approximately 580mW when supplying 20mA of load current. The package thermal impedance can be used to then calculate the resulting die temperature based on the maximum ambient temperature expected. If this exceeds the device's specified temperature range, the load current must be limited in the system.

The BQ78709-Q1 includes a die temperature monitor which detects if the die temperature exceeds approximately 120°C. If this occurs, the REGOUT LDO is disabled, and depending on configuration setting, the device also enters SHUTDOWN mode. If the REGOUT LDO is disabled due to overtemperature (but the device is not shut down) and the die temperature reduces below the threshold, the REGOUT LDO automatically powers on again.

7.4.7 Standalone Versus Host Interface

The BQ78709-Q1 can be configured to operate in a completely standalone mode, without any host processor in the system, or together with a host processor. If in standalone mode, the device can monitor conditions, control FETs based on threshold settings, and recover FETs when conditions allow, all without requiring any interaction with an external processor. If a host processor is present, the device can still be configured to operate fully autonomously, while the host processor can read measurements and exercise control as desired. Alternatively, the device can be configured for manual host control, such that the device can monitor and provide a flag when a protection alert or fault has occurred, but will rely on the host to disable FETs. Using the device in standalone

mode requires that all settings are programmed into the OTP by TI. This is only available for cases involving a significant shipment volume. Please contact your TI sales representative for information on this option.

The BQ78709-Q1 can be entirely configured by a host processor writing all settings to the device's internal registers across the serial communications interface, without requiring any OTP programming. Using this approach, settings must be reloaded from the host each time the device is reset or enters SHUTDOWN mode and is restarted.

7.4.8 ALERT Pin Operation

The BQ78709-Q1 includes functionality to generate an alarm signal at the ALERT pin, which can be used as an interrupt to a host processor. The ALERT pin is an open-drain pin which will be pulled low by the device whenever an alarm signal is generated. The alarm function includes a programmable mask, to allow the customer to decide which flags or events can trigger an alarm. The selected alarm flags remain latched until the host processor reads their status and clears the triggered alarm bits. The alarm mask can be changed during field operation, to mask or unmask individual flags from generating an alarm signal. The device also provides the unlatched, instantaneous value of each flag, in addition to the latched version. See the *BQ76907 Technical Reference Manual* for more details on this function.

7.4.9 Low Frequency Oscillator

The low-frequency oscillator (LFO) in the BQ78709-Q1 operates continuously while in NORMAL and SLEEP modes, and depending on the setting is shutdown (except when needed) during DEEPSLEEP mode. The LFO runs at approximately 262.144kHz during NORMAL mode and reduces to approximately 32.768kHz in SLEEP mode. The LFO is trimmed during manufacturing to meet the specified accuracy across temperatures.

7.4.10 I²C Serial Communications Interface

The I²C serial communications interface in the BQ78709-Q1 acts as a target device and supports rates up to 400kHz with an optional CRC check. The BQ78709-Q1 will initially power up by default in a mode determined by the OTP settings factory programmed by TI. The host can change the CRC mode setting while in CONFIG_UPDATE mode, then the new setting will take effect upon exit of CONFIG_UPDATE mode.

The I²C device address (as an 8-bit value including target address and R/W bit) is set by default as 0x10 (write), 0x11 (read), which can also be changed by the configuration setting.

The communications interface includes programmable timeout capability, with the internal I2C bus logic reset when an enabled timeout occurs. This is described in detail in the *BQ76907 Technical Reference Manual*.

An I²C write transaction is shown in Figure 7-1. Block writes are allowed by sending additional data bytes before the Stop. The I²C logic will auto-increment the register address after each data byte. The shaded regions show when the device may be clock stretching.

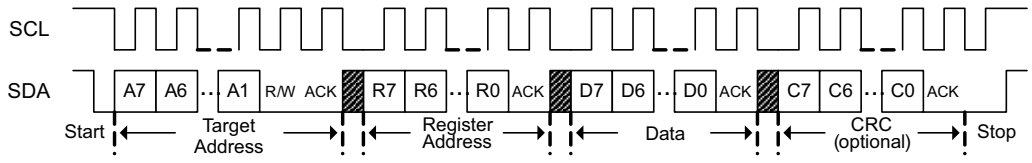


Figure 7-1. I²C Write

The CRC check is enabled by setting a data memory bit. When enabled, the CRC is calculated as follows:

- Note that the CRC is reset after each data byte and after each stop.
- In a single-byte write transaction, the CRC is calculated over the target address, register address, and data.
- In a block write transaction, the CRC for the first data byte is calculated over the target address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the target detects an invalid CRC, the I²C target will NACK the CRC, which causes the I²C target to go to an idle state.

Figure 7-2 shows a read transaction using a Repeated Start. The shaded regions show when the device may be clock stretching.

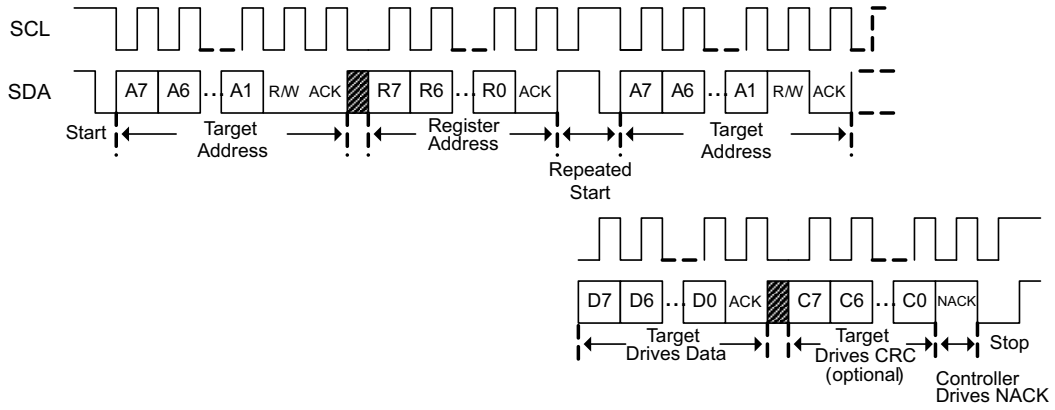


Figure 7-2. I²C Read with Repeated Start

Figure 7-3 shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read, the controller ACK's each data byte except the last and continues to clock the interface. The I²C block will auto-increment the register address after each data byte. The shaded regions show when the device may be clock stretching.

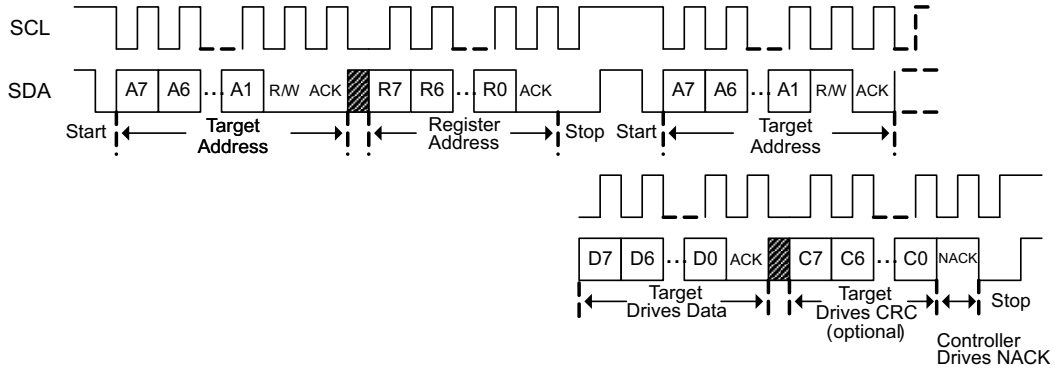


Figure 7-3. I²C Read Without Repeated Start

When enabled, the CRC for a read transaction is calculated as follows:

- Note that the CRC is reset after each data byte and after each stop.
- In a single-byte read transaction using a repeated start, the CRC is calculated beginning at the first start, so will include the target address, the register address, then the target address with read bit set, then the data byte.
- In a single-byte read transaction using a stop after the initial register address, the CRC is reset after the stop, so will only include the target address with read bit set and the data byte.
- In a block read transaction using repeated starts, the CRC for the first data byte is calculated beginning at the first start and will include the target address, the register address, then the target address with read bit set, then the data byte. The CRC for subsequent data bytes is calculated over the data byte only.
- In a block read transaction using a stop after the initial register address, the CRC is reset after the stop, so will only include the target address with read bit set and the first data byte. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the controller detects an invalid CRC, the I²C controller will NACK the CRC, which causes the I²C target to go to an idle state.

For more information, see the *BQ76907 Technical Reference Manual*.

7.5 Measurement Subsystem

7.5.1 Voltage Measurement

The BQ78709-Q1 device integrates a voltage ADC which is multiplexed between measurements of cell voltages, an internal temperature sensor, the TS pin, and also performs measurements of the voltage at the VC7 pin, the internal 1.8V LDO voltage, and the VSS rail (for diagnostic purposes). The BQ78709-Q1 device supports measurement of individual differential cell voltages in a series configuration, ranging from 2-series cells to 7-series cells. Each cell voltage measurement is a differential measurement of the voltage between two adjacent cell input pins, such as VC1-VC0, VC2-VC1, and so forth. The cell voltage measurements are processed based on trim corrections and then reported in 16-bit resolution using units of 1mV. The cell voltage measurements can support a recommended voltage range from -0.2V to 5.5V. The voltage ADC saturates at a level of 5 × VREF1 (approximately 6.06V) when measuring cell voltages, although for best performance it is recommended to stay at a maximum input of 5.5V.

7.5.1.1 Voltage ADC Scheduling

The BQ78709-Q1 voltage measurements are taken in a nested measurement loop that consists of multiple measurement slots. All active cell voltages are measured on each ADSCAN loop, then one slot is a "Shared Slot" which is used for different purposes (additional system and diagnostic measurements) on successive ADSCAN loops, resulting in a total of three (if two cells are active) to eight (if 7 cells are active) slots per ADSCAN loop. The width of the measurement slots is programmable, which allows each ADSCAN to range from about 1.1ms to 24ms during NORMAL mode, based on the setting.

The schedule of measurements is different in SLEEP mode versus NORMAL mode, and there is also a special measurement schedule used after initial powerup or reset to provide a fast powerup for the system. The details of the remaining measurement loops and the differences versus operating mode are described in the *BQ76907 Technical Reference Manual*.

7.5.1.2 Unused VC Pins

If the BQ78709-Q1 device is used in a system with fewer than 7-series cells, specific cells must be used for connection to real cells, as shown in Table 7-1. The unused cell inputs must be shorted out on the circuit board. The device only measures and reports data for those cells designated as real cells.

Table 7-1. Cell Usage

Number of Cell Used	Cell Connections	Shorted Connections
7	VC7–VC6, VC6–VC5, VC5–VC4, VC4–VC3, VC3–VC2, VC2–VC1, VC1–VC0	–
6	VC7–VC6, VC6–VC5, VC5–VC4, VC3–VC2, VC2–VC1, VC1–VC0	VC4–VC3
5	VC7–VC6, VC5–VC4, VC3–VC2, VC2–VC1, VC1–VC0	VC6–VC5, VC4–VC3
4	VC7–VC6, VC5–VC4, VC3–VC2, VC1–VC0	VC6–VC5, VC4–VC3, VC2–VC1
3	VC7–VC6, VC5–VC4, VC1–VC0	VC6–VC5, VC4–VC3, VC3–VC2, VC2–VC1
2	VC7–VC6, VC1–VC0	VC6–VC5, VC5–VC4,VC4–VC3, VC3–VC2, VC2–VC1

The unused cell input pins must be shorted to adjacent cell input pins, as shown in Figure 7-4 for a 6-series system.

It is also important to note that the range of voltages supported by the different VC pins differs depending on the pin. For example, pins VC5, VC6, and VC7 can only support measurements if their pin voltage is greater than or equal to 2V. Thus if implementing a 2-series system using the top and bottom cell input pins, the upper cell voltage may not be measured correctly if the lower cell voltage drops below 2V, since then VC6 would be below 2V.

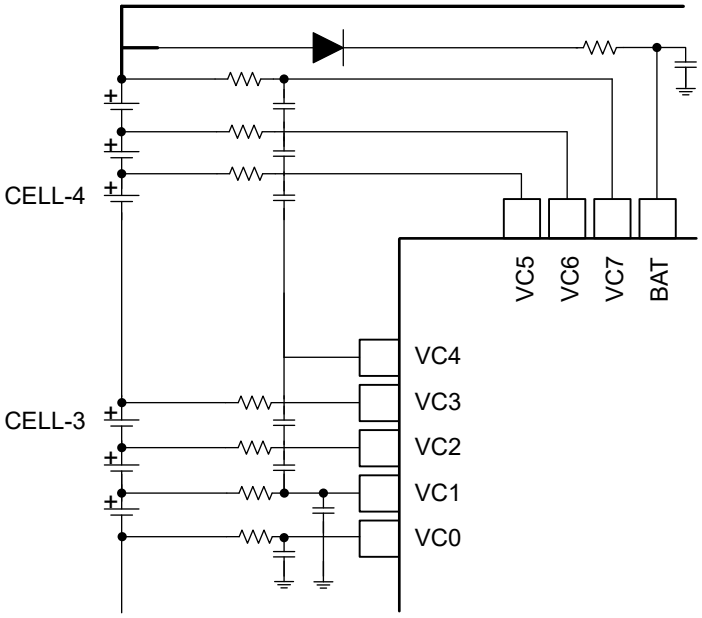


Figure 7-4. Connecting an Unused Cell Input Pin

The device data memory must be configured to specify which cell inputs are used for actual cells. The device uses this information to disable cell voltage protections associated with inputs that are not used. Voltage measurements for inputs used for real cells are reported in 16-bit format (in units of mV). See the *BQ76907 Technical Reference Manual* for further details.

7.5.1.3 General Purpose ADCIN Functionality

The TS pin on the BQ78709-Q1 device can be used for general purpose ADC input (ADCIN) measurement, if not being used for temperature measurement of a thermistor. When used for ADCIN functionality, the internal bandgap reference is used by the ADC, and the input range of the ADC is limited to 1.8V. The digital fullscale range of the ADC is effectively 1.6667 × VREF1, which is approximately 2.02V during normal operation.

The data memory settings control whether the TS pin is used for a thermistor or as a general-purpose ADC input. The resulting measurement of the TS pin is available in units of 16-bit ADC counts.

7.5.2 Current Measurement and Charge Integration

The BQ78709-Q1 device monitors pack current using a low-side sense resistor that connects to the SRP and SRN pins through an external RC filter, which must be connected such that a charging current will create a positive voltage on SRP relative to SRN. The differential voltage between SRP and SRN is digitized by an integrated coulomb counter ADC, which can digitize voltages over a ±200mV range and uses multiple digital filters to provide optimized measurement of the instantaneous and integrated current. The device supports a wide range of sense resistor values, with a larger value providing better resolution for the digitized result. The maximum value of the sense resistor must be limited to ensure the differential voltage remains within the ±200mV range for system operation when the current measurement is desired. For example, a system with a maximum discharge current of 200A during normal operation (not a fault condition) should limit the sense resistor to 1mΩ or below.

The SRP and SRN pins can also support higher positive voltages relative to VSS, such as may occur during overcurrent or short circuit in discharge conditions, without damage to the device, although the current is not accurately digitized in this case. For example, a system with a 1mΩ sense resistor and the Short Circuit in Discharge protection threshold programmed to a 500mV level would trigger an SCD protection fault when a discharge current of 500A was detected.

The coulomb counter integrates two hardware digital filters (CC1 and CC2), which each provide a separate digital output. The CC2 digital filter generates a 24-bit raw output and has programmable timing and resolution

output, with the output rate also affecting the resolution of the conversion. The effective resolution (defined as the resolution such that the data exhibits 1-sigma variation with ±1 LSB) of the coulomb counter conversions increases with longer timing between output data. The setting options when the coulomb counter is in full power mode are 366µs (which results in lowest effective resolution), 732µs, 1.46ms, or 2.93ms (which results in highest effective resolution). This output rate is set using data memory configuration bits. In addition, the coulomb counter supports a low power mode, which operates at a 16 times slower rate than the settings listed above, with similar resolution performance at each setting, but drawing only 4µA rather than ~60µA at full power.

The CC1 filter generates a 16-bit current measurement that is used for charge integration and other decision purposes, with one output generated every 250ms when the device is operating in NORMAL mode and the coulomb counter in full power mode, or one output every 4 seconds when the device is operating in low power mode.

The integrated passed charge (from integration of the CC1 processed result) is available as a 48-bit value, which includes the upper 16 bits of accumulated charge as the integer portion, the lower 32 bits of accumulated charge as the fractional portion, and a 32-bit accumulated time over which the charge has been integrated in units of seconds. The accumulated charge integration and timer can be reset by a command from the host over the digital communications interface. Note that the charge and time are not integrated while in SLEEP mode.

See the *BQ76907 Technical Reference Manual* for more details on current measurement, charge integration, and their associated programmable settings.

7.5.3 Internal Temperature Measurement

The BQ78709-Q1 device integrates the capability to measure its internal die temperature by digitizing the difference in internal transistor base-emitter voltages. This voltage is measured periodically as part of the measurement loop and is processed to provide a reported temperature value available through the digital communications interface.

The internal temperature is also compared to a programmable protection threshold to implement a die overtemperature protection. In response to this protection, the device can be configured to disable FETs and optionally enter SHUTDOWN mode. For more information on this, refer to the Internal Overtemperature Protection section in the *BQ76907 Technical Reference Manual*.

7.5.4 Thermistor Temperature Measurement

The BQ78709-Q1 device supports measurement of an external thermistor on the TS pin. The device includes an internal 20kΩ pullup resistor to bias the thermistor during measurement. The TS pin can be selected for thermistor measurement or general purpose ADCIN measurement using a data memory setting.

When the pin is selected for thermistor measurement, the internal pullup resistor is used to bias the pin during the measurement. In order to provide a high precision result, the device uses the same 1.8V internal LDO voltage for the ADC reference as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric measurement that removes the error contribution from the LDO voltage level. Because the pullup resistor is only enabled during the pin measurement, it is recommended to limit the capacitance at this node to reduce the effect of incomplete settling when the pullup resistor is biased. The capacitance is recommended to stay below 4nF when in highest resolution mode, or 500pF when in highest speed mode.

If the pin is selected for general purpose ADCIN measurement, the pullup resistor is not enabled during measurement, and the ADC uses VREF1 for its reference when measuring the pin.

The data is reported in units of 16-bit ADC counts. The fullscale digital value reflects an analog input level of its reference × 5 / 3. So when the TS pin is measuring a thermistor in ratiometric mode using the 1.8V internal regulator for its reference, the 16-bit LSB is 1.8V × 5 / 3 / 32768 ≅ 91.55µV. When the TS pin is measuring in ADCIN mode using the VREF1 reference, the 16-bit LSB is VREF1 × 5 / 3 / 32768 ≅ 61.80µV.

7.5.5 Factory Trim and Calibration

The BQ78709-Q1 device includes factory trim for the cell voltage ADC measurements, the stack measurement, the internal die temperature measurement, and the current measurements to optimize the measurement

performance even if no further calibration is performed by the customer. The trim information is used to correct the raw ADC readings before they are reported as 16-bit values after processing. The current measurement trim is performed to provide units of mA assuming a 1mΩ external sense resistor is used, although this can be modified by the user if different units are desired. The trimmed offset and gain values can be modified by the user to perform calibration on the customer production line, to further optimize performance in the system. For more details, see the *BQ76907 Technical Reference Manual*.

7.6 Protection Subsystem

7.6.1 Protections Overview

The BQ78709-Q1 integrates an extensive primary protection subsystem that can monitor a variety of parameters, initiate protective actions, and autonomously recover based on conditions. The device also includes a wide range of flexibility, such that the device can be configured to monitor and initiate protective action, but with recovery controlled by the host processor, or such that the device only monitors and alerts the host processor whenever conditions warrant protective action, but with action and recovery fully controlled by the host processor.

The protection subsystem includes a suite of individual protections which can be individually enabled and configured, including cell undervoltage and overvoltage, overcurrent in charge, two separate overcurrent in discharge protections, short circuit current in discharge, cell overtemperature and undertemperature in charge and discharge, internal die overtemperature, and a host processor communication watchdog timeout. The overcurrent in charge and discharge and short circuit in discharge protections are based on comparator decisions, while the remaining protections (such as those involving cell voltage, temperature, and host watchdog) are based on ADC measurement or logic operation. The device integrates NFET drivers for low-side CHG and DSG protection FETs, which can be configured in a series or parallel configuration and can also be used in pulse-width modulation mode to manually implement precharge or predischarge functionality.

7.6.2 Primary Protections

The BQ78709-Q1 integrates a broad suite of protections for battery management and provides the capability to enable individual protections, as well as to select which protections will result in autonomous control of the FETs. See the *BQ76907 Technical Reference Manual* for detailed descriptions of each protection function. The primary protection features include:

- Cell Undervoltage Protection
- Cell Overvoltage Protection
- Cell Open Wire Protection
- Overcurrent in Charge Protection
- Overcurrent in Discharge Protection (two tiers)
- Short Circuit in Discharge Protection
- Current Protection Latch
- Undertemperature in Charge Protection
- Undertemperature in Discharge Protection
- Overtemperature in Charge Protection
- Overtemperature in Discharge Protection
- Internal Overtemperature Protection
- Host Watchdog Fault Protection

The device also includes additional diagnostic checks which can also result in autonomous control of the FETs, depending on configuration settings.

7.6.3 CHG Detector

The BQ78709-Q1 provides a signal that indicates if the CHG pin voltage is above a level of approximately 2V. The raw value of this flag can be read through the communications interface, and an alarm can be generated on the ALERT pin whenever the debounced version of this flag changes state, based on device settings. This flag can be used by the system to assist in recovery from a current fault condition.

When a current fault occurs in a system, such as a short circuit event, the device generally disables its DSG FET and maybe also the CHG FET, depending on the settings. The device can be configured to wait a programmed delay and then reenable the FETs. If the short circuit condition is still present, then a new fault will be triggered, and the FETs disabled again. If a short persists, this cycle of periodically recovering and retriggering a fault can continue indefinitely, which is generally not acceptable.

An alternative is to only allow a limited number of retries and then disable further retries after that limit is reached. This capability is supported using the Current Protection Latch. This avoids the indefinite cycle of retries but then may render the pack unusable after retries are stopped.

If the pack is removable, such as in a power tool, then another option is to keep the FETs disabled until the pack has been removed from the system. In this case, if the CHG driver is disabled and a charger is not connected, then the CHG pin will be pulled up to the PACK+ voltage while a load is connected, resulting in the CHG Detector signal being asserted. When the pack is removed from the system (and the charger is still not connected), then the CHG pin will generally fall to near the BAT- voltage level, resulting in the CHG Detector signal being deasserted. A host processor within the battery pack can then use this signal to trigger recovery of the pack.

Note that the use of this CHG Detector for load removal is dependent on the system configuration and may not be usable in all cases. Thus, it is important for the pack designer to evaluate whether it will be applicable to the system or not. For more information on the CHG detector, see the *BQ76907 Technical Reference Manual*.

7.6.4 Cell Open-Wire Protection

The BQ78709-Q1 device supports the detection of a broken connection between a cell in the pack and the cell attachment to the PCB containing the BQ78709-Q1 device. Without this check, the voltage at the cell input pin of the BQ78709-Q1 device may persist for some time on the board-level capacitor, leading to incorrect voltage readings. The Cell Open Wire detection in the BQ78709-Q1 device operates by enabling a small current source from each cell to VSS at programmable intervals. If a cell input pin is floating due to an open wire condition, this current discharges the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage eventually triggers a protection fault on that particular cell and the cell above it.

The Cell Open Wire current will be enabled at a periodic interval set by configuration register. This provides programmability in the average current drawn from about 5.4nA to about 1.1µA, based on the typical current level of 55µA. See the *BQ76907 Technical Reference Manual* for more details.

Note

The Cell Open Wire check can create a cell imbalance, so the settings must be selected appropriately.

7.6.5 Diagnostic Checks

The BQ78709-Q1 includes several measurements and checks for diagnostic purposes. Some of these will trigger a protection fault, but they generally do not include an alert phase with a programmable delay period, they will immediately trigger a fault when they are detected. They are not all autonomously recoverable, but some can be manually recovered using a subcommand sent by the host. For more detail on each diagnostic, see the *BQ76907 Technical Reference Manual*.

VREF1 vs VREF2 Check—The device performs a regular comparison of the two internal voltage references and can trigger a fault if the result is outside an acceptable range. This is implemented using a measurement of the internal 1.8V LDO voltage (which is based on VREF2) with the ADC using VREF1 for its reference.

VSS Check—The device also includes a regular measurement of the VSS voltage as part of the measurement loop, comparing the resulting value to the expected value, to implement the VSSF diagnostic protection.

Stack Check—The device includes a regular measurement of the top-of-stack (TOS) voltage as part of the measurement loop. This measurement can be used by the host to compare with the sum of the individual differential cell voltage measurements, with a significant difference possibly indicating some type of malfunction.

REGOUT Check—The REGOUT LDO generates a flag if an error is detected, such as the regulator is in short circuit current limit. When detected, the device triggers the REGOUT Diagnostic Fault and can disable FETs based on settings.

LFO Integrity Check—The device integrates a special hardware block that monitors if the LFO stops oscillating or drops significantly in frequency versus its expected value. If this is detected, the device immediately transitions into SHUTDOWN mode.

Internal Factory Trim Check—The device includes a check of the digital trim and setting information within the device at the initial power-up or after any full reset. If an error is detected during this check, the device will immediately transition to SHUTDOWN mode.

Hardware Overtemperature Detector—The device integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device will automatically begin the sequence to enter SHUTDOWN, based on the configuration setting.

7.7 Cell Balancing

The BQ78709-Q1 supports passive cell balancing by bypassing the current of a selected cell using either integrated bypass switches between cells or external bypass FET switches. Balancing must be initiated and controlled manually from a host processor. For further details, see the *BQ76907 Technical Reference Manual*.

Adjacent as well as non-adjacent cells can be balanced. Balancing is controlled via subcommand from the host. When balancing is initiated, the device starts a timer and will begin balancing the specified cells for up to 20 seconds. The timer is reset if a new balancing subcommand is issued. This is included as a precaution, in case the host processor initiated balancing but then stopped communication with the BQ78709-Q1, so that balancing would not continue indefinitely. The host can also use the subcommand to disable balancing earlier when desired. When the subcommand is read, it reports a bitmask of which cells are being actively balanced.

The device can be configured to block balancing from being initiated while the pack is in SEALED mode if balancing is not intended to be utilized. The device can also be configured to disable balancing if the thermistor temperature or die temperature exceeds programmable thresholds. The customer should carefully analyze the thermal effect of the balancing on the device in the system. Based on the planned ambient temperature of the device during operation and the thermal properties of the package, the maximum power must be calculated that can be dissipated within the device and still ensure operation remains within the recommended operating temperature range. The cell balancing configuration can then be determined such that the device power remains below this level by reducing the number of cells being balanced simultaneously, or by reducing the balancing current of each cell by appropriate selection of the external resistance in series with each cell.

Due to the current that flows into the cell input pins on the BQ78709-Q1 while balancing is active, the measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. Balancing is temporarily disabled during the regular measurement loop while cell voltages or the top of stack voltage is being measured by the ADC. This occurs on every measurement loop, and so can result in a significant reduction in the average balancing current that flows. To help alleviate this, the device includes configuration bits to slow the measurement loop speed when cell balancing is active, which thereby increases the average balancing current. When the measurement loop is slowed, the response time to cell overvoltage or undervoltage conditions is also slowed accordingly.

7.8 Device Operational Modes

7.8.1 Overview of Operational Modes

This device provides four operational modes to support optimized features and power dissipation, with the device able to transition between modes either autonomously or controlled by a host processor.

- NORMAL mode: In this mode, the device performs frequent measurements of system current, cell voltages, internal and thermistor temperature, and various other voltages, operates protections as configured, and provides data and status updates. Battery protections are enabled, and the FET drivers are typically enabled (in the absence of any protection fault).

- SLEEP mode: In this mode, the device performs measurements, calculations, and data updates at adjustable time intervals. Between the measurement intervals, the device is operating in a reduced power stage to minimize total average current consumption. Battery protections are still enabled, and the FET drivers are typically enabled (in the absence of any protection fault).
- DEEPSLEEP mode: In this mode, the FET drivers are disabled, all battery protections are disabled, and no current or voltage measurements are taken. The REGOUT LDO can be kept powered, to maintain power to external circuitry, such as a host processor. Communications using I^2C are still active.
- SHUTDOWN mode: The device is completely disabled (including the internal 1.8V and REGOUT LDO), the CHG and DSG FETs are both disabled, all battery protections are disabled, and no measurements are taken. This is the lowest power state of the device, which may be used for shipment or long-term storage. All register settings are lost when in SHUTDOWN mode.

The device also includes a CONFIG_UPDATE mode, which is used for parameter updates. Transitioning between operational modes is shown in BQ78709-Q1 Operational Power Modes.

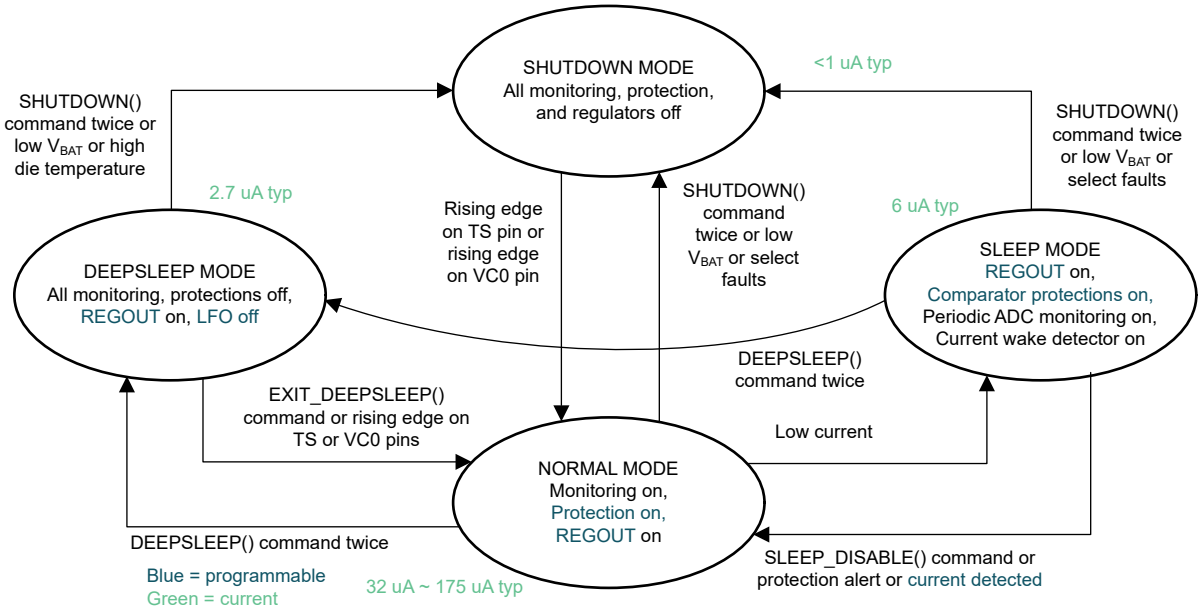


Figure 7-5. BQ78709-Q1 Operational Power Modes

7.8.2 NORMAL Mode

NORMAL mode is the highest performance mode of the device, in which the device is making regular measurement of voltage, current, and temperature, and the LFO (low frequency oscillator) is operating at full speed. Full battery protections are operating, based on device configuration settings. Measurements of cell voltages, current, temperature, and other parameters are taken continuously, with timing determined by settings.

The device will generally be in NORMAL mode whenever any active charging or discharging is underway. When the current measurement falls below a programmable current threshold, the system is considered in relax mode, and the device can autonomously transition into SLEEP mode, depending on the configuration. The device includes a current wake detector, which will trigger the device to exit SLEEP mode and return to NORMAL mode if a current in excess of a programmable threshold is detected.

7.8.3 SLEEP Mode

SLEEP mode is a reduced functionality state that can be optionally used to reduce power dissipation when there is little or no system load current or charging in progress, but still provides voltage at the battery pack terminals to keep the system alive. At initial power-up, the configuration setting determines whether the device can enter SLEEP mode. After initialization, SLEEP mode can be allowed or disallowed using subcommands. The device

includes a status bit available via command which indicates whether the device is presently in SLEEP mode or not.

When the magnitude of the current measurement falls below a programmable current threshold, the system is considered in relax mode, and the device will autonomously transition into SLEEP mode, if settings permit. During SLEEP mode, comparator-based protections operate the same as during NORMAL mode. Measurements of current, voltage, and temperature are taken using the ADC and coulomb counter at programmable intervals.

The device will exit SLEEP mode if a protection fault occurs, or current begins flowing, or via subcommand. The current is checked approximately every 2.44ms and, if it exceeds a programmable level in magnitude, the device transitions back to NORMAL mode.

The device also includes a 10-second hysteresis on the SLEEP mode entrance to avoid the device quickly entering and exiting SLEEP mode based on a dynamic load. After transitioning from SLEEP mode to NORMAL mode, the device will not enter SLEEP mode again for 10 seconds unless overridden via subcommand. For more details, see the *BQ76907 Technical Reference Manual*.

7.8.4 DEEPSLEEP Mode

The BQ78709-Q1 integrates a DEEPSLEEP mode, which is a low-power mode that allows the REGOUT LDO to remain powered, but disables most other subsystems. In this mode, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, and all voltage, current, and temperature measurements are disabled.

DEEPSLEEP mode can be entered through a subcommand sent by the host. The device will exit DEEPSLEEP mode and return to NORMAL mode if directed via subcommand or upon a rising edge on the TS or VC0 pins. In addition, if the BAT pin voltage falls below V_{PORA} - V_{PORA_HYS} while in DEEPSLEEP mode, the device will transition to SHUTDOWN mode.

When the device exits DEEPSLEEP mode and returns to NORMAL mode, it first completes a startup measurement loop and evaluates conditions relative to enabled protections, to ensure that conditions are acceptable to proceed. This may take approximately 8ms plus the time for the measurement loop to complete.

The REGOUT LDO will maintain its power state when entering DEEPSLEEP mode. The LFO may be disabled during DEEPSLEEP mode based on the setting. If disabled, it is wakened by I^2C communications, which may result in a longer than normal clock stretch before the device responds to communications.

7.8.5 SHUTDOWN Mode

SHUTDOWN mode is the lowest power mode of the BQ78709-Q1, which can be used for shipping or long-term storage. In this mode, the device loses all register state information, the internal logic is powered down, and the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, all voltage, current, and temperature measurements are disabled, and no communications are supported. When the device exits SHUTDOWN, it will read parameters stored in OTP (which TI programmed), which effectively sets the default values for settings. After device powerup, settings can then be changed by the host writing device registers.

The device can enter SHUTDOWN mode when directed by the host via subcommand. It can also be configured to enter SHUTDOWN mode automatically based on the top of stack voltage or the minimum cell voltage. The shutdown based on cell voltage does not apply to cell input pins not used for actual cells.

While the BQ78709-Q1 is in NORMAL mode or SLEEP mode, the device can also be configured to enter SHUTDOWN mode if the internal temperature measurement exceeds a programmable threshold.

When the device is wakened from SHUTDOWN, it requires approximately 10ms for the internal circuitry to power up, load settings from OTP memory, perform initial measurements, evaluate those relative to enabled protections, and then to enable FETs if conditions and settings allow.

The BQ78709-Q1 integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device will automatically begin the sequence to enter SHUTDOWN, based on the configuration setting.

The BQ78709-Q1 will wake from SHUTDOWN if a voltage is applied at the TS or VC0 pins above a level of approximately 1.2V. If the shutdown sequence has been initiated, but the device detects the wakeup criteria are present, then the device will stay in a "soft shutdown" state until the wakeup criteria are removed. While in "soft shutdown," FETs are disabled, and protections and measurements are stopped. The device will exit "soft shutdown" when conditions allow the device to continue into SHUTDOWN mode. The host can abort the entry into SHUTDOWN mode via command, and the device will restart operation with a full reset.

7.8.6 CONFIG_UPDATE Mode

The BQ78709-Q1 uses a special CONFIG_UPDATE mode to make changes to the data memory settings. If changes were made to the data memory settings while the normal measurement and protection functions were in operation, it could result in unexpected operation or consequences if settings used by the logic changed in the midst of operation. Changes to the data memory settings should generally only be done on the customer manufacturing line or in an offline condition, such as immediately after being powered from SHUTDOWN.

When in CONFIG_UPDATE mode, the device stops normal operation and stops all measurements and protection monitoring. The host can then make changes to data memory settings. After changes are complete, the host then sends the command to exit CONFIG_UPDATE mode, at which point the device restarts normal operation using the new data memory settings. For more information, see the *BQ76907 Technical Reference Manual*.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The BQ78709-Q1 device can be used with 2-series to 7-series battery packs, supporting a top-of-stack voltage ranging from 3V up to 38.5V. To design and implement a comprehensive set of parameters for a specific battery pack, during development customers can use the Battery Management Studio (bqStudio), which is a graphical user-interface tool installed on a PC. Using bqStudio, the device can be configured for specific application requirements during development once the system parameters, such as fault trigger thresholds for protection, enable or disable of certain features for operation, configuration of cells, and more are known. This results in a "golden image" of settings that can then be programmed into the device registers.

8.2 Typical Application

BQ78709-Q1 7-Series Cell Typical Implementation (Simplified Schematic) shows a simplified application schematic for a 7-series battery pack, using the BQ78709-Q1 with an external secondary protector, a host microcontroller, and a communications transceiver. This configuration uses low-side CHG and DSG FETs in series. Several points to consider in an implementation are included below:

- A series diode is recommended at the BAT pin, together with a capacitor from the pin to VSS. These components allow the device to continue operating for a short time when a pack short circuit occurs, which may cause the top-of-stack voltage to drop to approximately 0V. In this case, the diode prevents the BAT pin from being pulled low with the stack, and the device will continue to operate, drawing current from the capacitor. Generally, operation is only required for a short time, until the device detects the short circuit event and disables the DSG FET. A Schottky diode can be used if low voltage pack operation is needed, or a conventional diode can be used otherwise.
- The FET CHG and DSG drivers use the REGSRC pin for their supply, so the user may also prefer to include a diode between the top of stack and the REGSRC pin, similar to that used for the BAT pin. If any resistance (> 1Ω) is included in series between the top of stack and the REGSRC pin, it is recommended to include a 1µF capacitor at the REGSRC pin to VSS. The REGSRC pin can be shorted to the BAT pin and a single diode used, but this may result in the BAT pin voltage dropping more rapidly during a short circuit event due to the increased loading of the REGOUT regulator drawing from the REGSRC pin.
- The recommended minimum voltage on the VC0 to VC4 pins extends down to –0.2V, while the recommended minimum voltage on the VC5 to VC7 pins is limited to 2.0V, relative to VSS. This restriction exists to ensure the specified cell voltage measurement accuracy.
- TI recommends using 100Ω resistors in series with the SRP and SRN pins, and a 100nF with optional 100pF differential filter capacitance between the pins for filtering. The routing of these components, together with the sense resistor, to the pins must be minimized and fully symmetric, with all components recommended to stay on the same side of the PCB with the device. Capacitors connected from the pins to VSS can provide filtering of common mode transients from reaching the pins, but they may also have a slight impact on current measurement performance.
- The filter network connected between the sense resistor and the SRP and SRN pins introduces an analog filter delay that can be important when fast current protections are required, such as in determining the short circuit in discharge (SCD) time until FETs are disabled. If the delay introduced by this network is too long, the resistance and capacitance values can be reduced. This will have a tradeoff of providing less analog filtering of high-frequency components.
- Due to thermistors often being attached to cells and possibly needing long wires to connect back to the device, it may be helpful to add a capacitor from the thermistor pin to the device VSS. However, it is important to not use too large of a value of capacitor, since this will affect the settling time when the thermistor is biased and measured periodically. A rule of thumb is to keep the time constant of the circuit < 5% of the

measurement time. When ***Settings:Configuration:DA Config[IADCSPEED1:0]*** = 0x0, the measurement time is approximately 3ms. When using this speed setting, the time constant should generally be less than (20kΩ) × C, so a capacitor less than 7.5nF is recommended. When using faster speed settings, the capacitor value must be reduced accordingly.

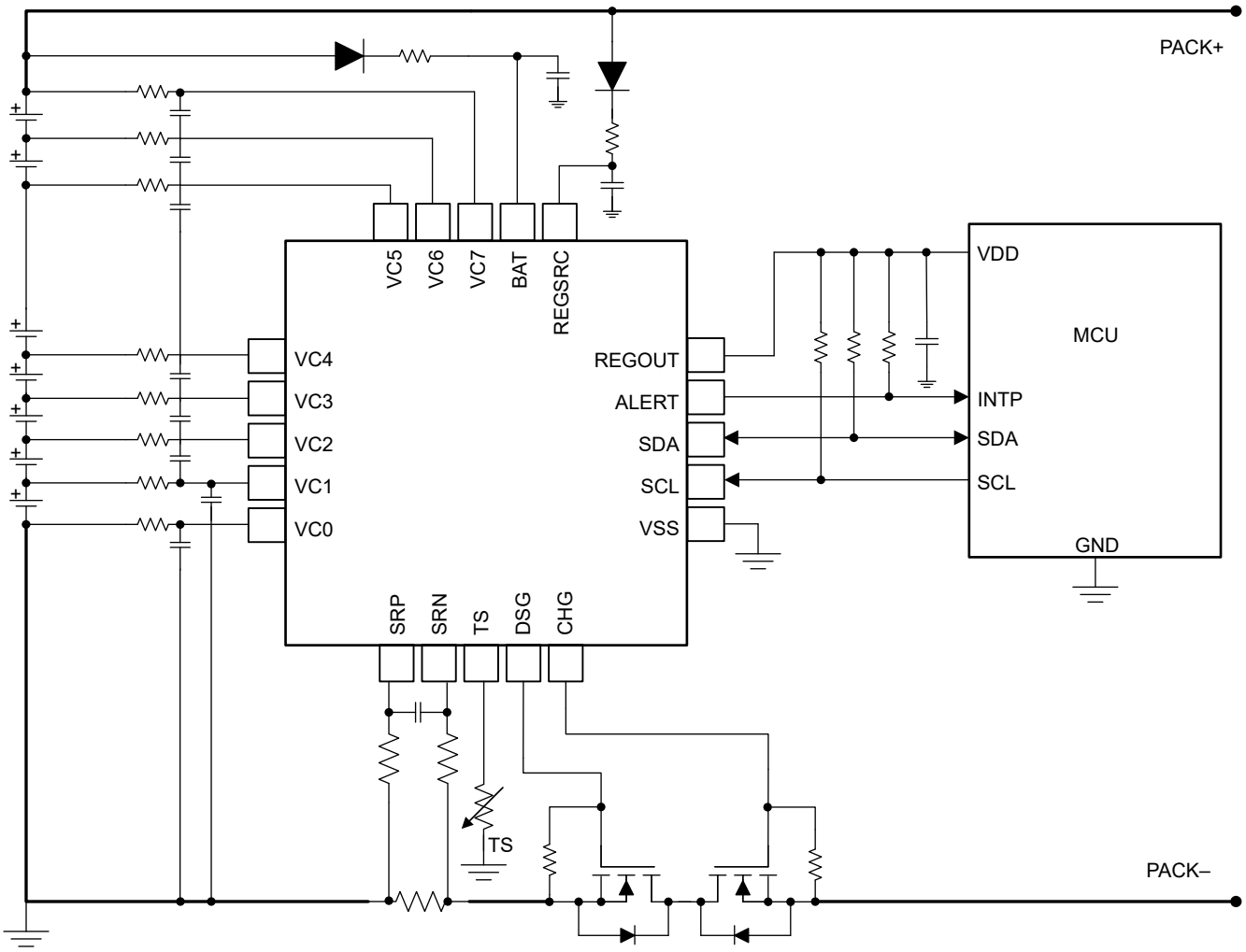


Figure 8-1. BQ78709-Q1 7-Series Cell Typical Implementation (Simplified Schematic)

A full schematic of a basic monitor circuit based on the BQ78709-Q1 for a 7-series battery pack evaluation module is shown below. Section 8.4.2 shows the board layout for this design.

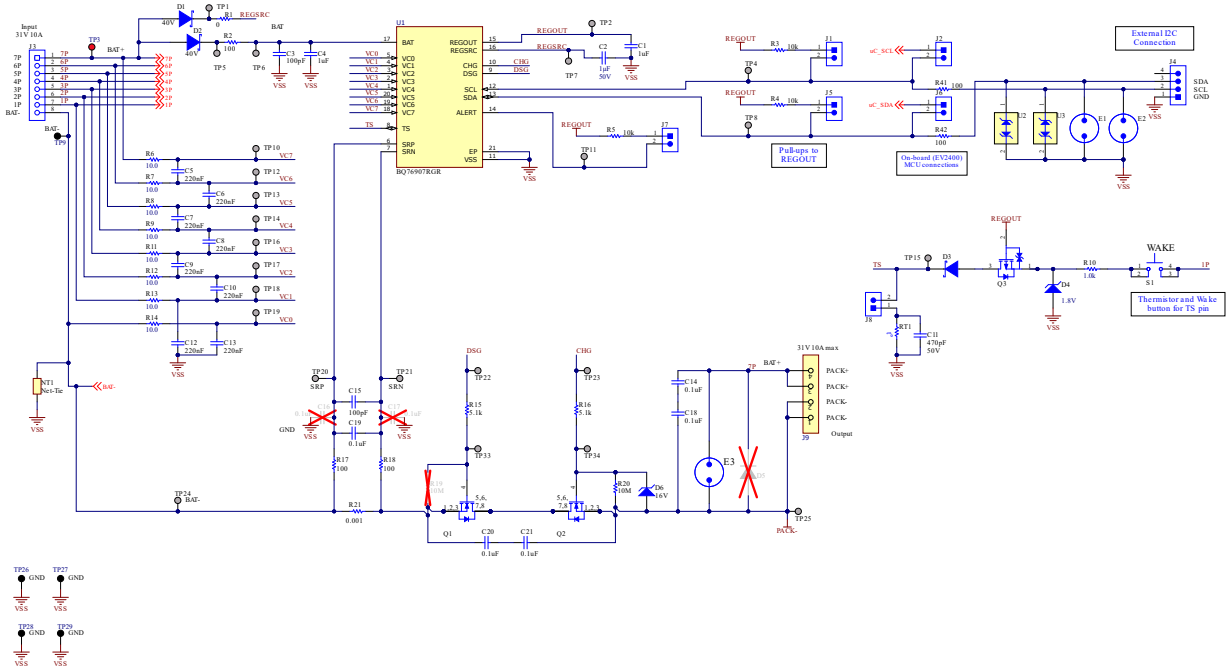


Figure 8-2. BQ78709-Q1 7-Series Cell Schematic Diagram—Monitor

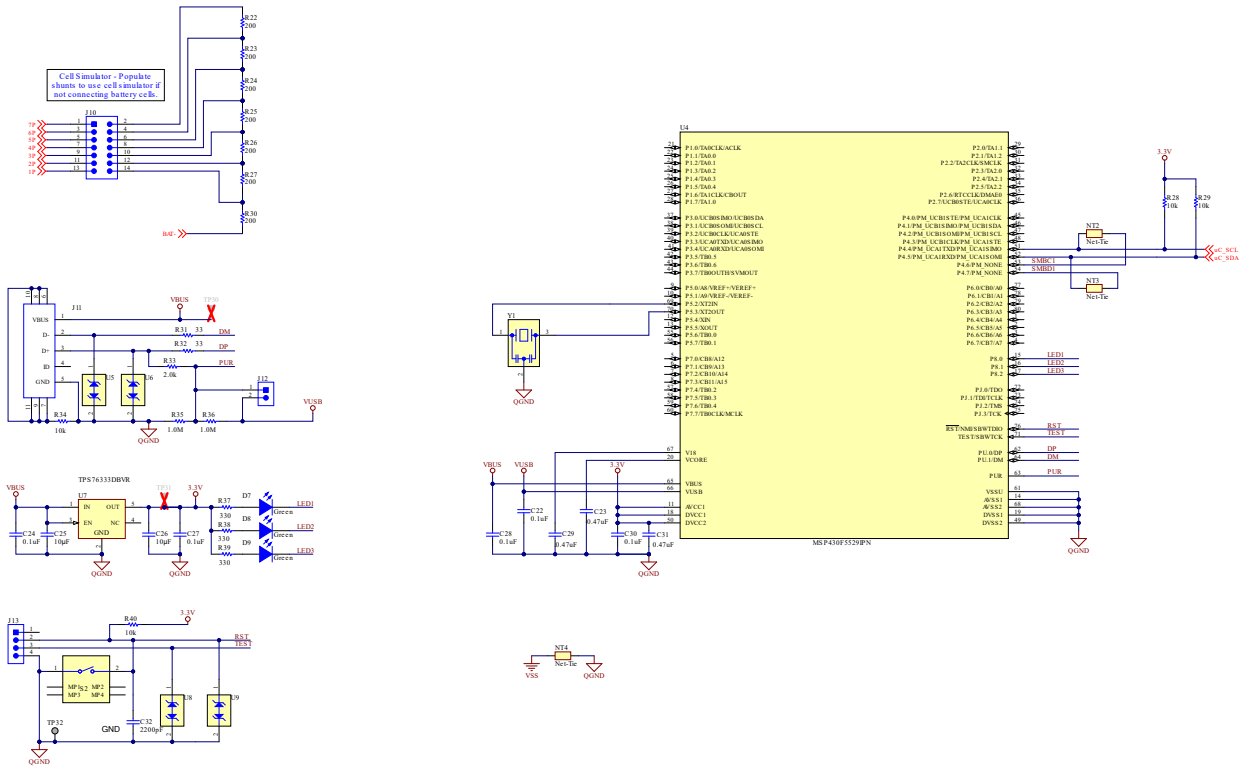


Figure 8-3. BQ78709-Q1 7-Series Cell Schematic Diagram—Additional Circuitry

8.2.1 Design Requirements

Table 8-1. BQ78709-Q1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Minimum system operating voltage	17.5V
Cell minimum operating voltage	2.5V
Series cell count	7
Sense resistor	1mΩ
Thermistor in use	yes
Charge voltage	29.75V
Maximum charge current	6.0A
Peak discharge current	40.0A
Configuration settings	programmed in registers during customer production
Measurement speed	Set to highest resolution (2.93ms per measurement)
Protection subsystem configuration	Series FET configuration, device monitors, disables FETs upon fault, recovers autonomously
OV protection threshold	4.30V
OV protection delay	375ms (16 ADSCAN cycles)
OV protection recovery hysteresis	100mV
UV protection threshold	2.5V
UV protection delay	141ms (6 ADSCAN cycles)
UV protection recovery hysteresis	100mV
SCD protection threshold	80mV (corresponding to a nominal 80A, based on a 1mΩ sense resistor)

Table 8-1. BQ78709-Q1 Design Requirements (continued)

DESIGN PARAMETER	EXAMPLE VALUE
SCD protection delay	45 to 60µs
OCD1 protection threshold	68mV (corresponding to a nominal 68A, based on a 1mΩ sense resistor)
OCD1 protection delay	10ms
OCD2 protection threshold	56mV (corresponding to a nominal 56A, based on a 1mΩ sense resistor)
OCD2 protection delay	81.1ms
OCC protection threshold	8mV (corresponding to a nominal 8A, based on a 1mΩ sense resistor)
OCC protection delay	159.2ms
OTD protection threshold	Code = 2592 (corresponding to ≅ 60°C)
OTD protection delay	2 seconds (17 FULLSCANs)
OTD protection recovery	Code = 2970 (corresponding to ≅ 55°C) for 2 seconds
OTC protection threshold	Code = 3888 (corresponding to ≅ 45°C)
OTC protection delay	2 seconds (17 FULLSCANs)
OTC protection recovery	Code = 4428 (corresponding to ≅ 40°C) for 2 seconds
UTD protection threshold	Code = 15169 (corresponding to ≅ –20°C)
UTD protection delay	7.97 seconds (68 FULLSCANs)
UTD protection recovery	Code = 13398 (corresponding to ≅ –10°C) for 2 seconds
UTC protection threshold	Code = 11319 (corresponding to ≅ 0°C)
UTC protection delay	5.04 seconds (43 FULLSCANs)
UTC protection recovery	Code = 10318 (corresponding to ≅ 5°C) for 2 seconds
Host watchdog timeout protection delay	5 seconds
ALERT pin functionality	Used for alarm interrupt function
REGOUT LDO Usage	Enabled with 3.3V output

8.2.2 Detailed Design Procedure

- Determine the number of series cells
  - This value depends on the cell chemistry and the load requirements of the system. For example, to support a minimum battery voltage of 18V using Li-CO_2 type cells with a cell minimum voltage of 3V, at least 6-series cells are required.
  - For the correct cell connections, see Usage of Unused Pins.
- Protection FET selection and configuration
  - The BQ78709-Q1 device is designed for use with low-side NFET protection.
  - The configuration must be selected for series versus parallel FETs, which may lead to different FET selections for charge versus discharge direction.
  - These FETs must be rated for the maximum:
    - Voltage, which must be approximately 5V (DC) to 10V (peak) per series cell.
    - Current, which must be calculated based on both the maximum DC current and the maximum transient current with some margin.
    - Power dissipation, which can be a factor of the RDS(ON) rating of the FET, the FET package, and the PCB design.
- Sense resistor selection
  - The resistance value must be selected to maximize the input range of the coulomb counter but not exceed the absolute maximum ratings, and avoid excessive heat generation within the resistor.
    - Using the normal maximum charge or discharge current, the sense resistor = 200mV / 40.0A = 5mΩ maximum.
    - Considering a short circuit discharge current of 80A, the recommended maximum SRP, SRN voltage of ≈0.75V, and the maximum SCD threshold of 500mV, the sense resistor must be below 500mV / 80A= 6.25mΩ maximum.

  - Further tolerance analysis (value tolerance, temperature variation, and so on) and PCB design margin should also be considered, so a sense resistor of 1mΩ is suitable with a 50ppm temperature coefficient and power rating of 1W.
- The REGOUT is selected to provide the supply for an external host processor and the pullup supply for the I^2C bus and ALERT pin, with output voltage selected for 3.3V.
  - A 1µF or larger capacitor must be placed at the REGOUT pin.
  - The REGOUT draws its input current from the REGSRC pin. This pin is connected to PACK+ through a series diode and 10Ω resistor, with a 1µF capacitor to VSS placed at the REGSRC pin.

8.2.3 Application Performance Plot

The scope plot below shows the response of the device to a short circuit in discharge (SCD) event and subsequent protection. The device was configured with SCD threshold = 10mV and SCD delay of 0µs to 15µs. A short circuit was applied through a 1mΩ sense resistor. The input filter network on the SRP and SRN pins consisted of 100Ω resistors and a 100nF differential capacitor, which results in a 20µs time constant. The *[SSA]* bit in *Alarm Status()* causes the ALERT pin to fall, which occurs between approximately 15µs and 30µs after the safety status is triggered and the DSG driver is disabled. The circuit included a 5.1kΩ resistor between the DSG pin and the DSG FET gate.

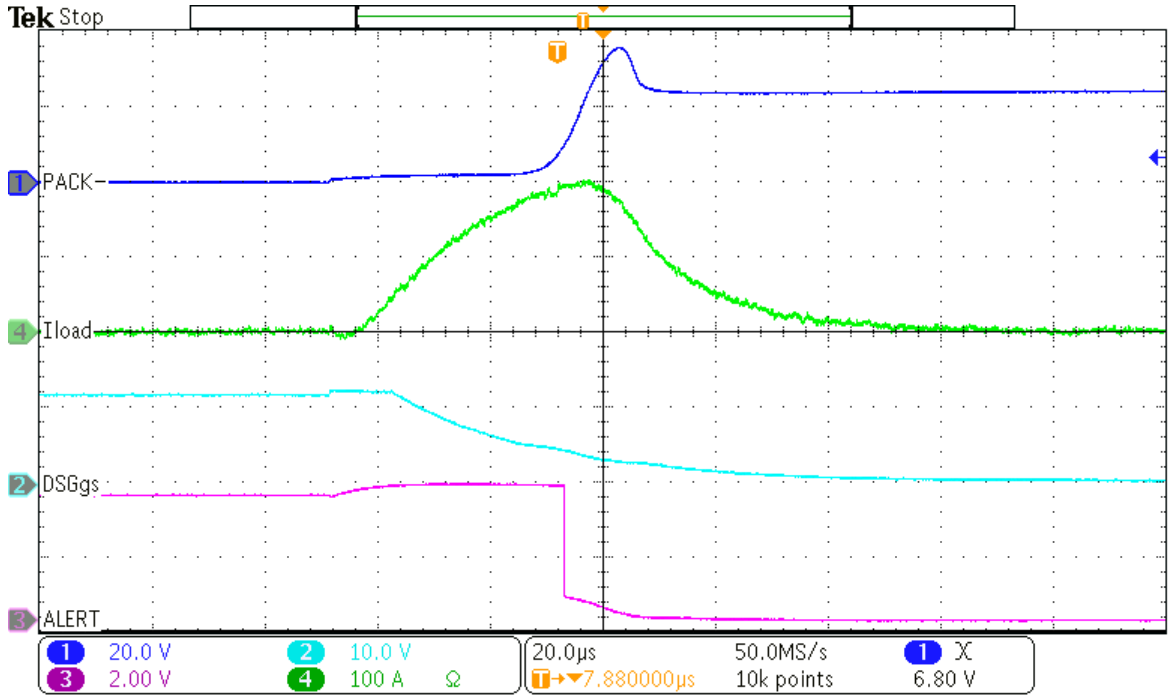


Figure 8-4. Scope plot of SCD event and protection. Load current measured directly at the SRN-SRP pins, which includes an RC delay versus the voltage at the sense resistor.

8.2.4 Random Cell Connection Support

The BQ78709-Q1 device supports a random connection sequence of cells to the device during pack manufacturing. For example, cell-6 in a 7-cell stack might be first connected at the input terminals leading to pins VC6 and VC5, then cell-2 can be connected at the input terminals leading to pins VC2 and VC1, and so on. It is not necessary to connect the negative terminal of cell-1 first at VC0. As another example, consider a cell stack that is already assembled and cells already interconnected to each other, then the stack is connected to the PCB through a connector, which is plugged or soldered to the PCB. In this case, the sequence order in which the connections are made to the PCB can be random in time, they do not need to be controlled in a certain sequence.

There are some restrictions to how the cells are connected during manufacturing:

- To avoid misunderstanding, note that the cells in a stack cannot be randomly connected to any VC pin on the device, such as the lowest cell (cell-1) connected to VC7, while the top cell (cell-7) is connected to VC1, and so on. It is important that the cells in the stack be connected in ascending pin order, with the lowest cell (cell-1) connected between VC1 and VC0, the next higher voltage cell (cell-2) connected between VC2 and VC1, and so on.
- The random cell connection support is possible due to high-voltage tolerance on pins VC1–VC7.

Note

VC0 has a lower voltage tolerance. This is because VC0 must be connected through the series-cell input resistor to the VSS pin on the PCB, before any cells are attached to the PCB. Thus, the VC0 pin voltage is expected to remain close to the VSS pin voltage during cell attach. If VC0 is not connected through the series resistor to VSS on the PCB, then cells cannot be connected in random sequence.

- Each of the VC1–VC7 pins includes a diode between the pin and the adjacent lower cell input pin (that is, between VC7 and VC6, between VC6 and VC5, and so on), which is reverse biased in normal operation. This means an upper cell input pin must not be driven to a low voltage while a lower cell input pin is driven to a higher voltage, since this would forward bias these diodes. During cell attach, the cell input terminals should generally be floating before they are connected to the appropriate cell. It is expected that transient current will flow briefly when each cell is attached, but the cell voltages will quickly stabilize to a state without DC current flowing through the diodes. However, if a large capacitance is included between a cell input pin and another terminal (such as VSS or another cell input pin), the transient current can become excessive and lead to device heating. Therefore, it is recommended to limit capacitances applied at each cell input pin to the values recommended in the specifications.

8.2.5 Startup Timing

At initial power up of the BQ78709-Q1 device from a SHUTDOWN state, the device progresses through a sequence of events before entering NORMAL mode operation. These are described in Table 8-2 for an example configuration, with approximate timing shown.

Table 8-2. Startup Sequence and Timing

STEP	COMMENT	APPROXIMATE TIME (relative to wakeup event)
Wakeup event	Either the TS pin or the VC0 pin is pulled up, triggering the device to exit SHUTDOWN mode.	0
REGOUT powered	Measured with the OTP programmed to autonomously power the REGOUT LDO.	2.6ms
First Cell-1 measurement completed	Data from first measurement of Cell-1 can be read back.	3.2ms

Table 8-2. Startup Sequence and Timing (continued)

STEP	COMMENT	APPROXIMATE TIME (relative to wakeup event)
INITCOMP, ADSCAN, and FULLSCAN asserted (7s)	These three signals are asserted together when the first startup sequence completes (measured with OTP programmed for them to appear on ALERT). ***[CVADCSPEED1:0]*** = 0x0, ***[IADCSPEED1:0]*** = 0x0, ***[SSADCSPEED1:0]*** = 0x0.	9.4ms
FETs enabled (7s)	Measured with the OTP programmed to autonomously enable FETs. ***[CVADCSPEED1:0]*** = 0x0, ***[IADCSPEED1:0]*** = 0x0, ***[SSADCSPEED1:0]*** = 0x0.	9.4ms
INITCOMP, ADSCAN, and FULLSCAN asserted (5s)	These three signals are asserted together when the first startup sequence completes (measured with OTP programmed for them to appear on ALERT). ***[CVADCSPEED1:0]*** = 0x0, ***[IADCSPEED1:0]*** = 0x0, ***[SSADCSPEED1:0]*** = 0x0.	8.6ms
FETs enabled (5s)	Measured with the OTP programmed to autonomously enable FETs. ***[CVADCSPEED1:0]*** = 0x0, ***[IADCSPEED1:0]*** = 0x0, ***[SSADCSPEED1:0]*** = 0x0.	8.6ms

Figure 8-5 shows an example of an oscilloscope plot of a startup sequence with the device configured in OTP for a 5s pack, with ***[FET_EN]*** = 1 for autonomous FET control and providing the *[INITCOMP]* flag on the ALERT pin. The TS pin is pulled up to initiate device wakeup from SHUTDOWN.

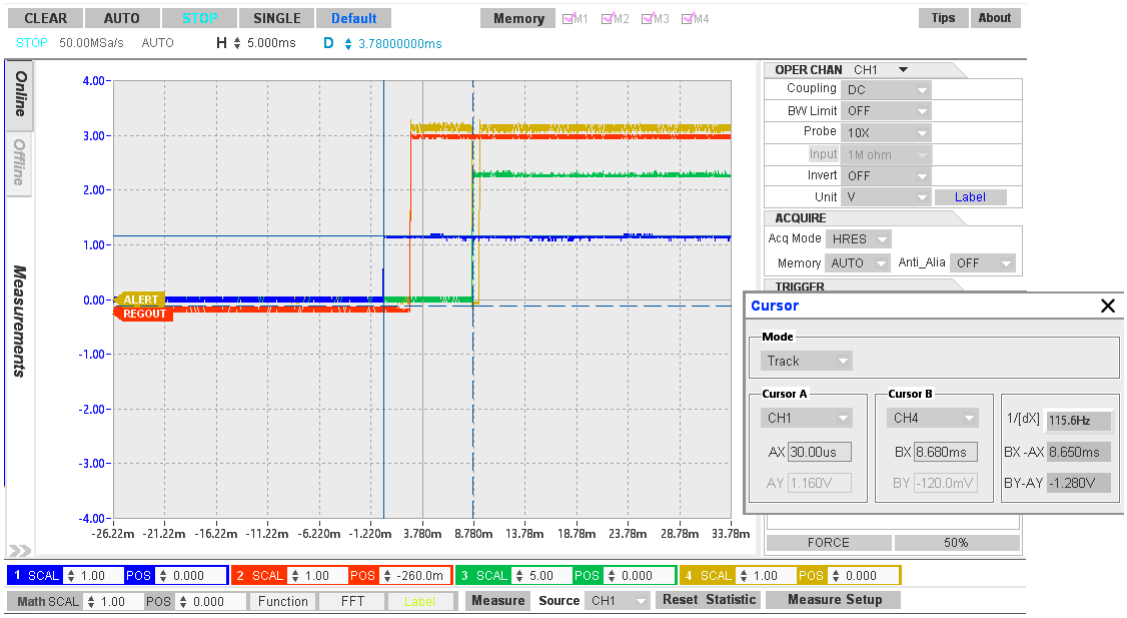


Figure 8-5. Startup Sequence for 5s Pack with the *[INITCOMP]* Flag Displayed on the ALERT Pin (TS Pin Voltage in Blue, DSG Pin Voltage Shown in Green)

8.2.6 FET Driver Turn-Off

The low-side CHG and DSG FET drivers operate differently when they are triggered to turn off their respective FET. The DSG driver includes an internal switch that drives the DSG pin toward the VSS pin level when the

driver is disabled. The driver is specified with a maximum fall time into a 20nF capacitive load, with 100Ω series resistance between the DSG pin and the DSG gate. If the driver is used with a larger capacitive load, the fall time generally increases. The system designer can optimize the series resistance value based on the board components and DSG FET(s) used.

The external series gate resistor between the DSG pin and the DSG FET gate is used to adjust the speed of the turn-off transient. A low resistance (such as 100Ω) will provide a fast turn-off during a short circuit event, but this may result in an overly large inductive spike at the top of the stack when the FET is disabled. A larger resistor value (such as 1kΩ or 4.7kΩ) reduces this speed and the corresponding inductive spike level.

The CHG FET driver will discharge the CHG pin toward the VSS pin level, but it includes an additional series PFET to support voltages below VSS. This is generally needed when a pack is heavily discharged, for example, if cells in a 7-series pack are at 2.5V per cell, PACK+ = 17.5V relative to the device VSS. Then if a charger is attached while the CHG FET is disabled and applies a full charge voltage across PACK+ relative to PACK–, such as 4.3V per cell, or 30.1V for the 7-S pack, this results in PACK– dropping to approximately –12.6V relative to VSS. To keep the CHG FET disabled, its gate voltage must drop to near this –12.6V level.

To support this type of case, the CHG FET driver in BQ78709-Q1 is designed to withstand voltages as low as –25V (recommended) relative to the VSS pin voltage by including a series PFET at the pin, with its gate connected to VSS. When the CHG driver is disabled, the driver will pull the pin voltage downward. As the pin voltage nears VSS, the PFET is disabled, so the pin becomes high impedance. At this point, the external gate-source resistor on the CHG FET will pull the pin voltage lower to the PACK– level, keeping the CHG FET disabled.

Oscilloscope captures of CHG and DSG driver turn-off are shown below, with the pins driving the gates of CSD18532Q5B NFETs, which have a typical C_{iss} of 3900pF. Figure 8-6 shows the signals when using a 1.35kΩ series gate resistor between the DSG pin and the FET gate, and a 2A load connected between PACK+ and PACK–.

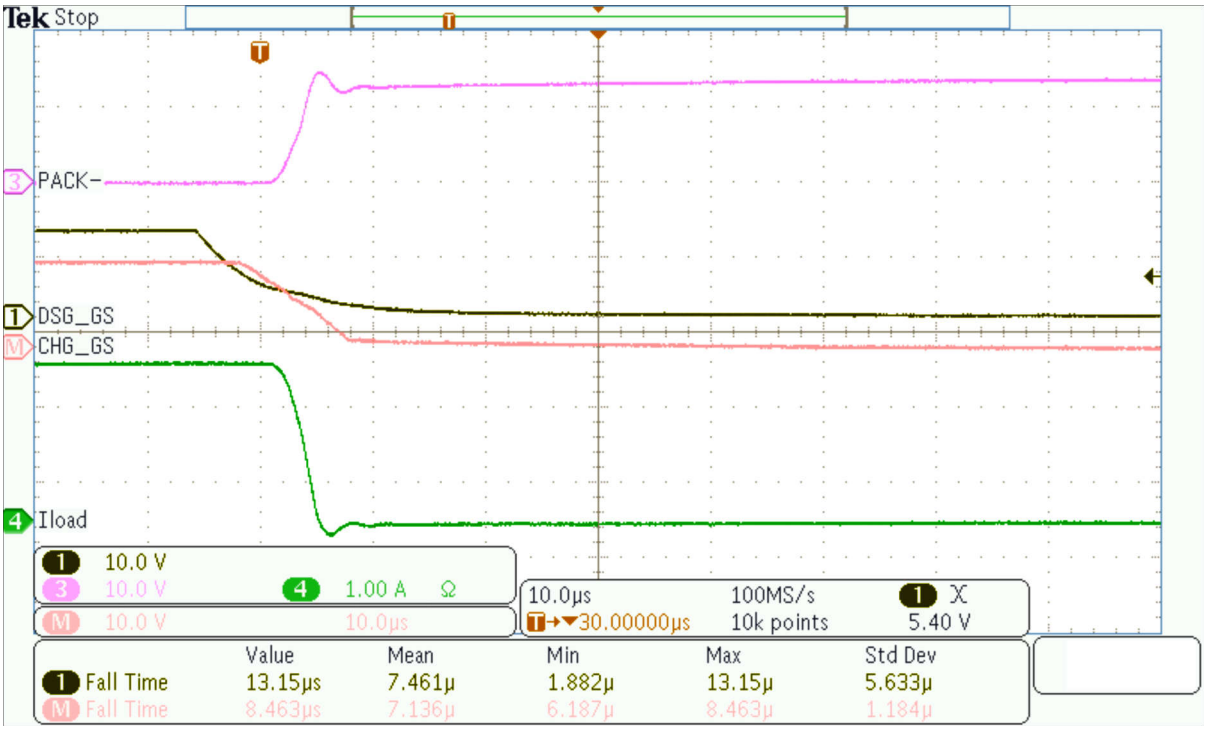


Figure 8-6. Moderate Speed FET Turn-Off, Using a 1.35kΩ Series Gate Resistor, and a 2A Load between PACK+ and PACK–.

A slower turn-off case is shown in Figure 8-7, using a 4.5kΩ series gate resistor, and a 2A load between PACK+ and PACK–.

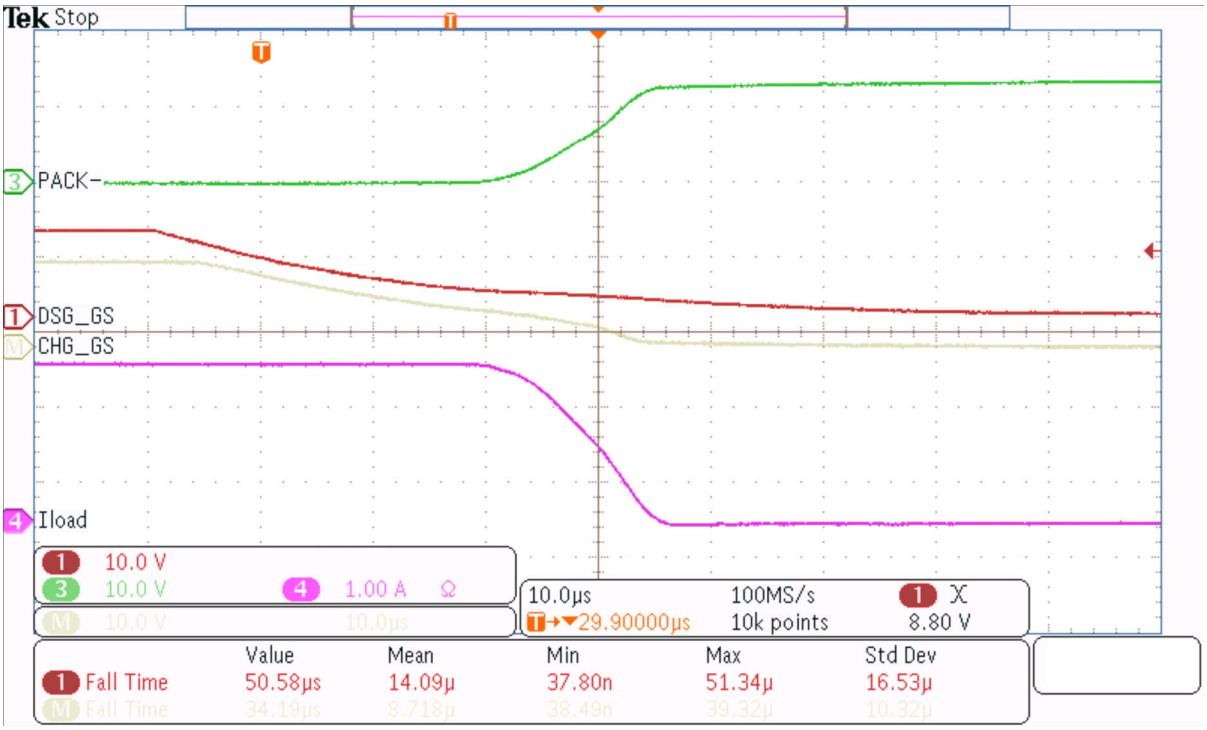


Figure 8-7. A Slower Turn-Off Case Using a 4.5kΩ Series Gate Resistor

A fast turn-off case is shown in Figure 8-8, in which a 100Ω series gate resistor is used between the DSG pin and the FET gate.

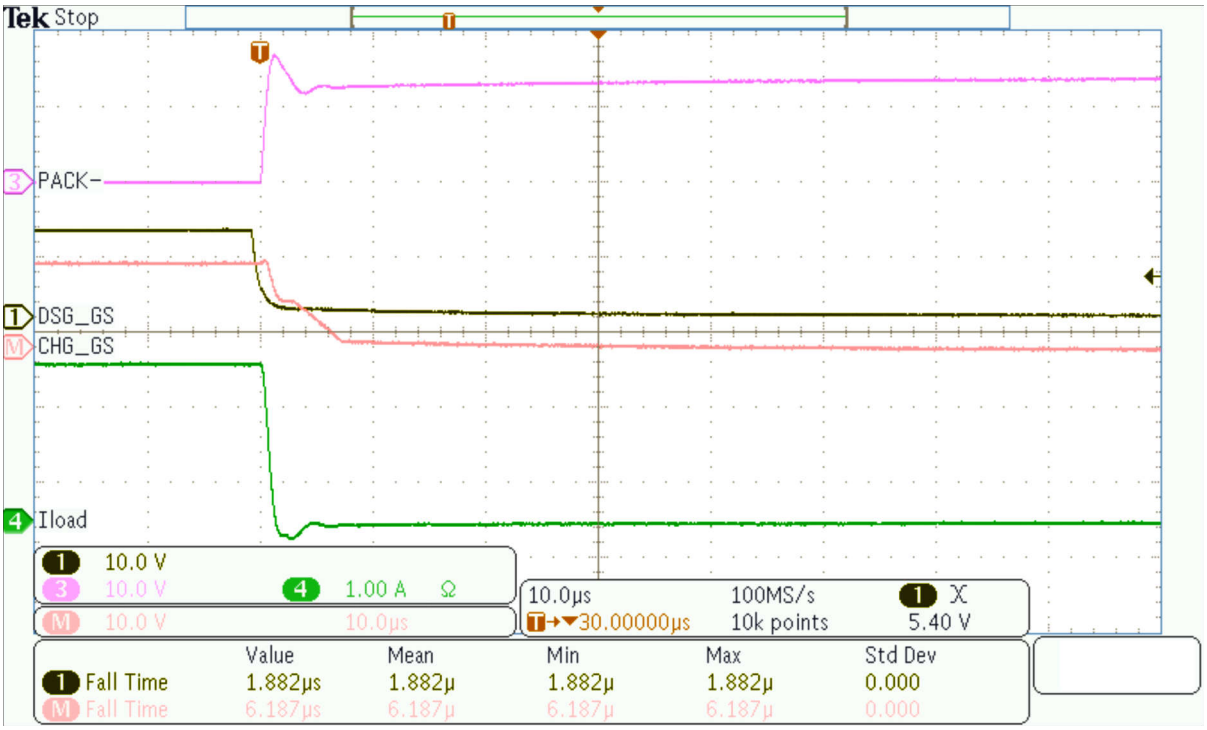


Figure 8-8. A Fast Turn-Off Case with a 100Ω Series Gate Resistor

8.2.7 Usage of Unused Pins

Some device pins may not be needed in a particular application. The manner in which each must be terminated in this case is described below.

Table 8-3. Terminating Unused Pins

Pin	Name	Recommendation
1–5, 18–20	VC0–VC7	Cell inputs 1 and 7 should always be connected to actual cells, with cells connected between VC1 and VC0, and between VC6 and VC7. VC0 must be connected through a resistor and capacitor on the PCB to pin 11 (VSS). Pins related to unused cells (which may be cell 2 – cell 6, pins 1–3, 19, 20) must be shorted directly to an adjacent VC pin. All VC pins must be connected to either an adjacent VC pin or an actual cell (through R and C).
6, 7	SRP, SRN	If not used, these pins must be connected to pin 11 (VSS).
8	TS	If not used, this pin must be connected to pin 11 (VSS).
9, 10	DSG, CHG	If not used, these pins must be left floating.
12, 13	SCL, SDA	If not used, these pins must be connected to pin 11 (VSS).
14, 15	ALERT, REGOUT	If not used, these pins must be left floating.
16	REGSRC	If neither the REGOUT regulator nor the CHG and DSG drivers are used, this pin must be connected to pin 17 (BAT).

8.3 Power Supply Recommendations

The BQ78709-Q1 device draws its supply current from the BAT pin, which is typically connected to the top of stack point through a series diode, to protect against any fault within the device resulting in unintended charging of the pack. A series resistor and capacitor is included to lowpass filter fast variations on the stack voltage. During a short circuit event, the stack voltage may be momentarily pulled to a very low voltage before the

protection FETs are disabled. In this case, the charge on the BAT pin capacitor will temporarily support the BQ78709-Q1 device's supply current, to avoid the device losing power.

The REGSRC pin serves as the supply voltage for the integrated REGOUT customer regulator and for the CHG and DSG FET drivers. This pin can also be connected to the top of stack through a diode, to similarly allow the voltage to hold up longer during a short circuit event. If a diode or any series resistance (> 1Ω) is included between the top of stack and the REGSRC pin, a minimum 1µF capacitor is recommended to be included at the REGSRC pin to VSS. It is also acceptable to short the REGSRC pin to the BAT pin, such that the same diode and filter circuit can support both pins. However, the load on the REGOUT pin will discharge the BAT capacitor faster in this case and must be considered by the system designer.

8.4 Layout

8.4.1 Layout Guidelines

- The quality of the Kelvin connections at the sense resistor is critical. The sense resistor should have a temperature coefficient no greater than 50ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the BQ78709-Q1 device. Parallel resistors can be used as long as good Kelvin sensing is ensured.
- In reference to the system circuitry, the following features require attention for component placement and layout: differential low-pass filter and I^2C communication.
- The BQ78709-Q1 device uses an integrating delta-sigma coulomb counter ADC for current measurements. For best performance, 100Ω resistors must be included from the sense resistor terminals to the SRP and SRN inputs of the device, with a 0.1µF filter capacitor placed across the SRP and SRN pins. Optional 0.1µF filter capacitors can be added for additional noise filtering at each sense input pin to ground. All filter components must be placed as close as possible to the device, rather than close to the sense resistor, and the traces from the sense resistor routed in parallel to the filter circuit. A ground plane can also be included around the filter network to add additional noise immunity.
- These filter components between the sense resistor and the SRP and SRN terminals provide filtering of noise components, but they also introduce an RC time constant delay, nominally 20µs using the two 100Ω and single differential 0.1µF components. If this delay introduces too much additional time into the response of the device to short circuit events, the filter time constant can be reduced, with the tradeoff of providing less filtering.
- The I^2C clock and data pins have integrated ESD protection circuits; however, adding a Zener diode and series resistor on each pin provides more robust ESD performance.

8.4.2 Layout Example

An example circuit layout using the BQ78709-Q1 device in a 7-series cell design is described below. The design implements the schematic shown in Figure 8-2 and Figure 8-3, and uses a 2.175-inch × 1.400-inch 2-layer circuit card assembly with cell connections on the left edge and pack connections along the bottom edge of the board. Wide trace areas are used, reducing voltage drops on the high current paths.

The board layout, which is shown in Figure 8-9 and Figure 8-10, includes spark gaps with the reference designator prefix *E*. These spark gaps are fabricated with the board and no component is installed.

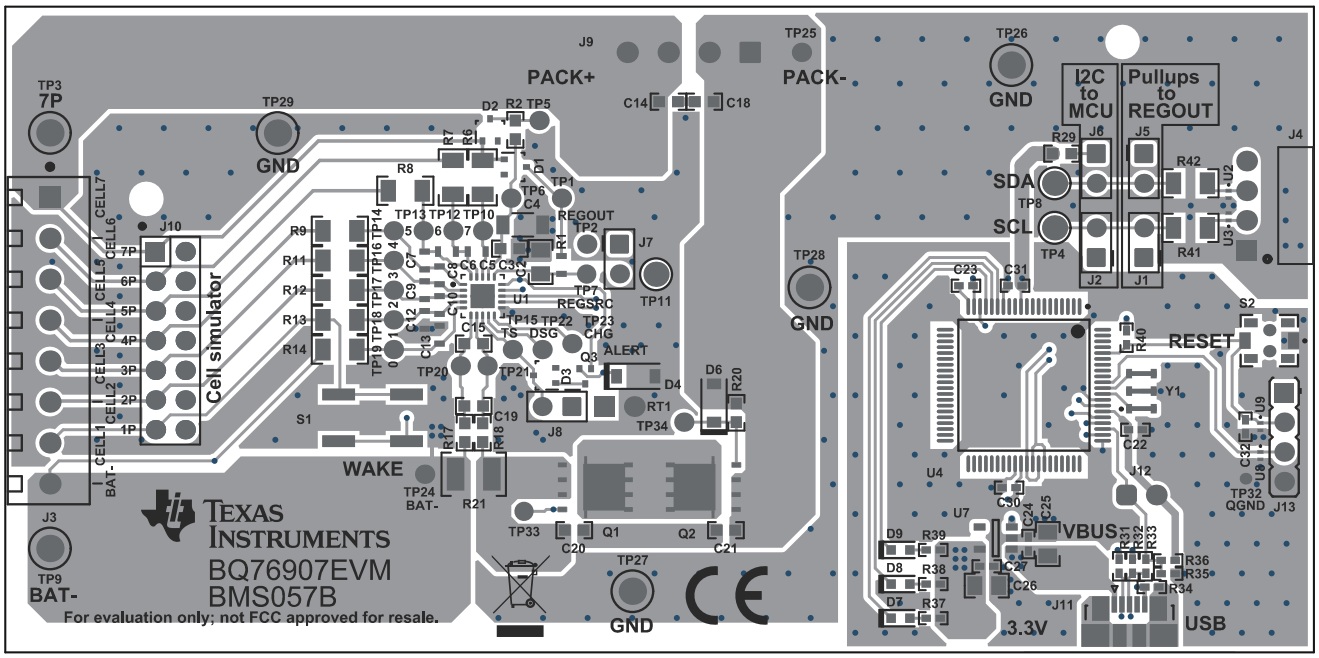


Figure 8-9. BQ78709-Q1 Two-Layer Board Layout—Top Layer

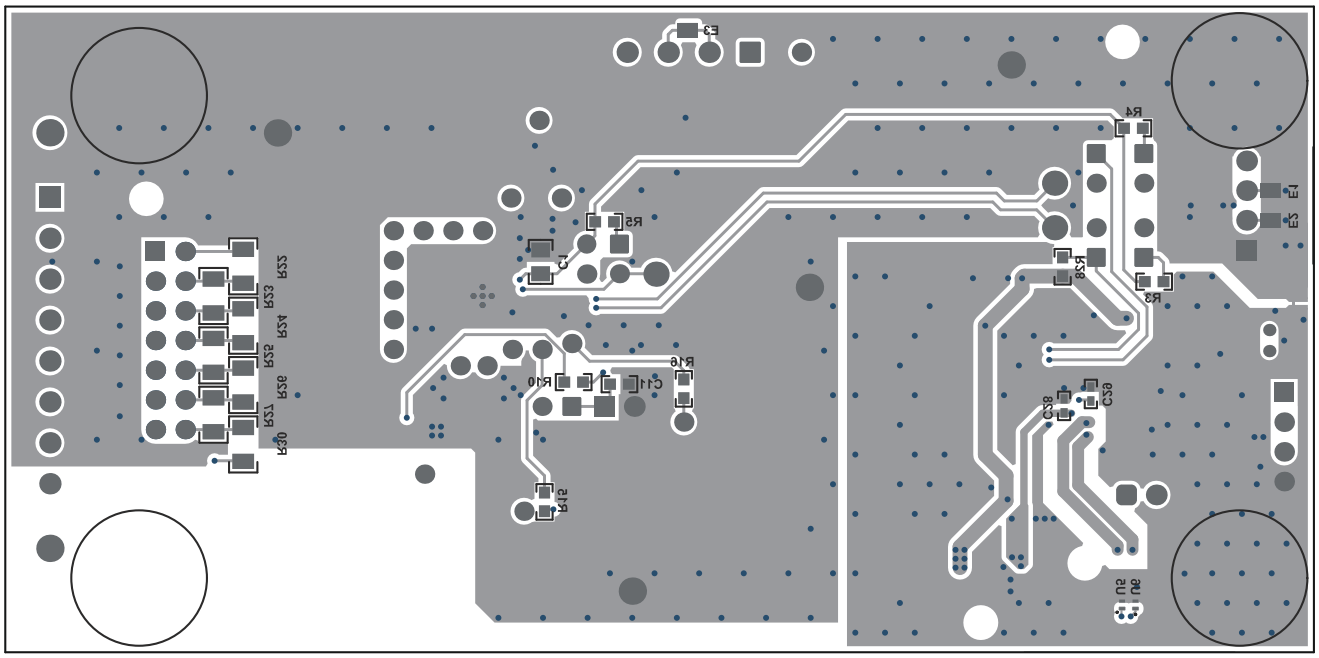


Figure 8-10. BQ78709-Q1 Two-Layer Board Layout—Bottom Layer

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For additional information, see the following related documents:

- Texas Instruments, *BQ76907 Technical Reference Manual*
- Texas Instruments, *BQ76907 Evaluation Module User's Guide*
- Texas Instruments, *Battery Management Studio (bqStudio) Software*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ78709QRGRRQ1	Active	Production	VQFN (RGR) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	709Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

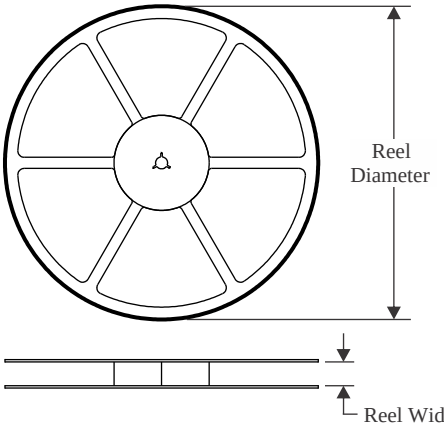
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

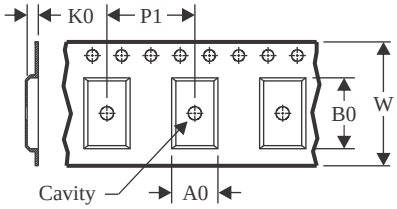
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

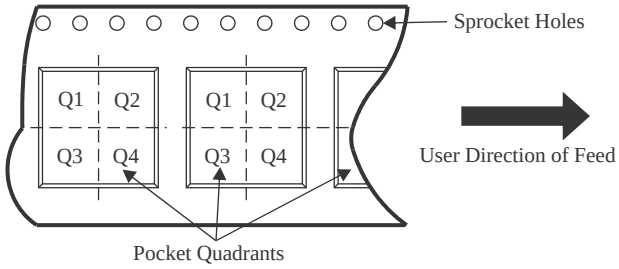


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

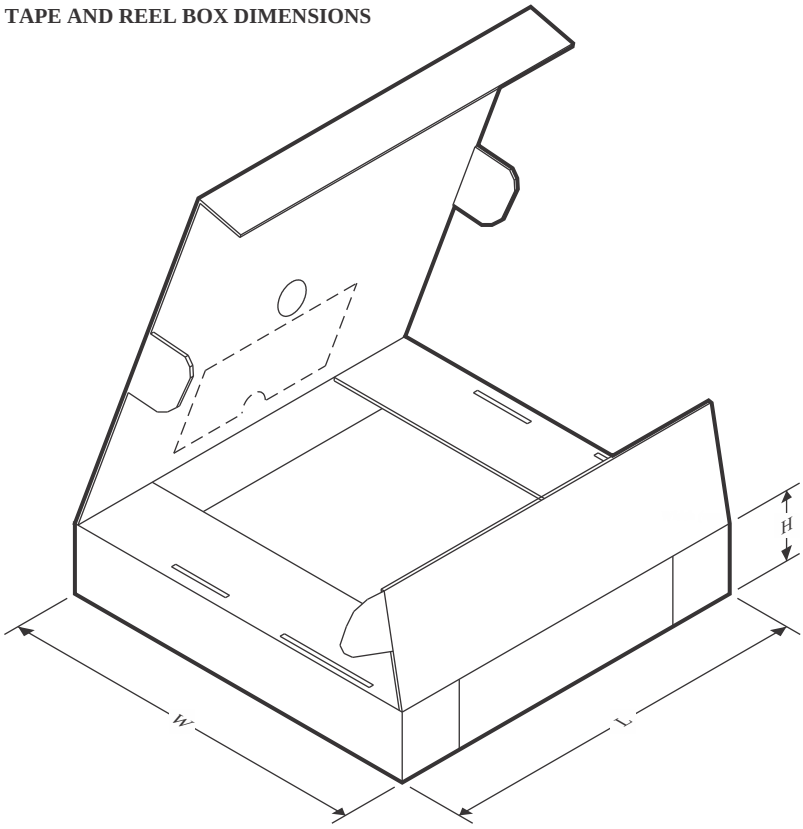
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ78709QRGRRQ1	VQFN	RGR	20	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ78709QRGRRQ1	VQFN	RGR	20	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

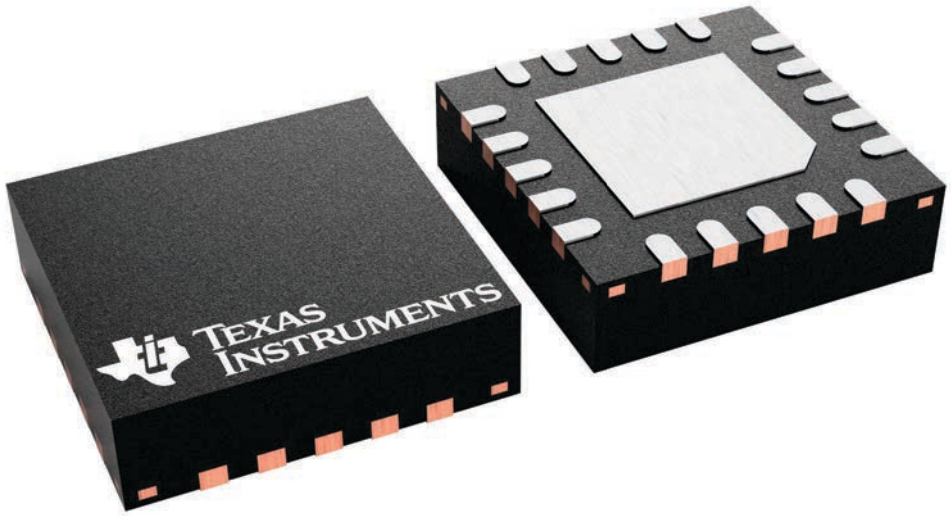
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



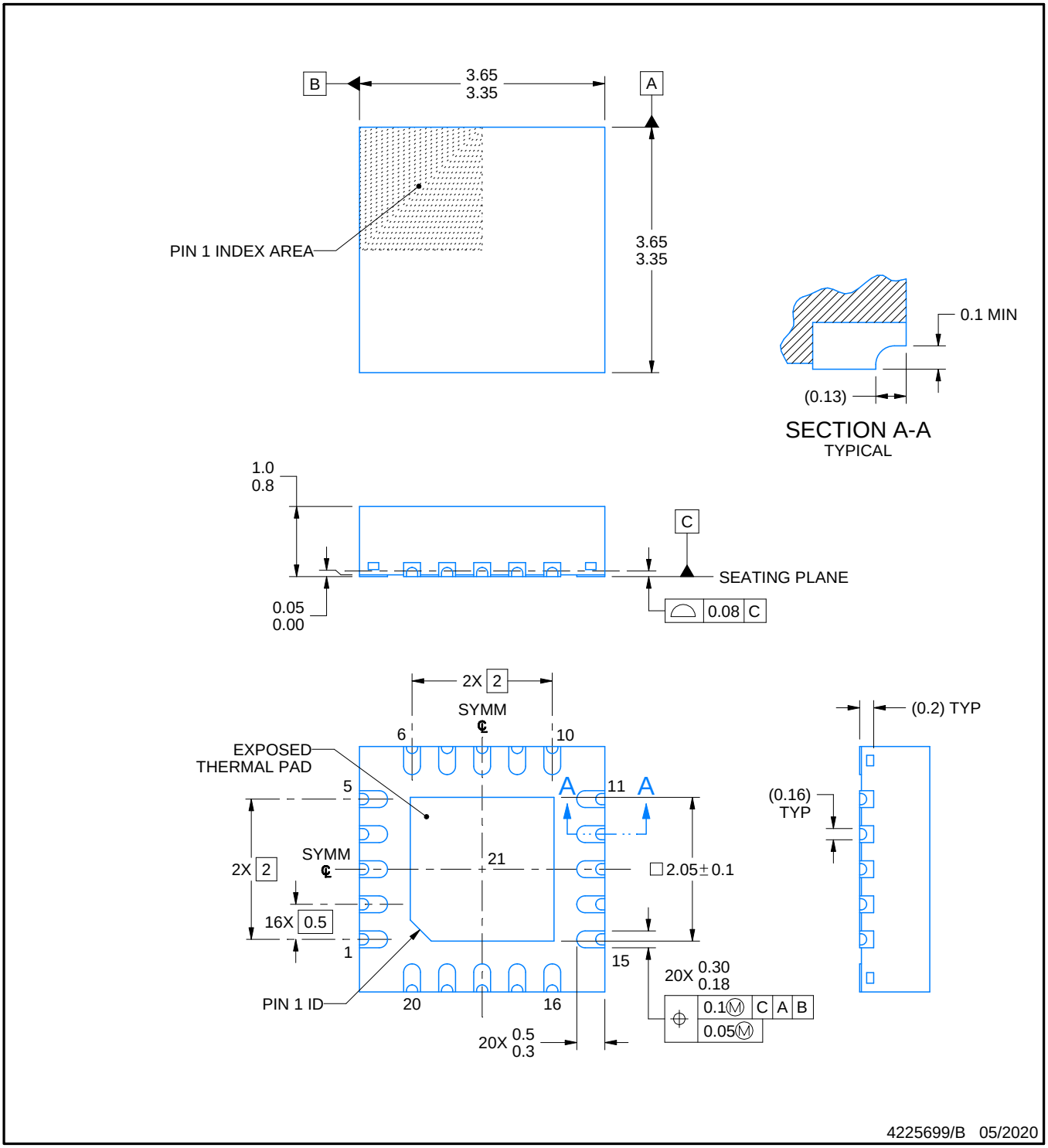
4228482/A

PACKAGE OUTLINE

RGR0020C

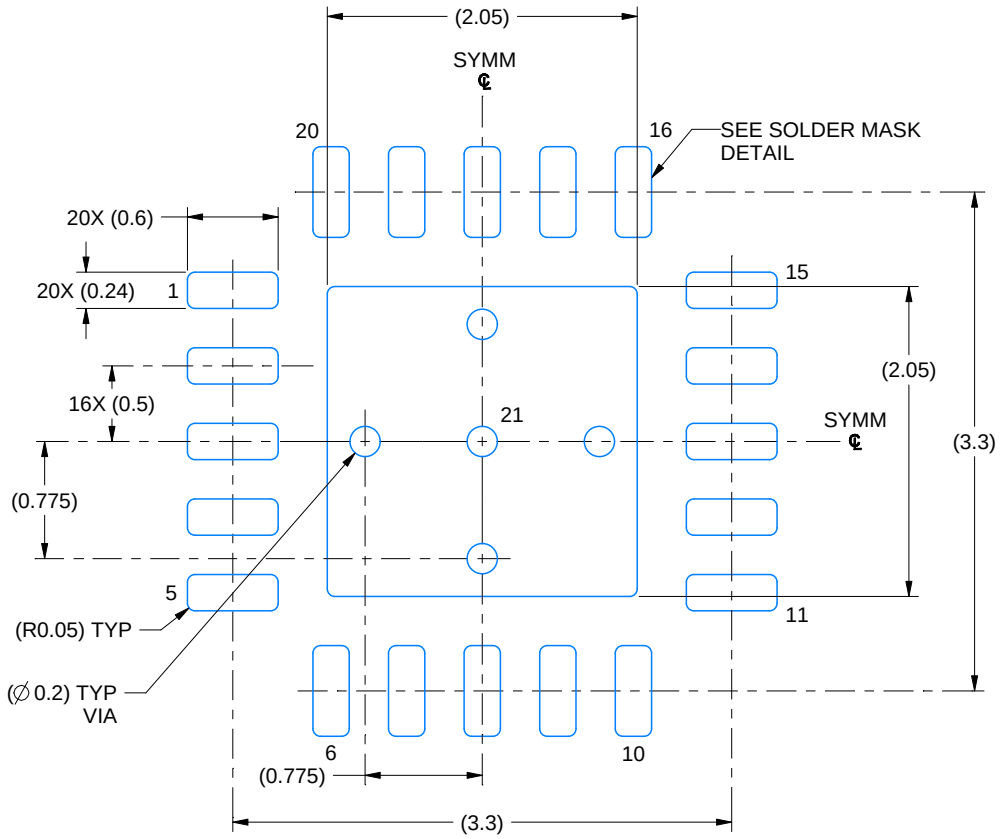
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

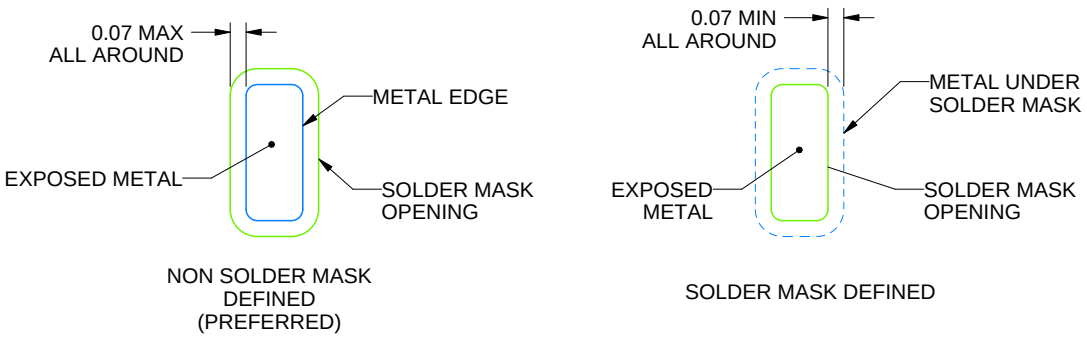


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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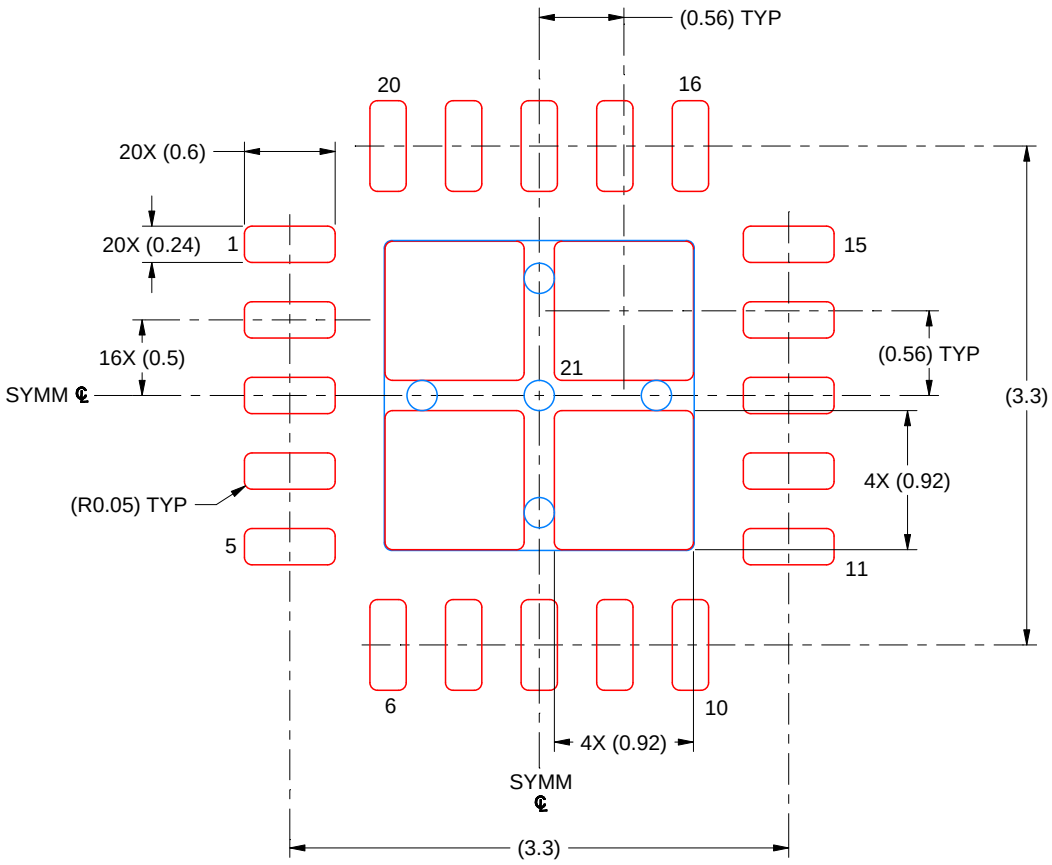
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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