

PowerLAN™ Master Gateway Battery Management Controller With PowerPump™ Cell Balancing Technology

FEATURES

- **bq78PL114** Designed for Managing 3- to 8-Series-Cell Battery Systems
- **bq78PL114S12** Firmware Upgrade Supports 3- to 12-Series-Cell Battery Systems
 - Adds Support for LCD and Electronic Paper Displays or EPDs
 - Configurable for 11-A, 26-A, or 110-A Operating Currents
- Systems With More Than Four Series Cells Require External **bq76PL102** Dual-Cell Monitors
- SmartSafety Features:
 - Prevention: Optimal Cell Management
 - Diagnosis: Improved Sensing of Cell Problems
 - Fail Safe: Detection of Event Precursors
- Rate-of-Change Detection of All Important Cell Characteristics:
 - Voltage
 - Impedance
 - Cell Temperature
- PowerPump Technology Transfers Charge Efficiently From Cell to Cell During All Operating Conditions, Resulting in Longer Run Time and Cell Life
 - **bq78PL114S12** Adds User-Configurable PowerPump Cell-Balancing Modes
- High-Resolution 18-Bit Integrating Delta-Sigma Coulomb Counter for Precise Charge-Flow Measurements and Gas Gauging
- Multiple Independent Δ - Σ ADCs: One-per-Cell Voltage, Plus Separate Temperature, Current, and Safety
- Simultaneous, Synchronous Measurement of Pack Current and Individual Cell Voltages
- Very Low Power Consumption
 - **bq78PL114**: < 250 μ A Active, < 150 μ A Standby, < 40 μ A Ship, and < 1 μ A Undervoltage Shutdown

- **bq78PL114S12**: < 300 μ A Active, < 185 μ A Standby, < 85 μ A Ship, and < 1 μ A Undervoltage Shutdown
- Accurate, Advanced Temperature Monitoring of Cells and MOSFETs With up to 12 Sensors
- Fail-Safe Operation of Pack Protection Circuits: Up to Three Power MOSFETs and One Secondary Safety Output (Fuse)
- Fully Programmable Voltage, Current, Balance, and Temperature-Protection Features
- External Inputs for Auxiliary MOSFET Control
- Smart Battery System 1.1 Compliant via SMBus

APPLICATIONS

- Portable Medical Instruments and Test Equipment
- Mobility Devices (E-Bike)
- Uninterruptible Power Supplies and Hand-Held Tools

DESCRIPTION

The **bq78PL114** master gateway battery controller is part of a complete Li-Ion control, monitoring, and safety solution designed for large series cell strings.

The **bq78PL114** and **bq78PL114S12** along with **bq76PL102** PowerLAN™ dual-cell monitors provide complete battery-system control, communications, and safety functions for a structure of three up to twelve series cells. This PowerLAN system provides simultaneous, synchronized voltage and current measurements using one A/D per-cell technology. This eliminates system-induced noise from measurements and allows the precise, continuous, real-time calculation of cell impedance under all operating conditions, even during widely fluctuating load conditions.

PowerPump technology transfers charge between cells to balance their voltage and capacity. Balancing is possible during all battery modes: charge, discharge, and rest. Highly efficient charge-transfer circuitry nearly eliminates energy loss while providing true real-time balance between cells, resulting in longer run-time and improved cycle life.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

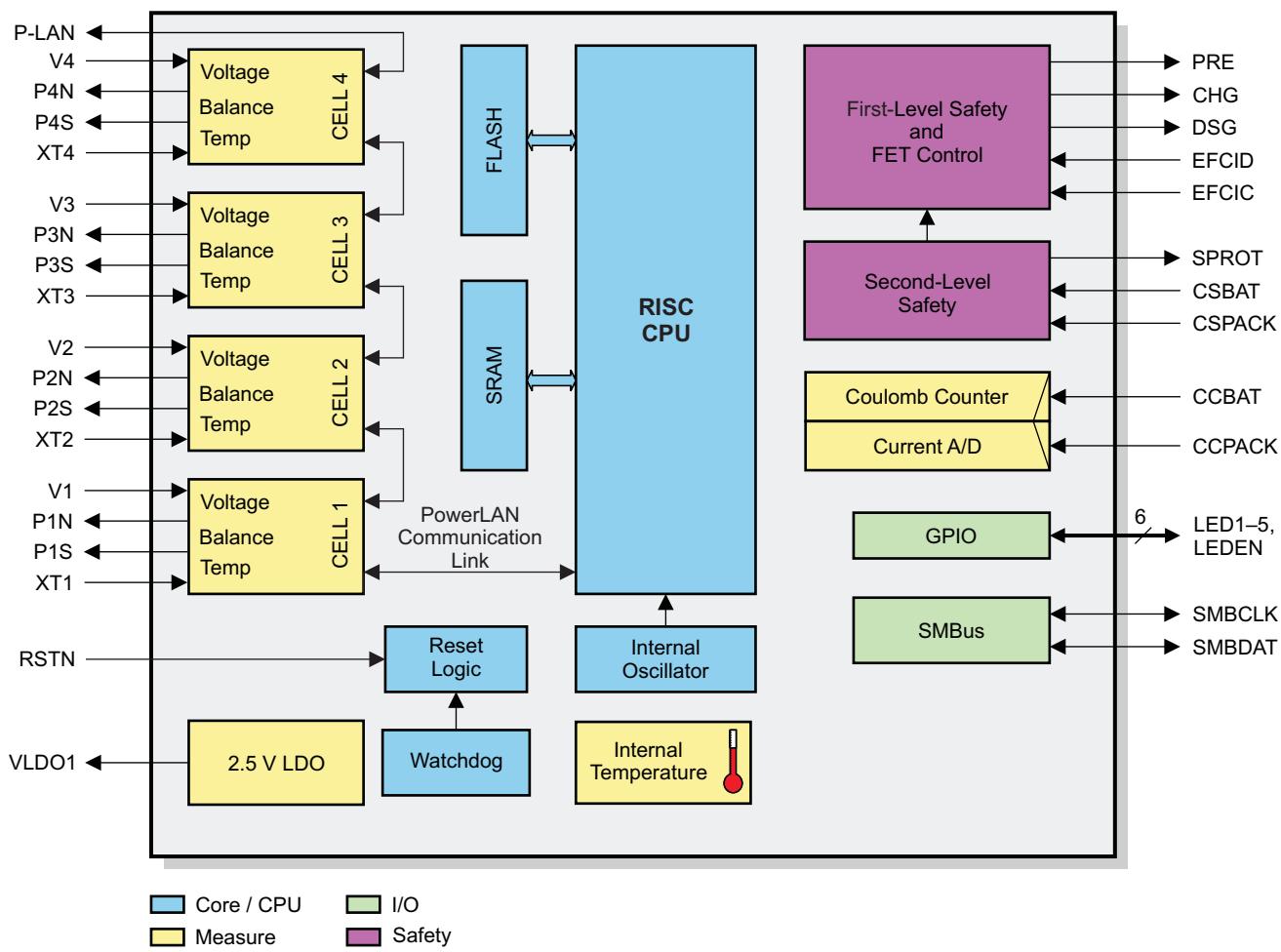
Temperature is sensed by up to 12 external sensors and one on-chip sensor. This permits accurate temperature monitoring of each cell individually. Firmware is then able to compensate for the temperature-induced effects on capacity, impedance, and OCV on a cell-by-cell basis, resulting in superior charge/ discharge and balancing control.

External MOSFET control inputs provide user- definable direct hardware control over MOSFET states. Smart control prevents excessive current through MOSFET body diodes. Auxiliary inputs can be used for enhanced safety and control in large multicell arrays.

The bq78PL114 is completely user-configurable, with parametric tables in flash memory to suit a variety of cell chemistries, operating conditions, safety controls, and data reporting needs. It is easily configured using the supplied bqWizard™ graphical user interface (GUI). The device is fully programmed and requires no algorithm or firmware development.

The bq78PL114 can be upgraded to the bq78PL114S12 by downloading the bq78PL114S12 firmware. The firmware can be downloaded using the bqWizard application or during manufacturing. Upgrading to the bq78PL114S12 changes the functionality of the LED1–LED5, LEDEN, and N/C pin #29. The bq78PL114S12 pin functions of LED1/SEG1–LED5/SEG5, PSH/BP/TP, and FIELD support LED, LCD, and electronic paper displays (EPDs). The user can configure the bq78PL114S12 for the desired display type.

In this document all descriptions for the bq78PL114 apply to the bq78PL114S12 except where different bq78PL114S12 functionality is specifically described.



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Figure 1. bq78PL114 Internal Block Diagram

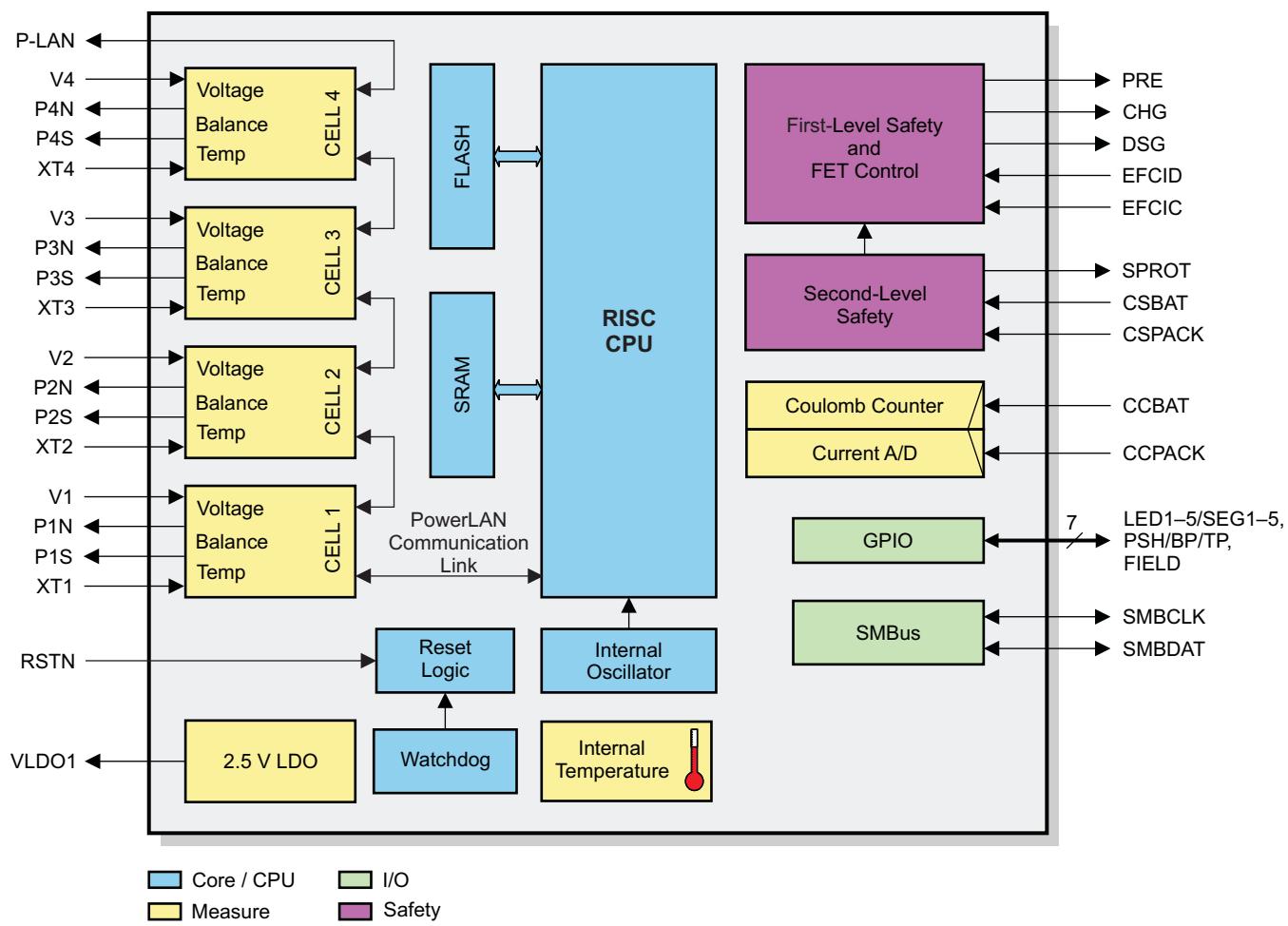


Figure 2. bq78PL114S12 Internal Block Diagram

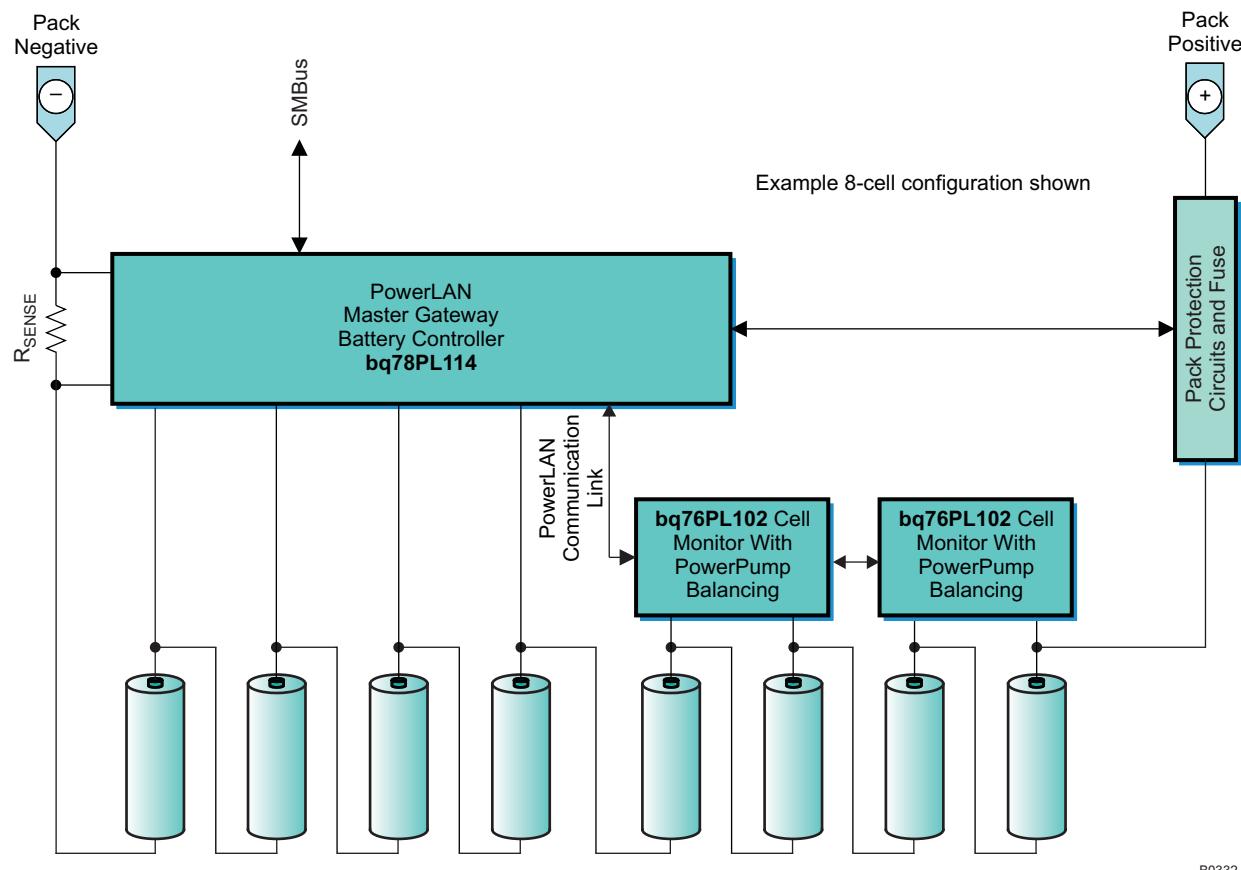


Figure 3. Example bq78PL114 PowerLAN Multicell System Implementation (8 Cells)

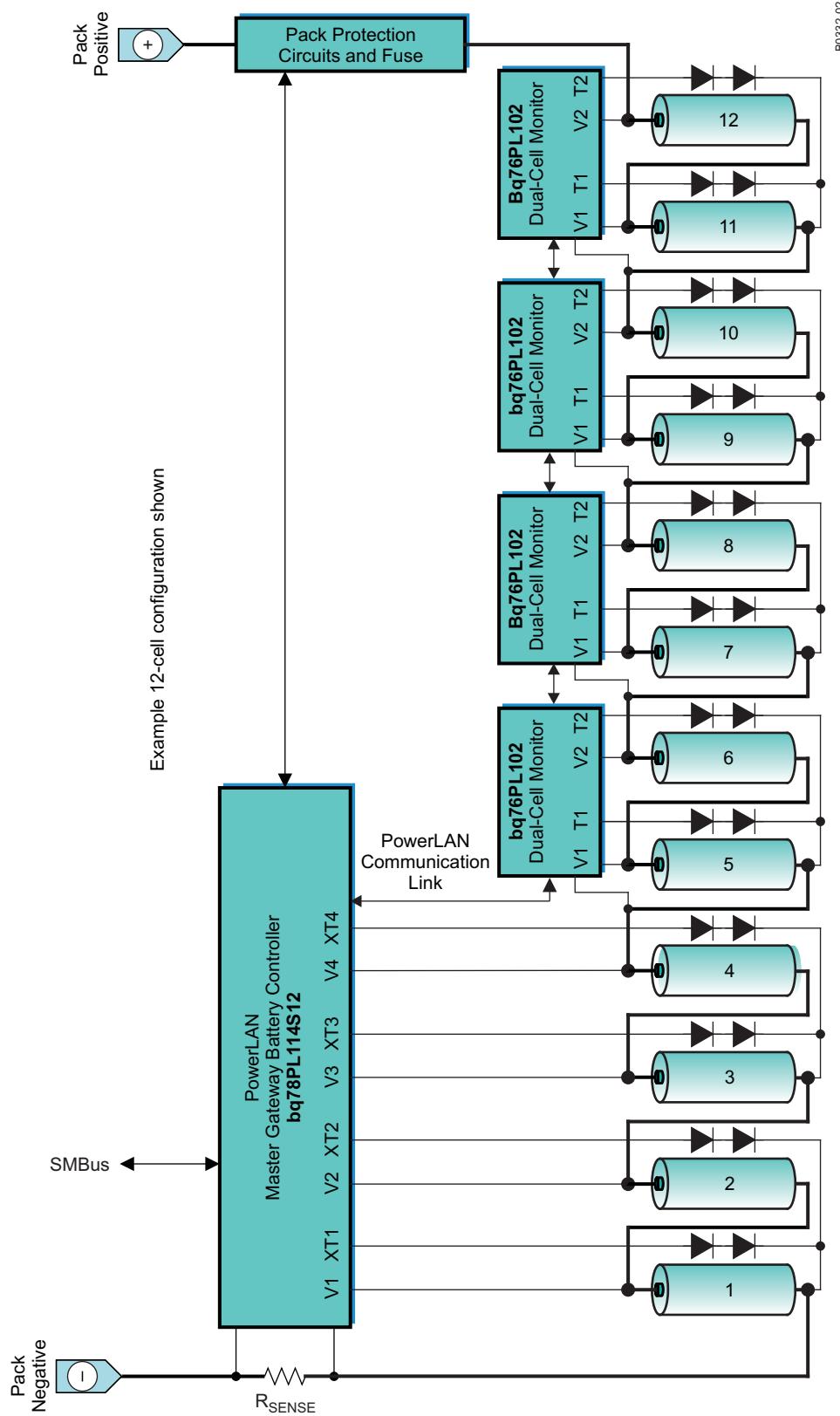
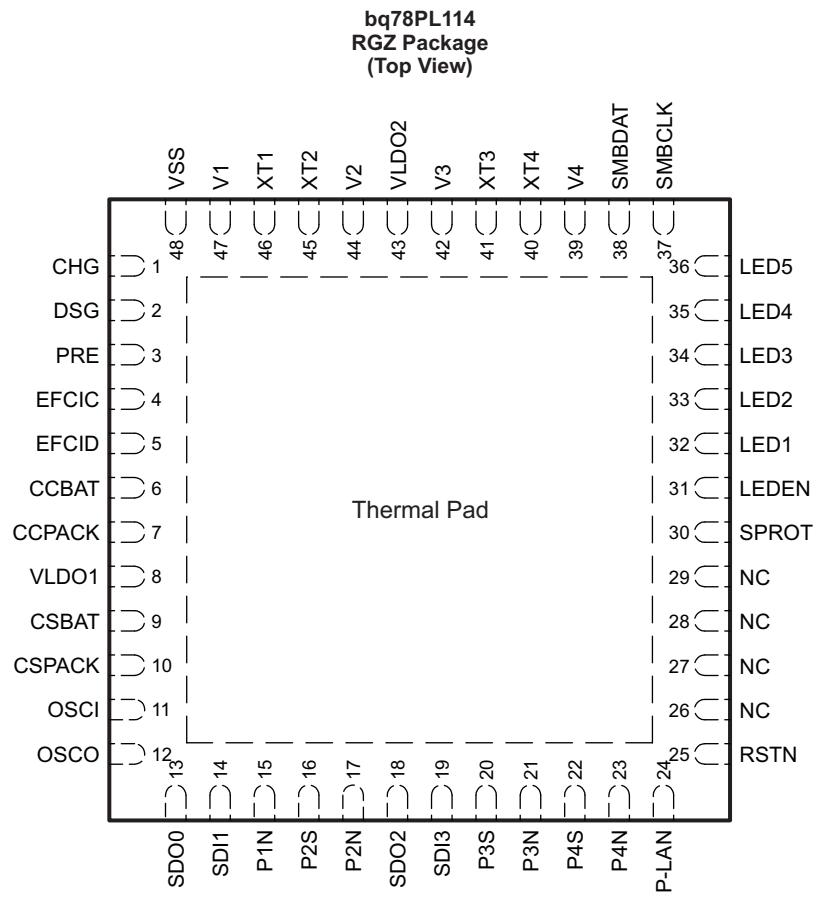


Figure 4. Example bq78PL114S12 System Implementation (12 Cells)

ORDERING INFORMATION

Product	Cell Configuration ⁽¹⁾	Package	Package Designator	Temperature Range	Ordering Number	Quantity, Transport Media
bq78PL114	3 to 8 series cells	QFN-48, 7-mm x 7-mm	RGZ	−40°C to 85°C	bq78PL114RGZT	250, tape and reel
					bq78PL114RGZR	2500, tape and reel
bq78PL114S 12	3 to 12 series cells	N/A	N/A	N/A	N/A	Firmware download and upgrade

(1) For configurations consisting of more than four series cells, additional bq76PL102 parts must be used.

AVAILABLE OPTIONS


P0023-16

Figure 5. bq78PL114 Pinout

bq78PL114 TERMINAL FUNCTIONS

NAME	NO.	TYPE ⁽¹⁾	DESCRIPTION
CCBAT	6	IA	Coulomb counter input (sense resistor), connect to battery negative
CCPACK	7	IA	Coulomb counter input (sense resistor), connect to pack negative
CHG	1	O	Charge MOSFET control (active-high, low opens MOSFET)
CSBAT	9	IA	Current sense input (safety), connect to battery negative
CSPACK	10	IA	Current sense input (safety), connect to pack negative
DSG	2	O	Discharge MOSFET control (active-high, low opens MOSFET)
EFCIC	4	I	External charge MOSFET control input

(1) I – input, IA – analog input, O – output, OA – analog output, P – power

bq78PL114 TERMINAL FUNCTIONS (continued)

NAME	NO.	TYPE ⁽¹⁾	DESCRIPTION
EFCID	5	I	External discharge MOSFET control input
LED1	32	O	LED1 – open-drain, active-low
LED2	33	O	LED2 – open-drain, active-low
LED3	34	O	LED3 – open-drain, active-low
LED4	35	O	LED4 – open-drain, active-low
LED5	36	O	LED5 – open-drain, active-low
LEDEN	31	IO	LEDEN – common-anode drive (active-low) and pushbutton input
NC	26	IO	Connect 1-MΩ resistor to VSS
NC	27	I	Connect 1-MΩ resistor to VSS
NC	28, 29	O	No connect
OSCI	11	I	External oscillator input (no connect, internal oscillator used)
OSCO	12	O	External oscillator output (no connect, internal oscillator used)
P1N	15	O	Charge-balance gate drive, cell 1 north
P2S	16	O	Charge-balance gate drive, cell 2 south
P2N	17	O	Charge-balance gate drive, cell 2 north
P3N	21	O	Charge-balance gate drive, cell 3 north
P3S	20	O	Charge-balance gate drive, cell 3 south
P4N	23	O	Charge-balance gate drive, cell 4 north
P4S	22	O	Charge-balance gate drive, cell 4 south
P-LAN	24	IO	PowerLAN I/O to external bq76PL102 nodes
PRE	3	O	Precharge MOSFET control (active-high)
RSTN	25	I	Device reset, active-low
SDI1	14	I	Connect to SDO0 via a capacitor
SDI3	19	I	Internal PowerLAN connection – connect to SDO2 through a 0.01-µF capacitor
SDO0	13	O	Requires 100-kΩ pullup resistor to VLDO1
SDO2	18	O	Internal PowerLAN connection – connect to SDI3 through a 0.01-µF capacitor
SMBCLK	37	IO	SMBus clock signal
SMBDAT	38	IO	SMBus data signal
SPROT	30	O	Secondary protection output, active-high (FUSE)
V1	47	IA	Cell-1 positive input
V2	44	IA	Cell-2 positive input
V3	42	IA	Cell-3 positive input
V4	39	IA	Cell-4 positive input
VLDO1	8	P	Internal LDO-1 output, bypass with 10-µF capacitor to VSS
VLDO2	43	P	Internal LDO-2 output, bypass with 10-µF capacitor to V2
VSS	48	IA	Cell-1 negative input
XT1	46	IA	External temperature-sensor-1 input
XT2	45	IA	External temperature-sensor-2 input
XT3	41	IA	External temperature-sensor-3 input
XT4	40	IA	External temperature-sensor-4 input
—	—	P	Thermal pad. Connect to VSS

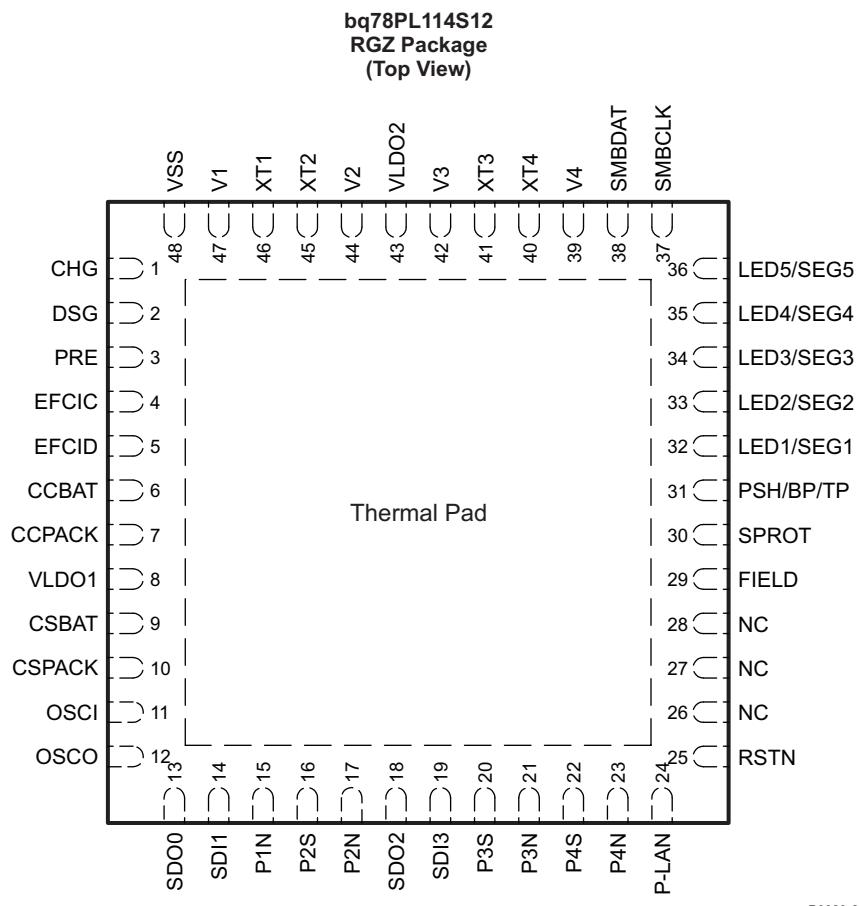


Figure 6. bq78PL114S12 Pinout

bq78PL114S12 TERMINAL FUNCTIONS

NAME	NO.	TYPE ⁽¹⁾	DESCRIPTION
CCBAT	6	IA	Coulomb counter input (sense resistor), connect to battery negative
CCPACK	7	IA	Coulomb counter input (sense resistor), connect to pack negative
CHG	1	O	Charge MOSFET control (active-high, low opens MOSFET)
CSBAT	9	IA	Current sense input (safety), connect to battery negative
CSPACK	10	IA	Current sense input (safety), connect to pack negative
DSG	2	O	Discharge MOSFET control (active-high, low opens MOSFET)
EFCIC	4	I	External charge MOSFET control input
EFCID	5	I	External discharge MOSFET control input
FIELD	29	O	EPD field segment
LED1/SEG1	32	O	LED1 – open-drain, active-low, LCD and EPD segment 1
LED2/SEG2	33	O	LED2 – open-drain, active-low, LCD and EPD segment 2
LED3/SEG3	34	O	LED3 – open-drain, active-low, LCD and EPD segment 3
LED4/SEG4	35	O	LED4 – open-drain, active-low, LCD and EPD segment 4
LED5/SEG5	36	O	LED5 – open-drain, active-low, LCD and EPD segment 5
N/C	26, 27	IO	Connect 1-MΩ resistor to VSS
N/C	28	O	No connect
OSCI	11	I	External oscillator input (no connect, internal oscillator used)

(1) I – input, IA – analog input, O – output, OA – analog output, P – power

bq78PL114S12 TERMINAL FUNCTIONS (continued)

NAME	NO.	TYPE ⁽¹⁾	DESCRIPTION
OSCO	12	O	External oscillator output (no connect, internal oscillator used)
P1N	15	O	Charge-balance gate drive, cell 1 north
P2N	17	O	Charge-balance gate drive, cell 2 north
P2S	16	O	Charge-balance gate drive, cell 2 south
P3N	21	O	Charge-balance gate drive, cell 3 north
P3S	20	O	Charge-balance gate drive, cell 3 south
P4N	23	O	Charge-balance gate drive, cell 4 north
P4S	22	O	Charge-balance gate drive, cell 4 south
P-LAN	24	IO	PowerLAN I/O to external bq76PL102 nodes
PRE	3	O	Precharge MOSFET control (active-high)
PSH/BP/TP	31	IO	Pushbutton detect for LED display, LCD backplane, EPD top plane and charge pump
RSTN	25	I	Device reset, active-low
SDI1	14	I	Connect to SDO0 via a capacitor
SDI3	19	I	Internal PowerLAN connection – connect to SDO2 through a 0.01- μ F capacitor
SDO0	13	O	Requires 100-k Ω pullup resistor to VLDO1
SDO2	18	O	Internal PowerLAN connection – connect to SDI3 through a 0.01- μ F capacitor
SMBCLK	37	IO	SMBus clock signal
SMBDAT	38	IO	SMBus data signal
SPROT	30	O	Secondary protection output, active-high (FUSE)
V1	47	IA	Cell-1 positive input
V2	44	IA	Cell-2 positive input
V3	42	IA	Cell-3 positive input
V4	39	IA	Cell-4 positive input
VLDO1	8	P	Internal LDO-1 output, bypass with 10- μ F capacitor to VSS
VLDO2	43	P	Internal LDO-2 output, bypass with 10- μ F capacitor to V2
VSS	48	IA	Cell-1 negative input
XT1	46	IA	External temperature-sensor-1 input
XT2	45	IA	External temperature-sensor-2 input
XT3	41	IA	External temperature-sensor-3 input
XT4	40	IA	External temperature-sensor-4 input
—	—	P	Thermal pad. Connect to VSS

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		RANGE	UNITS
T _A	Operating free-air temperature (ambient)	-40 to 85	°C
T _{stg}	Storage temperature	-65 to 150	°C
V4-V3	Maximum cell voltage	-0.5 to 5.0	V
V3-V2	Maximum cell voltage	-0.5 to 5.0	V
V2-V1	Maximum cell voltage	-0.5 to 5.0	V
V1-VSS	Maximum cell voltage	-0.5 to 5.0	V
Voltage on LEDEN, SPROT, CCBAT, CCPACK, CSBAT, CSPACK, XT1, XT2, OSCI, OSCO, P-LAN	Maximum voltage on any I/O pin with respect to VSS	-0.5 to (VLDO1 + 0.5)	V
Voltage on PSH/BP/TP (bq78PL114S12)	Maximum voltage range with respect to VSS	-0.5 to (VLDO1 + 0.5)	V
Voltage on LED1-LED5	Maximum voltage on I/O pin with respect to VSS	-0.5 to 5.5	V
Voltage on LED1/SEG1-LED5/SEG5 (bq78PL114S12)	Maximum voltage on I/O pin	-0.5 to 5.5	V
Voltage on XT3, XT4	Maximum voltage range with respect to V2	(V2 - 0.5) to (VLDO2 + 0.5)	V
EFCIC, EFCID	Maximum voltage range with respect to VSS	-0.5 to 5.5	V
Voltage on SMBCLK, SMBDAT	Maximum voltage range with respect to VSS	-0.5 to 6	V
Voltage on PRE, CHG, DSG	Maximum voltage range with respect to VSS	-0.5 to (VLDO1 + 0.5)	V
Current through PRE, CHG, DSG, LED1-LED5, P-LAN	Maximum current source/sink	20	mA
Current through LED1/SEG1-LED5/SEG5, (bq78PL114S12, LED mode)	Maximum current source/sink	20	mA
VLDO1 maximum current	Maximum current draw from VLDO	20	mA
ESD tolerance	JEDEC, JESD22-A114 human-body model, R = 1500 Ω, C = 100 pF	2	kV
Lead temperature, soldering	Total time < 3 seconds	300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{SUP}	Supply voltage—V1, V2, V3, V4	2.3	4.5		V
V _{Startup}	Minimum startup voltage—V1, V2	2.9			V
V _{IN}	Input cell voltage range—V(n+1) – V(n), n = 1, 2, 3, 4	0		4.5	V
C _{VLDO1}	VLDO 1 capacitor—VLDO1	2.2	10	47	μF
C _{VLDO2}	VLDO 2 capacitor—VLDO2	2.2	10	47	μF
C _{Vn}	Cell-voltage capacitor—Vn	1			μF

ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{CELL}}^{(1)}$ Operating range	Cells balanced	2.3		4.5	V
I_{DD} Operating-mode current	Measure / report state, bq78PLL114		250		μA
	Measure / report state, bq78PLL114S12		300		
I_{STBY} Standby-mode current	SMBCLK = SMBDAT = L, bq78PLL114		100		μA
	SMBCLK = SMBDAT = L, bq78PLL114S12		185		
I_{SHIP} Ship-mode current	bq78PLL114		30		μA
	bq78PLL114S12		85		
I_{ECUV} Extreme cell under voltage shutdown current	All cells < 2.7 V and any cell < ECUV set point			1	μA
V_{OL}	SPROT, LEDEN, PSH/BP/TP(bq78PL114S12), FIELD(bq78PL114S12)	$I_{\text{OL}} < 4 \text{ mA}$	0	0.5	V
$V_{\text{OH}}^{(2)}$	SPROT, LEDEN, PSH/BP/TP(bq78PL114S12), FIELD(bq78PL114S12)	$I_{\text{OH}} < -4 \text{ mA}$		$V_{\text{LDO1}} - 0.1$	V
V_{IL}	SPROT, LEDEN, PSH/BP/TP(bq78PL114S12), FIELD(bq78PL114S12)			$0.25 V_{\text{LDO1}}$	V
V_{IH}	SPROT, LEDEN, PSH/BP/TP(bq78PL114S12), FIELD(bq78PL114S12)			$0.75 V_{\text{LDO1}}$	V

(1) Device should be configured to enter shutdown state when cell voltages are below 2.5 V.

(2) Does not apply to SMBus pins.

Voltage-Measurement Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		2.5		4.5	V
Resolution			<1		mV
Accuracy	25°C		± 5		mV
	0°C to 60°C		± 10		

Current-Sense Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range ⁽¹⁾ (bq78PL114)		-0.2		0.2	V
Measurement range ⁽²⁾ (bq78PL114S12, 3-mΩ sense resistor)		-0.077		0.077	V
Measurement range ⁽²⁾ (bq78PL114S12, 1-mΩ and 10-mΩ sense resistors)		-0.1		0.1	V
Input offset	$T_A = 25^\circ\text{C}$		± 50		μV
Offset drift	$T_A = 0^\circ\text{C}$ to 60°C		0.5		$\mu\text{V}/^\circ\text{C}$
Resolution (bq78PL114)			18		μV
Resolution (bq78PL114S12, 3-mΩ sense resistor)			6.9		μV
Resolution (bq78PL114S12, 1-mΩ and 10-mΩ sense resistors)			10		μV
Full-scale error ⁽³⁾	$T_A = 25^\circ\text{C}$		$\pm 0.1\%$		
Full-scale error drift	$T_A = 0^\circ\text{C}$ to 60°C		50		$\text{PPM}/^\circ\text{C}$

(1) Default range. Corresponds to ± 10 A using a 5-mΩ sense resistor.

(2) The bq78PL114S12 firmware upgrade supports three sense-resistor options, 10 mΩ, 3 mΩ, and 1 mΩ.

(3) After calibration. Accuracy is dependent on system calibration and temperature coefficient of sense resistor.

Coulomb-Counter Characteristics^{(1) (2)}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			5		nVh
Integral nonlinearity			0.008%		
Snap-to-zero (deadband)			$\pm 100^{(3)}$		μV

(1) Shares common input with current-sense section

(2) After calibration. accuracy is dependent on system calibration and temperature coefficient of sense resistor.

(3) Corresponds to 20 mA using 5-mΩ sense resistor

Current-Sense (Safety) Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		-0.312		0.312	V
Resolution	Short-circuit detection		10		mV
	Overcurrent detection, charge and discharge		1.25		

(1) Post calibration: Dependent on system calibration and temperature coefficient of sense resistor. Uncertainty is 1.5 LSB.

Internal Temperature-Sensor Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		-30		85	°C
Resolution			0.1		°C
Accuracy ⁽¹⁾	-30° to 85°		± 1		°C

(1) After calibration

LDO Voltage Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO1}	$T_A = -40^\circ\text{C}$ to 85°C , load = 200 μA	2.425	2.5	2.575	V
V_{LDO2}	$T_A = -40^\circ\text{C}$ to 85°C , load = 2 mA	2.425	2.5	2.575	V

(1) After calibration

External Temperature-Sensor(s) Typical Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range ⁽²⁾		-40	90		$^\circ\text{C}$
Resolution			0.2		$^\circ\text{C}$
Accuracy ⁽³⁾	25°		±1		$^\circ\text{C}$
	0° to 85°		±2		

(1) Typical for dual-diode (MMBD4148 or equivalent) external sensor using recommended circuit

(2) Range of diode sensors may exceed operational limits of IC and battery cells.

(3) Typical behavior after calibration, final result dependent on specific component characteristics

SMBus Characteristics⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low voltage	0	0.8		V
V_{IH}	Input high voltage	2.1	5.5		V
V_{OL}	Output low voltage	350- μA sink current	0	0.4	V
C_I	Capacitance, each I/O pin			10	pF
f_{SCL}	SCLK nominal clock frequency	$T_A = 25^\circ\text{C}$	100		kHz
$R_{PU}^{(2)}$	Pullup resistors for SCLK, SDATA	V_{BUS} 5 V nominal	13.3	45.3	$\text{k}\Omega$
		V_{BUS} 3 V nominal	2.4	6.8	

(1) SMBus timing and signals meet the SMBus 2.0 specification requirements under normal operating conditions. All signals are measured with respect to PACK-negative.

(2) Pullups are typically implemented external to the battery pack, and are selected to meet SMBus requirements.

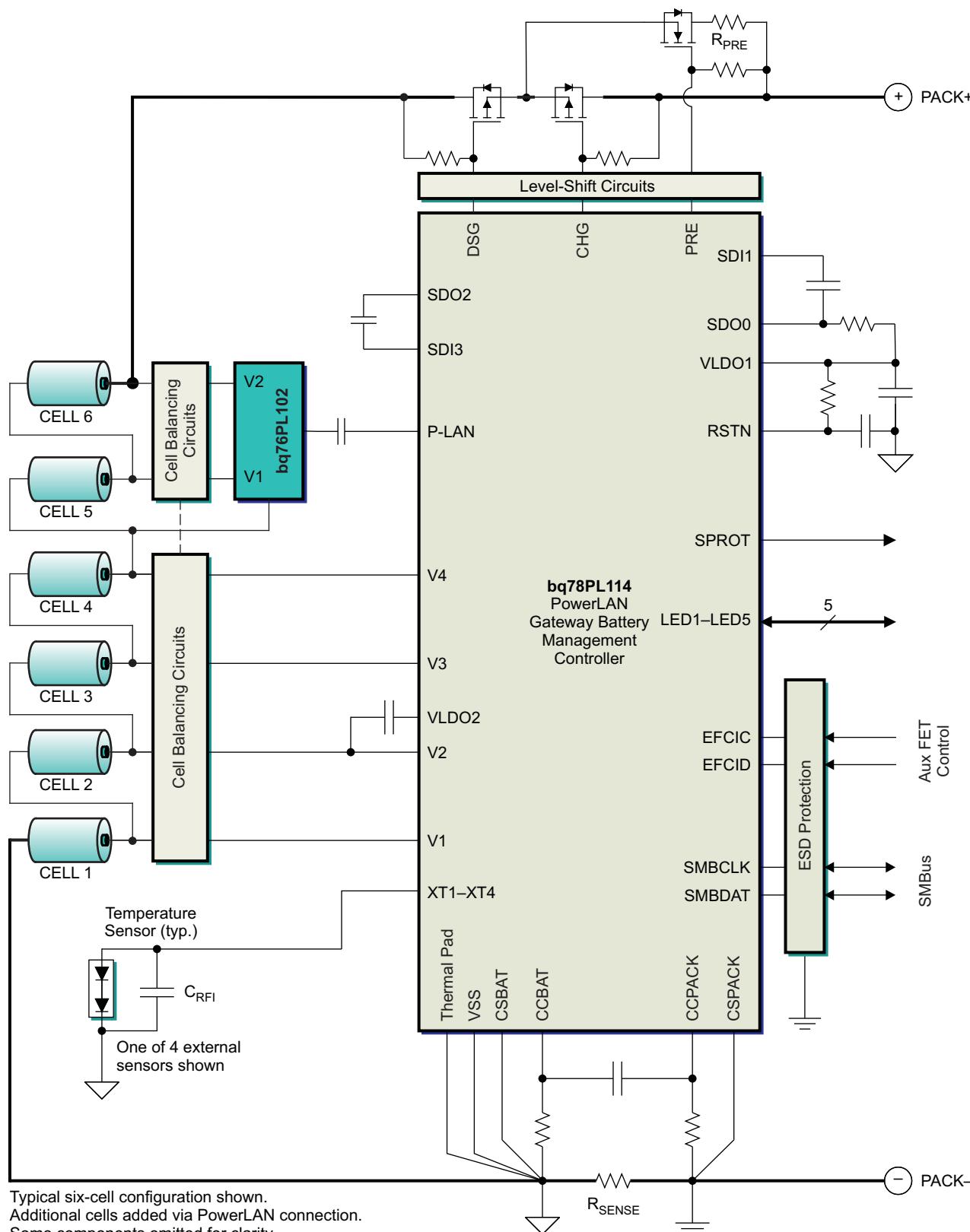


Figure 7. bq78PL114 Simplified Example Circuit Diagram

FEATURE SET

Primary (First-Level) Safety Features

The bq78PL114 implements a breadth of system protection features which are easily configured by the customer. First-level protections work by controlling the MOSFET switches. These include:

- Battery cell over/undervoltage protection
- Pack over/undervoltage protection
- Charge and discharge overcurrent protection
- Short-circuit protection
- External MOSFET control inputs (EFCIx) with programmable polarity
- Up to 12 external temperature inputs for accurate cell and MOSFET monitoring
- Watchdog timer protection
- Brownout detection and protection against extreme pack undervoltage

Secondary (Second-Level) Safety Features

The bq78PL114 can detect more serious system faults and activate the SPROT pin, which can be used to open an in-line chemical fuse to permanently disable the pack. Secondary optional features include

- Fully independent of first-level protections
- SmartSafety algorithms for early detection of potential faults
 - Temperature abnormalities (variances, extremes, rate of change, etc.)
 - Disconnected cell voltage inputs
 - Cell imbalance exceeds safety limits
 - Impedance rise due to cell or weld strap fault
- MOSFET failure or loss of MOSFET control
- Safety overvoltage, pack and cell
- Safety overtemperature, limits for both charge and discharge
- Safety overcurrent, charge and discharge
- Failed current measurement, voltage measurement, or temperature measurement

Charge Control Features

- Meets SMBus 2.0 and Smart Battery System (SBS) Specification 1.1 requirements
- Active cell balancing using patented PowerPump technology, which eliminates unrecoverable capacity loss due to normal cell imbalance
- Balancing-current monitoring to detect cell problems
- Simultaneous, synchronous measurement of all cell voltages in a pack
- Simultaneous, synchronous measurement of pack current with cell voltages
- Reports target charging current and/or voltage to an SBS Smart Charger
- Reports the chemical state-of-charge for each cell and pack
- Supports precharging and zero-volt charging with separate MOSFET control
- Programmable, Chemistry-specific parameters
- Fault reporting

Gas Gauging

- The bq78PL114 accurately reports battery cell and pack state-of-charge (SOC). No full charge/discharge cycle is required for accurate reporting.
- State-of-charge is reported via SMBus and optional display.
- 18-bit integrating delta-sigma ADC coulomb counter, with programmable snap-to-zero value

Display Types

- The bq78PL114 drives a three- to five-segment LED display in response to a pushbutton (LEDEN) input signal. Each LED pin can sink up to 10 mA.

- The bq78PL114S12 drives a three- to five-segment static liquid-crystal display.
- The bq78PL114S12 drives a three- to five-segment electronic paper display. An external 15-V voltage source is required. E Ink Corporation supplies this type of display.

The display type is selected via the parameter set.

Lifetime Logging (Readable via SMBus)

- Recording of faults, events, anomalies, minimum and maximum values
- Maximum/minimum temperature
- Maximum/minimum pack voltage
- Maximum/minimum cell voltage in a pack
- Maximum charge and discharge currents

Forensic Data Logging (Readable via SMBus)

- Last known full capacity of each cell
- Cycle count and/or cumulative number of ampere-hours delivered by the battery
- Battery pack status: being charged, discharged, or at rest
- Balancing effort required by each bank of cells to maintain balance
- Last 10 failures causing first-level safety action
- Forensic data up-loadable to host CPU via SMBus

Power Modes

- **Normal Mode:** The bq78PL114 performs measurements and calculations, makes decisions, and updates internal data approximately once per second. *All safety circuitry is fully functional in this mode.*
- **Standby Mode:** The bq78PL114 performs as in normal mode, but at a dramatically reduced rate to lower power consumption at times when the host computer is inactive or the battery system is not being used. *All safety circuitry remains fully functional in this mode.*
- **Ship Mode:** The bq78PL114 disables (opens) all the protection MOSFETs, and continues to monitor temperature and voltage, but at a reduced measurement rate to dramatically lower power consumption. Environmental data is saved in flash as a part of the historical record. *Safety circuitry is disabled in this mode.* The device does not enter this power state as a part of normal operation; it is intended for use after factory programming and test. Entry occurs only after a unique SMBus command is issued. Exit occurs when the SMBus lines return to an active state.
- **Extreme Cell Undervoltage (ECUV) Shutdown Mode:** In this mode, the bq78PL114 draws minimal current and the charge and discharge protection MOSFETs are disabled (opened). The precharge MOSFET remains enabled when a charge voltage is present. *Safety circuitry is disabled in this mode.* The device does not enter this mode as a part of normal operation; it enters this state during extreme cell undervoltage conditions (ECUV). The ECUV threshold is programmable between 2.3 V and 2.7 V, with 2.5 V being typical.

STATE	OVERCURRENT PROTECTION	ENTRY CONDITION	EXIT CONDITION
Active	Fully active	Normal operation as determined by firmware	Firmware directed to the following operating modes
Standby	Fully active	No load current flowing for predetermined time	Load activity
Ship	Not active	Protected SMBus command	SMBus becomes active
Extreme cell undervoltage	Not active (precharge enabled)	Enabled when $V_{cell} < ECUV$	V_{cell} charge above ECUV recovery threshold (2.7 V/cell typical)

OPERATION

The bq78PL114 battery-management controller serves as a master controller for a Li-Ion battery system consisting of up to 8 cells in series. The bq78PL114S12 firmware upgrade supports up to 12 cells in series. Any number of cells may be connected in parallel; other system or safety issues limit the number of parallel cells. The bq78PL114 provides extraordinarily precise state-of-charge gas gauging along with first- and second-level pack safety functions. Voltage and current measurements are performed synchronously and simultaneously for all cells in the system, allowing a level of precision not previously possible in battery management. Temperature is

measured by up to four additional external temperature sensors. With the bq78PL114S12 firmware upgrade, up to eight more are available in remote bq76PL102 dual-cell battery monitors. Coulomb counting is captured continuously by a dedicated 18-bit integrating delta-sigma ADC in the bq78PL114. The CPU in the bq78PL114 is also responsible for system data calculations, black-box forensic data storage, and communicating parameters via the SMBus interface. The bq78PL114S12 firmware can be downloaded to existing bq78PL114 parts using the bqWizard GUI or during the manufacturing checkout process.

PowerLAN Communication Link

PowerLAN technology is Texas Instruments' patented serial network and protocol designed specifically for battery management in a multicell system environment. The PowerLAN link is used to initiate and report measurements of cell voltage and temperature, and control cell balancing. The bq78PL114 serves as the master controller of the PowerLAN link and can interface to multiple bq76PL102 dual-cell battery monitors, which measure and balance additional cells. The bq78PL114 monitors the first three or four cells, and bq76PL102s can be added to monitor more series cells.

The PowerLAN link isolates voltages from adjacent bq76PL102 devices to permit high-voltage stack assembly without compromising precision and accuracy. The PowerLAN link is expandable to support up to 12 cells in series. Each bq76PL102 handles voltage and temperature measurements, as well as balancing for two cells. The PowerLAN link provides high ESD tolerance and high immunity to noise generated by nearby digital circuitry or switching currents. Each bq76PL102 has both a PowerLAN input and PowerLAN output: Received data is buffered and retransmitted, permitting high numbers of nodes without loss of signal fidelity. Signals are capacitor-coupled between nodes, providing dc isolation.

Safety

Unique in the battery-management controller market, the bq78PL114 simultaneously measures voltage and current using independent and highly accurate delta-sigma ADCs. This technique removes virtually all systemic noise from measurements, which are made during all modes of battery operation: charge, discharge, and rest. The bq78PL114 also directs all connected bq76PL102 dual-cell battery monitors to measure each cell voltage simultaneously with the bq78PL114 measurements. Battery impedance and self-discharge characteristics are thus measured with an unprecedented level of accuracy in real time. The bq78PL114 applies this precise information to SmartSafety algorithms to detect certain anomalies and conditions which may be indicative of internal cell faults, before they become serious problems.

The bq78PL114 uses its enhanced measurement system to detect system faults including cell under- and overvoltage, cell under- and overtemperature, system overvoltage, and system overcurrent. First-level safety algorithms first attempt to open the MOSFET safety switches. If this fails, second-level safety algorithms activate the SPROT output, normally used to open a fuse and provide permanent, hard protection for the systems. External MOSFET control inputs with programmable polarity can also be used to operate the safety MOSFETs under control of user supplied circuitry. The bq78PL114 continuously monitors these inputs. If any MOSFET fails to open when commanded; the 2nd level safety algorithms also activate the SPROT output. All first- and second-level safety algorithms have fully programmable time delays to prevent false triggering.

Cell Balancing

Patented PowerPump cell balancing technology drastically increases the useful life of battery packs by eliminating the cycle life fade of multi-cell packs due to cell imbalance. PowerPump technology efficiently transfers charge from cell to cell, rather than simply bleeding off charging energy as heat as is typically done with resistive-bleed balancing circuits. Balancing is configurable and may be performed during any battery operational modes: charge, discharge, or rest. Compared to resistive bleed balancing, virtually no energy is lost as heat. The actual balance current is externally scalable and can range from 10 mA to 1 A (100 mA typical) depending on component selection and system or cell requirements.

A variety of techniques, such as simple terminal voltage, terminal voltage corrected for impedance and temperature effects, or state-of-charge balancing, is easily implemented by the bq78PL114. By tracking the balancing required by individual cells, overall battery safety is enhanced, often allowing early detection of soft shorts or other cell failures. Balancing is achieved between all cells within the pack as dynamically determined by the bq78PL114.

Outputs

Charge Control

The CHG and PRE outputs are ordinarily used to drive MOSFET transistors controlling charge to the cell stack. Charge or precharge mode is selected based on the present cell voltage compared to the user-definable cell precharge, undervoltage, and temperature thresholds. When below these limits, the PRE signal is active and the CHG signal is inactive. This turns on the precharge MOSFET and is used to charge a depleted system through a current-limiting series resistor. When all cell voltages are above the limit and the temperature is above the charge temperature minimum, then the CHG output also becomes active and enables the charge MOSFET to turn on, providing a high-current path between charger and battery cells.

The CHG and PRE MOSFET control outputs are both disabled (low) when any cell reaches the safety cutoff limit or temperature threshold. During active charging modes (and above cell voltage thresholds), the discharge MOSFET is also enabled to avoid excessive heating of the body diode. Similarly, the charge MOSFET is active during discharge, provided current flow is in the correct direction and no safety violations are present.

The bq78PL114S12 firmware upgrade supports the following configurable cell-balancing features:

- Super-pump mode. When enabled this allows 60%–70% pump availability when there are no active safety events and current is not flowing. While in super-pump mode, temperature rate-of-rise features are not available.
- Option to disable cell balancing during discharge
- Option to disable cell balancing during charge

The CHG and PRE outputs are intended to drive buffer transistors acting as inverting level shifters.

Discharge Control

The DSG output operates similarly to control-system discharging. It is enabled (high) by default. If a cell voltage falls below a programmable threshold, or excessive current or other safety related fault is sensed, the DSG output is disabled (low) to prevent damage to the cells.

All facets of safely charging and discharging the cell stack are controlled by user-definable parameters which provide precise control over MOSFET states. Both system and cell over- and undervoltage limits are provided, as well as programmable hysteresis to prevent oscillation. Temperature and current thresholds are also provided, each with independent timers to prevent nuisance activations.

The DSG output is intended to drive a buffer transistor acting as an inverting level-shifter.

Display

The bq78PL114 shows state-of-charge indication on a five-LED display in a bar-graph format. LEDEN is a dual-function pin. One function is to control current to the LED display array. It also serves as an input that monitors for closure of a state-of-charge indicator (SOCi) push-button switch.

The bq78PL114S12 shows state-of-charge indication on LED, static liquid crystal, and electronic paper displays or EPDs in a bar-graph-type format. The parameter set allows selection of display type and configuration. PSH/BP/TP is a multifunction pin. In LED display mode, PSH serves as an input that monitors for closure of a state-of-charge indicator (SOCi) push-button switch. In LCD mode, this pin is used to drive the LCD backplane. In EPD mode, this pin drives the top plane common signal of the display.

For both the bq78PL114 and bq78PL114S12, in LED display mode the signals LED1/SEG1–LED5/SEG5 are current-sinking outputs designed to drive low-current LEDs.

For the bq78PL114S12 firmware in LCD and EPD modes, the LED1/SEG1–LED5/SEG5 pins drive the active segments through external buffer transistors. In EPD mode, the FIELD pin drives the display background field.

Electronic paper displays require an external power supply, typically 15 V, to power the display. In EPD mode the bq78PL114S12 strobes the display outputs for a user-programmable period of milliseconds to drive an external voltage multiplier or charge pump to the required display supply voltage. The display segments are then updated in a manner that ensures the required 0-Vdc segment voltage offset is maintained and keeps the external power supply at its nominal voltage.

Inputs

Current Measurement

Current is monitored by four separate ADCs. All use the same very low-value sense resistor, typically 10, 5, 3, or 1 milliohms in series with the pack negative connection. CCBAT and CCPACK connections to the sense resistor use an R/C filter for noise reduction. (CSBAT and CSPACK are direct connections used for secondary safety). The bq78PL114 requires a 5-milliohm sense resistor. The bq78PL114S12 can be configured to use 10-, 3-, or 1-milliohm sense resistors. When configured to use a 1-milliohm sense resistor, the maximum available pack capacity increases to 655 Ah from 65 Ah.

A 14-bit delta-sigma ADC is used to measure current flow accurately in both directions. The measurements are taken simultaneously and synchronously with all the cell voltage measurements, even those cells measured by bq76PL102 dual-cell battery monitors.

Coulomb Counting

A dedicated coulomb counter is used to measure charge flow with 18-bit precision in both directions by a calibrated, integrating delta-sigma ADC. This allows the bq78PL114 to keep very accurate state-of-charge (SOC) information and battery statistics. A small deadband is applied to further reduce noise effects. The coulomb counter is unique in that it continues to accumulate (integrate) current flow in either direction even as the rest of the internal microcontroller is placed in a very low power state, further lowering power consumption without compromising system accuracy.

Safety Current

Two additional ADCs are used to directly monitor for overcurrent or short-circuit current conditions, independently of the internal function. This provides a direct and rapid response to insure pack integrity and safe operation by opening the appropriate MOSFETs. These functions are implemented in hardware, and do not require firmware for functionality.

Voltage Measurement

Voltage measurement is performed by four independent delta-sigma ADCs which operate simultaneously and are triggered synchronously so that all voltages are read at precisely the same moment. The bq78PL114 coordinates the attached bq76PL102 dual-cell battery monitors so they also perform their cell voltage measurements in sync with the bq78PL114 voltage and current measurements. Voltage measurements are converted with better than 1 mV of resolution, providing superior accuracy. One-ADC-per-cell technology means that voltage is also measured simultaneously with current, permitting accurate, real-time cell impedance calculation during all operating conditions. This technique also provides greatly enhanced noise immunity and filtering of the input signal without signal loss.

Temperature Measurement

XT1–XT4 are dedicated temperature-sensor inputs. Each external sensor consists of a low-cost silicon diode (dual diode in one package is recommended) and capacitor combination. Temperatures for cells 5 and above are measured by up to four external bq76PL102(s), and the temperature data is received by the bq78PL114 or bq78PL114S12 over the PowerLAN link for processing. The bq78PL114 or bq78PL114S12 can report all of these temperatures individually. The bq78PL114 allows multiplexed configuration of up to twelve temperature sensors. This permits the pack designer to measure temperatures of all cells and other items such as the charge and discharge MOSFETs. The bq78PL114S12 firmware uses the internal temperature sensor of the device for board temperature measurements.

EFC_{IX}

The external MOSFET control inputs are for user control of MOSFETs based on external circuitry and conditions. The polarity of the input signal is user-programmable. These pins can be used to force the protection MOSFETs to an OFF state.

COMMUNICATIONS

SMBus

The bq78PL114 uses the industry-standard Smart Battery System's two-wire System Management Bus (SMBus) communications protocol for all external communication. SMBus version 2.0 is supported by the bq78PL114, and includes clock stretching, bus fault time-out detection, and optional packet error checking (PEC). For additional information, see the www.smbus.org and www.sbs-forum.org Web sites.

Smart Battery Data (SBData)

The data content and formatting of the bq78PL114 information conforms to the Smart Battery System's (SBS) Smart Battery Data specification, version 1.1. See the SBS/SMBus site at www.sbs-forum.com for further information regarding these specifications.

This SBS Data (SBData) specification defines read/write commands for accessing data commonly required in laptop computer applications. The commands are generic enough to be useful in most applications.

Because the bq78PL114 provides a wealth of control and battery information beyond the SBData standard, new command codes have been defined by Texas Instruments. In addition, new battery data features, such as state-of-health, use newly defined extended SBData command codes. Standard SMBus protocols are used, although additional data values beyond those defined by the Smart Battery Data specification are employed. (For example, the bq78PL114 typically is used in a multicell battery system and may report individual cell voltages for up to eight cells. The bq78PL114S12 can report individual cell voltages for up to 12 cells. The SBData command set only defines four cell-voltage registers.)

SBS Standard Data Parameter List (Abridged)⁽¹⁾

Command	Data Type	Description
00	R/W word (unsigned)	Manufacturer Access
01	R/W word (unsigned)	Remaining Capacity Alarm Level
02	R/W word (unsigned)	Remaining Time Alarm Level
03	R/W word (unsigned)	Battery Mode
04	R/W word (unsigned)	At Rate value used in AtRate calculations
05	Read word (unsigned)	At Rate Time to Full
06	Read word (unsigned)	At Rate Time to Empty
07	Read word (Boolean)	At Rate OK
08	Read word (unsigned)	Pack Temperature (maximum of all individual cells)
09	Read word (unsigned)	Pack Voltage (sum of individual cell readings)
0A	Read word (unsigned)	Pack Current
0B	Read word (unsigned)	Average Pack Current
0C	Read word (unsigned)	Max Error
0D	Read word (unsigned)	Relative State of Charge
0E	Read word (unsigned)	Absolute State of Charge
0F	Read word (unsigned)	Remaining Pack Capacity
10	Read word (unsigned)	Full Charge Capacity
11	Read word (unsigned)	Run Time to Empty
12	Read word (unsigned)	Average Time to Empty
13	Read word (unsigned)	Average Time to Full
14	Read word (unsigned)	Charging Current
15	Read word (unsigned)	Charging Voltage
16	Read word (unsigned)	Battery Status
17	Read word (unsigned)	Cycle Count
18	Read word (unsigned)	Design Capacity
19	Read word (unsigned)	Design Voltage
1A	Read word (unsigned)	Specification Information
1B	Read word (unsigned)	Manufacture Date
1C	Read word (unsigned)	Serial Number
1D–1F	Reserved	
20	Read block (string)	Pack Manufacturer Name (31 characters maximum)
21	Read block (string)	Pack Device Name (31 characters maximum)
22	Read block (string)	Pack Chemistry
23	Read block (string)	Manufacturer Data
24–2E	Reserved	
2F	R/W Block	Optional Manufacturer Function 5
30–3B	Reserved	
3C	R/W word (unsigned)	Optional Manufacturer Option 4 (Vcell 1)
3D	R/W word (unsigned)	Optional Manufacturer Option 3 (Vcell 2)
3E	R/W word (unsigned)	Optional Manufacturer Option 2 (Vcell 3)
3F	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 4)
40	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 5)
41	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 6)
42	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 7)
43	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 8)
44	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 9, bq78PL114S12 only)

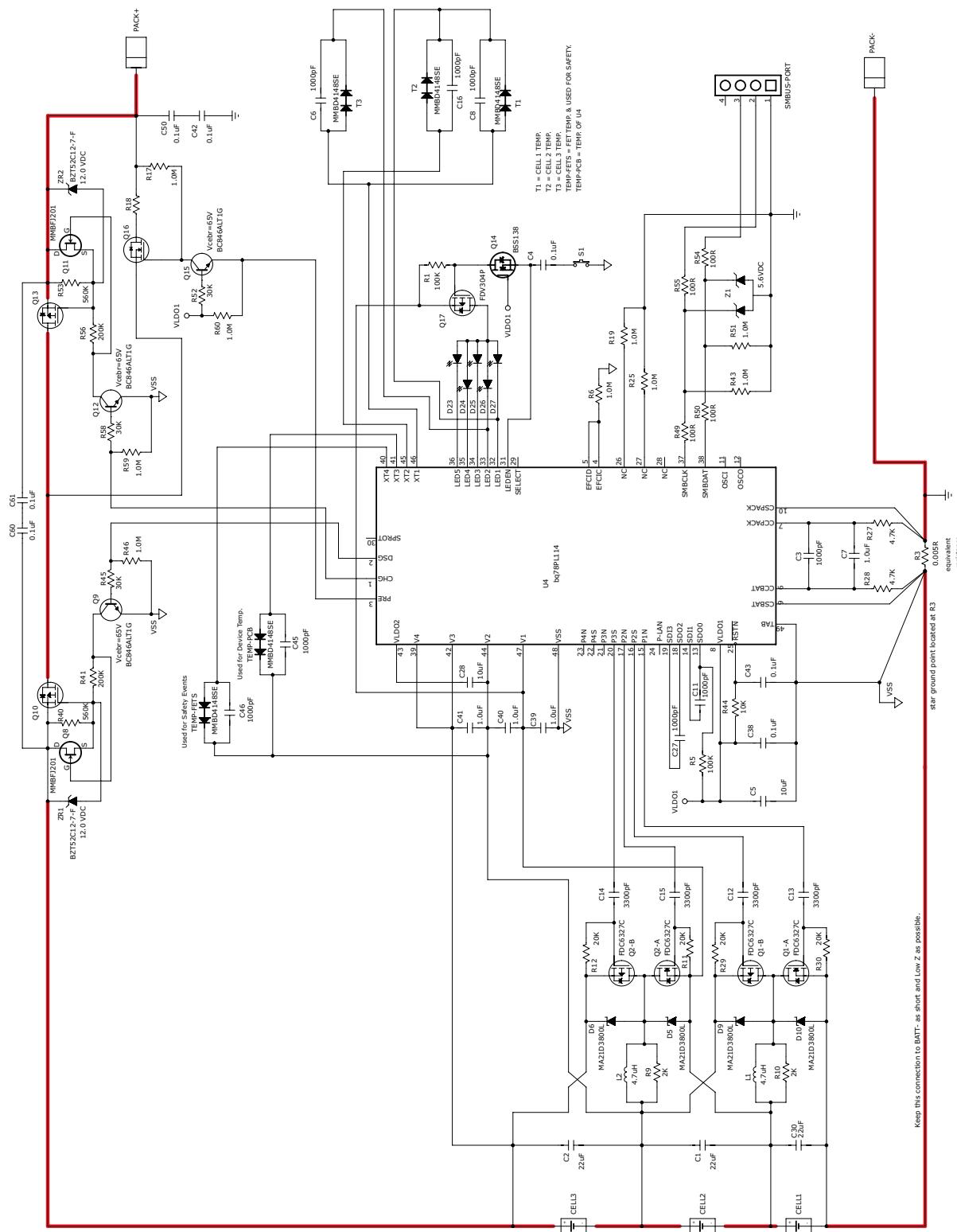
(1) Parameters 0x00–0x3F are compatible with the SBDATA specification.

Command	Data Type	Description
45	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 10, bq78PL114S12 only)
46	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 11, bq78PL114S12 only)
47	R/W word (unsigned)	Optional Manufacturer Option 1 (Vcell 12, bq78PL114S12 only)
48–4F	Unused	
50–55	Reserved	
56–57	Unused	
58–5A	Reserved	
5B–5F	Unused	
60–62	Reserved	
63–6F	Unused	
70	Reserved	
71–FF	Unused	

NOTE:

The bq78PL114 allows mapping of the eight cell voltage SBS locations to be different than its base address of 0x3C. The bq78PL114S12 does not support this feature.

REFERENCE SCHEMATICS



This configuration applies to the bq78PL114 only. The bq78PL114S12 has a different configuration for three-cell operation.

Figure 8. bq78PL114 Reference Schematic (3 Series Cells)

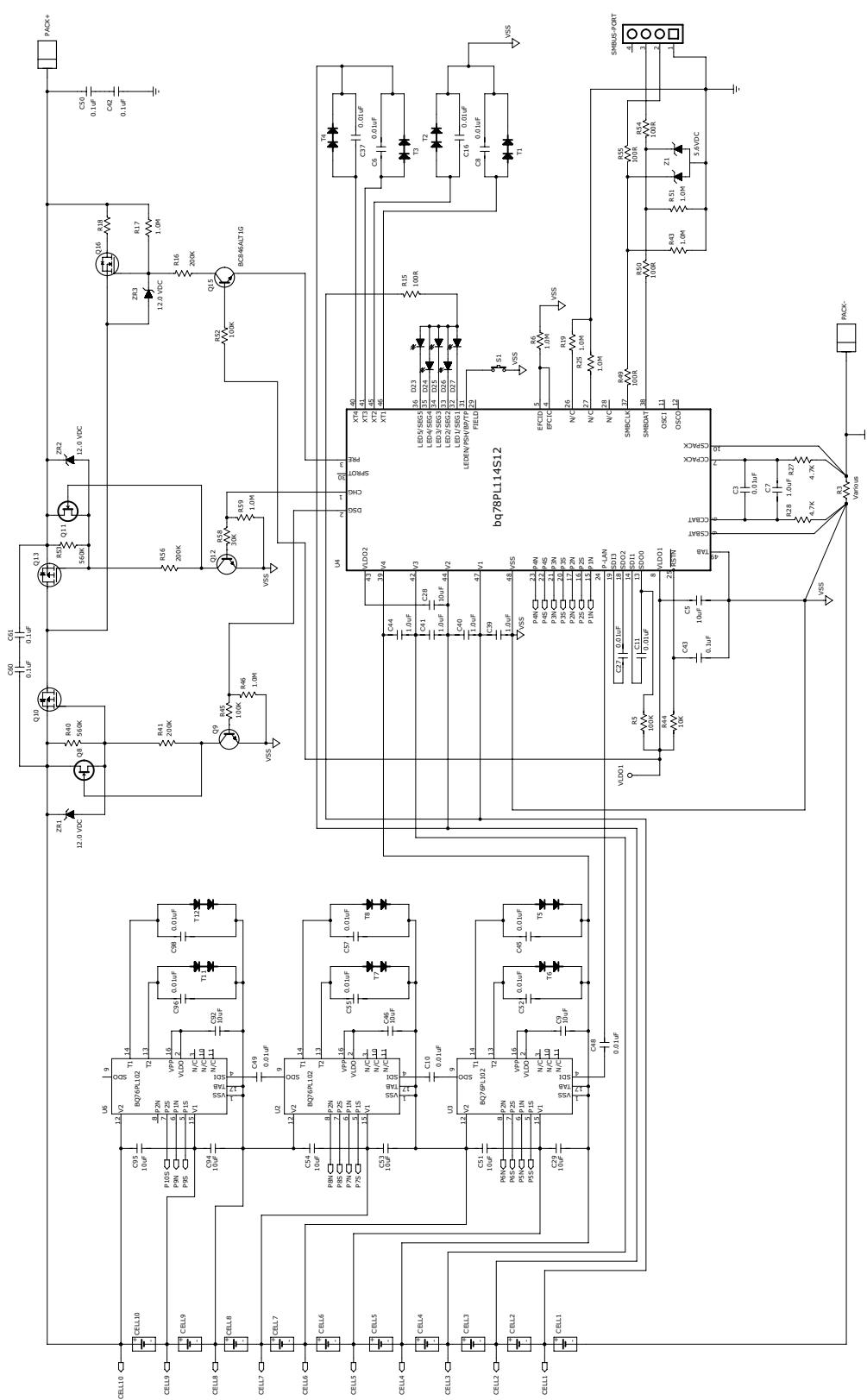
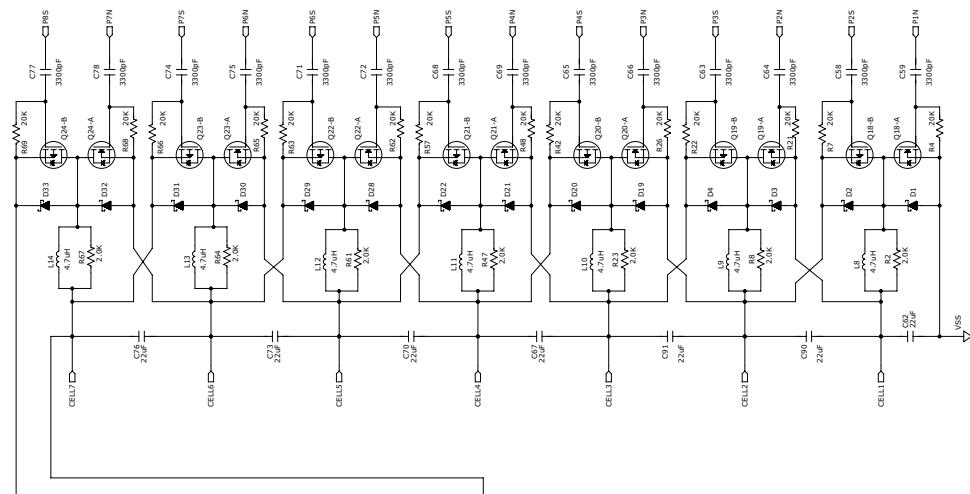
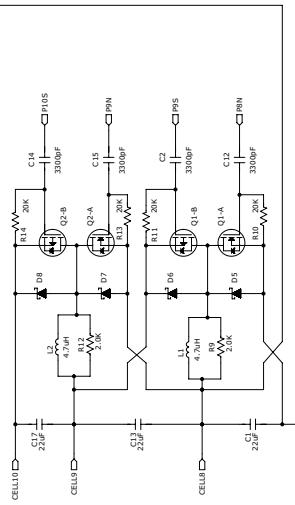


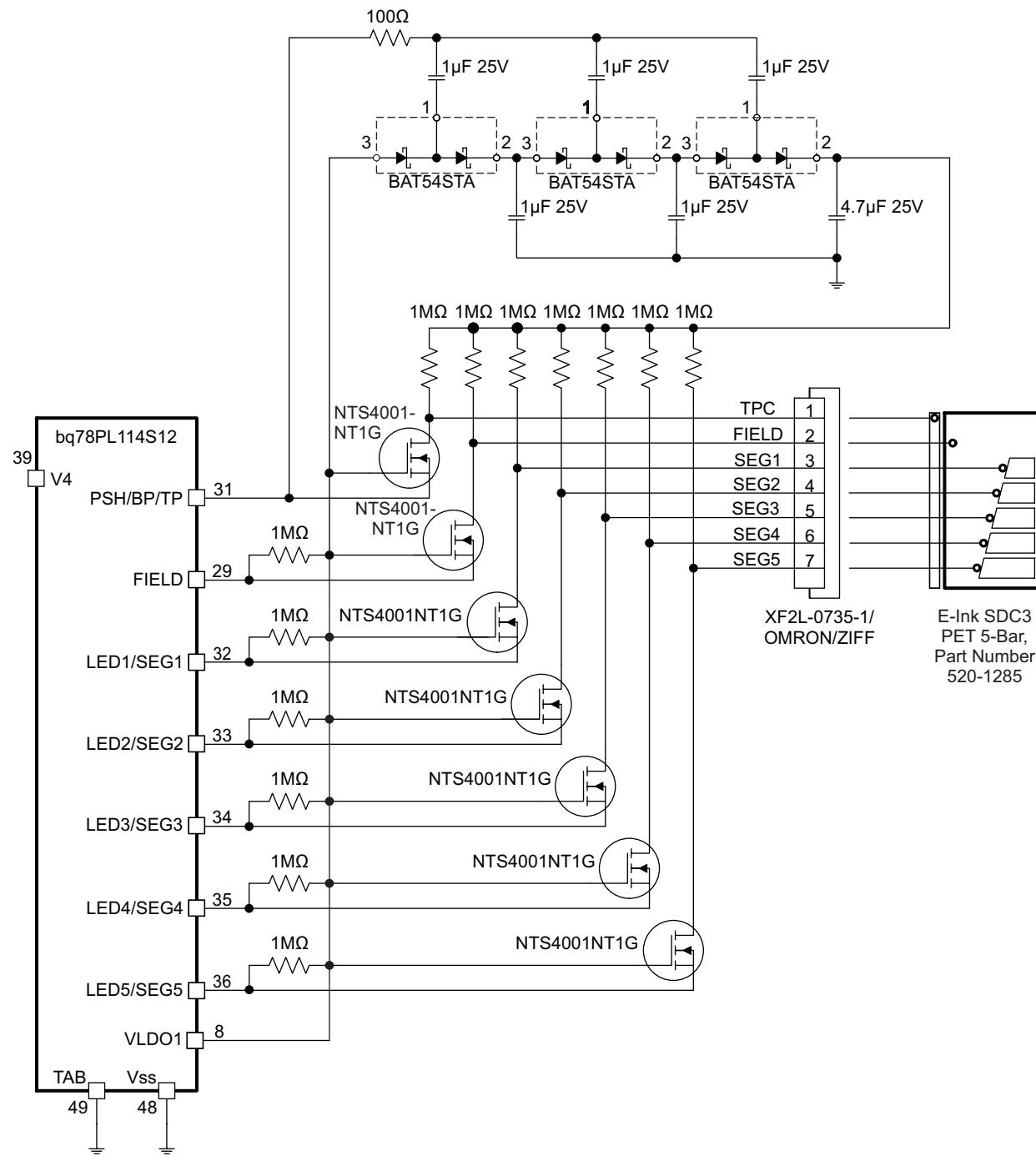
Figure 9. bq78PL114S12 Reference Schematic (10 Series Cells) (Sheet 1 of 2)

bq78PL114S12 Reference Schematic (10 Series Cells) (Sheet 2 of 2)



S002b

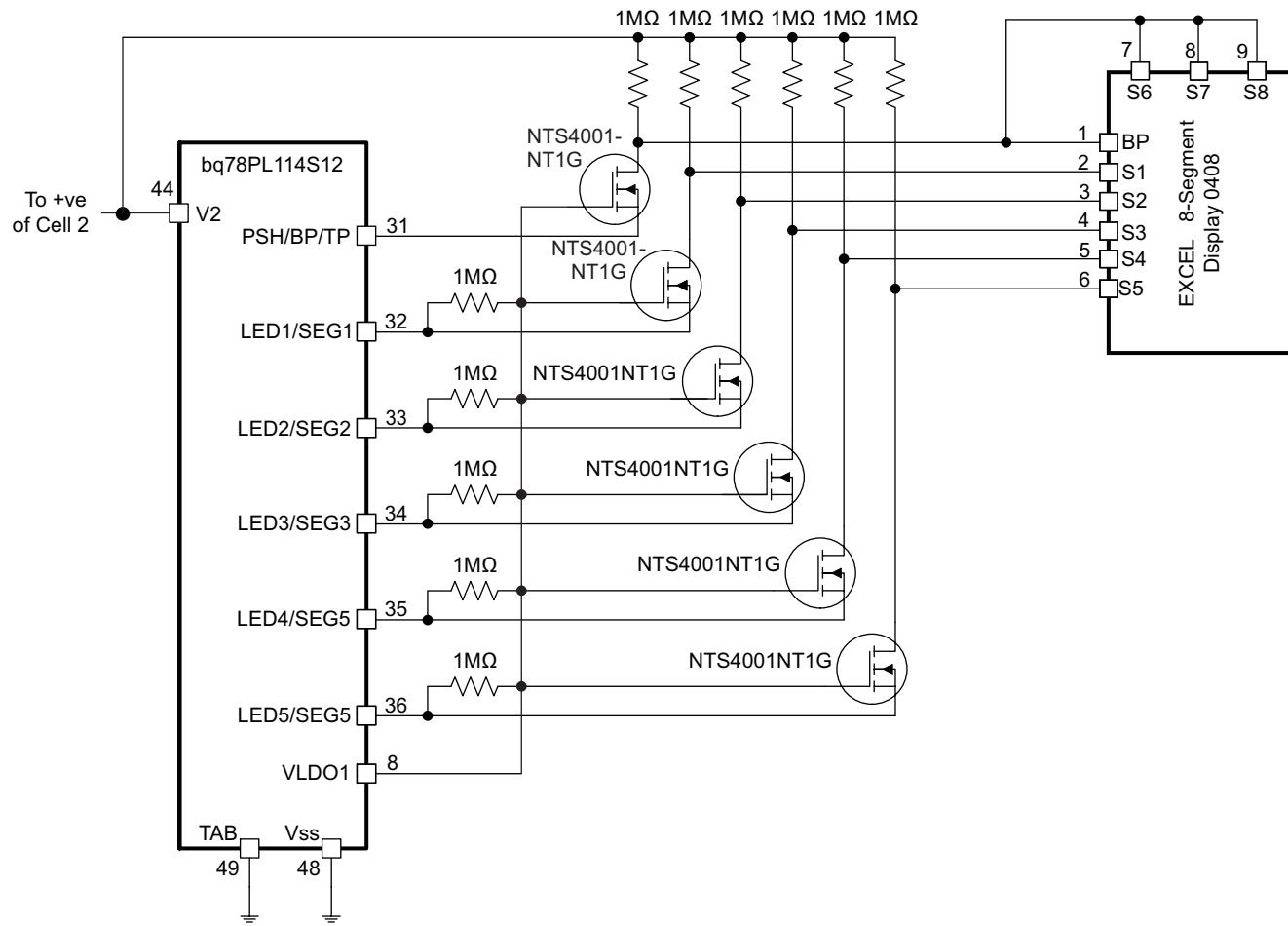




S003

NOTE: For reference only. Actual display used may require different operating voltage. Consult with display vendor.

Figure 10. Reference Schematic (Electronic-Paper Display Connections)



S004

NOTE: For reference only. Actual display used may require different operating voltage. Consult with display vendor.

Figure 11. Reference Schematic (LCD Connections)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ78PL114RGZR	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	78PL114 BQ
BQ78PL114RGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	78PL114 BQ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

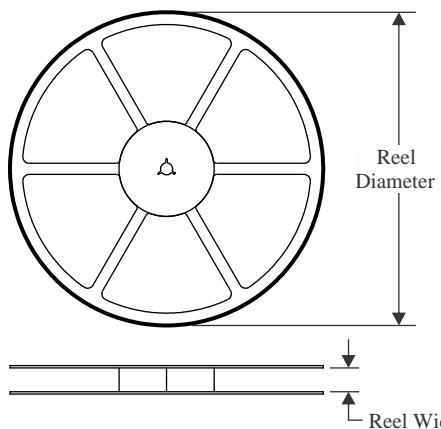
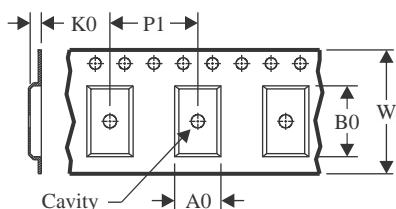
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

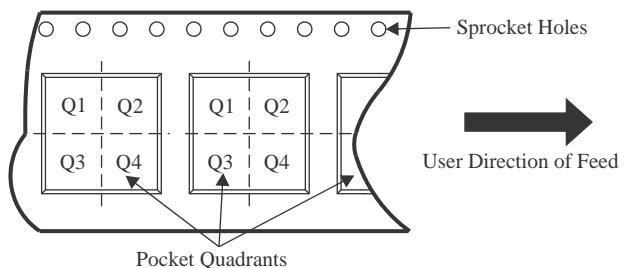
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ78PL114RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
BQ78PL114RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ78PL114RGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
BQ78PL114RGZT	VQFN	RGZ	48	250	213.0	191.0	35.0

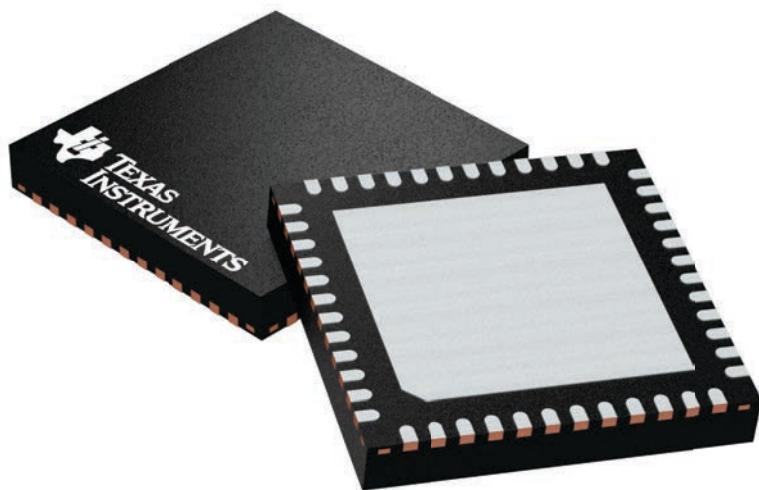
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

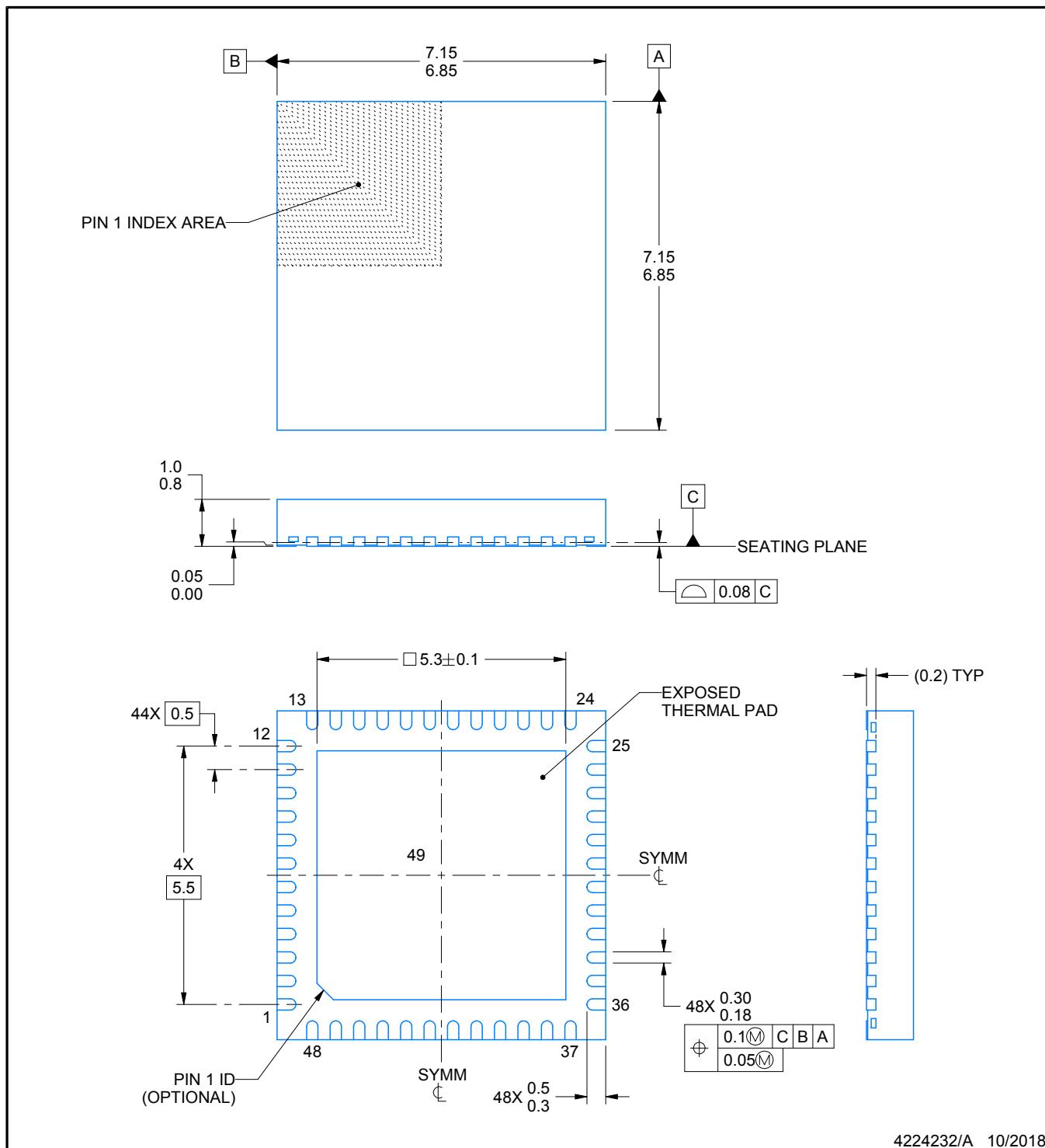
PACKAGE OUTLINE

RGZ0048H



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4224232/A 10/2018

NOTES:

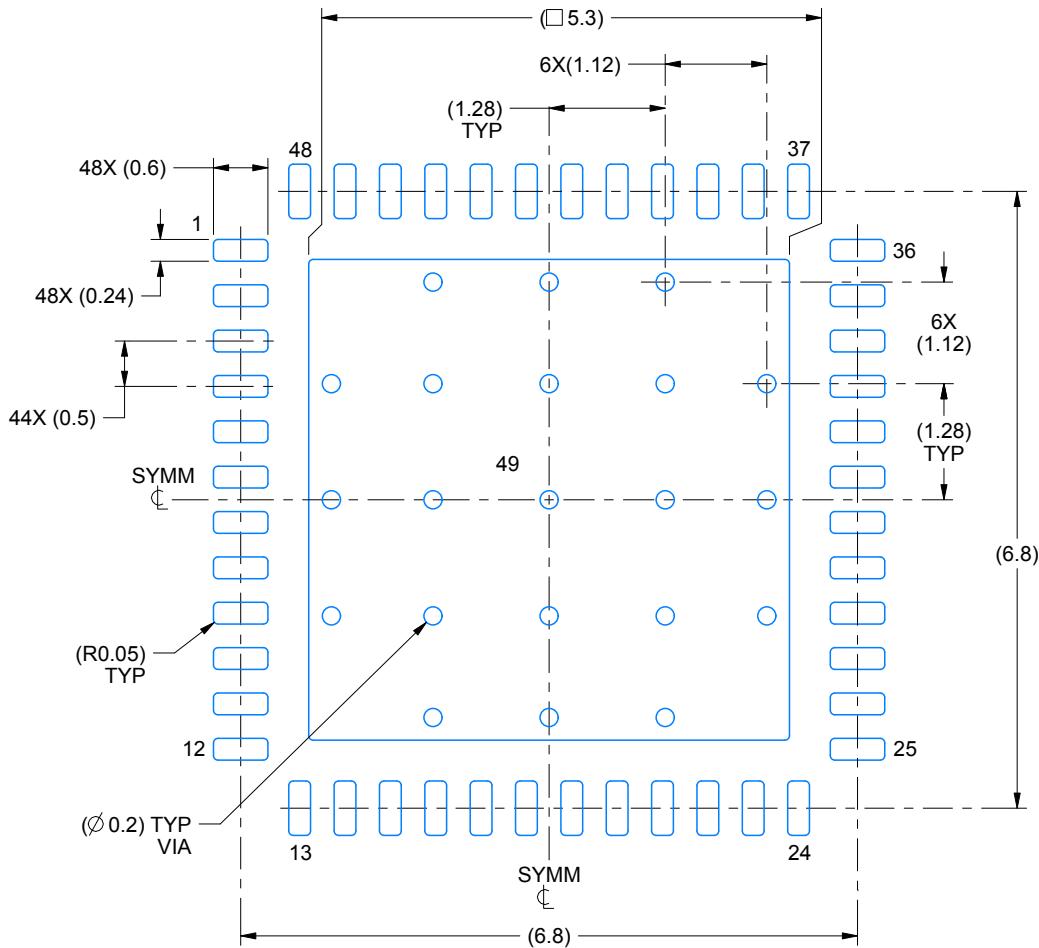
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

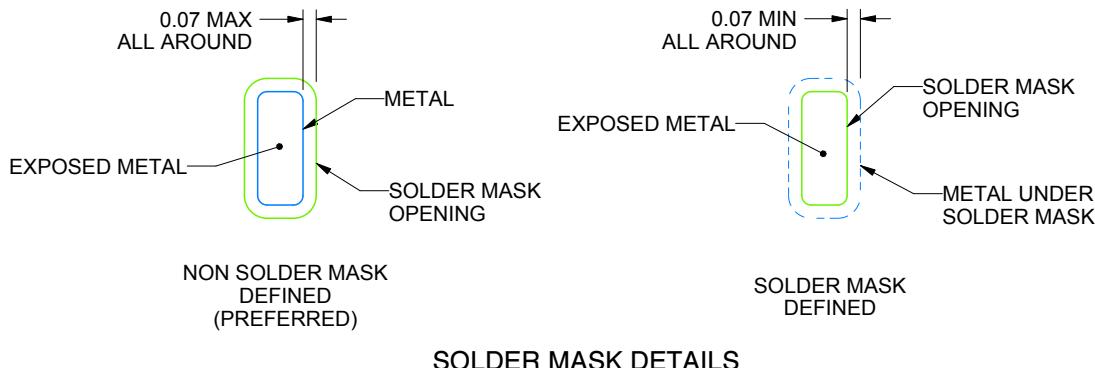
RGZ0048H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



4224232/A 10/2018

NOTES: (continued)

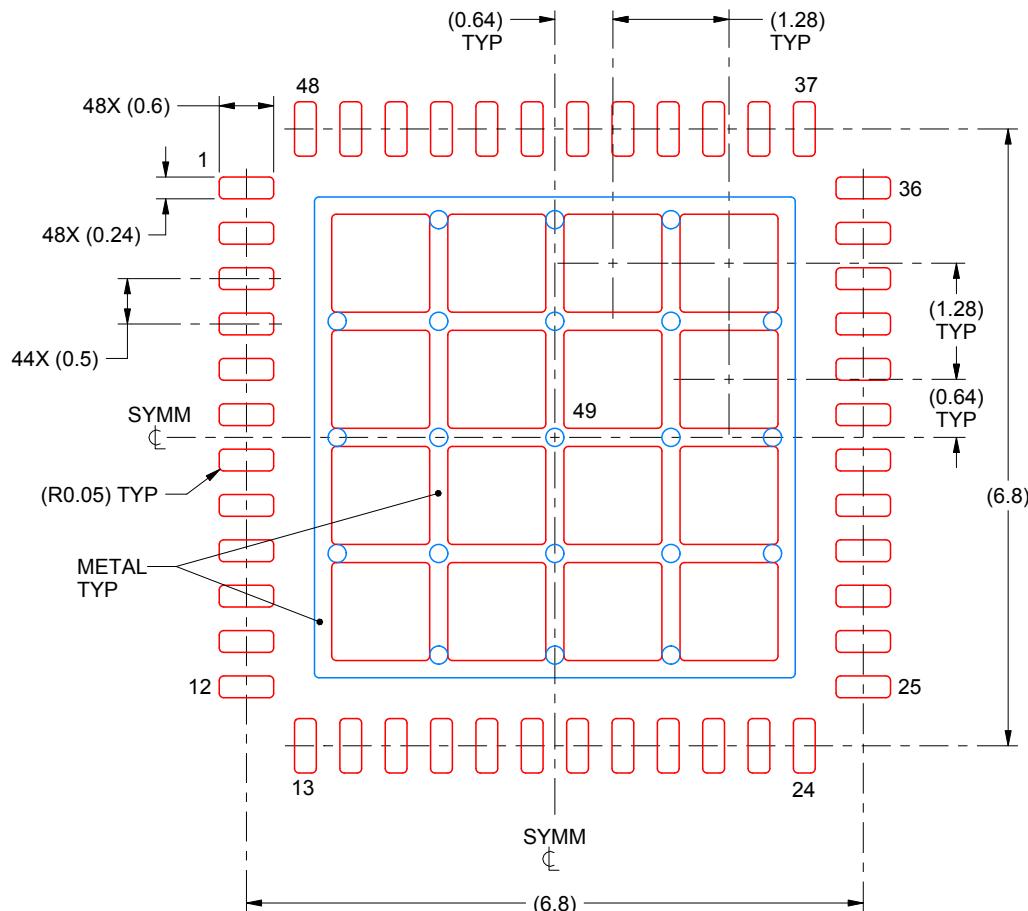
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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