

CD4016B Types CMOS Quad Bilateral Switch

1 Features

- 20V digital or $\pm 10V$ peak-to-peak switching
- 280 Ω typical on-state resistance for 15V operation
- Switch on-state resistance matched to within 10 Ω typ over 15V signal-input range
- High on/off output-voltage ratio: 65dB typ at $f_{is} = 10\text{kHz}$, $R_L = 10\text{k}\Omega$
- High degree of linearity: <0.5% distortion typ at $f_{is} = 1\text{kHz}$, $V_{is} = 5\text{V}_{p-p}$, $V_{DD} - V_{SS} = 10\text{V}$, $R_L = 10\text{k}\Omega$
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 100pA typ. at $V_{DD} - V_{SS} = 18\text{V}$, $T_A = 25^\circ\text{C}$
- Extremely high control input impedance (control circuit isolated from signal circuit: $10^{12} \Omega$ typ.)
- Low crosstalk between switches: -50dB typ at $f_{is} = 0.9\text{MHz}$, $R_L = 1\text{k}\Omega$
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40MHz (typical)
- 100% tested for quiescent current at 20V
- Maximum control input current of 1 μA at 18V over full package temperature range; 100nA at 18V at 25 $^\circ\text{C}$
- 5V, 10V, and 15V parametric ratings

2 Applications

- Analog signal switching/multiplexing signal gating
- Modulator squelch control
- Demodulator chopper
- Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital and digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

3 Description

For transmission or multiplexing of analog or digital signals high-voltage types (20V rating).

CD4016B *B* Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

The CD4016B *B* Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
CD4016B	N (PDIP, 14)	19.3mm \times 9.4mm
	D (SOIC, 14)	8.65mm \times 6mm

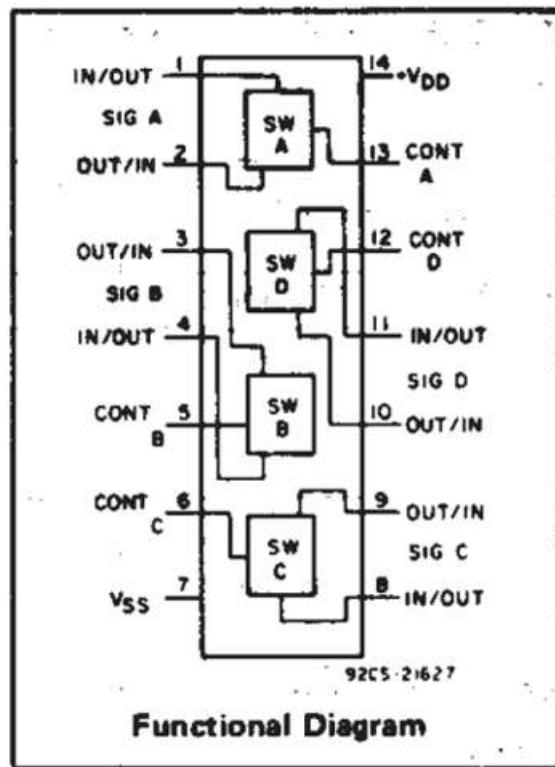
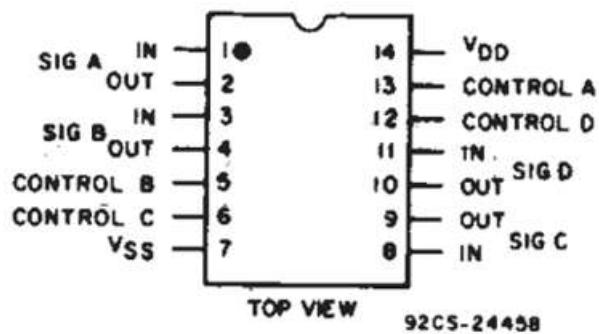
(1) For more information, see [Section 8](#).

(2) The package size (length \times width) is a nominal value and includes pins, where applicable.



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Terminal Assignment



Schematic Diagram - 1 of 4 Identical Sections

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		20	V
V_{DD}		-0.5	20	V
V_{SS}		-20	0.5	V
I_{SEL} or I_{EN}	Logic control input pin current (\bar{EN} , Ax, SELx)	-30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
I_S or I_D (CONT)	Source or drain continuous current (Sx, D)	-20	20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 1500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ ⁽¹⁾	Power supply voltage differential	3		18	V
V_{DD}	Positive power supply voltage	3		18	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}	V_{DD}		V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		V_{DD}	V
I_S or I_D (CONT)	Source or drain continuous current (Sx, D)	-10		10	mA
T_A	Ambient temperature	-55		125	°C

(1) V_{DD} and V_{SS} can be any value as long as $3V \leq (V_{DD} - V_{SS}) \leq 24V$, and the minimum V_{DD} is met.

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CD4016		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	93.7	109.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	72.5	69.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	68.0	67.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	50.3	25.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	67.3	67.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.5 Electrical Characteristics

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100Ω, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})								
I _{DD}	Quiescent Device Current	V _{IS} = 0 to 5V V _{DD} = 5V	T _A = -55°C				5	µA
			T _A = -40°C				5	
			T _A = 25°C			4.5	6	
			T _A = 85°C				7.5	
			T _A = 125°C				7.5	
		V _{IS} = 0 to 10V V _{DD} = 10V	T _A = -55°C				6	
			T _A = -40°C				6	
			T _A = 25°C			5	7	
			T _A = 85°C				15	
			T _A = 125°C				15	
		V _{IS} = 0 to 15V V _{DD} = 15V	T _A = -55°C				7	
			T _A = -40°C				7.2	
			T _A = 25°C			6	8	
			T _A = 85°C				30	
			T _A = 125°C				30	
		V _{IS} = 0 to 20V V _{DD} = 20V	T _A = -55°C				8.5	
			T _A = -40°C				8.5	
			T _A = 25°C			6.5	9	
			T _A = 85°C				150	
			T _A = 125°C				150	

4.5 Electrical Characteristics (continued)

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT			
r_{ON}	ON Resistance r_{ON} Max	to $(V_{DD}+V_{SS})/2$, $V_C = V_{DD}$, $RL = 10k\Omega$	$V_{DD} = 10V$ $V_{is} = V_{SS}$ or V_{DD}	$T_A = -55^\circ C$			600	Ω			
				$T_A = -40^\circ C$			610				
				$T_A = 25^\circ C$		250	660				
				$T_A = 85^\circ C$			840				
				$T_A = 125^\circ C$			960				
			$V_{DD} = 10V$ $V_{is} = 4.75$ to 5.75V	$T_A = -55^\circ C$			1870				
				$T_A = -40^\circ C$			1900				
				$T_A = 25^\circ C$			2000				
				$T_A = 85^\circ C$			2380				
				$T_A = 125^\circ C$			2600				
			$V_{DD} = 15V$ $V_{is} = V_{SS}$ or V_{DD}	$T_A = -55^\circ C$			360				
				$T_A = -40^\circ C$			370				
				$T_A = 25^\circ C$		200	400				
				$T_A = 85^\circ C$			520				
				$T_A = 125^\circ C$			600				
			$V_{DD} = 15V$ $V_{is} = 7.25$ to 7.75V	$T_A = -55^\circ C$			775	Ω			
				$T_A = -40^\circ C$			790				
				$T_A = 25^\circ C$			850				
				$T_A = 85^\circ C$			1080				
				$T_A = 125^\circ C$			1230				
r_{ON}	ON Resistance r_{ON} Max	to $(V_{DD}+V_{SS})/2$, $V_C = V_{DD}$, $RL = 10k\Omega$	$V_{DD} = 5V$ $V_{SS} = 0V$	$T_A = 25^\circ C$			580	Ω			
			$V_{DD} = 7.5V$ $V_{SS} = -7.5V$	$T_A = 25^\circ C$			200				
			$V_{DD} = 5V$ $V_{SS} = -5V$	$T_A = 25^\circ C$			250				
			$V_{DD} = 2.5V$ $V_{SS} = -2.5V$	$T_A = 25^\circ C$			520				
ΔR_{ON}	On-state resistance difference between any two switches	$R_L = 10k\Omega$, $V_C = V_{DD}$	$V_{DD} = 5V$				15	Ω			
			$V_{DD} = 10V$				10				
			$V_{DD} = 15V$				5				
THD	Total Harmonic Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 10k\Omega$, $f_{is} = 1kHz$ sine wave					0.4	%			
BW	-3-dB cutoff frequency (switch on)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$					40	MHz			
OISO	-50-dB feedthrough frequency (switch off)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$					1.25	MHz			
I_{is}	Input/Output Leakage Current (switch off)	$V_{DD} = 18V$ $V_C = 0V$ $V_{is} = 18V$, $V_{os} = 0V$ $V_{is} = 0V$, $V_{os} = 18V$	$T_A = -55^\circ C$			-0.1	0.1	μA			
			$T_A = -40^\circ C$			-0.1	0.1				
			$T_A = 25^\circ C$			0.000	1				
			$T_A = 85^\circ C$			-1	1				
			$T_A = 125^\circ C$			-1	1				
XTALK	-50-dB crosstalk frequency	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k\Omega$					0.9	MHz			

4.5 Electrical Characteristics (continued)

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT			
t_{pd}	Propagation delay	$V_C = V_{DD}$, $V_{SS} = GND$ $V_{IS} = \text{Square Wave 0 to } V_{DD}$, $C_L = 50pF$, $R_L = 200k\Omega$			$V_{DD} = 5V$			40 100			
		$V_{DD} = 10V$			20 40						
		$V_{DD} = 15V$			15 30						
C_{IS}	Input capacitance	$V_{DD} = 5V$, $VC = V_{SS} = -5V$			4			pF			
C_{OS}	Output capacitance	$V_{DD} = 5V$, $VC = V_{SS} = -5V$			4			pF			
C_{IOS}	Feed through	$V_{DD} = 5V$, $VC = V_{SS} = -5V$			0.2			pF			
V_{ILC}	Control input, low voltage (max)	$ I_{IS} < 10\mu A$, $V_{IS} = V_{SS}$, $V_{OS} = V_{DD}$, and $V_{IS} = V_{DD}$, $V_{OS} = V_{SS}$	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	$T_A = -55^\circ C$ $T_A = -40^\circ C$ $T_A = 25^\circ C$ $T_A = 85^\circ C$ $T_A = 125^\circ C$	0.9			V			
					0.9						
					0.7						
					0.4						
					0.4						
V_{IHC}	Control input, high voltage	See Figure 10	$V_{DD} = 5V$			3.5			V		
			$V_{DD} = 10V$			7			V		
			$V_{DD} = 15V$			11			V		
I_{IH}	Input High Leakage	$V_{DD} = 18V$			0.5			μA			
I_{IL}	Input Low Leakage	$V_{DD} = 18V$			-1 -0.1			μA			
	Crosstalk (control input to signal output)	$V_C = 10V$ (square wave), $t_r, t_f = 20ns$, $R_L = 10k\Omega$ $V_{DD} = 10V$	$V_{DD} = 10V$			50			mV		
	Turn-on propagation delay	$t_r, t_f = 20ns$ $C_L = 50pF$, $R_L = 1k\Omega$	$V_{DD} = 5V$			35 70			ns		
			$V_{DD} = 10V$			20 40			ns		
			$V_{DD} = 15V$			15 30			ns		
	Maximum control input repetition rate	$V_{IN} = V_{DD}$, $C_L = 50pF$, $R_L = 1k\Omega$ $V_C = 10V$ (square wave centered on 5V), $t_r, t_f = 20ns$, $V_{os} = 1/2V_{os}$ at 1kHz	$V_{DD} = 10V$			10			MHz		
C_{IN}	Input Capacitance				5 7.5			pF			

4.5 Electrical Characteristics (continued)

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I _{IS}	Switch input current	$V_{DD} = 5V$ $V_{is} = 0V$	$T_A = -55^\circ C$				0.25	mA
			$T_A = -40^\circ C$				0.2	
			$T_A = 25^\circ C$				0.2	
			$T_A = 85^\circ C$				0.12	
			$T_A = 125^\circ C$				0.14	
		$V_{DD} = 5V$ $V_{is} = 5V$	$T_A = -55^\circ C$				-0.25	mA
			$T_A = -40^\circ C$				-0.2	
			$T_A = 25^\circ C$				-0.2	
			$T_A = 85^\circ C$				-0.12	
			$T_A = 125^\circ C$				-0.14	
		$V_{DD} = 10V$ $V_{is} = 0V$	$T_A = -55^\circ C$				0.62	mA
			$T_A = -40^\circ C$				0.5	
			$T_A = 25^\circ C$				0.5	
			$T_A = 85^\circ C$				0.3	
			$T_A = 125^\circ C$				0.35	
		$V_{DD} = 10V$ $V_{is} = 10V$	$T_A = -55^\circ C$				-0.62	mA
			$T_A = -40^\circ C$				-0.5	
			$T_A = 25^\circ C$				-0.5	
			$T_A = 85^\circ C$				-0.3	
			$T_A = 125^\circ C$				-0.35	
		$V_{DD} = 15V$ $V_{is} = 0V$	$T_A = -55^\circ C$				1.8	mA
			$T_A = -40^\circ C$				1.4	
			$T_A = 25^\circ C$				1.5	
			$T_A = 85^\circ C$				1	
			$T_A = 125^\circ C$				1.1	
		$V_{DD} = 15V$ $V_{is} = 15V$	$T_A = -55^\circ C$				-1.8	mA
			$T_A = -40^\circ C$				-1.4	
			$T_A = 25^\circ C$				-1.5	
			$T_A = 85^\circ C$				-1	
			$T_A = 125^\circ C$				-1.1	
V _{OS}	Switch output voltage	$V_{DD} = 5V$ $V_{is} = 0V$					0.4	V
		$V_{DD} = 5V$ $V_{is} = 5V$					4.6	V
		$V_{DD} = 10V$ $V_{is} = 0V$					0.5	V
		$V_{DD} = 10V$ $V_{is} = 10V$					9.5	V
		$V_{DD} = 15V$ $V_{is} = 0V$					1.5	V
		$V_{DD} = 15V$ $V_{is} = 15V$					13.5	V

(1) Peak-to-Peak voltage symmetrical about $(V_{DD} - V_{EE}) / 2$.

4.6 Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS		
		V _{IN} (V)	V _{DD} (V)	+25				+25				
				-55	-40	+85	+125	TYP	MAX			
Quiescent Device Current, I _{DD}		0,5	5	025	0.25	7.5	7.5	0.01	0.25	μA		
		0,10	10	0.5	0.5	15	15	0.01	0.5			
		0,15	15	1	1	30	30	0.01	1			
		0,20	20	5	5	150	150	0.02	5			
Signal Inputs (V _{is}) and Output (V _{os})												
On-State Resistance, r _{on} MAX	V _C =V _{DD} R _L =10kΩ Returned to <u>V_{DD}–V_{SS}</u> 2	V _{is} =V _{DD} or V _{SS}	10	600	610	840	960	–	660	Ω		
		V _{is} =4.75 to 5.75V	10	1870	1900	2380	2600	–	2000			
		V _{is} =V _{DD} or V _{SS}	15	360	370	520	600	–	400			
		V _{is} =7.25 to 7.75V	15	775	790	1080	1230	–	850			
ΔOn-State Resistance Between Any 2 Switches, Δr _{on}	R _L =10kΩ, V _C = V _{DD}	5	–	–	–	–	–	15	–	Ω		
		10	–	–	–	–	–	10	–			
		15	–	–	–	–	–	5	–			
Total Harmonic Distortion, THD	V _C =V _{DD} =5V, V _{SS} = -5V, V _{is(p-p)} = 5V (Sine wave centered on 0V) R _L = 10kΩ, f _{is} = 1kHz sine wave	–	–	–	–	–	0.4	–	%			
-3dB Cutoff Frequency (Switch on)	V _C =V _{DD} =5V, V _{SS} =-5V, V _{is(p-p)} (Sine wave centered on 0V) R _L =1kΩ,	–	–	–	–	–	40	–	MHz			
-50dB Feed-through Frequency (Switch off)	V _C =V _{SS} = -5V, V _{is(p-p)} =5V (Sine wave centered on 0V) R _L = 1 kΩ	–	–	–	–	–	1.25	–	MHz			
Input/Output Leakage Current (Switch off) I _{is} MAX	V _C = 0V V _{is} = 18V, V _{OS} = 0V; V _{is} = 0V, V _{OS} = 18V	18	±0.1	±0.1	±1	±1	10 ⁻⁴	±0.1	μA			
-50dB Crosstalk Frequency	V _{C(A)} = V _{DD} = +5V, V _{C(B)} = V _{SS} = -5V, V _{is(A)} = 5V _{p-p} , 50Ω source R _L = 1kΩ	–	–	–	–	–	0.9	–	MHz			
Propagation Delay (Signal Input to Signal Output) t _{pd}	R _L = 200kΩ V _C = V _{DD} , V _{SS} = GND, C _L = 50pF V _{is} = Square Wave 0 to V _{DD} t _r , t _f = 20ns	5	–	–	–	–	40	100	ns			
		10	–	–	–	–	20	40				
		15	–	–	–	–	15	30				
Capacitance: Input, C _{is} Output, C _{os} Feed-through, C _{ios}	V _{DD} = +5V V _C =V _{SS} =-5V	–	–	–	–	–	4	–	pF			
		–	–	–	–	–	4	–				
		–	–	–	–	–	0.2	–				
Control (V _C)												
Control Input Low Voltage, V _{ILC} (MAX)	I _{is} <10 μA V _{is} = V _{SS} , V _{OS} = V _{DD} and V _{is} = V _{DD} , V _{OS} = V _{SS}	5,10, 15	0.9	0.9	0.4	0.4	–	0.7	V			
Control Input High Voltage, V _{ICH}	See Figure 4-8	5	3.5 (Min.)						V			
		10	7 (Min.)									
		15	11 (Min.)									
Input Current, I _{IN} (MAX)	Input Current, I _{IN} (MAX)V _{is} □ V _{DD} V _{DD} – V _{SS} = 18V V _{CC} □ V _{DD} – V _{SS}	18	±0.1	±0.1	±1	±1	±10 ⁻⁵	±0.1	μA			
			–	–	–	–	–	–				
			–	–	–	–	–	–				
Crosstalk (Control Input to Signal Output)	V _C = 10V (Sq. Wave) t _r , t _f = 20ns R _L = 10kΩ	10	–	–	–	–	50	–	mV			
			–	–	–	–	–	–				
			–	–	–	–	–	–				
Turn-On Propagation Delay	Turn-On Propagation Delay t _r , t _f = 20ns C _L = 50pF R _L = 1kΩ	5	–	–	–	–	35	70	ns			
		10	–	–	–	–	20	40				
		15	–	–	–	–	15	30				

4.6 Electrical Characteristics (continued)

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
			V _{IN} (V)	V _{DD} (V)	-55			+25			
					-40	+85	+125	TYP	MAX		
Maximum Control Input Repetition Rate	Maximum Control Input Repetition Rate V _{IS} = V _{DD} < V _{SS} = GND, R _L = 1kΩ to GND, C _L = 50pF, V _C = 10V(Square wave centered on 5V) t _r , t _f = 20ns, V _{OS} = ½ V _{DD} at 1kHz	10	—	—	—	—	—	10	—	MHz	
Input Capacitance, C _{IN}			—	—	—	—	—	5	7.5	μF	

4.7 Typical Characteristics

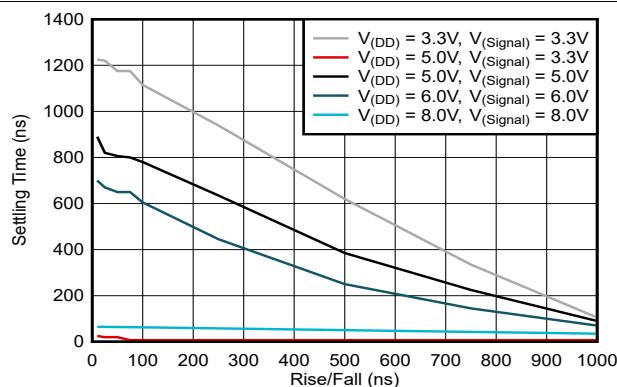


Figure 4-1. System Settling Time vs Signal Rise/Fall Time

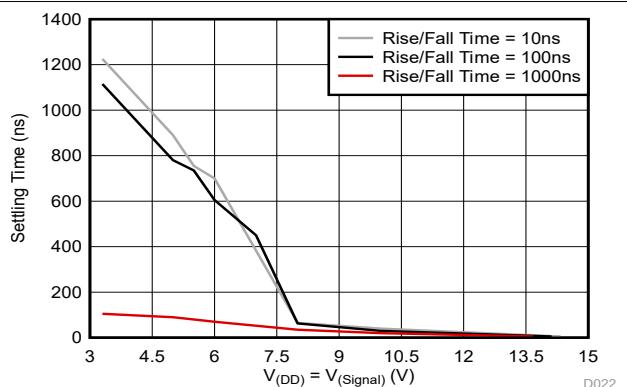


Figure 4-2. System Settling Time vs Signal Voltage

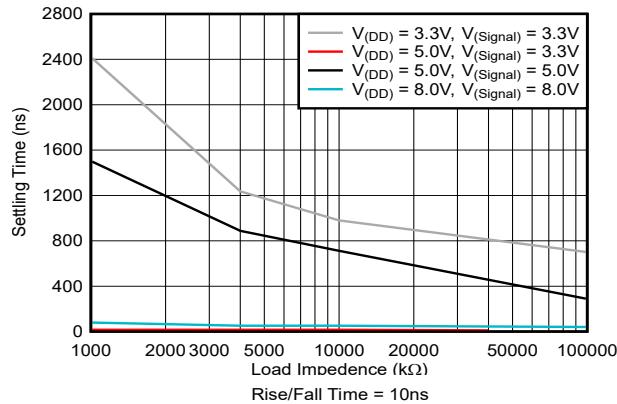


Figure 4-3. System Settling Time vs Signal Voltage

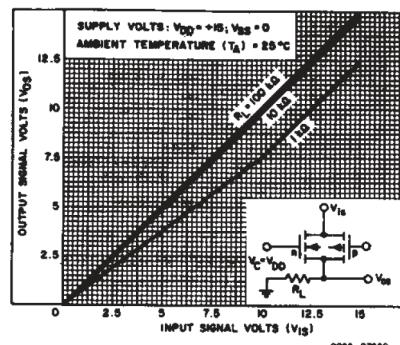


Figure 4-4. On-state Characteristics for 1 of 4 Switches with V_{DD} = +15V, V_{SS} = 0V.

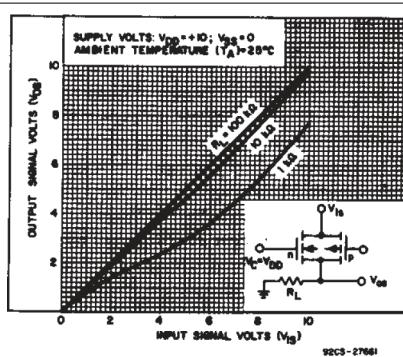


Figure 4-5. On-state Characteristics for 1 of 4 Switches with V_{DD} = +10V, V_{SS} = 0V.

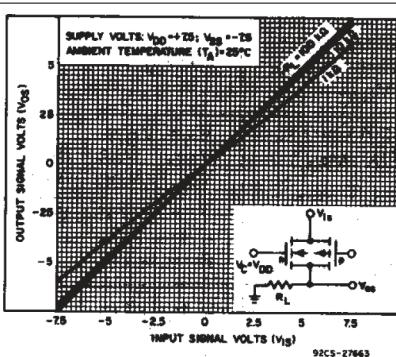


Figure 4-6. On-state Characteristics for 1 of 4 Switches with V_{DD} = +7.5V, V_{SS} = -7.5V.

4.7 Typical Characteristics (continued)

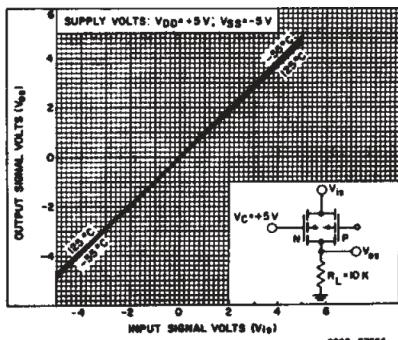


Figure 4-7. On-state Characteristics as a Function of Temp. for 1 of 4 Switches with $v_{DD} = +5V$, $v_{SS} = -5V$.

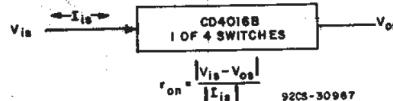


Figure 4-8. Determination of R_{on} As a Test Condition for Control Input High Voltage Specification.

5 Parameter Measurement Information

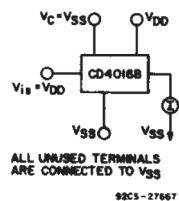


Figure 5-1. Off-state Switch Input or Output Leakage Current Test Circuit.

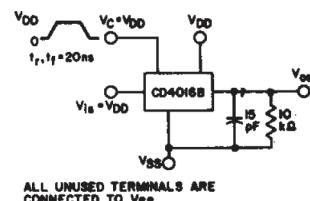


Figure 5-2. Test Circuit for Square-wave Response.

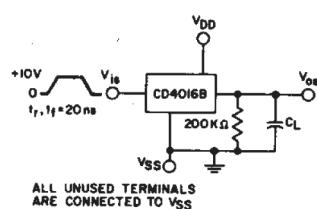


Figure 5-3. Propagation Delay Time Signal Input (v_{iS}) To Signal Output (v_{os})

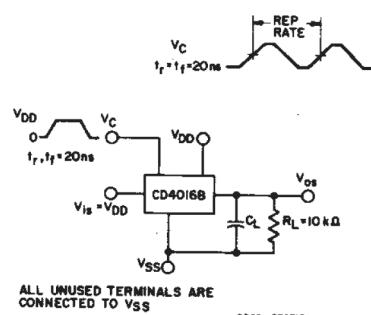
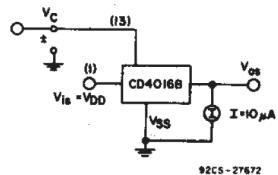
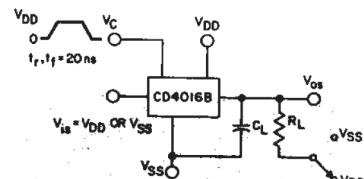


Figure 5-4. MAX Control-input Repetition Rate.



SWITCH THRESHOLD VOLTAGE IS DEFINED AS THE VOLTAGE APPLIED TO A TRANSMISSION GATE CONTROL WHICH CAUSES $10\mu A$ OF TRANSMISSION GATE CURRENT.

Figure 5-5. Switch Threshold Voltage.



ALL UNUSED TERMINALS ARE CONNECTED TO VSS.

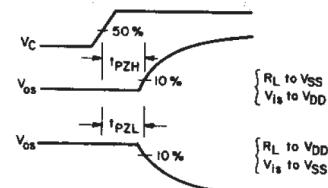


Figure 5-6. Turn-On Propagation Delay-control Input.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Documentation Support

6.1.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.1.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

6.1.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

6.1.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.1.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2024) to Revision E (August 2024)	Page
• Added Settling Time plots.....	10

Changes from Revision C (September 2003) to Revision D (May 2024)	Page
• Increased IDD max/typ for the lower Temperature cases.....	5
• Changed typical IIH to 0.5µA.....	5
• Changed typical IIL to -0.1µA.....	5

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9064001CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A
CD4016BE	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4016BE
CD4016BE.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4016BE
CD4016BEE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4016BE
CD4016BF	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4016BF
CD4016BF.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4016BF
CD4016BF3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A
CD4016BF3A.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A
CD4016BM	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	CD4016BM
CD4016BM96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM
CD4016BM96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM
CD4016BMT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	CD4016BM
CD4016BNSR	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016B
CD4016BNSR.A	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016B
CD4016BPW	NRND	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B
CD4016BPW.A	NRND	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B
CD4016BPWR	NRND	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B
CD4016BPWR.A	NRND	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

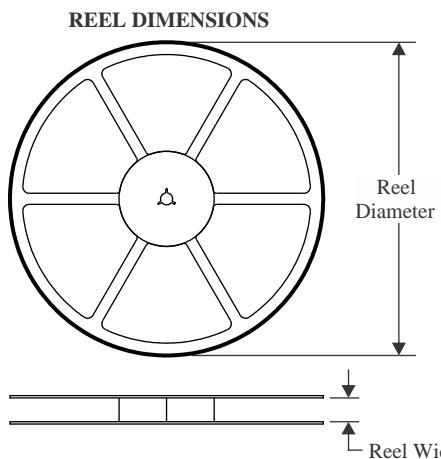
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4016B, CD4016B-MIL :

- Catalog : [CD4016B](#)
- Military : [CD4016B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4016BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4016BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4016BM96	SOIC	D	14	2500	353.0	353.0	32.0
CD4016BNSR	SOP	NS	14	2000	353.0	353.0	32.0
CD4016BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

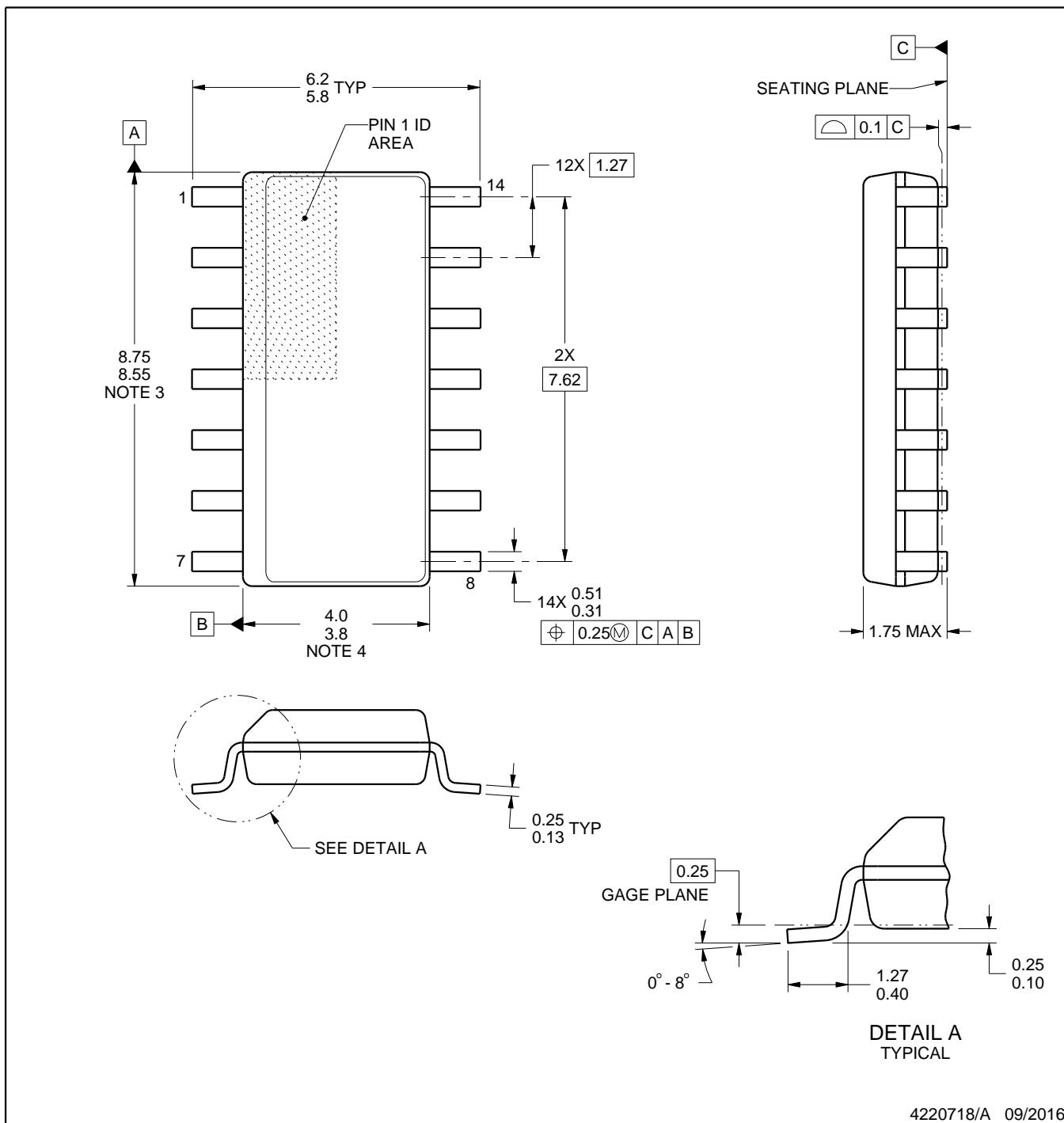
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
CD4016BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BPW	PW	TSSOP	14	90	530	10.2	3600	3.5
CD4016BPW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

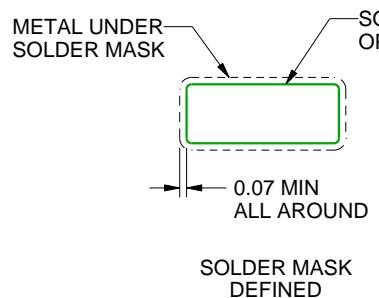
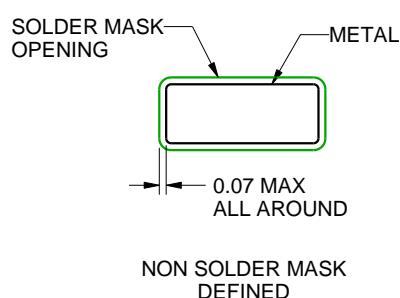
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

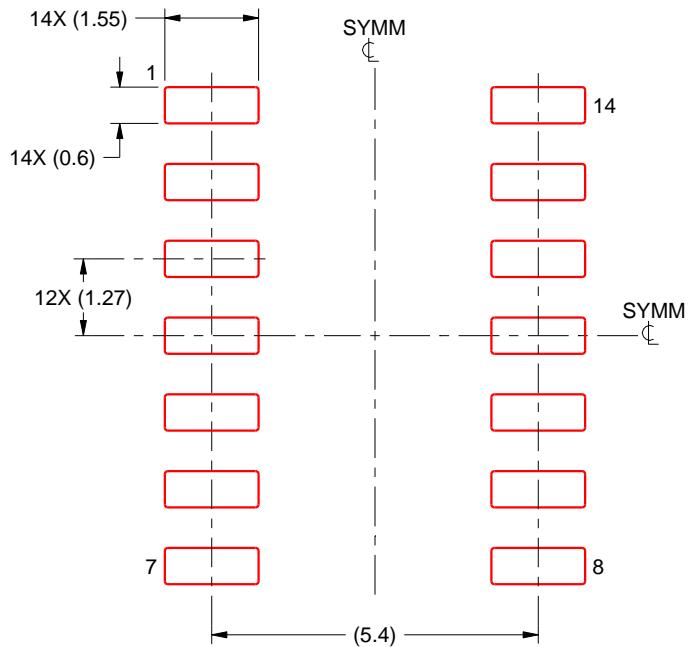
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

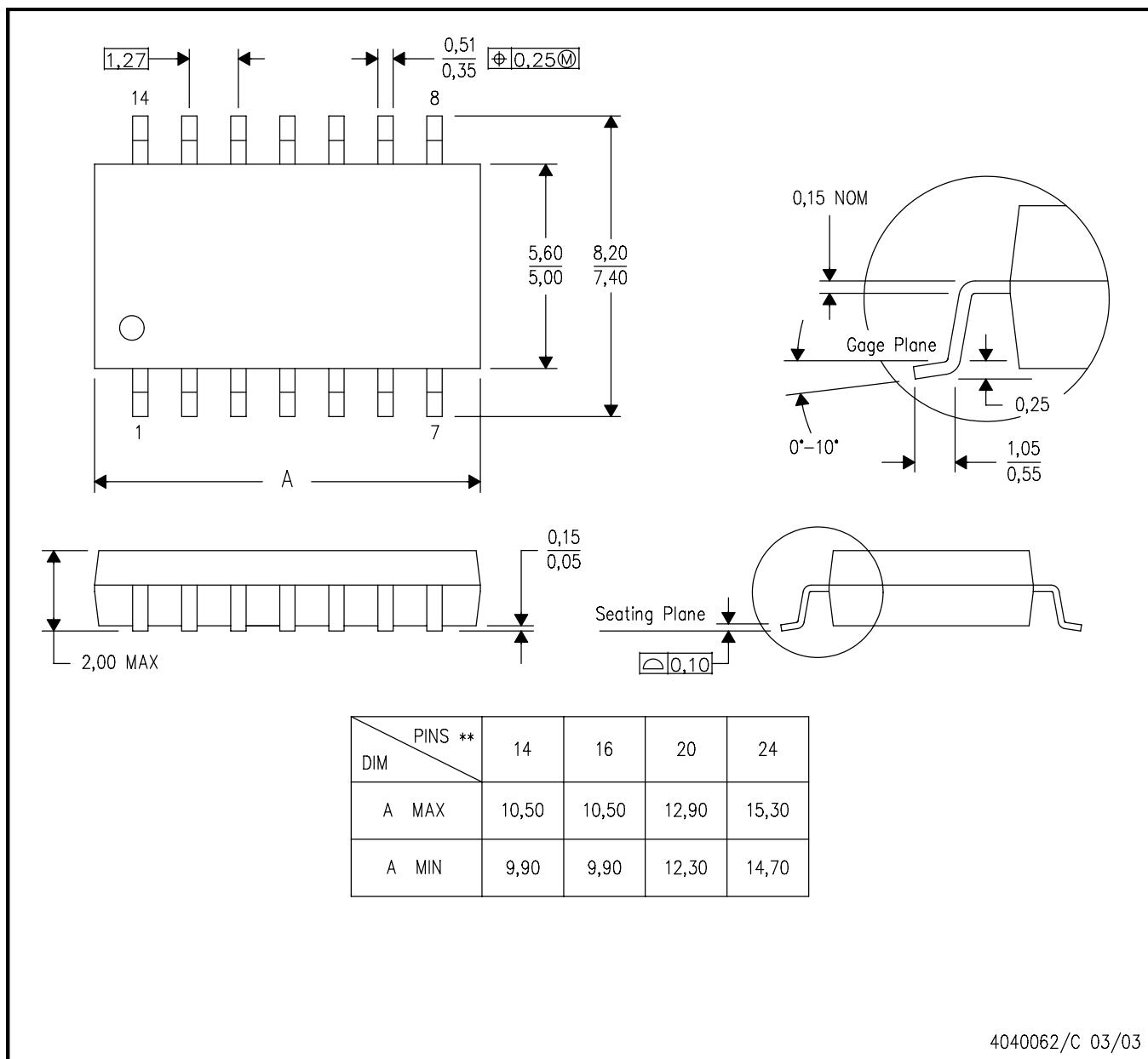
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

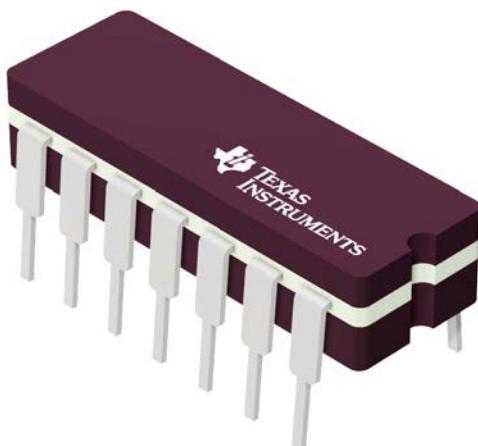
4040062/C 03/03

GENERIC PACKAGE VIEW

J 14

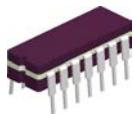
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

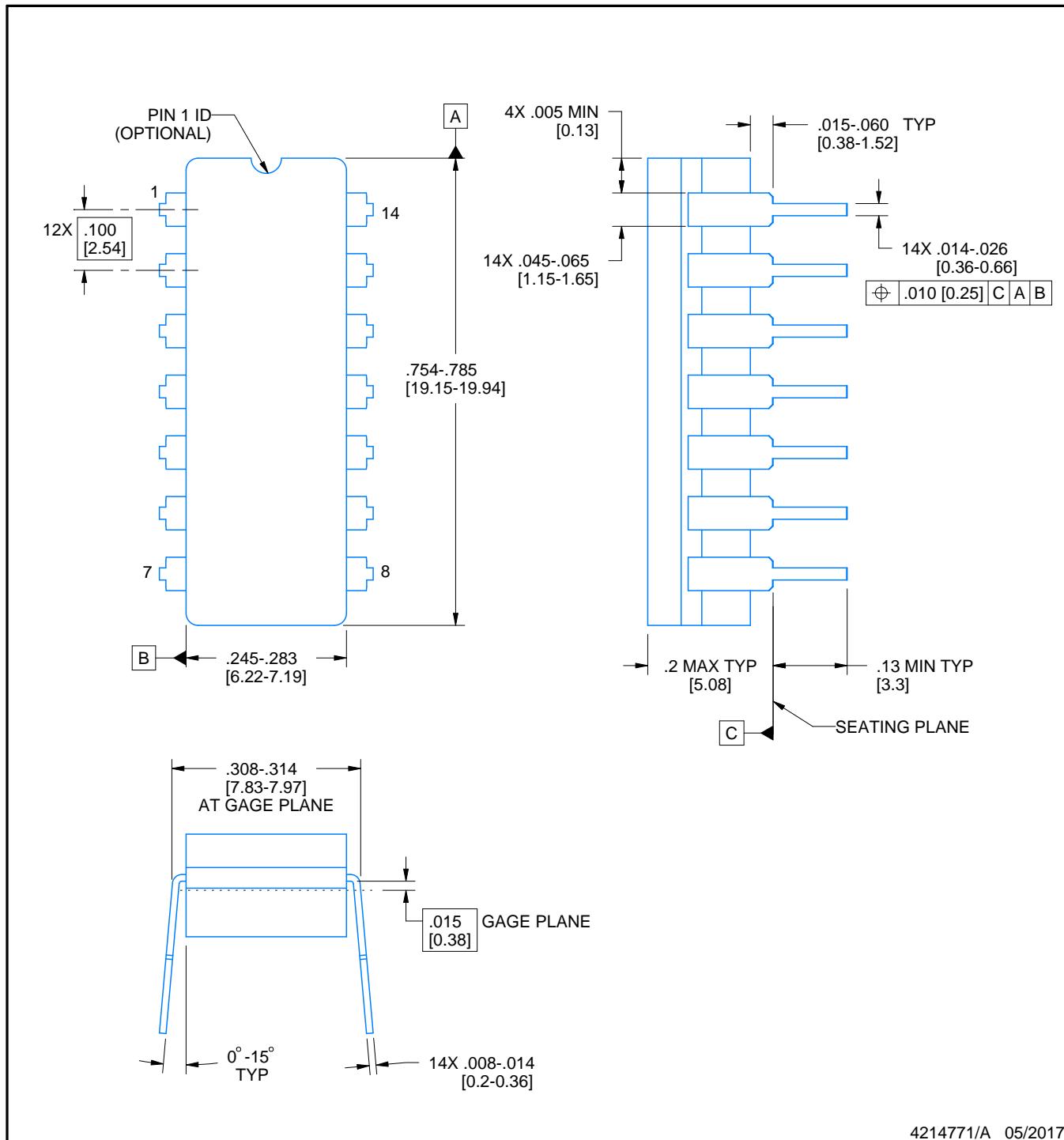


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

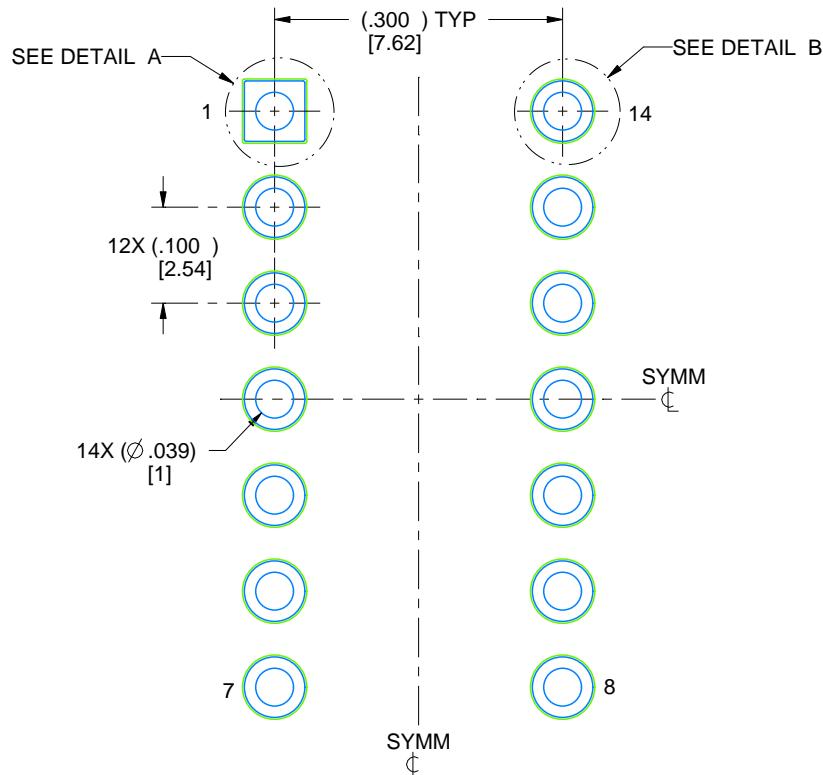
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

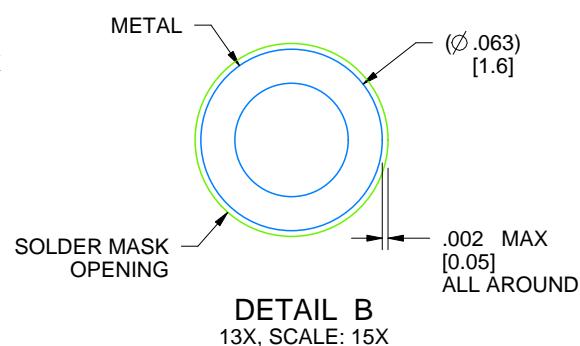
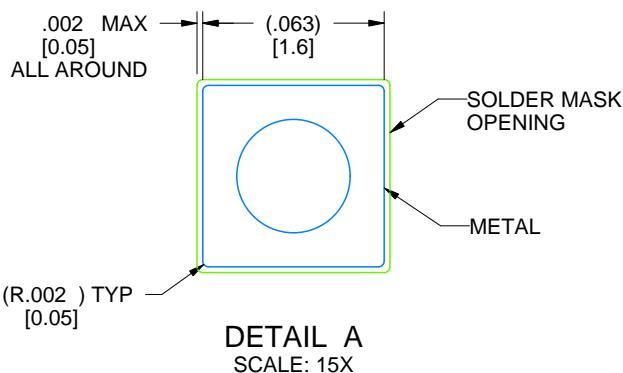
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

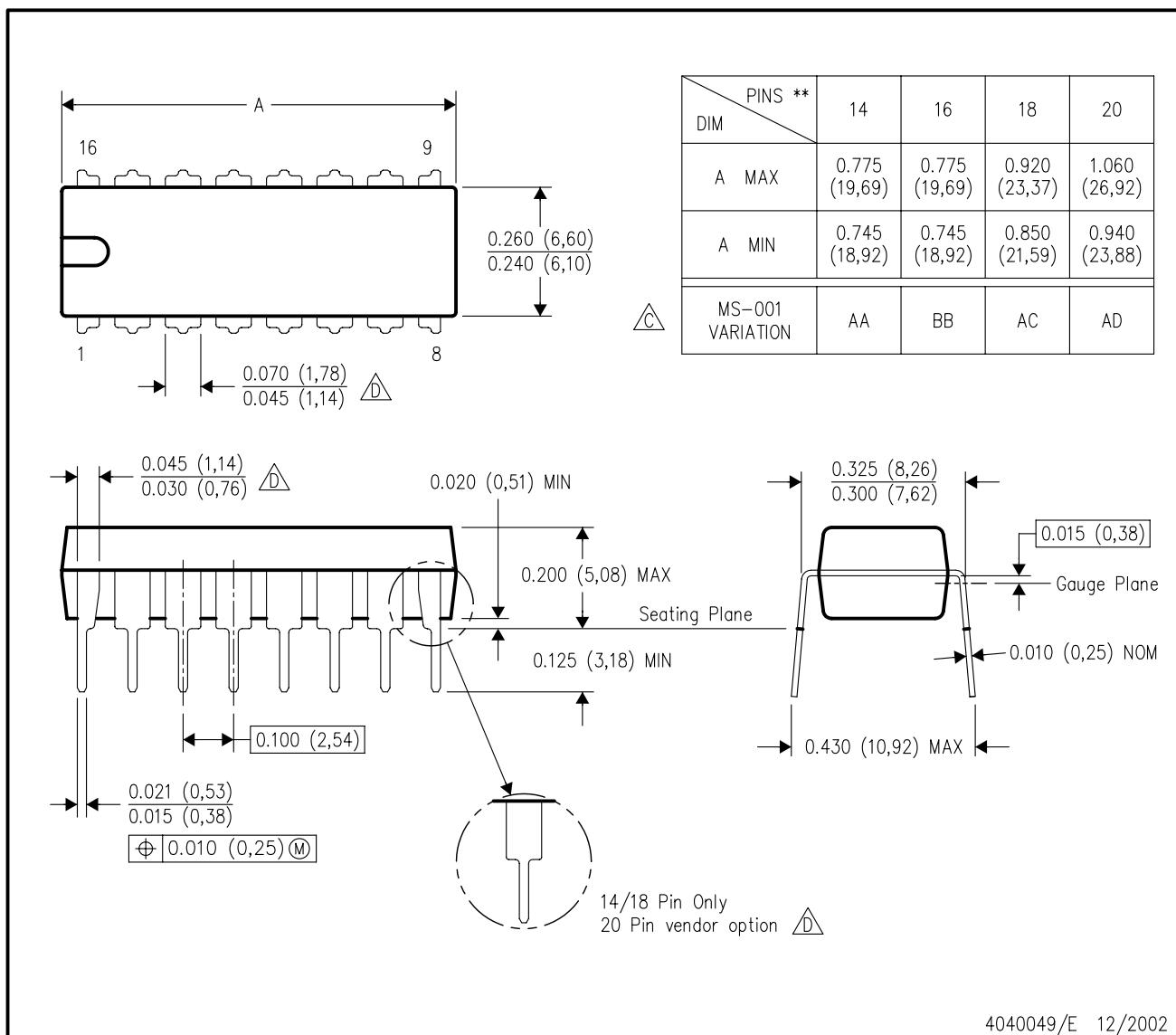


4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



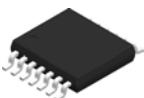
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

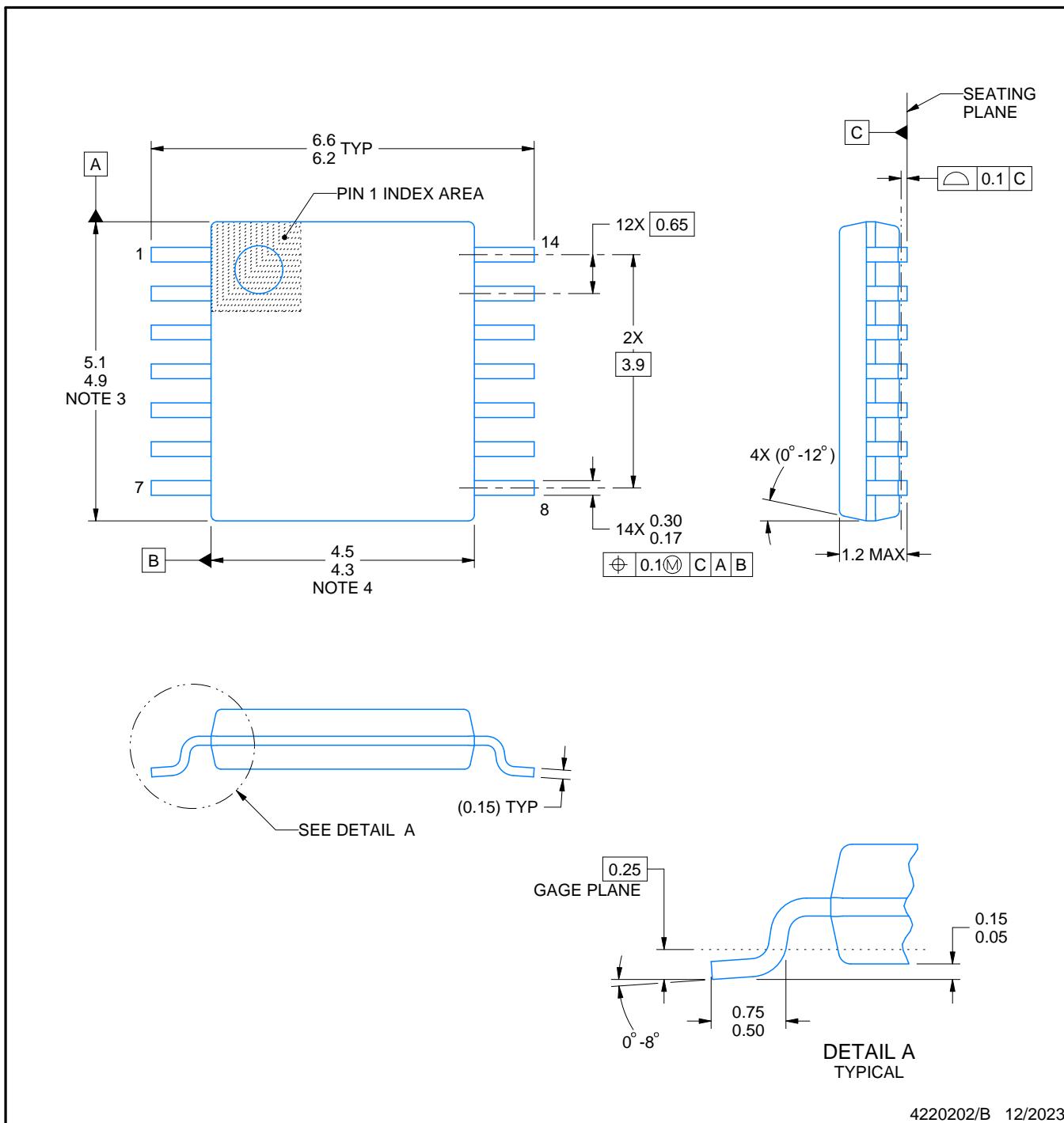
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

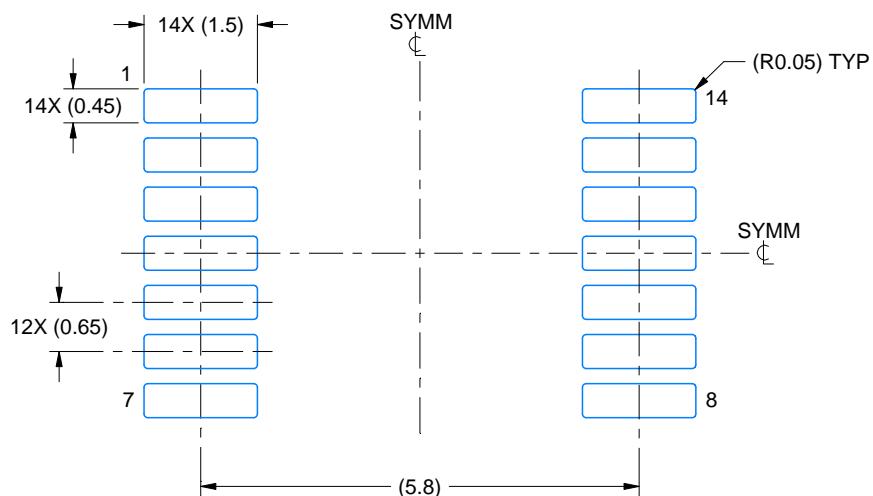
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

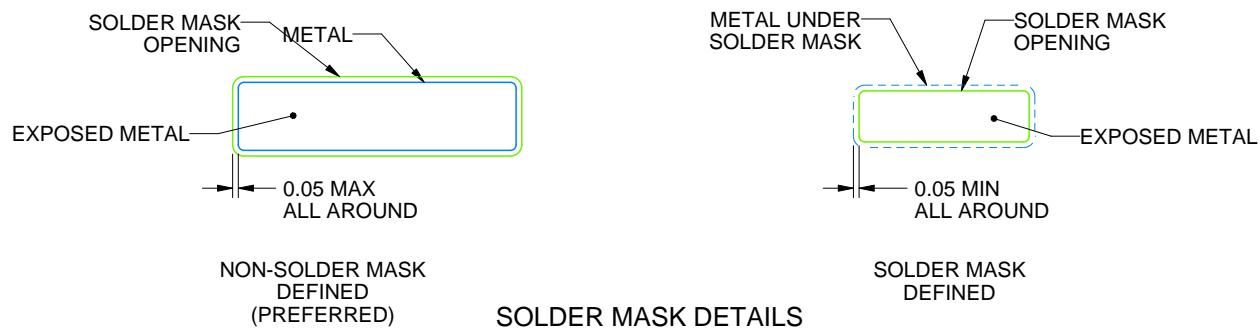
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

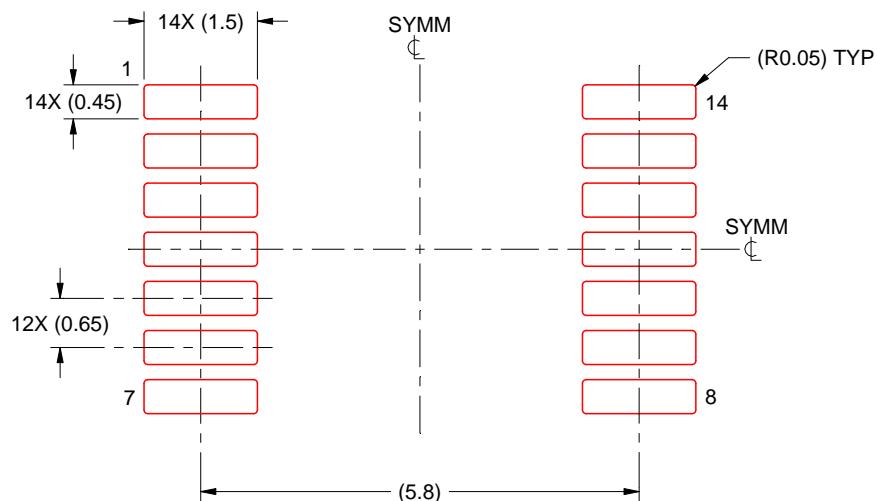
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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