

CD405xB CMOS Single 8-Channel Analog Multiplexer or Demultiplexer With Logic-Level Conversion

1 Features

- Wide range of digital and analog signal levels:
 - Digital: 3V to 20V
 - Analog: $\leq 20V_{P-P}$
- Single supply range : 3V to 20V (performance degrades for $V_{DD} < 3V$)
- Dual Supply range: $\pm 3V$ to $\pm 10V$
- Low ON resistance, 125 Ω (typical) over input range for $V_{DD} = 15V$
- Low channel leakage of $\pm 10pA$ (typical) at $V_{DD} = 15V$
- Low quiescent power dissipation : 0.2 μW (typical)
- Bidirectional signal path
- ESD protection HBM: 3000V, CDM: 2000V
- Pin compatible with industry standard 4051

2 Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- [Factory automation](#)
- [Televisions](#)
- [Appliances](#)
- [Consumer audio](#)
- Programmable logic circuits
- [Sensors](#)

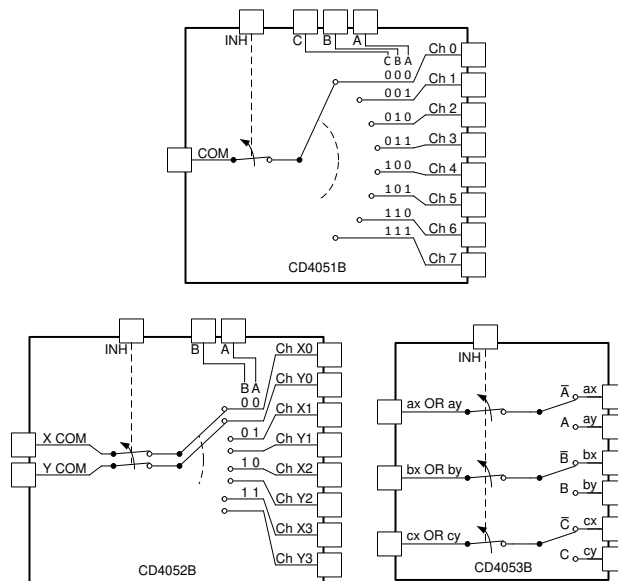
3 Description

The CD405xB analog multiplexers and demultiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
CD405xB	J (CDIP, 16)	19.50mm × 6.92mm
	N (PDIP, 16)	19.3mm × 9.4mm
	D (SOIC, 16)	9.9mm × 3.9mm
	NS (SOP, 16)	10.2mm × 7.8mm
	PW (TSSOP, 16)	5mm × 6.4mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Diagrams of CD4051B



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4 Pin Configuration and Functions

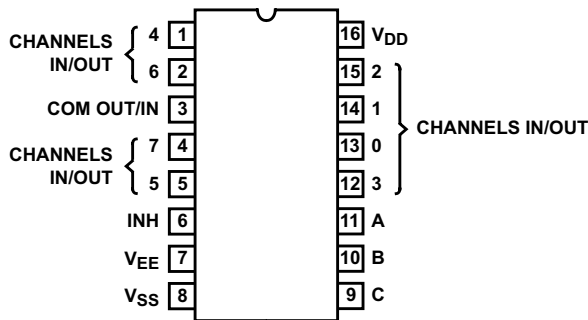


Figure 4-1. CD4051B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP (Top View)

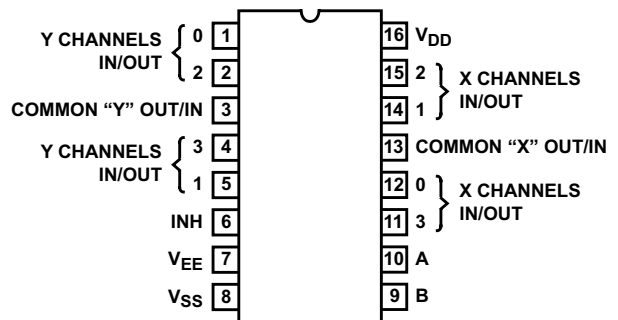


Figure 4-2. CD4052B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP (Top View)

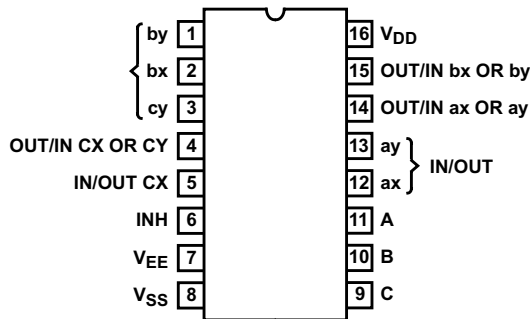


Figure 4-3. CD4053B E, M, NS, and PW Package, 16-Pin PDIP, CDIP, SOIC, SOP, and TSSOP (Top View)

Table 4-1. Pin Functions CD4051B

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	CH 4 IN/OUT	I/O	Channel 4 in/out
2	CH 6 IN/OUT	I/O	Channel 6 in/out
3	COM OUT/IN	I/O	Common out/in
4	CH 7 IN/OUT	I/O	Channel 7 in/out
5	CH 5 IN/OUT	I/O	Channel 5 in/out
6	INH	I	Disables all channels. See Table 7-1 .
7	V _{EE}	—	Negative power input
8	V _{SS}	—	Ground
9	C	I	Channel select C. See Table 7-1 .
10	B	I	Channel select B. See Table 7-1 .
11	A	I	Channel select A. See Table 7-1 .
12	CH 3 IN/OUT	I/O	Channel 3 in/out
13	CH 0 IN/OUT	I/O	Channel 0 in/out
14	CH 1 IN/OUT	I/O	Channel 1 in/out
15	CH 2 IN/OUT	I/O	Channel 2 in/out
16	V _{DD}	—	Positive power input

(1) I = input, O = output

Table 4-2. Pin Functions CD4052B

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	Y CH 0 IN/OUT	I/O	Channel Y0 in/out
2	Y CH 2 IN/OUT	I/O	Channel Y2 in/out
3	Y COM OUT/IN	I/O	Y common out/in
4	Y CH 3 IN/OUT	I/O	Channel Y3 in/out
5	Y CH 1 IN/OUT	I/O	Channel Y1 in/out
6	INH	I	Disables all channels. See Table 7-1 .
7	V _{EE}	—	Negative power input
8	V _{SS}	—	Ground
9	B	I	Channel select B. See Table 7-1 .
10	A	I	Channel select A. See Table 7-1 .
11	X CH 3 IN/OUT	I/O	Channel X3 in/out
12	X CH 0 IN/OUT	I/O	Channel X0 in/out
13	X COM IN/OUT	I/O	X common out/in
14	X CH 1 IN/OUT	I/O	Channel in/out
15	X CH 2 IN/OUT	I/O	Channel in/out
16	V _{DD}	—	Positive power input

(1) I = input, O = output

Table 4-3. Pin Functions CD4053B

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	BY IN/OUT	I/O	B channel Y in/out
2	BX IN/OUT	I/O	B channel X in/out
3	CY IN/OUT	I/O	C channel Y in/out
4	CX OR CY OUT/IN	I/O	C common out/in
5	CX IN/OUT	I/O	C channel X in/out
6	INH	I	Disables all channels. See Table 7-1 .
7	V _{EE}	—	Negative power input
8	V _{SS}	—	Ground
9	C	I	Channel select C. See Table 7-1 .
10	B	I	Channel select B. See Table 7-1 .
11	A	I	Channel select A. See Table 7-1 .
12	AX IN/OUT	I/O	A channel X in/out
13	AY IN/OUT	I/O	A channel Y in/out
14	AX OR AY OUT/IN	I/O	A common out/in
15	BX OR BY OUT/IN	I/O	B common out/in
16	V _{DD}	—	Positive power input

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT		
	Supply Voltage	V+ to V-, Voltages Referenced to V _{SS} Terminal	-0.5	20	V	
	DC Input Voltage		-0.5	V _{DD} +0.5	V	
	DC Input Current	Any One Input	-10	10	mA	
T _{JMAX1}	Maximum junction temperature, ceramic package			175	°C	
T _{JMAX2}	Maximum junction temperature, plastic package			150	°C	
T _{stg}	Storage temperature			-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature Range		-55		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CD405x				UNIT
		E (PDIP)	M (SOIC)	NS (SOP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	67	73	64	116.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS					MIN	TYP	MAX	UNIT	
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})										
	V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	TEMP					
Quiescent Device Current, I_{DD} Max		0V	0V	5V	-55°C			60	μA	
					-40°C			60		
					25°C		17	60		
					85°C			150		
					125°C			150		
		0V	0V	10V		-55°C				60
						-40°C				60
						25°C		18		60
						85°C				300
						125°C				300
		0V	0V	15V		-55°C				60
						-40°C				60
						25°C		18		60
						85°C				600
						125°C				600
		0V	0V	20V		-55°C				100
						-40°C				100
						25°C		18		100
						85°C				3000
						125°C				3000
Drain to Source ON Resistance r_{ON} Max $0 \leq V_{IS} \leq V_{DD}$		0V	0V	5V	-55°C			800	Ω	
					-40°C			850		
					25°C		470	1050		
					85°C			1200		
					125°C			1300		
		0V	0V	10V		-55°C				310
						-40°C				300
						25°C		180		400
						85°C				520
						125°C				550
		0V	0	15V		-55°C				200
						-40°C				210
						25°C		125		240
						85°C				300
						125°C				300
Change in ON Resistance (Between Any Two Channels), ΔR_{ON}		0V	0V	5V	25°C		15	Ω		
		0V	0V	10V		10				
		0V	0V	15V		5				

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT			
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max)		0V	0V	18V	-55°C		± 100	nA				
					-40°C		± 100					
					25°C	± 0.3	± 100 ⁽²⁾					
					85°C		± 1000 ⁽²⁾					
					125°C		± 1000 ⁽²⁾					
ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max)		5 or 0	-5V	0V	10.5V	85°C	± 300	nA				
		5	0V	0V	18V	85°C	± 300					
Capacitance	Input, C_{IS}	0V	0V	10V	25°C	5		pF				
	Output, C_{OS}					CD4051	30					
	Output, C_{OS}					CD4052	18					
	Output, C_{OS}					CD4053	9					
	Feed through, C_{IOS}						0.2					
Prop Delay		V_{DD}	$R_L = 200k\Omega$		5V	25°C	30	60	ns			
			$C_L = 50pF$		10V		15	30				
			$t_r, t_f = 20ns$		15V		10	20				
CONTROL (ADDRESS OR INHIBIT), V_C												
Input Low Voltage, V_{IL} , Max									V			
										5V	-55°C	0.8
											-40°C	0.8
											25°C	0.8
											85°C	0.8
											125°C	0.8
										10V	-55°C	0.8
											-40°C	0.8
											25°C	0.8
											85°C	0.8
											125°C	0.8
										15V	-55°C	0.8
											-40°C	0.8
											25°C	0.8
											85°C	0.8
125°C	0.8											

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
Input High Voltage, V_{IH} , Min		5V		-55°C			3.5	V	
				-40°C			3.5		
				25°C			3.5		
				85°C			3.5		
				125°C			3.5		
		10V		-55°C			7		
				-40°C			7		
				25°C	7				
				85°C			7		
				125°C			7		
		15V		-55°C			11		
				-40°C			11		
				25°C	11				
				85°C			11		
				125°C			11		
Input current, I_{IN} (Max)		$V_{IN} = 0, 18$		18V		-55°C			±1
						-40°C			±1
						25°C	±0.6		±1
						85°C			±1
						125°C			±1
Propagation Delay Time	Address-to-Signal OUT (Channels ON or OFF) (See Figure 10, Figure 11, and Figure 15)	$t_r, t_f = 20ns,$ $C_L = 50pF,$ $R_L = 10k\Omega$	0V	0V	5V	450 720		ns	
			0V	0V	10V	160 320			
			0V	0V	15V	120 240			
			-5V	0V	5V	225 450			
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 11)	$t_r, t_f = 20ns,$ $C_L = 50pF,$ $R_L = 1k\Omega$	0V	0V	5V	400 720		ns	
			0V	0V	10V	160 320			
			0V	0V	15V	120 240			
			-10V	0V	5V	200 400			
Propagation Delay Time	Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 17)	$t_r, t_f = 20ns,$ $C_L = 50pF,$ $R_L = 10k\Omega$	0V	0V	5V	200 450		ns	
			0V	0V	10V	90 210			
			0V	0V	15V	70 160			
			-10V	0V	5V	130 300			
Input Capacitance, C_{IN} (Any Address or Inhibit Input)			-5V	0V	5V	25°C	5	7.5	pF

- (1) Peak-to-Peak voltage symmetrical about $(V_{DD} - V_{EE}) / 2$.
 (2) Determined by minimum feasible leakage measurement for automatic testing.

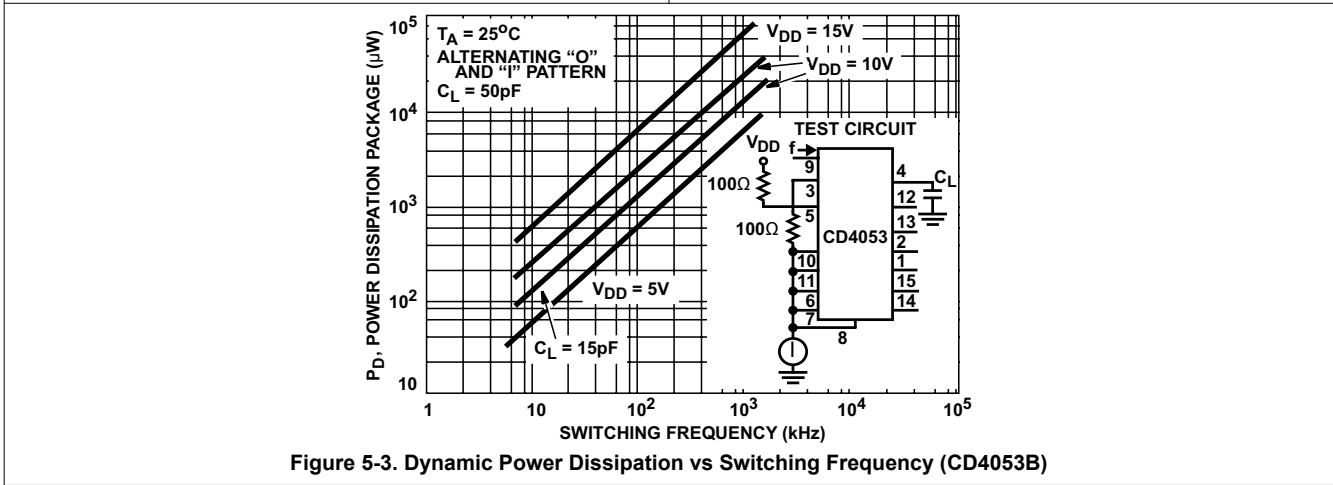
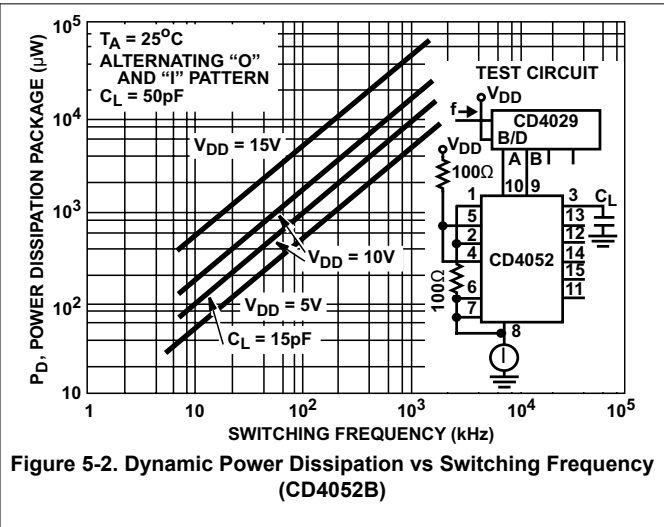
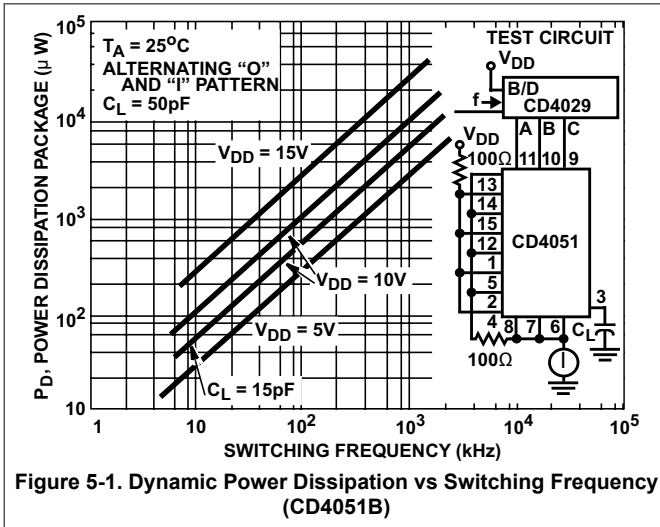
5.6 AC Performance Characteristics

$V_{DD} = +15V$, $V_{SS} = V_{EE} = 0V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP	UNIT		
	V_{IS} (V)	V_{DD} (V)	R_L (k Ω)				
Cutoff (–3dB) Frequency Channel ON (Sine Wave Input)	5 ⁽¹⁾	10	1	V_{OS} at Common OUT/IN	CD4053	30	MHz
		10	1		CD4052	25	
		10	1		CD4051	20	
	$V_{EE} = V_{SS}$, $20\text{Log}(V_{OS}/V_{IS}) = -3\text{dB}$			V_{OS} at Any Channel		60	
Total Harmonic Distortion, THD	2 ⁽¹⁾	5	10			0.3%	%
	3 ⁽¹⁾	10	10			0.2%	
	5 ⁽¹⁾	15	10			0.12%	
	$V_{EE} = V_{SS}$, $f_{IS} = 1\text{kHz}$ Sine Wave						
–40dB Feedthrough Frequency (All Channels OFF)	5 ⁽¹⁾	10	1	V_{OS} at Common OUT/IN	CD4053	8	MHz
					CD4052	10	
					CD4051	12	
	$V_{EE} = V_{SS}$, $20\text{Log}(V_{OS}/V_{IS}) = -40\text{dB}$			V_{OS} at Any Channel		8	
–40dB Signal Crosstalk Frequency	5 ⁽¹⁾	10	1			3	MHz
	$V_{EE} = V_{SS}$, $20\text{Log}(V_{OS}/V_{IS}) = -3\text{dB}$			Between Sections, CD4052 Only	Measured on Common	6	
					Measured on Any Channel	10	
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	
					In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to- Signal Crosstalk		10	10 ⁽²⁾			65	mV _{PEAK}
	$V_{EE} = 0$, $V_{SS} = 0$, t_r , $t_f = 20\text{ns}$, mV _{PEAK} $V_{CC} = V_{DD} - V_{SS}$ (Square Wave)					65	mV _{PEAK}

- (1) Peak-to-Peak voltage symmetrical about $(V_{DD} - V_{EE}) / 2$.
(2) Both ends of channel.

5.7 Typical Characteristics



6 Parameter Measurement Information

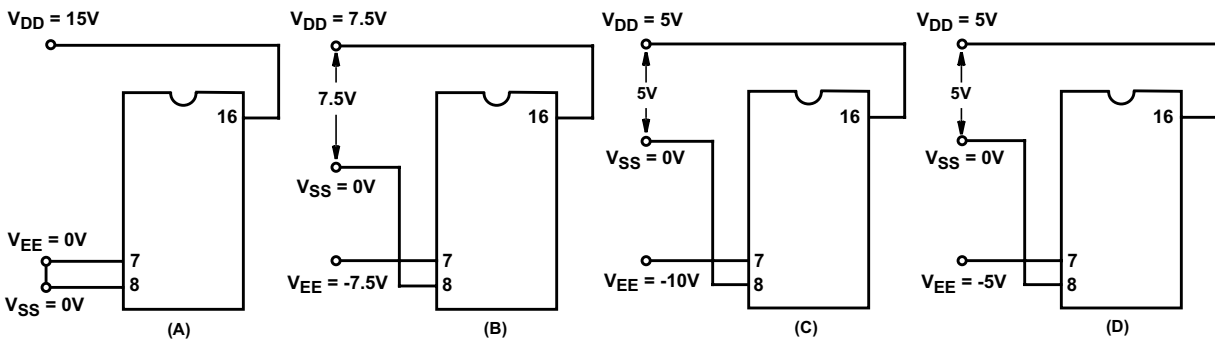


Figure 6-1. Typical Bias Voltages

Note

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 = V_{SS} and 1 = V_{DD} . The analog signal (through the TG) may swing from V_{EE} to V_{DD} .

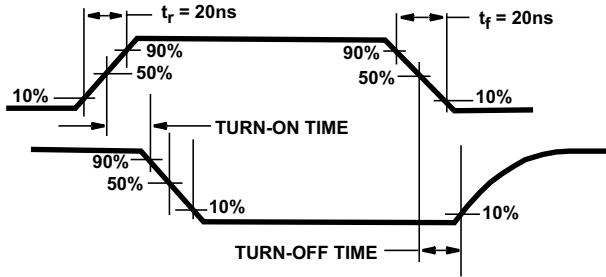


Figure 6-2. Waveforms, Channel Being Turned ON ($R_L = 1k\Omega$)

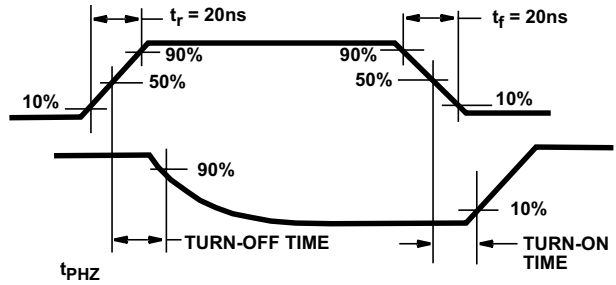


Figure 6-3. Waveforms, Channel Being Turned OFF ($R_L = 1k\Omega$)

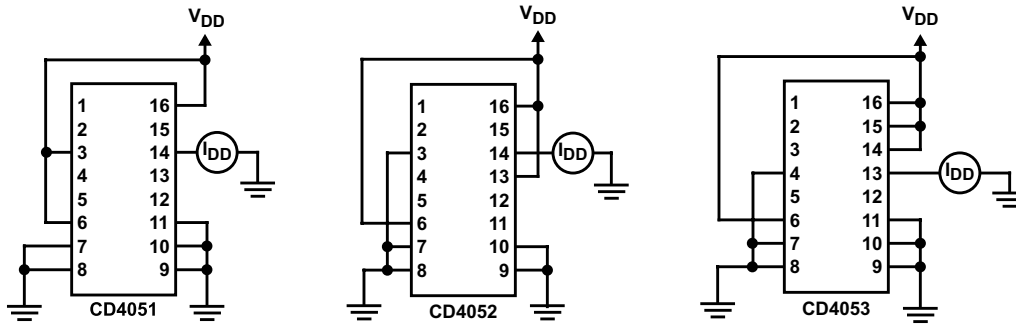
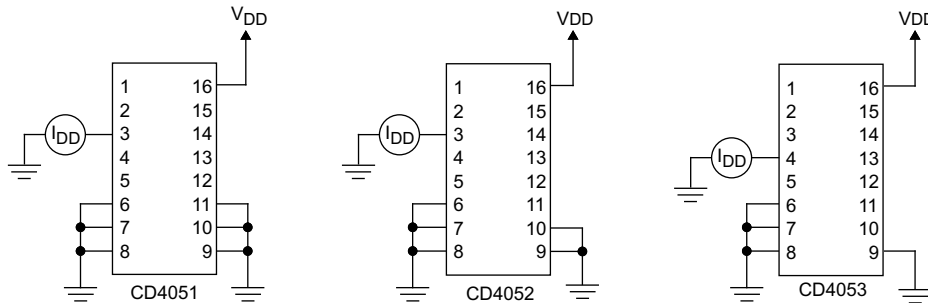


Figure 6-4. OFF Channel Leakage Current – Any Channel OFF



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Figure 6-5. On Channel Leakage Current – Any Channel On

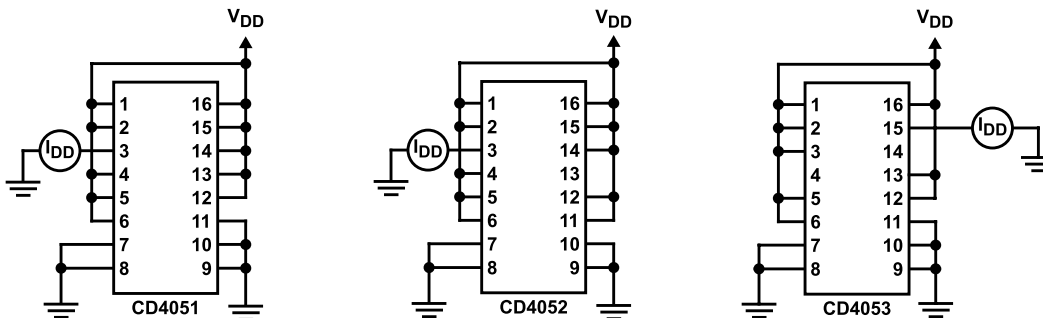


Figure 6-6. OFF Channel Leakage Current – All Channels OFF

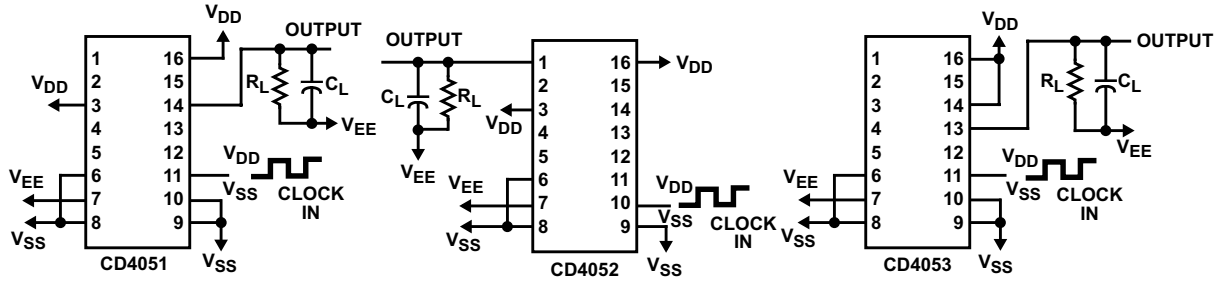


Figure 6-7. Propagation Delay – Address Input to Signal Output

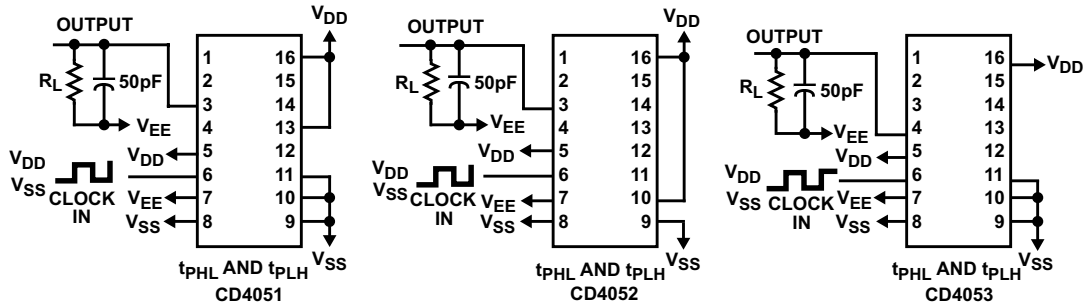


Figure 6-8. Propagation Delay – Inhibit Input to Signal Output

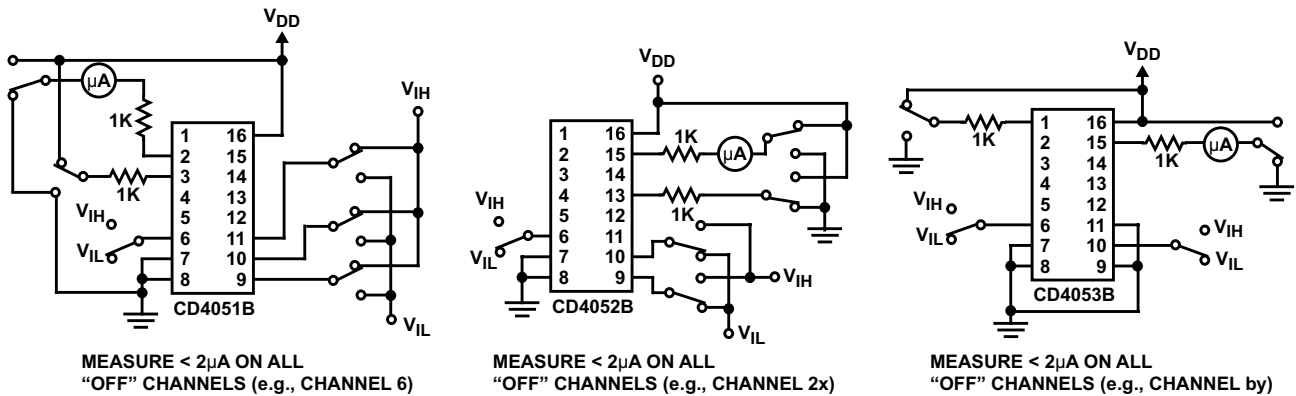


Figure 6-9. Input Voltage Test Circuits (Noise Immunity)

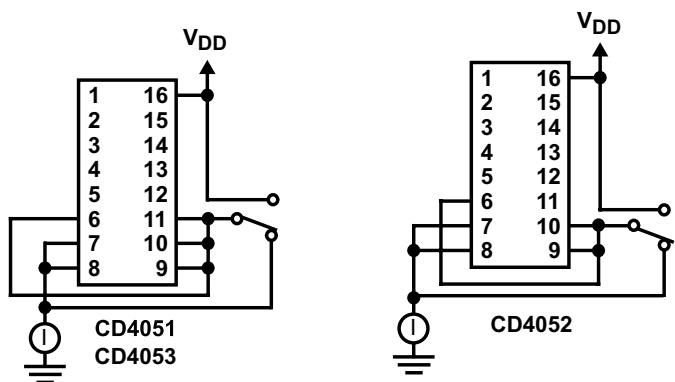


Figure 6-10. Quiescent Device Current

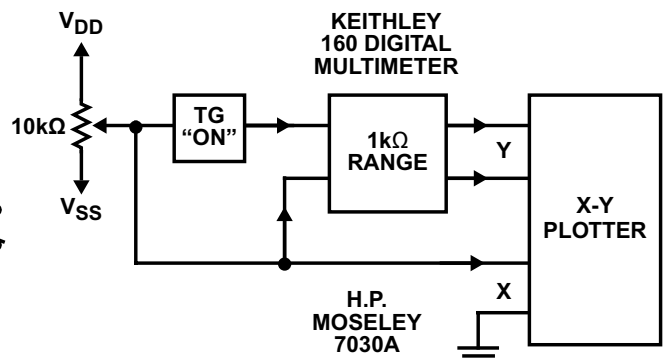


Figure 6-11. Channel ON Resistance Measurement Circuit

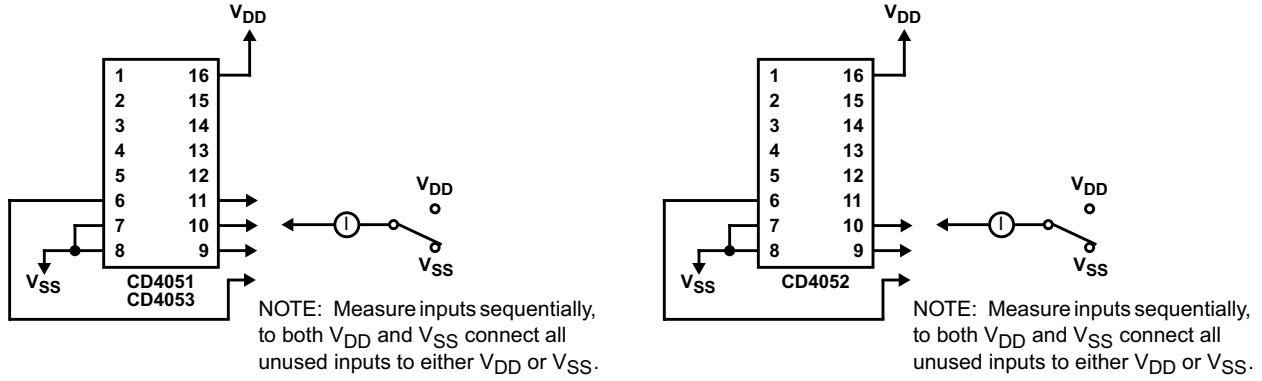


Figure 6-12. Input Current

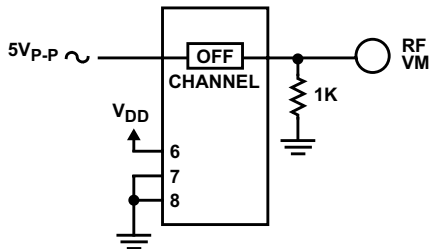


Figure 6-13. Feed-Through (All Types)

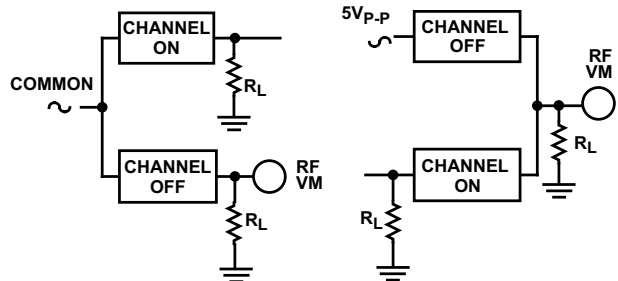
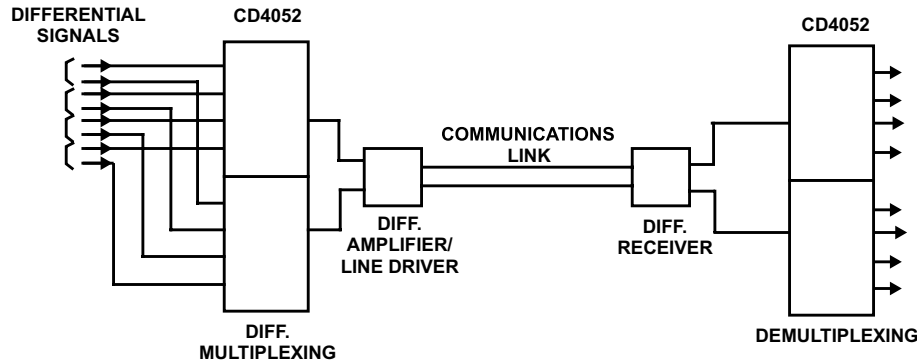


Figure 6-14. Crosstalk Between Any Two Channels (All Types)



Figure 6-15. Crosstalk Between Duals or Triplets (CD4052B, CD4053B)



Special Considerations: In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4051B, CD4052B or CD4053B.

Figure 6-16. Typical Time-Division Application of the CD4052B

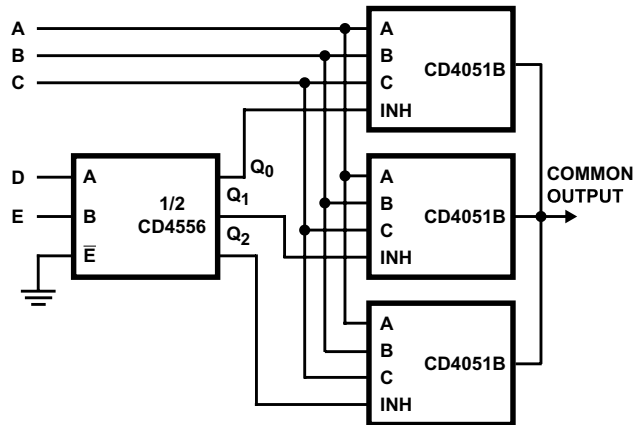


Figure 6-17. 24-to-1MUX Addressing

7 Detailed Description

7.1 Overview

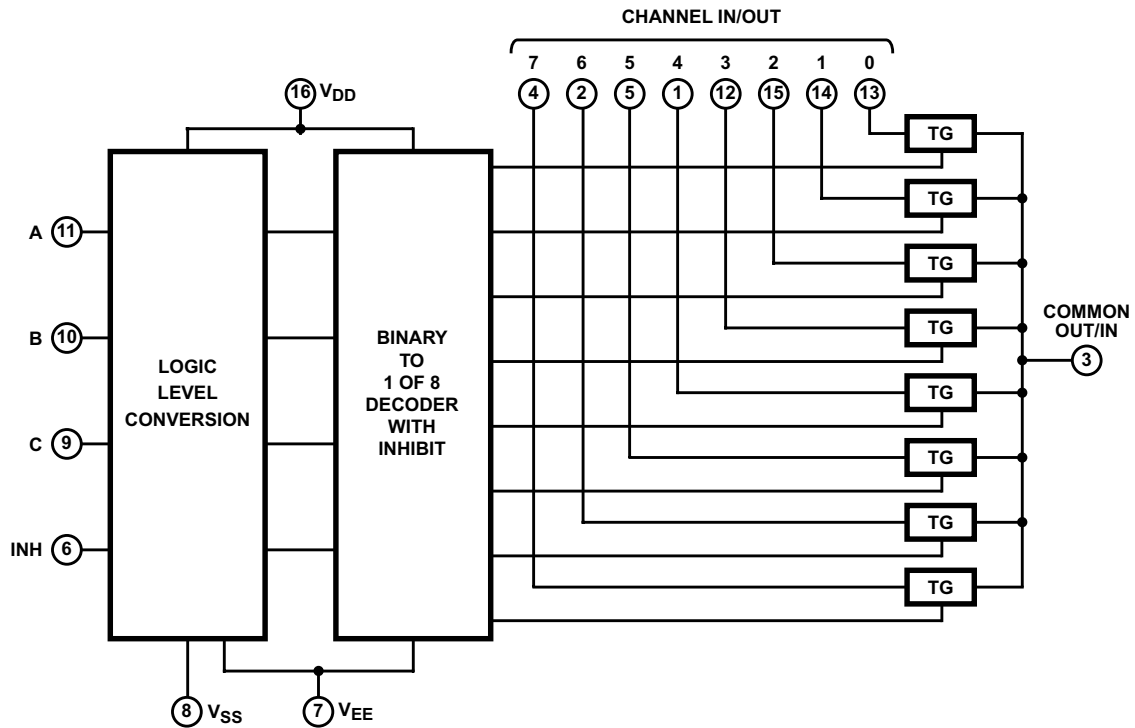
The CD4051B device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B device is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

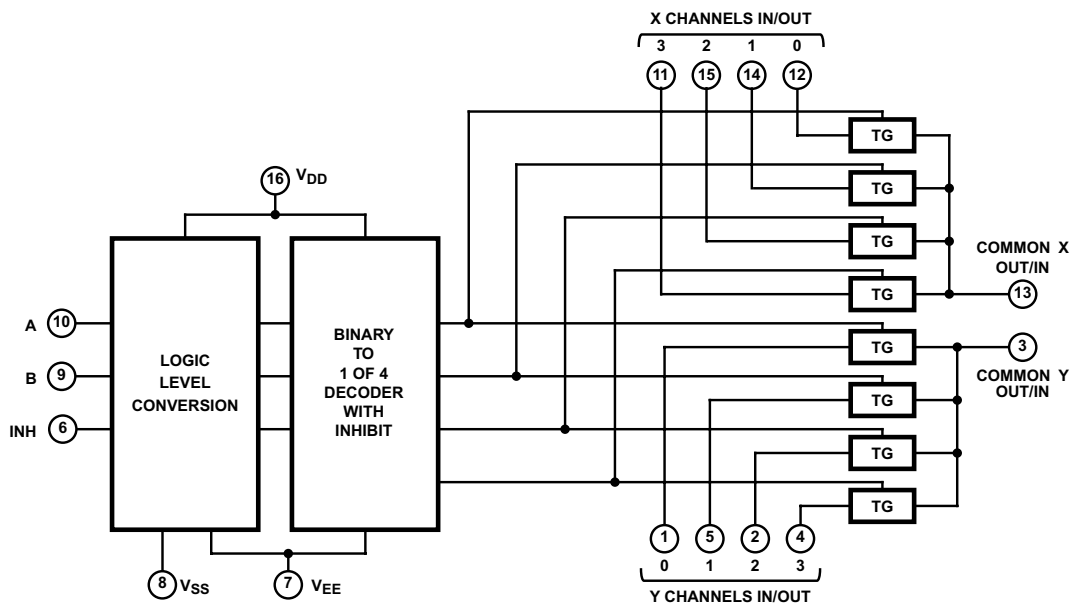
When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

7.2 Functional Block Diagrams



All inputs are protected by standard CMOS protection network.

Figure 7-1. Functional Block Diagram, CD4051B



All inputs are protected by standard CMOS protection network.

Figure 7-2. Functional Block Diagram, CD4052B



All inputs are protected by standard CMOS protection network.

Figure 7-3. Functional Block Diagram, CD4053B

7.3 Feature Description

The CD405xB line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3V to 20V, and analog signals are accepted at levels $\leq 20V$. The devices have low ON resistance, typically 125Ω over $15V_{P-P}$ signal input range for $V_{DD} - V_{EE} = 18V$. This feature allows for very little signal loss through the switch.

The CD405xB devices also have high OFF resistance, which keeps from the devices from wasting power when the switch is in the OFF position, with typical channel leakage of $\pm 100pA$ at $V_{DD} - V_{EE} = 18V$.

Binary address decoding on the chip makes channel selection simple. When channels are changed, a break-before-make system eliminates channel overlap.

7.4 Device Functional Modes

Table 7-1. Truth Table

INPUT STATES ⁽¹⁾				ON CHANNEL(S)
INHIBIT	C	B	A	
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	None
CD4053B				
0	X	X	0	ax
0	X	X	1	ay
0	X	0	X	bx
0	X	1	X	by
0	0	X	X	cx
0	1	X	X	cy
1	X	X	X	None

(1) X = Do not care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The CD405xB multiplexers and demultiplexers can be used for a wide variety of applications.

8.2 Typical Application

One application of the CD4051B is to use it in conjunction with a microcontroller to poll a keypad. [Figure 8-1](#) shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This application is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. This setup also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.

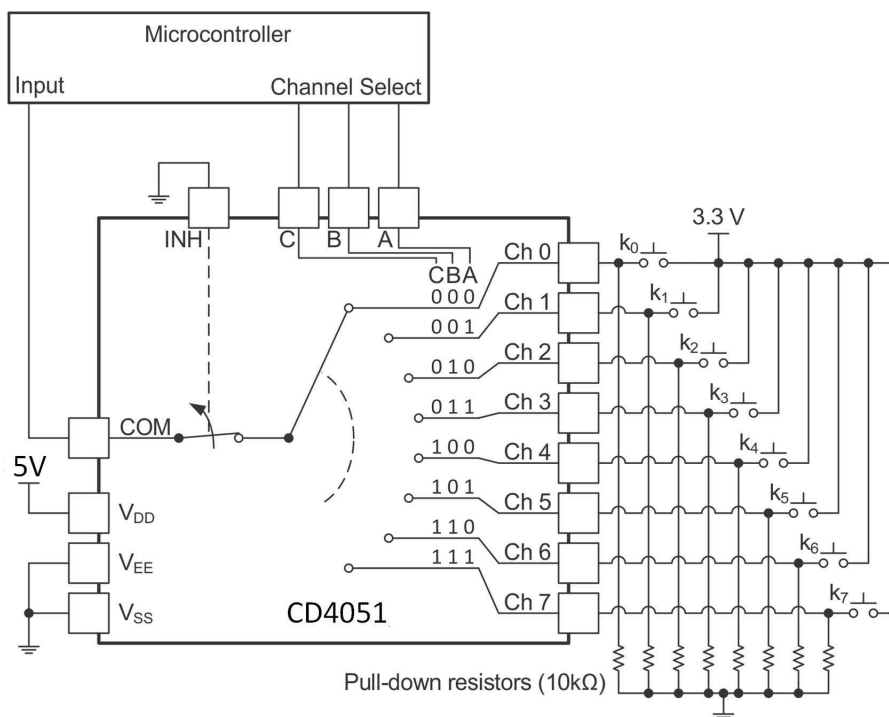


Figure 8-1. The CD4051B Being Used to Help Read Button Presses on a Keypad

8.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For switch time specifications, see propagation delay times in [Section 5.5](#).
 - Inputs cannot be pushed more than 0.5V above V_{DD} or below V_{EE} .
 - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in [Section 5.5](#).
2. Recommended Output Conditions:
 - Outputs cannot be pulled above V_{DD} or below V_{EE} .
3. Input or output current consideration:
 - The CD405xB series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

8.2.3 Application Curve

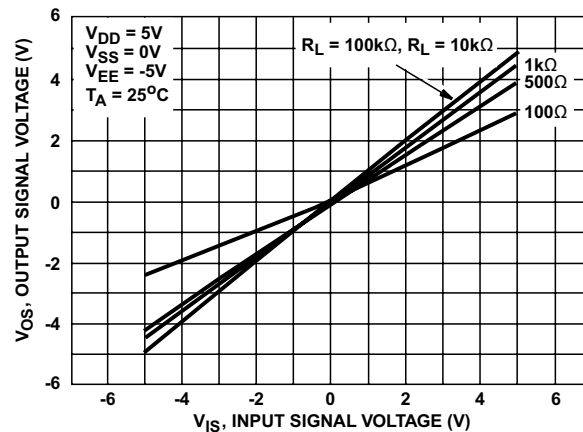


Figure 8-2. ON Characteristics for 1 of 8 Channels (CD4051B)

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 5.5](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC} , then a 0.01 μF or 0.022 μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1 μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This reflection is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. [Figure 8-3](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

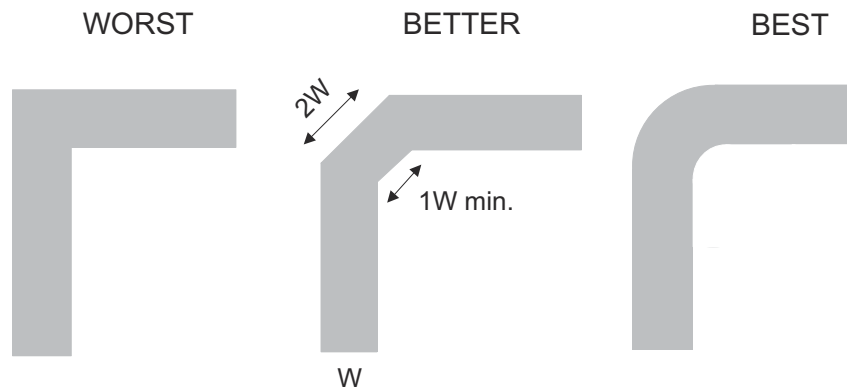


Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (February 2025) to Revision O (May 2026)	Page
• Updated D (SOIC, 16) package size.....	1
• Added SOIC to CD4052B and CD4053B pin diagrams.....	3

Changes from Revision M (November 2024) to Revision N (February 2025)	Page
• Updated Section 1	1
• Removed Figure 5-4 and Figure 5-5.....	10
• Updated Section 7.1	14
• Updated Section 7.3	16
• Updated Figure 8-1 to 5V VDD.....	18

Changes from Revision L (September 2023) to Revision M (November 2024)	Page
• Updated the <i>Typical Characteristics</i> section.....	10
• Added Figure 5-4 and Figure 5-5.....	10

Changes from Revision K (March 2023) to Revision L (September 2023)	Page
• Changed the format of the <i>Package Information</i> table to include package lead size.....	1
• Changed the format of the <i>ESD Ratings</i> , <i>Electrical Characteristics</i> , and <i>AC Performance</i> to consolidate package specifications.....	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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