

## CMOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

### High-Voltage Types (20-Volt Rating)

■ CD4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

The CD4085B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- Medium-speed operation –  $t_{PLH} = 90$  ns;  $t_{PLH} \approx 125$  ns (typ.) at 10 V
- Individual inhibit controls
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) .....  $-0.5$  V to  $+20$  V

INPUT VOLTAGE RANGE, ALL INPUTS .....  $-0.5$  V to  $V_{DD} + 0.5$  V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10$  mA

POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500 mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at 12 mW/ $^\circ\text{C}$  to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100 mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{STG}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

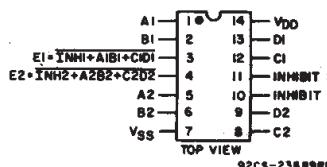
LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch (1.59  $\pm$  0.79 mm) from case for 10 s max .....  $+265^\circ\text{C}$

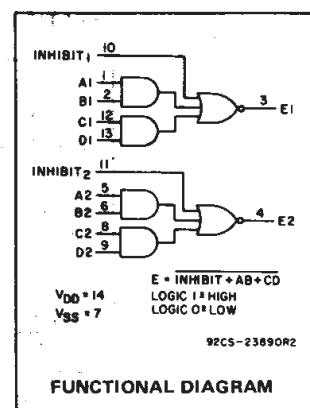
### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ )	3	18	V



Terminal Assignment



FUNCTIONAL DIAGRAM

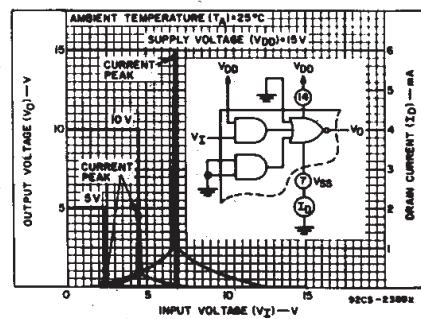


Fig. 1 – Typical voltage and current transfer characteristics.

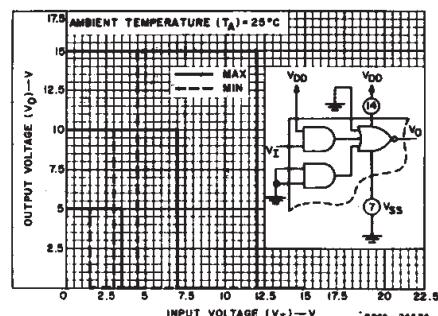


Fig. 2 – Min. and max. voltage transfer characteristics.

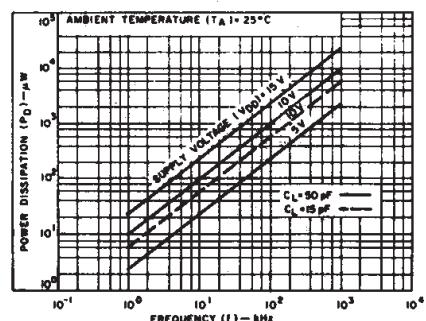


Fig. 3 – Typical power dissipation vs. frequency.

## CD4085B Types

### STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current $I_{DD}$ Max.	-	0.5	5	1	1	30	30	-	0.02	1	$\mu A$
	-	0.10	10	2	2	60	60	-	0.02	2	
	-	0.15	15	4	4	120	120	-	0.02	4	
	-	0.20	20	20	20	600	600	-	0.04	20	
Output Low (Sink) Current, $I_{OL}$ Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	$mA$
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, $I_{OH}$ Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	$mA$
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Volt- age: Low-Level, $V_{OL}$ Max.	-	0.5	5	0.05				-	0	0.05	$V$
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Volt- age: High-Level, $V_{OH}$ Min.	-	0.5	5	4.95				4.95	5	-	$V$
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage, $V_{IL}$ Max.	0.5,4.5	-	5	1.5				-	-	1.5	$V$
	1.9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, $V_{IH}$ Min.	0.5,4.5	-	5	3.5				3.5	-	-	$V$
	1.9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current, $I_{IN}$ Max.	-	0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu A$

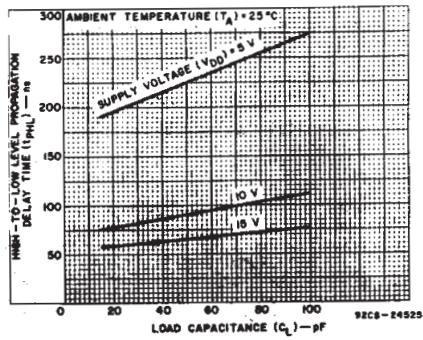


Fig. 4 - Typical data high-to-low level propagation delay time vs. load capacitance.

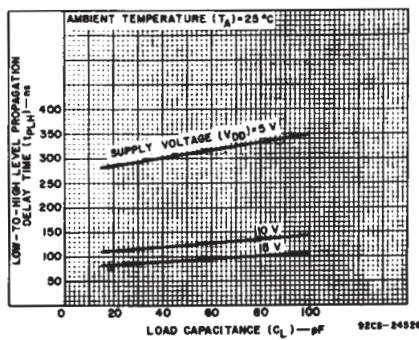


Fig. 5 - Typical data low-to-high level propagation delay time vs. load capacitance.

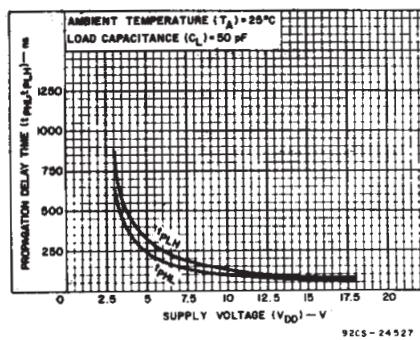


Fig. 6 - Typical data propagation delay time vs. supply voltage.

## CD4085B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	CONDITIONS		LIMITS		UNITS
	$V_{DD}$ V	Typ.	Max.		
Propagation Delay Time (Data): High-to-Low Level, $t_{PHL}$	5	225	450		ns
	10	90	180		
	15	65	130		
Low-to-High Level, $t_{PLH}$	5	310	620		ns
	10	125	250		
	15	90	180		
Propagation Delay Time (Inhibit): High-to-Low Level, $t_{PHL}$	5	150	300		ns
	10	60	120		
	15	40	80		
Low-to-High Level, $t_{PLH}$	5	250	500		ns
	10	100	200		
	15	70	140		
Transition Time, $t_{THL}, t_{TLH}$	5	100	200		ns
	10	50	100		
	15	40	80		
Input Capacitance, $C_{IN}$	Any Input	5	7.5	pF	

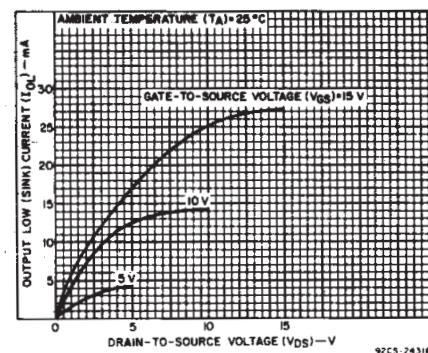


Fig. 7 – Typical output low (sink) current characteristics.

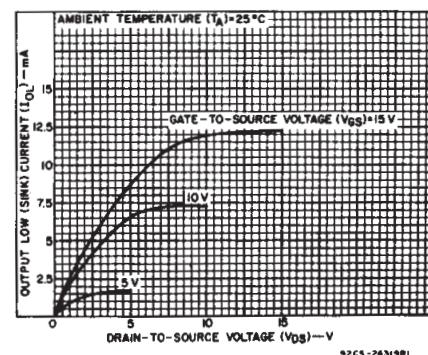


Fig. 8 – Minimum output low (sink) current characteristics.

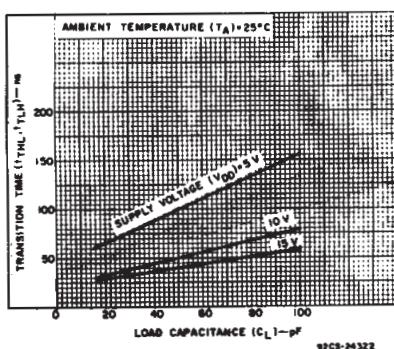


Fig. 9 – Typical transition time vs. load capacitance.

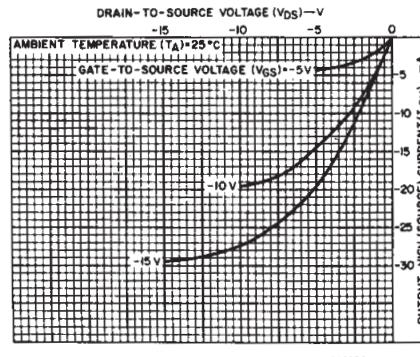


Fig. 10 – Typical output high (source) current characteristics.

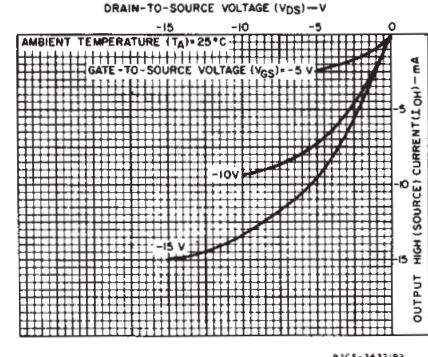


Fig. 11 – Minimum output high (source) current characteristics.

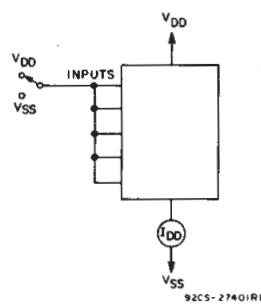


Fig. 12 – Quiescent device current test circuit.

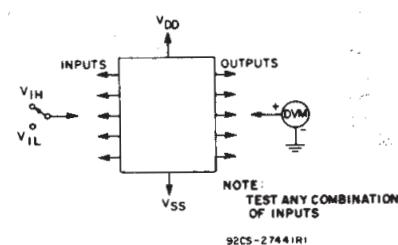


Fig. 13 – Input voltage test circuit.

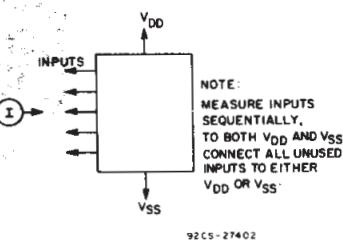


Fig. 14 – Input current test circuit.

## CD4085B Types

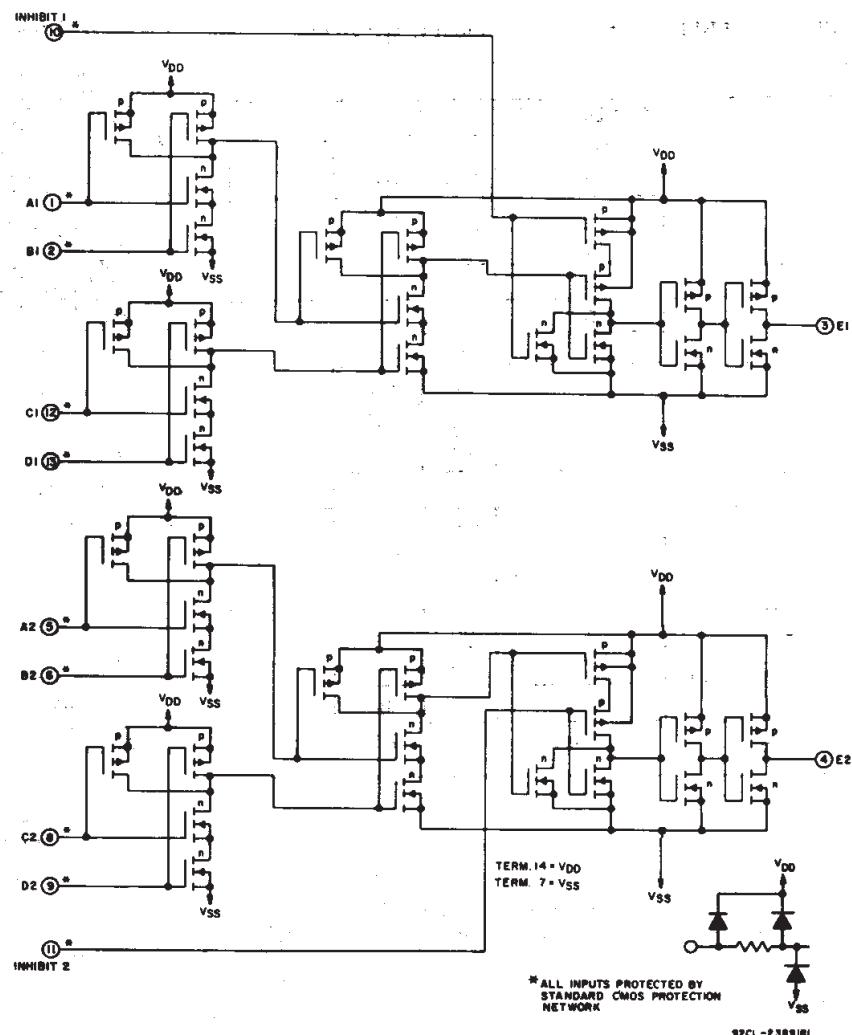
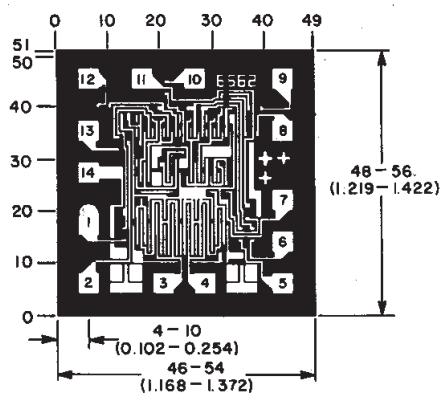


Fig. 15 – CD4085 schematic diagram.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and Pad Layout for CD4085BH.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4085BE	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4085BE
CD4085BE.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4085BE
CD4085BF	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4085BF
CD4085BF.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4085BF
CD4085BF3A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4085BF3A
CD4085BF3A.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4085BF3A
CD4085BM	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4085BM
CD4085BM.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4085BM
CD4085BPWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM085B
CD4085BPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM085B

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

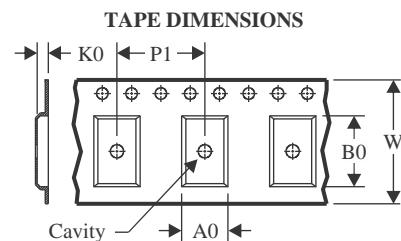
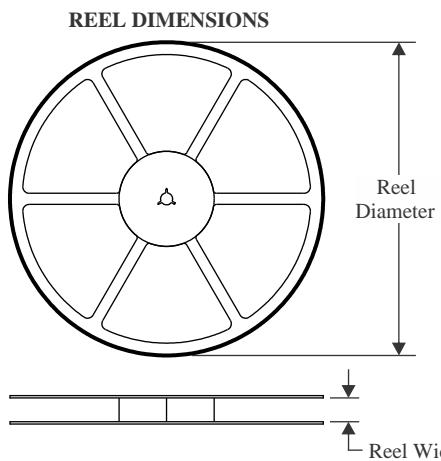
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4085B, CD4085B-MIL :**

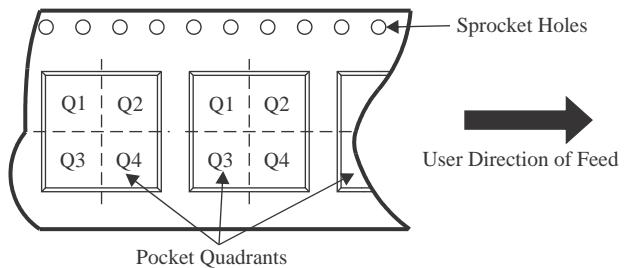
- Catalog : [CD4085B](#)
- Military : [CD4085B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


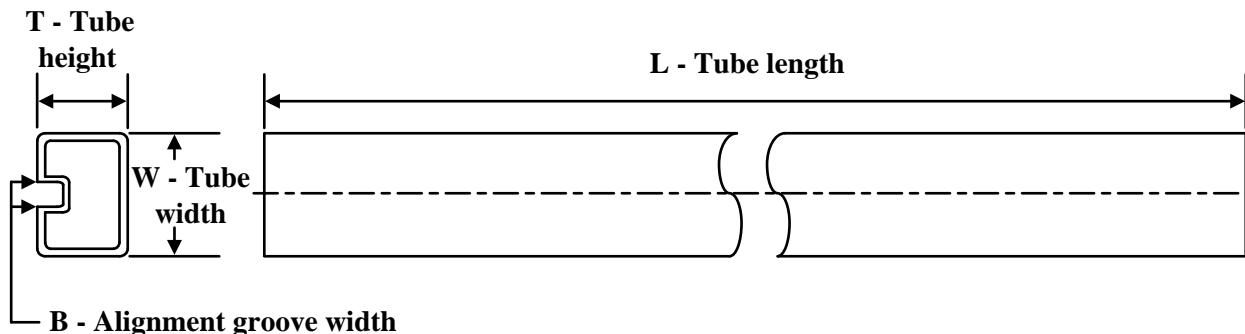
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4085BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4085BPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

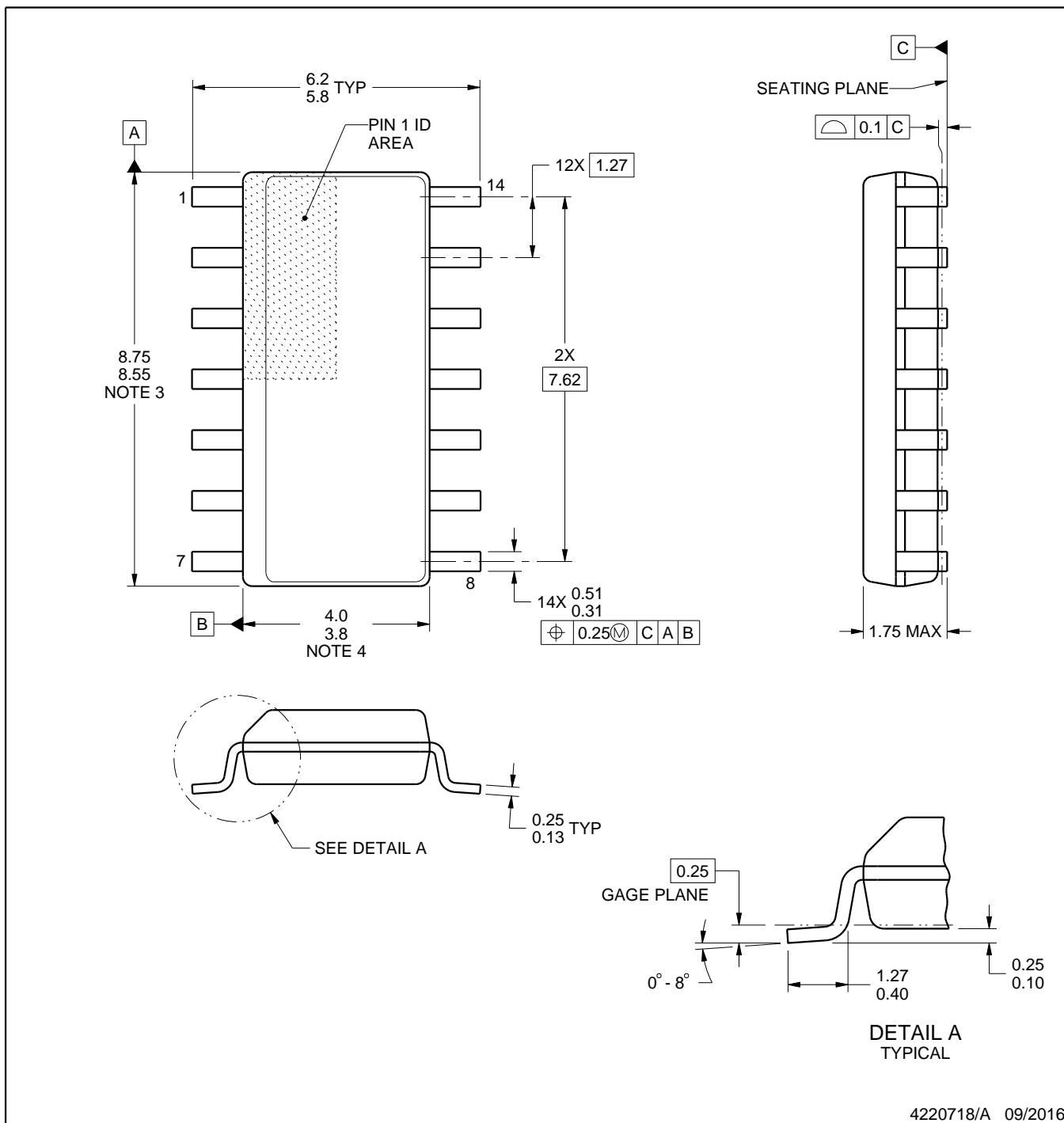
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4085BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4085BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4085BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4085BE.A	N	PDIP	14	25	506	13.97	11230	4.32
CD4085BM	D	SOIC	14	50	506.6	8	3940	4.32
CD4085BM.A	D	SOIC	14	50	506.6	8	3940	4.32

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

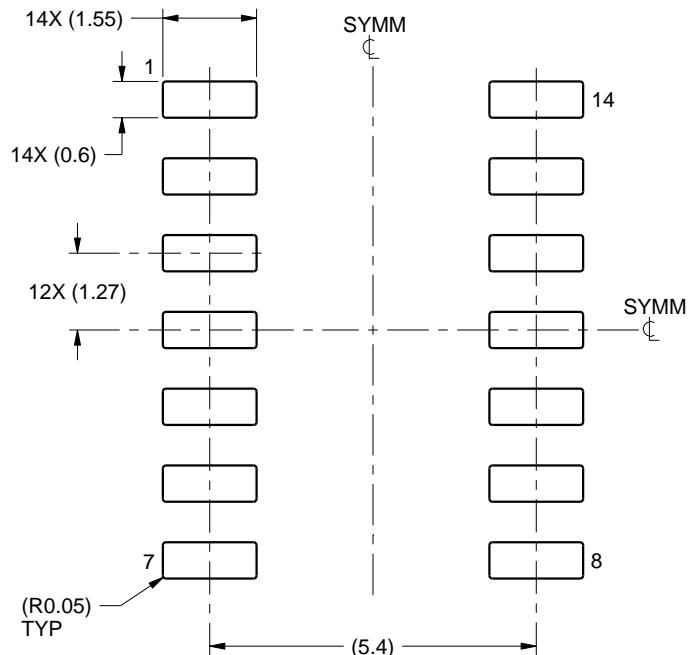
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

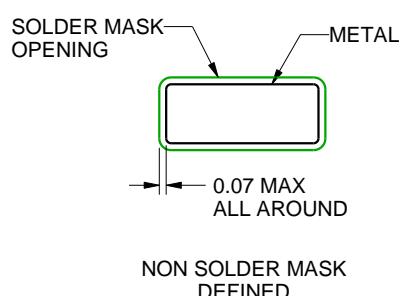
D0014A

SOIC - 1.75 mm max height

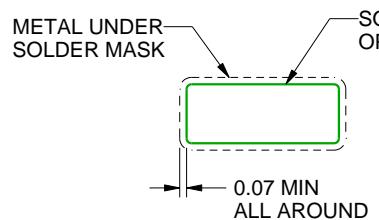
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

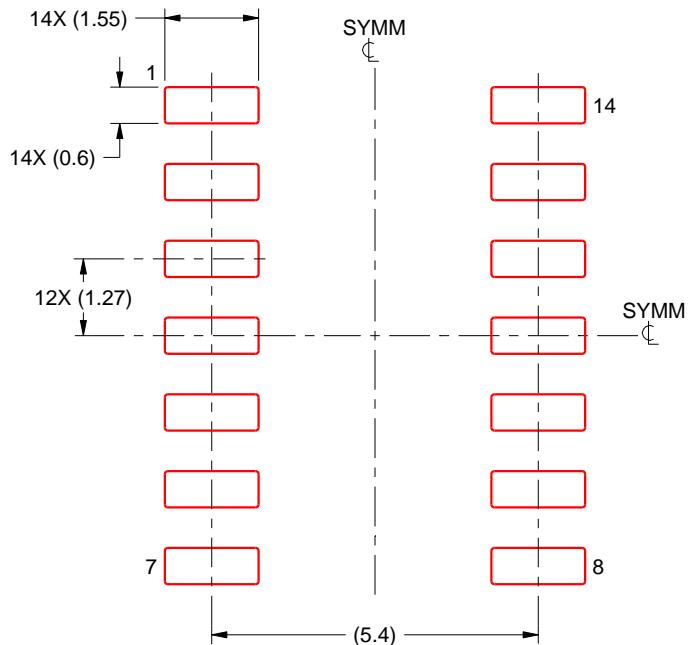
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

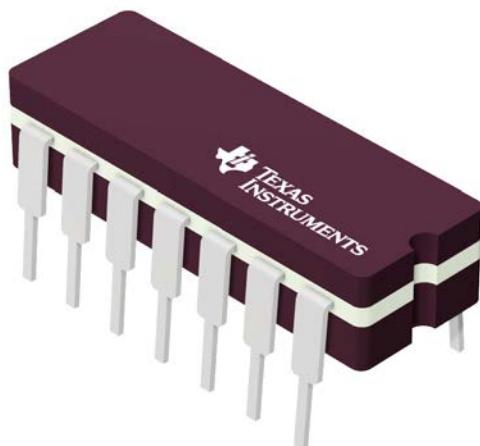
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

**J 14**

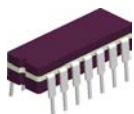
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

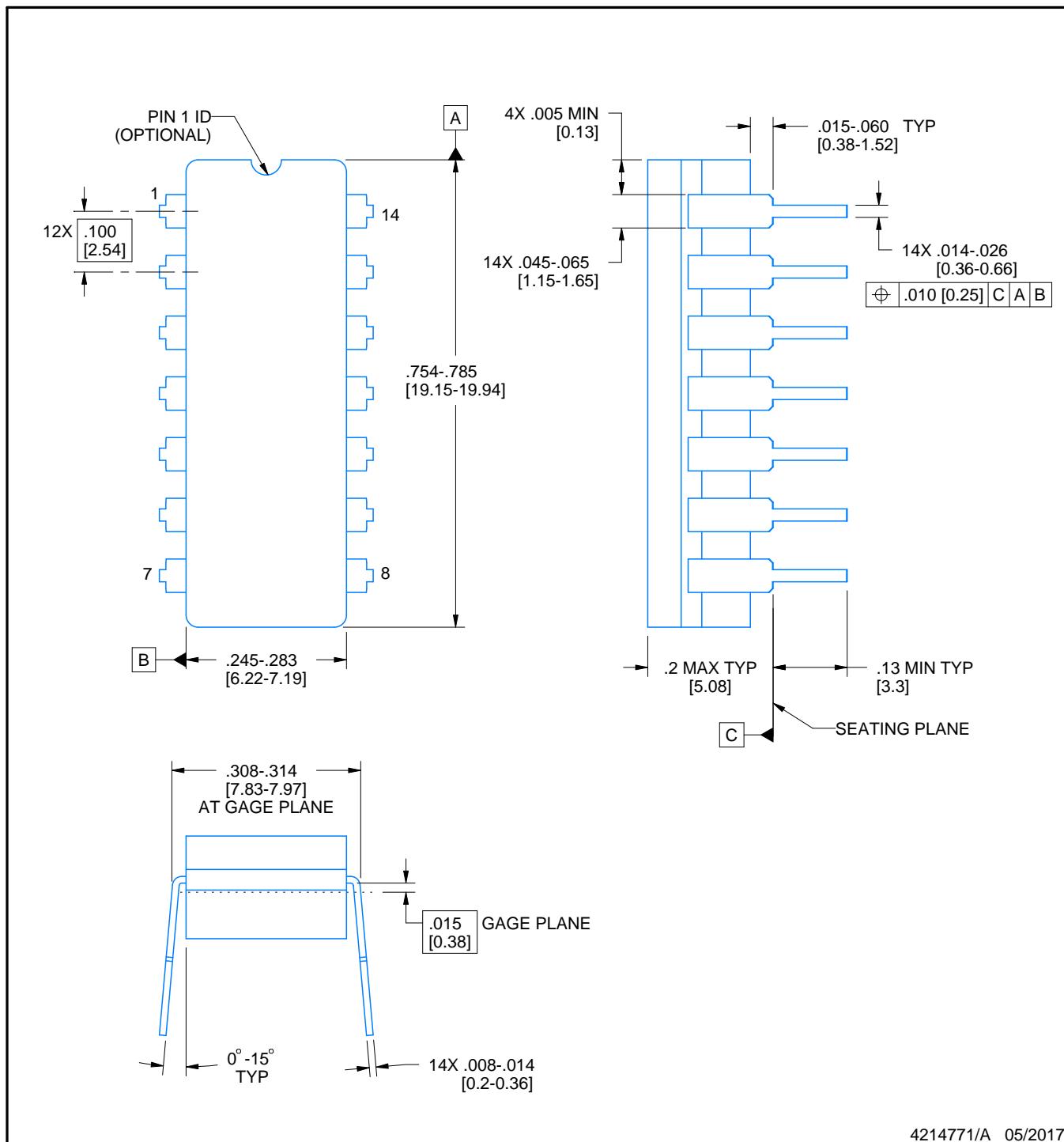


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

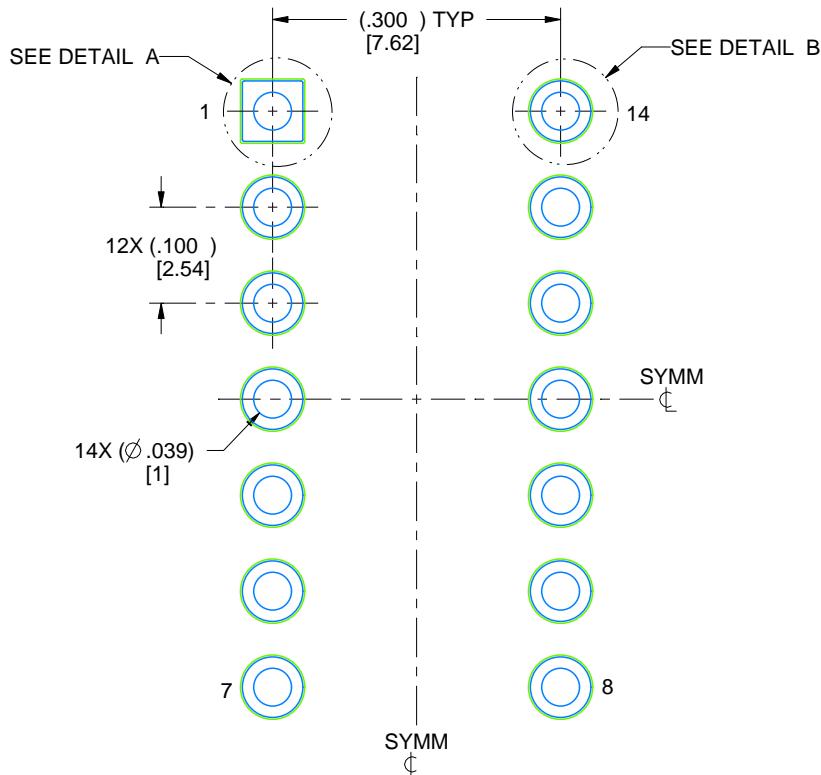
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

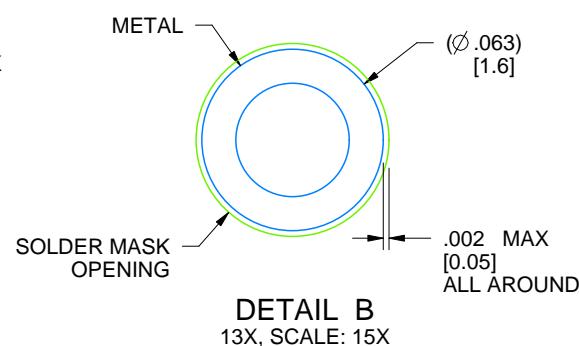
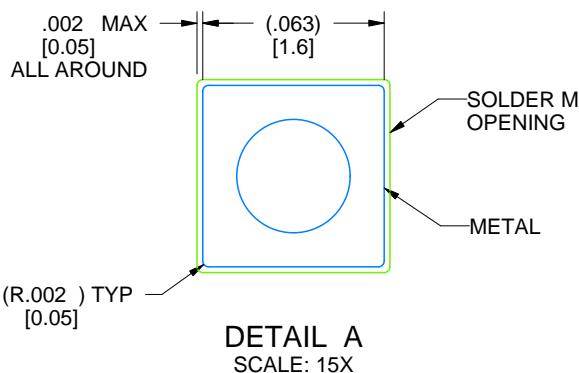
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

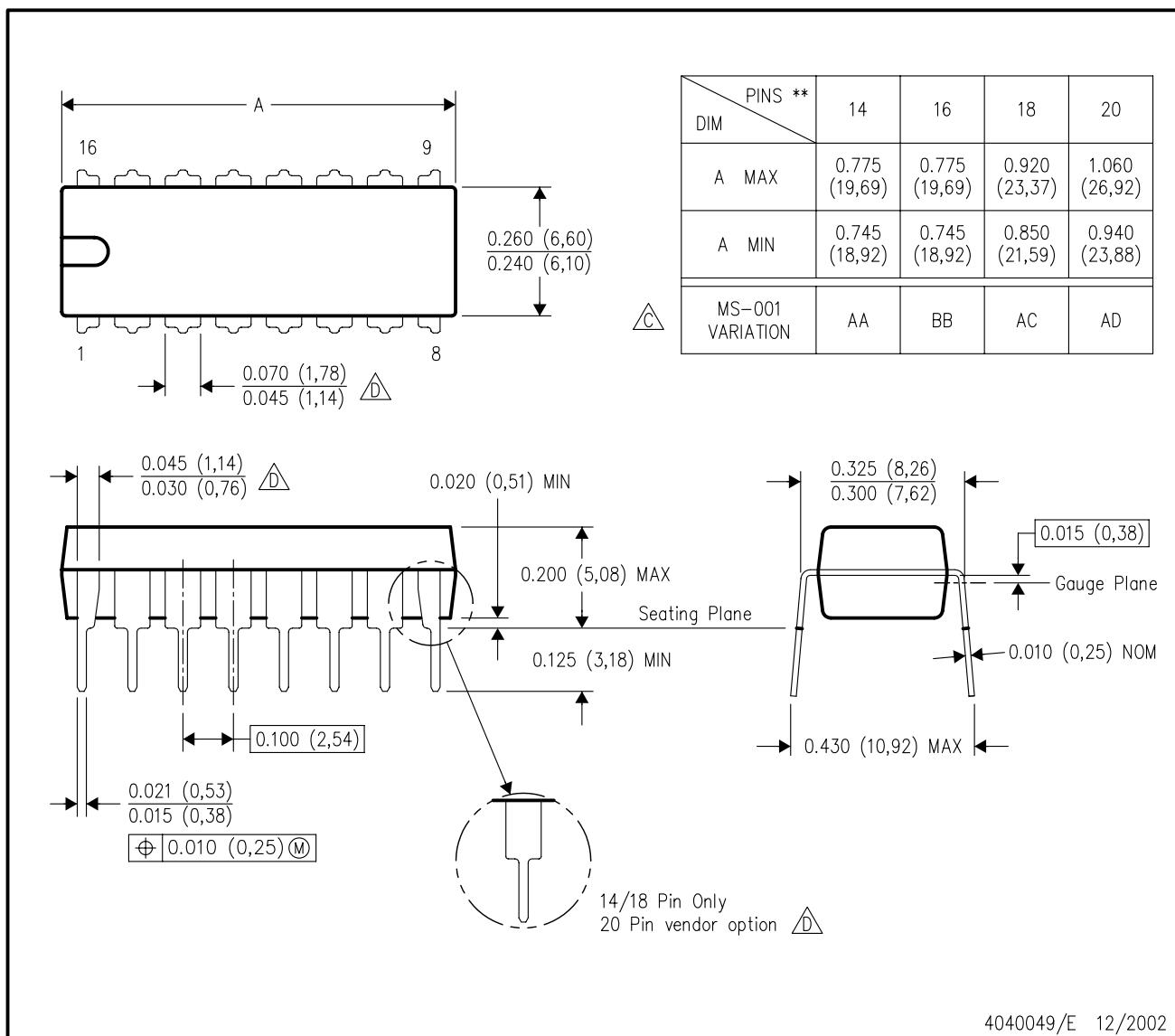


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## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



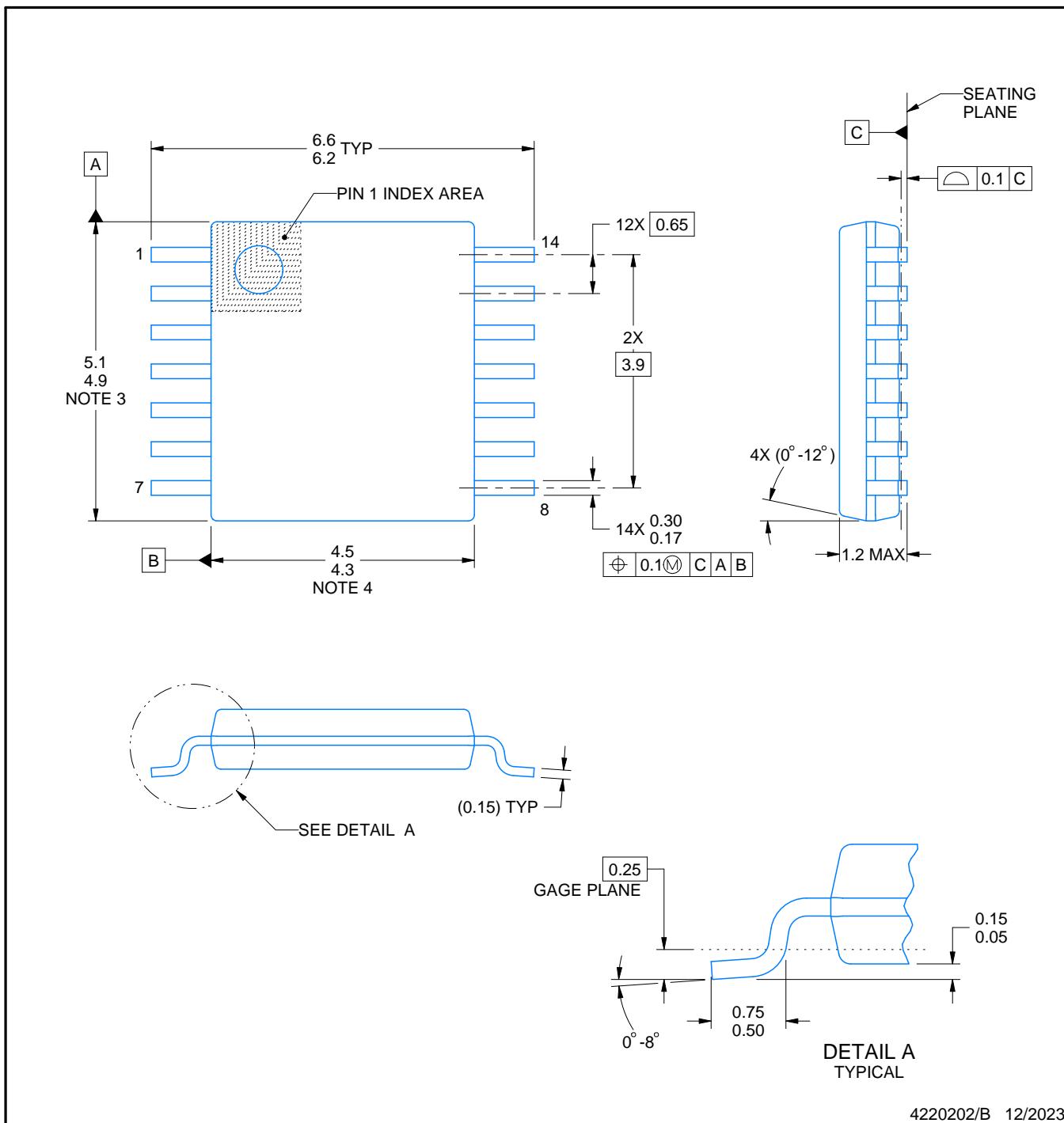
# PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

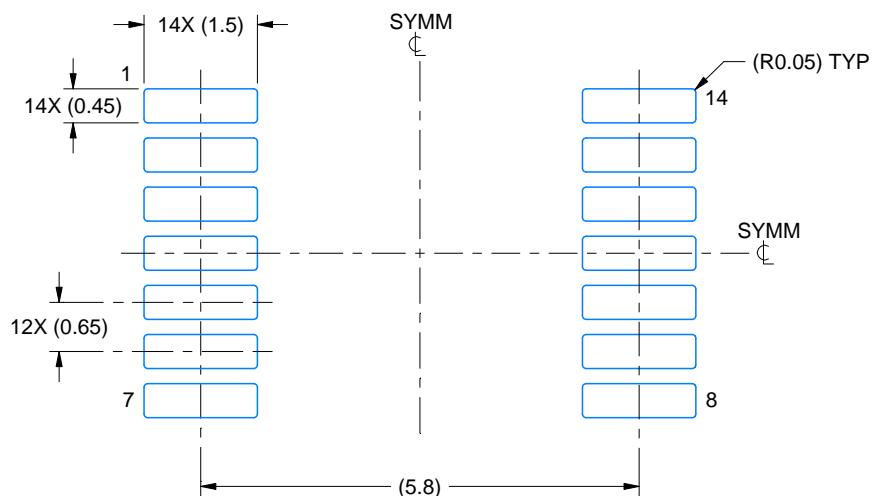
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

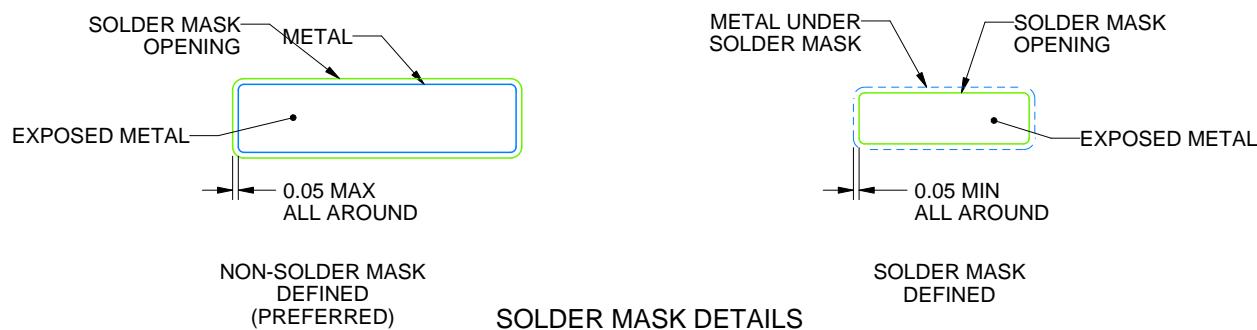
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

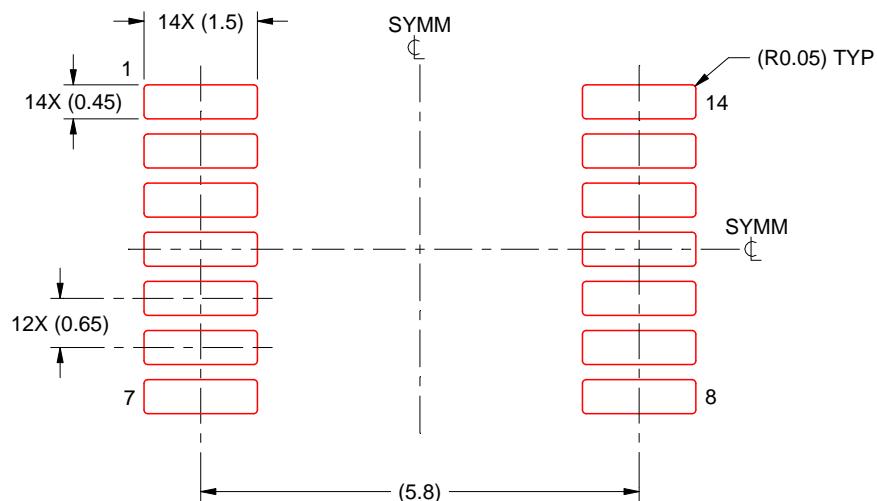
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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