

# CD4585B Types

## CMOS 4-Bit Magnitude Comparator

### High Voltage Types (20-Volt Rating)

■ CD4585B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4585B has eight comparing inputs (A3, B3, through A0, B0), three outputs (A < B, A = B, A > B) and three cascading inputs (A < B, A = B, A > B) that permit systems designers to expand the comparator function to 8, 12, 16.....4N bits. When a single CD4585B is used, the cascading inputs are connected as follows: (A < B) = low, (A = B) = high, (A > B) = high.

Cascading these units for comparison of more than 4 bits is accomplished as shown in Fig. 13.

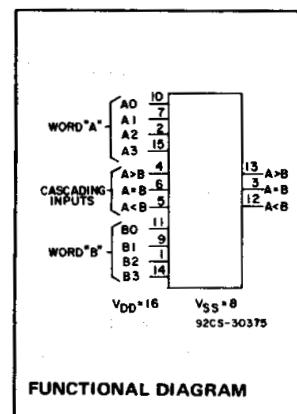
The CD4585B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- Expansion to 8,12,16.....4N bits by cascading units
- Medium-speed operation: compares two 4-bit words in 180 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu$ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range) range = 1 V at  $V_{DD} = 5$  V  
2 V at  $V_{DD} = 10$  V  
2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Servo motor controls ■ Process controllers



FUNCTIONAL DIAGRAM

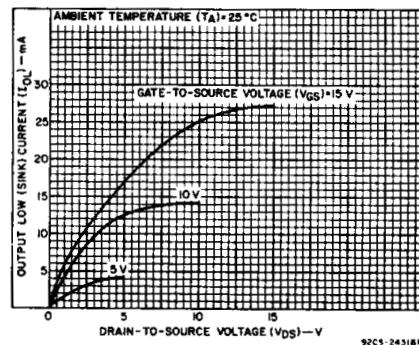


Fig.1 – Typical output low (sink) current characteristics.

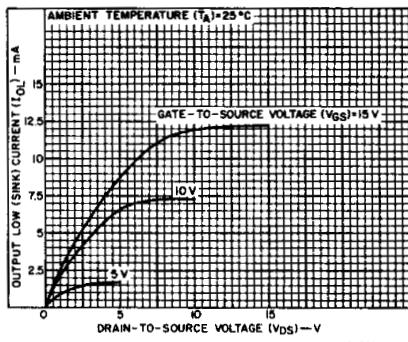


Fig.2 – Minimum output low (sink) current characteristics.

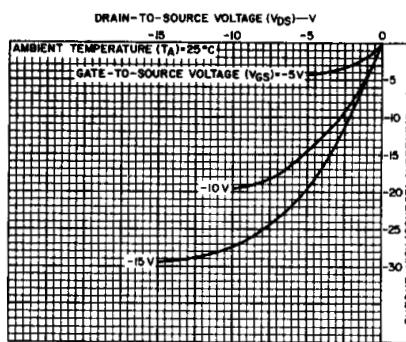


Fig.3 – Typical output high (source) current characteristics.

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	.....	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal) .....	.....	-0.5V to $V_{DD}$ +0.5V
INPUT VOLTAGE RANGE, ALL INPUTS .....	.....	-0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT .....	.....	$\pm 10$ mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ .....	.....	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ .....	.....	Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ .....	.....	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....	.....	-55°C to +125°C
STORAGE TEMPERATURE RANGE ( $T_{STG}$ ) .....	.....	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch (1.59 $\pm$ 0.79mm) from case for 10s max .....	.....	+265°C

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ )	3	18	V

## CD4585B Types

### TRUTH TABLE

INPUTS				COMPARING			CASCAADING			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	X	X	X	X	X	1	0	0	1			
A3 = B3	A2 > B2	X	X	X	X	1	0	0	1			
A3 = B3	A2 = B2	A1 > B1	X	X	X	1	0	0	1			
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	1	0	0	1			
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1			
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	X	0	1	0			
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	X	1	0	0			
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	1	0	0			
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	1	0	0			
A3 = B3	A2 < B2	X	X	X	X	X	1	0	0			
A3 < B3	X	X	X	X	X	X	1	0	0			

X = Don't Care

Logic 1 = High Level

Logic 0 = Low Level

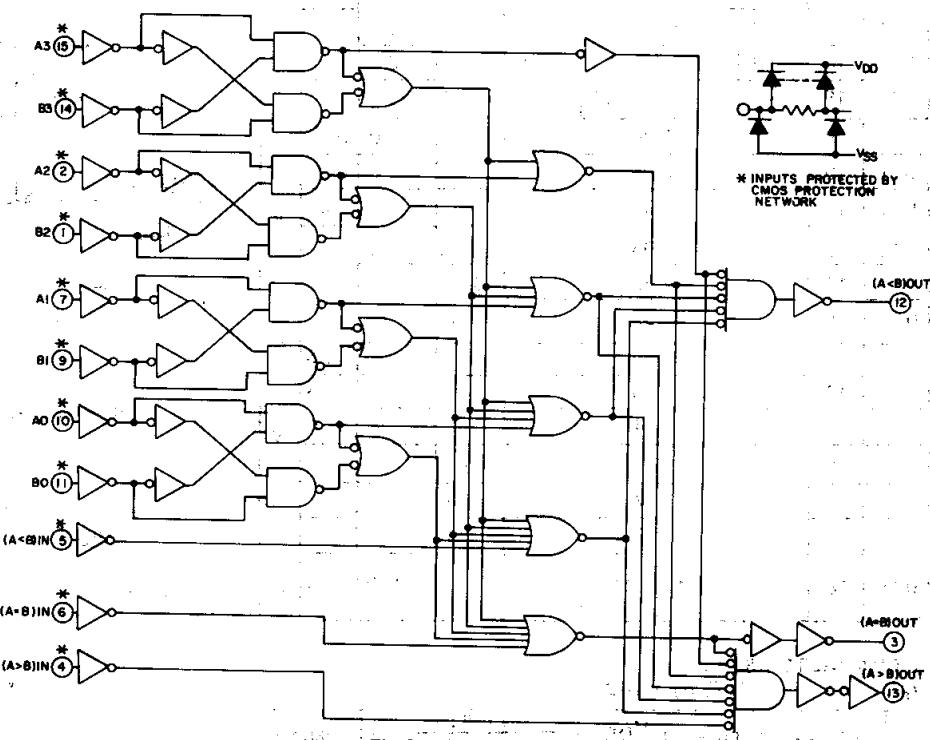


Fig. 4 - Logic diagram.

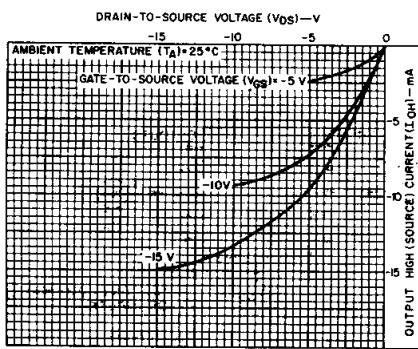


Fig. 5 - Minimum output high (source) current characteristics.

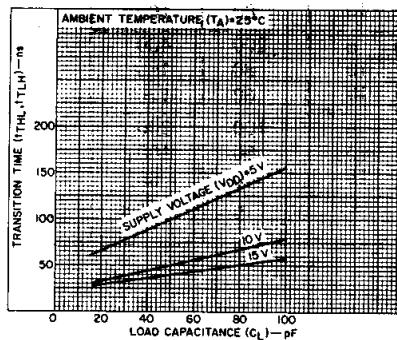


Fig. 6 - Typical transition time as a function of load capacitance.

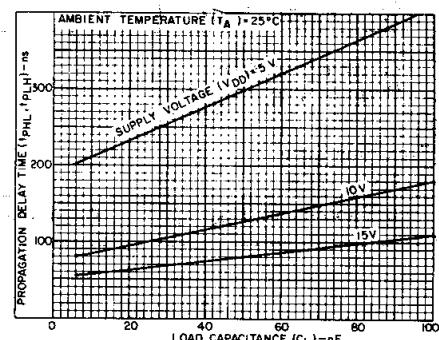


Fig. 7 - Typical propagation delay time ("comparing inputs" to outputs) as a function of load capacitance.

# CD4585B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						U N I T S	
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD}$ Max.	-	0,5	5	5	5	150	150	-	0.04	5	$\mu A$
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	$mA$
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, $I_{OH}$ Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	$mA$
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0,5	5	0.05			-	0	0.05	-	$V$
	-	0,10	10	0.05			-	0	0.05	-	
	-	0,15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, $V_{OH}$ Min.	-	0,5	5	4.95			4.95	5	-	-	$V$
	-	0,10	10	9.95			9.95	10	-	-	
	-	0,15	15	14.95			14.95	15	-	-	
Input Low Voltage $V_{IL}$ Max.	0.5,4.5	-	5	1.5			-	-	1.5	-	$V$
	1.9	-	10	3			-	-	3	-	
	1.5,13.5	-	15	4			-	-	4	-	
Input High Voltage, $V_{IH}$ Min.	0.5,4.5	-	5	3.5			3.5	-	-	-	$V$
	1.9	-	10	7			7	-	-	-	
	1.5,13.5	-	15	11			11	-	-	-	
Input Current $I_{IN}$ Max.	-	0,18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu A$

## DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ C$ ; Input  $t_r, t_f = 20 \text{ ns}$ ,  $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	$V_{DD}$ Volts	LIMITS		UNITS	
			Typ.	Max.		
Propagation Delay Time: Comparing Inputs to Outputs, $t_{PHL}, t_{PLH}$			5	300	ns	
			10	125		
			15	80		
Cascading Inputs to Outputs, $t_{PHL}, t_{PLH}$			5	200	ns	
			10	80		
			15	60		
Transition Time, $t_{THL}, t_{TLH}$			5	100	ns	
			10	50		
			15	40		
Input Capacitance, $C_{IN}$	Any Input	-	5	7.5	pF	

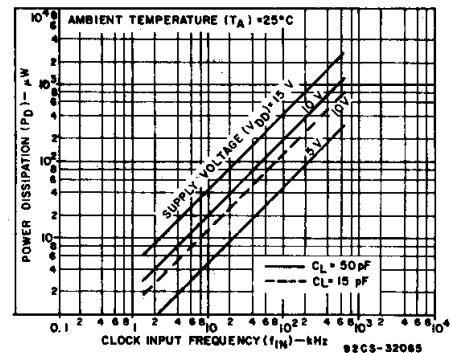


Fig. 8 - Typical dynamic power dissipation as a function of clock input frequency (see Fig. 9 - dynamic power dissipation test circuit).

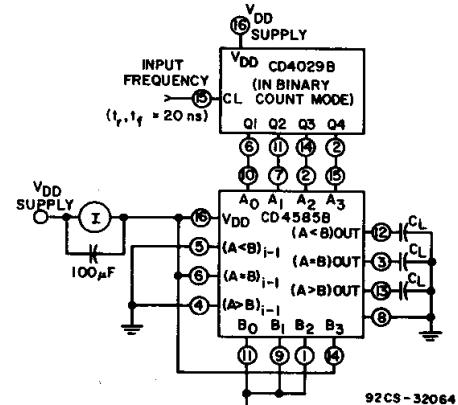


Fig. 9 - Dynamic power dissipation test circuit.

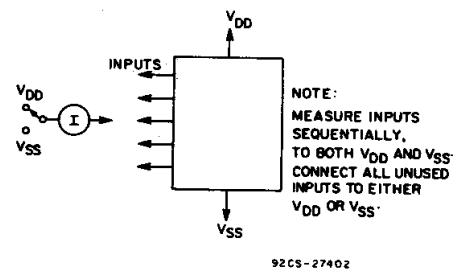


Fig. 10 - Input current test circuit.

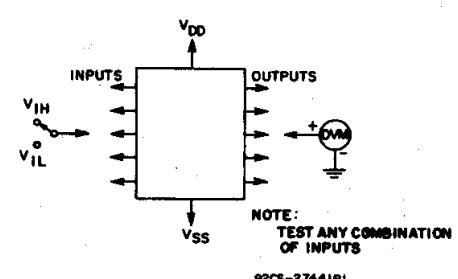


Fig. 11 - Input-voltage test circuit.

## CD4585B Types

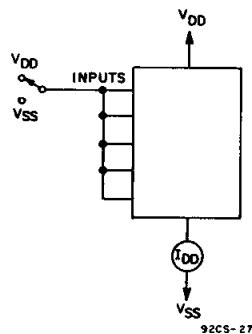
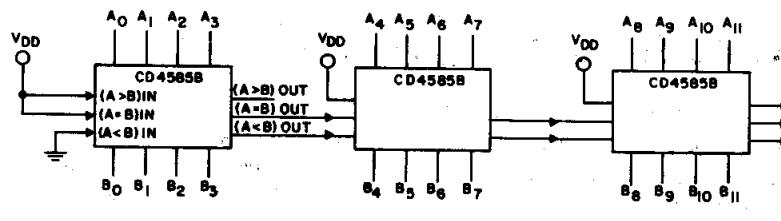


Fig. 12 — Quiescent-device-current test circuit.



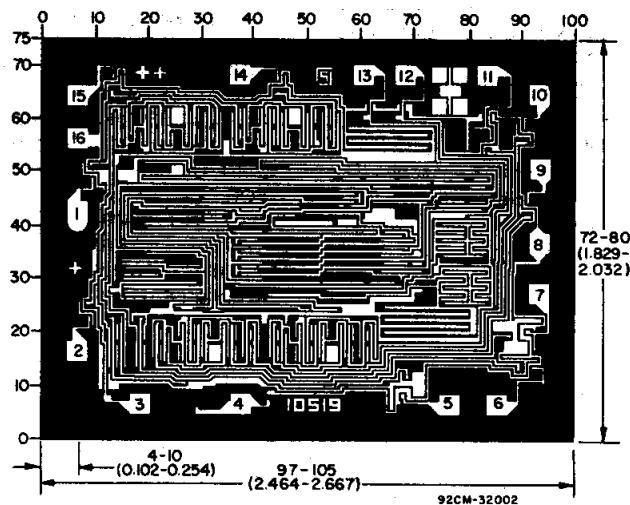
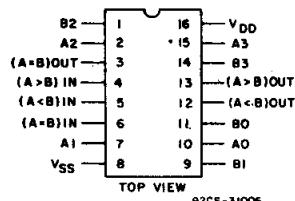
$t_p \text{ TOTAL} = t_p \text{ (COMPARE)} + 2 \times t_p \text{ (INPUTS)} + t_p \text{ (OUTPUTS)}$ , AT  $V_{DD} = 10V$   
(3 STAGES)

$$= 120 + 2(80) = 280 \text{ ns (TYP.)}$$

92CM-31007RI

Fig. 13 — Typical speed characteristics of a 12-bit comparator.

### TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD4585BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
7703702EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7703702EA CD4585BF3A
CD4585BE	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4585BE
CD4585BE.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4585BE
CD4585BEE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4585BE
CD4585BF3A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7703702EA CD4585BF3A
CD4585BF3A.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7703702EA CD4585BF3A
CD4585BNSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4585B
CD4585BNSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4585B
CD4585BPW	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM585B
CD4585BPW.A	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM585B
CD4585BPWE4	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM585B
CD4585BPWG4	Active	Production	TSSOP (PW)   16	90   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM585B

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

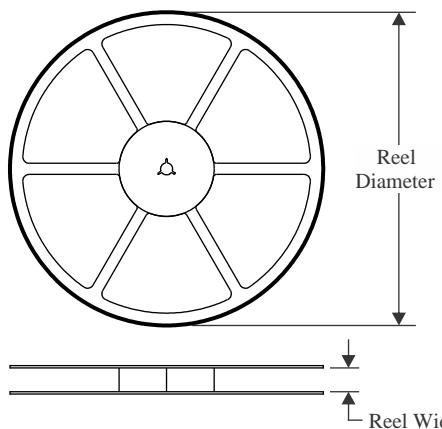
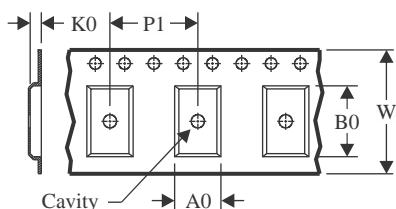
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4585B, CD4585B-MIL :**

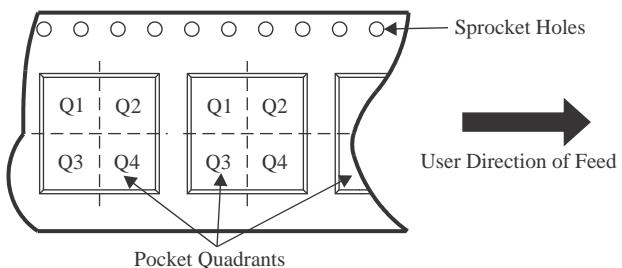
- Catalog : [CD4585B](#)
- Military : [CD4585B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

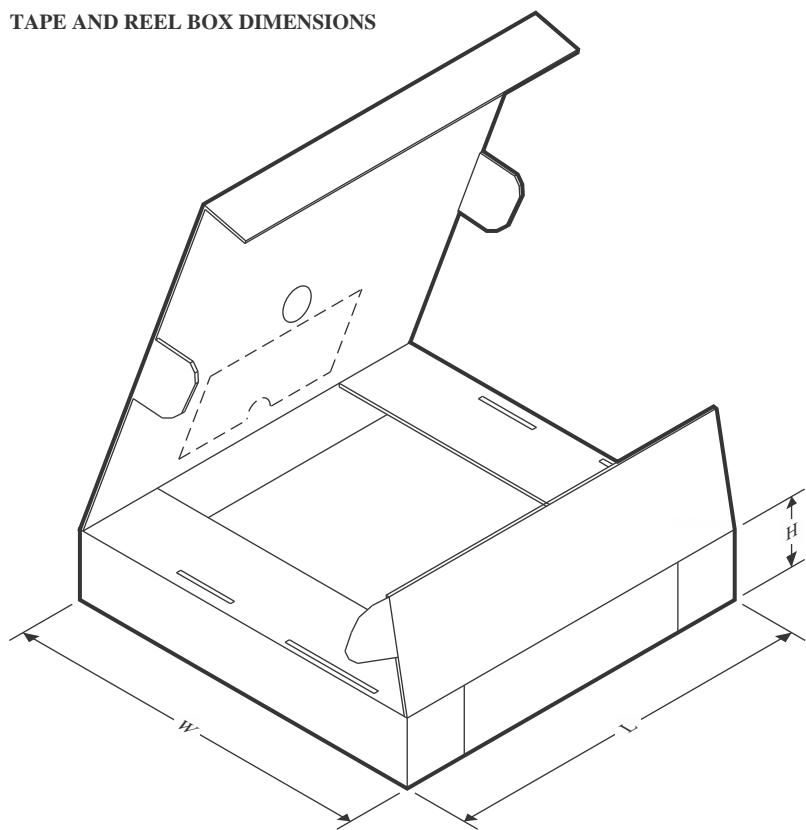
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


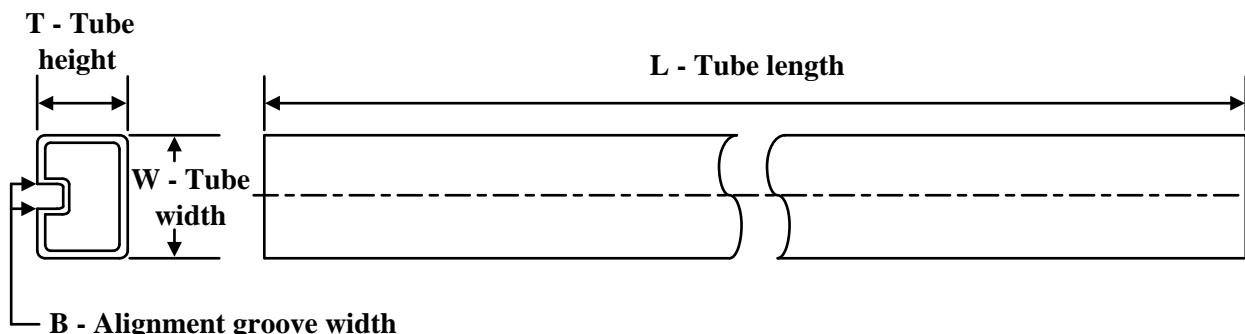
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4585BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4585BNSR	SOP	NS	16	2000	353.0	353.0	32.0

**TUBE**


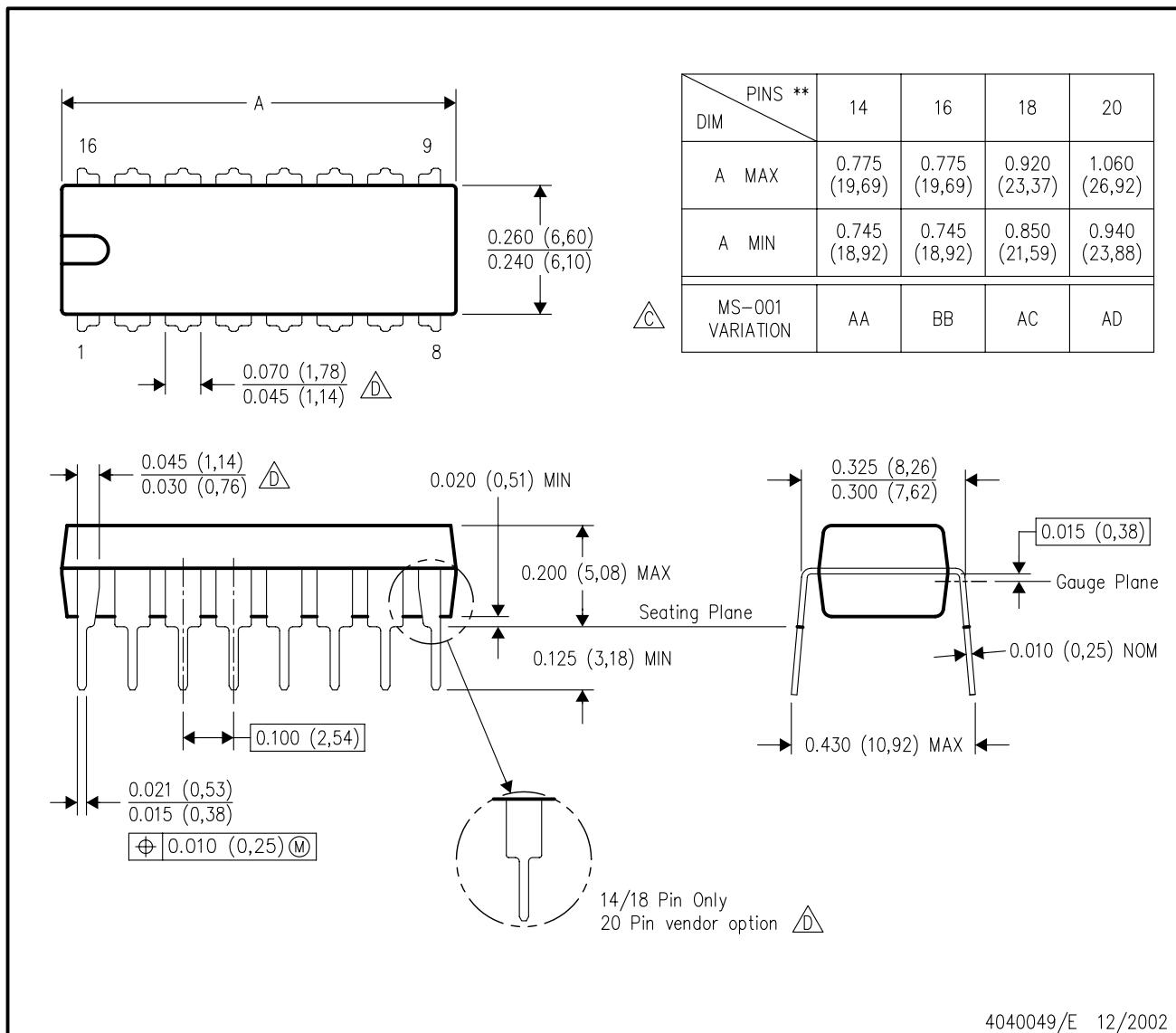
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
CD4585BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4585BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4585BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4585BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4585BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4585BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4585BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4585BPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4585BPWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4585BPWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

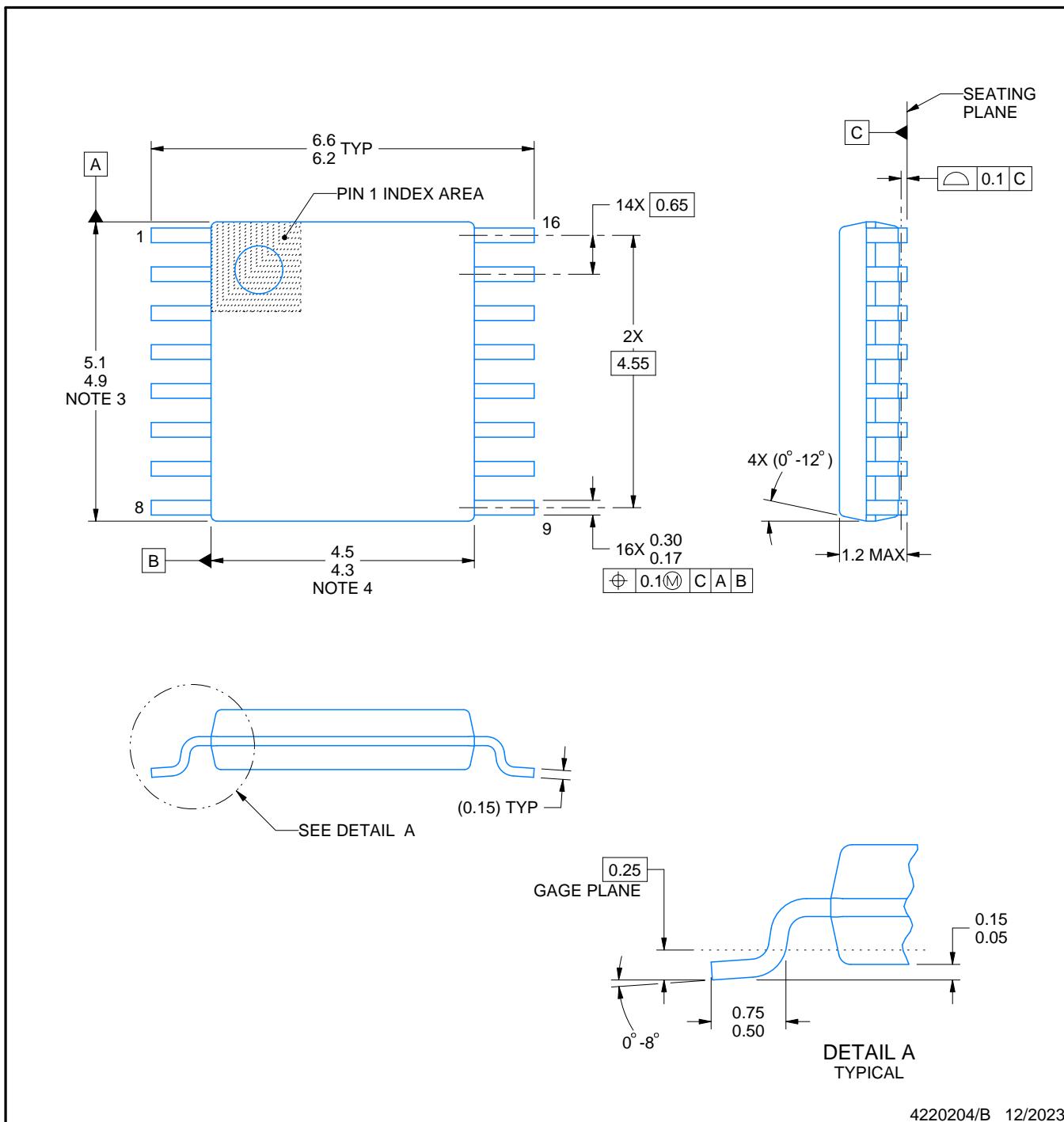
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

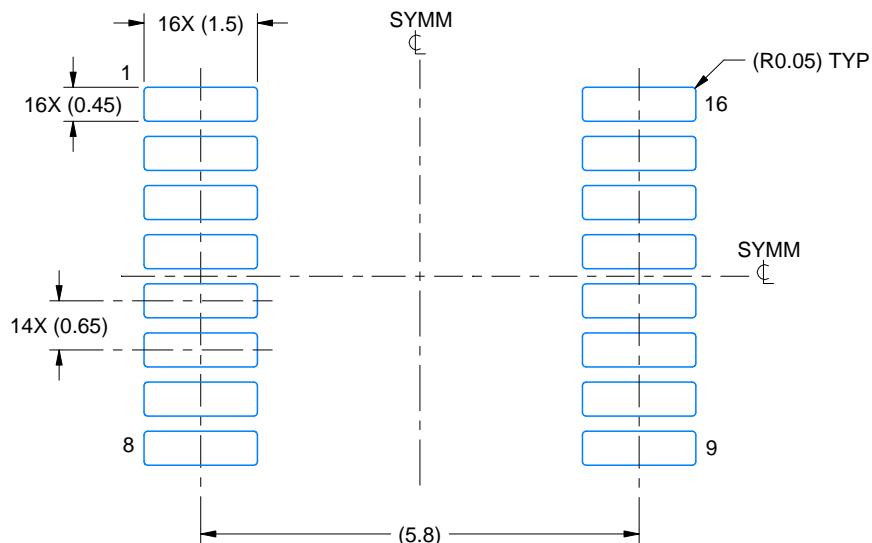
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

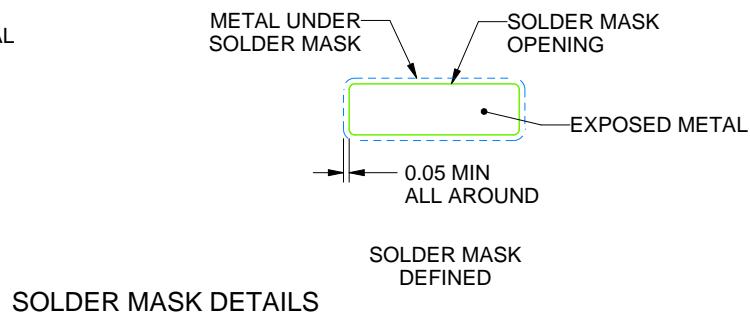
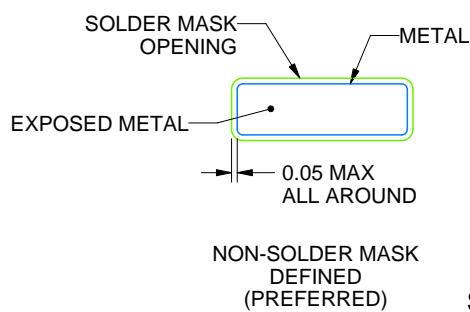
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

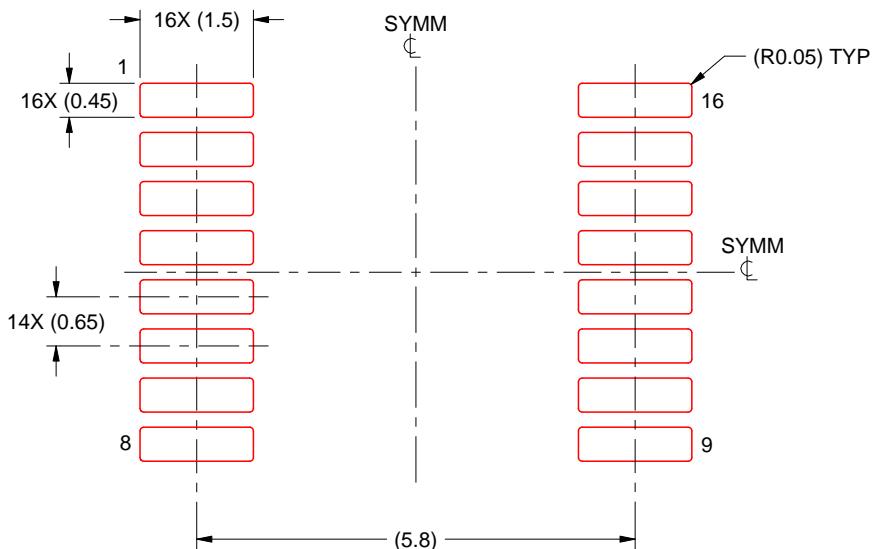
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

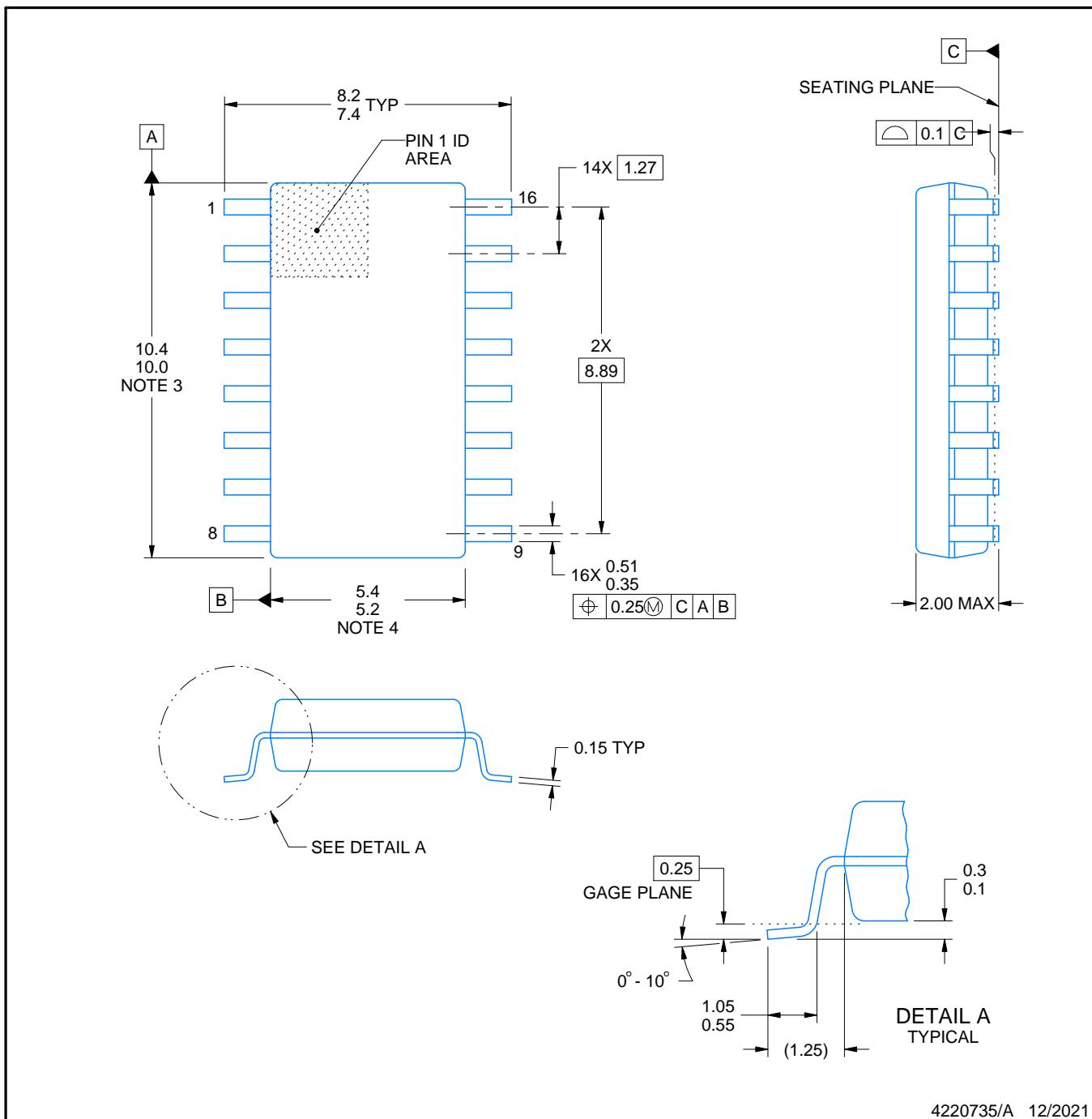
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# PACKAGE OUTLINE

## SOP - 2.00 mm max height

SOP



### NOTES:

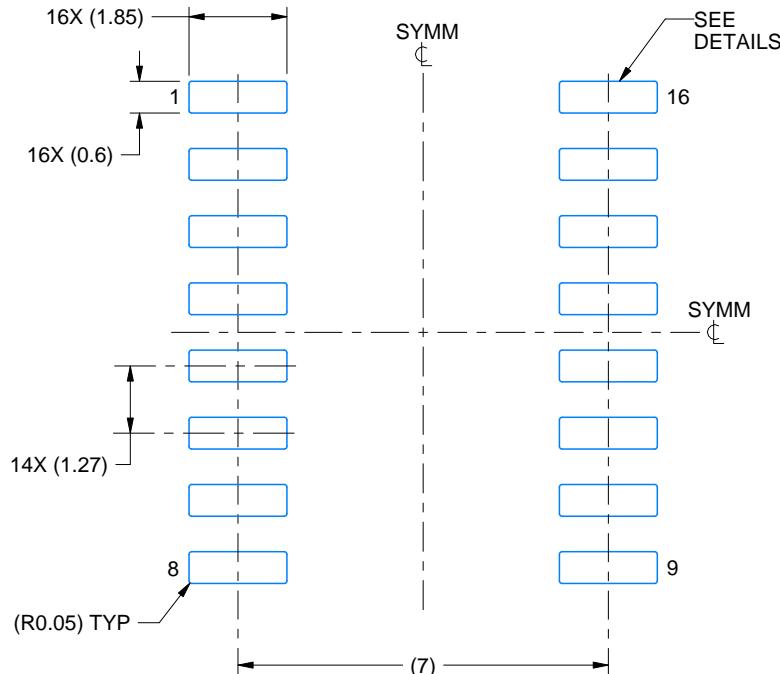
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

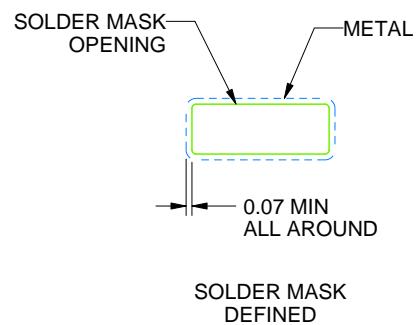
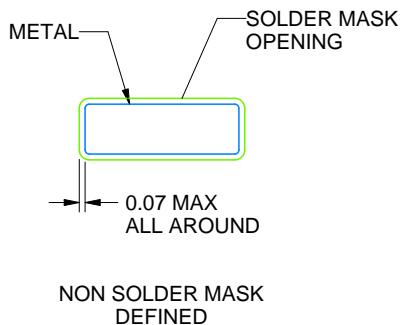
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

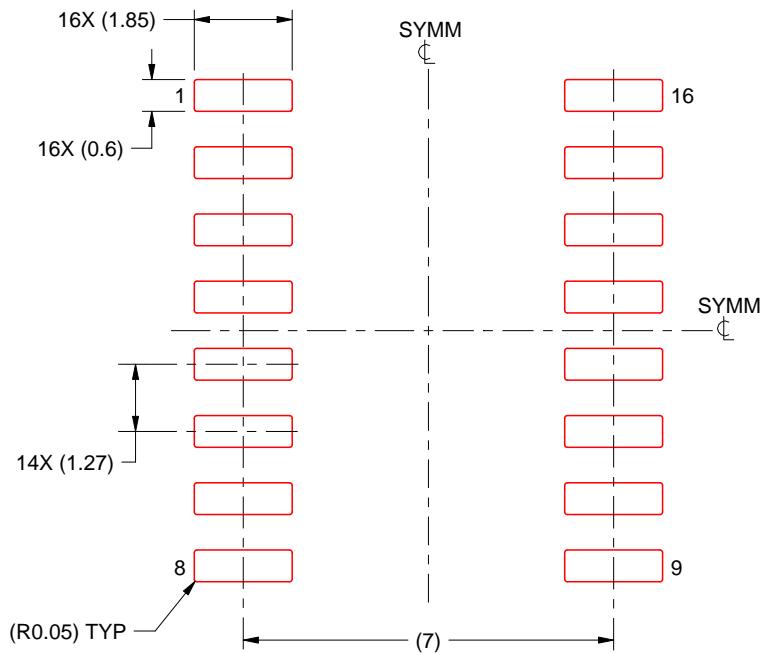
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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