CDx4HC147, CD74HCT147 High-Speed CMOS Logic 10- to 4-Line Priority Encoder

1 Features

- Buffered inputs and outputs
- Typical propagation delay: 13ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C
- Fanout (over temperature range)
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range: -55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2V to 6V Operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT types
  - 4.5V to 5.5V Operation
  - Direct LSTTL input logic compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

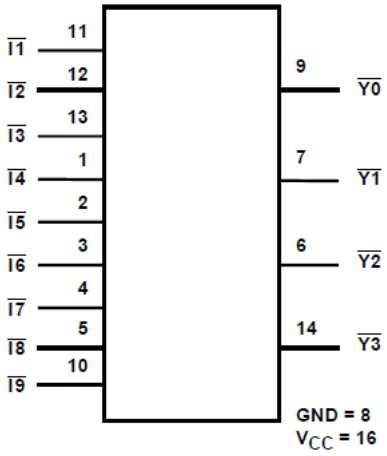
2 Description

The CDx4HC147 and CD74HCT147 are 9-input priority encoders. These devices provide the 10-line to 4-line priority encoding function by use of the implied decimal “zero.”

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)(2)
CD54HC147	J (CDIP, 16)	21.34mm × 6.92mm
CD74HC147	N (PDIP, 16)	19.31mm × 6.35mm
	D (SOIC, 16)	9.90mm × 3.90mm
	PW (TSSOP, 16)	5.00mm × 4.40mm
CD74HCT147	N (PDIP, 16)	19.31mm × 6.35mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

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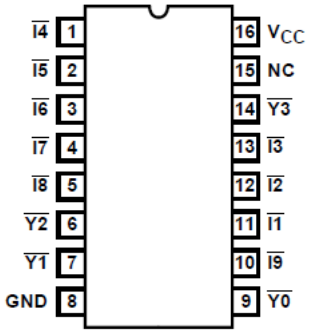
3 Pin Configuration and Functions



CD54HC147 J Package; CD74HC(T)147 N, D, or PW Package;
16-Pin CDIP, PDIP, SOIC, or TSSOP
(Top View)

Table 3-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	$\overline{I4}$	I	Active low input 4
2	$\overline{I5}$	I	Active low input 5
3	$\overline{I6}$	I	Active low input 6
4	$\overline{I7}$	I	Active low input 7
5	$\overline{I8}$	I	Active low input 8
6	$\overline{Y2}$	O	Active low output 2
7	$\overline{Y1}$	O	Active low output 1
8	GND	—	Ground
9	$\overline{I0}$	I	Active low input 0
10	$\overline{I9}$	I	Active low input 9
11	$\overline{I1}$	I	Active low input 1
12	$\overline{I2}$	I	Active low input 2
13	$\overline{I3}$	I	Active low input 3
14	$\overline{Y3}$	O	Active low output 3
15	NC	N/A	No internal connection
16	V_{CC}	—	Positive supply

1. I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input diode current	For V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output diode current	For V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Output source or sink current per output pin	For V_O > -0.5V or V_O < V_{CC} + 0.5V		±25	mA
	Continuous current through V_{CC} or GND			±50	mA

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6V		400	
T_A	Temperature range		-55	125	°C

4.3 Thermal Information

THERMAL METRIC		N (PDIP) 16 PINS	NS (SOP) 16 PINS	D (SOIC) 16 PINS	PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	67	64	117.2	137.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

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4.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
V_{IH}	High-level input voltage			2	1.5			1.5		1.5		V
				4.5	3.15			3.15		3.15		V
				6	4.2			4.2		4.2		V
V_{IL}	Low-level input voltage			2			0.5		0.5		0.5	V
				4.5			1.35		1.35		1.35	V
				6			1.8		1.8		1.8	V
V_{OH}	High-level output voltage CMOS loads	V_{IH} or V_{IL}	-0.02	2	1.9			1.9		1.9		V
			-0.02	4.5	4.4			4.4		4.4		V
			-0.02	6	5.9			5.9		5.9		V
	High-level output voltage TTL loads		–4	4.5	3.98			3.84		3.7		V
			–5.2	6	5.48			5.34		5.2		V
V_{OL}	Low-level output voltage CMOS loads	V_{IH} or V_{IL}	0.02	2			0.1		0.1		0.1	V
			0.02	4.5			0.1		0.1		0.1	V
			0.02	6			0.1		0.1		0.1	V
	Low-level output voltage TTL loads		4	4.5			0.26		0.33		0.4	V
			5.2	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} or GND		6			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_{CC} or GND	0	6			8		80		160	µA
HCT TYPES												
V_{IH}	High-level input voltage			4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High-level output voltage CMOS loads	V_{IH} or V_{IL}	-0.02	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads		-4	4.5	3.98			3.84		3.7		V
V_{OL}	Low-level output voltage CMOS loads	V_{IH} or V_{IL}	0.02	4.5			0.1		0.1		0.1	V
	Low-level output voltage TTL		4	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} and GND	0	5.5			±0.1		±1		±1	µA
I_{CC}	Quiescent device current	V_{CC} or GND	0	5.5			8		80		160	µA
ΔICC[(1)]	Additional quiescent device current per input pin: 1 Unit Load	V_{CC} -2.1		4.5 to 5.5		100	360		450		490	µA

(1) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.

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HCT Input Loading Table

4.4 Electrical Characteristics

INPUT	UNIT LOADS(1)
$\overline{I}_{\overline{1}}$, $\overline{I}_{\overline{2}}$, $\overline{I}_{\overline{3}}$, $\overline{I}_{\overline{6}}$, $\overline{I}_{\overline{7}}$	1.1
$\overline{I}_{\overline{4}}$, $\overline{I}_{\overline{5}}$, $\overline{I}_{\overline{8}}$, $\overline{I}_{\overline{9}}$	1.5

(1) Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25ºC.

4.5 Switching Characteristics

Input t_t = 6ns. Unless otherwise specified, C_L = 50pF

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_{PLH}, t_{PHL}	Propagation delay, input to output	C_L = 50pF	2			160		200		240	ns
			4.5			32		40		48	
			5		13						
			6			27		34		41	
t_{TLH}, t_{THL}	Transition times	C_L = 50pF	2			75		95		110	ns
			4.5			15		19		22	
			6			13		16		19	
C_{IN}	Input capacitance					10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)		5		32						pF
HCT TYPES											
t_{PLH}, t_{PHL}	Propagation delay, input to output	C_L = 50pF	4.5			35		44		53	ns
			5		14						ns
t_{TLH}, t_{THL}	Transition times	C_L = 50pF	4.5			15		19		22	ns
C_{IN}	Input capacitance					10		10		10	pF
C_{PD}	Power dissipation capacitance(1) (2)		5		42						pF

(1) C_{PD} is used to determine the dynamic power consumption, per gate.
(2) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

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5 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

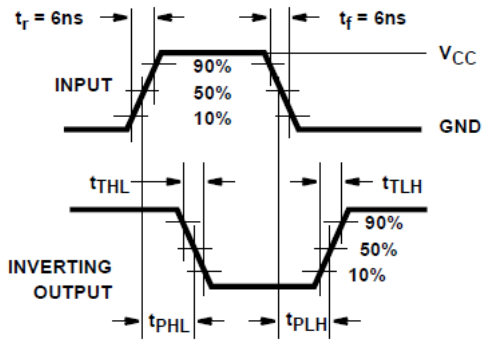

Figure 5-1. HC and HCU transition times and propagation delay times, combination logic

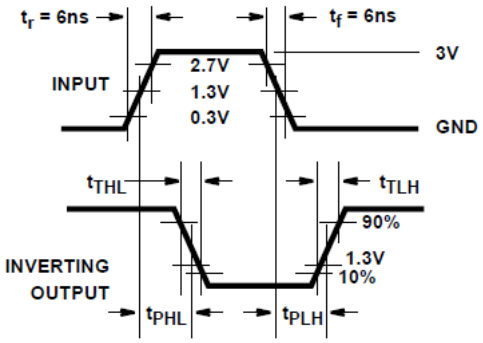

Figure 5-2. HCT transition times and propagation delay times, combination logic

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6 Detailed Description

6.1 Overview

The CDx4HC147 and CD74HCT147 devices are high speed silicon-gate CMOS devices and are pin-compatible with low power Schottky TTL (LSTTL).

The CDx4HC147 and CD74HCT147 9-input priority encoders accept data from nine active LOW inputs ($\overline{I1}$ to $\overline{I9}$) and provide binary representation on the four active LOW outputs ($\overline{Y0}$ to $\overline{Y3}$). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I9}$ having the highest priority.

These devices provide the 10-line to 4-line priority encoding function by use of the implied decimal “zero”. The “zero” is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

6.2 Functional Block Diagram

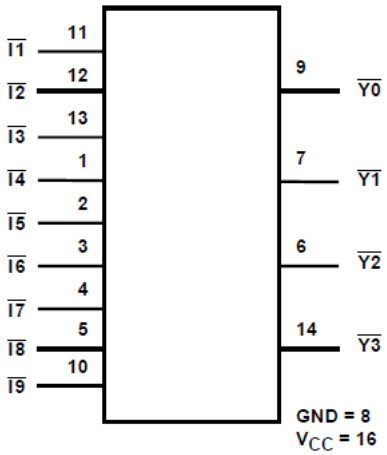

Figure 6-1. Functional Block Diagram

6.3 Device Functional Modes

Function Table lists the functional modes of the CDx4HC(T)147.

Table 6-1. Truth Table (1) (2) (3)

INPUTS									OUTPUTS			
$\overline{I1}$	$\overline{I2}$	$\overline{I3}$	$\overline{I4}$	$\overline{I5}$	$\overline{I6}$	$\overline{I7}$	$\overline{I8}$	$\overline{I9}$	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

(1) H = High logic level
(2) L = Low logic level
(3) X = Don't care

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

7.2.2 Layout Example

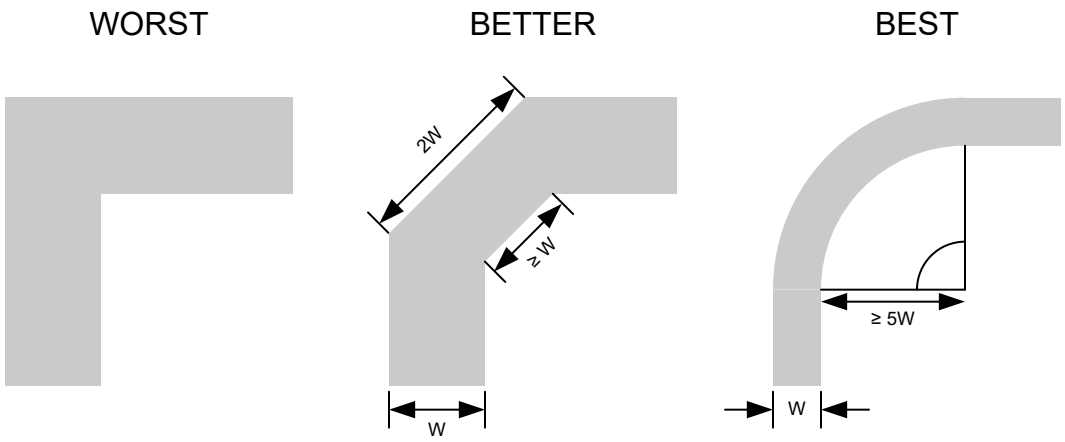

Figure 7-1. Example Trace Corners for Improved Signal Integrity

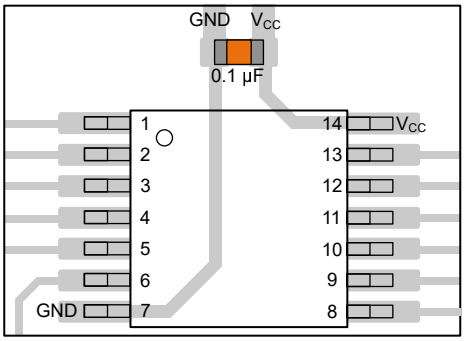

Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages

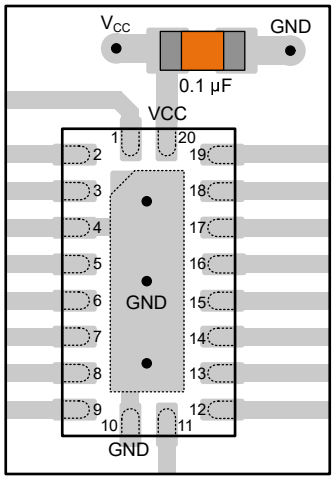

Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages

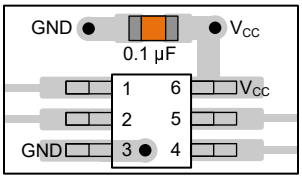

Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

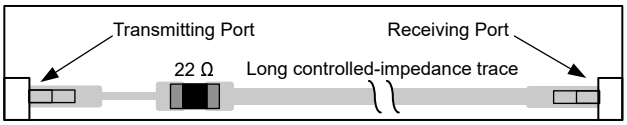

Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October 2003) to Revision G (January 2025)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards	1
• Added *Device Information* table, *Pin Functions* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated thermal values to reflect current function. D was 73 is now 117.2; PW was 108 is now 137.5	4

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8406401EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8406401EA CD54HC147F3A
CD54HC147F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8406401EA CD54HC147F3A
CD54HC147F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8406401EA CD54HC147F3A
CD74HC147E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC147E
CD74HC147E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC147E
CD74HC147M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC147M
CD74HC147M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC147M
CD74HC147M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC147M
CD74HC147M96G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC147M
CD74HC147M96G4.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC147M
CD74HC147MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC147M
CD74HC147PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ147
CD74HC147PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ147
CD74HC147PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ147
CD74HC147PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ147
CD74HCT147E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT147E
CD74HCT147E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT147E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC147, CD74HC147 :

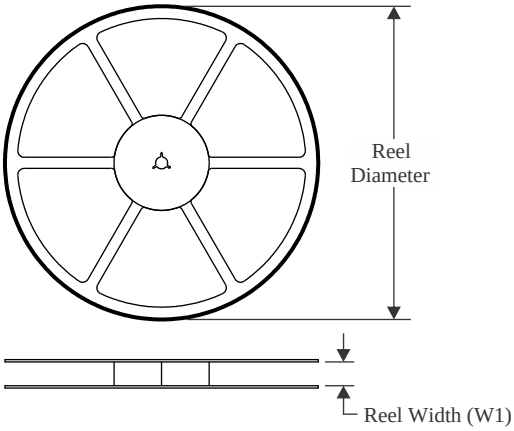
- Catalog : CD74HC147
- Military : CD54HC147

NOTE: Qualified Version Definitions:

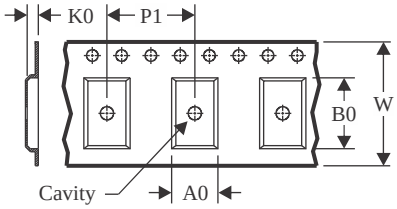
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

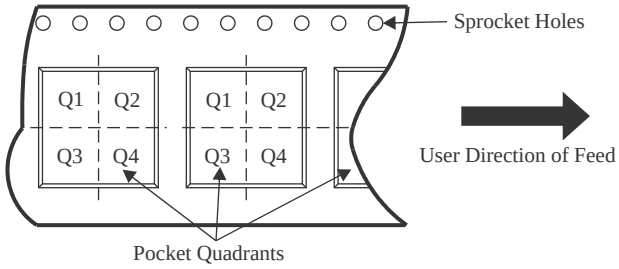


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

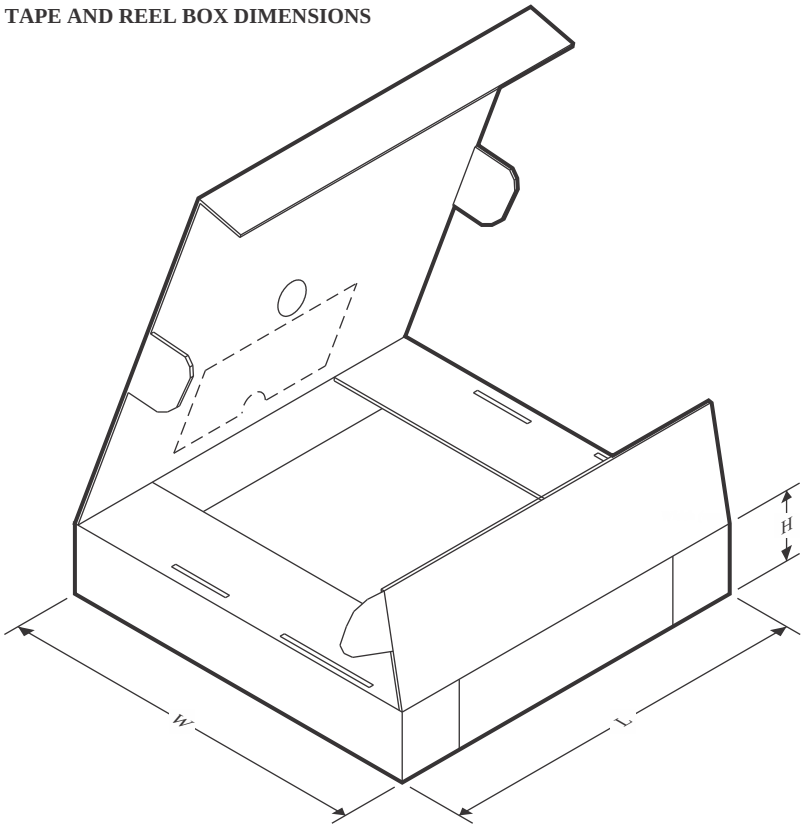
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC147M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC147PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

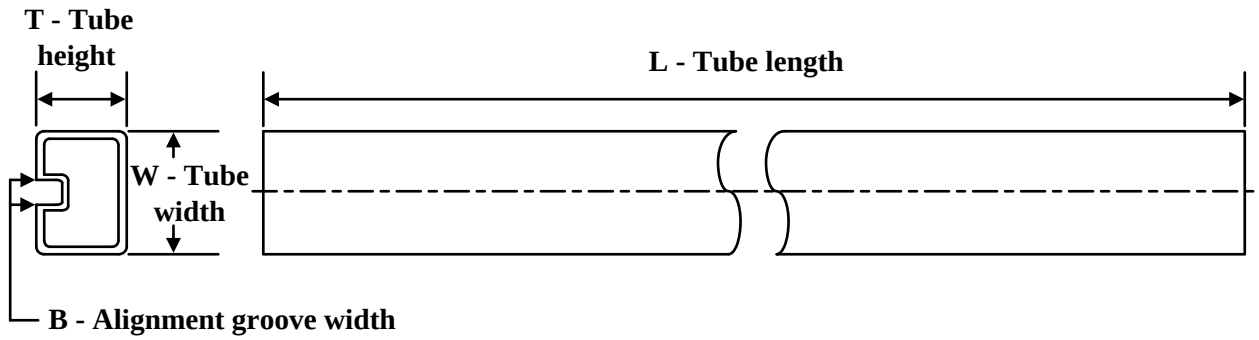
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC147M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC147PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

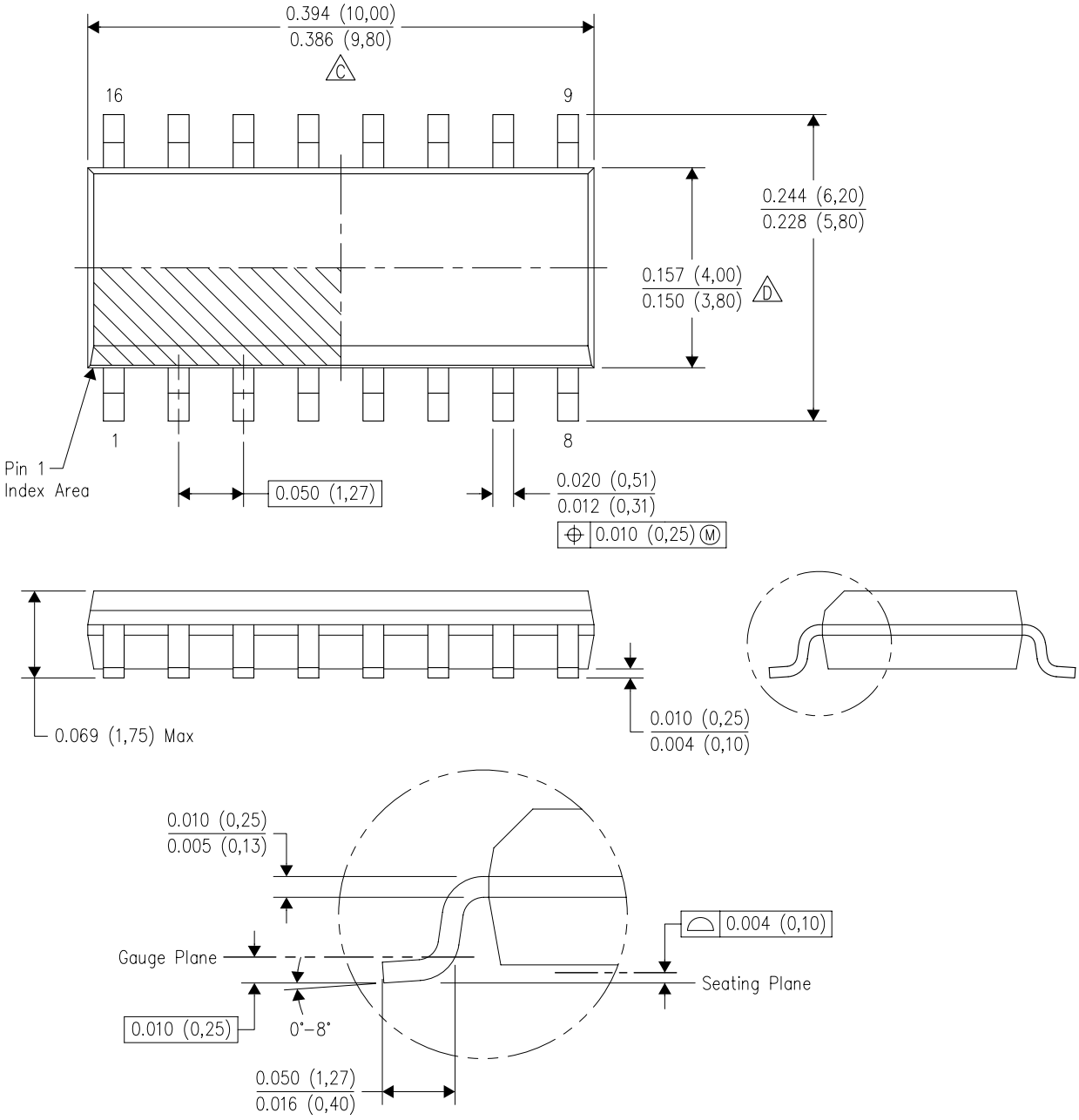
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC147E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC147E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC147E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC147E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT147E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT147E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT147E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT147E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

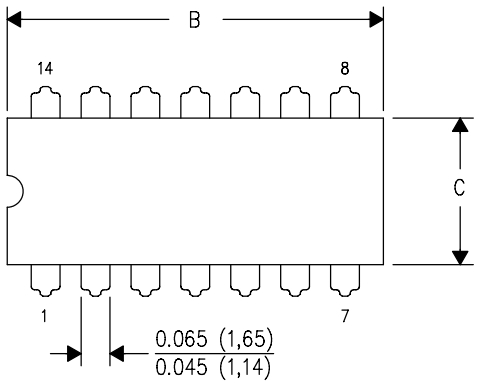


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

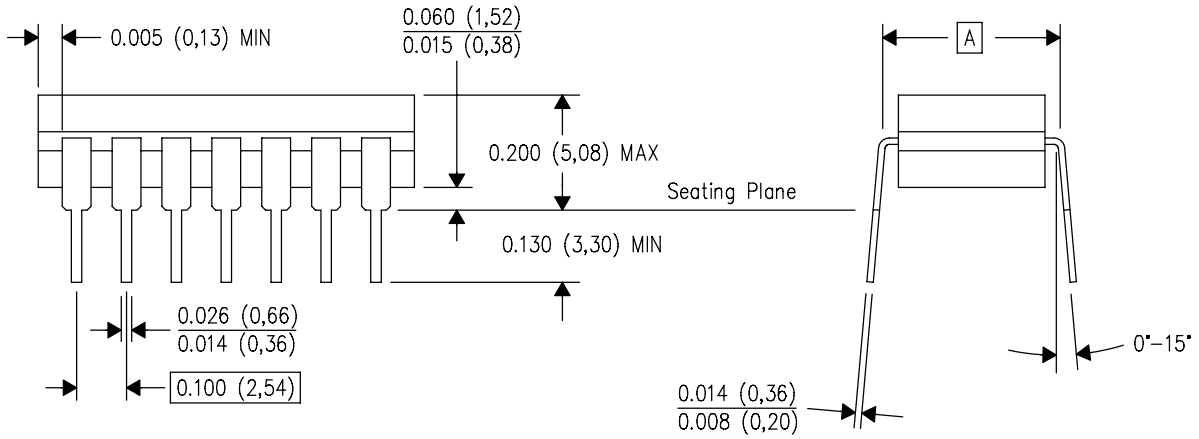
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

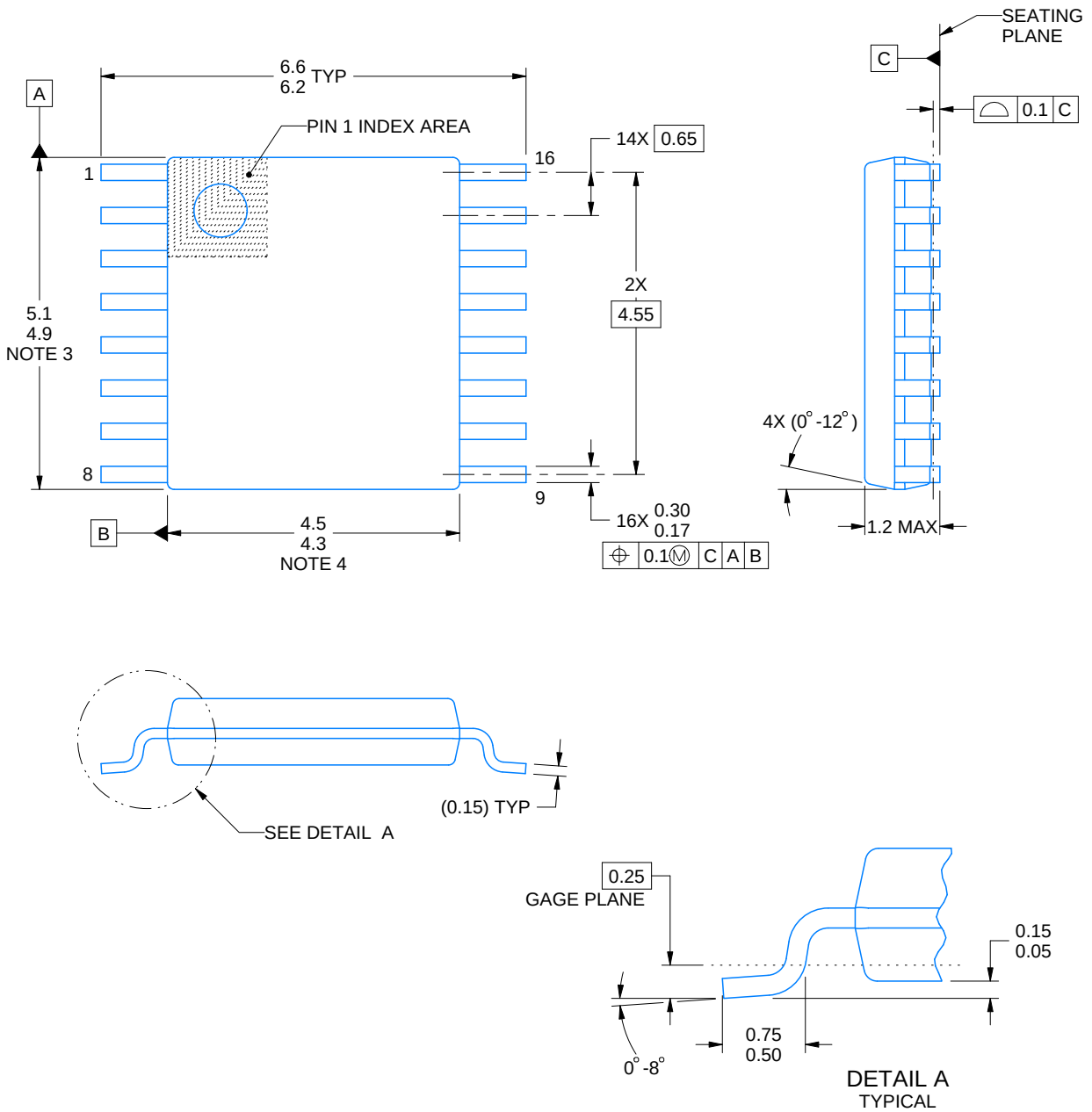
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

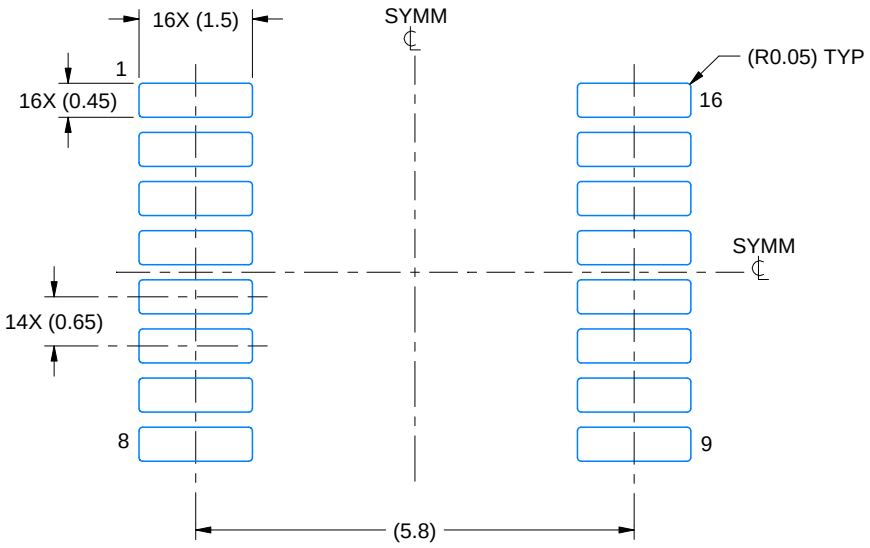
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



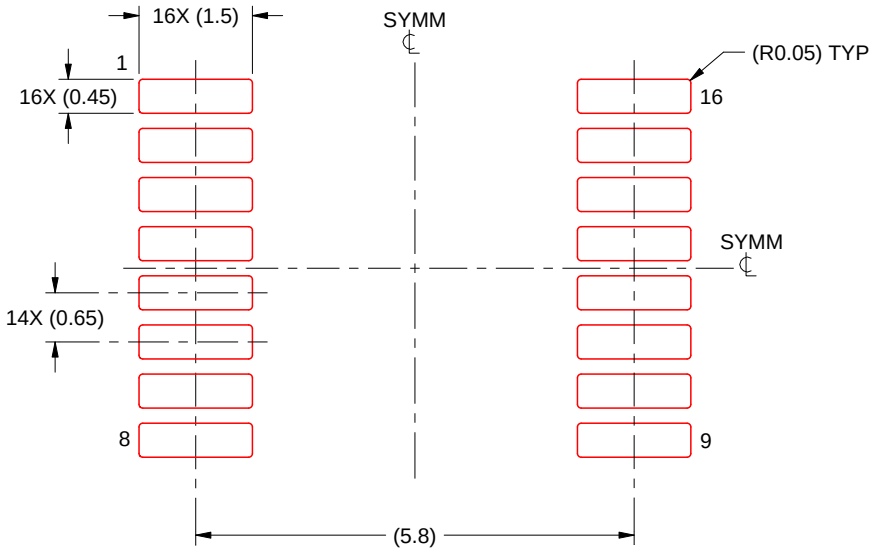
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

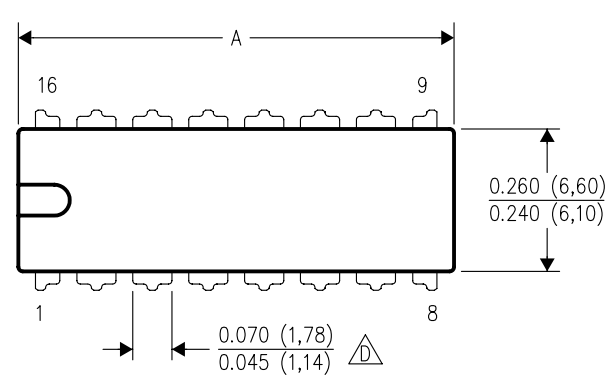
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

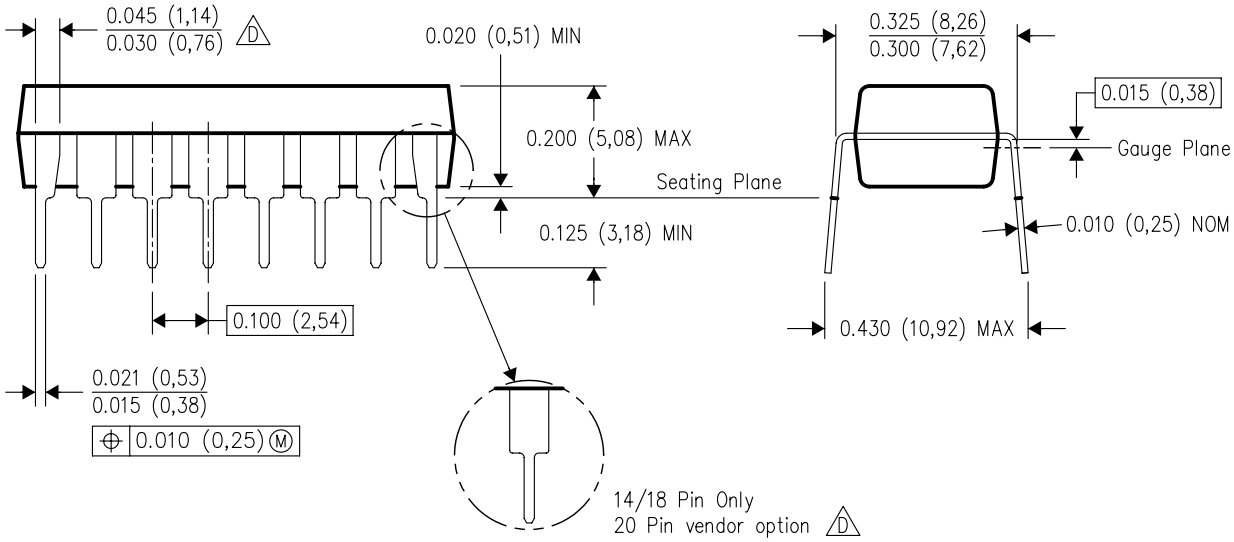
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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