

# CDx4HC688, CDx4HCT688 High-Speed CMOS Logic 8-Bit Magnitude Comparator

## 1 Features

- Cascadable
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL Loads
  - Bus driver outputs: 15 LSTTL Loads
- Wide operating temperature range:  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2 V to 6 V operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5 V to 5.5 V operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V}$  (max),  $V_{IH} = 2\text{ V}$  (min)
  - CMOS input compatibility,  $I_I \leq 1\text{ }\mu\text{A}$  at  $V_{OL}, V_{OH}$

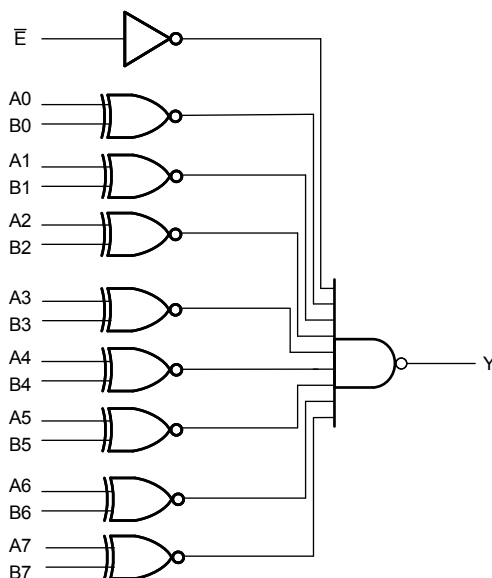
## 2 Description

The 'HC688 and 'HCT688 are 8-bit magnitude comparators designed for use in computer and logic applications that require the comparison of two 8-bit binary words. When the compared words are equal the output (Y) is low and can be used as the enabling input for the next device in a cascaded application.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD74HC688M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT688M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC688E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT688E	PDIP (20)	25.40 mm × 6.35 mm
CD74HC688NSR	SO (20)	15.00 mm × 5.30 mm
CD74HC688PWR	TSSOP (20)	6.50 mm × 4.40 mm
CD54HC688F3A	CDIP (20)	26.92 mm × 6.92 mm
CD54HCT688F3A	CDIP (20)	26.92 mm × 6.92 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagram



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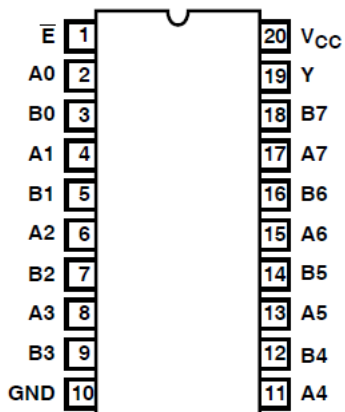
## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (February 2022) to Revision E (October 2022)</b>	<b>Page</b>
• Increased R $\theta$ JA for packages: DW (58 to 109.1); N (69 to 84.6); NS (60 to 113.4); PW (83 to 131.8).....	<b>4</b>

<b>Changes from Revision C (August 2003) to Revision D (February 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	<b>1</b>

## 4 Pin Configuration and Functions



J, N, DW, NS, or PW package  
20-Pin CDIP, PDIP, SOIC, SO, TSSOP  
Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		–0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < –0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>OK</sub>	Output diode current	For V <sub>O</sub> < –0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20	mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > –0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±50	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature range		–65	150	°C
	Lead temperature (Soldering 10s) (SOIC - lead tips only)			300	°C

- (1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress-only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### 5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V <sub>I</sub> , V <sub>O</sub>	Input or output voltage		0	V <sub>CC</sub>	V
t <sub>t</sub>	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T <sub>A</sub>	Temperature range		–55	125	°C

### 5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	109.1	84.6	113.4	131.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	76	72.5	78.6	72.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	77.6	65.3	78.4	82.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	51.5	55.3	47.1	21.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	77.1	65.2	78.1	82.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V <sub>IH</sub>	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V <sub>IL</sub>	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		
			6	1.8			1.8		1.8		
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = –20 µA	2	1.9			1.9		1.9		V
		I <sub>OH</sub> = –20 µA	4.5	4.4			4.4		4.4		
		I <sub>OH</sub> = –20 µA	6	5.9			5.9		5.9		
	High level output voltage	I <sub>OH</sub> = –4 mA	4.5	3.98			3.84		3.7		
		I <sub>OH</sub> = –5.2 mA	6	5.48			5.34		5.2		
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 µA	2	0.1			0.1		0.1		V
		I <sub>OL</sub> = 20 µA	4.5	0.1			0.1		0.1		
		I <sub>OL</sub> = 20 µA	6	0.1			0.1		0.1		
	Low level output voltage	I <sub>OL</sub> = 4 mA	4.5	0.26			0.33		0.4		
		I <sub>OL</sub> = 5.2 mA	6	0.26			0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	±0.1			±1		±1		µA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	8			80		160		µA
HCT TYPES											
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2			2		2		V
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = –20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage	I <sub>OH</sub> = –4 mA	4.5	3.98			3.84		3.7		
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 µA	4.5	0.1			0.1		0.1		V
	Low level output voltage	I <sub>OL</sub> = 4 mA	4.5	0.26			0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	±0.1			±1		±1		µA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	8			80		160		µA
ΔI <sub>CC</sub> <sup>(1)</sup>	Additional supply current per input pin	Enable inputs held at V <sub>CC</sub> –2.1	4.5 to 5.5	100 252			315		343		µA
		Data inputs held at V <sub>CC</sub> –2.1	4.5 to 5.5	100 126			157.5		171.5		µA

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>.

## 5.5 Switching Characteristics

$C_L = 50\text{pF}$ . Input  $t_r$ ,  $t_f = 6\text{ ns}$

PARAMETER		V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay (Figure 6-1) An to output	2			170		210		255	ns
		4.5		14 <sup>(3)</sup>	34		42		51	
		6			29		36		43	
t <sub>PLH</sub> , t <sub>PHL</sub>	Bn to output	2			170		210		255	ns
		4.5		14 <sup>(3)</sup>	34		42		51	
		6			29		36		43	
t <sub>PLH</sub> , t <sub>PHL</sub>	E̅ to output	2			120		150		180	ns
		4.5		9 <sup>(3)</sup>	24		30		36	
		6			20		26		30	
t <sub>TLH</sub> , t <sub>THL</sub>	Output transition time (Figure 6-1)	2			75		95		110	ns
		4.5			15		19		22	
		6			13		16		19	
C <sub>IN</sub>	Input capacitance				10		10		10	pF
C <sub>PD</sub>	Power dissipation capacitance <sup>(1) (2)</sup>				22 <sup>(4)</sup>					pF
HCTYPES										
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay (Figure 6-1) An to output	4.5		14 <sup>(3)</sup>	34		42		51	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Bn to output	4.5		14 <sup>(3)</sup>	34		42		51	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	E̅ to output	4.5		9 <sup>(3)</sup>	24		30		36	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Output transition time (Figure 6-1)	4.5			15		19		22	ns
C <sub>IN</sub>	Input capacitance				10		10		10	pF
C <sub>PD</sub>	Power dissipation capacitance <sup>(1) (2)</sup>	5		22 <sup>(4)</sup>						pF

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per gate.

(2)  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

(3)  $C_L = 15\text{ pF}$  and  $V_{CC} = 5\text{ V}$ .

(4)  $C_L = 15\text{ pF}$ .

## 6 Parameter Measurement Information

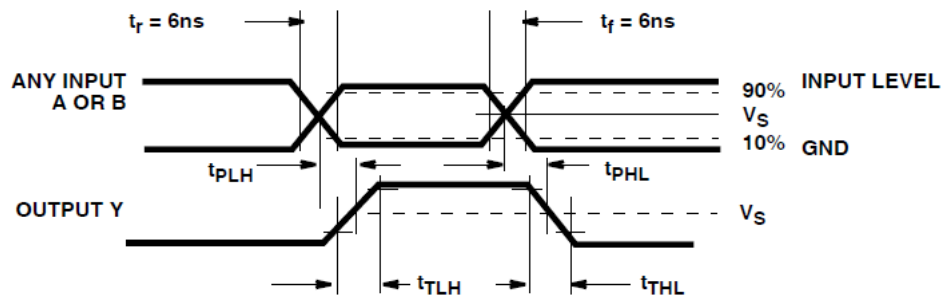


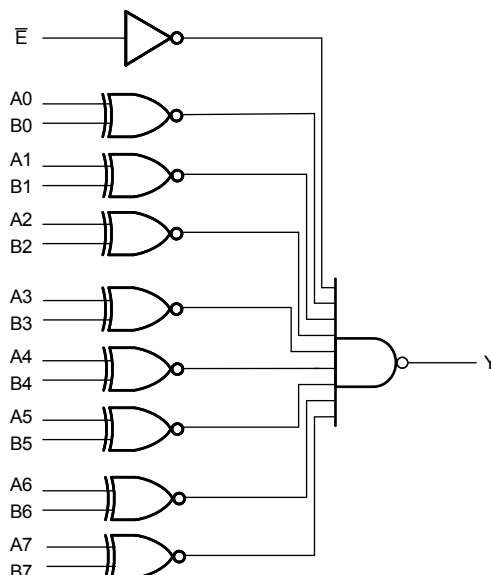
Figure 6-1. Propagation Delay and Transition Times

## 7 Detailed Description

### 7.1 Overview

The 'HC688 and 'HCT688 are 8-bit magnitude comparators designed for use in computer and logic applications that require the comparison of two 8-bit binary words. When the compared words are equal the output (Y) is low and can be used as the enabling input for the next device in a cascaded application.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

Table 7-1. Truth Table<sup>(1)</sup>

INPUTS		OUTPUTS
A, B	$\bar{E}$	Y
A = B	L	L
A $\neq$ B	L	H
X	H	H

(1) H = high voltage level, L = low voltage level, X = don't care.



## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-8685701RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8685701RA CD54HCT688F3A
<a href="#">CD54HC688F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681801RA CD54HC688F3A
CD54HC688F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8681801RA CD54HC688F3A
<a href="#">CD54HCT688F</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT688F
CD54HCT688F.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT688F
<a href="#">CD54HCT688F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8685701RA CD54HCT688F3A
CD54HCT688F3A.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8685701RA CD54HCT688F3A
<a href="#">CD74HC688E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC688E
CD74HC688E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC688E
<a href="#">CD74HC688M</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HC688M
<a href="#">CD74HC688M96</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC688M
CD74HC688M96.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC688M
<a href="#">CD74HC688NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC688M
CD74HC688NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC688M
<a href="#">CD74HC688PWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ688
CD74HC688PWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ688
<a href="#">CD74HC688PWT</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-55 to 125	HJ688
<a href="#">CD74HCT688E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT688E
CD74HCT688E.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT688E
CD74HCT688EE4	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT688E
<a href="#">CD74HCT688M96</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT688M
CD74HCT688M96.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT688M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC688, CD54HCT688, CD74HC688, CD74HCT688 :**

- Catalog : [CD74HC688](#), [CD74HCT688](#)
- Military : [CD54HC688](#), [CD54HCT688](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

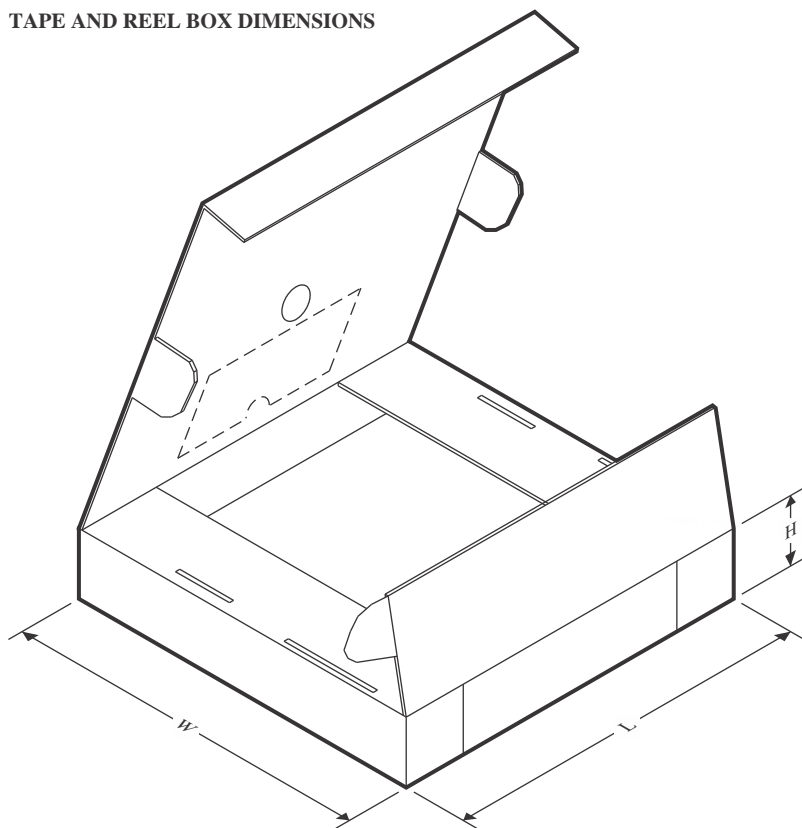
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC688M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC688NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
CD74HC688PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
CD74HCT688M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HCT688M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC688M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HC688NSR	SOP	NS	20	2000	356.0	356.0	45.0
CD74HC688PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
CD74HCT688M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT688M96	SOIC	DW	20	2000	356.0	356.0	45.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC688E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC688E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT688E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT688E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT688EE4	N	PDIP	20	20	506	13.97	11230	4.32



## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



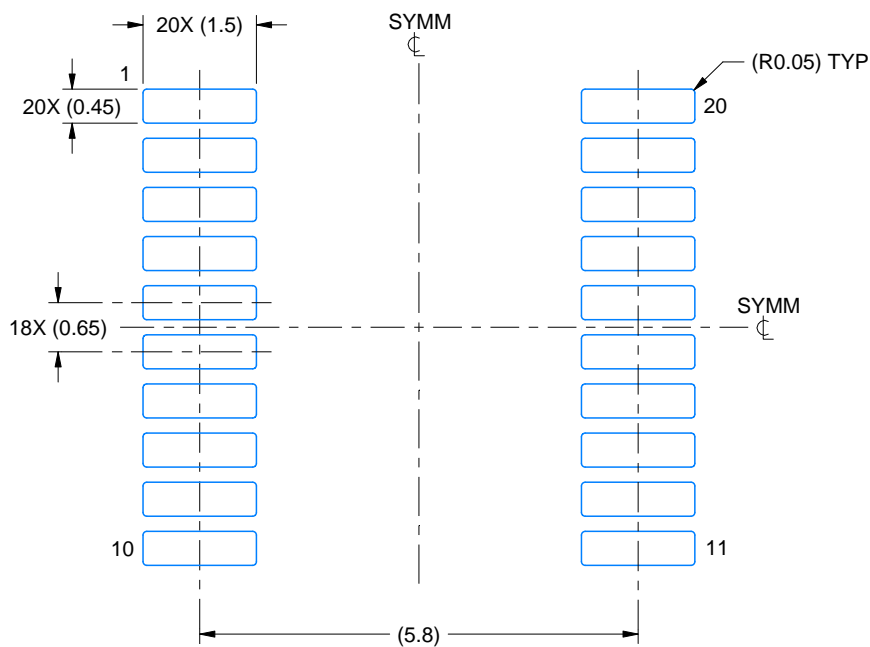
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



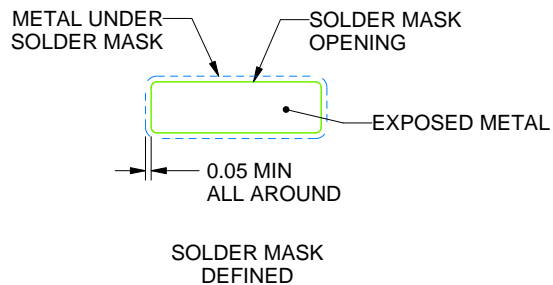
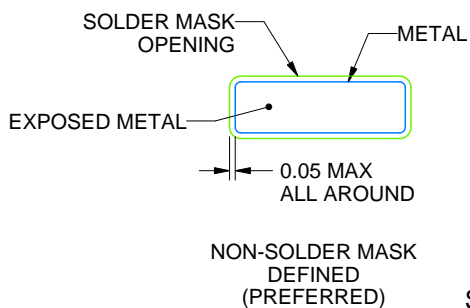
**PW0020A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

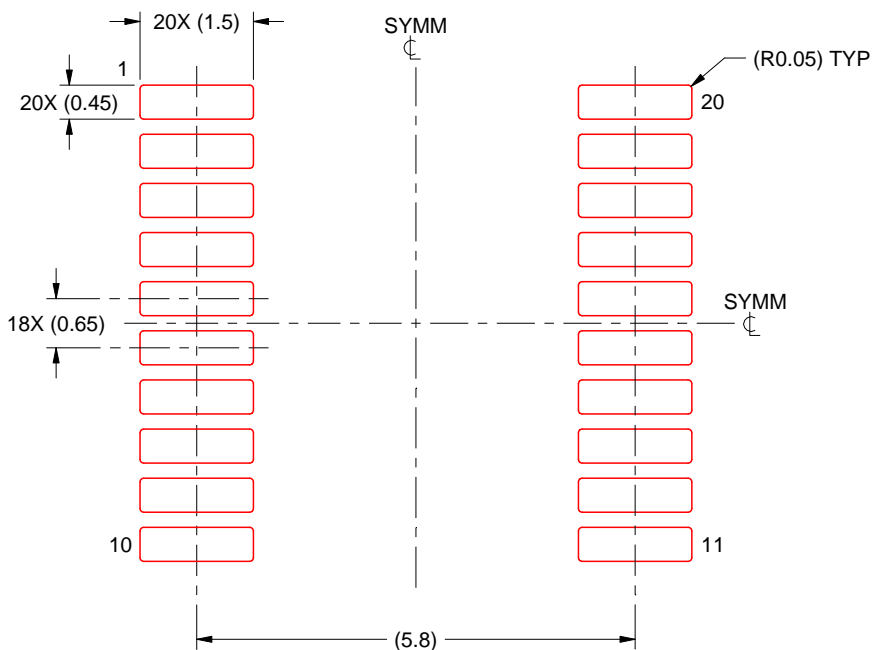
6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

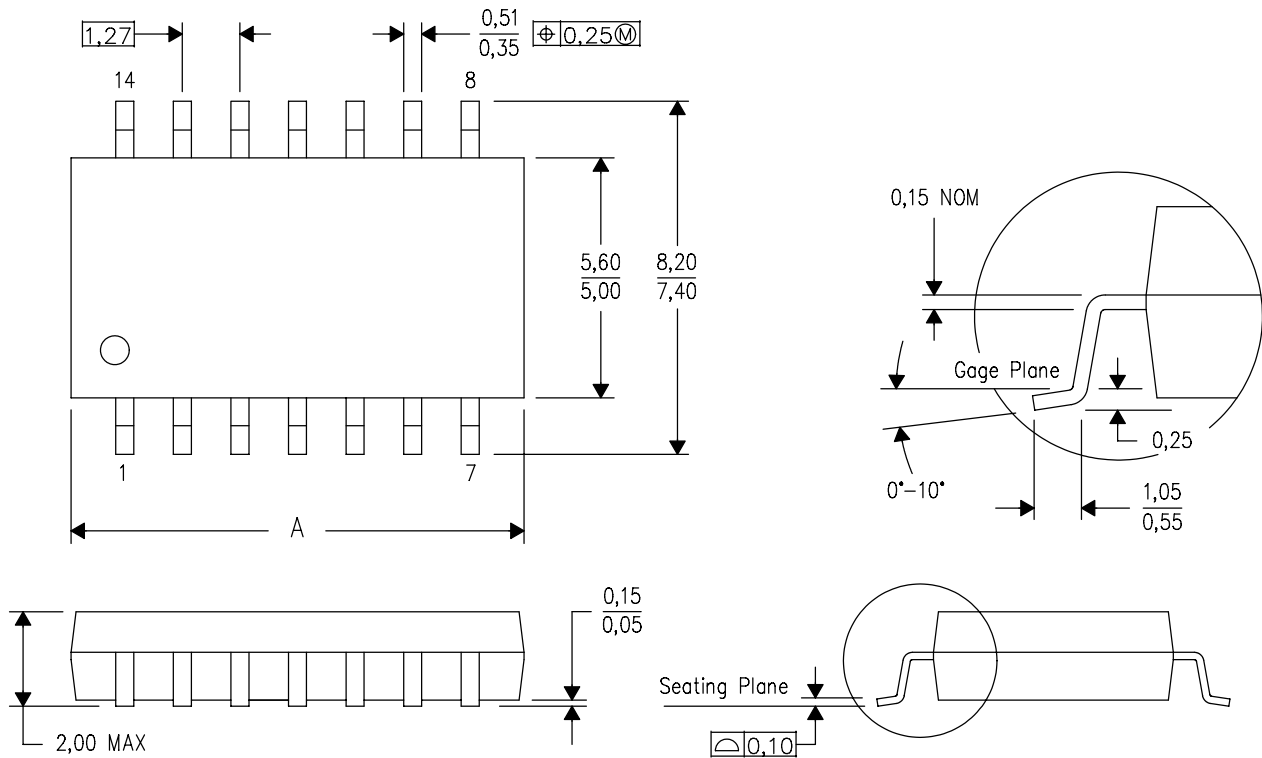
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

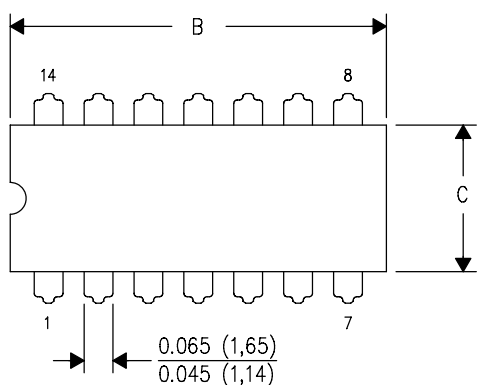
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

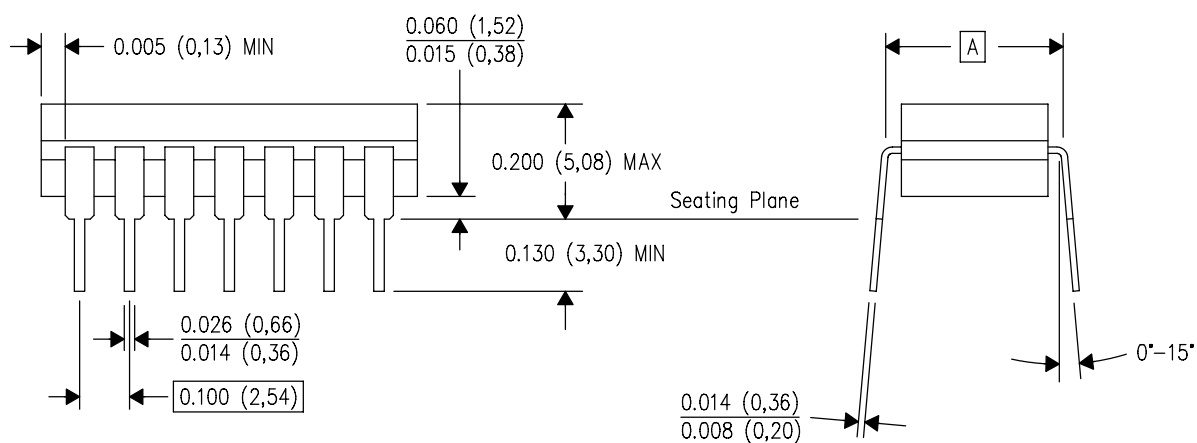
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



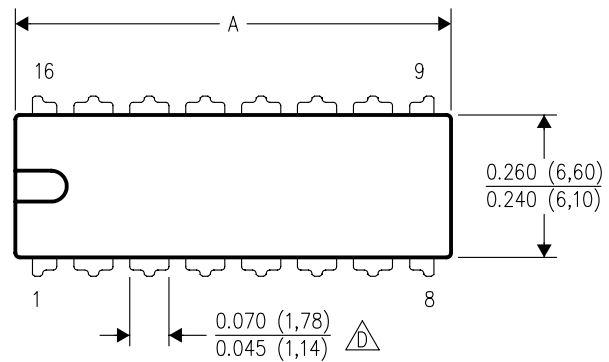
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

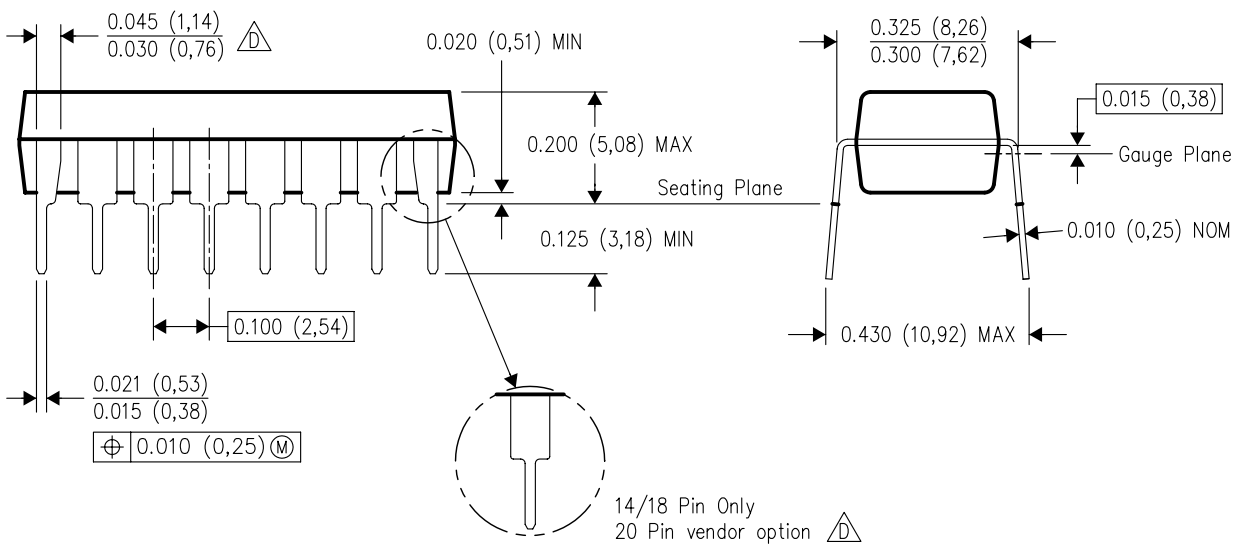
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



**SOIC - 2.65 mm max height**

Technical drawing of a 20-pin connector, showing top, side, and detail views with dimensions and feature callouts.

**Top View:**

- Overall width: 10.63 (9.97 TYP)
- Overall height: 13.0 (12.6 NOTE 3)
- Pin 1 ID Area: Indicated by a dotted rectangle.
- Pin 1 location: 7.6 (7.4 NOTE 4) from the left edge.
- Pin 11 location: 11.43 (2X) from the bottom edge.
- Pin 20 location: 1.27 (18X) from the top edge.
- Pin 10 location: 10.63 (9.97 TYP) from the left edge.
- Pin 11 location: 11.43 (2X) from the bottom edge.
- Pin 20 location: 1.27 (18X) from the top edge.

**Side View:**

- Seating Plane: Indicated by a dashed line.
- Pin 1 ID Area: Indicated by a dotted rectangle.
- Pin 1 location: 7.6 (7.4 NOTE 4) from the left edge.
- Pin 11 location: 11.43 (2X) from the bottom edge.
- Pin 20 location: 1.27 (18X) from the top edge.
- Pin 10 location: 10.63 (9.97 TYP) from the left edge.
- Pin 11 location: 11.43 (2X) from the bottom edge.
- Pin 20 location: 1.27 (18X) from the top edge.

**Detail A (Typical):**

- Pin 1 ID Area: Indicated by a dotted rectangle.
- Pin 1 location: 7.6 (7.4 NOTE 4) from the left edge.
- Pin 11 location: 11.43 (2X) from the bottom edge.
- Pin 20 location: 1.27 (18X) from the top edge.
- Pin 10 location: 10.63 (9.97 TYP) from the left edge.
- Pin 11 location: 11.43 (2X) from the bottom edge.
- Pin 20 location: 1.27 (18X) from the top edge.

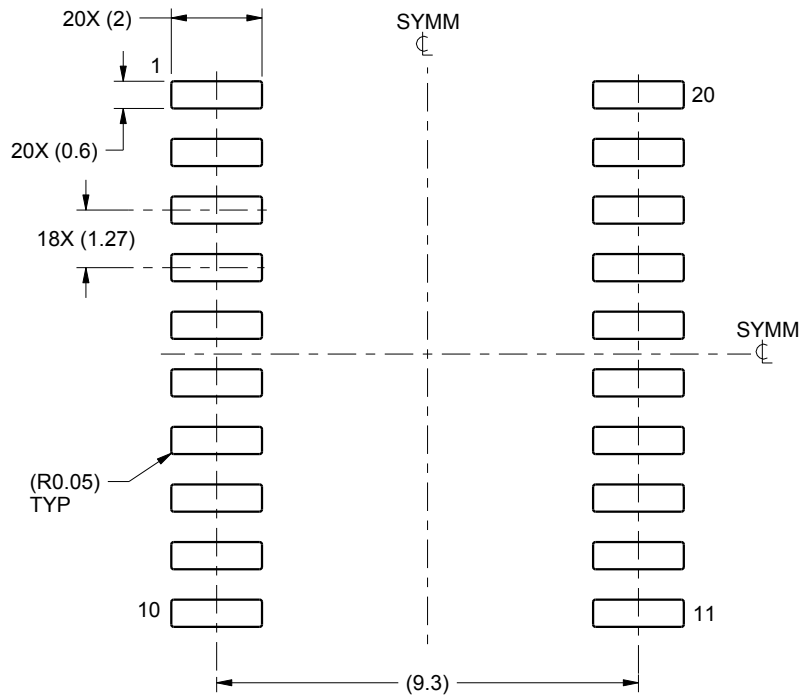
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

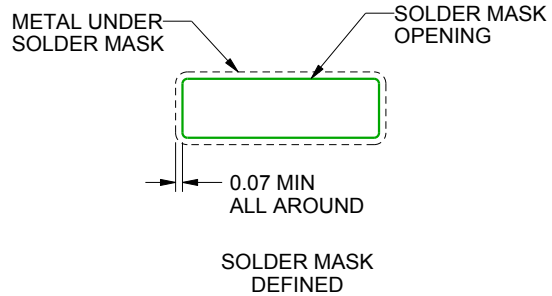
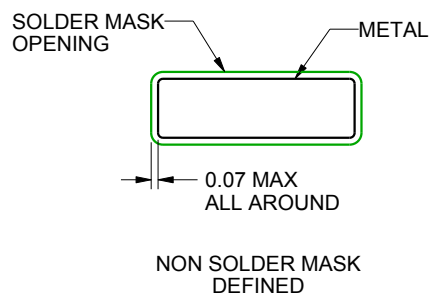
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

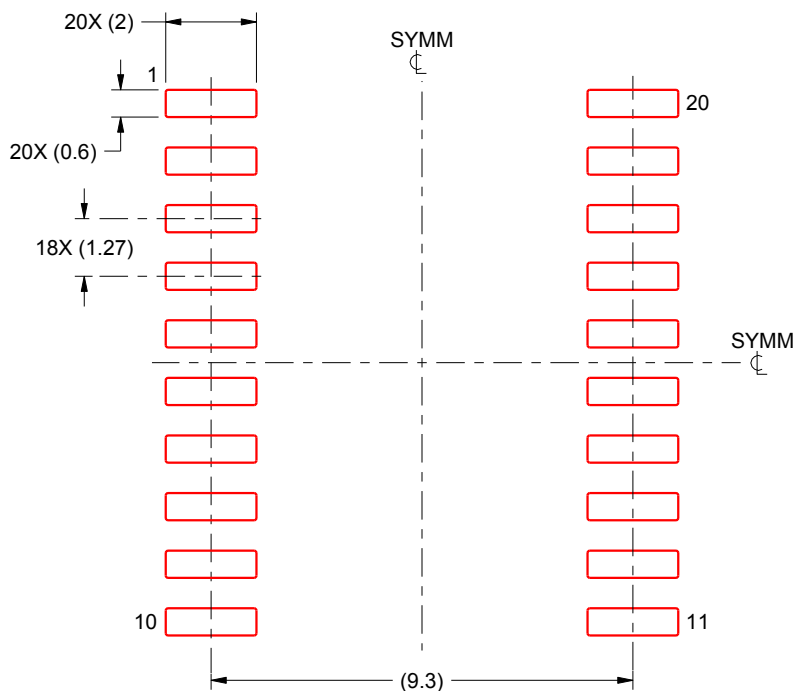
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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