CD74HC4518, CD54HC4520, CD74HC4520, CD74HCT4520

Data sheet acquired from Harris Semiconductor
SCHS216D

November 1997 - Revised October 2003

High-Speed CMOS Logic Dual Synchronous Counters

Features

- **Positive or Negative Edge Triggering**
- **Synchronous Internal Carry Propagation**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The CD74HC4518 is a dual BCD up-counter. The 'HC4520 and CD74HCT4520 are dual binary up-counters. Each device consists of two independent internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or the negative-going transition of CLOCK. The counters are cleared by high levels on the MASTER RESET lines. The counter can be cascaded in the ripple mode by connecting Q_3 to the ENABLE input of the subsequent counter while the CLOCK input of the latter is held low.

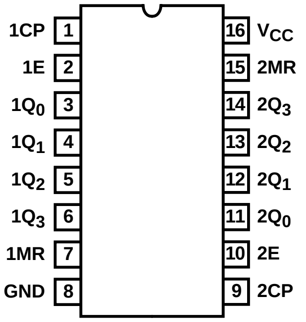
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4520F3A	-55 to 125	16 Ld CERDIP
CD74HC4518E	-55 to 125	16 Ld PDIP
CD74HC4520E	-55 to 125	16 Ld PDIP
CD74HC4520M	-55 to 125	16 Ld SOIC
CD74HC4520MT	-55 to 125	16 Ld SOIC
CD74HC4520M96	-55 to 125	16 Ld SOIC
CD74HCT4520E	-55 to 125	16 Ld PDIP
CD74HCT4520M	-55 to 125	16 Ld SOIC
CD74HCT4520MT	-55 to 125	16 Ld SOIC
CD74HCT4520M96	-55 to 125	16 Ld SOIC

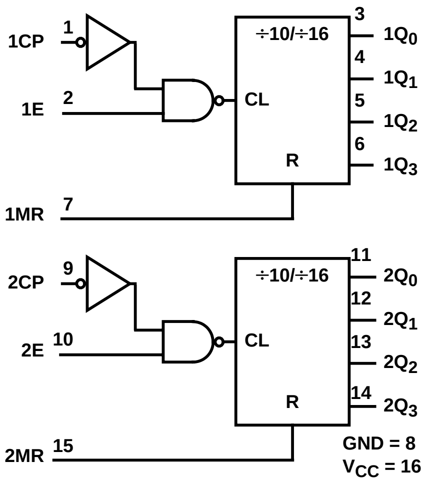
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

**CD54HC4520
(CERDIP)
CD74HC4518
(PDIP)
CD74HC4520, CD74HCT4520,
(PDIP, SOIC)**
TOP VIEW



Functional Diagram



TRUTH TABLE

CP	E	MR	OUTPUT STATE
↑	H	L	Increment Counter
L	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q_0 thru Q_3 = L

H = High State.

L = Low State.

↑ = High-to-Low Transition.

↓ = Low-to-High Transition.

X = Don’t Care.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
  For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . ±20mA
DC Output Diode Current, I_{OK}
  For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
  For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . ±50mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
  E (PDIP) Package 67
  M (SOIC) Package. 73
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
  (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
  HC Types . . . . 2V to 6V
  HCT Types . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Time
  2V . . . . 1000ns (Max)
  4.5V. . . . . 500ns (Max)
  6V . . . . 400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		VCC (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
MR	1.2
CP	0.25
ENABLE	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Maximum Clock Frequency	f_{MAX}	2	6	-	-	5	-	4	-	MHz
		4.5	30	-	-	24	-	20	-	MHz
		6	35	-	-	28	-	24	-	MHz
CP Pulse Width	t_W	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR Pulse Width	t_W	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns

Prerequisite for Switching Specifications **(Continued)**

PARAMETER	SYMBOL	V_{CC} (V)	$25^{o}C$			$-40^{o}C$ TO $85^{o}C$		$-55^{o}C$ TO $125^{o}C$		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Set-up Time, Enable to CP	t_{SU}	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Removal Time, MR to CP	t_{REM}	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Set-up Time, CP to Enable	t_{SU}	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Removal Time, MR to Enable	t_{REM}	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
HCT TYPES										
Maximum Clock Frequency	f_{MAX}	4.5	25	-	-	20	-	17	-	MHz
Clock Pulse Width	t_W	4.5	20	-	-	25	-	30	-	ns
MR Pulse Width	t_W	4.5	20	-	-	25	-	30	-	ns
Set-up Time, Enable to CP	t_{SU}	4.5	16	-	-	20	-	24	-	ns
Removal Time, MR tp Enable	t_{REM}	4.5	0	-	-	0	-	0	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	$25^{o}C$			$-40^{o}C$ TO $85^{o}C$		$-55^{o}C$ TO $125^{o}C$		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay CP to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	240	-	300	-	360	ns
		C_L = 50pF	4.5	-	-	48	-	60	-	72	ns
		C_L = 15pF	5	-	20	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	41	-	51	-	61	ns
Enable to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	240	-	300	-	360	ns
		C_L = 50pF	4.5	-	-	48	-	60	-	72	ns
		C_L = 15pF	5	-	20	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	41	-	51	-	61	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	150	-	190	-	225	ns
		C_L = 50pF	4.5	-	-	30	-	38	-	45	ns
		C_L = 15pF	5	-	12	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	26	-	33	-	38	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
		C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
		CL = 50pF	6			13		16		19	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f_{MAX}	CL = 15pF	5		60						MHz
Power Dissipation Capacitance (Note 3, 4)	C_{PD}	C_L = 15pF	5	-	33	-	-	-	-	-	pF

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HCT TYPES											
Propagation Delay CP to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	53	-	66	-	80	ns
		C_L = 15pF	5	-	22	-	-	-	-	-	ns
Enable to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C_L = 15pF	5	-	23	-	-	-	-	-	ns
MR to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	35	-	44	-	53	ns
		C_L = 15pF	5	-	14	-	-	-	-	-	ns
Output Transition Time	t_{THL}, t_{TLH}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Maximum Clock Frequency	f_{MAX}	CL = 15pF	5	-	50	-	-	-	-	-	MHz
Power Dissipation Capacitance (Note 3,4)	C_{PD}	-	5	-	33	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per counter.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Timing Diagram

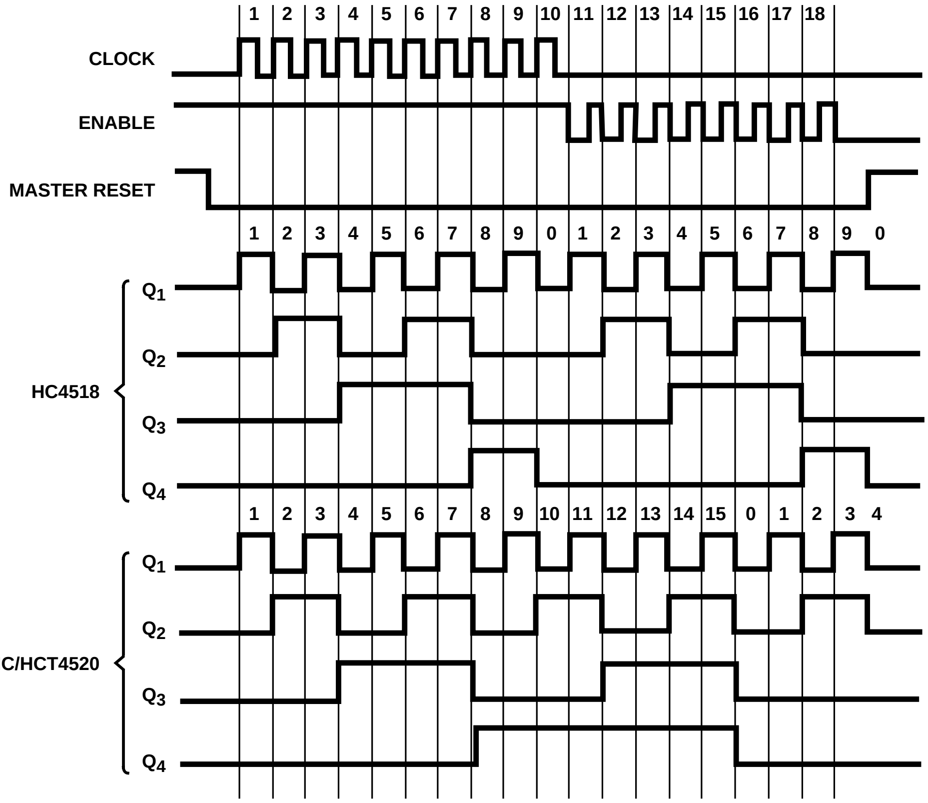
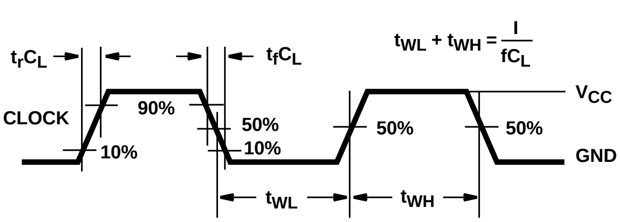


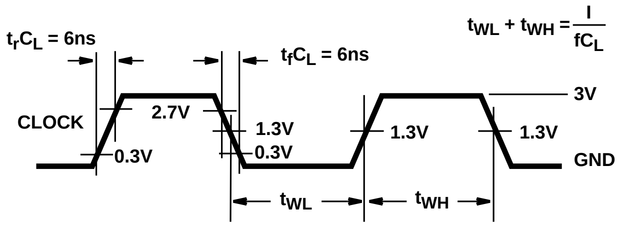
FIGURE 1.

Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 3. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

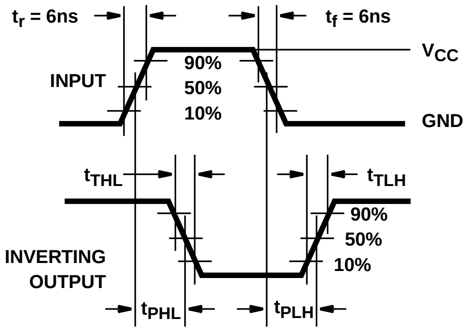


FIGURE 4. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

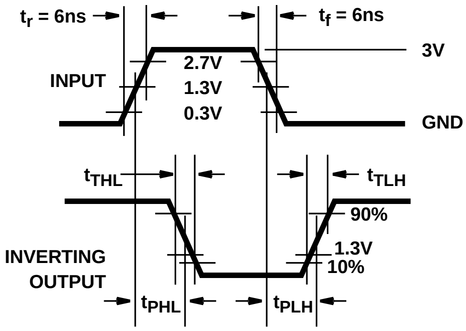


FIGURE 5. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

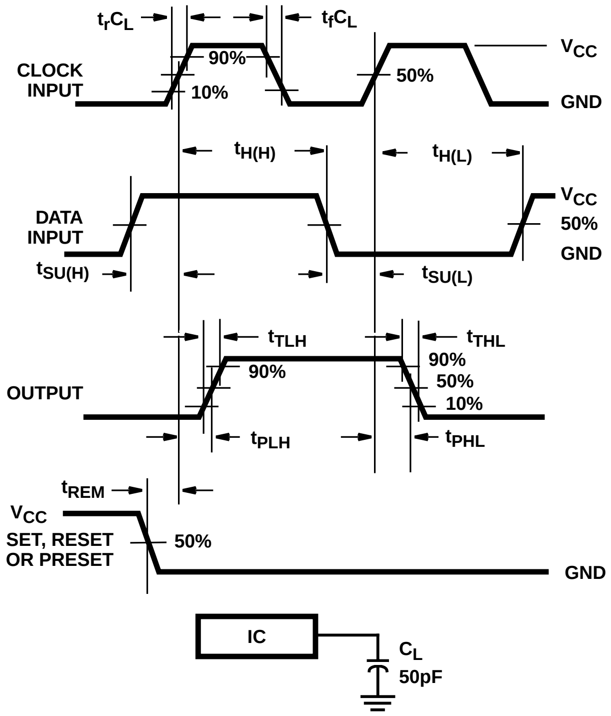


FIGURE 6. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

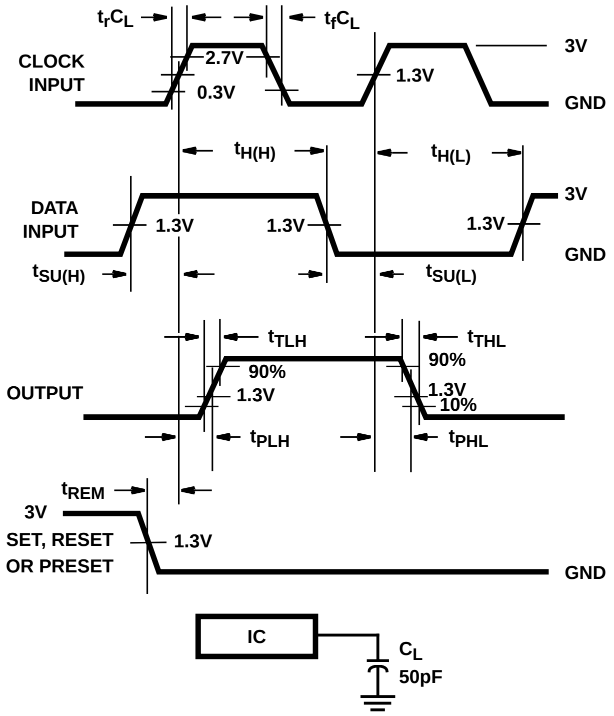


FIGURE 7. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8995401EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8995401EA CD54HC4520F3A
CD54HC4520F	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4520F
CD54HC4520F.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4520F
CD54HC4520F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8995401EA CD54HC4520F3A
CD54HC4520F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8995401EA CD54HC4520F3A
CD74HC4518E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4518E
CD74HC4518E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4518E
CD74HC4520E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4520E
CD74HC4520E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4520E
CD74HC4520M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4520M
CD74HC4520M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4520M
CD74HC4520M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4520M
CD74HC4520M96G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4520M
CD74HC4520MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4520M
CD74HCT4520E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4520E
CD74HCT4520E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4520E
CD74HCT4520M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT4520M
CD74HCT4520M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4520M
CD74HCT4520M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4520M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4520, CD74HC4520 :

- Catalog : CD74HC4520

- Military : CD54HC4520

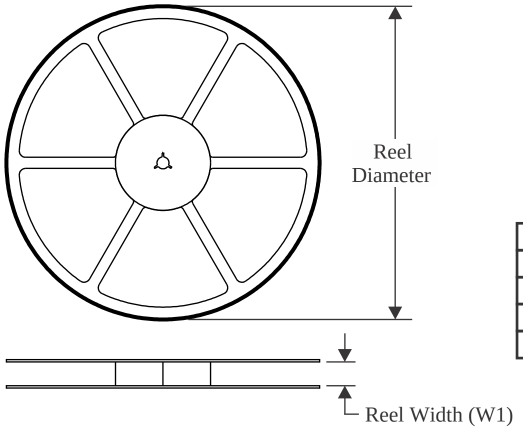
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

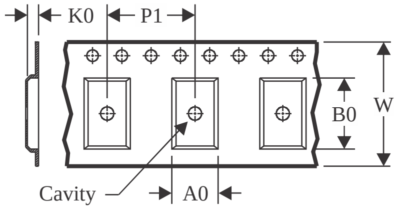
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

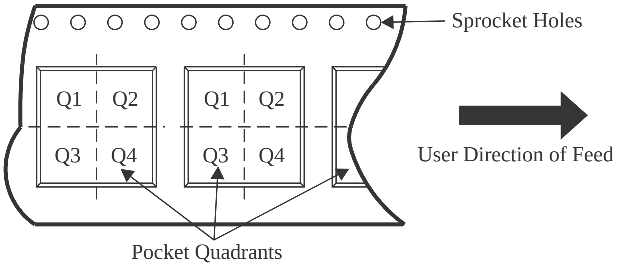


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

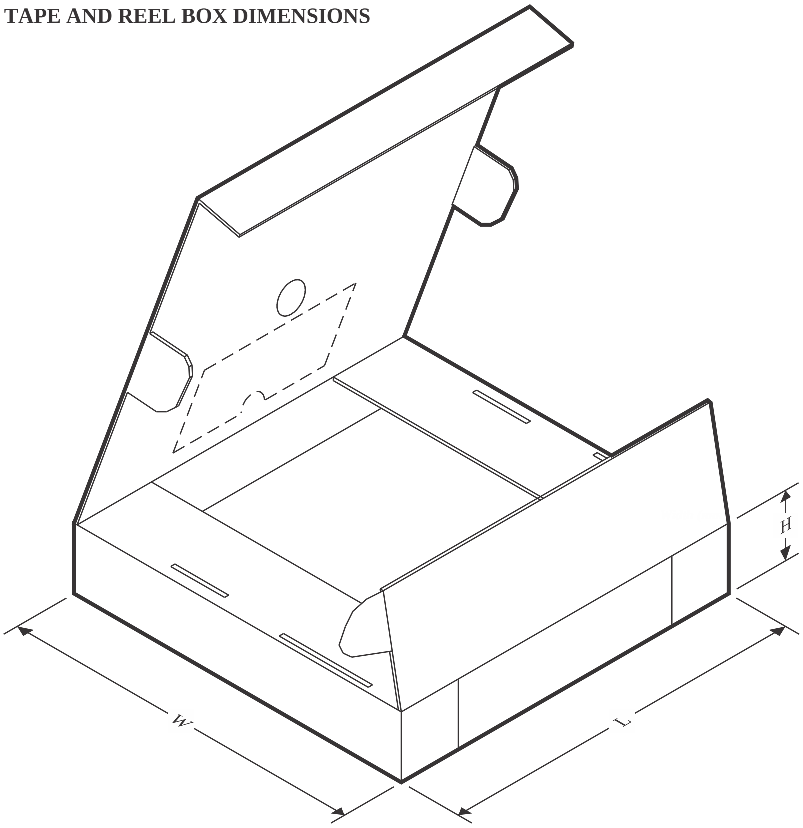
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4520M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4520M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

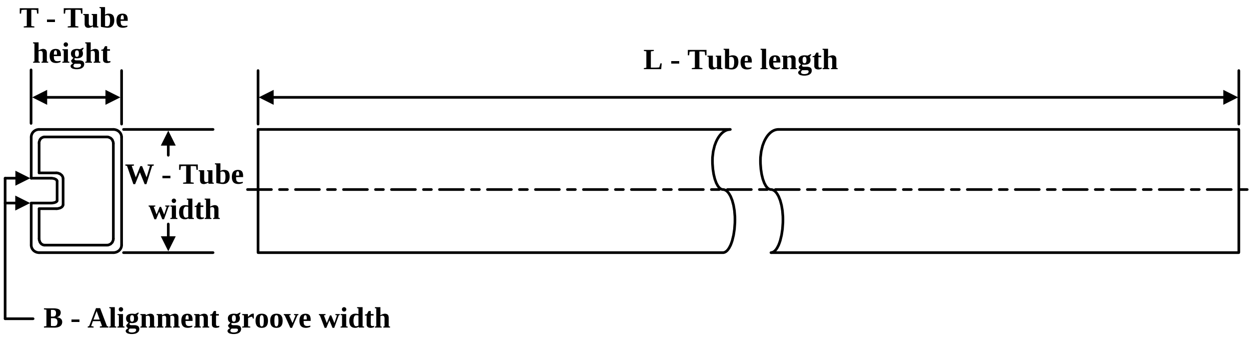
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4520M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT4520M96	SOIC	D	16	2500	353.0	353.0	32.0

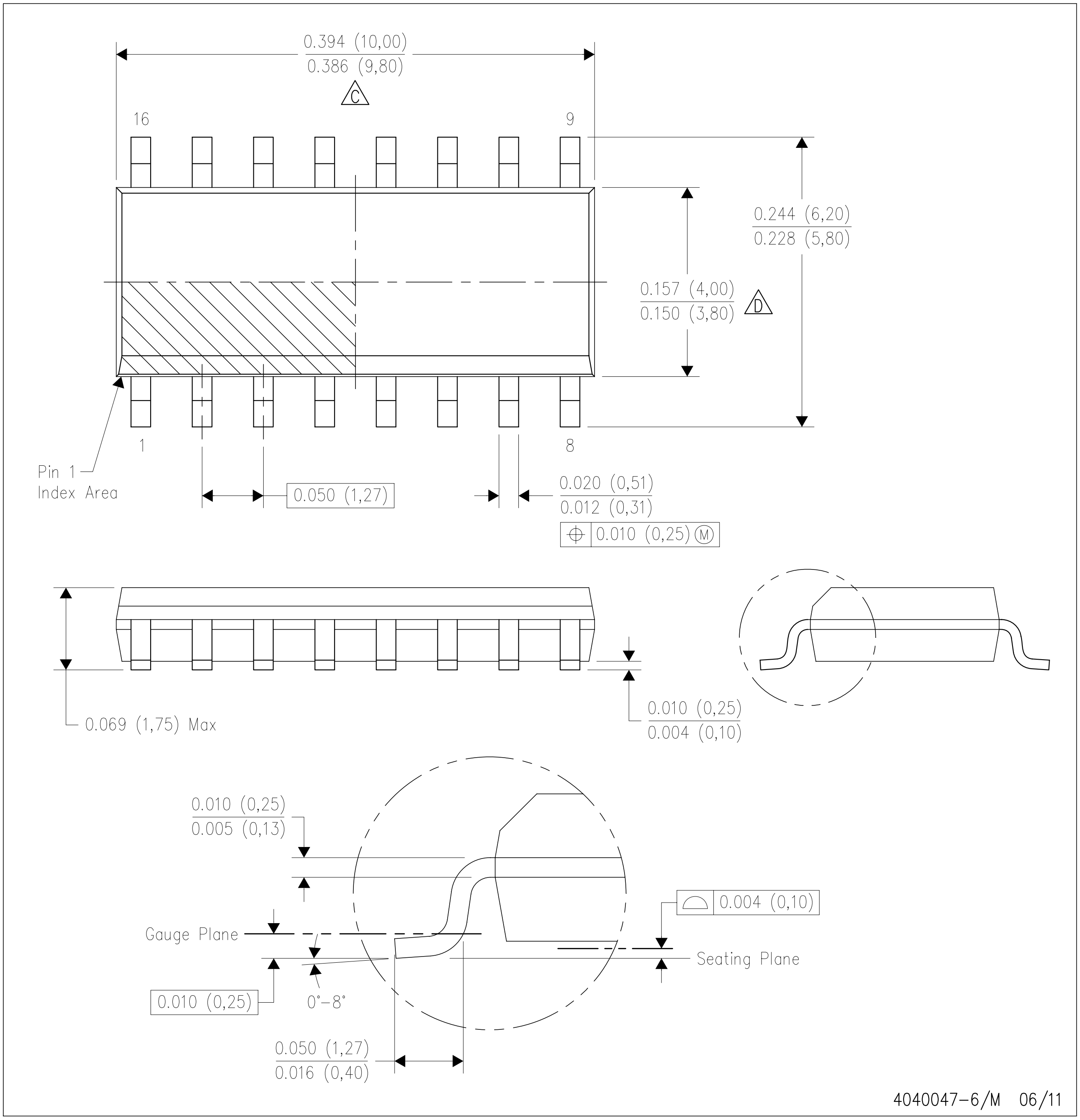
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC4518E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4518E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4518E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4518E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4520E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4520E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4520E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4520E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4520E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4520E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4520E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4520E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



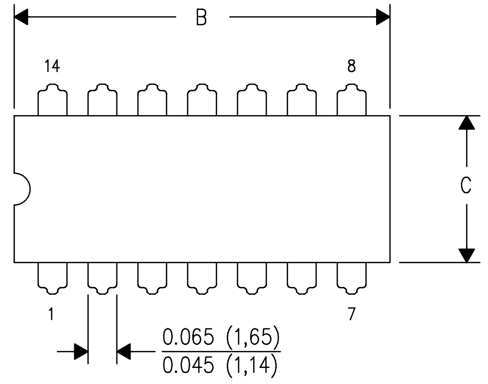
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

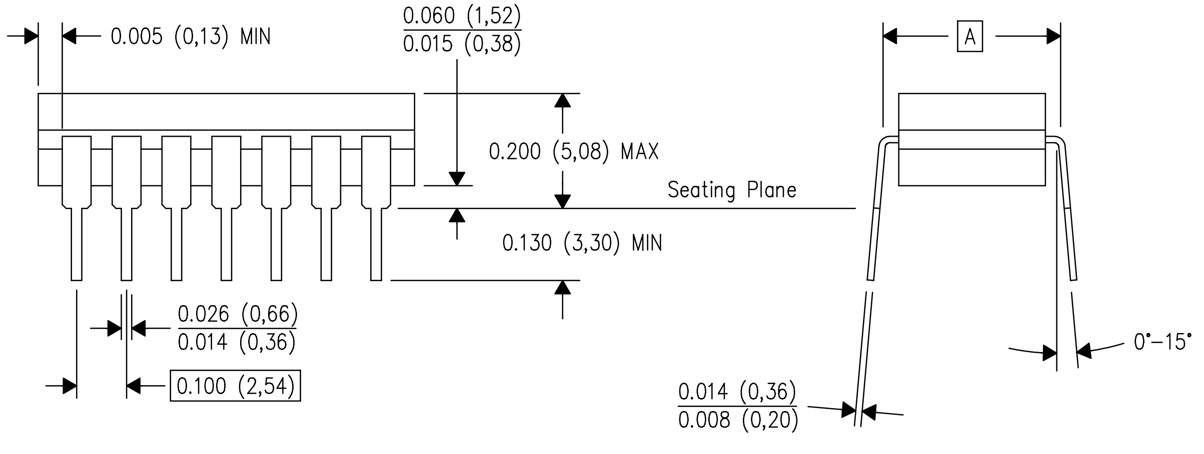
J (R–GDIP–T**)

CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



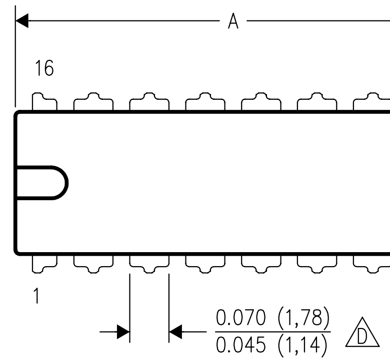


4040083/F 03/03

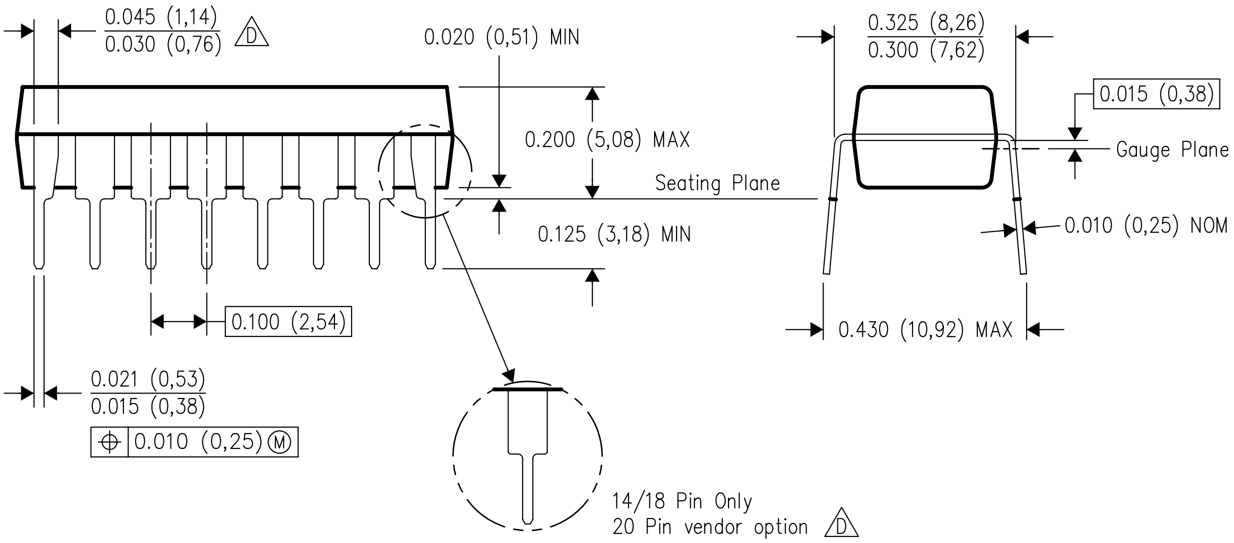
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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