

CSD95410 Synchronous Buck NexFET™ Smart Power Stage

1 Features

- 90-A peak continuous current
- Over 95% system efficiency at 30 A
- High-frequency operation (up to 1.75 MHz)
- Diode emulation function
- Temperature compensated bi-directional current sense
- Analog temperature output
- Fault monitoring
- 3.3-V and 5-V PWM signal compatible
- Tri-state PWM input
- Integrated bootstrap switch
- Optimized dead-time for shoot-through protection
- High-density industry common QFN 5-mm × 6-mm footprint
- Ultra-low-inductance package
- System optimized PCB footprint
- Thermally enhanced topside cooling
- RoHS compliant: lead-free terminal plating
- Halogen free

2 Applications

- Multiphase synchronous buck converters
 - High-frequency applications
 - High-current, low-duty cycle applications
- Point-of-load DC-DC converters
- Memory and graphic cards
- Desktop and server VR12.x / VR13.x / VR14.x V-core synchronous buck converters

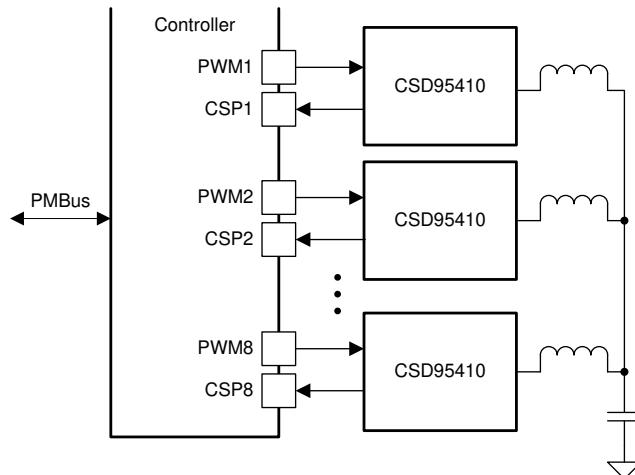
3 Description

The CSD95410 NexFET™ power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and power MOSFETs to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small 5-mm × 6-mm outline package. It also integrates the accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. In addition, the PCB footprint has been optimized to help reduce design time and simplify the completion of the overall system design.

Device Information

DEVICE	MEDIA	QTY	PACKAGE ⁽¹⁾	SHIP
CSD95410	13-Inch Reel	2500	QFN 5.00-mm × 6.00-mm	Tape and Reel
CSD95410T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
September 2020	*	Initial release.

5 Device and Documentation Support

5.1 Device Support

5.1.1 Third-Party Products Disclaimer

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5.2 Documentation Support

5.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.5 Trademarks

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5.6 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

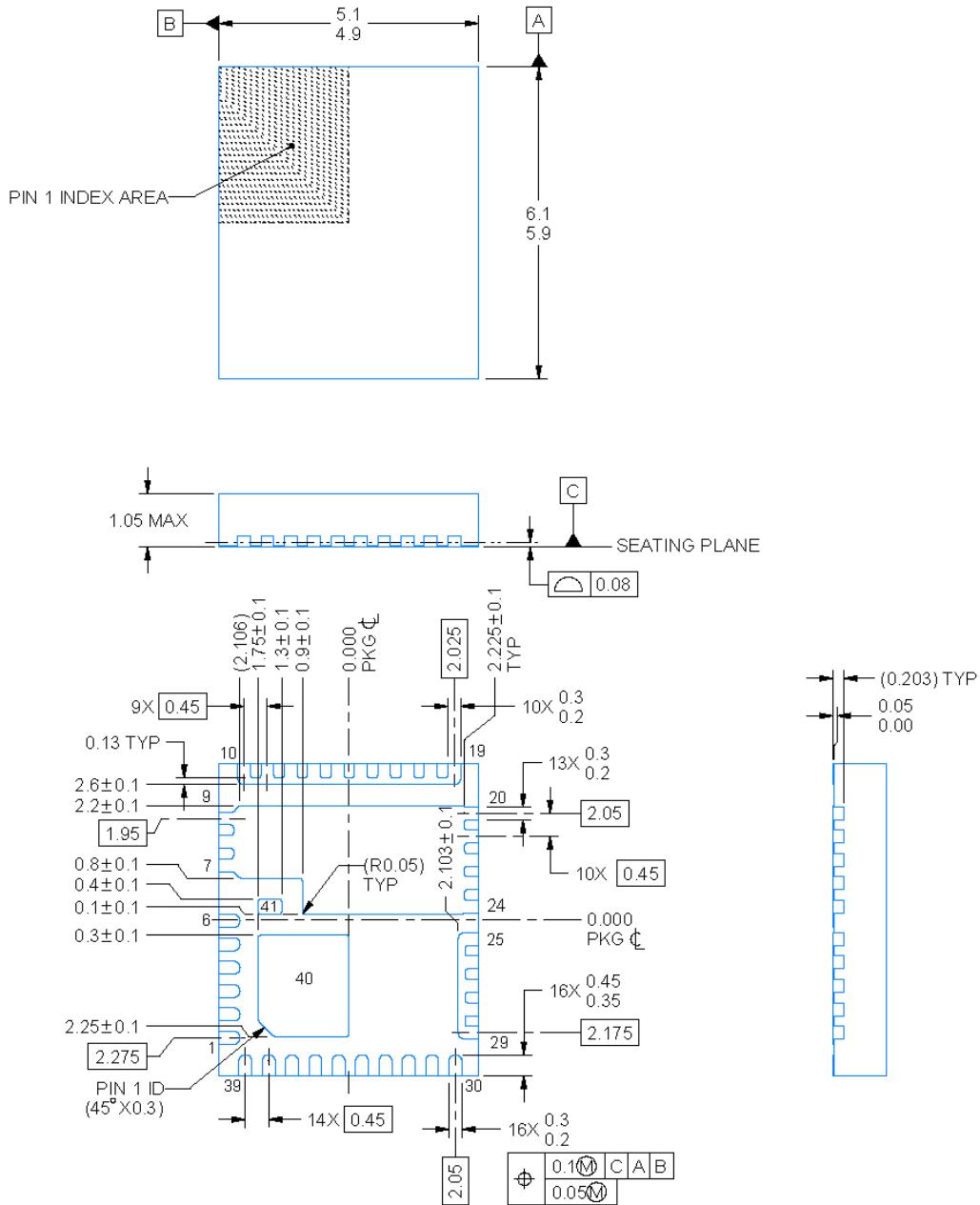
[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

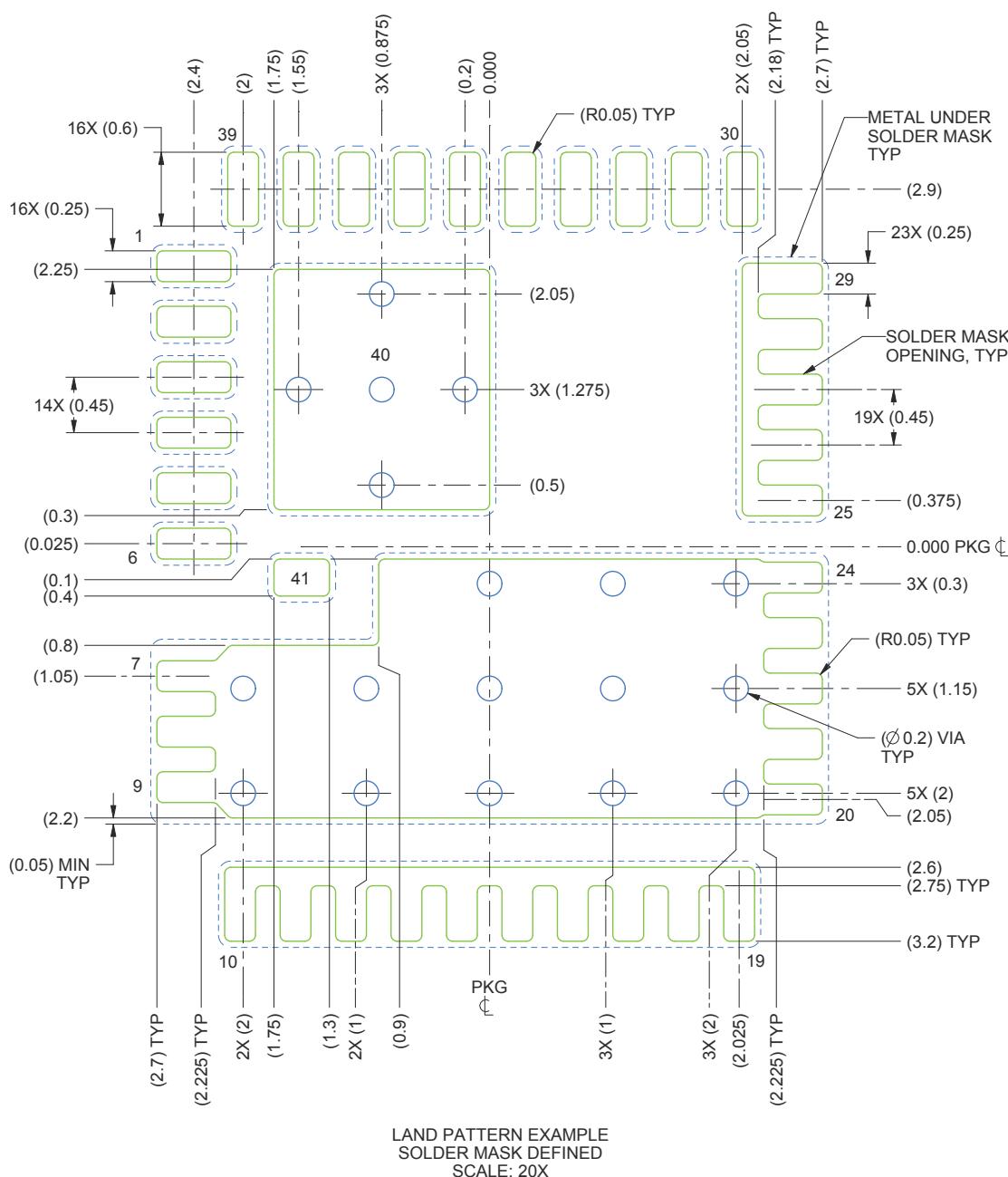
6.1 Mechanical Drawing



4224073/C 10/2018

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

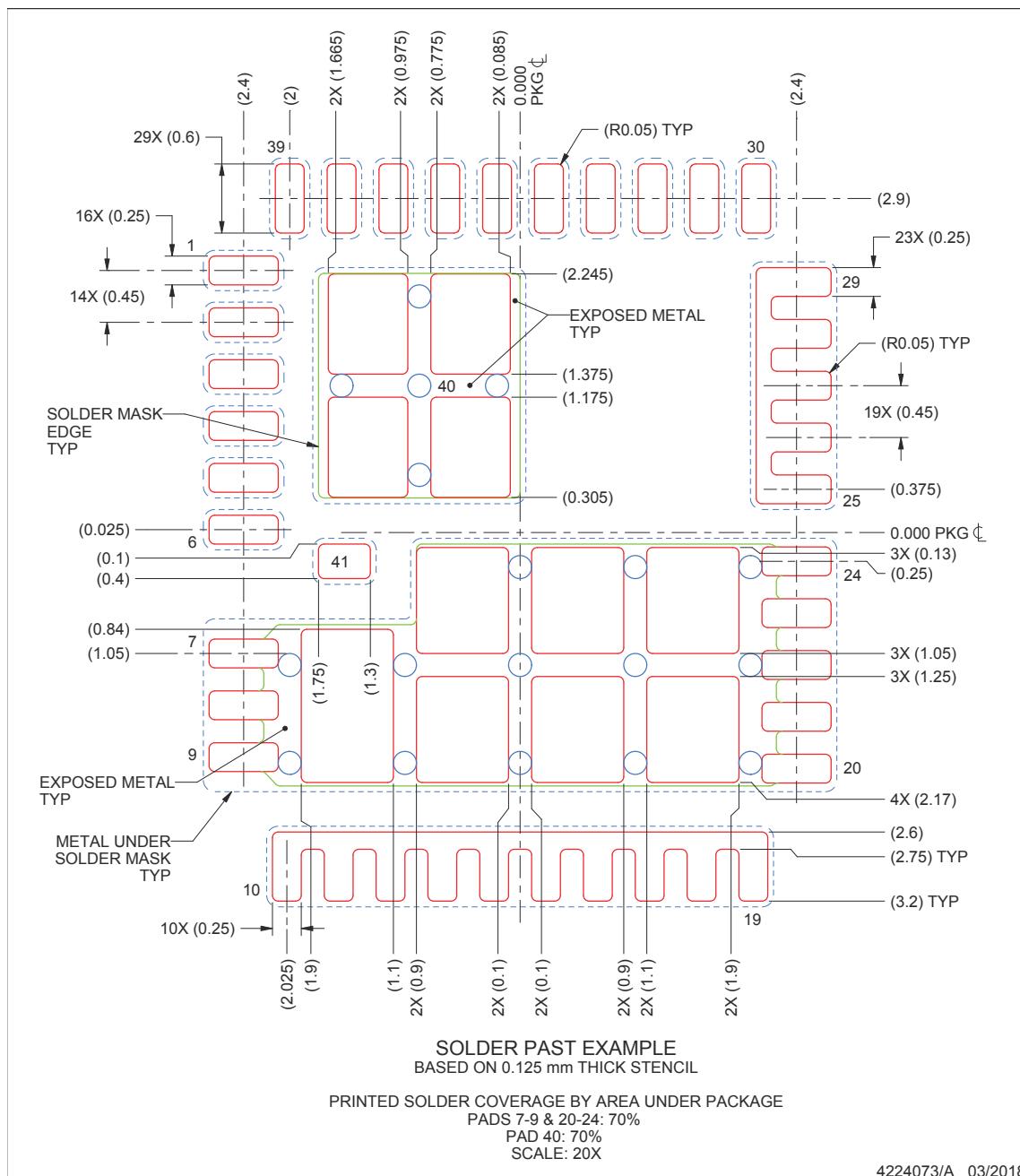
6.2 Recommended PCB Land Pattern



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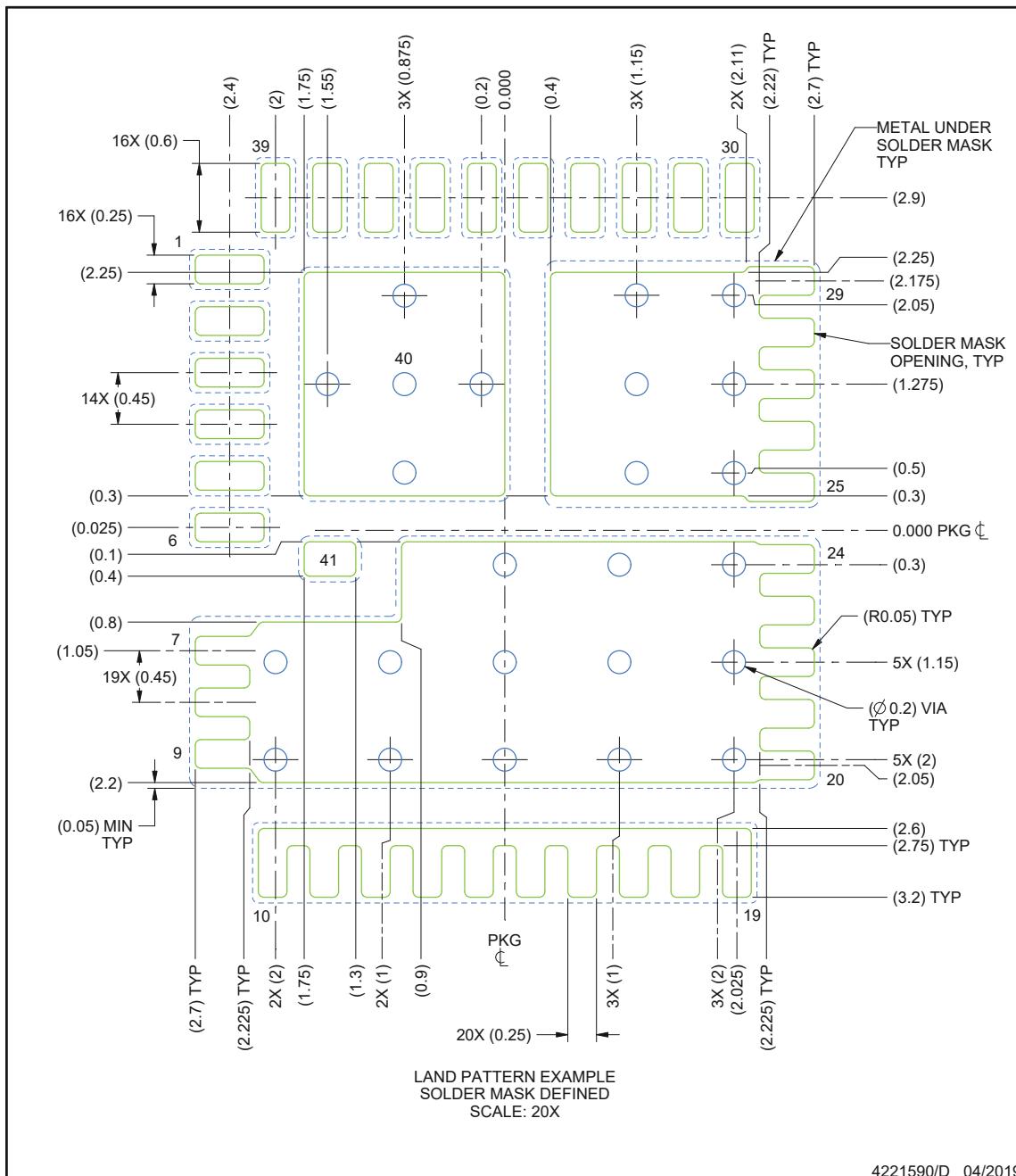
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to thermal pads on the board. For more information, see [QFN/SON PCB Attachment](#) (SLUA271).

6.3 Recommended Stencil Opening



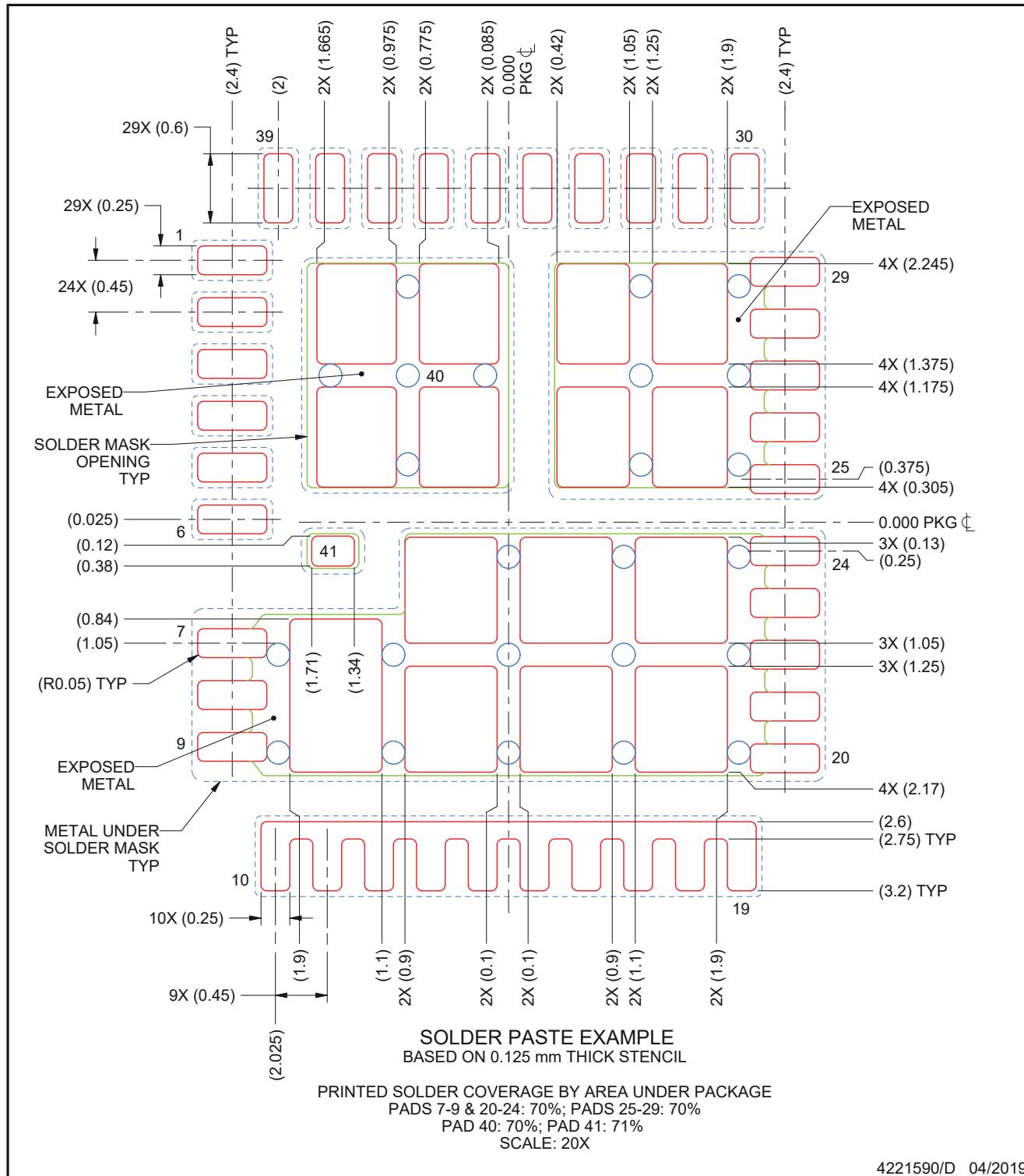
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

6.4 Alternate Industry Standard Compatible PCB Land Pattern



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

6.5 Alternate Industry Standard Compatible Stencil Opening



6.6 Package Option Addendum

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD95410RRB	Active	Production	VQFN-CLIP (RRB) 41	2500 LARGE T&R	ROHS Exempt	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	95410RRB
CSD95410RRB.A	Active	Production	VQFN-CLIP (RRB) 41	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	95410RRB
CSD95410RRBT	Active	Production	VQFN-CLIP (RRB) 41	250 SMALL T&R	ROHS Exempt	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 125	95410RRB
CSD95410RRBT.A	Active	Production	VQFN-CLIP (RRB) 41	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	95410RRB

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

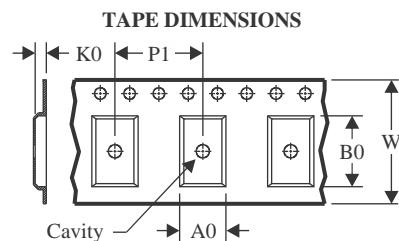
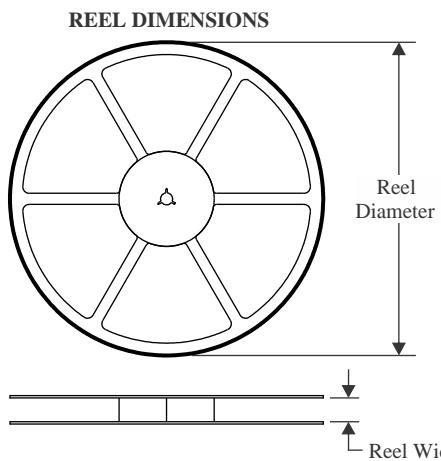
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

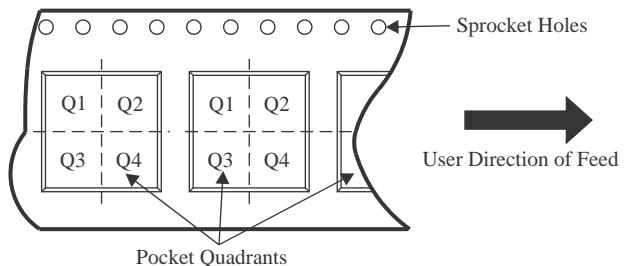
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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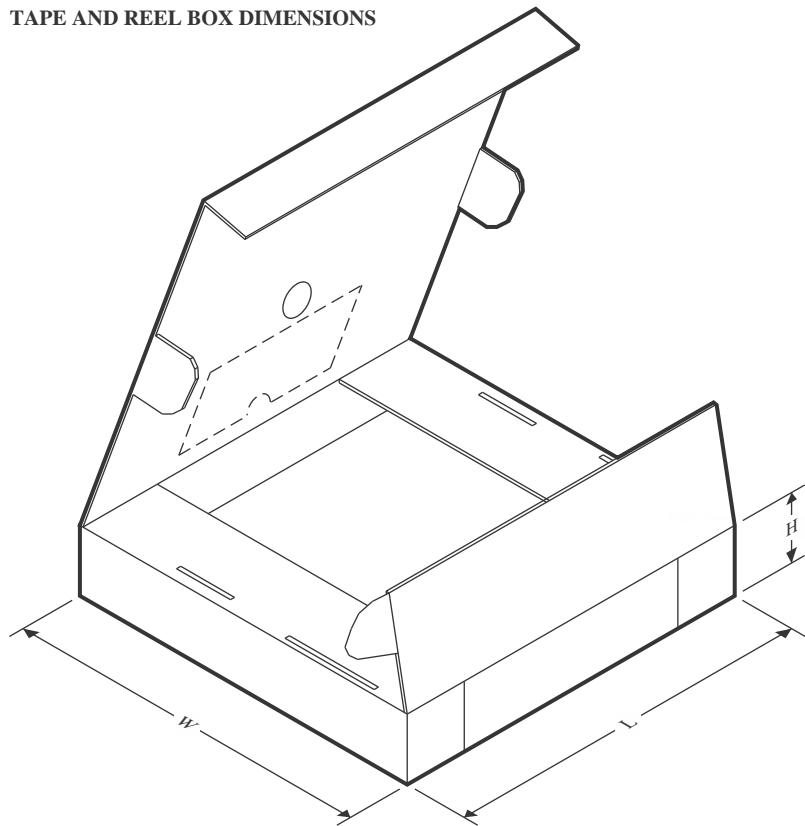
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD95410RRB	VQFN-CLIP	RRB	41	2500	330.0	12.4	5.3	6.3	1.2	8.0	12.0	Q1
CSD95410RRBT	VQFN-CLIP	RRB	41	250	180.0	12.4	5.3	6.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD95410RRB	VQFN-CLIP	RRB	41	2500	367.0	367.0	38.0
CSD95410RRBT	VQFN-CLIP	RRB	41	250	213.0	191.0	35.0

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