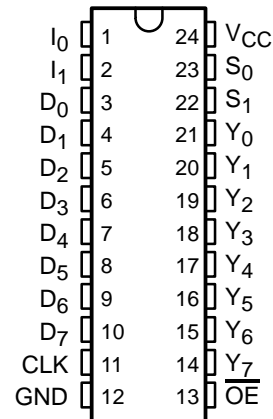


# CY29FCT520T MULTILEVEL PIPELINE REGISTER WITH 3-STATE OUTPUTS

SCCS011C – MAY 1994 – REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29520
- Reduced  $V_{OH}$  (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Single- and Dual-Pipeline Operation Modes
- Multiplexed Data Inputs and Outputs
- CY29FCT520T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- CY29FCT520ATDMB, CY29FCT520BTDMB
  - 32-mA Output Sink Current
  - 12-mA Output Source Current
- 3-State Outputs

D, P, OR SO PACKAGE  
(TOP VIEW)



## description

The CY29FCT520T is a multilevel 8-bit-wide pipeline register. The device consists of four registers, A1, A2, B1, and B2, which are configured by the instruction inputs  $I_0$ ,  $I_1$  as a single four-level pipeline or as two two-level pipelines. The contents of any register can be read at the multiplexed output at any time by using the multiplex-selection controls ( $S_0$  and  $S_1$ ).

The pipeline registers are positive-edge triggered, and data is shifted by the rising edge of the clock input. Instruction  $I = 0$  selects the four-level pipeline mode. Instruction  $I = 1$  selects the two-level B pipeline, while  $I = 2$  selects the two-level A pipeline.  $I = 3$  is the hold instruction; no shifting is performed by the clock in this mode.

In the two-level operation mode, data is shifted from level 1 to level 2 and new data is loaded into level 1.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CY29FCT520T

## MULTILEVEL PIPELINE REGISTER

### WITH 3-STATE OUTPUTS

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PIPELINE INSTRUCTION TABLE

I = 0		I = 1		I = 2		I = 3	
I <sub>1</sub> = 0	I <sub>0</sub> = 0	I <sub>1</sub> = 0	I <sub>0</sub> = 1	I <sub>1</sub> = 1	I <sub>0</sub> = 0	I <sub>1</sub> = 1	I <sub>0</sub> = 1
Single four-level		Dual two-level		Hold			

ORDERING INFORMATION

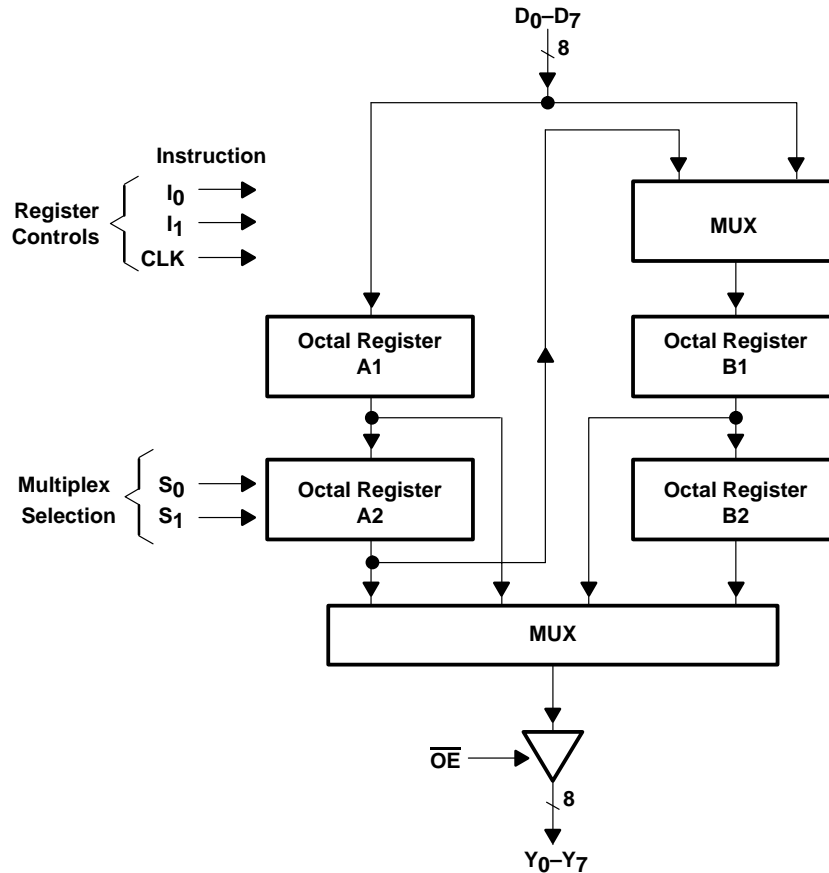
T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – SO	Tube	6.0	CY29FCT520CTSOC	29FCT520C
		Tape and reel	6.0	CY29FCT520CTSOCT	
	SOIC – SO	Tube	7.5	CY29FCT520BTSOC	29FCT520B
		Tape and reel	7.5	CY29FCT520BTSOCT	
	DIP – P	Tube	14.0	CY29FCT520ATPC	CY29FCT520ATPC
	SOIC – SO	Tube	14.0	CY29FCT520ATSOC	29FCT520A
		Tape and reel	14.0	CY29FCT520ATSOCT	
–55°C to 125°C	CDIP – D	Tube	8.0	5962-9220504MLA (CY29FCT520BTDMB)	
		Tube	16.0	5962-9220502MLA (CY29FCT520ATDMB)	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE

INPUTS		OUTPUT
S <sub>1</sub>	S <sub>0</sub>	
1	1	A1
1	0	A2
0	1	B1
0	0	B2

**logic diagram**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): P package	67°C/W
(see Note 2): SO package	46°C/W
Ambient temperature range with power applied, $T_A$	–65°C to 135°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# CY29FCT520T

## MULTILEVEL PIPELINE REGISTER

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

		CY29FCT520ATDMB CY29FCT520BTDMB			CY29FCT520T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			–12			–32	mA
I <sub>OL</sub>	Low-level output current			32			64	mA
T <sub>A</sub>	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY29FCT520ATDMB CY29FCT520BTDMB			CY29FCT520T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = –18 mA			–0.7	–1.2				V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = –18 mA						–0.7	–1.2	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –12 mA		2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = –15 mA				2.4	3.3		
		I <sub>OH</sub> = –32 mA				2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA			0.3	0.55				V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA						0.3	0.55	
V <sub>hys</sub>	All inputs			0.2			0.2		V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>				5				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>							5	
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V				±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V							±1	
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V				±1				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V							±1	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V				±1			±1	μA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V		–60	–120	–225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V					–60	–120	–225	
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V				10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V							10	
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V				–10				μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V							–10	
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V			0.1	0.2				mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V						0.1	0.2	
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open			0.5	2				mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open						0.5	2	

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND



**CY29FCT520T**  
**MULTILEVEL PIPELINE REGISTER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS			CY29FCT520ATDMB CY29FCT520BTDMB			CY29FCT520T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I <sub>CCD</sub> ††	V <sub>CC</sub> = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V				0.06	0.12				mA/ MHz
	V <sub>CC</sub> = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V							0.06	0.12	
I <sub>C</sub> <sup>#</sup>	V <sub>CC</sub> = 5.5 V, Outputs open, f <sub>0</sub> = 10 MHz, OE = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V		0.7	1.4				mA
			V <sub>IN</sub> = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V		2.8	5.6				
			V <sub>IN</sub> = 3.4 V or GND		5.1	14.3				
	V <sub>CC</sub> = 5.25 V, Outputs open, f <sub>0</sub> = 10 MHz, OE = GND	One bit switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V					0.7	1.4	
			V <sub>IN</sub> = 3.4 V or GND					1.2	3.4	
		Eight bits switching at f <sub>1</sub> = 5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.2 V					2.8	5.6	
			V <sub>IN</sub> = 3.4 V or GND					5.1	14.3	
C <sub>i</sub>					5	10		5	10	pF
C <sub>o</sub>					9	12		9	12	pF

† Typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

†† This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4$  V)

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.

# CY29FCT520T

## MULTILEVEL PIPELINE REGISTER

### WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY29FCT520ATDMB		CY29FCT520BTDMB		UNIT
		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, CLK high or low	8		6		ns
$t_{su}$	Setup time, before CLK $\uparrow$	Data	6	2.8		ns
		I	6	4.5		
$t_h$	Hold time, after CLK $\uparrow$	Data	2	2		ns
		I	2	2		

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY29FCT520AT		CY29FCT520BT		CY29FCT520CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, CLK high or low	7		5.5		5.5		ns
$t_{su}$	Setup time, before CLK $\uparrow$	Data	5	2.5		2.5		ns
		I	5	4		4		
$t_h$	Hold time, after CLK $\uparrow$	Data	2	2		2		ns
		I	2	2		2		

switching characteristics over operating free-air temperature range (see Figure 1)

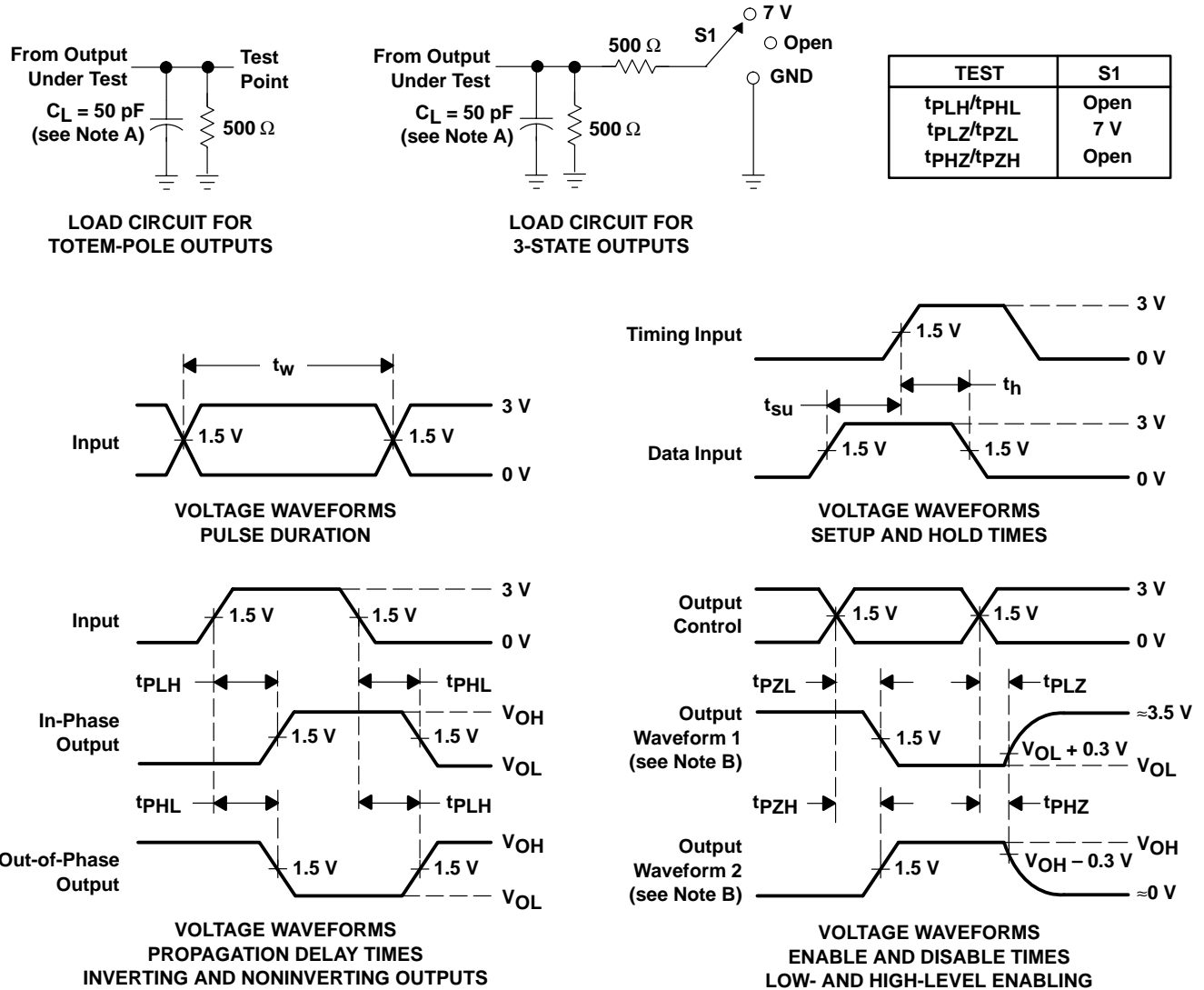
PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY29FCT520ATDMB		CY29FCT520BTDMB		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	CLK	Y	2	16	2	8	ns
$t_{PHL}$			2	16	2	8	
$t_{PLH}$	$S_0$ or $S_1$	Y	2	15	2	8	ns
$t_{PHL}$			2	15	2	8	
$t_{PHZ}$	$\overline{OE}$	Y	1.5	13	1.5	7.5	ns
$t_{PLZ}$			1.5	13	1.5	7.5	
$t_{PZH}$	$\overline{OE}$	Y	1.5	16	1.5	8	ns
$t_{PZL}$			1.5	16	1.5	8	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY29FCT520AT		CY29FCT520BT		CY29FCT520CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	CLK	Y	2	14	2	7.5	2	6	ns
$t_{PHL}$			2	14	2	7.5	2	6	
$t_{PLH}$	$S_0$ or $S_1$	Y	2	13	2	7.5	2	6	ns
$t_{PHL}$			2	13	2	7.5	2	6	
$t_{PHZ}$	$\overline{OE}$	Y	1.5	12	1.5	7	1.5	6	ns
$t_{PLZ}$			1.5	12	1.5	7	1.5	6	
$t_{PZH}$	$\overline{OE}$	Y	1.5	15	1.5	7.5	1.5	6	ns
$t_{PZL}$			1.5	15	1.5	7.5	1.5	6	



## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9220502MLA</a>	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220502ML A
<a href="#">5962-9220504MLA</a>	Active	Production	CDIP (JT)   24	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9220504ML A
<a href="#">CY29FCT520ATSOC</a>	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT520A
CY29FCT520ATSOC.B	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT520A
<a href="#">CY29FCT520BTSOC</a>	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT520B
CY29FCT520BTSOC.B	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT520B

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TUBE



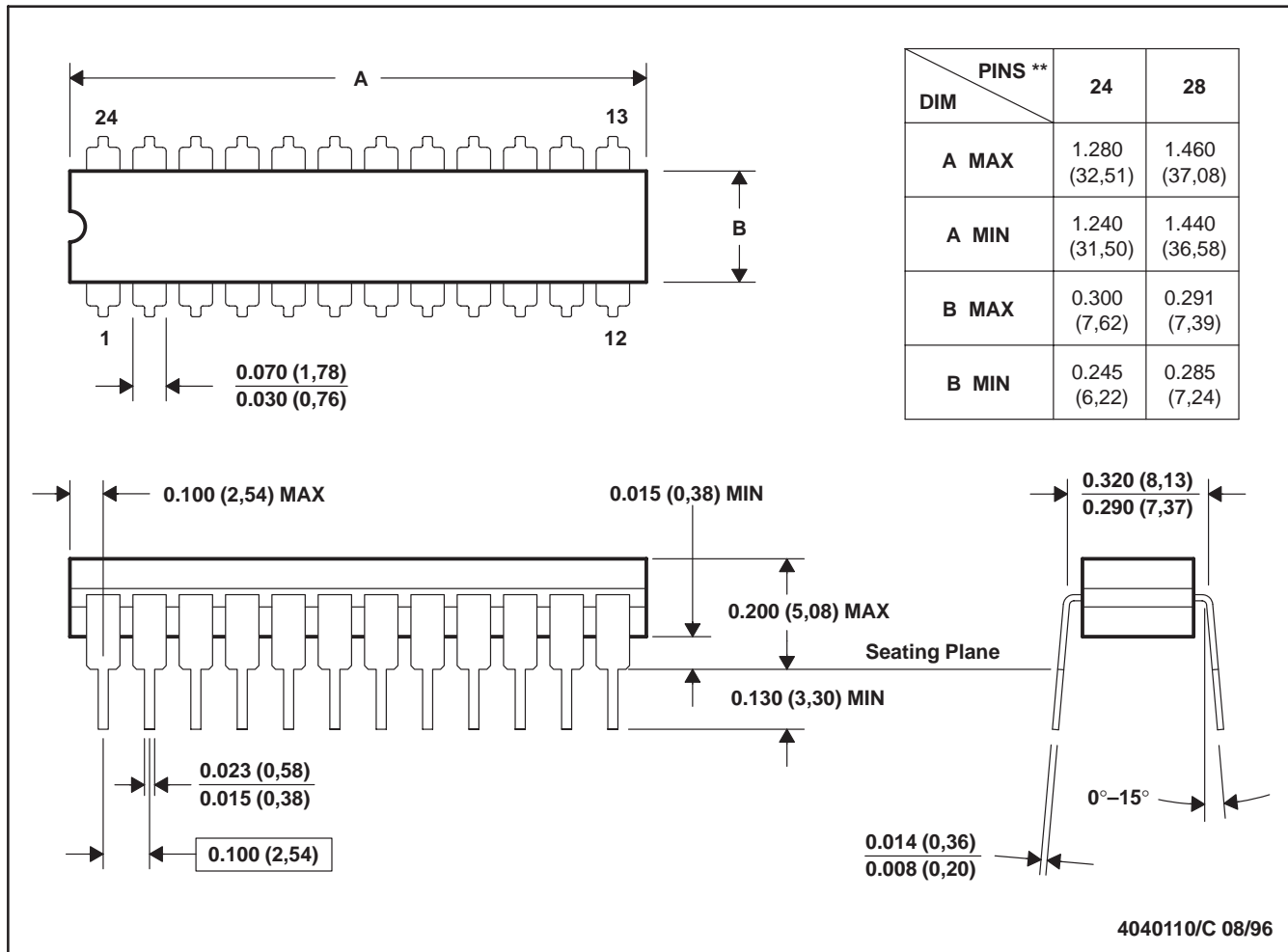
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY29FCT520ATSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY29FCT520ATSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY29FCT520BTSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY29FCT520BTSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

## JT (R-GDIP-T\*\*)

24 LEADS SHOWN

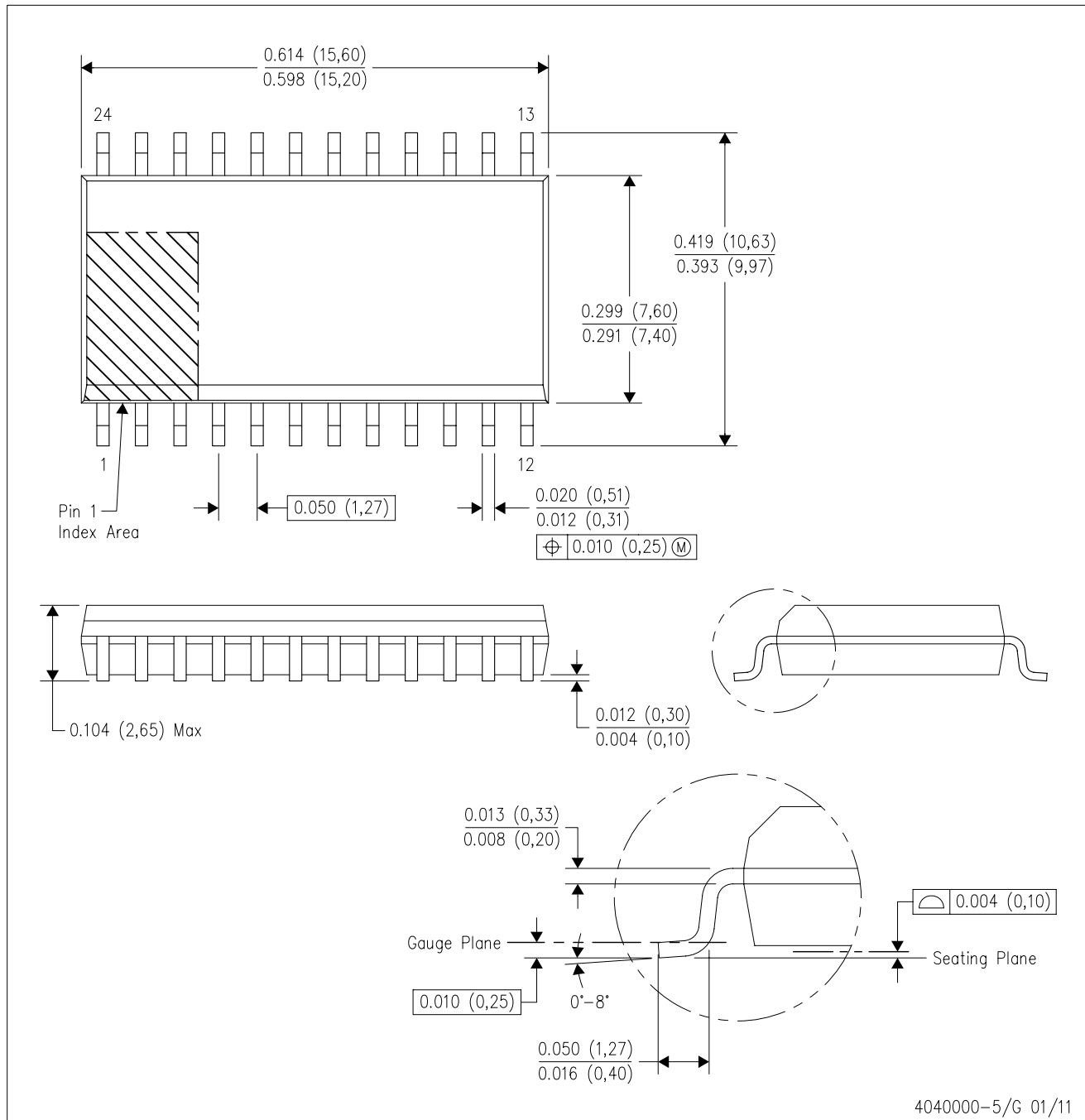
## CERAMIC DUAL-IN-LINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification.
  - E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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