Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

CY74FCT16245T
CY74FCT162245T
CY74FCT162H245T

16-Bit Transceivers

SCCS026B - July 1994 - Revised September 2001

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of –40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16245T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce)<1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162245T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

CY74FCT162H245T Features:

- **Bus hold on data inputs**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

These 16-bit transceivers are designed for use in bidirectional synchronous communication between two buses, where high speed and low power are required. With the exception of the CY74FCT16245T, these devices can be operated either as two independent octals or a single 16-bit transceiver. Direction of data flow is controlled by (DIR), the Output Enable ($\overline{OE}$) transfers data when LOW and isolates the buses when HIGH.

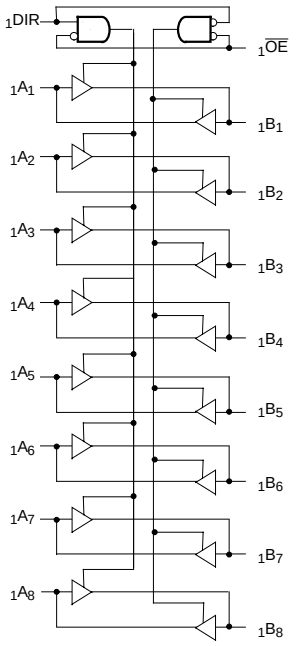
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16245T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

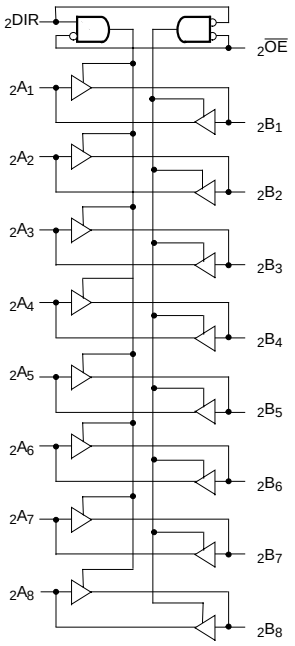
The CY74FCT162245T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162245T is ideal for driving transmission lines.

The CY74FCT162H245T is a 24-mA balanced output part that has bus hold on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Logic Block Diagrams CY74FCT16245T,CY74FCT162245T, CY74FCT162H245T



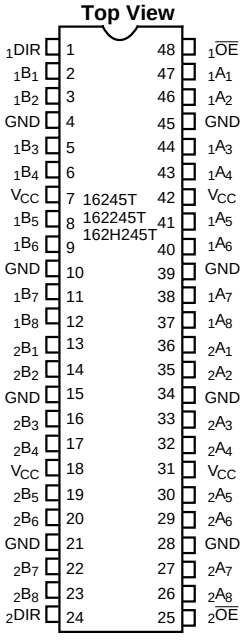
FCT16245–1



FCT16245–2

Pin Configuration

SSOP/TSSOP Top View



FCT16245–3

Pin Description

Name	Description
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
DIR	Direction Control
A	Inputs or Three-State Outputs[1]
B	Inputs or Three-State Outputs[1]

Function Table[2]

Inputs		Outputs
$\overline{OE}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....Com'l -55°C to +125°C

Ambient Temperature with Power Applied.....Com'l -55°C to +125°C

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Notes:
1. On CY74FCT162H245T these pins have bus hold.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

Parameter	Description		Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_H	Input Hysteresis[6]					100		mV
V_{IK}	Input Clamp Diode Voltage		V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_{IH}	Input HIGH Current	Standard	V_{CC}=Max., V_I=V_{CC}				±1	µA
		Bus Hold					±100	
I_{IL}	Input LOW Current	Standard	V_{CC}=Max., V_I=GND				±1	µA
		Bus Hold					±100	µA
I_{BBH} I_{BBL}	Bus Hold Sustain Current on Bus Hold Input[7]		V_{CC}=Min.	V_I=2.0V	–50			µA
				V_I=0.8V	+50			
I_{BHHO} I_{BHLO}	Bus Hold Overdrive Current on Bus Hold Input[7]		V_{CC}=Max., V_I=1.5V				TBD	mA
I_{OZH}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=2.7V				±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)		V_{CC}=Max., V_{OUT}=0.5V				±1	µA
I_{OS}	Short Circuit Current[8]		V_{CC}=Max., V_{OUT}=GND		–80	–140	–200	mA
I_O	Output Drive Current[8]		V_{CC}=Max., V_{OUT}=2.5V		–50		–180	mA
I_{OFF}	Power-Off Disable		V_{CC}=0V, V_{OUT}≤4.5V[9]				±1	µA

Output Drive Characteristics for CY74FCT16245T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162245T, CY74FCT162H245T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[8]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[8]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Notes:

5. Typical values are at V_{CC}=5.0V, T_A=+25˚C ambient.
6. This parameter is specified but not tested.
7. Pins with bus hold are described in Pin Description.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
9. Tested at +25˚C.

Capacitance[6] (T_A = +25˚C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[10]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=DIR=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	60	100	µA/MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=DIR=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=DIR=GND	$V_{IN}=V_{CC}$ or V_{IN}=GND	2.4	4.5[13]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	74FCT16245T 74FCT162245T		74FCT16245AT 74FCT162245AT 74FCT162H245AT		Unit	Fig. No.[15]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output A to B, B to A	1.5	7.0	1.5	4.5	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B	1.5	9.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B	1.5	7.5	1.5	5.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time DIR to A or B	1.5	9.5	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A or B	1.5	7.5	1.5	5.0	ns	1, 7, 8
$t_{SK(O)}$	Output Skew[16]		0.5		0.5	ns	—

Parameter	Description	74FCT16245CT 74FCT162245CT 74FCT162H245CT		Unit	Fig. No.[15]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output A to B, B to A	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B	1.5	4.8	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time DIR to A or B	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A or B	1.5	4.8	ns	1, 7, 8
$t_{SK(O)}$	Output Skew[16]		0.5	ns	—

Note:
14. Minimum limits are specified but not tested on Propagation Delays.
15. See “Parameter Measurement Information” in the General Information section.
16. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT16245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT16245TPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162245

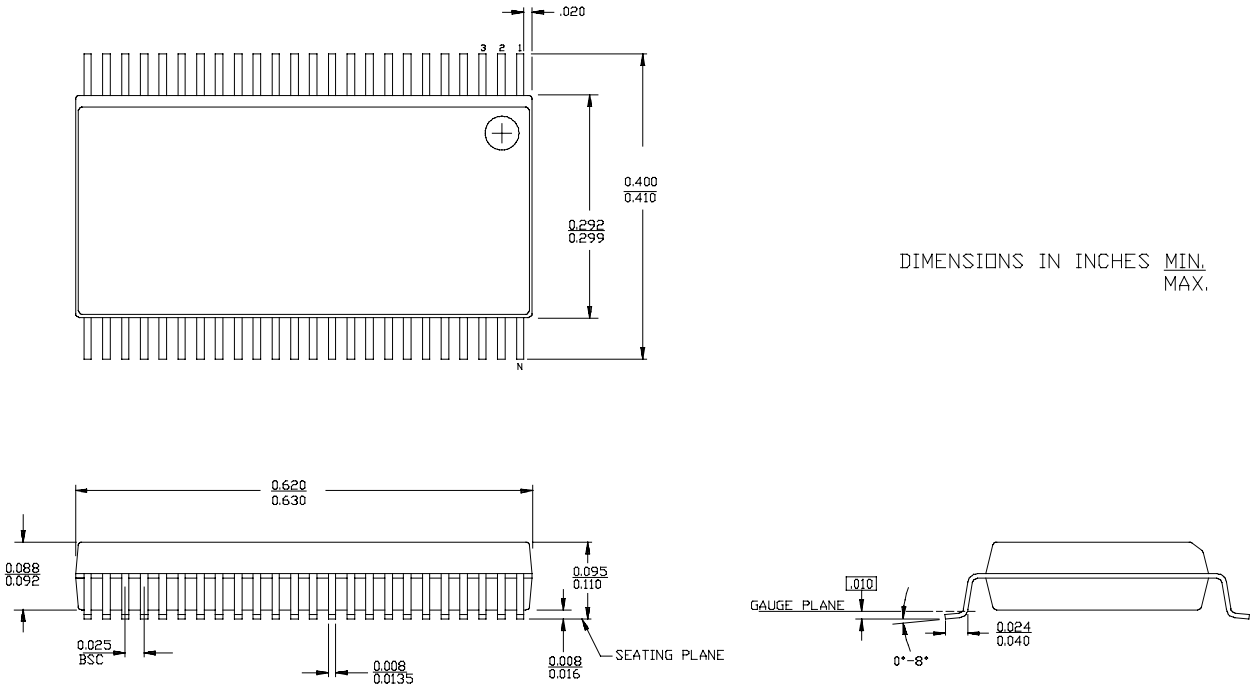
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162245CTPVCT	O48	48-Lead (300-Mil) SSOP	
4.5	74FCT162245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162245ATPVCT	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT162245TPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162H245

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	74FCT162H245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162H245CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162H245CTPVCT	O48	48-Lead (300-Mil) SSOP	
4.5	74FCT162H245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162H245ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162H245ATPVCT	O48	48-Lead (300-Mil) SSOP	

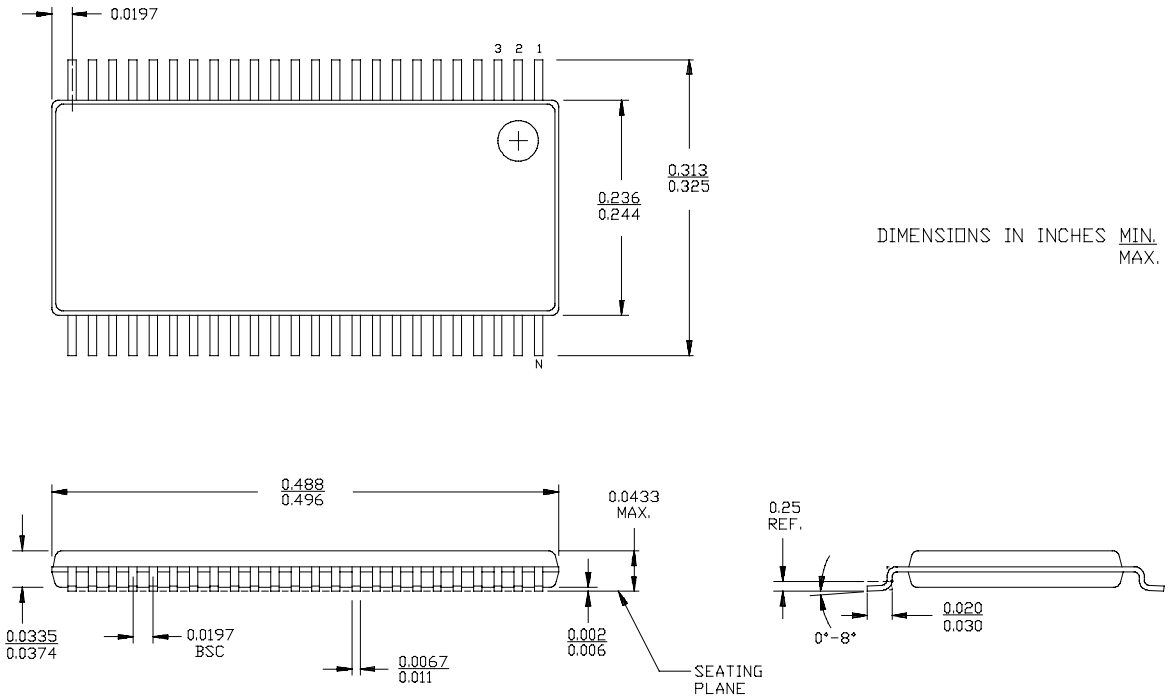
Package Diagrams

48-Lead Shrunk Small Outline Package O48



Package Diagrams

48-Lead Thin Shrunk Small Outline Package Z48



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74FCT162245ATPACT	Obsolete	Production	TSSOP (DGG) | 48	-	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245A
74FCT162245CTPACT	Obsolete	Production	TSSOP (DGG) | 48	-	-	Call TI	Call TI	-40 to 85	FCT162245C
CY74FCT162245ATPVC	Obsolete	Production	SSOP (DL) | 48	-	-	Call TI	Call TI	-40 to 85	FCT162245A
CY74FCT162245CTPVC	Obsolete	Production	SSOP (DL) | 48	-	-	Call TI	Call TI	-40 to 85	FCT162245C
CY74FCT162245TPACT	Obsolete	Production	TSSOP (DGG) | 48	-	-	Call TI	Call TI	-40 to 85	FCT162245
CY74FCT162245TPVC	Obsolete	Production	SSOP (DL) | 48	-	-	Call TI	Call TI	-40 to 85	FCT162245
CY74FCT162245TPVCT	Obsolete	Production	SSOP (DL) | 48	-	-	Call TI	Call TI	-40 to 85	FCT162245
CY74FCT16245ATPACT	Obsolete	Production	TSSOP (DGG) | 48	-	-	Call TI	Call TI	-40 to 85	FCT16245A
CY74FCT16245ATPVCT	Obsolete	Production	SSOP (DL) | 48	-	-	Call TI	Call TI	-40 to 85	FCT16245A
CY74FCT16245CTPVCT	Obsolete	Production	SSOP (DL) | 48	-	-	Call TI	Call TI	-40 to 85	FCT16245C
CY74FCT16245TPACT	Obsolete	Production	TSSOP (DGG) | 48	-	-	Call TI	Call TI	-40 to 85	FCT16245
CY74FCT16245TPVC	Obsolete	Production	SSOP (DL) | 48	-	-	Call TI	Call TI	-40 to 85	FCT16245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

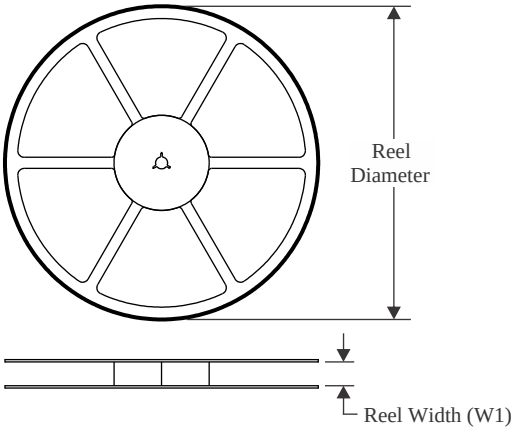
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

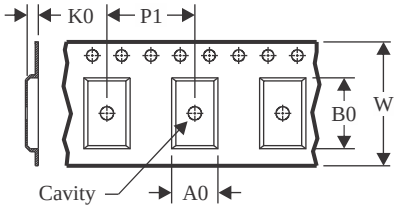
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

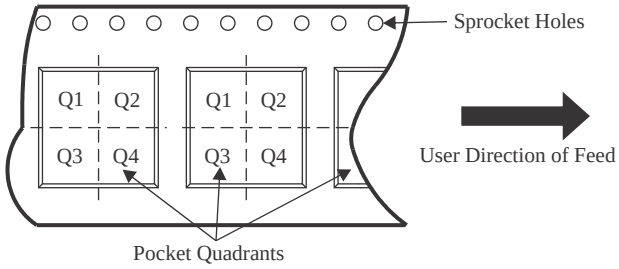


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

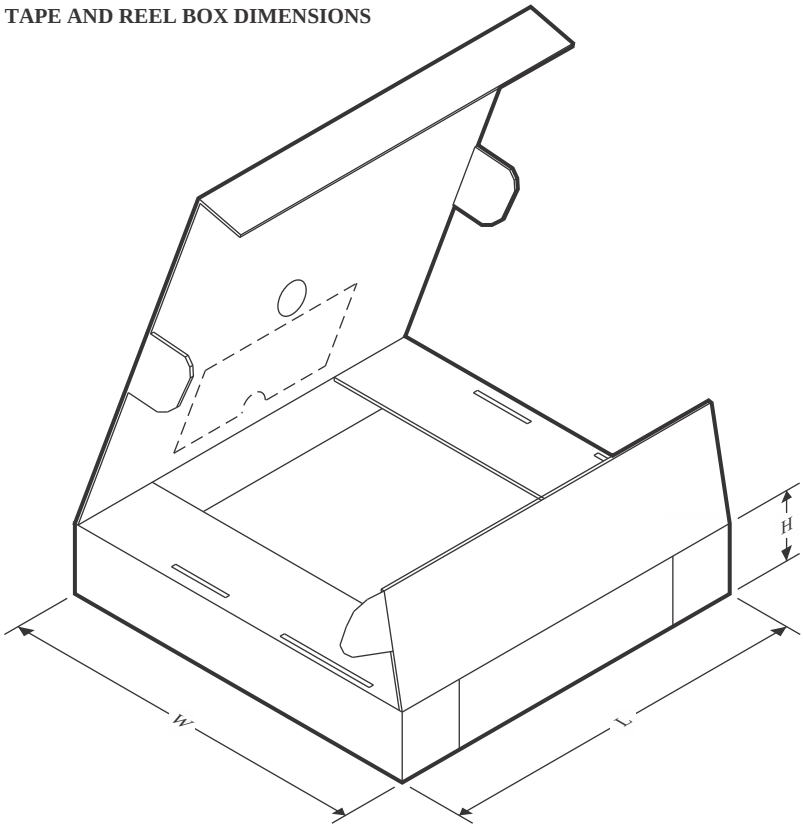
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162245ATPACT	TSSOP	DGG	48	0	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

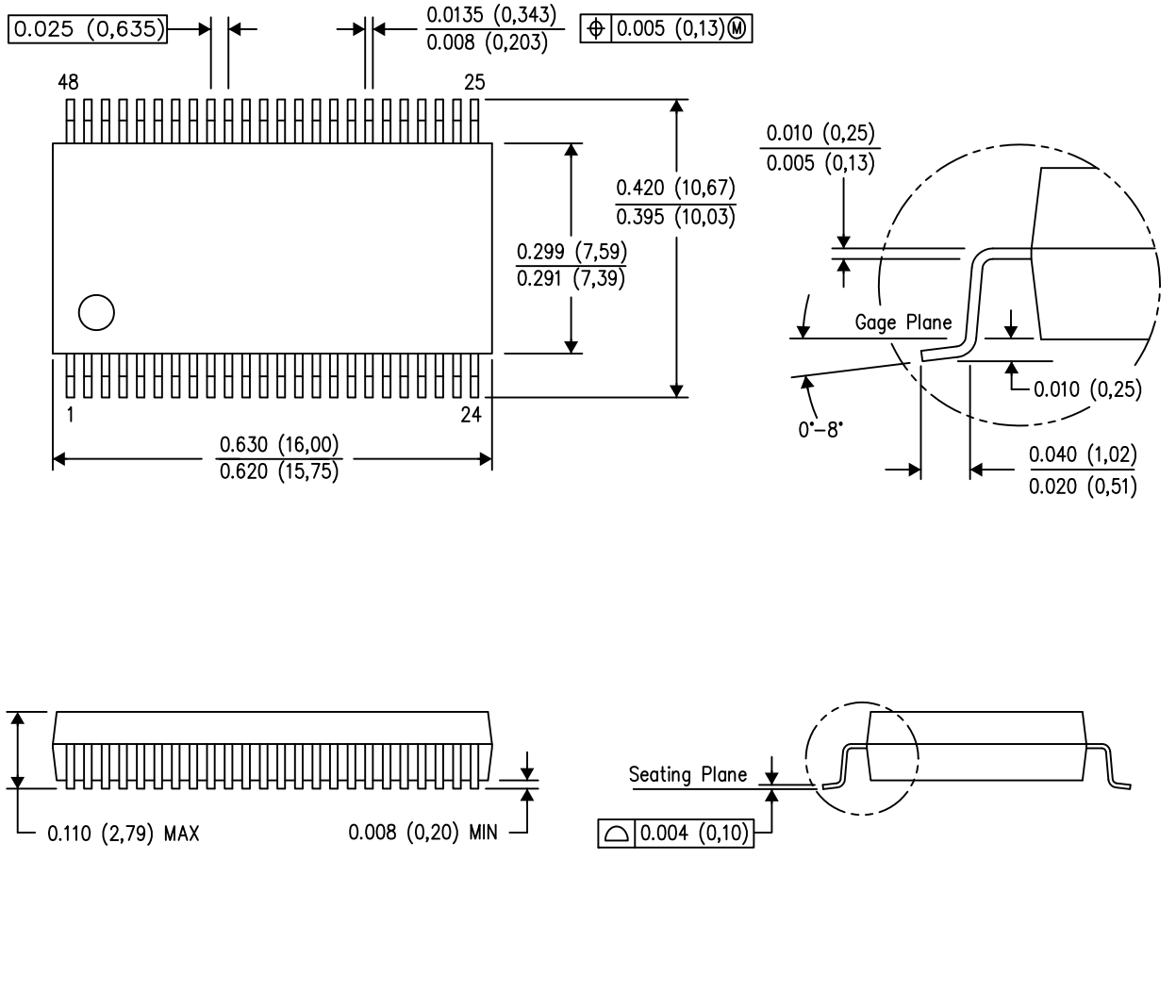
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

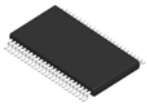
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162245ATPACT	TSSOP	DGG	48	0	356.0	356.0	45.0

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

PowerPAD is a trademark of Texas Instruments.

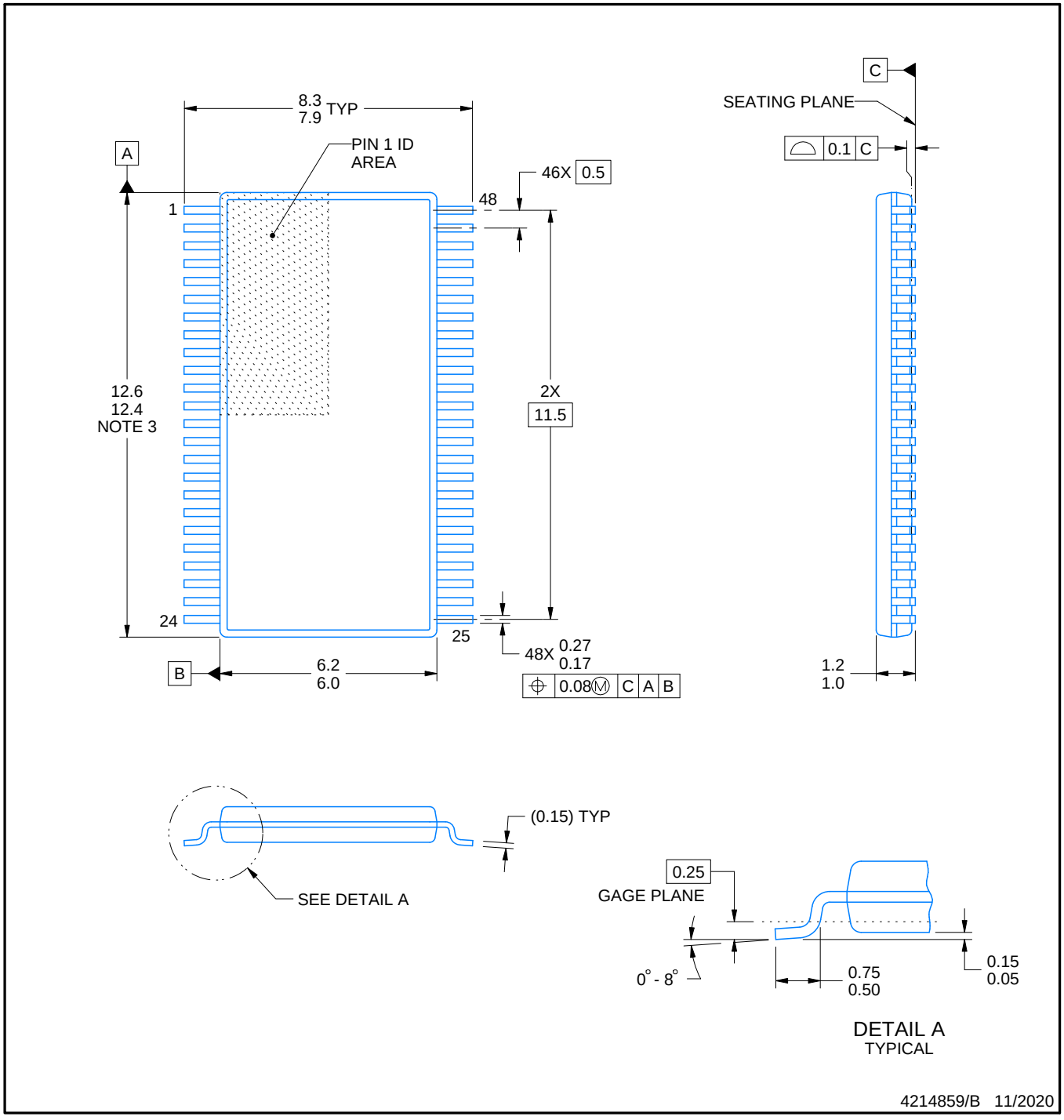


PACKAGE OUTLINE

DGG0048A

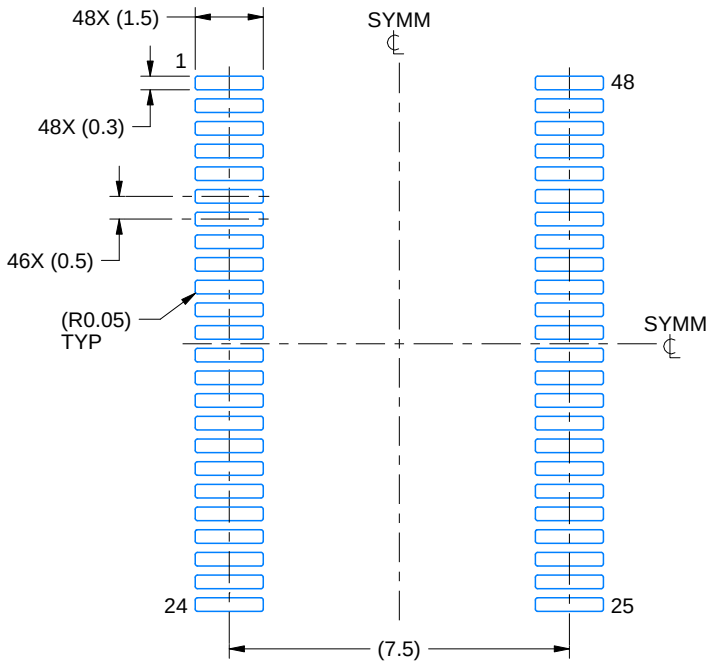
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

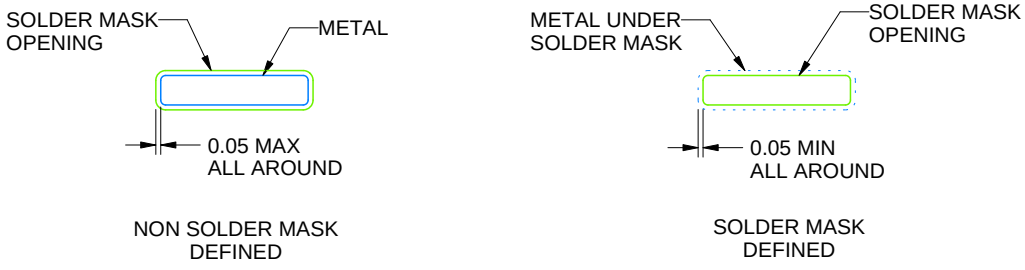


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

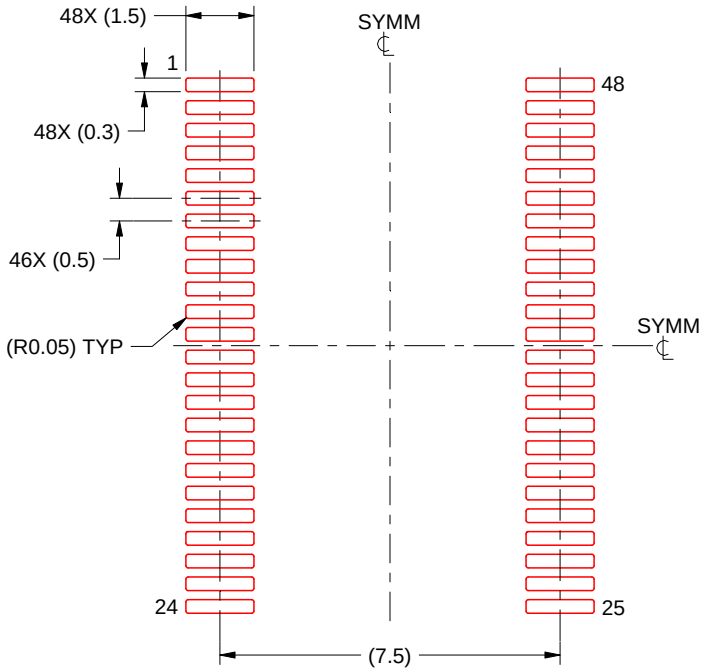


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

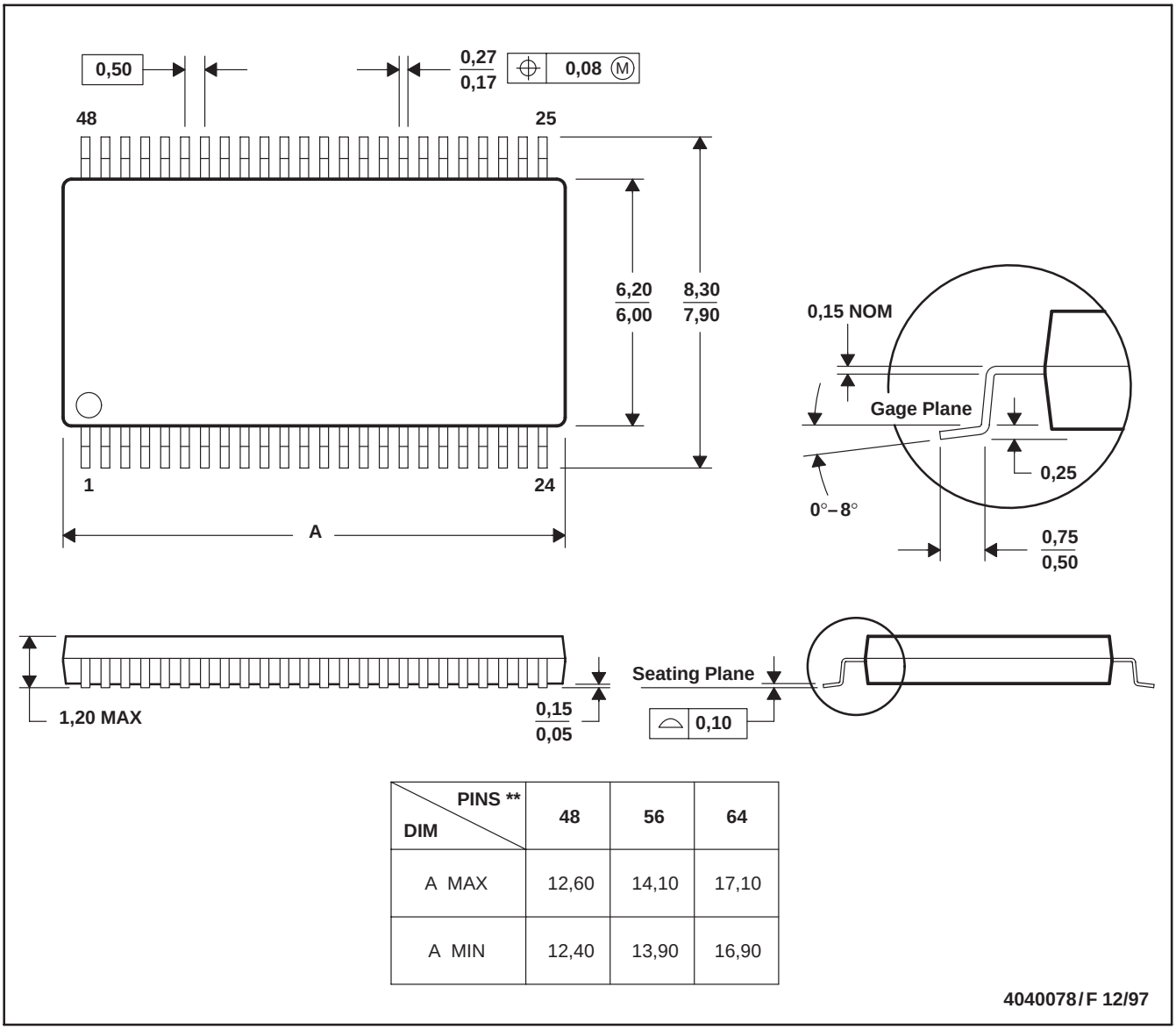
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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