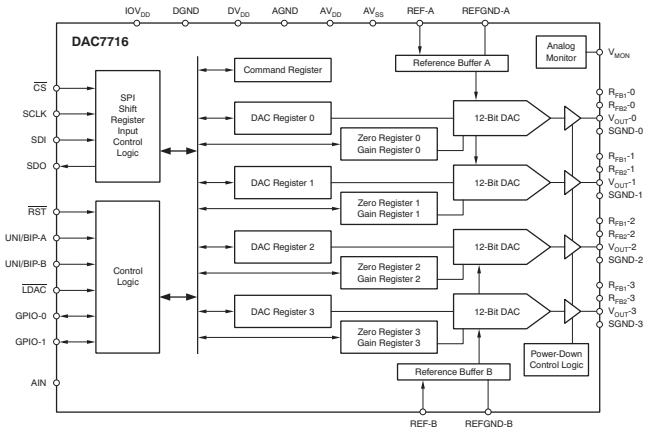
Quad, 12-Bit, High-Accuracy, ±16V Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Bipolar Output: Up to ±16V**
- **Unipolar Output: 0V to +20V**
- **12-Bit Monotonic**
- **Relative Accuracy: 1 LSB Max**
- **Low Zero and Gain Errors**
  - **Before User Calibration: 0.5 LSB**
  - **After User Calibration: 0.0078 LSB Zero Error, 0.0625 LSB Gain Error**
- **Low Noise: 60nV/√Hz**
- **Settling Time: 6μs**
- **Configurable Gain: x2/x4**
- **Analog Output Monitor**
- **Power-Down Mode**
- **SPI™: Up to 50MHz, 1.8V/3V/5V Logic**
- **Daisy-Chain Mode**
- **Operating Temperature: –40°C to +105°C**
- **Packages: QFN-40 (6x6mm), TQFP-48 (7x7mm)**

APPLICATIONS

- **Automatic Test Equipment**
- **Instrumentation**
- **Industrial Process Control**
- **Communications**



DESCRIPTION

The DAC7716 is a high-accuracy, quad-channel, 12-bit digital-to-analog converter (DAC) that operates from supply voltages of ±5V to ±18V in bipolar output mode, and from ±5V to +24V/–12V in unipolar mode. With a 5V reference, the DAC7716 can be configured to output ±10V, ±5V, 0V to 20V, or 0V to 10V. The DAC7716 provides 12-bit monotonicity, excellent integral nonlinearity (INL) error of ±1 LSB, low glitch, and low noise over the operating temperature range of –40°C to +105°C. This device is trimmed in production for very low zero and gain errors. In addition, the DAC7716 implements a user-programmable system-level calibration function to achieve ±0.0078 LSB zero error and ±0.0625 LSB gain error.

The DAC7716 has integrated reference buffers and output buffers. It features a standard high-speed 1.8V, 3V, or 5V serial peripheral interface (SPI) that operates at clock rates of up to 50MHz to communicate with a DSP or microprocessor. The four DAC channels and the auxiliary registers are addressed with four address bits. The device features double-buffered interface logic for simultaneous updates of all DACs. An asynchronous load input ($\overline{LDAC}$) transfers data from the input data register to the DAC latch, and the contents of the DAC latch set the output voltage. The asynchronous $\overline{RST}$ input sets the output of all four DACs to 0V. The V_{MON} pin is an analog monitor output that multiplexes the individual DAC outputs or the AIN pin.

The DAC7716 is pin-compatible with the DAC8734 (16-bit) and the DAC8234 (14-bit).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL LINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC7716	±1	±1	QFN-40	RHA	–40°C to +105°C	DAC7716
	±1	±1	TQFP-48	PFB	–40°C to +105°C	DAC7716

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			DAC7716	UNIT
AV_{DD} to AV_{SS}(2)			–0.3 to 38	V
AV_{DD} to AGND(2)			–0.3 to 25	V
AV_{SS} to AGND, DGND(2)			–19 to 0.3	V
DV_{DD} to DGND			–0.3 to 6	V
IOV_{DD} to DGND			–0.3 to DV_{DD} + 0.3	V
Digital input voltage to DGND			–0.3 to IOV_{DD} + 0.3	V
SDO to DGND			–0.3 to IOV_{DD} + 0.3	V
SGND-x, REFGND-x, AGND to DGND			–0.3 to +0.3	V
V_{OUT}-x, R_{FB1}-x, R_{FB2}-x, V_{MON}, AIN to AV_{SS}			–0.3 to AV_{DD} + 0.3	V
REF-x to REFGND-x, AGND			–0.3 to min(AV_{DD}/2, –AV_{SS}/2)	V
GPIO-x to DGND			–0.3 to 6	V
GPIO-x input current			5	mA
Operating temperature range			–40 to +105	°C
Storage temperature range			–65 to +150	°C
Maximum junction temperature (T_J max)			+150	°C
ESD ratings	Human body model (HBM)		4	kV
	Charged device model (CDM)		1	kV
Thermal impedance	Junction-to-ambient, θ_{JA}	TQFP	57	°C/W
		QFN	32	°C/W
	Junction-to-case, θ_{JC}	TQFP	35	°C/W
		QFN	20	°C/W
Power dissipation(3)			(T_J max – T_A) / θ_{JA}	W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
(2) AV_{SS} must be < –3.5V if AV_{DD} ≥ 1V.
(3) T_A is the ambient temperature.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +11V to +18V, AV_{SS} = –11V to –18V, V_{REF} = REF-A = REF-B = +5V, DV_{DD} = +5V, IOV_{DD} = +1.8V to DV_{DD}, AGND = DGND = REFGND-A = REFGND-B = SGND-x = 0V, and DAC gain = 4, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7716			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE					
Bipolar Output					
Resolution		12			Bits
Linearity error, INL				±1	LSB
Differential linearity error, DNL				±1	LSB
Bipolar zero error(1)	T_A = +25°C, before user calibration			±0.5	LSB
	T_A = +25°C, after user calibration(2)		±0.0078		LSB
Bipolar zero error TC(2)			±0.5		ppm FSR/°C
Gain error(1)	T_A = +25°C, before user calibration			±0.5	LSB
	T_A = +25°C, after user calibration(2)		±0.0625		LSB
Gain error TC(2)			±0.5		ppm FSR/°C
DC crosstalk(2)(3)	Output unloaded			±0.1	LSB
Unipolar Output					
Resolution		12			Bits
Linearity error, INL	AV_{DD} = +21V, AV_{SS} = –11V			±1	LSB
Differential linearity error, DNL	AV_{DD} = +21V, AV_{SS} = –11V			±1	LSB
Zero error	AV_{DD} = +21V, AV_{SS} = –11V, T_A = +25°C, before user calibration			±0.5	LSB
	AV_{DD} = +21V, AV_{SS} = –11V, T_A = +25°C, after user calibration(2)		±0.0078		LSB
Zero error TC(2)	AV_{DD} = +21V, AV_{SS} = –11V		±0.2		ppm FSR/°C
Gain error	AV_{DD} = +21V, AV_{SS} = –11V, T_A = +25°C, before user calibration			±0.5	LSB
	AV_{DD} = +21V, AV_{SS} = –11V, T_A = +25°C, after user calibration(2)		±0.0625		LSB
Gain error TC(2)	AV_{DD} = +21V, AV_{SS} = –11V		±0.5		ppm FSR/°C
DC crosstalk(2)(3)	AV_{DD} = +21V, AV_{SS} = –11V, output unloaded			±0.1	LSB
ANALOG OUTPUT (V_{OUT}-0 to V_{OUT}-3)					
Bipolar voltage output(4)	AV_{DD} = +16.5V, AV_{SS} = –16.5V, V_{REF} = +7.5V, gain = 4	–15		+15	V
	V_{REF} = +5V, gain = 4	–10		+10	V
Unipolar voltage output(4)	AV_{DD} = +21V, AV_{SS} = –11V, V_{REF} = +5V, gain = 4	0		+20	V
Output voltage drift vs time	Operating for 500 hours at +25°C		2		ppm of FSR
	Operating for 1000 hours at +25°C		3		ppm of FSR
Output impedance(2)	±3mA load current		0.005		Ω
Short-circuit current(2)(5)			10		mA
Load current(4)	Output changes no more than ±1 LSB		±3		mA
Capacitive load stability(2)				700	pF
Power-supply rejection(2)(4)	AV_{DD} = +5V to +18V, AV_{SS} = –5V to –18V, DV_{DD} = 5V ±10%, V_{REF} = 2V		±0.1		LSB

(1) See the *User Calibration for Zero-Code Error and Gain Error* section for details.
(2) Specified by design and characterization.
(3) *DC crosstalk* is the dc change in the output of one channel as a result of a full-scale code change and subsequent output change on another channel. The DAC outputs are buffered by op amps that share common AV_{DD} and AV_{SS} power supplies. Multiple V_{DD} and V_{SS} terminals are provided to minimize dc crosstalk.
(4) The analog output must not be greater than (AV_{DD} – 1.0V) and must not be less than (AV_{SS} + 1.0V).
(5) When the output current is greater than the specification, the current is clamped at the specified maximum value.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +11V to +18V, AV_{SS} = –11V to –18V, V_{REF} = REF-A = REF-B = +5V, DV_{DD} = +5V, IOV_{DD} = +1.8V to DV_{DD}, AGND = DGND = REFGND-A = REFGND-B = SGND-x = 0V, and DAC gain = 4, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7716			UNIT
		MIN	TYP	MAX	
AC PERFORMANCE(6)					
Settling time	To 0.1% of FS, C_L = 200pF, R_L= 10kΩ, output changes from –10V to +10V or +10V to –10V		6		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, output changes from –10V to +10V or +10V to –10V		7		µs
	To 1 LSB, C_L = 200pF, R_L = 10kΩ, code changes 512 LSBs		3		µs
Slew rate(7)	C_L = 200pF, R_L = 10kΩ		5		V/µs
Recovery time from power-down mode	Delay from clearing bit PD-x to when DAC returns to normal operation		50		µs
Digital-to-analog glitch(8)	1 LSB code change around midscale		8		nV-s
Glitch impulse peak amplitude	1 LSB code change around midscale		15		mV
Channel-to-channel isolation(9)			–80		dB
DAC-to-DAC crosstalk(10)			2		nV-s
Digital crosstalk(11)			2		nV-s
Digital feedthrough(12)			2		nV-s
Output noise	0.1Hz to 10Hz, ±10V output range, gain = 4, midscale code		1		μV_{RMS}
	0.1Hz to 100kHz, ±10V output range, gain = 4, midscale code		40		μV_{RMS}
1/f corner frequency			500		Hz
Output noise spectral density	T_A = +25°C, at 10kHz, ±10V output range, gain = 4, midscale code		60		$nV/\sqrt{Hz}$
	T_A = +25°C, at 10kHz, 0V to +10V output range, gain = 2, midscale code		45		$nV/\sqrt{Hz}$
MONITOR PIN (V_{MON})(6)					
Output impedance			2200		Ω
High-impedance leakage current				100	nA
Continuous current limit				0.5	mA
REFERENCE INPUT					
Reference input voltage range		1		8	V
Reference input dc impedance		10	100		MΩ
Reference input capacitance(6)			20		pF

(6) Specified by design and characterization.
(7) Slew rate is measured from 10% to 90% of the transition when the output changes from negative full-scale to positive full-scale.
(8) *Digital-to-analog glitch* is defined as the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 000h and FFFh in twos complement format.
(9) *Channel-to-channel isolation* refers to the ratio of the signal amplitude at the output of one DAC channel to the amplitude of the sinusoidal signal on the reference input of another DAC channel. It is expressed in dB and measured at midscale.
(10) *DAC-to-DAC crosstalk* is the glitch impulse that appears at the output of one DAC as a result of both the full-scale digital code and subsequent analog output change at another DAC. It is measured with $\overline{LDAC}$ tied low and expressed in nV-s.
(11) *Digital crosstalk* is the glitch impulse transferred to the output of one converter as a result of a full-scale code change in the DAC input register of another converter. It is measured when the DAC output is not updated, and is expressed in nV-s.
(12) *Digital feedthrough* is the glitch impulse injected to the output of a DAC as a result of a digital code change in the DAC input register of the same DAC. It is measured with the full-scale digital code change without updating the DAC output, and is expressed in nV-s.

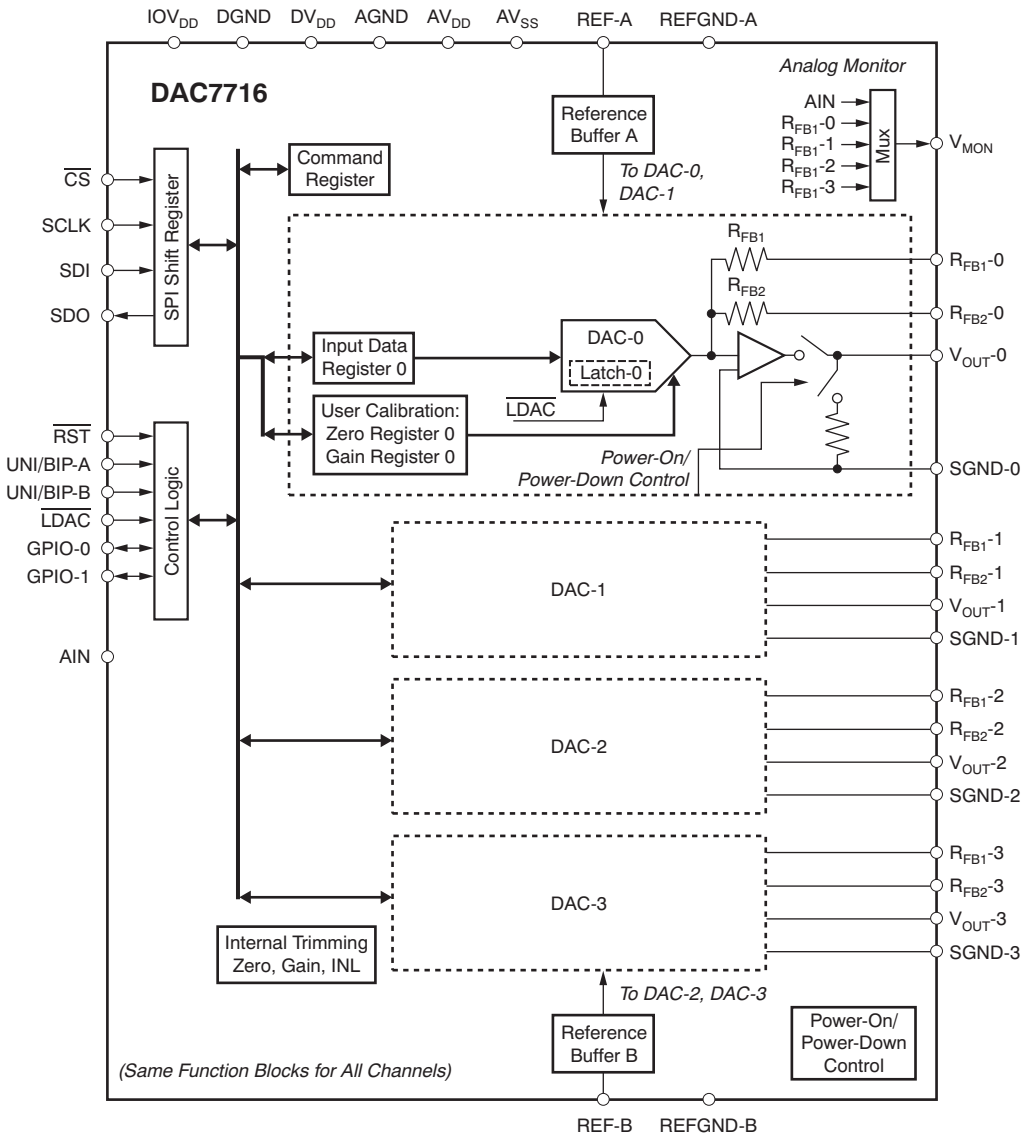
ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, AV_{DD} = +11V to +18V, AV_{SS} = –11V to –18V, V_{REF} = REF-A = REF-B = +5V, DV_{DD} = +5V, IOV_{DD} = +1.8V to DV_{DD}, AGND = DGND = REFGND-A = REFGND-B = SGND-x = 0V, and DAC gain = 4, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7716			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS(13) (SDI, $\overline{CS}$, SCLK, $\overline{RST}$, UNI/BIP-A, UNI/BIP-B, $\overline{LDAC}$, GPIO-x)					
High-level input voltage, V_{IH}	IOV_{DD} = 4.5V to 5.5V	2.5		IOV_{DD} + 0.3	V
	IOV_{DD} = 2.7V to 3.3V	2.1		IOV_{DD} + 0.3	V
	IOV_{DD} = +1.8V	1.6		IOV_{DD} + 0.3	V
Low-level input voltage, V_{IL}	IOV_{DD} = 4.5V to 5.5V	–0.3		0.8	V
	IOV_{DD} = 2.7V to 3.3V	–0.3		0.6	V
	IOV_{DD} = +1.8V	–0.3		0.2	V
Input current				1	µA
Input capacitance			5		pF
DIGITAL OUTPUTS(13) (SDO, GPIO-x)					
SDO high-level output voltage, V_{OH}	IOV_{DD} = 2.7V to 5.5V, sourcing 1mA	IOV_{DD} – 0.4			V
	IOV_{DD} = +1.8V, sourcing 200µA	1.6			V
SDO low-level output voltage, V_{OL}	IOV_{DD} = 2.7V to 5.5V, sinking 1mA			0.4	V
	IOV_{DD} = +1.8V, sinking 200µA			0.2	V
SDO high-impedance leakage				1	µA
SDO high-impedance output capacitance			10		pF
GPIO low-level output voltage, V_{OL}	IOV_{DD} = 2.7V to 5.5V, sinking 1mA	0		0.4	V
	IOV_{DD} = +1.8V, sinking 1mA	0		0.4	V
GPIO open-drain high-level output leakage current	GPIO in Hi-Z and configured as output			1	µA
POWER SUPPLY					
AV_{DD}(14)		+4.75		+24	V
AV_{SS}(15)		–18		–4.75	V
DV_{DD}		+2.7		+5.5	V
IOV_{DD}		+1.7		DV_{DD}	V
AI_{DD} (normal operation)	±10V output range, no loading current, V_{OUT} = 0V		2.7	3.4	mA/Channel
AI_{DD} (power-down)				100	µA
AI_{SS} (normal operation)	±10V output range, no loading current, V_{OUT} = 0V		3.3	4.0	mA/Channel
AI_{SS} (power-down)				100	µA
DI_{DD}	Static current through the DV_{DD} pin with V_{IH} = IOV_{DD} and V_{IL} = DGND		25	50	µA
IOI_{DD}	V_{IH} = IOV_{DD}, V_{IL} = DGND		±1	±10	µA
Power dissipation (normal operation)	±12V power, no loading current, V_{OUT} = 0V		290		mW
TEMPERATURE RANGE					
Specified performance		–40		+105	°C

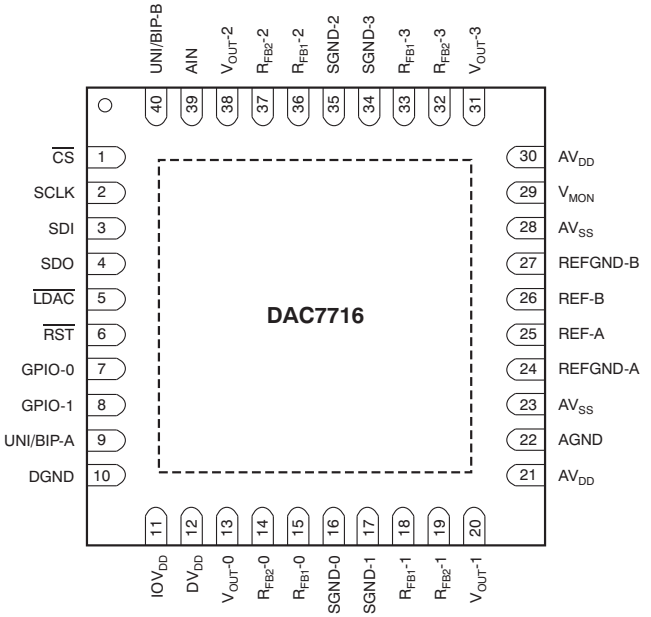
(13) Specified by design and characterization.
(14) AV_{DD} should not be greater than +24V or less than +4.75V. Also, AV_{DD} should not be less than (2 × V_{REF} + 1V) for bipolar output mode and should not be less than (Gain × V_{REF} + 1V) for unipolar output mode. In any case, (AV_{DD} – AV_{SS}) ≤ +36V.
(15) AV_{SS} should not be greater than –4.75V or less than –18V. Also, AV_{SS} should not be greater than (–2 × V_{REF} – 1V). In any case, (AV_{DD} – AV_{SS}) ≤ +36V.

FUNCTIONAL BLOCK DIAGRAM

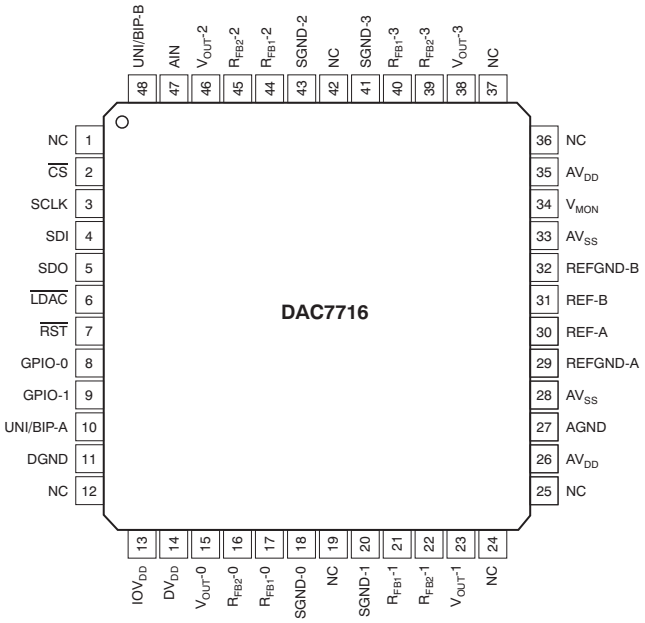


PIN CONFIGURATIONS

RHA PACKAGE[1]
QFN-40
(TOP VIEW)



PFB PACKAGE
TQFP-48
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to AV_{SS} or left floating.

PIN DESCRIPTIONS

PIN NAME	PIN NO.		I/O	DESCRIPTION
	QFN-40	TQFP-48		
$\overline{CS}$	1	2	I	SPI bus chip select input (active low). Data are not clocked into the SPI shift register unless $\overline{CS}$ is low. When $\overline{CS}$ is high, SDO is in a high-impedance state.
SCLK	2	3	I	SPI bus clock
SDI	3	4	I	SPI bus input data
SDO	4	5	O	SPI output data
$\overline{LDAC}$	5	6	I	Load DAC latch control input (active low). When $\overline{LDAC}$ is low, the DAC latch is transparent and the contents of the Input Data Register are transferred to it. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated.
$\overline{RST}$	6	7	I	Reset input (active low). Logic low on this pin resets the input registers and DACs to the values defined by the UNI/BIP pins, and sets the Gain Register and Zero Register to default values.
GPIO-0	7	8	I/O	General-purpose digital input/output 0. This pin is a bidirectional, digital input/output, and has an open-drain output. A 10kΩ pull-up resistor to IOV_{DD} is needed when this pin is used as an output. See the *GPIO Pins* section for details.
GPIO-1	8	9	I/O	General-purpose digital input/output 1. This pin is a bidirectional, digital input/output, and has an open-drain output. A 10kΩ pull-up resistor to IOV_{DD} is needed when this pin is used as an output. See the *GPIO Pins* section for details.
UNI/BIP-A	9	10	I	Output mode selection of group A (DAC-0 and DAC-1). When UNI/BIP-A is tied to IOV_{DD}, group A is in unipolar output mode; when tied to DGND, group A is in bipolar output mode. The input data written to the DAC are straight binary for unipolar output mode and twos complement for bipolar output mode.
DGND	10	11	I	Digital ground
IOV_{DD}	11	13	I	Interface power
DV_{DD}	12	14	I	Digital power
V_{OUT}-0	13	15	O	DAC-0 output

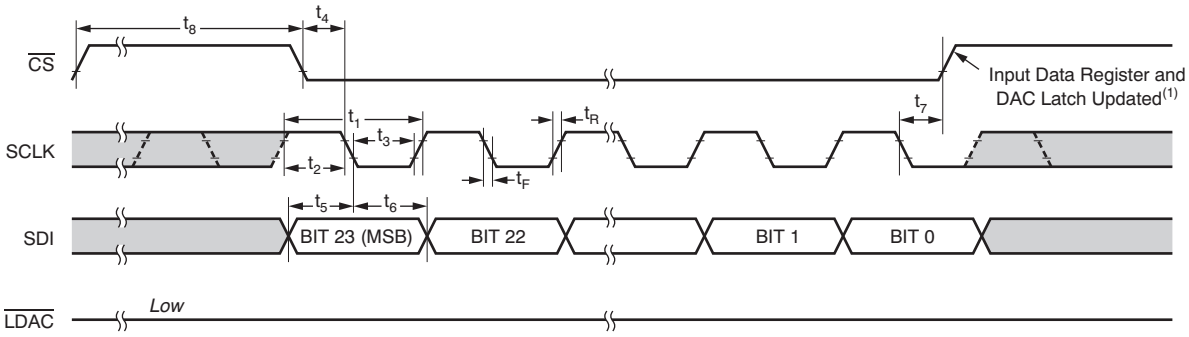
PIN DESCRIPTIONS (continued)

PIN NAME	PIN NO.		I/O	DESCRIPTION
	QFN-40	TQFP-48		
R_{FB2}-0(1)	14	16	O	DAC-0 R_{FB2} feedback
R_{FB1}-0(1)	15	17	O	DAC-0 R_{FB1} feedback
SGND-0	16	18	I	DAC-0 signal ground. Connected to REFGND-A.
SGND-1	17	20	I	DAC-1 signal ground. Connected to REFGND-A.
R_{FB1}-1(1)	18	21	O	DAC-1 R_{FB1} feedback
R_{FB2}-1(1)	19	22	O	DAC-1 R_{FB2} feedback
V_{OUT}-1	20	23	O	DAC-1 output
AV_{DD}	21, 30	26, 35	I	Positive analog power supply
AGND	22	27	I	Analog ground
AV_{SS}	23, 28	28, 33	I	Negative analog power supply
REFGND-A	24	29	I	Reference REF-A ground. Connect to AGND.
REF-A	25	30	I	Group A (DAC-0, DAC-1) reference input
REF-B	26	31	I	Group B (DAC-2, DAC-3) reference input
REFGND-B	27	32	I	Reference REF-B ground. Connect to AGND.
V_{MON}	29	34	O	Analog monitor output. This pin is either in Hi-Z status, or connected to one of the four DAC outputs or AIN, depending on the content of the Monitor Register.
V_{OUT}-3	31	38	O	DAC-3 output
R_{FB2}-3(1)	32	39	O	DAC-3 R_{FB2} feedback
R_{FB1}-3(1)	33	40	O	DAC-3 R_{FB1} feedback
SGND-3	34	41	I	DAC-3 signal ground. Connected to REFGND-B.
SGND-2	35	43	I	DAC-2 signal ground. Connected to REFGND-B.
R_{FB1}-2(1)	36	44	O	DAC-2 R_{FB1} feedback
R_{FB2}-2(1)	37	45	O	DAC-2 R_{FB2} feedback
V_{OUT}-2	38	46	O	DAC-2 output
AIN	39	47	I	Auxiliary analog input. Connected to the analog monitor mux.
UNI/BIP-B	40	48	I	Output mode selection of group B (DAC-2 and DAC-3). When UNI/BIP-A is tied to IOV_{DD}, group B is in unipolar output mode; when tied to DGND, group B is in bipolar output mode. The input data written to the DAC are straight binary for unipolar output mode, and twos complement for bipolar output mode.
NC	—	1, 12, 19, 24, 25, 36, 37, 42		Not connected

(1) To set the DAC-x gain = 2, connect R_{FB1}-x and R_{FB2}-x to V_{OUT}-x, and set the corresponding GAIN bit in the Command Register to '0'. To set the DAC-x gain = 4, connect R_{FB1}-x to V_{OUT}-x, keep R_{FB2}-x open, and set the corresponding GAIN bit in the Command Register to '1'. After power-on reset or user reset, the GAIN bits are set to '1' by default; for gain = 2, the gain bits must be cleared to '0'.

TIMING DIAGRAMS

Case 1: Stand-alone mode, $\overline{LDAC}$ tied low.



Case 2: Stand-alone mode, $\overline{LDAC}$ active high.

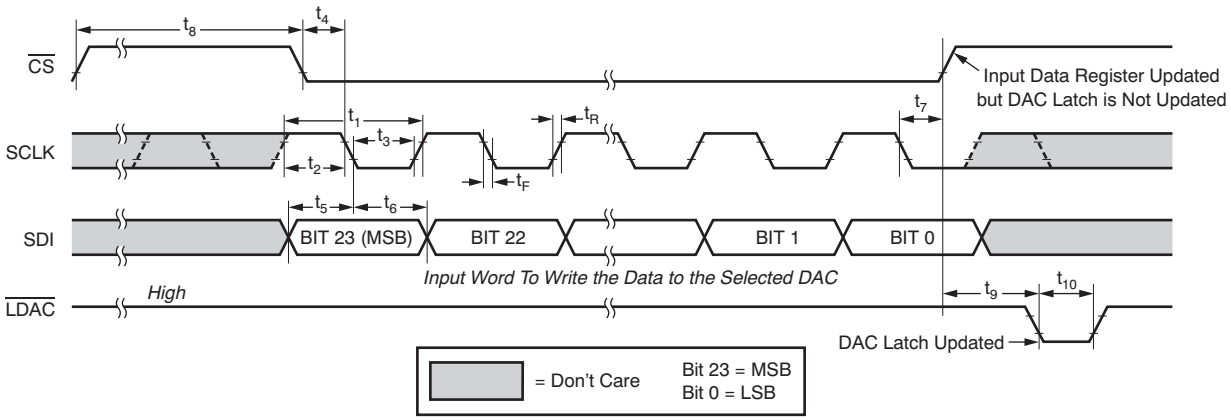


Figure 1. SPI Timing for Stand-Alone Mode

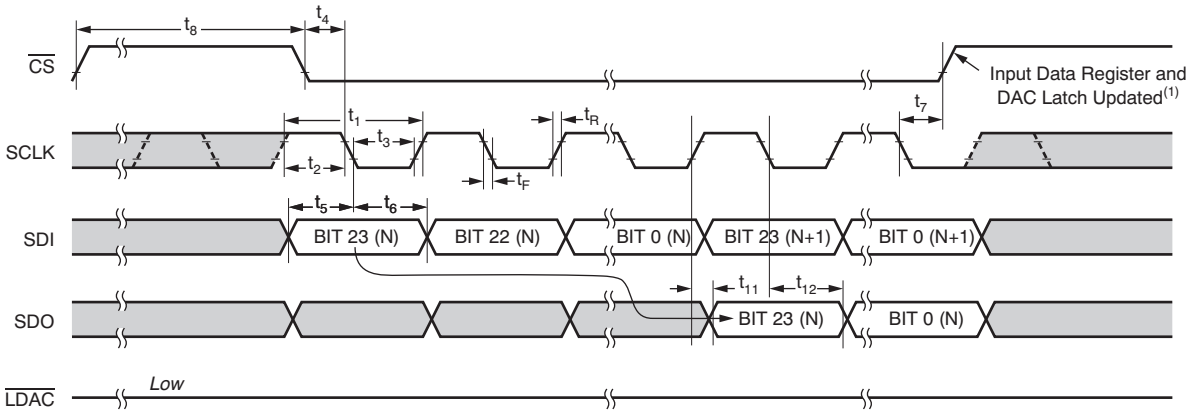
TIMING CHARACTERISTICS For Figure 1(1)(2)(3)

At T_A = –40°C to +105°C, unless otherwise noted.

PARAMETER		2.7V ≤ DV_{DD} ≤ 5.5V, IOV_{DD} = 1.8V		2.7V ≤ DV_{DD} ≤ 3.6V, 2.7V ≤ IOV_{DD} ≤ DV_{DD}		3.6V < DV_{DD} ≤ 5.5V, 2.7V ≤ IOV_{DD} ≤ DV_{DD}		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCLK}	Clock frequency		30		40		50	MHz
t_1	SCLK cycle time	33		25		20		ns
t_2	SCLK high time	16		12		10		ns
t_3	SCLK low time	16		12		10		ns
t_4	$\overline{CS}$ falling edge to SCLK falling edge(4)	11		9		7		ns
t_5	Input data setup time	5		5		5		ns
t_6	Input data hold time	5		5		5		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	15		12		10		ns
t_8	$\overline{CS}$ high time	60		50		30		ns
t_9	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	30		25		20		ns
t_{10}	$\overline{LDAC}$ pulse width	25		20		15		ns
	$\overline{RST}$ pulse width	25		20		15		ns

(1) Specified by design and characterization.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) All input signals are specified with t_R = t_F = 2ns (10% to 90% of IOV_{DD}) and timed from a voltage level of IOV_{DD}/2.
(4) The first SCLK edge after $\overline{CS}$ goes low must be a falling edge.

Case 3: Daisy-Chain mode, $\overline{\text{LDAC}}$ tied low.



Case 4: Daisy-Chain mode, $\overline{\text{LDAC}}$ active.

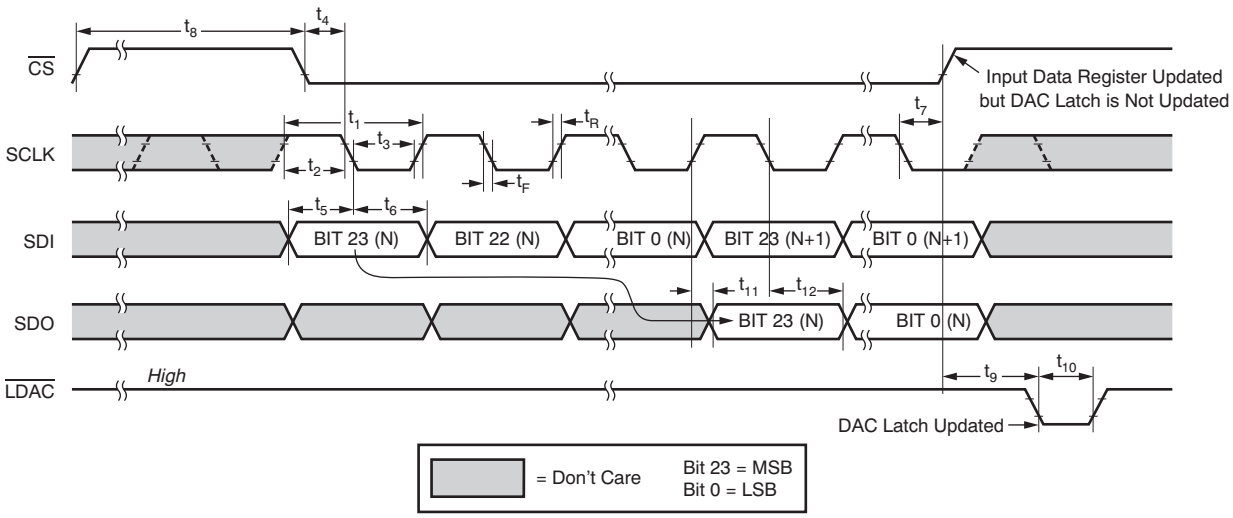


Figure 2. SPI Timing for Daisy-Chain Mode

Case 5: Readback for Stand-alone mode.

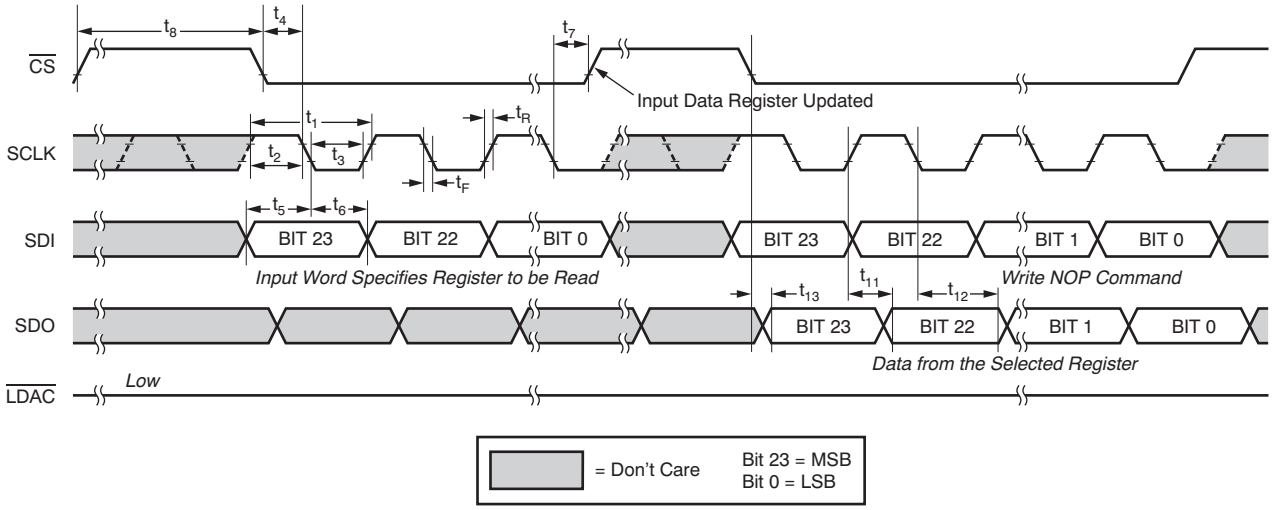


Figure 3. SPI Timing for Readback Operation in Stand-Alone Mode

TIMING CHARACTERISTICS For Figure 2 to Figure 3[1][2][3]

At T_A = –40°C to +105°C, unless otherwise noted.

PARAMETER		2.7V ≤ DV_{DD} ≤ 5.5V, IOV_{DD} = 1.8V		2.7V ≤ DV_{DD} ≤ 3.6V, 2.7V ≤ IOV_{DD} ≤ DV_{DD}		3.6V < DV_{DD} ≤ 5.5V, 2.7V ≤ IOV_{DD} ≤ DV_{DD}		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCLK}	Clock frequency		15		20		25	MHz
t_1	SCLK cycle time	66		50		40		ns
t_2	SCLK high time	33		25		20		ns
t_3	SCLK low time	33		25		20		ns
t_4	$\overline{CS}$ falling edge to SCLK falling edge[4]	25		22		17		ns
t_5	Input data setup time	5		5		5		ns
t_6	Input data hold time	5		5		5		ns
t_7	SCLK falling edge to $\overline{CS}$ rising edge	15		12		10		ns
t_8	$\overline{CS}$ high time	60		50		30		ns
t_9	$\overline{CS}$ rising edge to $\overline{LDAC}$ falling edge	30		25		20		ns
t_{10}	$\overline{LDAC}$ pulse width	25		20		15		ns
t_{11}	SDO data valid from SCLK rising edge		25		20		15	ns
t_{12}	SDO data hold time from SCLK falling edge	30		25		20		ns
t_{13}	SDO data valid from $\overline{CS}$ falling edge		20		17		12	ns
	$\overline{RST}$ pulse width	25		20		15		ns

(1) Specified by design and characterization.
(2) Sample tested during the initial release and after any redesign or process changes that may affect these parameters.
(3) All input signals are specified with t_R = t_F = 2ns (10% to 90% of IOV_{DD}) and timed from a voltage level of IOV_{DD}/2.
(4) The first SCLK edge after $\overline{CS}$ goes low must be a falling edge.

TYPICAL CHARACTERISTICS

LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

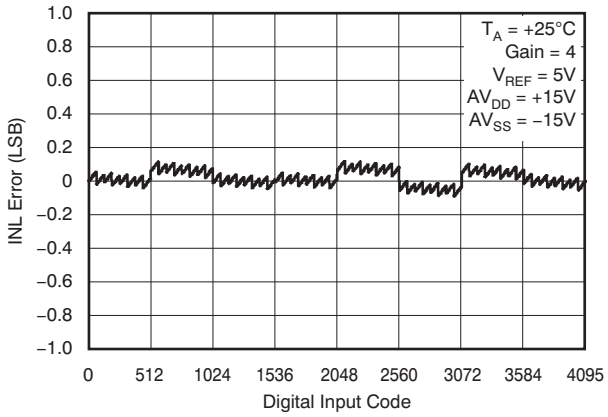


Figure 4.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

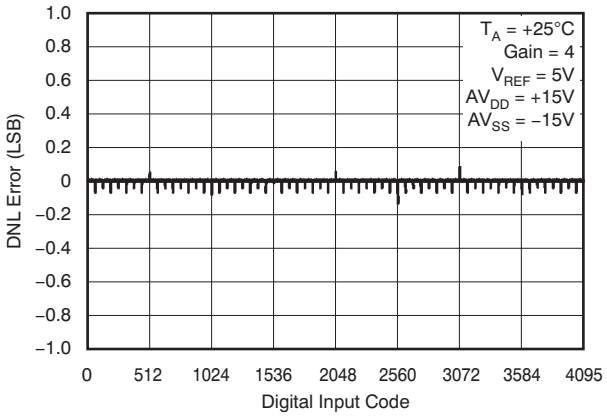


Figure 5.

LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

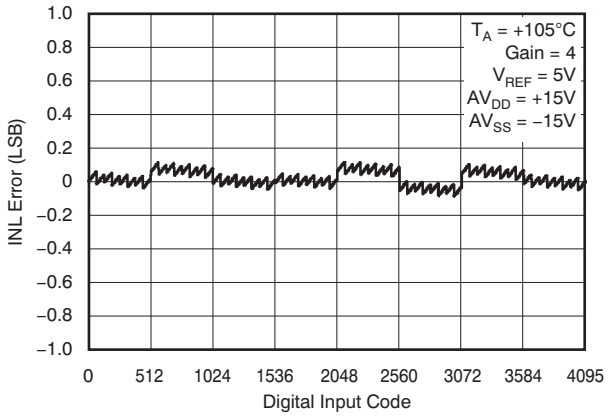


Figure 6.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

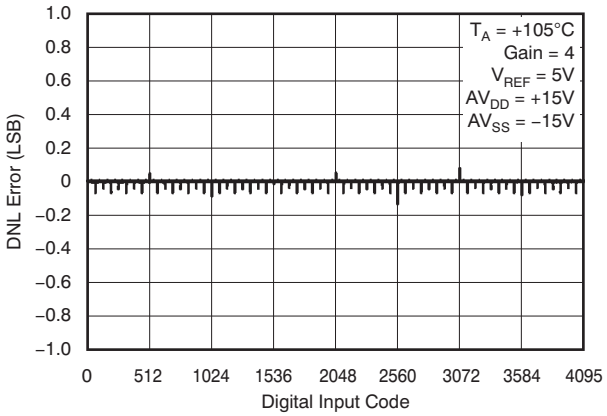


Figure 7.

LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

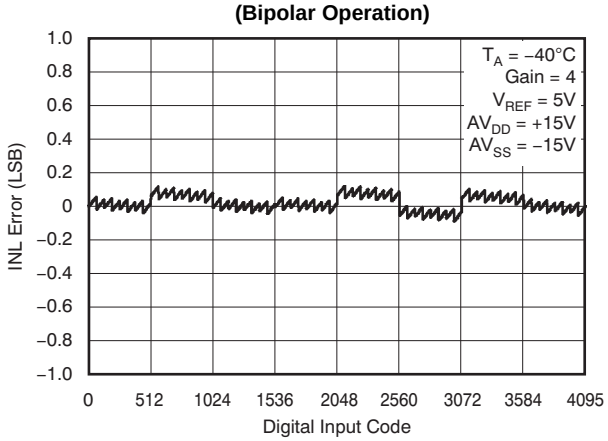


Figure 8.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

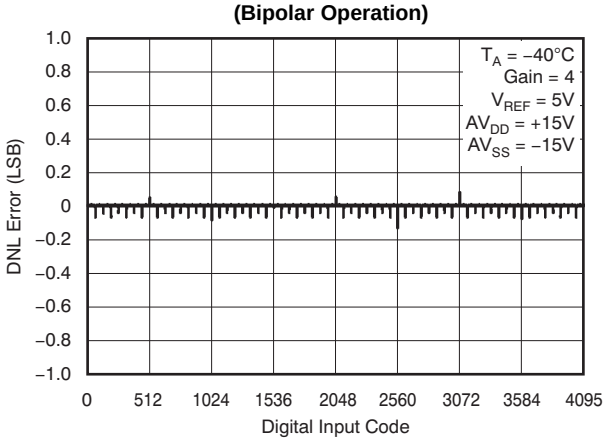


Figure 9.

TYPICAL CHARACTERISTICS (continued)

LINEARITY ERROR vs DIGITAL INPUT CODE (All Channels, Bipolar Operation)

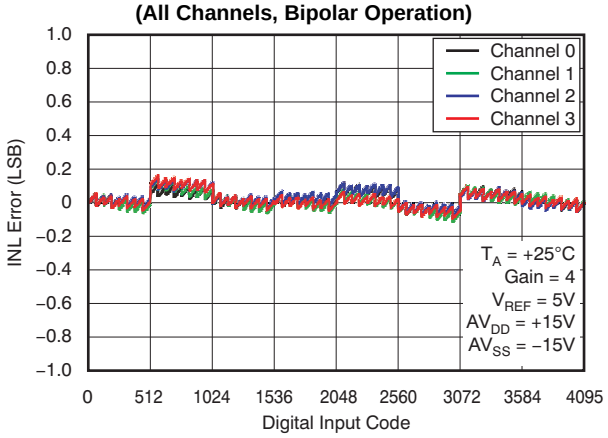


Figure 10.

LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

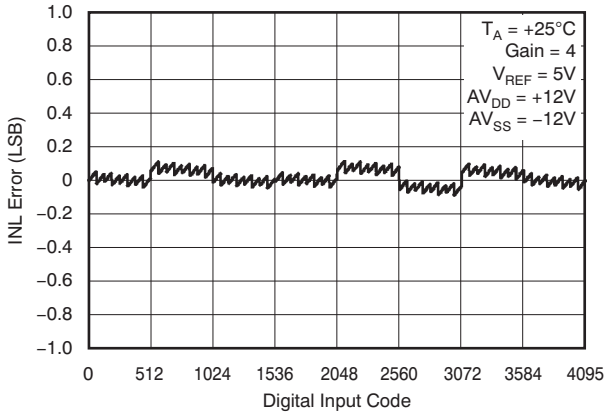


Figure 11.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (Bipolar Operation)

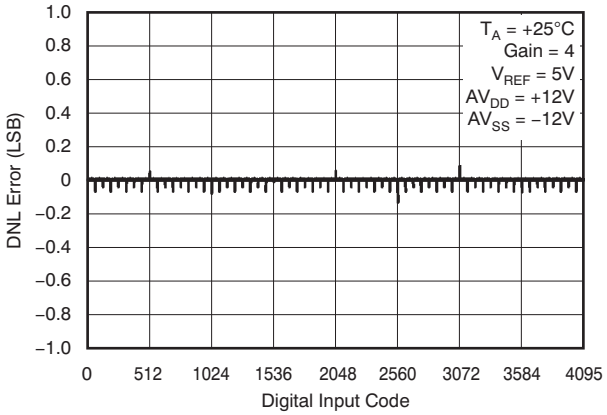


Figure 12.

LINEARITY ERROR vs DIGITAL INPUT CODE (Unipolar 0V to 20V Operation)

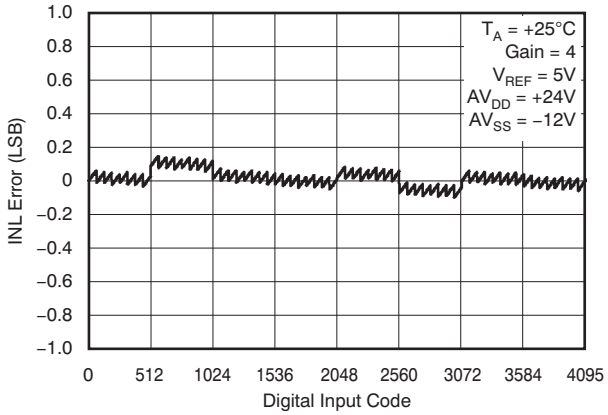


Figure 13.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE (Unipolar 0V to 20V Operation)

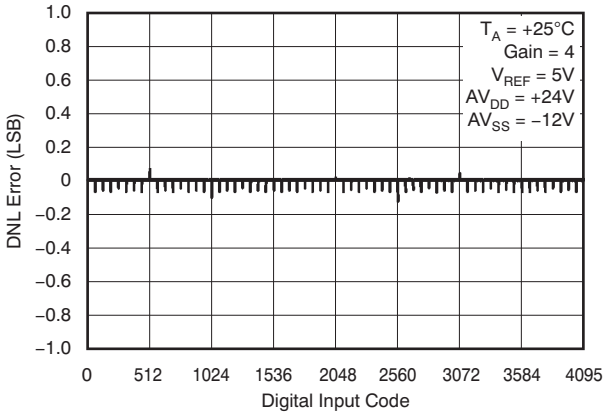


Figure 14.

TYPICAL CHARACTERISTICS (continued)

LINEARITY ERROR vs TEMPERATURE (Bipolar Operation)

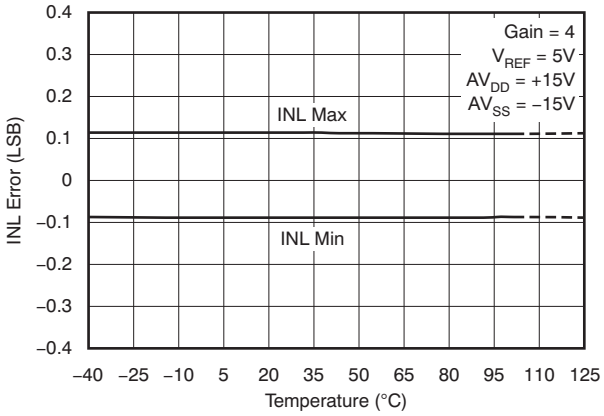


Figure 15.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE (Bipolar Operation)

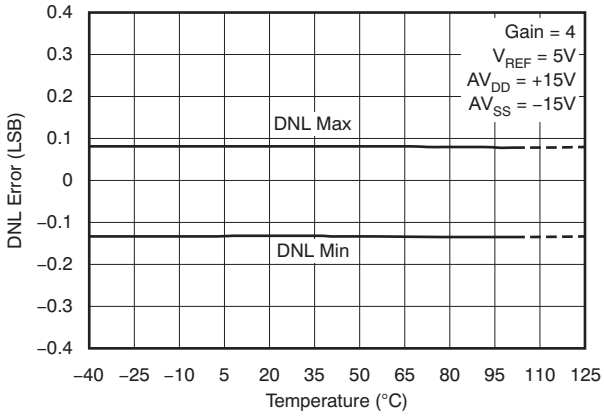


Figure 16.

LINEARITY ERROR vs REFERENCE VOLTAGE (Bipolar Operation)

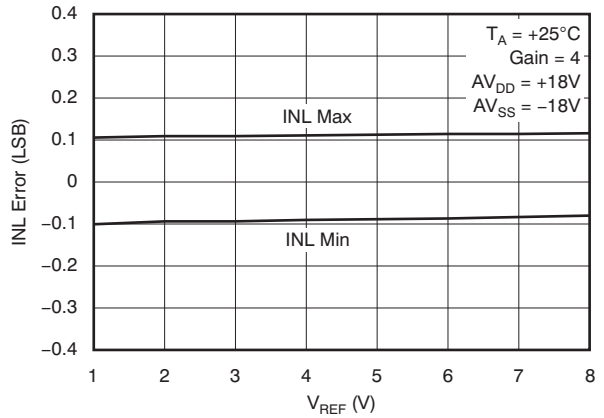


Figure 17.

DIFFERENTIAL LINEARITY ERROR vs REFERENCE VOLTAGE (Bipolar Operation)

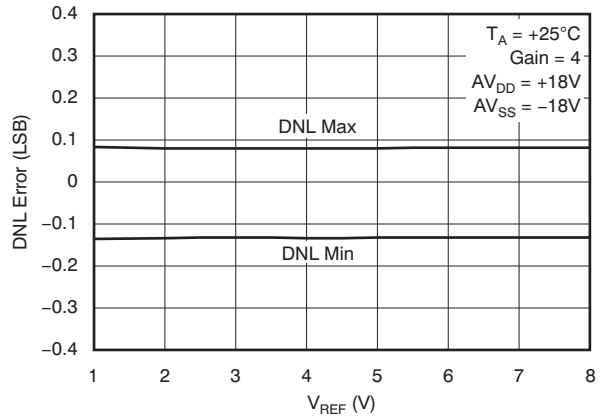


Figure 18.

LINEARITY ERROR vs SUPPLY VOLTAGE (Bipolar Operation)

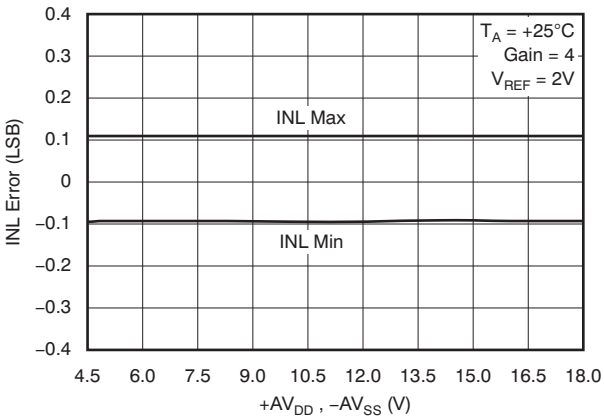


Figure 19.

DIFFERENTIAL LINEARITY ERROR vs SUPPLY VOLTAGE (Bipolar Operation)

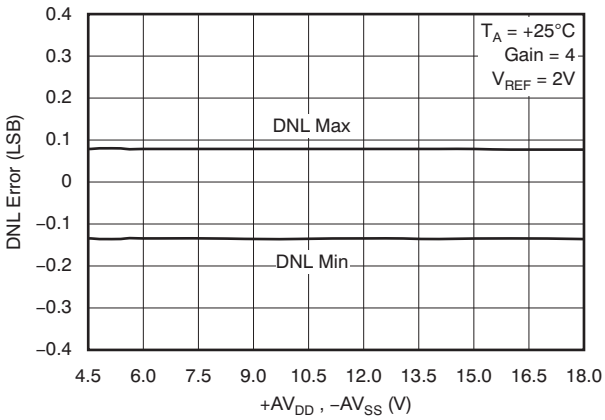


Figure 20.

TYPICAL CHARACTERISTICS (continued)

BIPOLAR GAIN ERROR vs REFERENCE VOLTAGE (10 Units, 40 Channels Total)

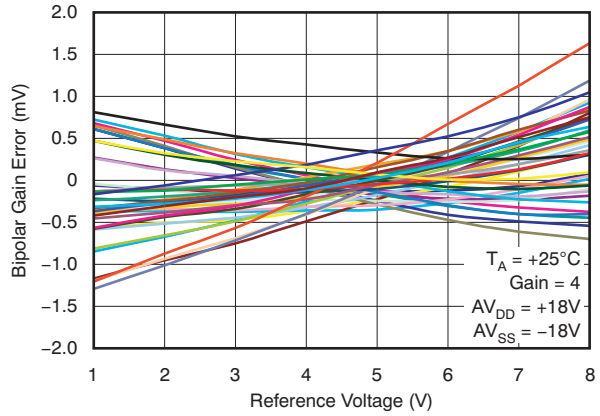


Figure 21.

BIPOLAR ZERO ERROR vs REFERENCE VOLTAGE (10 Units, 40 Channels Total)

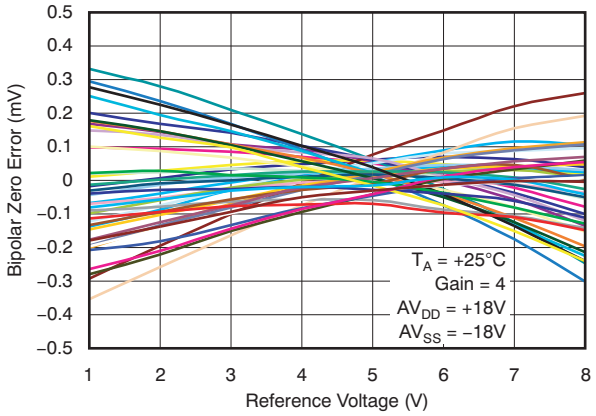


Figure 22.

BIPOLAR GAIN ERROR vs TEMPERATURE (10 Units, 40 Channels Total)

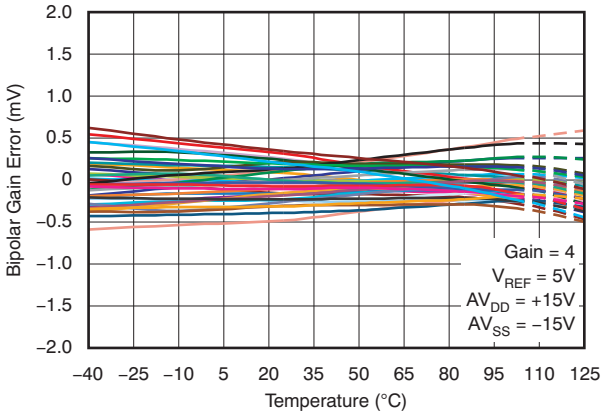


Figure 23.

BIPOLAR ZERO ERROR vs TEMPERATURE (10 Units, 40 Channels Total)

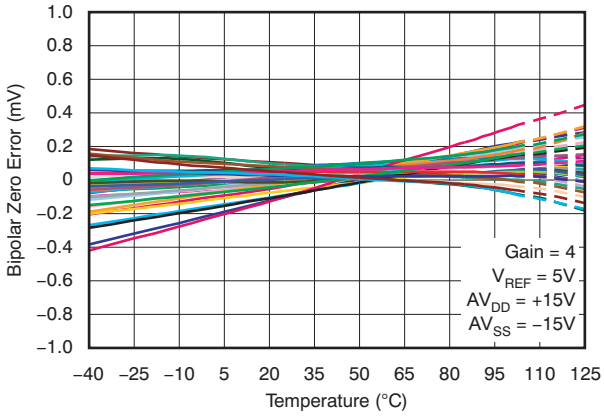


Figure 24.

UNIPOLAR ZERO ERROR vs REFERENCE VOLTAGE (10 Units, 40 Channels Total)

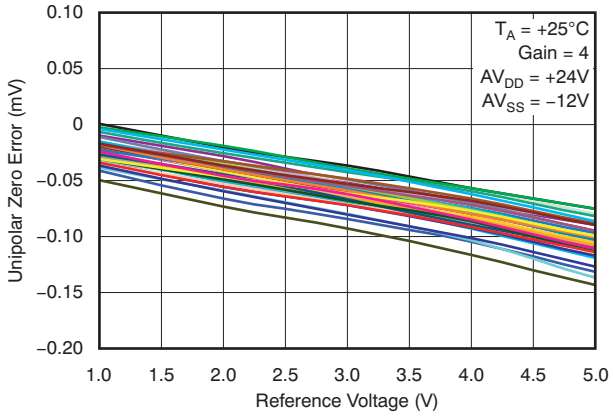


Figure 25.

UNIPOLAR ZERO ERROR vs TEMPERATURE (10 Units, 40 Channels Total)

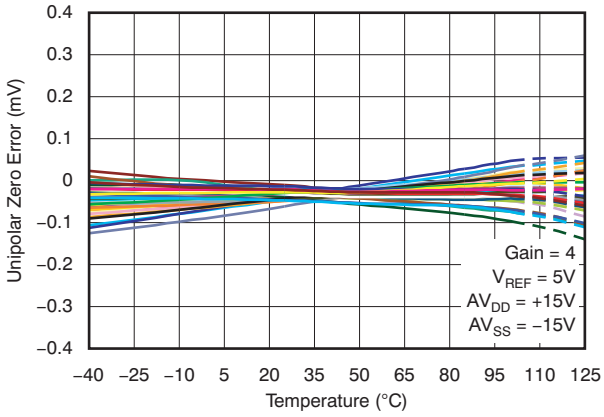


Figure 26.

TYPICAL CHARACTERISTICS (continued)

TOTAL SUPPLY CURRENT vs DIGITAL INPUT CODE

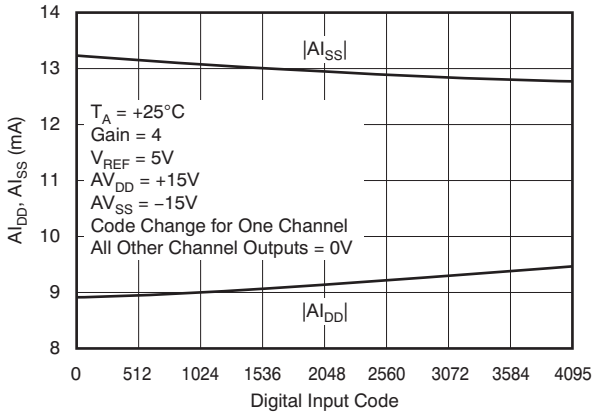


Figure 27.

DELTA OUTPUT VOLTAGE vs SOURCE/SINK CURRENT (Bipolar Operation)

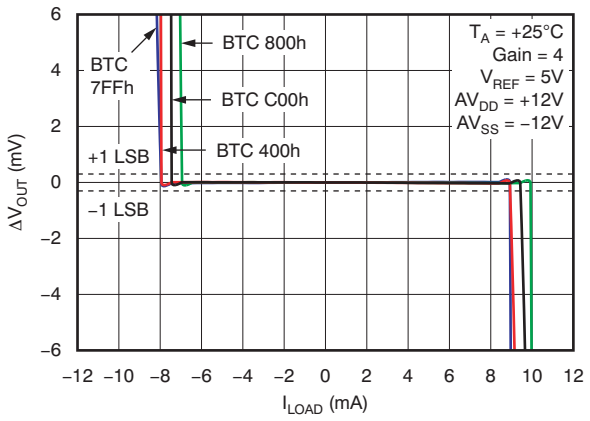


Figure 28.

MAJOR CARRY GLITCH

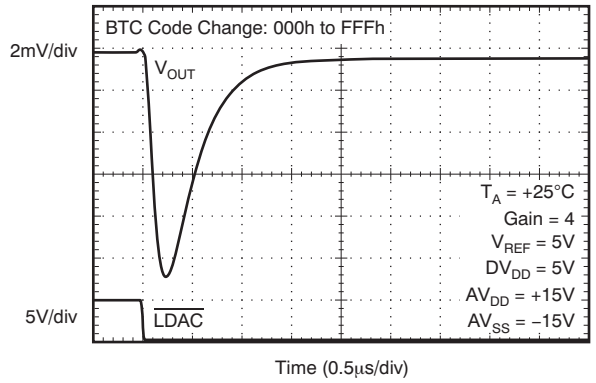


Figure 29.

MAJOR CARRY GLITCH

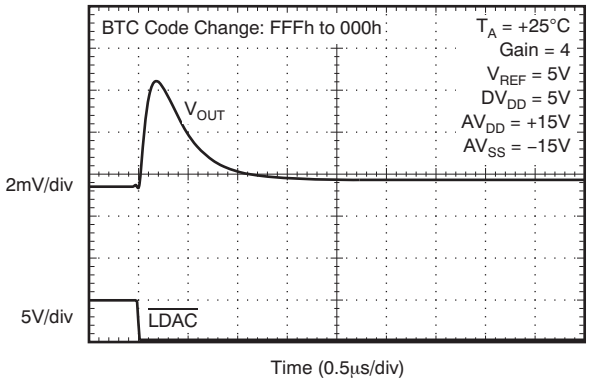


Figure 30.

SETTLING TIME (+10V to –10V Transition)

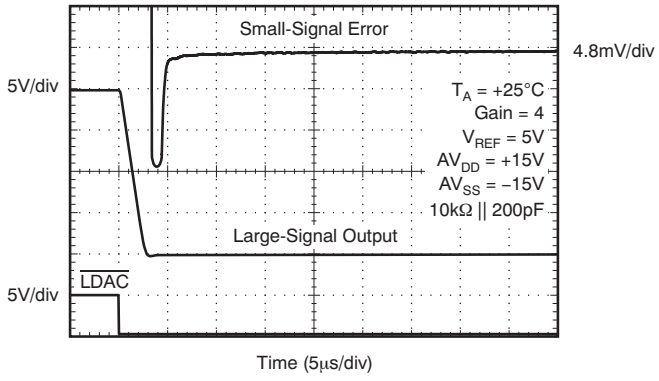


Figure 31.

SETTLING TIME (–10V to +10V Transition)

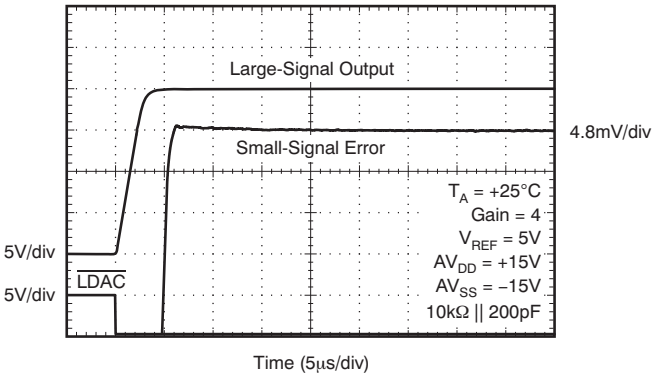


Figure 32.

TYPICAL CHARACTERISTICS (continued)

0.1Hz TO 10Hz NOISE (Bipolar Operation)

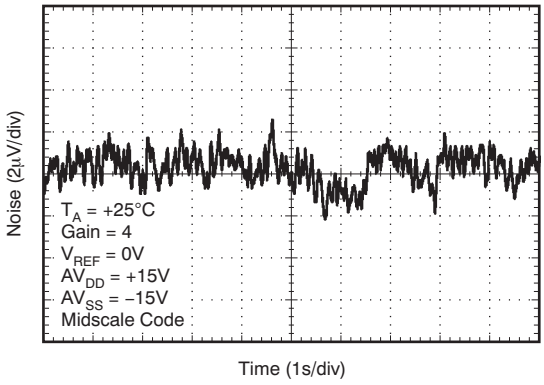


Figure 33.

IOV_{DD} SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

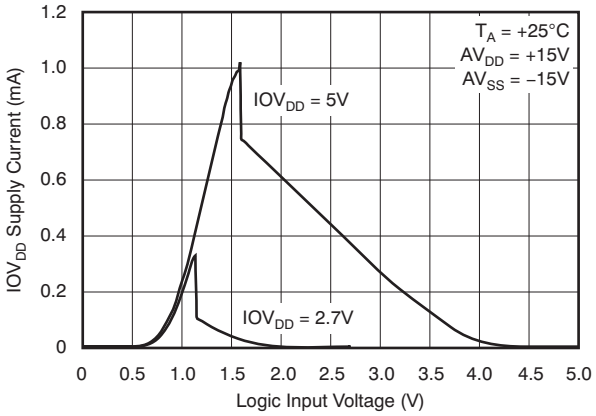


Figure 34.

AI_{DD} PRODUCTION DISTRIBUTION

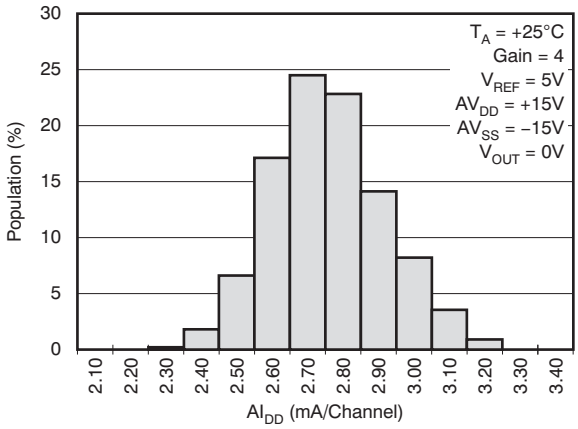


Figure 35.

AI_{SS} PRODUCTION DISTRIBUTION

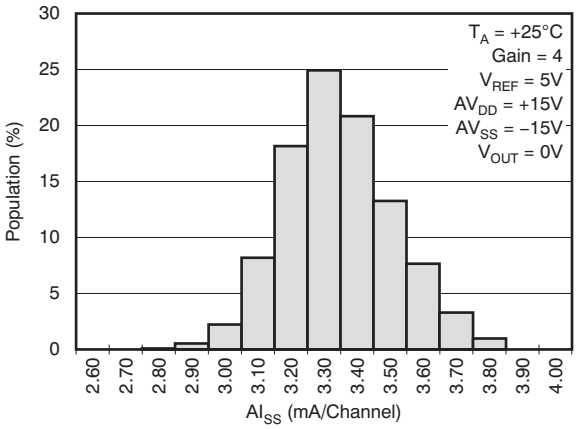


Figure 36.

BIPOLAR GAIN ERROR PRODUCTION DISTRIBUTION

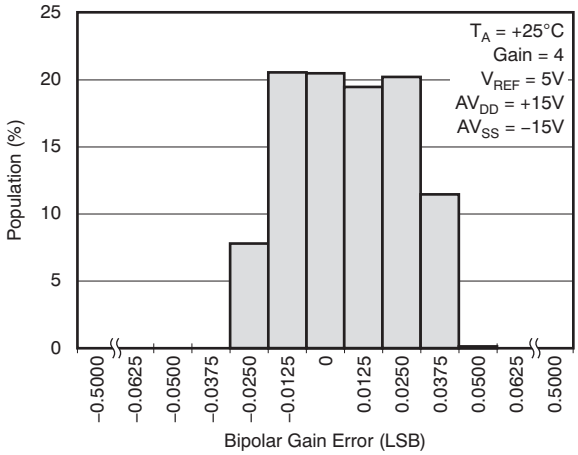


Figure 37.

BIPOLAR ZERO ERROR PRODUCTION DISTRIBUTION

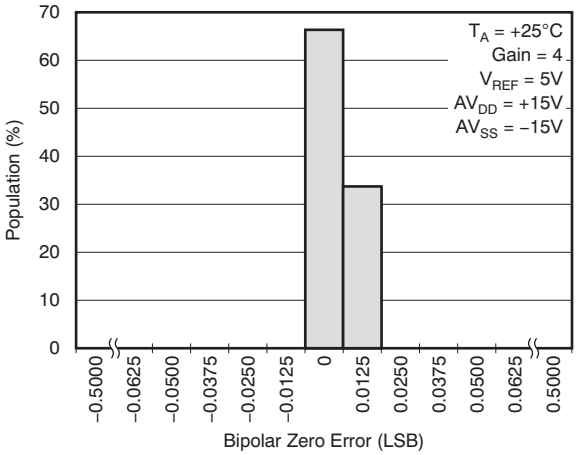


Figure 38.

TYPICAL CHARACTERISTICS (continued)

UNIPOLAR GAIN ERROR PRODUCTION DISTRIBUTION

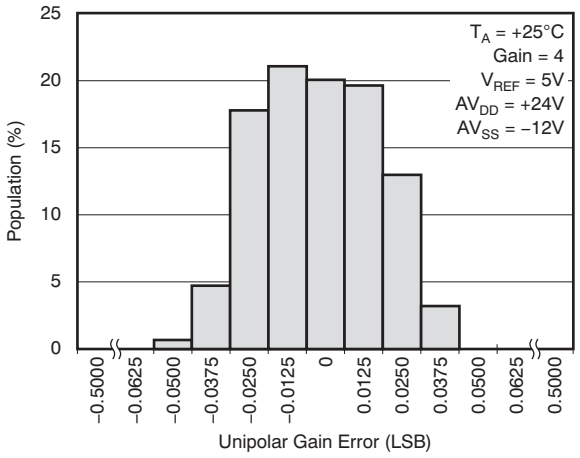


Figure 39.

UNIPOLAR ZERO ERROR PRODUCTION DISTRIBUTION

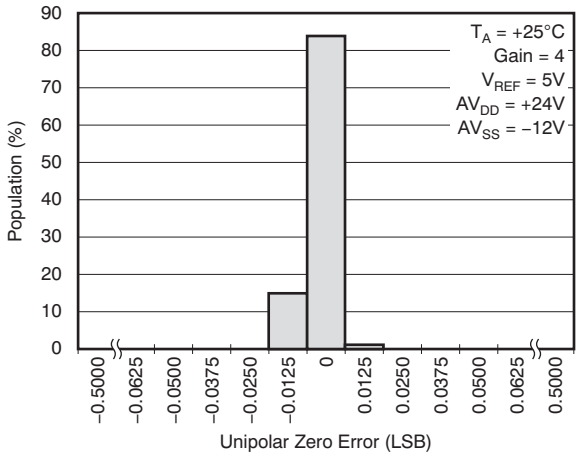


Figure 40.

THEORY OF OPERATION

DAC ARCHITECTURE

The DAC7716 is a highly-integrated, quad-channel, 12-bit, voltage-output DAC with internal reference buffers and output buffers. Each channel consists of an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier, as shown in Figure 41. The DAC7716 has a high-impedance, buffered reference input; the output of the reference buffers drives the R-2R ladders. The output buffer is designed to allow user-configurable adjustments, giving the DAC7716 four different output voltage range settings. With the production trim process, this device has excellent dc accuracy and ac performance.

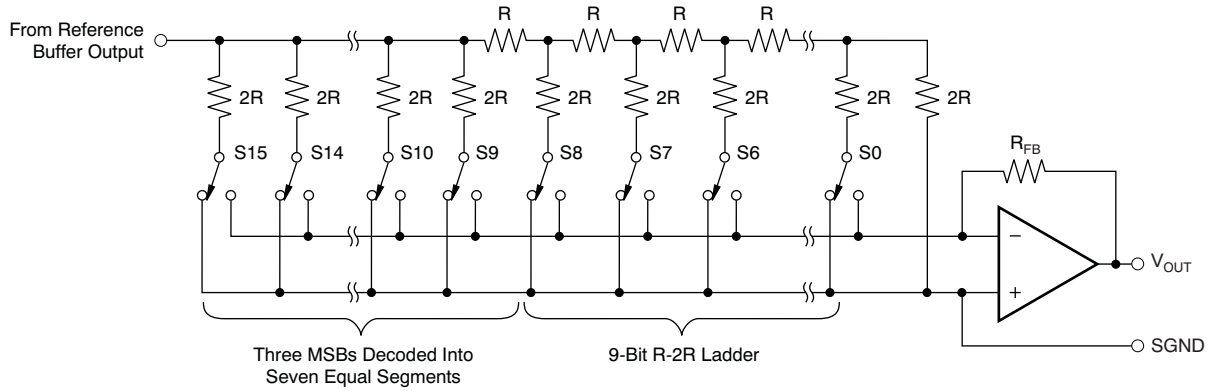


Figure 41. DAC7716 Architecture

CHANNEL GROUPS

The four DAC channels are arranged into two groups (A and B) with two channels per group. Group A consists of DAC-0 and DAC-1, and Group B consists of DAC-2 and DAC-3. The two DAC channels of Group A derive their reference voltage from REF-A, and those of Group B from REF-B.

USER-CALIBRATION FOR ZERO ERROR AND GAIN ERROR

The DAC7716 implements a user-calibration function that allows for trimming the system gain and zero errors. Each DAC channel has a Gain Register and Zero Register and the DAC output is calibrated according to the value of the corresponding registers. The range of gain adjustment is typically ±0.195% of full-scale with 0.0625 LSB per step. The zero code adjustment is typically ±0.0488% of full-scale with 0.0078 LSB per step. The input data format of the Gain and Zero registers is twos complement. Refer to Table 9 and Table 10 for more details.

If the system-level calibration is not needed, these registers should be left at the respective default values (0000h) at power-on.

TRANSFER FUNCTION FOR THE ANALOG OUTPUTS (V_{OUT}-0 to V_{OUT}-3)

For bipolar output:

$$V_{OUT} = Gain \times V_{REF} \times \left(\frac{INPUT\_CODE}{4096} + \frac{ZERO\_CODE}{128 \times 4096} \right) \times \left(1 + \frac{GAIN\_CODE}{32 \times 4096} \right) \quad (1)$$

For unipolar output:

$$V_{OUT} = Gain \times V_{REF} \times \left(\frac{INPUT\_CODE}{4096} + \frac{ZERO\_CODE}{128 \times 4096} \right) \times \left(1 + \frac{GAIN\_CODE}{16 \times 4096} \right) \quad (2)$$

Where:

GAIN is the DAC gain, which can be set to x2 or x4 and is determined by the connection of pins R_{FB1}-x and R_{FB2}-x to V_{OUT}-x, and the GAIN bit in the Command Register.

INPUT_CODE is the decimal equivalent value of the code written into the DAC input register.

ZERO_CODE is the decimal equivalent value of the code written into the Zero Register.

GAIN_CODE is the decimal equivalent value of the code written into the Gain Register.

Note that the output voltage must not be greater than (AV_{DD} – 1.0V) or less than (AV_{SS} + 1.0V); otherwise, the output may be saturated.

Input Data Format

For bipolar output operation, INPUT_CODE is always twos complement, and can accept values between –2048 to 2047.

For unipolar output operation, INPUT_CODE is always straight binary, and can accept values between 0 to 4095.

GAIN_CODE is always in twos complement format, and can accept values between –128 and +127.

ZERO_CODE is always in twos complement format and can accept values between –256 and +255.

The data written to the Command and Monitor registers are written as specified in the definitions. For read operations, the read-back data format is the same as the format used to write to the device. Refer to the *Internal Registers* section for more details.

OUTPUT RANGE

Each channel of the DAC7716 implements an output amplifier that provides a unipolar output or a bipolar output with a gain of 2 or 4. The output span equals the gain times the reference voltage. For a 5V reference, the output range can be configured as ±10V, ±5V, 0V to 20V, or 0V to 10V. The status of the UNI/BIP pin determines the output mode (unipolar or bipolar) of each group. When the UNI/BIP-A pin is high, the outputs of Group A (DAC-0 and DAC-1) are unipolar; when the pin is low, the outputs of Group A are bipolar. Similarly, the UNI/BIP-B pin defines the output mode of Group B (DAC-2 and DAC-3).

Each individual DAC can be configured with a gain of 4 or a gain of 2. To set the gain = 4, connect R_{FB1}-x to V_{OUT}-x with R_{FB2}-x left open, and set the gain bit for that channel to '1' in the Command Register. To set the gain = 2, connect both R_{FB1}-x and R_{FB2}-x to V_{OUT}-x, and set the gain bit for that channel to '0'. The gain bits in the Command Register are set to '1' by default at power-on or reset, and must be cleared to '0' for gain = 2.

Note that the power supplies must meet the following requirements:

- AV_{DD} must not be greater than 24V or less than 4.75V, and AV_{SS} must not be greater than –4.75V or less than –18V. In any case, (AV_{DD} – AV_{SS}) ≤ 36V.
- For bipolar mode: $AV_{DD} \geq 2 \times V_{REF} + 1V$, and $AV_{SS} \leq -2 \times V_{REF} - 1V$.
- For unipolar mode: $AV_{DD} \geq Gain \times V_{REF} + 1V$, and $AV_{SS} \leq -2 \times V_{REF} - 1V$.

For example, for a 5V reference in bipolar operation, the minimum supplies must be at least ±11V, regardless of whether the output range is ±5V or ±10V. For unipolar operation with the same reference, the supplies must be at least ±11V for a 0V to 10V operation, and +21V/–11V for a 0V to +20V operation.

UPDATING THE DAC OUTPUTS

The DAC7716 has a double-buffered interface that consists of two register banks for every channel: the input register and the DAC latch. The digital code is transferred from the SPI shift register to the addressed channel input register upon completion of a valid write sequence. The DAC latch contains the digital code used by the resistor R-2R ladder. The contents of the DAC latch define the output from the DAC. The DAC outputs can be updated individually or simultaneously. The DAC7716 updates the DAC latch only if it has been accessed since the last time the $\overline{\text{LDAC}}$ pin was brought low or the LD bit in the Command Register was set to '1', thereby eliminating any unnecessary glitch. The DAC channels that were not accessed are not reloaded, and the output values remain unchanged.

Individual DAC Channel Update

In this mode, the $\overline{\text{LDAC}}$ pin is held low while the $\overline{\text{CS}}$ pin is low and the data are clocked into the SPI shift register. At the end of the data transfer into the shift register, the $\overline{\text{CS}}$ pin is brought high. This action updates both the addressed input data register and the corresponding DAC latch register. The DAC latch register controls the R-2R switches; thus, an update on the DAC latch register updates the corresponding DAC channel analog output.

Simultaneous Update of Multiple DAC Channels

In this mode, the $\overline{\text{LDAC}}$ pin is held high while the $\overline{\text{CS}}$ pin is low and data are clocked into the SPI shift register. At the end of the data transfer into the shift register, the $\overline{\text{CS}}$ pin is brought high. This action updates only the addressed input data register; it does not update the DAC latch register or change the output. The DAC latch and the analog output are updated only when the $\overline{\text{LDAC}}$ pin goes low, or when the LD bit in the Command Register is set to '1' at anytime after the input data register is written.

HARDWARE RESET

When the $\overline{\text{RST}}$ pin is low, the device is in hardware reset. All the analog outputs (V_{OUT}-0 to V_{OUT}-3), the input registers, and the DAC latches are set to the reset values shown in Table 1. All registers are loaded with default values. Communication is disabled, and the signals on the SDI, $\overline{\text{CS}}$, and SCLK pins are ignored. On the rising edge of the $\overline{\text{RST}}$ pin, the analog outputs (V_{OUT}-0 to V_{OUT}-3) maintain the reset value (0V) until a new value is programmed. After the $\overline{\text{RST}}$ pin goes high, the device returns to normal operation. Note that the default values of the gain bits in the Command Register are '1' after a reset. For gain = 2, the gain bits must be cleared to '0'.

Table 1. Reset Values

UNI/BIP PIN	OUTPUT MODE	INPUT FORMAT	VALUE OF INPUT REGISTER AND DAC LATCH	V_{OUT}
DGND	Bipolar	Twos Complement	0000h	0V
IOV_{DD}	Unipolar	Straight Binary	0000h	0V

Setting the RST bit in the Command Register to '1' performs a software reset, which is functionally the same as a hardware reset. After reset completes, the RST bit returns to '0' automatically.

POWER-ON RESET

On power-on, the input data registers and DAC latches are loaded with the value defined by the UNI/BIP pins (see Table 1). All other registers are loaded with default values. After power-on, the outputs of the V_{OUT} pins are set to 0V.

ANALOG OUTPUT MONITOR PIN (V_{MON})

The V_{MON} pin is the analog output monitor. The analog output monitor function consists of an analog multiplexer addressed via the serial interface, allowing one of the four channel outputs or the AIN input to be routed to this pin for monitoring. The monitor function is controlled by the Monitor Register, which allows the monitored output to be enabled or disabled. When all multiplexer channels are disabled, the monitor output is high impedance; therefore, several monitor outputs can be connected in parallel with only one enabled at a time. Table 5 shows the settings relevant to the monitor function.

Note that the multiplexer is implemented as a series of analog switches. Care should be taken to ensure the maximum current from the V_{MON} pin must not be greater than the given specification because such a condition could conceivably cause a large amount of current to flow from the input of the multiplexer (that is, from V_{OUT}-x or AIN) to the output of the multiplexer (V_{MON}). Also, the V_{MON} pin output impedance is approximately 2.2kΩ; therefore, V_{MON} should be measured with a high-impedance input.

POWER-DOWN MODE

The DAC7716 implements a group power-down feature to reduce power consumption in case some channels are idle. When the power-down bit (PD-A and/or PD-B) in the Command Register is set to '1', the corresponding group goes into a power-down state. During power-down, the reference buffer and output buffers of that group are powered down and the corresponding analog outputs are set to 0V through an internal 10kΩ resistor to AGND. The contents of the internal registers do not change, and the bus interface remains active in order to continue communication and receive commands from the host controller. Any internal register can be read from or written to. The host controller can wake the device from power-down mode and return to normal operating mode by clearing the power-down bit (PD-A and/or PD-B) in the Command Register. Recovery completes in approximately 50µs.

POWER-SUPPLY SEQUENCING

In order to ensure proper initialization of the DAC7716, the digital supplies (DV_{DD} and IOV_{DD}) and logic inputs (UNI/BIP-x) must be applied before AV_{SS} and AV_{DD}. Additionally, AV_{SS} must be applied before AV_{DD} unless both can ramp up at the same time. REF-x should be applied after AV_{DD} comes up in order to make sure the ESD protection circuitry does not turn on.

GENERAL-PURPOSE INPUT/OUTPUT PINS (GPIO-0, -1)

The GPIO-0 and GPIO-1 pins are general-purpose, bidirectional, digital input/output (I/O) signals, as Figure 42 shows. These pins can receive an input or produce an output. When the GPIO-n pin acts as an output, it has an open-drain, and the status is determined by the corresponding GPIO-n bit of the Command Register. The output status is high impedance when the GPIO-n bit is set to '1', and is logic low when the GPIO-n bit is cleared ('0'). Note that a 10kΩ pullup resistor is required when using the GPIO-n pin as an output.

To use the GPIO-n pin as an input, the GPIO-n bits in the Command Register must be set to '1'. When the GPIO-n pin acts as input, the digital value on the pin is acquired by reading the GPIO-n bit.

After a power-on reset or any forced hardware or software reset, all GPIO-n bits are set to '1', and the GPIO-n pin goes to a high-impedance state.

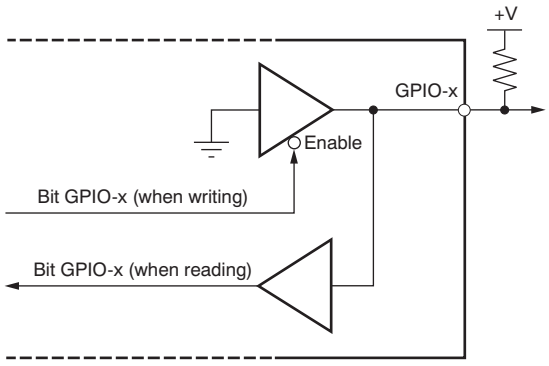


Figure 42. GPIO Pins

SERIAL INTERFACE

The DAC7716 is controlled over a versatile, three-wire serial interface that operates at clock rates of up to 50MHz and is compatible with SPI, QSPI™, Microwire™, and DSP™ standards.

SPI Shift Register

The SPI Shift Register is 24 bits wide. Data are loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. The falling edge of $\overline{CS}$ starts the communication cycle. Data are latched into the SPI Shift Register on the falling edge of SCLK while $\overline{CS}$ is low. When $\overline{CS}$ is high, SCLK is blocked, SDI is ignored, and the SDO line is in a high-impedance state. The contents of the SPI Shift Register are loaded into the addressed internal register on the rising edge of $\overline{CS}$. The SPI Shift Register consists of a read/write bit, four register address bits, 12 data bits, and seven reserved bits, as shown in Table 2. The timing for this operation is shown in the *Timing Diagrams* section. When the device is loaded, the command is decoded, and the new data are transferred into the proper data registers.

The serial interface works with both continuous and non-continuous serial clocks. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data.

Stand-Alone Operation

The first falling edge of $\overline{CS}$ starts the operation cycle. Exactly 24 falling clock edges must be applied before $\overline{CS}$ is brought back high again. If $\overline{CS}$ is brought high before the 24th falling SCLK edge, then the data are ignored. If more than 24 falling SCLK edges are applied before $\overline{CS}$ is brought high, then the last 24 bits are considered. The addressed internal register is updated from the Shift Register on the rising edge of $\overline{CS}$. In order for another serial transfer to take place, $\overline{CS}$ must be brought low again.

When the data have been transferred into the chosen register of the addressed DAC, all DAC latches and analog outputs can be updated by taking the $\overline{LDAC}$ pin low or setting the LD bit in the Command Register.

Daisy-Chain Operation

For systems that contain more than one device, the SDO pin can be used to daisy-chain multiple devices together. Daisy-chain operation can be useful in system diagnostics and in reducing the number of serial interface lines. Note that before daisy-chain operation can begin, the SDO pin must be enabled by clearing the SDO disable bit in the Command Register (DSDO = '0'). By default, this bit is cleared after power-on or reset. The first falling edge of $\overline{CS}$ starts the operation cycle. SCLK is continuously applied to the input shift register when $\overline{CS}$ is low. If more than 24 clock pulses are applied, the data ripple out of the shift register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where *N* is the total number of DAC7716s in the chain. When the serial transfer to all devices is complete, $\overline{CS}$ is taken high. This action latches data from the SPI shift register into the device input register of each device in the daisy-chain, and prevents any further data from being clocked in.

Read-Back Operation

The READ command is used to start read-back operation. However, before read-back operation can be initiated, the SDO pin must be enabled by clearing the DSDO bit in the Command Register (DSDO = '0'); this bit is cleared by default. Read-back operation is then started by executing a READ command (R/W bit = '1'; see Table 2). Bits A3 to A0 in the READ command select the register to be read. The remaining data in the command are *don't care* bits. During the next SPI operation, the data that appear on the SDO output are from the previously addressed register. For a read of a single register, a NOP command can be used to clock out the data from the selected register on SDO. Multiple registers can be read if multiple READ commands are issued. The readback diagram in Figure 43 shows the read-back sequence. The read-back data format is the same format as what was used to write to the device.

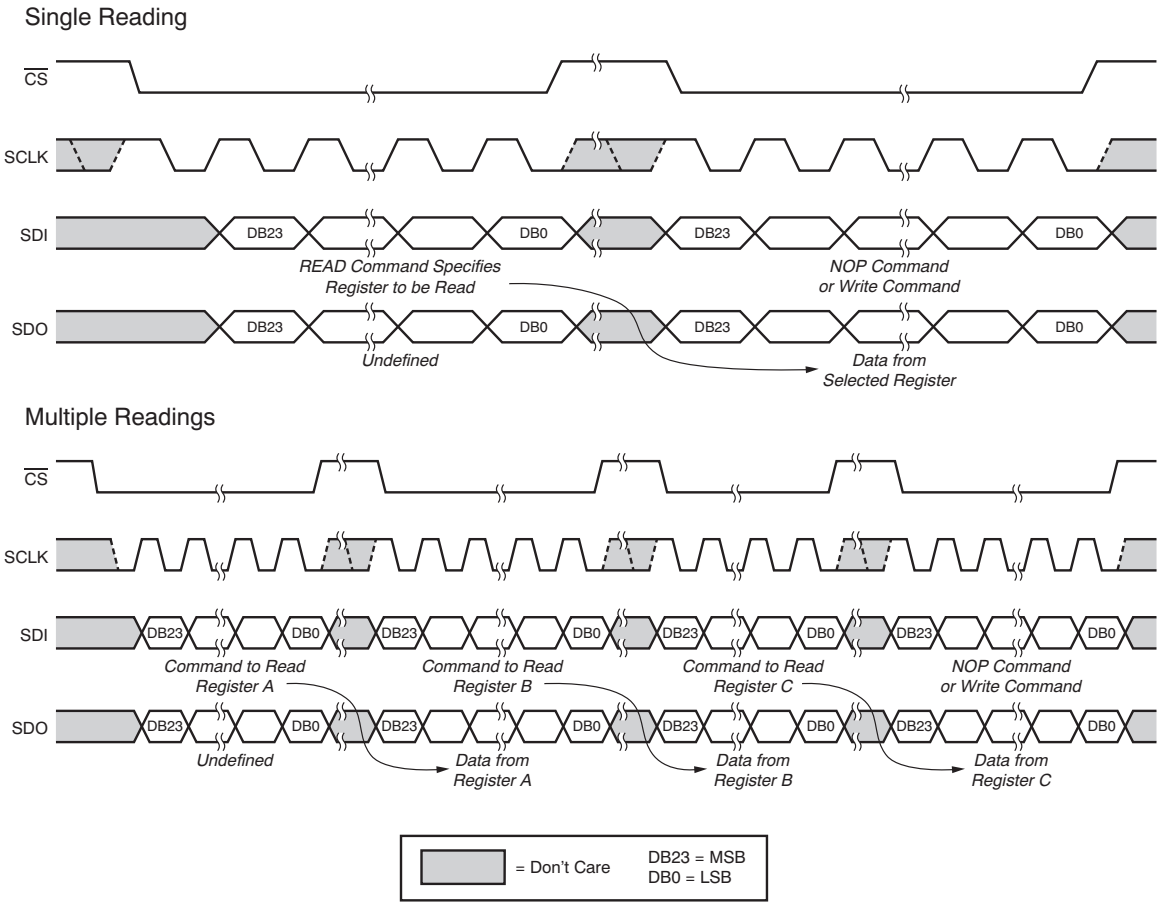


Figure 43. Read-Back Operation

SPI SHIFT REGISTER

The SPI Shift Register is 24 bits wide, as shown in Table 2. By default, the SPI shift register resets to 000000h at power-on or after a reset.

Table 2. SPI Shift Register Format

MSB									
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15:DB4	DB3:DB0
R/$\overline{W}$	0	0	0	A3	A2	A1	A0	DATA	Rsvd(1)

(1) Writing to a reserved bit has no effect; reading the bit returns '0'.

R/$\overline{W}$—Indicates a read from or a write to the addressed register.

R/$\overline{W}$ = '0' sets a write operation and the data are written to the specified register.

R/$\overline{W}$ = '1' sets a read-back operation. For read operation, bits A3 to A0 select the register to be read. The remaining are *don't care* bits. During the next SPI operation, the data appearing on SDO pin are from the previously addressed register.

[A3:A0]—Address bits that specify which register is accessed.

DATA—12 data bits

All DAC7716 registers (command registers and data registers) are 16-bit. Table 3 shows the register map.

Table 3. Register Map

ADDRESS BITS				DATA BITS													REGISTER
A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5: DB4	DB3: DB2	DB1: DB0	
0	0	0	0	A/B	LD	RST	PD-A	PD-B	Rsvd(1)	GPIO-1	GPIO-0	DSDO	NOP	GAIN Bits	GAIN Bits	Rsvd(1)	Command Register
0	0	0	1	MDAC-3	MDAC-2	MDAC-1	MDAC-0	AIN	Reserved(1)								Monitor Register
0	1	0	0	D11:D0											Reserved(1)		DAC-0
0	1	0	1	D11:D0											Reserved(1)		DAC-1
0	1	1	0	D11:D0											Reserved(1)		DAC-2
0	1	1	1	D11:D0											Reserved(1)		DAC-3
1	0	0	0	Reserved(1)							Z8:Z0						Zero Register-0
1	0	0	1	Reserved(1)							Z8:Z0						Zero Register-1
1	0	1	0	Reserved(1)							Z8:Z0						Zero Register-2
1	0	1	1	Reserved(1)							Z8:Z0						Zero Register-3
1	1	0	0	Reserved(1)								G7:G0					Gain Register-0
1	1	0	1	Reserved(1)								G7:G0					Gain Register-1
1	1	1	0	Reserved(1)								G7:G0					Gain Register-2
1	1	1	1	Reserved(1)								G7:G0					Gain Register-3
Others				Reserved(1)													—

(1) Writing to a reserved bit has no effect; reading the bit returns '0'.

INTERNAL REGISTERS

The DAC7716 internal registers consist of the Command Register, the Monitor Register, the DAC Input Data Registers, the Zero Registers, and the Gain Registers.

Command Register. Default = 033Ch.

The Command Register determines the actions performed by the DAC7716.

Table 4. Command Register

BIT	NAME	DEFAULT VALUE	DESCRIPTION
DB15	A/B	0	A/B bit. When A/B = '0', reading DAC-x returns the value in the Input Data Register. When A/B = '1', reading DAC-x returns the value in the DAC latch.
DB14	LD	0	Synchronously update DACs bit. Functions in the same manner as the $\overline{\text{LDAC}}$ pin. When $\overline{\text{LDAC}}$ is tied high, set LD = '1' at any time after the write operation and the correction process proceeds to synchronously update all DAC latches with the content of the corresponding Input Data Register, and sets V_{OUT} to a new level. The DAC7716 updates the DAC latch only if it has been accessed since the last time $\overline{\text{LDAC}}$ was brought low or the LD bit was set to '1', thereby eliminating unnecessary glitch. Any DACs that were not accessed are not reloaded. After updating, the bit returns to '0'. Refer to the *Updating Via $\overline{\text{LDAC}}$* section for details. When the $\overline{\text{LDAC}}$ pin is tied low, the LD bit is ignored.
DB13	RST	0	Software reset bit. Set the RST bit to '1' to reset the device; functions the same as a hardware reset. After reset completes, the RST bit returns to '0'.
DB12	PD-A	0	Power-down bit for Group A. Setting the PD-A bit to '1' places Group A (DAC-0 and DAC-1) into power-down operation. All output buffers are in Hi-Z and all analog outputs (V_{OUT}-x) connect to AGND through an internal 10kΩ resistor. The interface remains active. Setting the PD-A bit to '0' returns Group A to normal operation.
DB11	PD-B	0	Power-down bit for Group B. Setting the PD-B bit to '1' places Group B (DAC-2 and DAC-3) into power-down operation. All output buffers are in Hi-Z and all analog outputs (V_{OUT}-x) connect to AGND through an internal 10kΩ resistor. The interface remains active. Setting the PD-B bit to '0' returns Group B to normal operation.
DB10	Rsvd	0	Reserved. Writing to this bit has no effect; reading this bit returns '0'.
DB9	GPIO-1	1	GPIO-1 status bit. Writing a '1' to the GPIO-1 bit puts the GPIO-1 pin into a Hi-Z state (default). Writing a '0' to the GPIO-1 bit forces the GPIO-1 pin low. When reading this bit, the digital value on the GPIO-1 pin is acquired.
DB8	GPIO-0	1	GPIO-0 status bit. Writing a '1' to the GPIO-0 bit puts the GPIO-1 pin into a Hi-Z state (default). Writing a '0' to the GPIO-0 bit forces the GPIO-1 pin low. When reading this bit, the digital value on the GPIO-0 pin is acquired.
DB7	DSDO	0	Disable SDO bit. Set the DSDO bit to '0' to enable the SDO pin (default). The SDO pin works as a normal SPI output. Set the DSDO bit to '1' to disable the SDO pin. The SDO pin is always in a Hi-Z state regardless of the status of the $\overline{\text{CS}}$ pin is.
DB6	NOP	0	No operation bit. Writing '0' or '1' to this bit has no effect and the bit returns to '0' at the end of the write operation. Reading the bit always returns '0'.
DB5	GAIN-3	1	DAC-3 gain bit. Set the GAIN-3 bit to '1' for a gain = 4. Set the GAIN-3 bit to '0' for a gain = 2.
DB4	GAIN-2	1	DAC-2 gain bit. Set the GAIN-2 bit to '1' for a gain = 4. Set the GAIN-2 bit to '0' for a gain = 2.
DB3	GAIN-1	1	DAC-1 gain bit. Set the GAIN-1 bit to '1' for a gain = 4. Set the GAIN-1 bit to '0' for a gain = 2.
DB2	GAIN-0	1	DAC-0 gain bit. Set the GAIN-0 bit to '1' for a gain = 4. Set the GAIN-0 bit to '0' for a gain = 2.
DB1:DB0	—	0	Reserved. Writing to these bits has no effect; reading these bits returns '0'.

Monitor Register. Default = 0000h.

The Monitor Register selects one of the four DAC outputs or the external signal AIN that is to be monitored through the V_{MON} pin. Only one bit can be set to '1' at a time. When all bits = '0', the monitor is disabled and V_{MON} is placed in a high-impedance state. The default value after power-on or reset is 0000h.

Table 5. Monitor Register

DB15	DB14	DB13	DB12	DB11	DB10:DB0	V_{MON} CONNECTS TO
0	0	0	0	1	Reserved(1)	AIN
0	0	0	1	0	Reserved(1)	DAC-0
0	0	1	0	0	Reserved(1)	DAC-1
0	1	0	0	0	Reserved(1)	DAC-2
1	0	0	0	0	Reserved(1)	DAC-3
0	0	0	0	0	Reserved(1)	Monitor disabled, Hi-Z (default)

(1) Writing to a reserved bit has no effect; reading the bit returns '0'.

Input Data Register for DAC-n (where n = 0, 1, 2, or 3). Default = 0000h.

This register stores the DAC data written to the device. When the data are loaded into the corresponding DAC latch, the DAC output changes to the new level defined by the DAC data. The default value after power-on or reset is 0000h.

For bipolar operation, the input data format is always twos complement. For unipolar operation, the input data format is always straight binary.

Table 6. DAC-n (*n* = 0, 1, 2, or 3) Input Data Register

MSB															LSB
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
D11(1)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Reserved(2)			

(1) D11:D0 are the DAC data bits.
(2) Writing to a reserved bit has no effect; reading the bit returns '0'.

Table 7. DAC Output vs Twos Complement Code for Bipolar Output Operation

TWOS COMPLEMENT CODE (D11:D0)	OUTPUT	DESCRIPTION
0111 1111 1111	+0.5 × Gain × V_{REF} × (2047/2048)	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
0000 0000 0000	+0.5 × Gain × V_{REF} × (048)	+1 LSB
0000 0000 0000	0	Zero
1111 1111 1111	–0.5 × Gain × V_{REF} × (048)	–1 LSB
••• •••	••• •••	••• •••
1000 0000 0000	–0.5 × Gain × V_{REF} × (2048/2048)	–Full-Scale

Table 8. DAC Output vs Straight Binary Code for Unipolar Output Operation

STRAIGHT BINARY CODE (D11:D0)	OUTPUT	DESCRIPTION
1111 1111 1111	Gain × V_{REF} × (4095/4096)	+Full-Scale – 1 LSB
••• •••	••• •••	••• •••
1000 0000 0000	Gain × V_{REF} × (2048/4096)	Full-Scale
0111 1111 1111	Gain × V_{REF} × (2047/4096)	Full-Scale – 1 LSB
••• •••	••• •••	••• •••
0000 0000 0000	0	Zero

Zero Register n (where n = 0, 1, 2, or 3). Default = 0000h.

The Zero Register stores the user-calibration data that are used to eliminate the offset error. The data are nine bits wide, 0.0078 LSB/step, and the total adjustment is typically –2 LSB to +1.9922 LSB, or ±0.0488% of full-scale range. The Zero Register uses a twos complement data format in both bipolar and unipolar modes of operation.

Table 9. Zero Register

DB15:DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reserved(1)	Z8	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0

(1) Writing to a reserved bit has no effect; reading the bit returns '0'.

Z8:Z0—OFFSET BITS	ZERO ADJUSTMENT
011111111	+1.9922 LSB
011111110	+1.9844 LSB
••• ••• •••	••• ••• •••
000000001	+1.00781 LSB
000000000	0 LSB (default)
111111111	–1.00781 LSB
••• ••• •••	••• ••• •••
100000001	–1.9922 LSB
100000000	–2 LSB

Gain Register n (where n = 0, 1, 2, or 3). Default = 0000h.

The Gain Register stores the user-calibration data that are used to eliminate the gain error. The data are eight bits wide, 0.0625 LSB/step, and the total adjustment is typically –8 LSB to +7.9375 LSB, or ±0.195% of full-scale range. The Gain Register uses a twos complement data format in both bipolar and unipolar modes of operation.

Table 10. Gain Register

DB15:DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reserved(1)	G7	G6	G5	G4	G3	G2	G1	G0

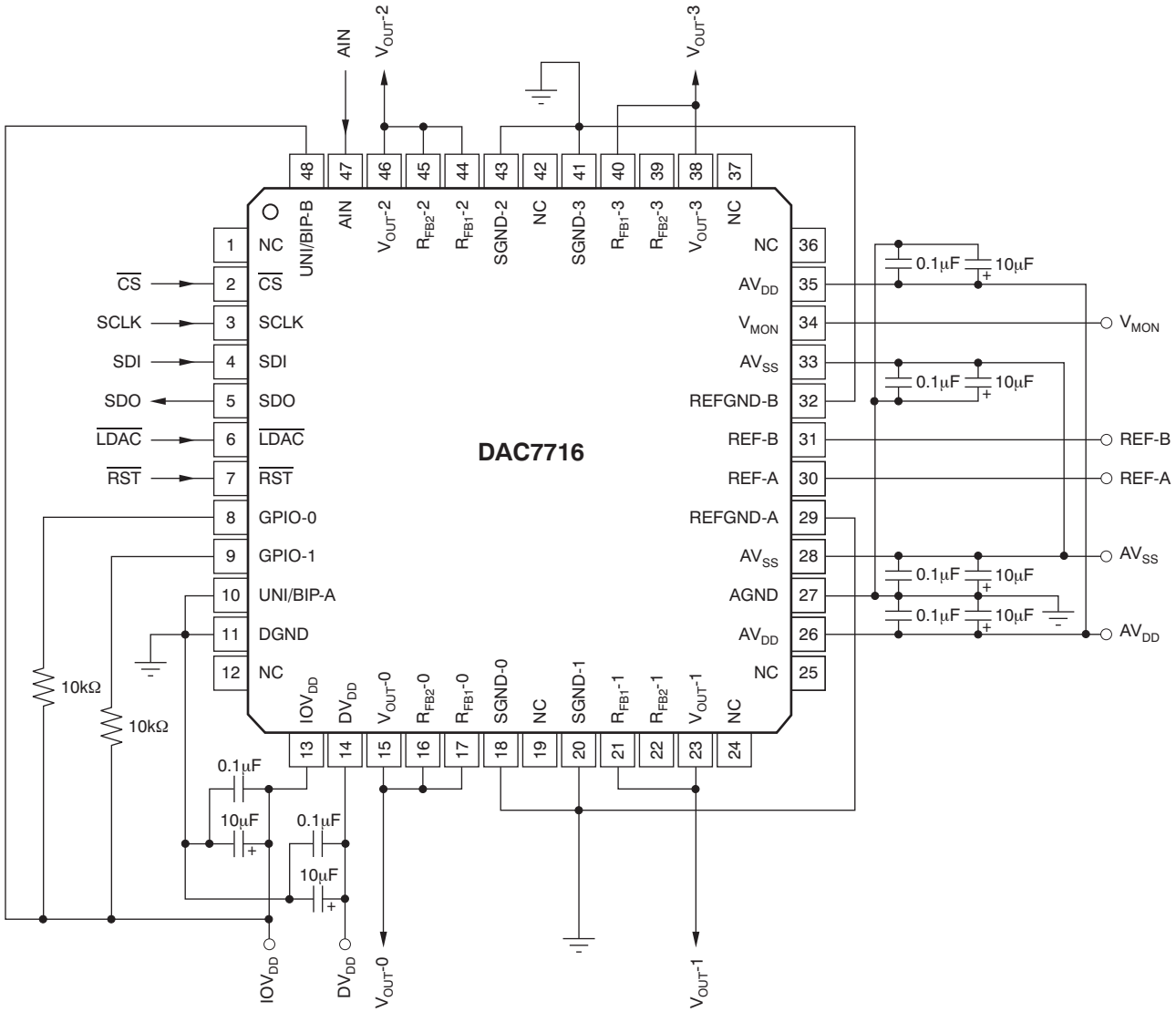
(1) Writing to a reserved bit has no effect; reading the bit returns '0'.

G7:G0—GAIN-CODE BITS	GAIN ADJUSTMENT
01111111	+7.9375 LSB
01111110	+7.875 LSB
••• ••• •••	••• ••• •••
00000001	+0.0625 LSB
00000000	0 LSB (default)
11111111	–0.0625 LSB
••• ••• •••	••• ••• •••
10000001	–7.9375 LSB
10000000	–8 LSB

APPLICATION INFORMATION

BASIC OPERATION

The DAC7716 is a highly-integrated device with high-performance reference buffers and output buffers, greatly reducing the printed circuit board (PCB) area and cost. On-chip reference buffers eliminate the need for a negative external reference. Configurable on-chip output buffers support four different output modes. Figure 44 shows a basic application for the DAC7716.



NOTES: AV_{DD} = +15V, AV_{SS} = –15V, DV_{DD} = +5V, IOV_{DD} = +1.8 to +5V, REF-A = +5V, and REF-B = +2.5V.
The gain bits in the Command Register are: GAIN-0 = '0', GAIN-1 = '1', GAIN-2 = '0', and GAIN-3 = '1'.
The DACs are set to the following gains: DAC-0 = x2, DAC-1 = x4, DAC-2 = x2, and DAC-3 = x4.
The output ranges are: V_{OUT}-0 = –5V to +5V
V_{OUT}-1 = –10V to +10V,
V_{OUT}-2 = 0V to +5V,
V_{OUT}-3 = 0V to +10V.

Figure 44. Basic Application Example

USER ZERO- AND GAIN-CALIBRATION

The DAC7716 is trimmed during production for nominal operating conditions to have very low gain error and offset error. However, to trim the offset and gain errors introduced at other conditions of operation or by other components in the signal chain, the DAC7716 has a user zero and gain digital calibration feature for each DAC channel. Figure 45 and Figure 46 illustrate the relationship of zero and gain calibration for the DAC7716 in unipolar output and bipolar output configurations, respectively.

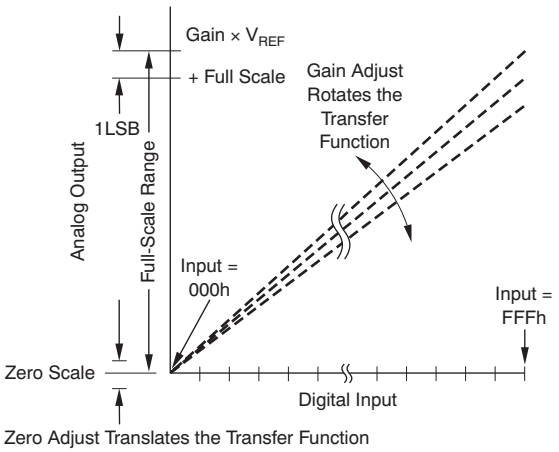


Figure 45. Relationship of Zero and Gain Calibration for a Unipolar Output Configuration

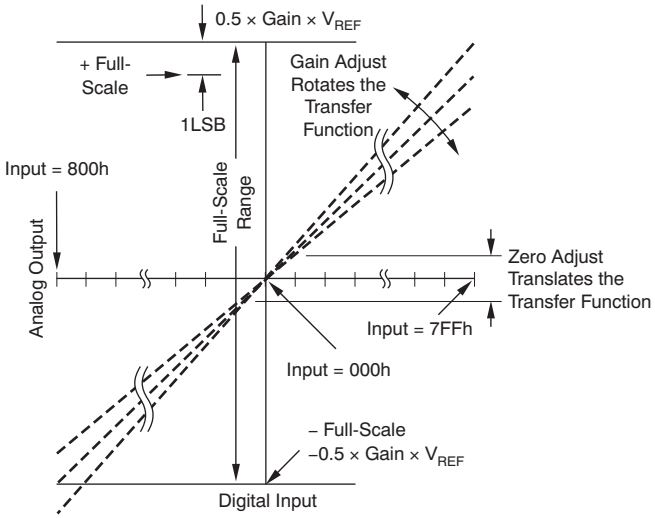


Figure 46. Relationship of Zero and Gain Calibration for a Bipolar Output Configuration

System Zero Adjust Example

The DAC7716 zero calibration feature can minimize system offset errors to 0.00019% FSR or 38µV over a 20V output range. The total adjustment range is approximately ±0.0488% of FSR, or ±9.7mV over a 20V output span.

Assuming that the DAC has been set up with a full-scale range of 20V, and the offset error to be eliminated from the signal chain is –1mV, then the step size = 0.0000019 × 20V = 38µV.

$$\text{Number of Steps of Zero Calibration} = \frac{-1 \times \text{Offset\_Error}}{\text{Step Size}} \quad (3)$$

Where *Offset_Error* is the value of the offset error to be corrected.

For this example, the number of steps of zero calibration = 1mV / 38µV ≈ 26. Therefore, the Zero Register should be coded with the twos complement of 26 = 0 0001 1010.

Suppose the offset error to be eliminated is +1mV instead; then the number of steps of zero calibration is the twos complement equivalent of –26, which is 1 1110 0110.

System Gain Adjust Example

The DAC7716 gain calibration feature can minimize system gain errors to 0.001525% FSR or 305µV over a 20V output range. The total adjustment range is approximately ±0.195% FSR, or –39mV to +38.7mV over a 20V output span.

Assuming that the DAC has been set up with a full-scale range of 20V, and the gain error to be eliminated from the signal chain is –10mV, then the step size = 0.00001525 × 20V = 305µV.

$$\text{Number of Steps of Gain Calibration} = \frac{-1 \times \text{Gain\_Error}}{\text{Step Size}} \quad (4)$$

Where *Gain_Error* is the value of the gain error to be corrected.

For this example, the number of steps of the gain calibration = 10mV/305µV ≈ 33. Therefore, the Gain Register should be coded with the twos complement of 33 = 0010 0001.

Suppose the gain error to be eliminated is +10mV instead; then the number of steps of Gain calibration is the twos complement equivalent of –33, which is 1101 1111.

LAYOUT AND GROUNDING

Precision analog circuits require careful layout, adequate bypass capacitors, and a clean, well-regulated power supply to obtain the best possible dc and ac performance. A careful consideration of the power-supply and ground-return layout helps to ensure the rated performance.

The PCB must be designed so that the analog and digital sections are separated and confined to certain areas of the board. Fast switching signals, such as clocks, must be shielded with the digital ground to avoid radiating noise to other sections of the board, and must never be run near the reference inputs. It is essential to minimize noise on the reference inputs because it couples through to the DAC output. Avoid crossover of digital and analog signals. Traces on opposite sides of the board must run at right angles to each other. This configuration reduces the effects of feedthrough on the board. A microstrip technique may be considered, but may not always be possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side.

DGND is the return path for digital currents and AGND is the analog power ground for the DAC. For the best ac performance, care should be taken to connect DGND and AGND with very low resistance back to the supply ground. If multiple devices require an AGND-to-DGND connection, the connection must be made at one point only. The star ground point must be established as close as possible to the device. Each DAC has a ground pin (SGND-x) that must be connected directly to the corresponding reference ground in low-impedance paths to achieve the best performance. SGND-0 and SGND-1 must be connected with REFGND-A, and SGND-2 and SGND-3 must be connected with REFGND-B. It is critical that this trace resistance be extremely small in order to prevent the voltage drops across the path from affecting device linearity and gain performance. The reference ground pins, REFGND-A and REFGND-B, must be connected to analog ground AGND.

POWER-SUPPLY NOISE

The DAC7716 should have ample supply bypassing of 1µF to 10µF in parallel with 0.1µF on each supply, located as close to the package as possible; ideally, placed next to the device. The 1µF to 10µF capacitors must be a tantalum-bead type. The 0.1µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as common ceramic types that provide a low-impedance path to ground at high frequencies to handle transient currents because of internal logic switching. The power-supply lines must use traces as wide as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line. Apart from these considerations, the wideband noise on the AV_{DD}, AV_{SS}, DV_{DD}, and IOV_{DD} supplies should be filtered before being fed to the DAC in order to obtain the best noise performance possible.

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the DAC7716 over its full operating temperature range, a precision voltage reference must be used. Consideration should be given to the selection of a precision voltage reference. The DAC7716 has two reference inputs, REF-A and REF-B. The voltages applied to the reference inputs are used to provide a buffered positive and negative reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device. There are four possible sources of error to consider when choosing a voltage reference for high-accuracy applications: initial accuracy, temperature coefficient of the output voltage, long-term drift, and output voltage noise. Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with a low initial accuracy error specification is preferred. Long-term drift is a measurement of how much the reference output voltage drifts over time. A reference with a tight, long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime. The temperature coefficient of a reference output voltage affects INL, DNL, gain error, and zero error. Choose a reference with a tight temperature coefficient specification to reduce the dependence of the DAC output voltage on ambient conditions. In high-accuracy applications that have a relatively low noise budget, reference output voltage noise must be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the TI REF50xx (2V to 5V) and REF32xx (1.25V to 4V), provide low-drift and high-accuracy reference voltage.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7716SPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SPFBG4.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716
DAC7716SRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC7716

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

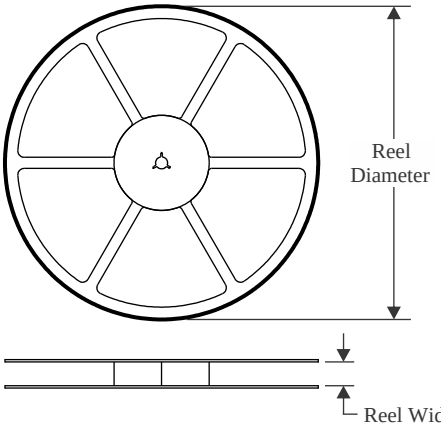
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

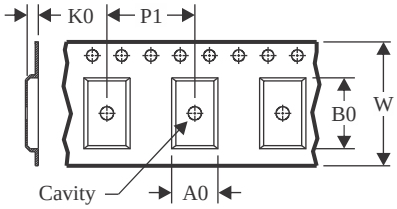
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

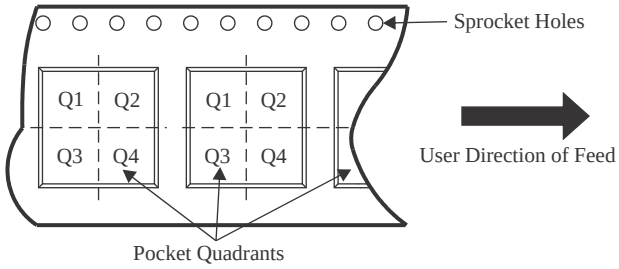


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

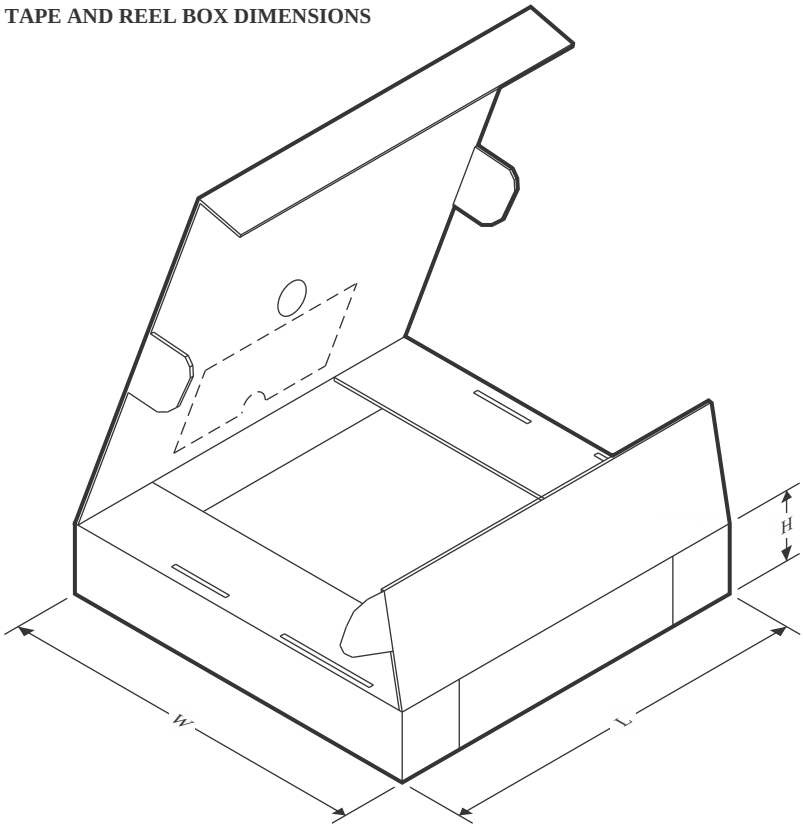
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7716SPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DAC7716SRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

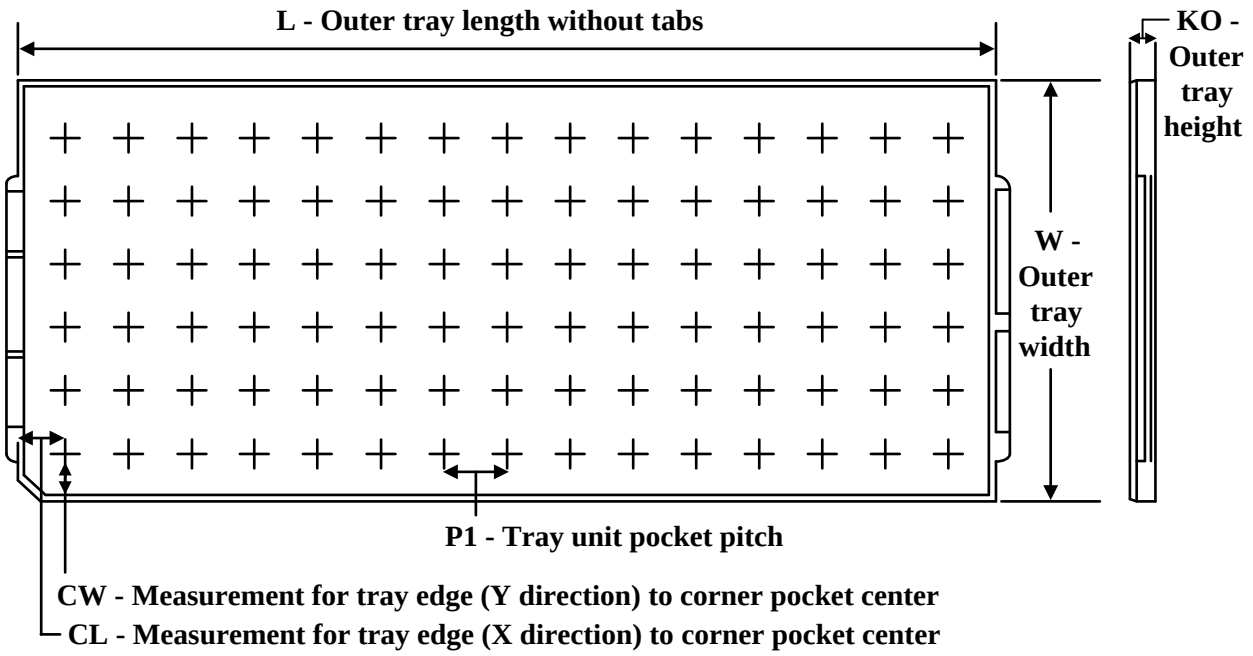
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7716SPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
DAC7716SRHAR	VQFN	RHA	40	2500	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC7716SPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DAC7716SPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DAC7716SPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DAC7716SPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

GENERIC PACKAGE VIEW

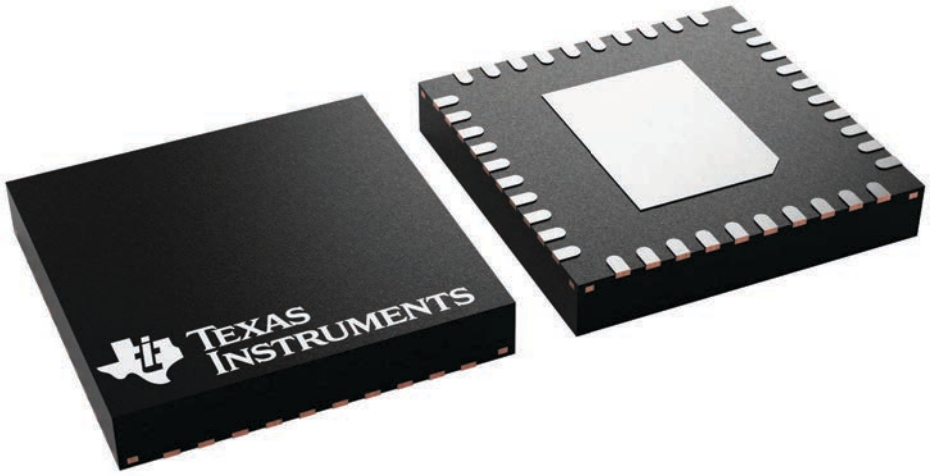
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



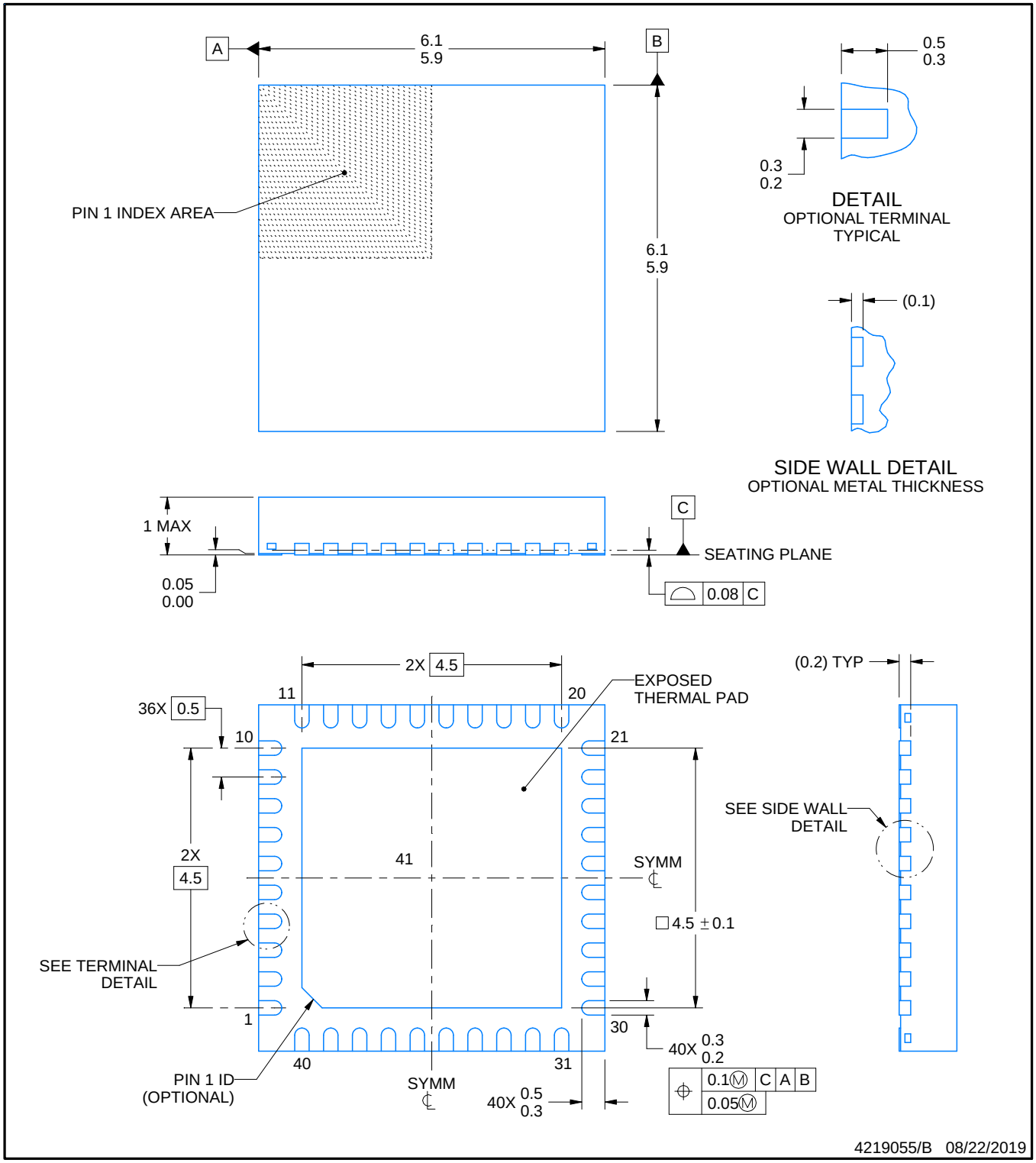
4225870/A

PACKAGE OUTLINE

RHA0040H

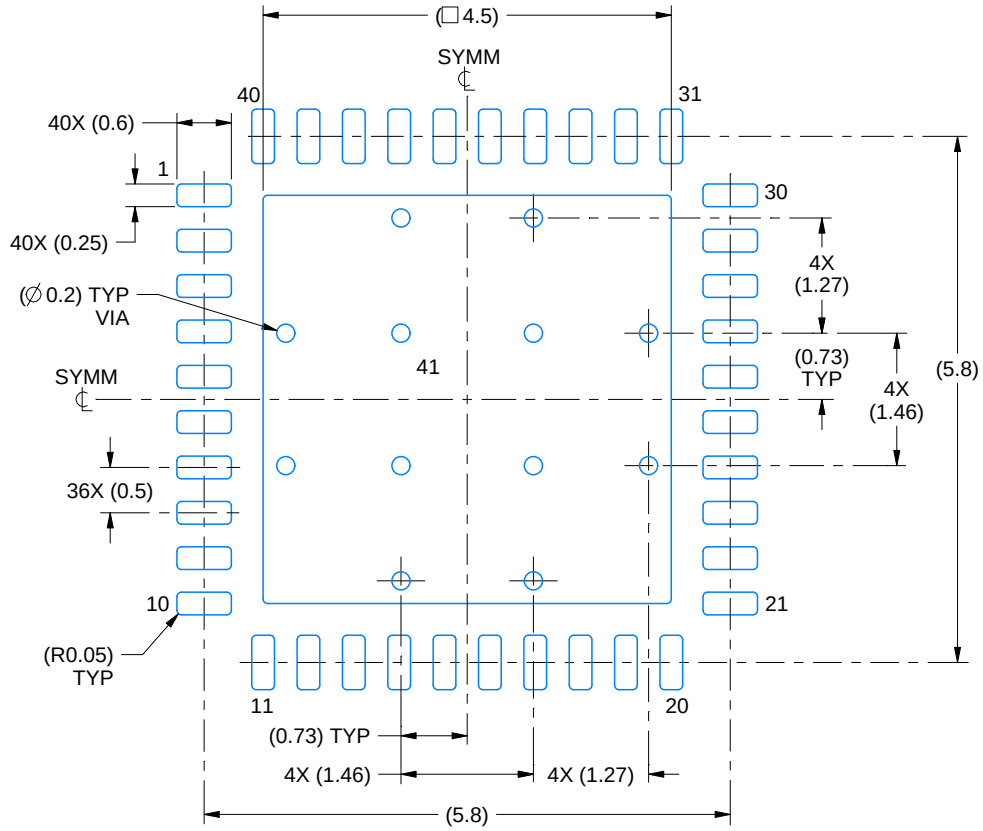
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

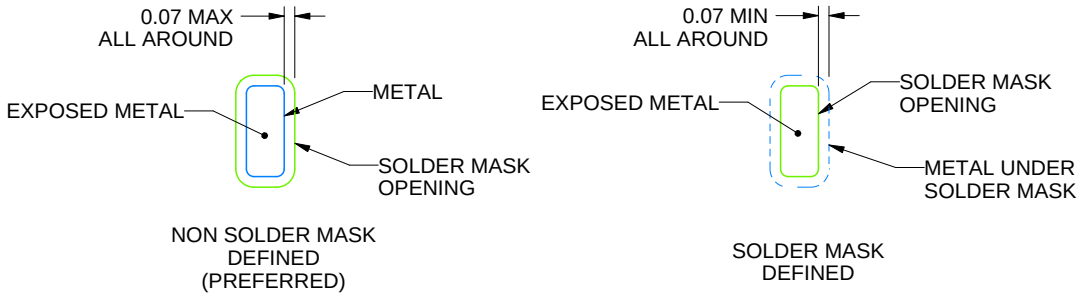


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

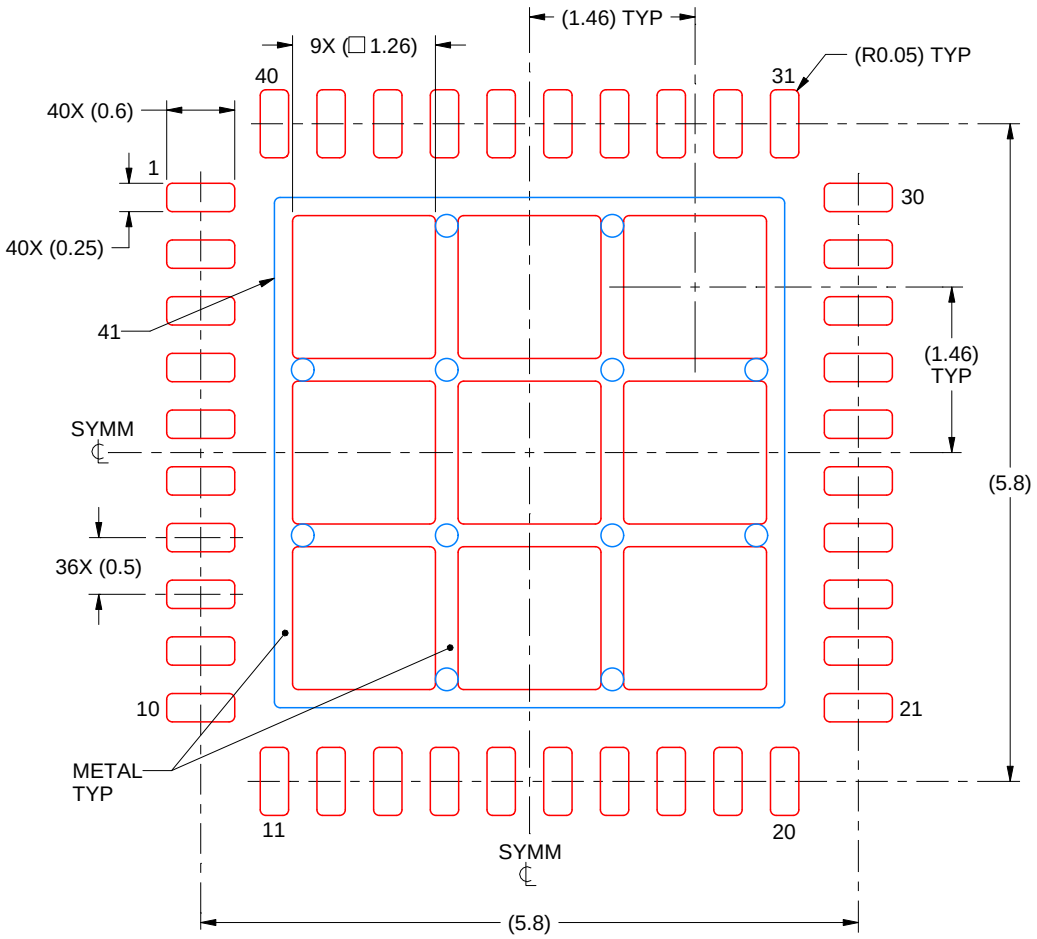


SOLDER MASK DETAILS

4219055/B 08/22/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
70% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219055/B 08/22/2019

NOTES: (continued)

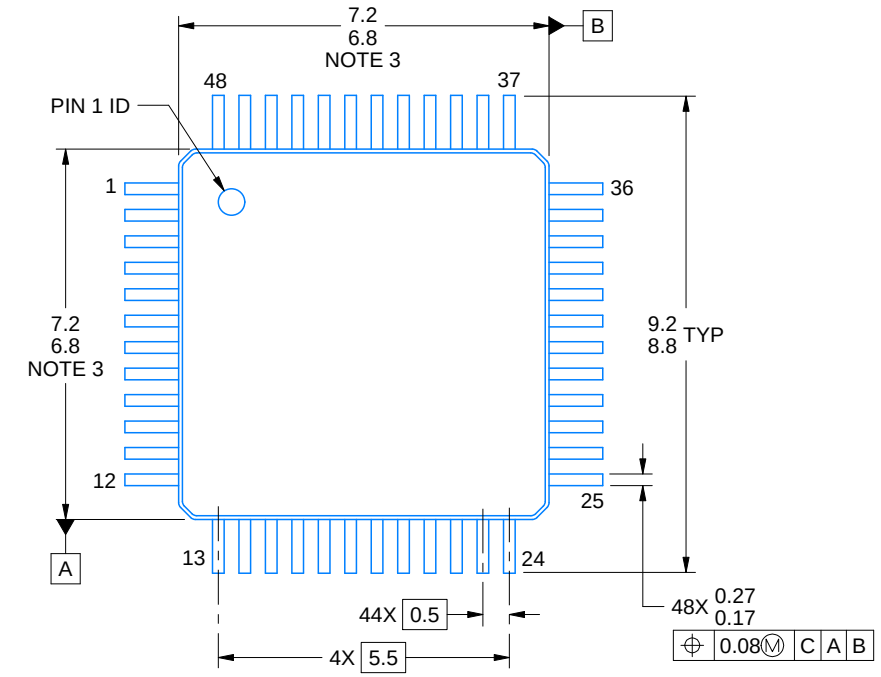
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

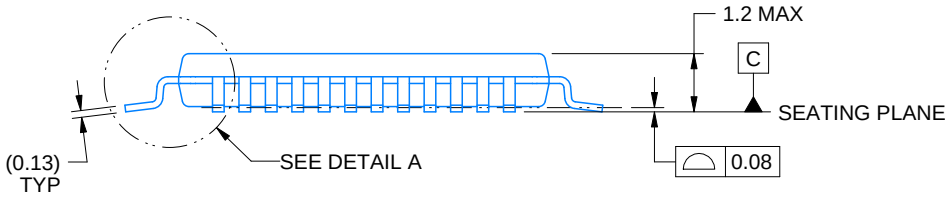
PACKAGE OUTLINE

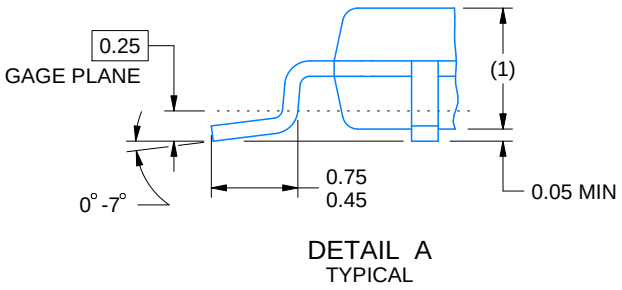
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK





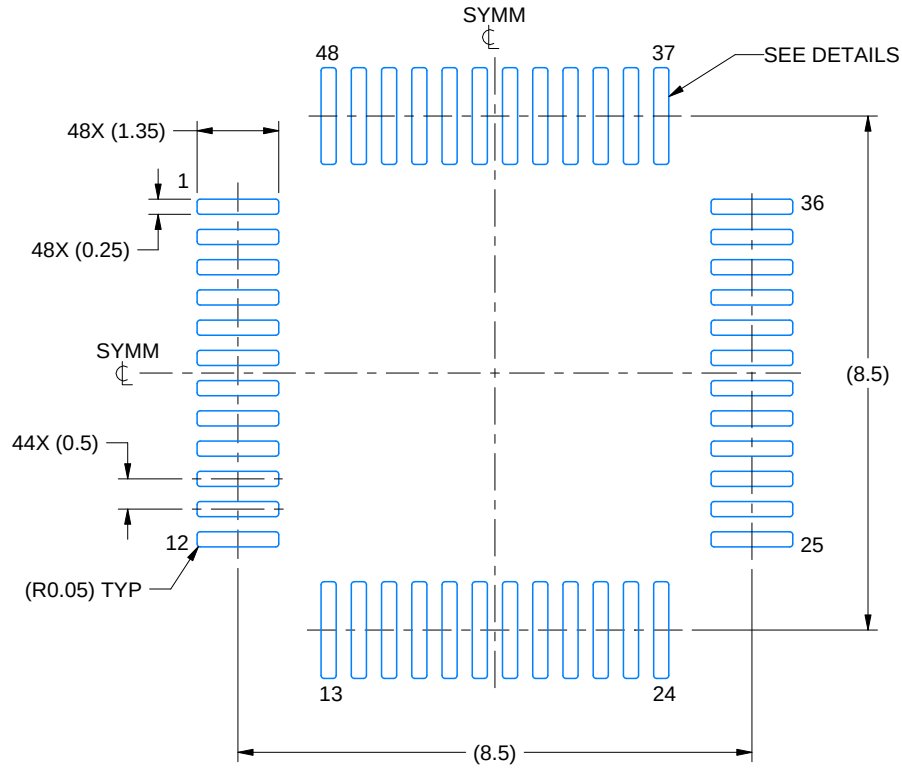


DETAIL A
TYPICAL

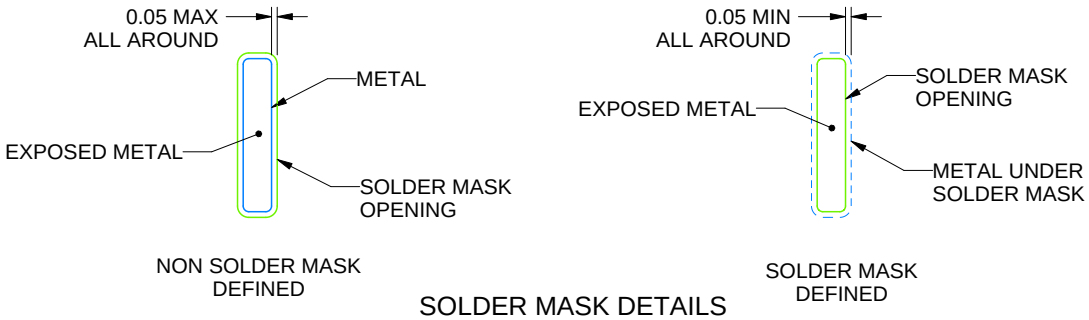
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

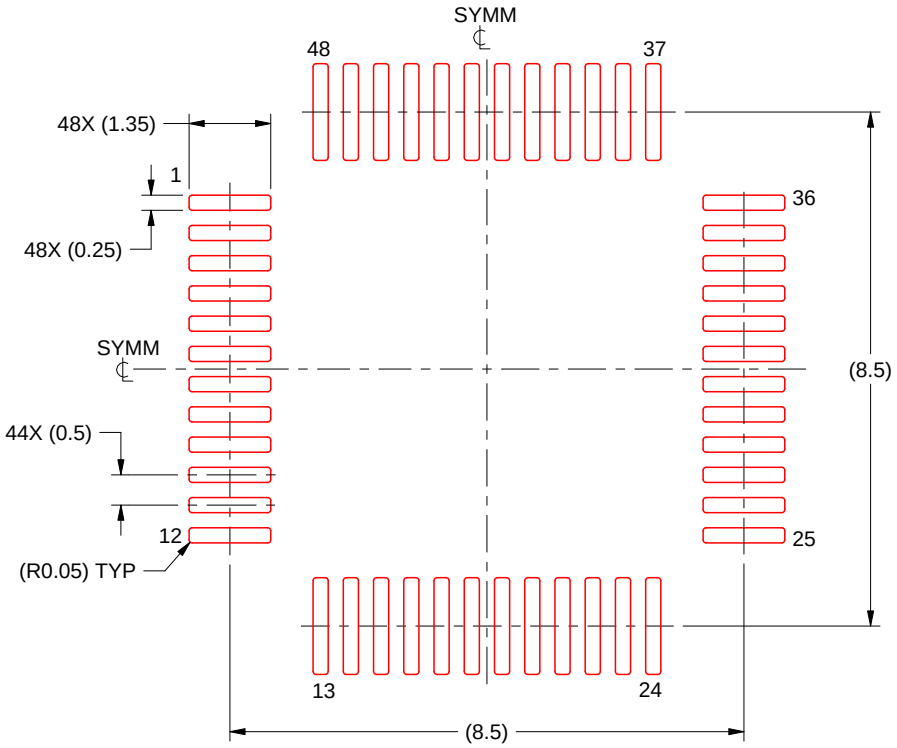


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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