

DLP651NE 0.65-Inch 1080p Digital Micromirror Device

1 Features

- The 0.65-inch diagonal micromirror array
 - 1080p (1920 × 1080) display resolution
 - 7.6 μ m micromirror pitch
 - $\pm 12^\circ$ micromirror tilt (relative to a flat surface)
 - Corner illumination
- High-speed serial interface (HSSI) input data bus
- Supports 1080p (Full HD) at up to 240Hz
- Laser-phosphor, LED, RGB laser, and lamp operation supported by [DLPC7530](#) display controller, [DLPA100](#) power management, and motor driver IC

2 Applications

- [Laser TVs](#)
- [Smart Projectors](#)
- [Enterprise Projectors](#)

3 Description

The DLP651NE digital micromirror device (DMD) is a digitally controlled micro-electromechanical system (MEMS) spatial light modulator (SLM) that enables bright 1080p display systems. The DLP® Products 0.65-inch 1080p chipset is composed of the DMD, [DLPC7530](#) display controller, and [DLPA100](#) power and motor driver. The compact physical size of the chipset provides a complete system solution that enables a small form factor 1080p displays.

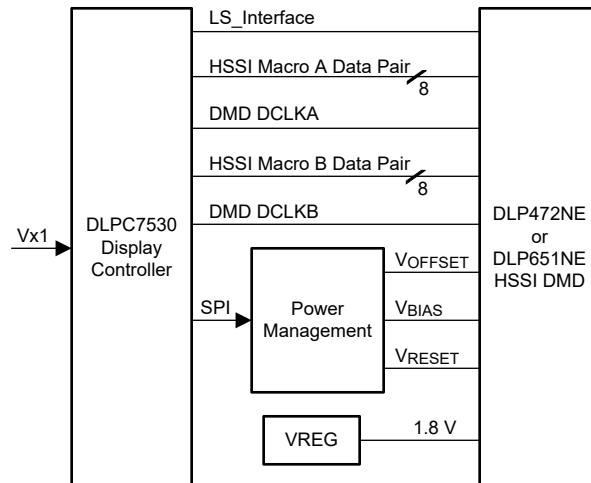
The DMD ecosystem includes established resources to help the user accelerate the design cycle, visit the [DLP® Products third-party search tools](#) to find approved optical module manufacturers and third-party providers.

Visit [Getting Started With TI DLP Display Technology](#) to learn more about how to start designing with the DMD.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE |
|-------------|------------------------|-----------------|
| DLP651NE | FYP(149) | 32.2mm × 22.3mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 Features | 1 | 7 Application and Implementation | 30 |
| 2 Applications | 1 | 7.1 Application Information..... | 30 |
| 3 Description | 1 | 7.2 Typical Application..... | 30 |
| 4 Pin Configuration and Functions | 3 | 7.3 Temperature Sensor Diode..... | 32 |
| 5 Specifications | 6 | 8 Power Supply Recommendations | 33 |
| 5.1 Absolute Maximum Ratings..... | 6 | 8.1 Power Supply Sequence Requirements..... | 33 |
| 5.2 Storage Conditions..... | 6 | 8.2 DMD Power Supply Power-Up Procedure..... | 33 |
| 5.3 ESD Ratings..... | 7 | 8.3 DMD Power Supply Power-Down Procedure..... | 33 |
| 5.4 Recommended Operating Conditions..... | 7 | 9 Layout | 35 |
| 5.5 Thermal Information..... | 9 | 9.1 Layout Guidelines..... | 35 |
| 5.6 Electrical Characteristics..... | 10 | 9.2 Impedance Requirements..... | 35 |
| 5.7 Switching Characteristics..... | 11 | 9.3 Layers..... | 35 |
| 5.8 Timing Requirements..... | 11 | 9.4 Trace Width, Spacing..... | 36 |
| 5.9 System Mounting Interface Loads..... | 15 | 9.5 Power..... | 36 |
| 5.10 Micromirror Array Physical Characteristics..... | 16 | 9.6 Trace Length Matching Recommendations..... | 36 |
| 5.11 Micromirror Array Optical Characteristics..... | 18 | 10 Device and Documentation Support | 38 |
| 5.12 Window Characteristics..... | 19 | 10.1 Third-Party Products Disclaimer..... | 38 |
| 5.13 Chipset Component Usage Specification..... | 19 | 10.2 Device Support..... | 38 |
| 6 Detailed Description | 20 | 10.3 Documentation Support..... | 38 |
| 6.1 Overview..... | 20 | 10.4 Receiving Notification of Documentation Updates..... | 39 |
| 6.2 Functional Block Diagram..... | 21 | 10.5 Support Resources..... | 39 |
| 6.3 Feature Description..... | 22 | 10.6 Trademarks..... | 39 |
| 6.4 Device Functional Modes..... | 22 | 10.7 Electrostatic Discharge Caution..... | 39 |
| 6.5 Optical Interface and System Image Quality Considerations..... | 22 | 10.8 Glossary..... | 39 |
| 6.6 Micromirror Array Temperature Calculation..... | 23 | 11 Revision History | 39 |
| 6.7 Micromirror Power Density Calculation..... | 24 | 12 Mechanical, Packaging, and Orderable Information | 40 |
| 6.8 Window Aperture Illumination Overfill Calculation.... | 26 | 12.1 Package Option Addendum..... | 41 |
| 6.9 Micromirror Landed-On/Landed-Off Duty Cycle..... | 27 | | |

4 Pin Configuration and Functions

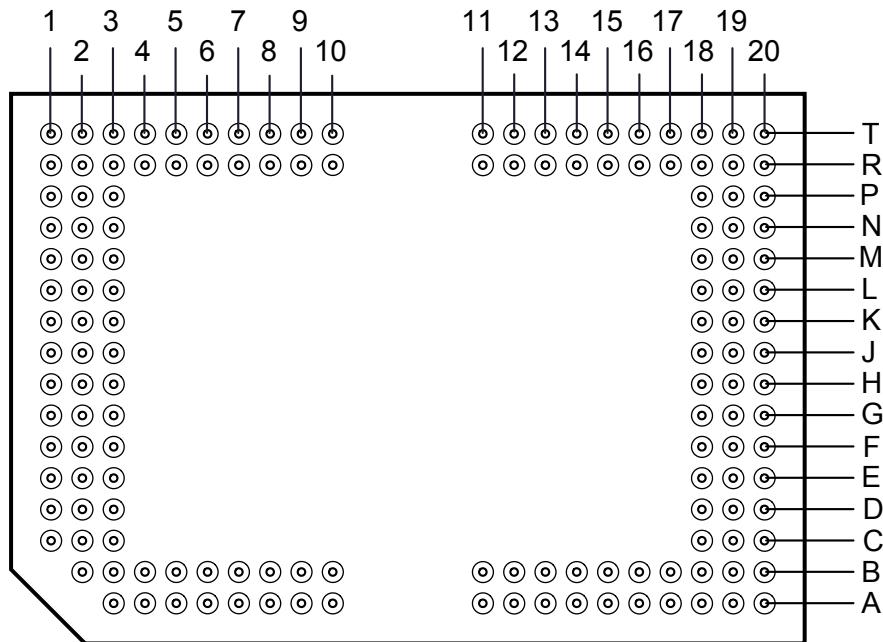


Figure 4-1. FYP Package 149-Pin CPGA Bottom View

Table 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | TRACE LENGTH (mm) |
|---------|--------|---------------------|---|-------------------|
| NAME | PAD ID | | | |
| D_AP(0) | J1 | I | High-speed differential data pair lane A0 | 18.09088 |
| D_AN(0) | H1 | I | High-speed differential data pair lane A0 | 18.0916 |
| D_AP(1) | G1 | I | High-speed differential data pair lane A1 | 18.11696 |
| D_AN(1) | F1 | I | High-speed differential data pair lane A1 | 18.11641 |
| D_AP(2) | A3 | I | High-speed differential data pair lane A2 | 11.11822 |
| D_AN(2) | A4 | I | High-speed differential data pair lane A2 | 11.11745 |
| D_AP(3) | D2 | I | High-speed differential data pair lane A3 | 12.04461 |
| D_AN(3) | C2 | I | High-speed differential data pair lane A3 | 12.04491 |
| D_AP(4) | F2 | I | High-speed differential data pair lane A4 | 15.1345 |
| D_AN(4) | E2 | I | High-speed differential data pair lane A4 | 15.13457 |
| D_AP(5) | A5 | I | High-speed differential data pair lane A5 | 12.80888 |
| D_AN(5) | A6 | I | High-speed differential data pair lane A5 | 12.80825 |
| D_AP(6) | A7 | I | High-speed differential data pair lane A6 | 6.34763 |
| D_AN(6) | A8 | I | High-speed differential data pair lane A6 | 6.34706 |
| D_AP(7) | A9 | I | High-speed differential data pair lane A7 | 4.45653 |
| D_AN(7) | A10 | I | High-speed differential data pair lane A7 | 4.45875 |
| DCLK_AP | C1 | I | High-speed differential clock A | 15.08029 |
| DCLK_AN | D1 | I | High-speed differential clock A | 15.07977 |
| D_BP(0) | A11 | I | High-speed differential data pair lane B0 | 4.06642 |
| D_BN(0) | A12 | I | High-speed differential data pair lane B0 | 4.06697 |
| D_BP(1) | A13 | I | High-speed differential data pair lane B1 | 6.42676 |

Table 4-1. Pin Functions (continued)

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | TRACE LENGTH (mm) |
|------------------|---|---------------------|--|-------------------|
| NAME | PAD ID | | | |
| D_BN(1) | A14 | I | High-speed differential data pair lane B1 | 6.42716 |
| D_BP(2) | A15 | I | High-speed differential data pair lane B2 | 11.90485 |
| D_BN(2) | A16 | I | High-speed differential data pair lane B2 | 11.90509 |
| D_BP(3) | A18 | I | High-speed differential data pair lane B3 | 13.80223 |
| D_BN(3) | A19 | I | High-speed differential data pair lane B3 | 13.80269 |
| D_BP(4) | D19 | I | High-speed differential data pair lane B4 | 12.45294 |
| D_BN(4) | C19 | I | High-speed differential data pair lane B4 | 12.45252 |
| D_BP(5) | H20 | I | High-speed differential data pair lane B5 | 15.7909 |
| D_BN(5) | J20 | I | High-speed differential data pair lane B5 | 15.79026 |
| D_BP(6) | D20 | I | High-speed differential data pair lane B6 | 11.02899 |
| D_BN(6) | E20 | I | High-speed differential data pair lane B6 | 11.02947 |
| D_BP(7) | F20 | I | High-speed differential data pair lane B7 | 14.7517 |
| D_BN(7) | G20 | I | High-speed differential data pair lane B7 | 14.75085 |
| DCLK_BP | B17 | I | High-speed differential clock B | 9.17864 |
| DCLK_BN | B18 | I | High-speed differential clock B | 9.17821 |
| LS_WDATA_P | T10 | I | LVDS Data | 11.27905 |
| LS_WDATA_N | R11 | I | LVDS Data | 6.76474 |
| LS_CLK_P | R9 | I | LVDS CLK | 13.5461 |
| LS_CLK_N | R10 | I | LVDS CLK | 12.56934 |
| LS_RDATA_A_BISTA | T13 | O | LVC MOS Output | 3.12045 |
| BIST_B | T12 | O | LVC MOS Output | 5.63628 |
| AMUX_OUT | B20 | O | Analog Test Mux | 9.3849 |
| DMUX_OUT | R14 | O | Digital Test Mux | 3.85333 |
| DMD_DEN_ARSTZ | T11 | I | ARSTZ | 5.86593 |
| TEMP_N | R8 | I | Temp Diode N | 14.63792 |
| TEMP_P | R7 | I | Temp Diode P | 15.93219 |
| VDD | B7, B13, C18, E3, H3, J2, K3, L2, L19, M1, M2, N3, N19, P2, P18, R3, R5, R12, R17, R19, T2, T4, T6, T8, T18 | P | Digital core supply voltage | Plane |
| VDDA | B4, B9, B11, B16, C20, D3, E18, G2, G19 | P | HSSI supply voltage | Plane |
| VRESET | B3, R1 | P | Supply voltage for negative bias of micromirror reset signal | Plane |
| VBIAS | E1, P1 | P | Supply voltage for positive bias of micromirror reset signal | Plane |
| VOFFSET | A20, B2, T1, T20 | P | Supply voltage for HVC MOS logic, stepped up logic level | Plane |

Table 4-1. Pin Functions (continued)

| PIN | | TYPE ⁽¹⁾ | PIN DESCRIPTION | TRACE LENGTH (mm) |
|------|--|---------------------|-----------------|-------------------|
| NAME | PAD ID | | | |
| VSS | A17, B6, B10, B14, D18, F3, F19, J3, K2, K19, L1, L3, M3, N2, N18, N20, P3, P20, R2, R4, R6, R13, R20, T5, T7, T16, T17, T19 | G | Ground | Plane |
| VSSA | B5, B8, B12, B15, B19, C3, E19, G3, H2, H19, K1, N1, P19, R18, T3, T9 | G | Ground | Plane |
| N/C | R15, T14, T15, R16, H18, J18, G18, J19, F18, K20, K18, M19, L20, M18, L18, M20 | | No connect | |

(1) I=Input, O=Output, P=Power, G=Ground, NC = No connect

5 Specifications

5.1 Absolute Maximum Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

| PARAMETER NAME | DESCRIPTION | MIN | MAX | UNIT |
|---|---|------|-----------|------|
| Supply Voltage | | | | |
| V_{DD} | Supply voltage for LVC MOS core logic and LVC MOS low speed interface (LSIF) ⁽¹⁾ | -0.5 | 2.3 | V |
| V_{DDA} | Supply voltage for high speed serial interface (HSSI) receivers ⁽¹⁾ | -0.3 | 2.2 | V |
| V_{OFFSET} | Supply voltage for HVC MOS and micromirror electrode ^{(1) (2)} | -0.5 | 11 | V |
| V_{BIAS} | Supply voltage for micromirror electrode ⁽¹⁾ | -0.5 | 17 | V |
| V_{RESET} | Supply voltage for micromirror electrode ⁽¹⁾ | -13 | 0.5 | V |
| $ V_{DDA} - V_{DD} $ | Supply voltage delta (absolute value) ⁽³⁾ | | 0.3 | V |
| $ V_{BIAS} - V_{OFFSET} $ | Supply voltage delta (absolute value) ⁽⁴⁾ | | 11 | V |
| $ V_{BIAS} - V_{RESET} $ | Supply voltage delta (absolute value) ⁽⁵⁾ | | 30 | V |
| Input Voltage | | | | |
| | Input voltage for other inputs – LSIF and LVC MOS ⁽¹⁾ | -0.5 | 2.45 | V |
| | Input voltage for other inputs – HSSI ^{(1) (6)} | -0.2 | V_{DDA} | V |
| Low speed interface (LSIF) | | | | |
| f_{CLOCK} | LSIF clock frequency (LS_CLK) | | 130 | MHz |
| $ V_{ID} $ | LSIF differential input voltage magnitude ⁽⁶⁾ | | 810 | mV |
| I_{ID} | LSIF differential input current ⁽⁷⁾ | | 10 | mA |
| High speed serial interface (HSSI) | | | | |
| f_{CLOCK} | HSSI clock frequency (DCLK) | | 1.65 | GHz |
| $ V_{ID} $ | HSSI differential input voltage magnitude Data Lane ⁽⁶⁾ | | 700 | mV |
| $ V_{ID} $ | HSSI differential input voltage magnitude Clock Lane ⁽⁶⁾ | | 700 | mV |
| Environmental | | | | |
| T_{ARRAY} | Temperature, operating ⁽⁸⁾ | 0 | 90 | °C |
| T_{ARRAY} | Temperature, non-operating ⁽⁸⁾ | -40 | 90 | °C |
| T_{DP} | Dew point temperature, operating and non-operating (non-condensing) | | 81 | °C |

- (1) All voltage values are with respect to the ground terminals (V_{SS}). The following required power supplies must be connected for proper DMD operation: V_{DD} , V_{DDA} , V_{OFFSET} , V_{BIAS} , and V_{RESET} . All V_{SS} connections are also required.
- (2) V_{OFFSET} supply transients must fall within specified voltages.
- (3) Exceeding the recommended allowable absolute voltage difference between V_{DDA} and V_{DD} may result in excessive current draw.
- (4) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
- (5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
- (6) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS and HSSI differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (7) Differential inputs must not exceed the specified limit or damage may result to the internal termination resistors. Specification applies to both the High speed serial interface (HSSI) and the low speed interface (LSI).
- (8) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) in the package thermal resistances using the *Micromirror Array Temperature Calculation*.

5.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------|---|-----|-----|------|
| T_{DMD} | DMD storage temperature | -40 | 80 | °C |
| T_{DP-AVG} | Average dew point temperature (non-condensing) ⁽¹⁾ | | 28 | °C |

5.2 Storage Conditions (continued)

Applicable for the DMD as a component or non-operating in a system.

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|--------------|--|-----|-----|--------|
| T_{DP-ELR} | Elevated dew point temperature range (non-condensing) ⁽²⁾ | 28 | 36 | °C |
| CT_{ELR} | Cumulative time in the elevated dew point temperature range | | 24 | Months |

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.

(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR} .

5.3 ESD Ratings

| SYMBOL | PARAMETER | DESCRIPTION | VALUE | UNIT |
|-------------|-------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| $V_{(ESD)}$ | Electrostatic discharge | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | V |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

Over operating free-air temperature range and supply voltages (unless otherwise noted) ⁽¹⁾

| PARAMETER NAME | | MIN | NOM | MAX | UNIT |
|---|---|---------------------|-----|-------|------|
| Supply Voltages^{(2) (3)} | | | | | |
| V_{DD} | Supply voltage for LVCMOS core logic and low speed interface (LSIF) | 1.71 | 1.8 | 1.95 | V |
| V_{DDA} | Supply voltage for high speed serial interface (HSSI) receivers | 1.71 | 1.8 | 1.95 | V |
| V_{OFFSET} | Supply voltage for HVCmos and micromirror electrode ⁽⁴⁾ | 9.5 | 10 | 10.5 | V |
| V_{BIAS} | Supply voltage for micromirror electrode | 15.5 | 16 | 16.5 | V |
| V_{RESET} | Supply voltage for micromirror electrode | -12.5 | -12 | -11.5 | V |
| $ V_{DDA} - V_{DD} $ | Supply voltage delta, absolute value ⁽⁵⁾ | | | 0.3 | V |
| $ V_{BIAS} - V_{OFFSET} $ | Supply voltage delta, absolute value ⁽⁶⁾ | | | 10.5 | V |
| $ V_{BIAS} - V_{RESET} $ | Supply voltage delta, absolute value | | | 29 | V |
| LVCMOS Input | | | | | |
| V_{IH} | High level input voltage ⁽⁷⁾ | $0.7 \times V_{DD}$ | | | V |
| V_{IL} | Low level input voltage ⁽⁷⁾ | $0.3 \times V_{DD}$ | | | V |
| Low Speed Interface (LSIF) | | | | | |
| f_{CLOCK} | LSIF clock frequency (LS_CLK) ⁽⁸⁾ | 108 | 120 | 130 | MHz |
| DCD_{IN} | LSIF duty cycle distortion (LS_CLK) | 44% | | 56% | |
| $ V_{ID} $ | LSIF differential input voltage magnitude ⁽⁸⁾ | 150 | 350 | 440 | mV |
| V_{LVDS} | LSIF voltage ⁽⁸⁾ | 575 | | 1520 | mV |
| V_{CM} | Common mode voltage ⁽⁸⁾ | 700 | 900 | 1300 | mV |
| Z_{LINE} | Line differential impedance (PWB/trace) | 90 | 100 | 110 | Ω |
| Z_{IN} | Internal differential termination resistance | 80 | 100 | 120 | Ω |
| High Speed Serial Interface (HSSI) | | | | | |
| f_{CLOCK} | HSSI clock frequency (DCLK) ⁽⁹⁾ | 1.2 | | 1.6 | GHz |
| DCD_{IN} | HSSI duty cycle distortion (DCLK) | 44% | 50% | 56% | |
| $ V_{ID} $ Data | HSSI differential input voltage magnitude Data Lane ⁽⁹⁾ | 100 | | 600 | mV |
| $ V_{ID} $ CLK | HSSI differential input voltage magnitude Clock Lane ⁽⁹⁾ | 295 | | 600 | mV |

5.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted) ⁽¹⁾

| PARAMETER NAME | | MIN | NOM | MAX | UNIT |
|-----------------------------------|--|------|----------|-----|--------------------|
| V _{CM_{DC}} Data | Input common mode voltage (DC) Data Lane ⁽⁹⁾ | 200 | 600 | 800 | mV |
| V _{CM_{DC}} CLK | Input common mode voltage (DC) Clk Lane ⁽⁹⁾ | 200 | 600 | 800 | mV |
| V _{CM_{ACP-P}} | AC peak to peak (ripple) on common mode voltage of Data Lane and Clock Lane ⁽⁹⁾ | | | 100 | mV |
| Z _{LINE} | Line differential impedance (PWB/trace) | | 100 | | Ω |
| Z _{IN} | Internal differential termination resistance (R _{XTERM}) | 80 | 100 | 120 | Ω |
| Environmental | | | | | |
| T _{ARRAY} | Array temperature, long-term operational ^{(10) (11) (12) (13)} | 10 | 40 to 70 | | °C |
| | Array temperature, short-term operational, 500hr max ^{(11) (14)} | 0 | 10 | | °C |
| T _{DP-AVG} | Average dew point temperature (non-condensing) ⁽¹⁵⁾ | | 28 | | °C |
| T _{DP-ELR} | Elevated dew point temperature range (non-condensing) ⁽¹⁶⁾ | 28 | 36 | | °C |
| CT _{ELR} | Cumulative time in elevated dew point temperature range | | 24 | | Months |
| Q _{AP-ILL} | Window aperture illumination overfill ^{(17) (18)} | | 17 | | W/cm ² |
| LAMP ILLUMINATION | | | | | |
| ILL _{UV} | Illumination wavelength < 395nm ⁽¹⁰⁾ | 0.68 | 2 | | mW/cm ² |
| ILL _{VIS} | Illumination wavelengths between 395nm and 800nm | | 29.3 | | W/cm ² |
| ILL _{IR} | Illumination wavelength > 800nm | | 10 | | mW/cm ² |
| SOLID STATE ILLUMINATION | | | | | |
| ILL _{UV} | Illumination wavelength < 410nm ⁽¹⁰⁾ | | 3 | | mW/cm ² |
| ILL _{VIS} | Illumination wavelengths between 410nm and 800nm | | 34.7 | | W/cm ² |
| ILL _{IR} | Illumination wavelength > 800nm | | 10 | | mW/cm ² |

- (1) Recommended Operating Conditions are applicable after the DMD is installed in the final product.
- (2) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
- (3) All voltage values are with respect to the V_{SS} ground pins.
- (4) V_{OFFSET} supply transients must fall within the specified max voltages.
- (5) To prevent excess current, the supply voltage delta | V_{DDA} – V_{DD} | must be less than the specified limit.
- (6) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than the specified limit.
- (7) The LVCMOS input pin is DMD_DEN_ARSTZ.
- (8) See the low-speed interface (LSIF) timing requirements in Timing Requirements.
- (9) See the high-speed serial interface (HSSI) timing requirements in Timing Requirements.
- (10) Simultaneous exposure of the DMD to the maximum Recommended Operating Conditions for temperature and UV illumination will reduce device lifetime.
- (11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point (TP1) shown in Figure 6-1 and the package thermal resistances using the Micromirror Array Temperature Calculation.
- (12) Per Figure 5-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to Micromirror Landed Duty Cycle for a definition of micromirror landed duty cycle.
- (13) Long-term is defined as the usable life of the device.
- (14) Short-term is the total cumulative time over the useful life of the device.
- (15) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (16) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
- (17) The active area of the DMD is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects on the performance of an end application using the DMD. The illumination optical system should be designed to minimize light flux incident outside the active array. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.
- (18) Applies to the region in red in Figure 5-2.

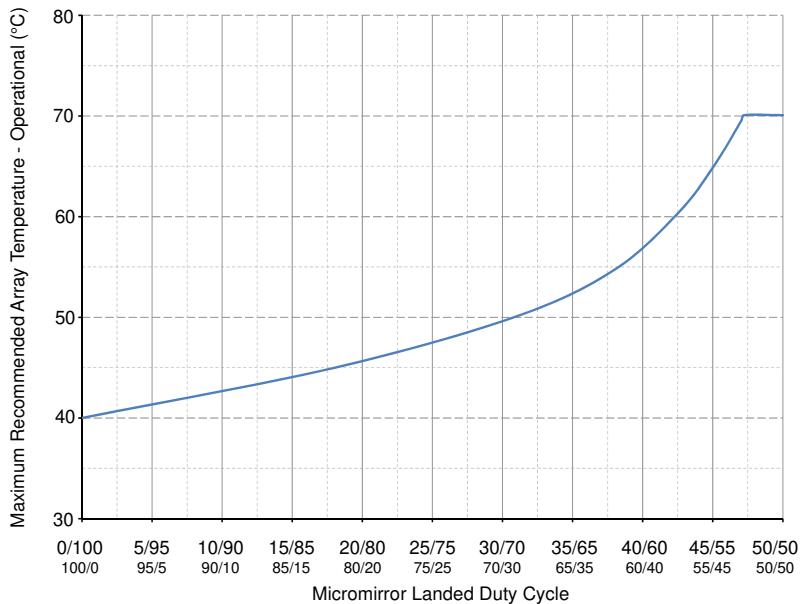


Figure 5-1. Maximum Recommended Array Temperature—Derating Curve

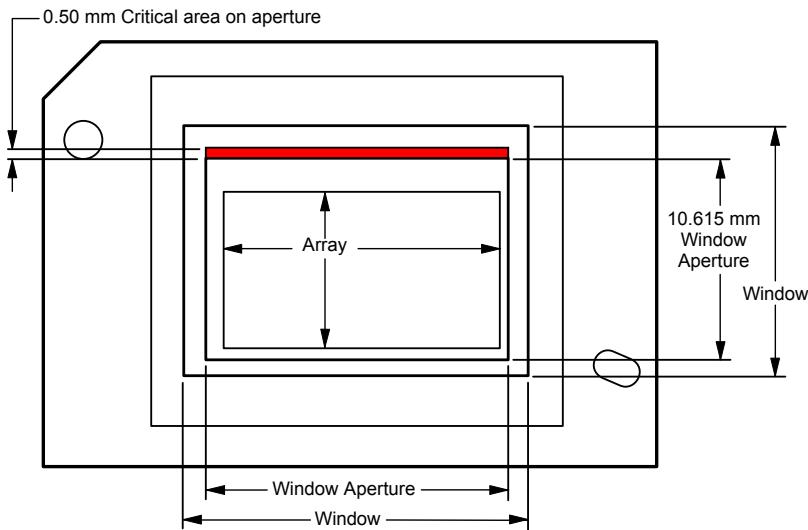


Figure 5-2. Illumination Overfill Diagram—Critical Area

5.5 Thermal Information

| THERMAL METRIC | DLP651NE | UNIT |
|--|-------------|------|
| | FYP Package | |
| | 149 PINS | |
| Thermal resistance, active area to test point 1 (TP1) ⁽¹⁾ | 0.60 | °C/W |

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems must be designed to minimize the light energy falling outside the window's clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

5.6 Electrical Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

| SYMBOL | PARAMETER ^{(1) (2)} | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|---|-----------------------|-----------------------|-----|------|
| Current – Typical | | | | | | |
| I _{DD} | Supply current V _{DD} ⁽³⁾ | | 800 | 1250 | mA | |
| I _{DDA} | Supply current V _{DDA} ⁽³⁾ | | 900 | 1200 | mA | |
| I _{DDA} | Supply current V _{DDA} ⁽³⁾ | single macro mode | 500 | 600 | mA | |
| I _{OFFSET} | Supply current V _{OFFSET} ^{(4) (5)} | | 23 | 35 | mA | |
| I _{BIAS} | Supply current V _{BIAS} ^{(4) (5)} | | 2.4 | 3.8 | mA | |
| I _{RESET} | Supply current V _{RESET} ⁽⁵⁾ | | -10.5 | -7.7 | mA | |
| Power – Typical | | | | | | |
| P _{DD} | Supply power dissipation V _{DD} ⁽³⁾ | | 1440 | 2437.5 | mW | |
| P _{DDA} | Supply power dissipation V _{DDA} ⁽³⁾ | | 1620 | 2340 | mW | |
| P _{DDA} | Supply power dissipation V _{DDA} ⁽³⁾ | single macro mode | 900 | 1170 | mW | |
| P _{OFFSET} | Supply power dissipation V _{OFFSET} ^{(4) (5)} | | 230 | 367.5 | mW | |
| P _{BIAS} | Supply power dissipation V _{BIAS} ^{(4) (5)} | | 38.4 | 62.7 | mW | |
| P _{RESET} | Supply power dissipation V _{RESET} ⁽⁵⁾ | | 92.4 | 131.25 | mW | |
| P _{TOTAL} | Supply power dissipation Total | | 3420.8 | 5338.95 | mW | |
| LVC MOS Input | | | | | | |
| I _{IL} | Low level input current ⁽⁶⁾ | V _{DD} = 1.95V, V _I = 0V | -100 | | | nA |
| I _{IH} | High level input current ⁽⁶⁾ | V _{DD} = 1.95V, V _I = 1.95V | | 135 | μA | |
| LVC MOS Output | | | | | | |
| V _{OH} | DC output high voltage ⁽⁷⁾ | I _{OH} = -2mA | 0.8 × V _{DD} | | | V |
| V _{OL} | DC output low voltage ⁽⁷⁾ | I _{OL} = 2mA | | 0.2 × V _{DD} | | V |
| Receiver Eye Characteristics | | | | | | |
| A1 | Minimum data eye opening ⁽⁸⁾ | | 100 | 600 | mV | |
| A1 | Minimum clock eye opening ⁽⁸⁾ | | 295 | 600 | mV | |
| A2 | Maximum signal swing ^{(8) (9)} | | | 600 | mV | |
| X1 | Maximum eye closure ⁽⁸⁾ | | | 0.275 | UI | |
| X2 | Maximum eye closure ⁽⁸⁾ | | | 0.4 | UI | |
| t _{DRIFT} | Drift between Clock and Data between Training Patterns | | | 20 | ps | |
| Capacitance | | | | | | |
| C _{IN} | Input capacitance LVC MOS | f = 1MHz | | 10 | pF | |
| C _{IN} | Input capacitance LSIF (low speed interface) | f = 1MHz | | 20 | pF | |
| C _{IN} | Input capacitance HSSI (high speed serial interface) - Differential - Clock and Data pins | f = 1MHz | | 5 | pF | |
| C _{OUT} | Output capacitance | f = 1MHz | | 10 | pF | |

- (1) All power supply connections are required to operate the DMD: V_{DD}, V_{DDA}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are required to operate the DMD.
- (2) All voltage values are with respect to the ground pins (V_{SS}).
- (3) To prevent excess current, the supply voltage delta | V_{DDA} – V_{DD} | must be less than specified limit.
- (4) To prevent excess current, the supply voltage delta | V_{BIAS} – V_{OFFSET} | must be less than specified limit.
- (5) Supply power dissipation based on three global resets in 200μs.
- (6) LVC MOS input specifications are for pin DMD_DEN_ARSTZ.
- (7) LVC MOS output specification is for pins LS_RDATA_A and LS_RDATA_B.
- (8) Refer to [Figure 5-12](#) (1e-12 BER).

(9) Defined in the *Recommended Operating Conditions*

5.7 Switching Characteristics

Over operating free-air temperature range and supply voltages (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------|--|---|------|-----|------|------|
| t_{pd} | Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output | $C_L = 5\text{pF}$ | | | 11.1 | ns |
| t_{pd} | Output propagation, clock to Q, rising edge of LS_CLK (differential clock signal) input to LS_RDATA output | $C_L = 10\text{pF}$ | | | 11.3 | ns |
| | Slew rate, LS_RDATA | 20% to 80%, $C_L < 40\text{p}$ | 0.35 | | | V/ns |
| | Output duty cycle distortion, LS_RDATA_A and LS_RDATA_B | $50 - (C2Q_{rise} - C2Q_{fall}) \times 130\text{e}6 \times 100$ | 40% | | 60% | |

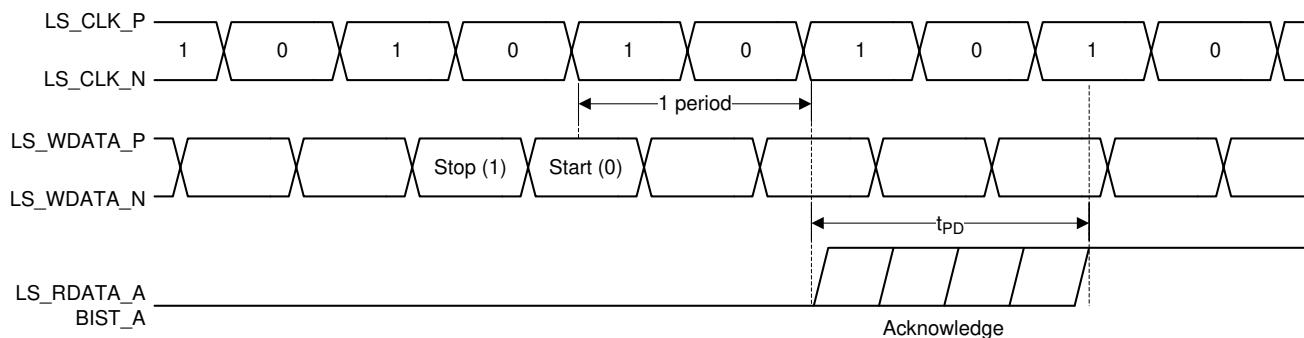


Figure 5-3. Switching Characteristics

5.8 Timing Requirements

Over operating free-air temperature range and supply voltages (unless otherwise noted)

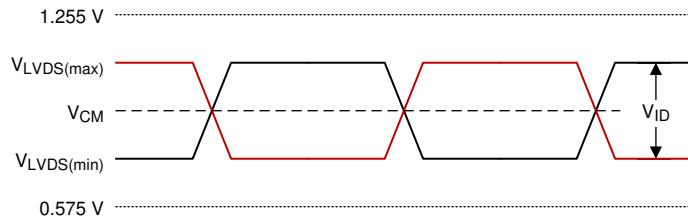
| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|------------------------------------|--|-------|-----|-----|------|
| LVC MOS | | | | | | |
| t_r | Rise time ⁽¹⁾ | 20% to 80% reference points | | | 25 | ns |
| t_f | Fall time ⁽¹⁾ | 80% to 20% reference points | | | 25 | ns |
| Low Speed Interface (LSIF) | | | | | | |
| t_r | Rise time ⁽²⁾ | 20% to 80% reference points | | | 450 | ps |
| t_f | Fall time ⁽²⁾ | 80% to 20% reference points | | | 450 | ps |
| $t_{W(H)}$ | Pulse duration high ⁽³⁾ | LS_CLK. 50% to 50% reference points | 3.1 | | | ns |
| $t_{W(L)}$ | Pulse duration low ⁽³⁾ | LS_CLK. 50% to 50% reference points | 3.1 | | | ns |
| t_{su} | Setup time ⁽⁴⁾ | LS_WDATA valid before rising edge of LS_CLK (differential) | 1.5 | | | ns |
| t_h | Hold time ⁽⁴⁾ | LS_WDATA valid after rising edge of LS_CLK (differential) | 1.5 | | | ns |
| High Speed Serial Interface (HSSI) | | | | | | |
| t_r | Rise time ⁽⁵⁾ , Data | from -A1 to A1 minimum eye height specification | 50 | 115 | | ps |
| t_r | Rise time ⁽⁵⁾ , Clock | from -A1 to A1 minimum eye height specification | 50 | 135 | | ps |
| t_f | Fall time ⁽⁵⁾ , Data | from A1 to -A1 minimum eye height specification | 50 | 115 | | ps |
| t_f | Fall time ⁽⁵⁾ , Clock | from A1 to -A1 minimum eye height specification | 50 | 135 | | ps |
| $t_{W(H)}$ | Pulse duration high ⁽⁶⁾ | DCLK. 50% to 50% reference points | 0.275 | | | ns |
| $t_{W(L)}$ | Pulse duration low ⁽⁶⁾ | DCLK. 50% to 50% reference points | 0.275 | | | ns |

5.8 Timing Requirements (continued)

Over operating free-air temperature range and supply voltages (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------|----------------|-----------------|-------|-------|-----|------|
| t_c | Cycle time (6) | DCLK | 0.625 | 0.833 | ns | |

- (1) See the LVC MOS Rise, Fall Time Slew Rate Figures. Specification is for DMD_DEN_ARSTZ pin (LVC MOS).
- (2) See the figure for rise and fall time for LSIF.
- (3) See the figure for pulse duration high and low time for LSIF.
- (4) See the figure for setup and hold time for LSIF.
- (5) See figure for rise and fall time for HSSI.
- (6) See the figure for pulse duration high and low and cycle time for HSSI.



A. See [Equation 1](#) and .

Figure 5-4. LSIF Waveform Requirements

$$V_{LVDS(\max)} = V_{CM(\max)} + \left| \frac{1}{2} \times V_{ID(\max)} \right| \quad (1)$$

$$V_{LVDS(\min)} = V_{CM(\min)} - \left| \frac{1}{2} \times V_{ID(\max)} \right| \quad (2)$$

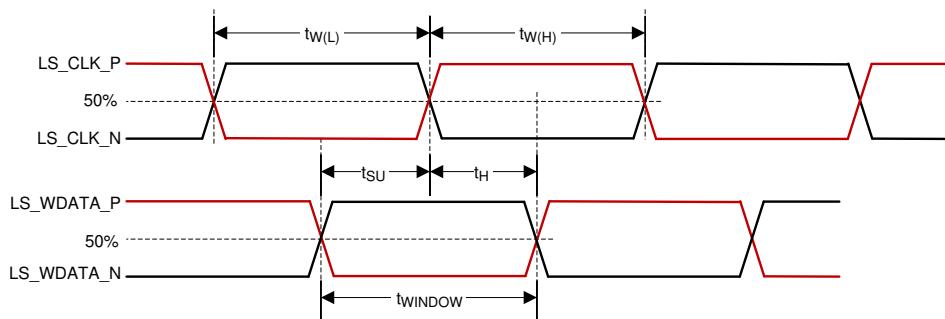


Figure 5-5. LSIF Timing Requirements

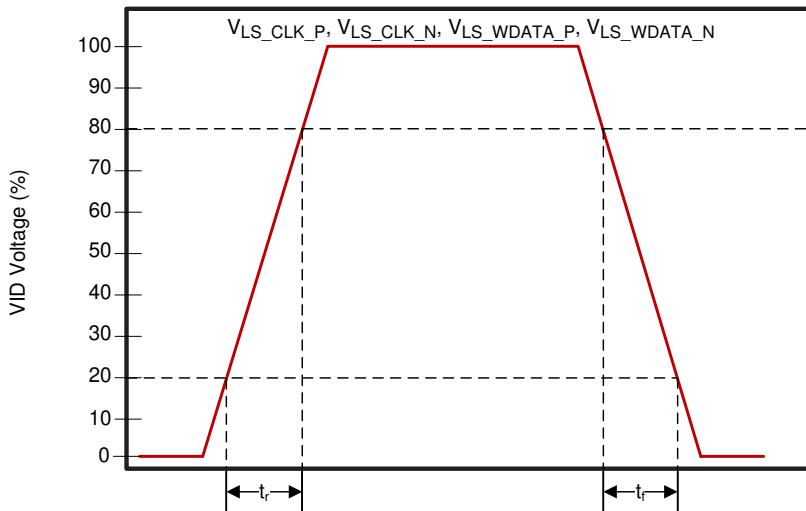


Figure 5-6. LSIF Rise, Fall Time Slew Rate

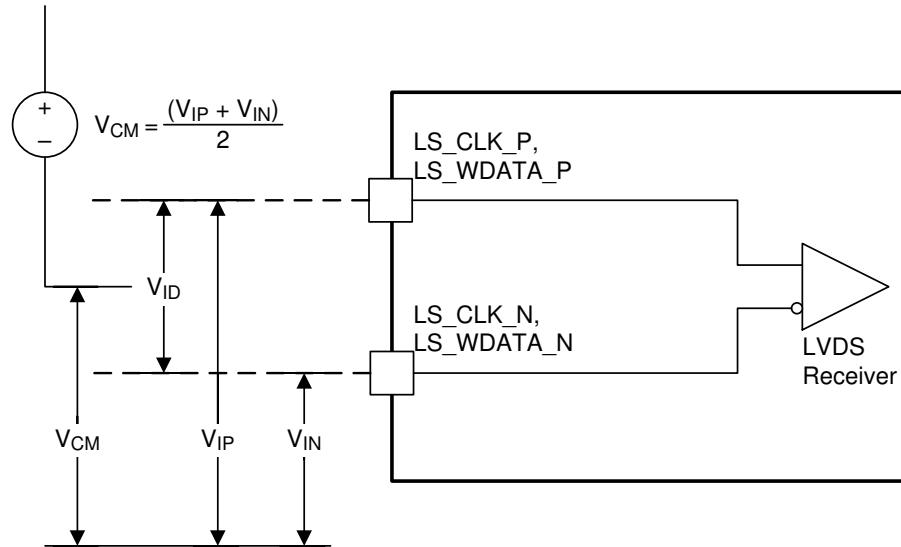


Figure 5-7. LSIF Voltage Requirements

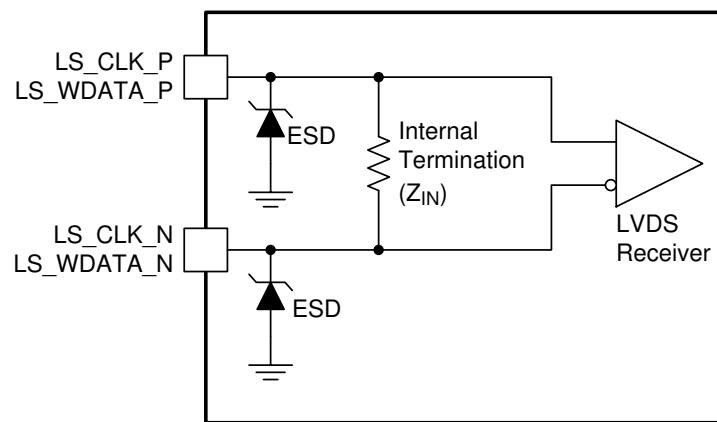


Figure 5-8. LSIF Equivalent Input

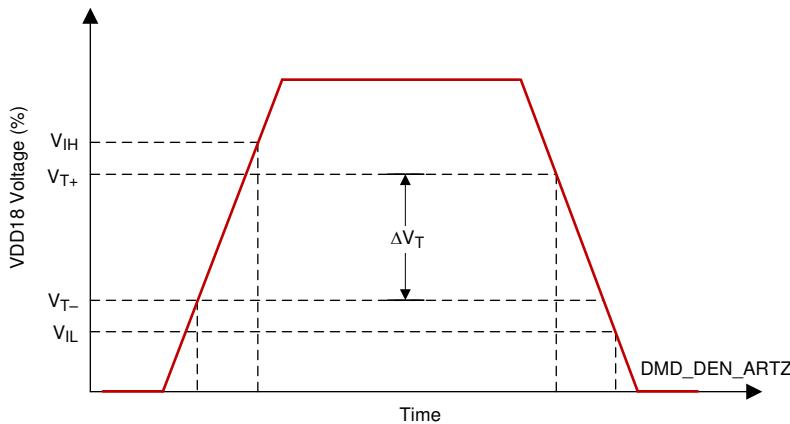


Figure 5-9. LVC MOS Input Hysteresis

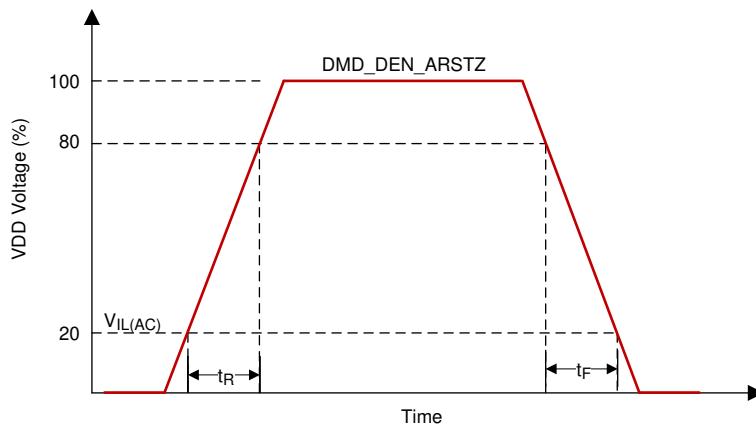
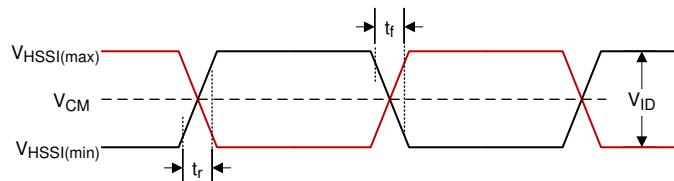


Figure 5-10. LVC MOS Rise, Fall Time Slew Rate



A. See [Equation 3](#) and [Equation 4](#)

Figure 5-11. HSSI Waveform Requirements

$$V_{HSSI(max)} = V_{CM(max)} + \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (3)$$

$$V_{HSSI(min)} = V_{CM(min)} - \left| \frac{1}{2} \times V_{ID(max)} \right| \quad (4)$$

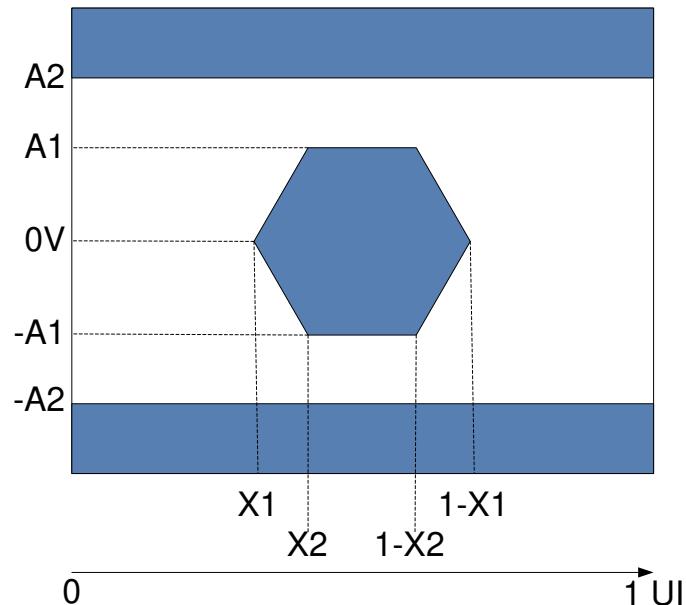


Figure 5-12. HSSI Eye Characteristics

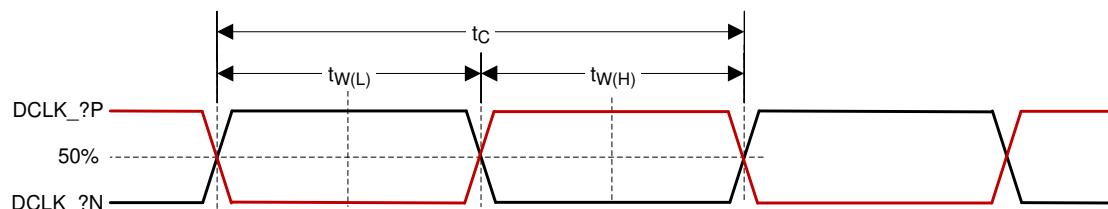


Figure 5-13. HSSI CLK Characteristics

5.9 System Mounting Interface Loads

| PARAMETER | MIN | TYP | MAX | UNIT |
|--|-----|-----|-----|------|
| When loads are applied on both the electrical and thermal interface areas | | | | |
| Maximum load to be applied to the electrical interface area ⁽¹⁾ | | | 111 | N |
| Maximum load to be applied to the thermal interface area ⁽¹⁾ | | | 111 | N |
| When load is applied on the electrical interface area only | | | | |
| Maximum load to be applied to the electrical interface area ⁽¹⁾ | | | 222 | N |
| Maximum load to be applied to the thermal interface area ⁽¹⁾ | | | 0 | N |

(1) The load should be applied uniformly in the corresponding areas shown in Figure 5-14.

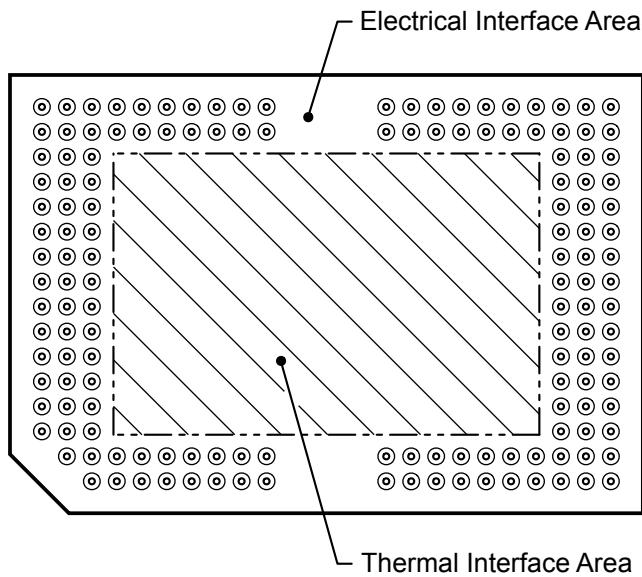


Figure 5-14. System Mounting Interface Loads

5.10 Micromirror Array Physical Characteristics

| SYMBOL | PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------|--|--|-----|--------|-----|-------------------|
| M | Number of active columns ⁽¹⁾ | | | 1920 | | micromirrors |
| N | Number of active rows ⁽¹⁾ | | | 1080 | | micromirrors |
| P | Micromirror (pixel) pitch ⁽¹⁾ | | | 7.6 | | um |
| | Micromirror active array width ⁽¹⁾ | (micromirror pitch) × (number of active columns) | | 14.592 | | mm |
| | Micromirror active array height ⁽¹⁾ | (micromirror pitch) × (number of active rows) | | 8.208 | | mm |
| | Micromirror active border ⁽²⁾ | Pond of micromirror (POM) | | 14 | | micromirrors/side |

(1) See [Figure 6-15](#).

(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

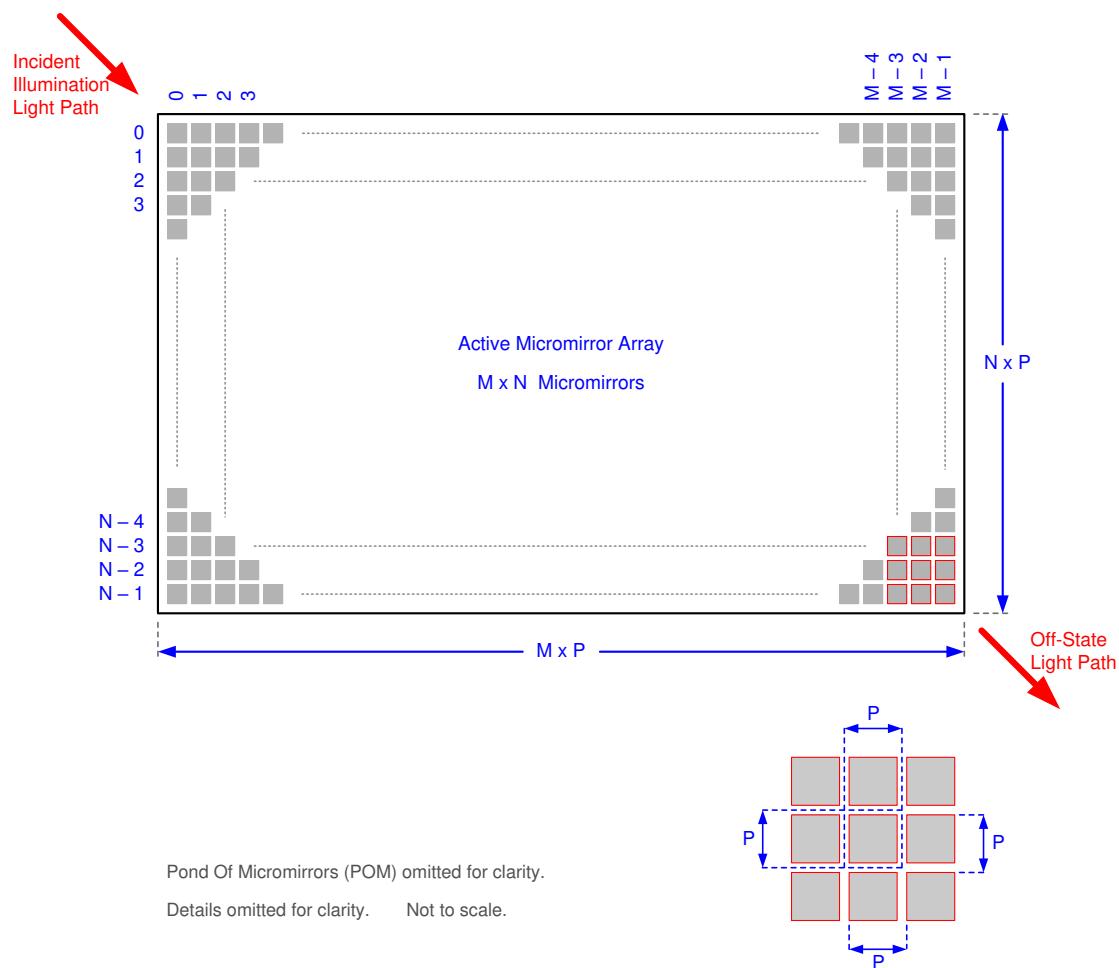
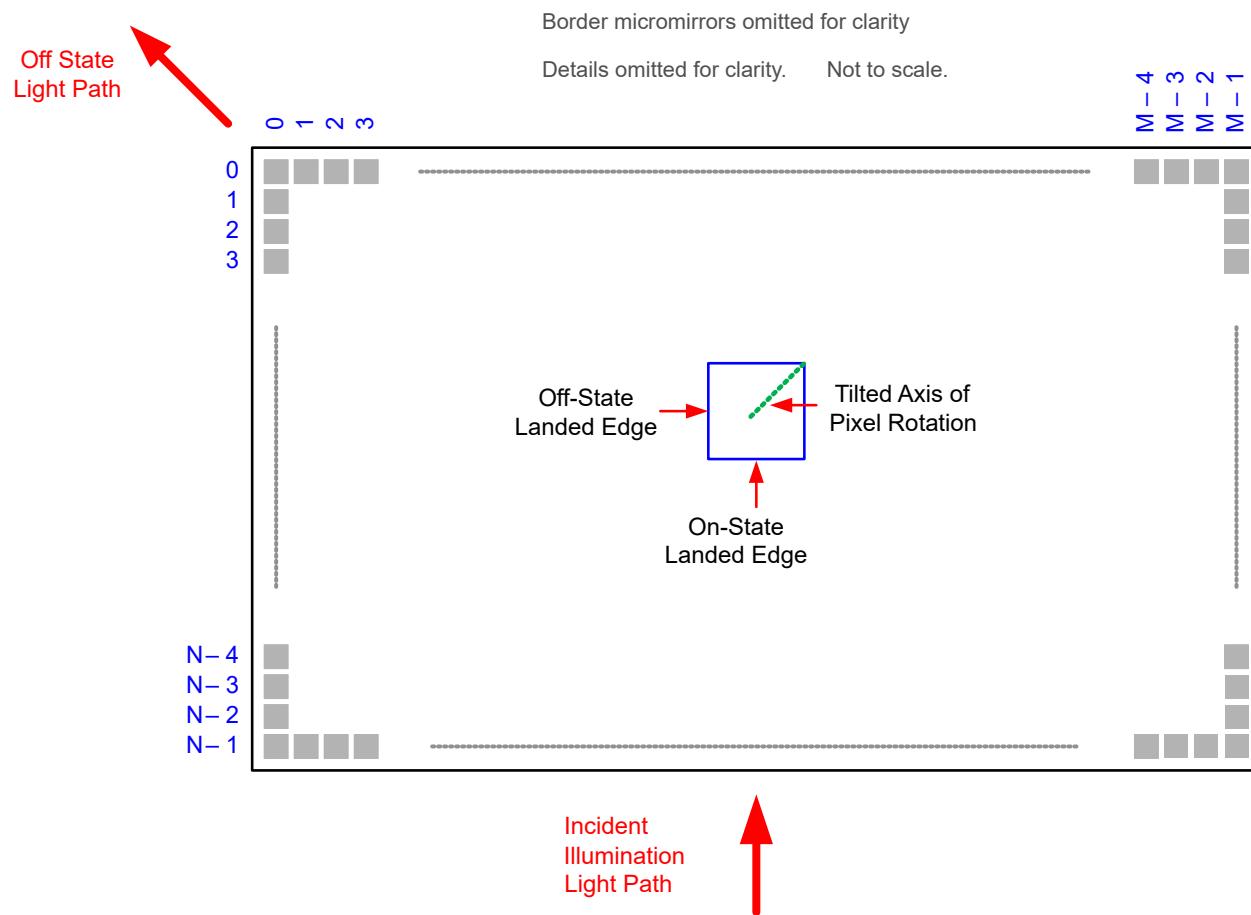


Figure 5-15. Micromirror Array Physical Characteristics

5.11 Micromirror Array Optical Characteristics

| PARAMETER | TEST CONDITION | MIN | NOM | MAX | UNIT |
|--|--|--------------------------------|-----|-----|--------------|
| Micromirror tilt angle, variation device to device ⁽²⁾ ⁽³⁾ ⁽⁴⁾ ⁽⁵⁾ | Landed State ⁽¹⁾ | 11 | 12 | 13 | degrees |
| Image performance ⁽⁶⁾ | Bright pixel(s) in active area ⁽⁷⁾ | Gray 10 screen ⁽¹⁰⁾ | | 0 | micromirrors |
| | Bright pixel(s) in the POM ^{(7) (9)} | Gray 10 screen ⁽¹⁰⁾ | | 1 | |
| | Dark pixel(s) in the active area ⁽⁸⁾ | White screen ⁽¹¹⁾ | | 4 | |
| | Adjacent pixel(s) ⁽¹²⁾ | Any screen | | 0 | |
| | Unstable pixel(s) in active area ⁽¹³⁾ | Any screen | | 0 | |

- (1) Measured relative to the plane formed by the overall micromirror array
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) This represents the variation that can occur between any two individual micromirrors, located on the same device or on different devices.
- (4) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variations within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
- (5) See [Figure 5-16](#).
- (6) Conditions of acceptance. All DMD image performance returns are evaluated using the following projected image test conditions:
 - Test set degamma shall be linear.
 - Test set brightness and contrast shall be set to nominal.
 - The diagonal size of the projected image shall be a minimum of 60 inches.
 - The projections screen shall be a 1x gain.
 - The projected image shall be inspected from an 8-foot minimum viewing distance.
 - The image shall be in focus during all image performance tests.
- (7) Bright pixel definition: a single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.
- (8) Dark pixel definition: a single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.
- (9) POM definition: The rectangular border of off-state mirrors surrounding the active area.
- (10) Gray 10 screen definition: A full screen with RGB values set to R=10/255, G=10/255, B=10/255.
- (11) White screen definition: A full screen with RGB values set to R=255/255, G=255/255, B=255/255.
- (12) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point. Also referred to as a cluster
- (13) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.



- A. Pond of micromirrors (POM) omitted for clarity.
- B. Refer to the *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 5-16. Micromirror Landed Orientation and Tilt

5.12 Window Characteristics

| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------------|-----|-----------------|-----|------|
| Window material designation | WLP | | Corning EagleXG | | |
| Window refractive index | at wavelength 546.1nm | | 1.5119 | | |

5.13 Chipset Component Usage Specification

Reliable function and operation of the DLP651NE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

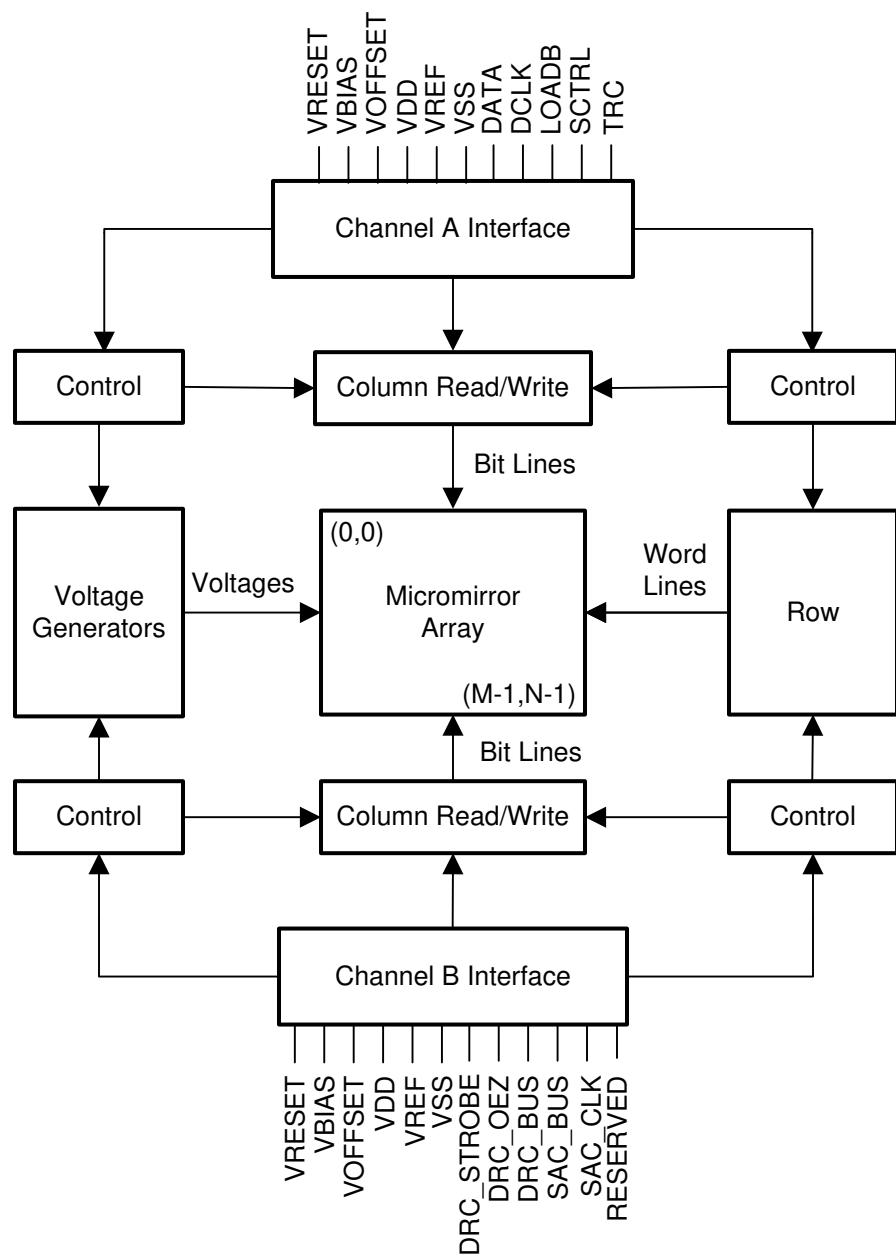
6 Detailed Description

6.1 Overview

The DMD is a 0.65-inch diagonal spatial light modulator that consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-optical-electrical-mechanical system (MOEMS). The fast switching speed of the DMD micromirrors, combined with advanced DLP image processing algorithms, enables frame rates of up to 240Hz to be displayed. The electrical interface is low-voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to [Section 6.2](#). The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of the underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP 0.65" 1080p chipset is comprised of the DLP651NE DMD, [DLPC7530](#) display controller, the [DLPA100](#) power management and motor driver. To ensure reliable operation, the DLP651NE DMD must always be used with the DLP display controller and the power and motor specified in the chipset.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Interface

The DMD requires four DC voltages: 1.8V source, V_{OFFSET} , V_{RESET} , and V_{BIAS} . In a typical configuration, 3.3V is created by the [DLPA100](#) power management and motor driver and is used on the DMD board to create the 1.8V. The TI voltage regulator [TPS65145](#) takes in the 3.3V and outputs V_{OFFSET} , V_{RESET} , and V_{BIAS} .

6.3.2 Timing

The data sheet specifies the timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered. Timing reference loads are not intended to be precise representations of any particular system environment or depict the actual load presented by a production test. TI recommends that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. Use the specified load capacitance value for characterization and measurement of AC timing signals only. This load capacitance value does not indicate the maximum load the device is capable of driving.

6.4 Device Functional Modes

DMD functional modes are controlled by the DLPC7530 display controller. See the [DLPC7530 Display Controller Data Sheet](#) or contact a TI applications engineer.

6.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relates to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance are contingent on compliance with the optical system operating conditions described in the following sections.

6.5.1 Numerical Aperture and Stray Light Control

TI recommends that the light cone angle defined by the numerical aperture of the illumination optics is the same as the light cone angle defined by the numerical aperture of the projection optics. This angle must not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD, such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and active area could occur.

6.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

6.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit the light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level to be acceptable.

6.6 Micromirror Array Temperature Calculation

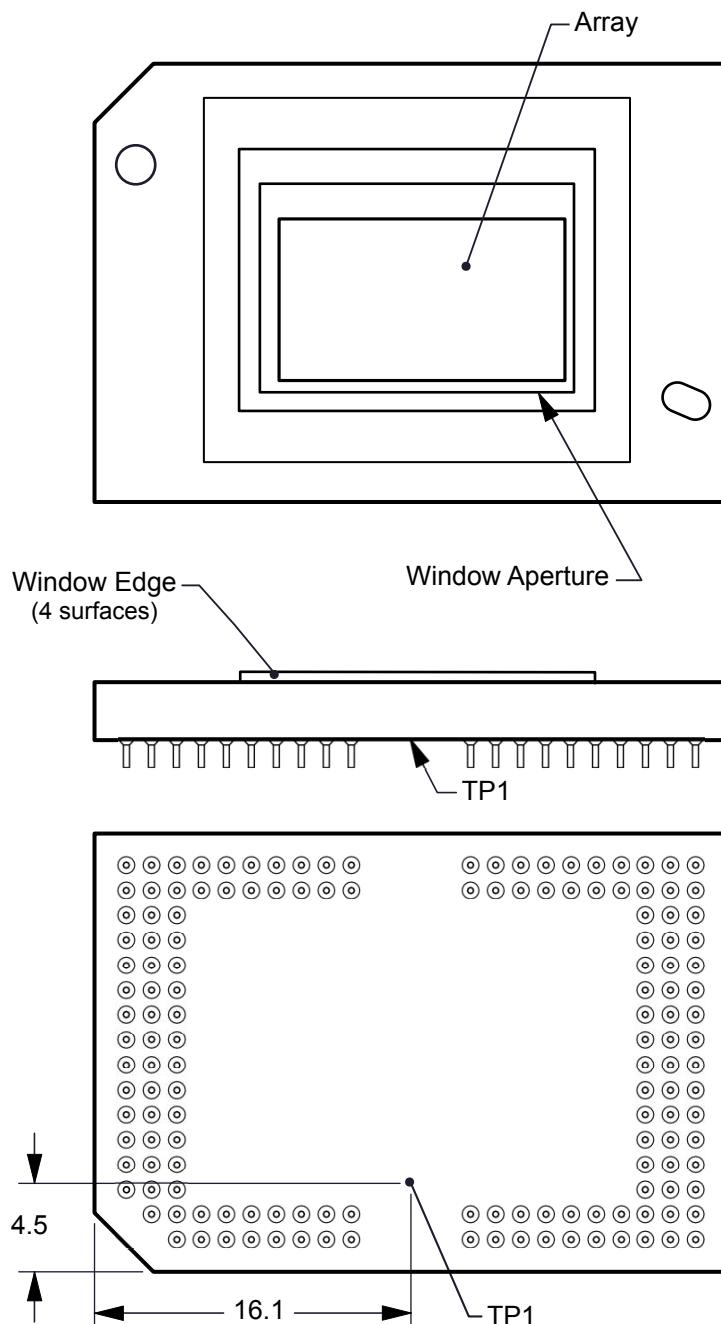


Figure 6-1. DMD Thermal Test Point

Micromirror array temperature cannot be measured directly; therefore, it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC}) \quad (5)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (6)$$

where

- T_{ARRAY} = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY-TO-CERAMIC}$ = Thermal resistance of package specified in *Thermal Information* from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity \times $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.45

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 3.0W. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single-chip or multi-chip DMD system. It assumes an illumination distribution of 83.7% on the active array and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$$Q_{INCIDENT} = 48W \text{ (measured)} \quad (7)$$

$$T_{CERAMIC} = 55.0^{\circ}\text{C} \text{ (measured)} \quad (8)$$

$$Q_{ELECTRICAL} = 3.0W \quad (9)$$

$$Q_{ARRAY} = 3.0W + (0.45 \times 48W) = 24.6W \quad (10)$$

$$T_{ARRAY} = 55.0^{\circ}\text{C} + (24.6W \times 0.6^{\circ}\text{C}/W) = 69.8^{\circ}\text{C} \quad (11)$$

6.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and the ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV-RATIO} \times Q_{INCIDENT}] \times 1000\text{mW/W} \div A_{ILL}$ (mW/cm²)
- $ILL_{VIS} = [OP_{VIS-RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm²)
- $ILL_{IR} = [OP_{IR-RATIO} \times Q_{INCIDENT}] \times 1000\text{mW/W} \div A_{ILL}$ (mW/cm²)
- $ILL_{BLU} = [OP_{BLU-RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm²)
- $ILL_{BLU1} = [OP_{BLU1-RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm²)
- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ (cm²)

where:

- ILL_{UV} = UV illumination power density on the DMD (mW/cm^2)
- ILL_{VIS} = VIS illumination power density on the DMD (W/cm^2)
- ILL_{IR} = IR illumination power density on the DMD (mW/cm^2)
- ILL_{BLU} = BLU illumination power density on the DMD (W/cm^2)
- ILL_{BLU1} = BLU1 illumination power density on the DMD (W/cm^2)
- A_{ILL} = illumination area on the DMD (cm^2)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- A_{ARRAY} = area of the array (cm^2) (data sheet)
- OV_{ILL} = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV-RATIO}$ = ratio of the optical power for wavelengths $<410\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS-RATIO}$ = ratio of the optical power for wavelengths $\geq410\text{nm}$ and $\leq800\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR-RATIO}$ = ratio of the optical power for wavelengths $>800\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU-RATIO}$ = ratio of the optical power for wavelengths $\geq410\text{nm}$ and $\leq475\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1-RATIO}$ = ratio of the optical power for wavelengths $\geq410\text{nm}$ and $\leq440\text{nm}$ to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and the overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array (OV_{ILL}) and the percent of the total illumination that is on the active array. From these values, the illumination area (A_{ILL}) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$$Q_{INCIDENT} = 48\text{W} \text{ (measured)}$$

$$A_{ARRAY} = (14.5920\text{mm} \times 8.2080\text{mm}) \div 100\text{mm}^2/\text{cm}^2 = 1.1977\text{cm}^2 \text{ (data sheet)}$$

$$OV_{ILL} = 16.3\% \text{ (optical model)}$$

$$OP_{UV-RATIO} = 0.00017 \text{ (spectral measurement)}$$

$$OP_{VIS-RATIO} = 0.99977 \text{ (spectral measurement)}$$

$$OP_{IR-RATIO} = 0.00006 \text{ (spectral measurement)}$$

$$OP_{BLU-RATIO} = 0.28100 \text{ (spectral measurement)}$$

$$OP_{BLU1-RATIO} = 0.03200 \text{ (spectral measurement)}$$

$$A_{ILL} = 1.1977\text{cm}^2 \div (1 - 0.163) = 1.4310\text{cm}^2$$

$$ILL_{UV} = [0.00017 \times 48\text{W}] \times 1000\text{mW/W} \div 1.4310\text{cm}^2 = 5.702\text{mW/cm}^2$$

$$ILL_{VIS} = [0.99977 \times 48W] \div 1.4310\text{cm}^2 = 33.54\text{W/cm}^2$$

$$ILL_{IR} = [0.00006 \times 48W] \times 1000\text{mW/W} \div 1.4310\text{cm}^2 = 2.013\text{mW/cm}^2$$

$$ILL_{BLU} = [0.28100 \times 48W] \div 1.4310\text{cm}^2 = 9.43\text{W/cm}^2$$

$$ILL_{BLU1} = [0.03200 \times 48W] \div 1.4310\text{cm}^2 = 1.07\text{W/cm}^2$$

6.8 Window Aperture Illumination Overfill Calculation

The amount of optical overfill on the critical area of the window aperture cannot be measured directly. For systems with uniform illumination on the array, the amount is determined using the total measured incident optical power on the DMD, and the ratio of the total optical power on the DMD that is on the defined critical area. The optical model is used to determine the percent of optical power on the window aperture critical area and estimate the size of the area.

- $Q_{AP-ILL} = [Q_{INCIDENT} \times OP_{AP_ILL_RATIO}] + A_{AP_ILL}(\text{W/cm}^2)$

where:

- Q_{AP-ILL} = window aperture illumination overfill (W/cm^2)
- $Q_{INCIDENT}$ = total incident optical power on the DMD (Watts) (measured)
- $OP_{AP_ILL_RATIO}$ = ratio of the optical power on the critical area of the window aperture to the total optical power on the DMD (optical model)
- A_{AP_ILL} = size of the window aperture critical area (cm^2) (data sheet)
- OP_{CA_RATIO} = percent of the window aperture critical area with incident optical power (%) (optical model)

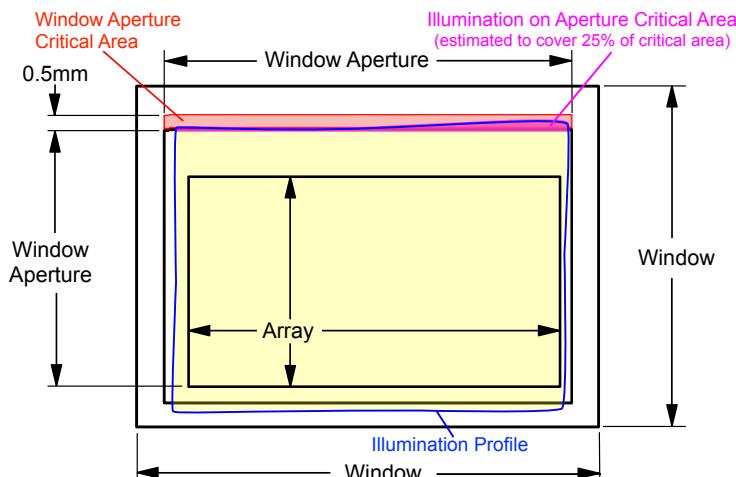


Figure 6-2. Illumination Overfill Diagram—Critical Area

$Q_{INCIDENT}=48\text{W}$ (measured)

$OP_{AP_ILL_RATIO}=0.312\%$ (optical model)

$OP_{CA_RATIO}=25\%$ (optical model)

Length of the window aperture for critical area = 1.5998cm (data sheet mechanical icd)

Width of critical area = 0.050cm (data sheet)

$$A_{AP-ILL} = 1.5998\text{cm} \times 0.050\text{cm} = 0.079990\text{cm}^2$$

$$Q_{AP-ILL} = (48\text{W} \times 0.00312) + (0.079990\text{cm}^2 \times 0.25) = 7.5\text{W/cm}^2$$

6.9 Micromirror Landed-On/Landed-Off Duty Cycle

6.9.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the percentage of time that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

For example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time); whereas 0/100 indicates that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

6.9.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD useful life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical, whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

6.9.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD useful life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD useful life. This is quantified in the derating curve shown in *Maximum Recommended Array Temperature—Derating Curve*. The importance of this curve is that:

- All points along this curve represent the same useful life.
- All points above this curve represent a lower useful life (and the further away from the curve, the lower the useful life).
- All points below this curve represent a higher useful life (and the further away from the curve, the higher the useful life).

In practice, this curve specifies the maximum operating DMD temperature for a given long-term average landed duty cycle.

6.9.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in [Table 6-1](#).

Table 6-1. Grayscale Value and Landed Duty Cycle

| GRAYSCALE VALUE | LANDED DUTY CYCLE |
|-----------------|-------------------|
| 0% | 0/100 |

Table 6-1. Grayscale Value and Landed Duty Cycle (continued)

| GRAYSCALE VALUE | LANDED DUTY CYCLE |
|-----------------|-------------------|
| 10% | 10/90 |
| 20% | 20/80 |
| 30% | 30/70 |
| 40% | 40/60 |
| 50% | 50/50 |
| 60% | 60/40 |
| 70% | 70/30 |
| 80% | 80/20 |
| 90% | 90/10 |
| 100% | 100/0 |

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed to achieve the desired white point.

Use this equation to calculate the landed duty cycle of a given pixel during a given time period:

$$\begin{aligned}
 \text{Landed Duty Cycle} = & \\
 (\text{Red_Cycle_ \%} \times \text{Red_Scale_Value}) + & \\
 (\text{Green_Cycle_ \%} \times \text{Green_Scale_Value}) + & \\
 (\text{Blue_Cycle_ \%} \times \text{Blue_Scale_Value})
 \end{aligned}$$

where

- Red_Cycle_%, represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 30%, 50%, and 20% respectively (to achieve the desired white point), then the landed duty cycle for various combinations of red, green, and blue color intensities is shown in [Table 6-2](#) and [Table 6-3](#).

Table 6-2. Example Landed Duty Cycle for Full-Color, Color Percentage

| CYCLE PERCENTAGE | | |
|------------------|-------|------|
| RED | GREEN | BLUE |
| 30% | 50% | 20% |

Table 6-3. Example Landed Duty Cycle for Full-Color

| RED | GREEN | BLUE | LANDED DUTY CYCLE |
|------|-------|------|-------------------|
| | | | |
| 0% | 0% | 0% | 0/100 |
| 100% | 0% | 0% | 30/70 |
| 0% | 100% | 0% | 50/50 |
| 0% | 0% | 100% | 20/80 |
| 0% | 12% | 0% | 6/94 |

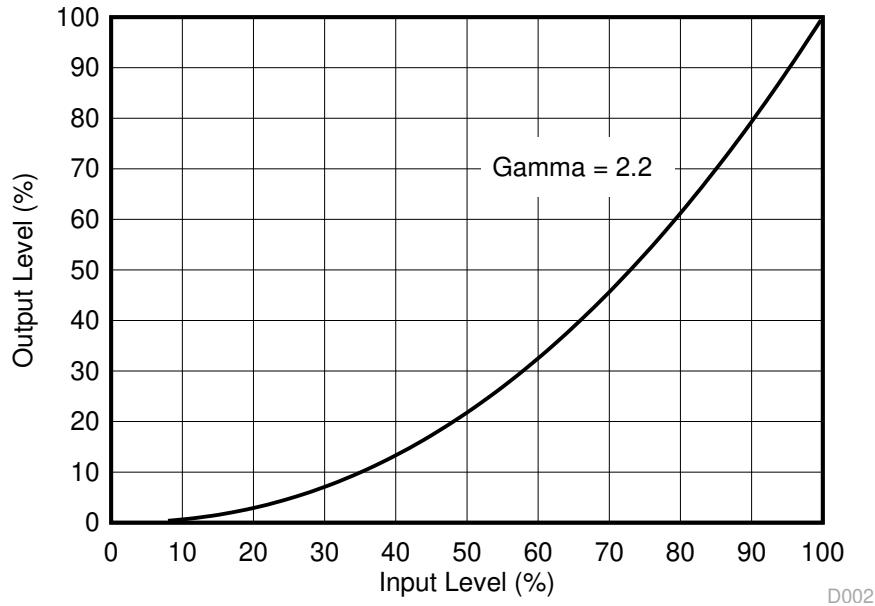
**Table 6-3. Example Landed Duty Cycle for Full-Color
(continued)**

| SCALE VALUE | | | LANDED DUTY CYCLE |
|-------------|-------|------|-------------------|
| RED | GREEN | BLUE | |
| 0% | 0% | 35% | 7/93 |
| 60% | 0% | 0% | 18/82 |
| 0% | 100% | 100% | 70/30 |
| 100% | 0% | 100% | 50/50 |
| 100% | 100% | 0% | 80/20 |
| 0% | 12% | 35% | 13/87 |
| 60% | 0% | 35% | 25/75 |
| 60% | 12% | 0% | 24/76 |
| 100% | 100% | 100% | 100/0 |

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLPC7530 controller, the gamma function affects the landed duty cycle.

Gamma is a power function of the form $\text{Output_Level} = A \times \text{Input_Level}^{\text{Gamma}}$, where A is a scaling factor that is typically set to 1.

In the DLPC7530 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in [Figure 6-3](#).


Figure 6-3. Example of Gamma = 2.2

From [Figure 6-3](#), if the gray scale value of a given input pixel is 40% (before gamma is applied), then the grayscale value is 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact on the displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

Consideration must also be given to any image processing that occurs before the DLPC7530 controller.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

DMDs are spatial light modulators, which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC7530 controller. Typical applications using the DLP651NE DMD include Laser TVs, smart projectors, and enterprise projectors.

DMD power-up and power-down sequencing is strictly controlled by the DLPC7530 through the TPS65145 PMIC. Refer to [Section 8](#) for power-up and power-down specifications. To ensure reliable operation, the DLP651NE DMD must always be used with [DLPC7530](#) controller, a [DLPA100](#) PMIC/motor driver, and a [TPS65145](#) PMIC.

7.2 Typical Application

The DLP651NE DMD, combined with DLPC7530 digital controller and a power management device provides, full 1080p resolution for bright, colorful display applications. A typical display system using laser phosphor illumination combines the DLP651NE DMD, [DLPC7530](#) display controller, [TPS65145](#) voltage regulator and [DLPA100](#) PMIC and motor driver. The diagram below shows a system block diagram for the Laser Phosphor configuration of the DLP 0.65" 1080p chipset. [Figure 7-2](#) shows a system block diagram for the LED configuration of the DLP 0.65" 1080p chipset. The components include DLP651NE DMD, [DLPC7530](#) display controller and [DLPA100](#) PMIC and motor driver and a [TPS65145](#) PMIC.

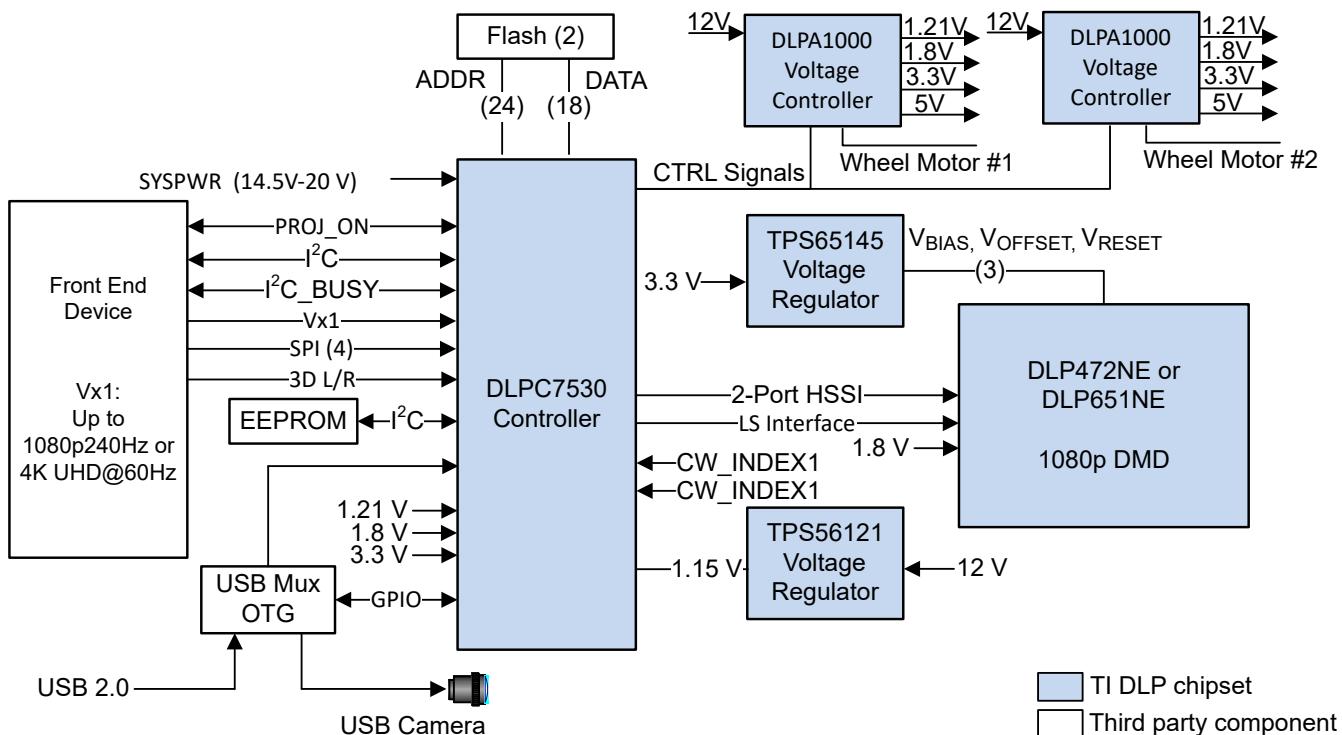


Figure 7-1. Typical Full HD Laser Phosphor Application Diagram

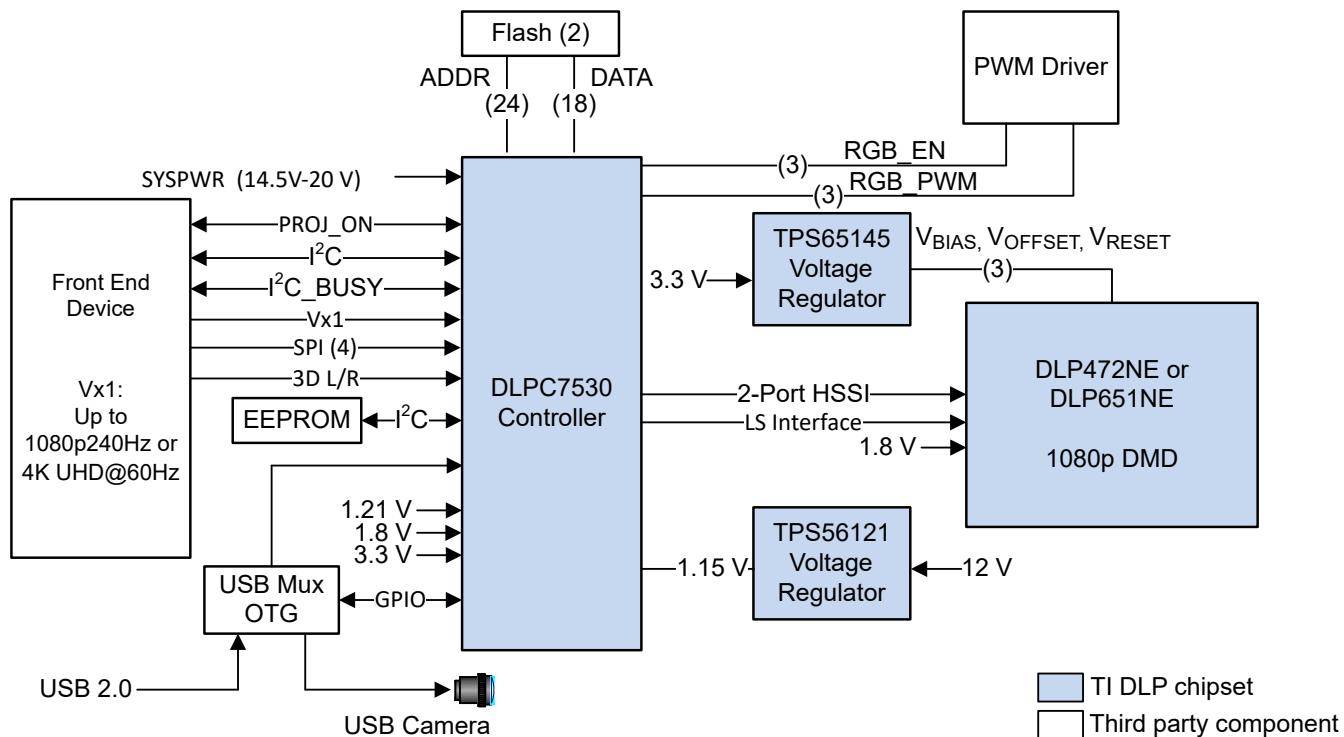


Figure 7-2. Typical Full HD LED Application Diagram

7.2.1 Design Requirements

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The type of illumination used and desired brightness have a major effect on the overall system design and size.

The display system uses the DLP651NE DMD as the core imaging device and contains a 0.65-inch array of micromirrors. The [DLPC7530](#) controller is the digital interface between the DMD and the rest of the system, taking digital input from the front-end receiver and driving the DMD over a high-speed interface. The [DLPA100](#) PMIC serves as a voltage regulator for the controller, the color filter wheel, and the phosphor wheel motor control. The [TPS65145](#) provides the DMD reset, offset, and bias voltages. The [LMR33630C](#) provides 1.8V power to the DLP651NE DMD.

7.2.2 Detailed Design Procedure

For a complete DLP system, an optical module or light engine is required that contains the DLP651NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DMD must always be used with [DLPC7530](#) display controller and the [TPS65145](#) PMIC and [DLPA100](#). Refer to the DMD board reference design and DLPC7530 reference design for layout and design recommendations.

7.2.3 Application Curve

In a typical projector application, the luminous flux on the screen from the DMD depends on the optical design of the projector. The efficiency and total power of the illumination optical system and the projection optical system determine the overall light output of the projector. The DMD is inherently a linear spatial light modulator, so its efficiency just scales the light output. [Figure 7-3](#) describes the relationship of laser input optical power to light output for a laser-phosphor illumination system, where the phosphor is not at its thermal quenching limit.

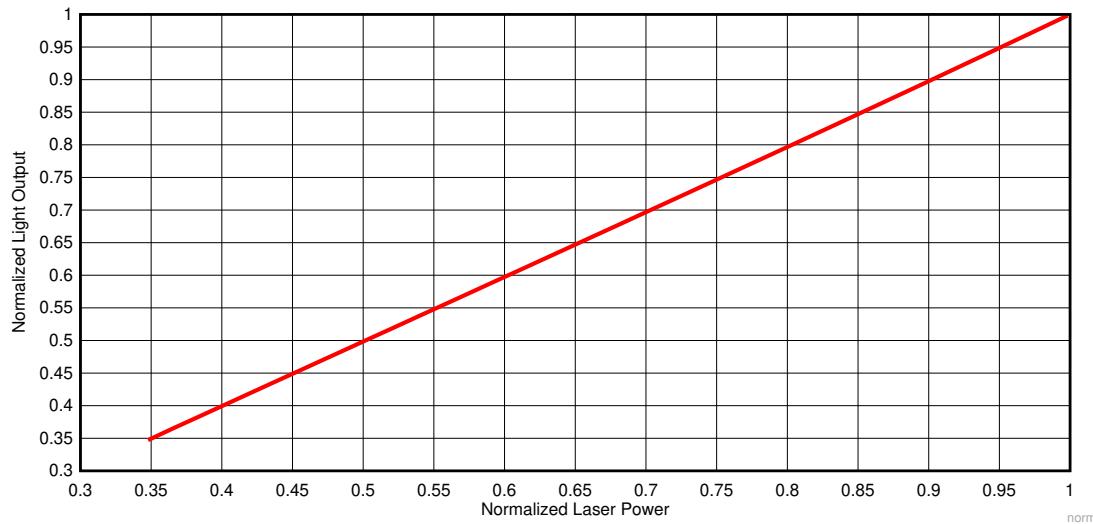
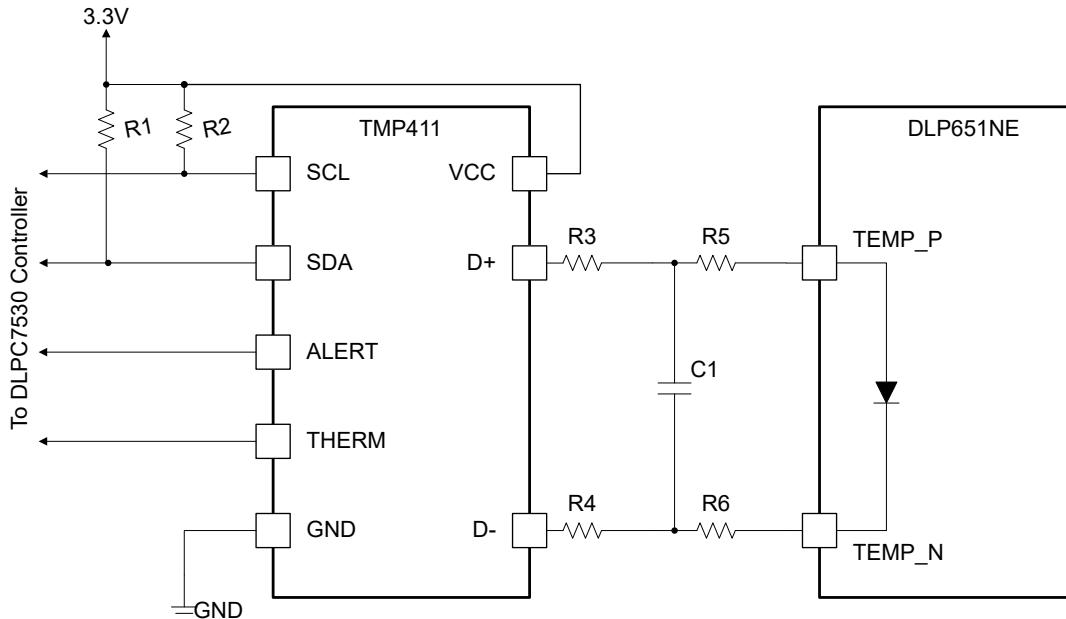


Figure 7-3. Normalized Light Output vs Normalized Laser Power for Laser Phosphor Illumination

7.3 Temperature Sensor Diode

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in the sample schematic. The software application contains functions to configure the [TMP411](#) to read the DLP651NE DMD temperature sensor diode. This data can be leveraged by the customer to incorporate additional functionality in the overall system design, such as adjusting illumination, fan speeds, and so on. All communication between the [TMP411](#) and the [DLPC7530](#) controller happens over the I²C interface. The [TMP411](#) connects to the DMD through the pins outlined in [Pin Functions](#).

Leave TEMP_N and TEMP_P pins unconnected (NC) if the temp sensor is not used.



- A. Details are omitted for clarity.
- B. See the [TMP411](#) data sheet for the system board layout recommendations.
- C. See the [TMP411](#) data sheet for the suggested component values for R1, R2, R3, R4, and C1.
- D. R5 = 0Ω. R6 = 0Ω. Place 0Ω resistors close to the DMD package pins.

Figure 7-4. TMP411 Sample Schematic

8 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- V_{SS}
- V_{BIAS}
- V_{DD}
- V_{OFFSET}
- V_{RESET}

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See the DMD power supply sequencing requirements in [Figure 8-1](#).

V_{BIAS} , V_{DD} , V_{OFFSET} , and V_{RESET} power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements results in a significant reduction in the DMD reliability and lifetime. Common ground V_{SS} must also be connected.

8.1 Power Supply Sequence Requirements

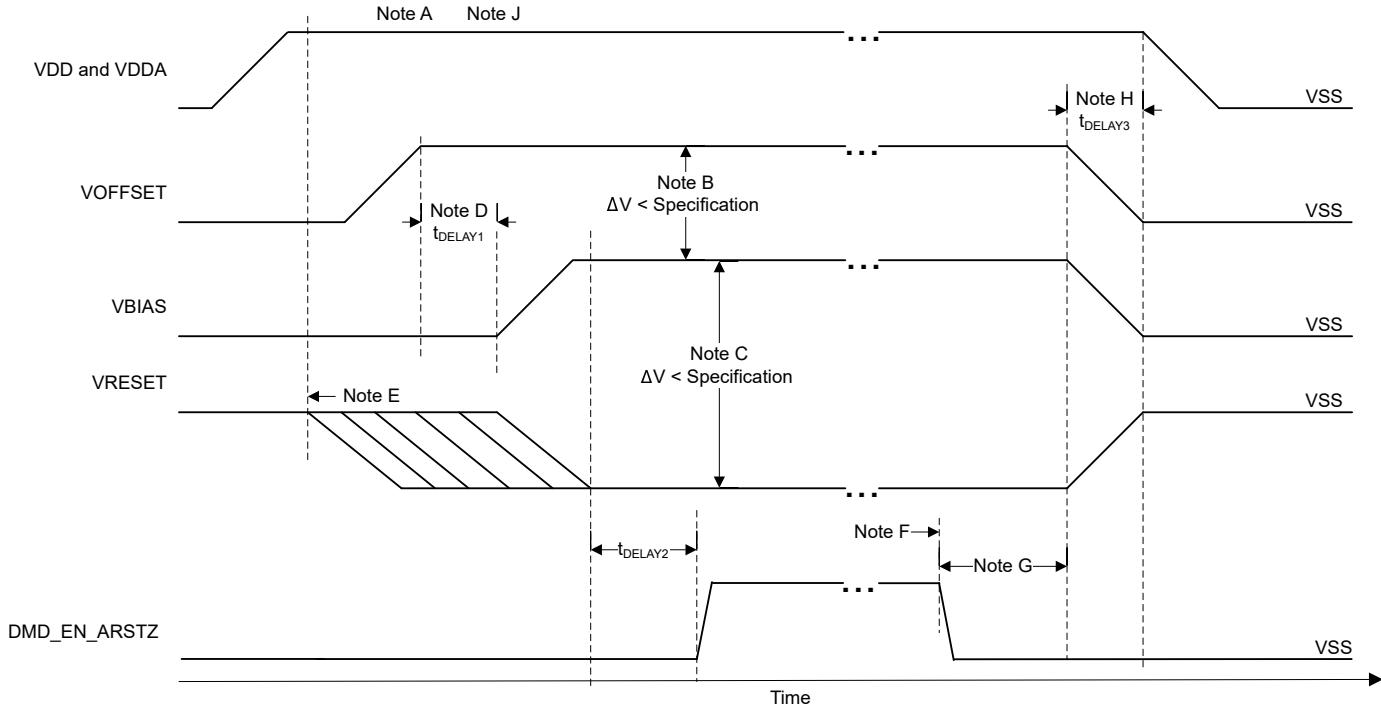
| SYMBOL | PARAMETER | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------------|-------------------|---|-----|-----|-----|---------|
| t_{DELAY1} | Delay requirement | from V_{OFFSET} power up to V_{BIAS} power up | 1 | 2 | | ms |
| t_{DELAY2} | Delay requirement | from V_{BIAS} and V_{RESET} powered on and stable to DMD_EN_ARSTZ going high | 20 | | | μ s |
| t_{DELAY3} | Delay requirement | from V_{OFFSET} , V_{BIAS} , and V_{RESET} powered down to when V_{DD} and V_{DDA} can power down | 50 | | | μ s |

8.2 DMD Power Supply Power-Up Procedure

- During power-up, V_{DD} must always start and settle before V_{OFFSET} plus t_{DELAY1} specified in the *Power Supply Sequence Requirements*, V_{BIAS} , and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} .
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the *Absolute Maximum Ratings*, *Recommended Operating Conditions*, and the *DMD Power Supply Requirements*.
- During power-up, LVCMOS input pins must not be driven high until after V_{DD} has settled at the operating voltage listed in the *Recommended Operating Conditions*.

8.3 DMD Power Supply Power-Down Procedure

- During power-down, V_{DD} must be supplied until after V_{BIAS} , V_{RESET} , and V_{OFFSET} are discharged to within the specified limit of ground. See the *Power Supply Sequence Requirements*.
- During power-down, it is a strict requirement that the voltage difference between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in the *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{BIAS} .
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the *Absolute Maximum Ratings*, the *Recommended Operating Conditions*, and the *DMD Power Supply Requirements*.
- During power-down, LVCMOS input pins must be less than specified in the *Recommended Operating Conditions*.



- A. See the *Pin Functions* table.
- B. To prevent excess current, the supply voltage difference $|V_{BIAS} - V_{OFFSET}|$ must be less than the specified limit in the *Recommended Operating Conditions*.
- C. To prevent excess current, the supply difference $|V_{BIAS} - V_{RESET}|$ must be less than the specified limit in the *Recommended Operating Conditions*.
- D. V_{BIAS} must power up after V_{OFFSET} has powered up, per t_{DELAY1} specification in the *Power Supply Sequence Requirements*.
- E. V_{RESET} , V_{OFFSET} , and V_{BIAS} ramps must start after V_{DD} and V_{DDA} are powered up and stable.
- F. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates DMD_EN_ARSTZ and disables V_{BIAS} , V_{RESET} , and V_{OFFSET} .
- G. Under power-loss conditions, where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, DMD_EN_ARSTZ goes low.
- H. V_{DD} must remain powered on and stable until after V_{OFFSET} , V_{BIAS} , and V_{RESET} are powered off, per t_{DELAY3} specification in the *Power Supply Sequence Requirements*.
- I. To prevent excess current, the supply voltage delta $|V_{DDA} - V_{DD}|$ must be less than the specified limit in the *Recommended Operating Conditions*.
- J. Not to scale. Details are omitted for clarity.

Figure 8-1. DMD Power Supply Requirements

9 Layout

9.1 Layout Guidelines

The DLP651NE DMD is part of a chipset that is controlled by the [DLPC7530](#) display controller in conjunction with the [TPS65145](#) PMIC and the [DLPA100](#) power and motor controller. These guidelines are targeted at designing a PCB board with the DLP651NE DMD. The DMD board is a high-speed multi-layer PCB, with primarily high-speed digital logic, including double data rate 3.2Gbps and 250Mbps differential data buses run to the DMD. TI recommends that full or mini power planes be used for V_{OFFSET} , V_{RESET} , and V_{BIAS} . Solid planes are required for ground (V_{SS}). The target impedance for the PCB is $50\Omega \pm 10\%$ with exceptions listed in [Table 9-1](#). TI recommends a 10-layer stack-up as described in [Table 9-2](#). TI recommends manufacturing the PCB with a high-quality FR-4 material.

9.2 Impedance Requirements

TI recommends a target impedance for the PCB of $50\Omega \pm 10\%$ for all signals. The exceptions are listed in [Table 9-1](#).

Table 9-1. Special Impedance Requirements

| SIGNAL TYPE | SIGNAL NAME | IMPEDANCE (Ω) |
|---------------------------------|---|--|
| DMD High Speed Data Signals | DMD_HSSI0_N_(0...7), DMD_HSSI0_P_(0...7), DMD_HSSI1_N_(0...7), DMD_HSSI1_P_(0...7), DMD_HSSI0_CLK_N, DMD_HSSI0_CLK_P, DMD_HSSI1_CLK_N, DMD_HSSI1_CLK_P | 100 Ω differential (50 Ω single ended) |
| DMD Low Speed Interface Signals | DMD_LS0_WDATA_N, DMD_LS0_WDATA_P, DMD_LS0_CLK_N, DMD_LS0_CLK_P | 100 Ω differential (50 Ω single ended) |

9.3 Layers

[Table 9-2](#) shows the layer stack-up and copper weight for each layer.

Table 9-2. Layer Stack-Up

| LAYER NO. | LAYER NAME | COPPER WT. (oz.) | COMMENTS |
|-----------|---|--------------------------|--|
| 1 | Side A—DMD, primary components, power mini-planes | 0.5 oz. (before plating) | DMD and escapes. Two data input connectors. Top components including power generation and two data input connectors. Low frequency signals routing. Should have copper fill (GND) plated up to 1 oz. |
| 2 | Ground | 0.5 | Solid ground plane (net GND) reference for signal layers #1, 3 |
| 3 | Signal (high frequency) | 0.5 | High speed signal layer. High speed differential data busses from input connector to DMD |
| 4 | Ground | 0.5 | Solid ground plane (net GND) reference for signal layers #3, #5 |
| 5 | Power | 0.5 | Primary split power planes for 1.8 V, 3.3 V, 10 V, -14 V, 18 V |
| 6 | Power | 0.5 | Primary split power planes for 1.8 V, 3.3 V, 10 V, -14 V, 18 V |
| 7 | Ground | 0.5 | Solid ground plane (net GND) reference for signal layer #8 |
| 8 | Signal (high frequency) | 0.5 | High speed signal layer. High speed differential data busses from input connector to DMD |
| 9 | Ground | 0.5 | Solid ground plane (net GND) Reference for signal layers #8, 10 |
| 10 | Side B—Secondary components, power mini-planes | 0.5 oz. (before plating) | Discrete components if necessary. Low frequency signals routing. Should be copper fill plated up to 1 oz. |

9.4 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005"/0.015" (Trace-Width/Spacing) design rule. Use an analysis of impedance and stack-up requirements to determine and calculate actual trace widths.

Maximize the width of all voltage signals as space permits. Follow the width and spacing requirements listed in [Table 9-3](#).

Table 9-3. Special Trace Widths, Spacing Requirements

| SIGNAL NAME | MINIMUM TRACE WIDTH (MIL) | MINIMUM TRACE SPACING (MIL) | LAYOUT REQUIREMENT |
|---------------------|---------------------------|-----------------------------|---|
| GND | MAXIMIZE | 5 | Maximize trace width to connecting pin as a minimum. |
| P3P3V | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias. |
| P1P8V | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary with multiple vias. |
| V _{OFFSET} | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary. |
| V _{RESET} | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary. |
| V _{BIAS} | 40 | 15 | Create mini planes on layers 1 and 10 as needed. Connect to devices on layers 1 and 10 as necessary. |

9.5 Power

TI strongly discourages signal routing on power planes or on planes adjacent to power planes. If signals must be routed on layers adjacent to power planes, they must not cross splits in power planes to prevent EMI and preserve signal integrity.

Connect all internal digital ground (GND) planes in as many places as possible. Connect all internal ground planes with a minimum distance between connections of 0.5". Extra vias may not be required if there are sufficient ground vias due to normal ground connections of devices.

Connect power and ground pins of each component to the power and ground planes with at least one via for each pin. Minimize trace lengths for component power and ground pins. (ideally, less than 0.100").

Ground plane slots are strongly discouraged.

9.6 Trace Length Matching Recommendations

[Table 9-4](#) and [Table 9-5](#) describe recommended signal trace length matching requirements. Follow these guidelines to avoid routing long traces over large areas of the PCB:

- Match the trace lengths so that longer signals route in a serpentine pattern
- Minimize the number of turns.
- Ensure that the turn angles are no sharper than 45 degrees.

[Figure 9-1](#) shows an example of the HSSI signal pair routing.

Signals listed in [Table 9-4](#) are specified for data rate operation at up to 3.2Gbps. Minimize the layer changes for these signals. Minimize the number of vias. Avoid sharp turns and layer switching while minimizing the lengths. When layer changes are necessary, place GND vias around the signal vias to provide a signal return path. The distance from one pair of differential signals to another must be at least two times the distance within the pair.

Table 9-4. HSSI High Speed DMD Data Signals

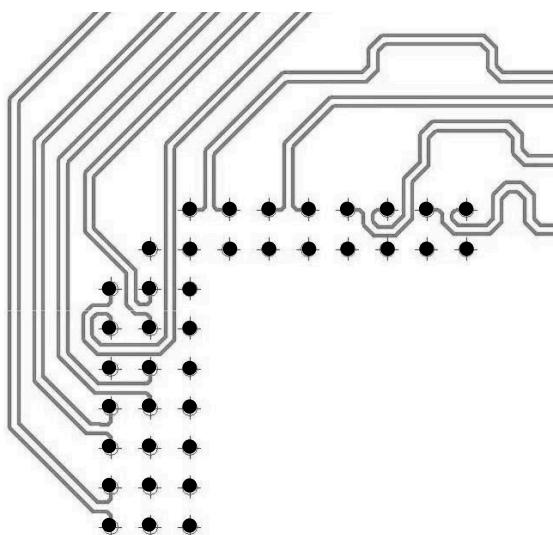
| SIGNAL NAME | REFERENCE SIGNAL | ROUTING SPECIFICATION | UNIT |
|---|------------------------------------|-----------------------|------|
| DMD_HSSI0_N(0...7), DMD_HSSI0_P(0...7) | DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P | ±0.25 | inch |

Table 9-4. HSSI High Speed DMD Data Signals (continued)

| SIGNAL NAME | REFERENCE SIGNAL | ROUTING SPECIFICATION | UNIT |
|---|------------------------------------|-----------------------|------|
| DMD_HSSI1_N(0...7), DMD_HSSI1_P(0...7) | DMD_HSSI0_CLK_N, DMD_HSSI_CLK_P | ± 0.25 | inch |
| DMD_HSSI0_CLK_P | DMD_HSSI1_CLK_P | ± 0.05 | inch |
| Intra-pair P | Intra-pair N | ± 0.01 | inch |

Table 9-5. Other Timing Critical Signals

| SIGNAL NAME | CONSTRAINTS | ROUTING LAYERS |
|---|---|----------------|
| LS_CLK_P, LS_CLK_N LS_WDATA_P, LS_WDATA_N LS_RDATA_A | Intra-pair (P to N) Matched to 0.01 inches Signal-to-signal Matched to +/- 0.25 inches | Layers 3, 8 |


Figure 9-1. Example HSSI PCB Routing

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Device Support

10.2.1 Device Nomenclature

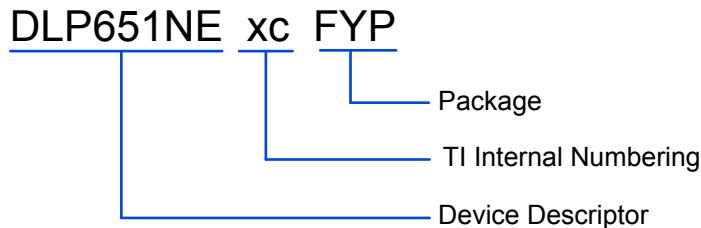


Figure 10-1. Part Number Description

10.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in [Figure 10-2](#). The 2-dimensional matrix code is an alpha-numeric string that contains the DMD part number, Part 1 and Part 2 of the serial number.

Example:

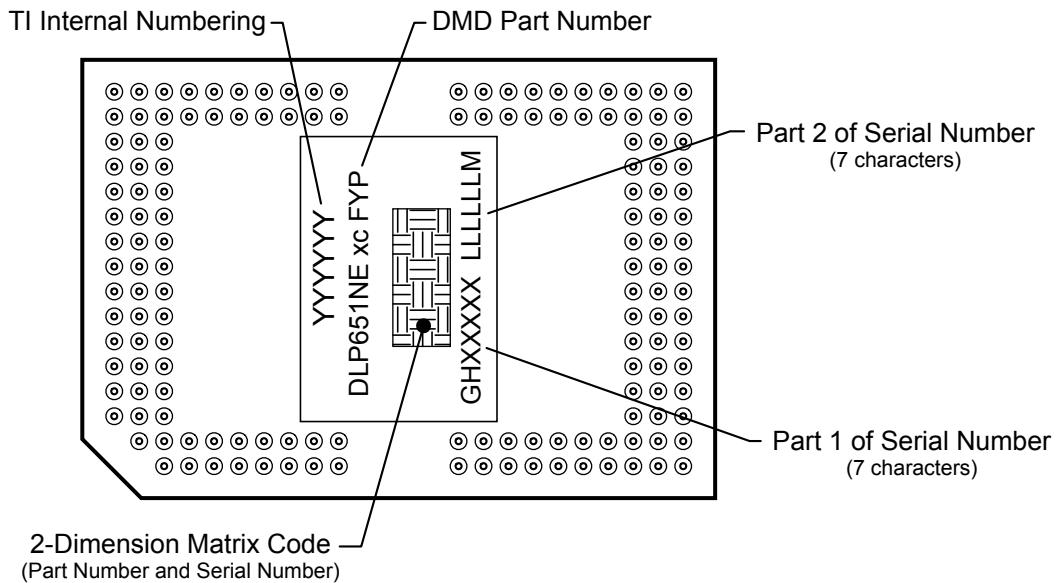


Figure 10-2. DMD Marking Locations

10.3 Documentation Support

10.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- [DLPC7530 Display Controller Data Sheet](#)

- [TPS65145 Data Sheet](#)
- [DLPA100 Power and Motor Driver Data Sheet](#)

10.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.

DLP® is a registered trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (January 2025) to Revision C (September 2025) | Page |
|--|-------------|
| • Updated the <i>Recommended Operating Conditions</i> | 7 |
| • Fixed a device typo in <i>Thermal Information</i> | 9 |
| • Corrected typo in line $Q_{ARRAY}=3.0W + (0.45 \times 48W)=24.6W$ | 23 |

| Changes from Revision A (May 2022) to Revision B (January 2025) | Page |
|--|-------------|
| • Updated the controller to DLPC7530 throughout the document..... | 1 |
| • Added the links to the DLP Products third-party search tools and Getting Started with TI DLP Display Technology..... | 1 |
| • Updated Micromirror Array Optical Characteristics Table..... | 18 |
| • Updated Micromirror Array Temperature Calculation..... | 23 |
| • Added the Micromirror Power Density Calculation section..... | 24 |
| • Added the topic Window Aperture Illumination Overfill Calculation..... | 26 |
| • Updated the equation to calculate the landed duty cycle..... | 27 |
| • Changes to Typical Application re: Laser Phosphor configuration and LED configuration..... | 30 |

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish ⁽⁴⁾ | MSL Peak Temp ⁽³⁾ | Op Temp (°C) | Device Marking ⁽⁵⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|---------------------------------|------------------------------|--------------|---------------------------------|
| DLP651NEA0FYP | ACTIVE | CPGA | FYP | 149 | 33 | RoHS & Green | Call TI | Call TI | | see Figure 10-2 |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|------------------|--------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| DLP651NEA0FYP | Active | Production | CPGA (FYP) 149 | 33 JEDEC TRAY (5+1) | Yes | NIAU | N/A for Pkg Type | 0 to 70 | |
| DLP651NEA0FYP.A | Active | Production | CPGA (FYP) 149 | 33 JEDEC TRAY (5+1) | Yes | NIAU | N/A for Pkg Type | 0 to 70 | |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

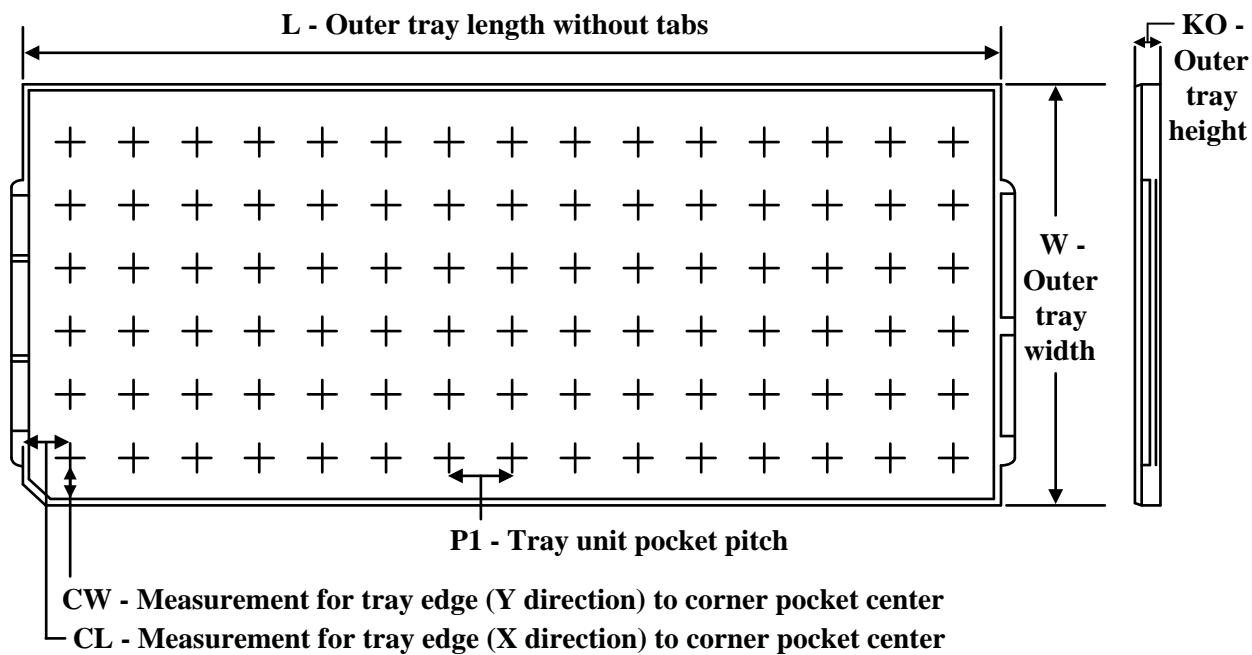
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|-----------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| DLP651NEA0FYP | FYP | CPGA | 149 | 33 | 3 x 11 | 150 | 315 | 135.9 | 12190 | 27.5 | 20 | 27.45 |
| DLP651NEA0FYP.A | FYP | CPGA | 149 | 33 | 3 x 11 | 150 | 315 | 135.9 | 12190 | 27.5 | 20 | 27.45 |

NOTES: UNLESS OTHERWISE SPECIFIED:

- 1 SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
- 2 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
- 3 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
- 4 SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
- 5 BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
- 6 MAXIMUM ENCAPSULANT PROFILE SHOWN
- 7 ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
- 8 SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

© COPYRIGHT 2019 TEXAS INSTRUMENTS UNPUBLISHED, ALL RIGHTS RESERVED.

| REV | DESCRIPTION | DATE | APPROVED |
|-----|------------------------------|----------|--------------|
| A | ECO 2180591, INITIAL RELEASE | 04/04/19 | F. ARMSTRONG |

D

D

C

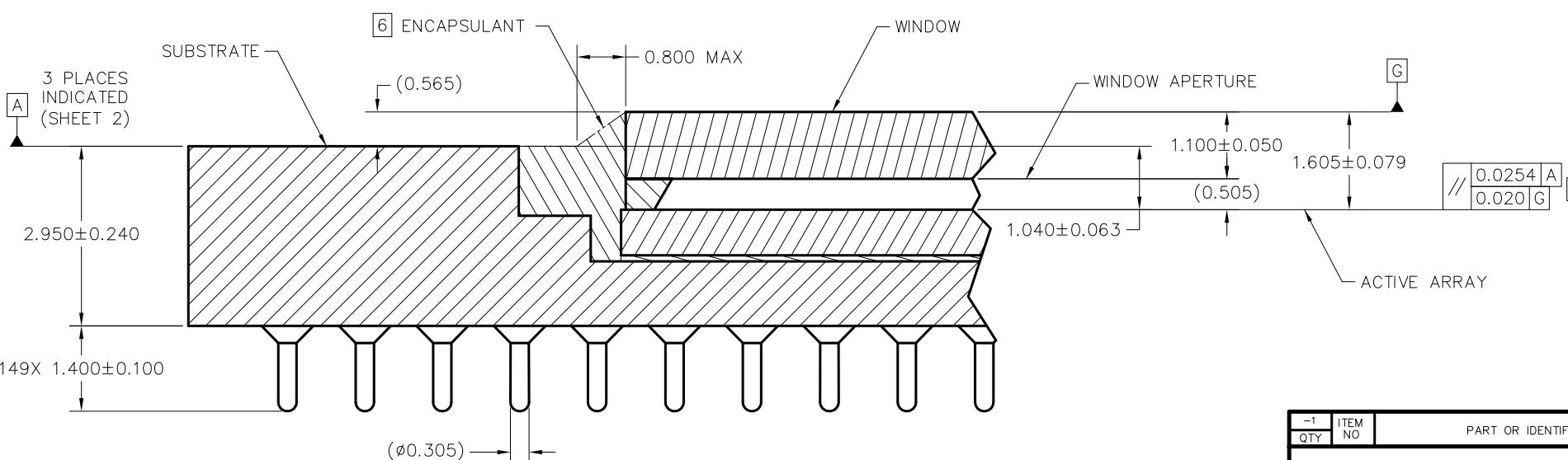
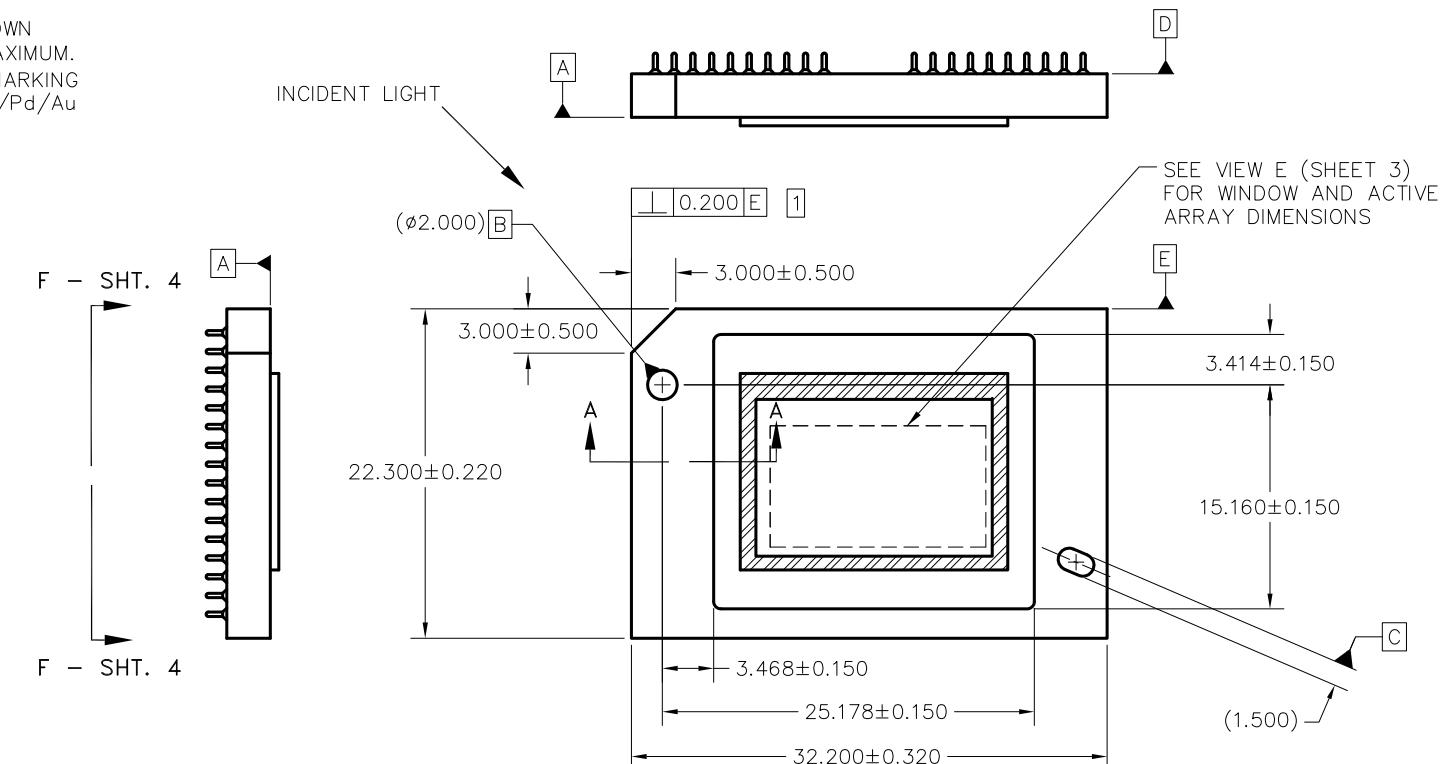
C

B

B

A

A

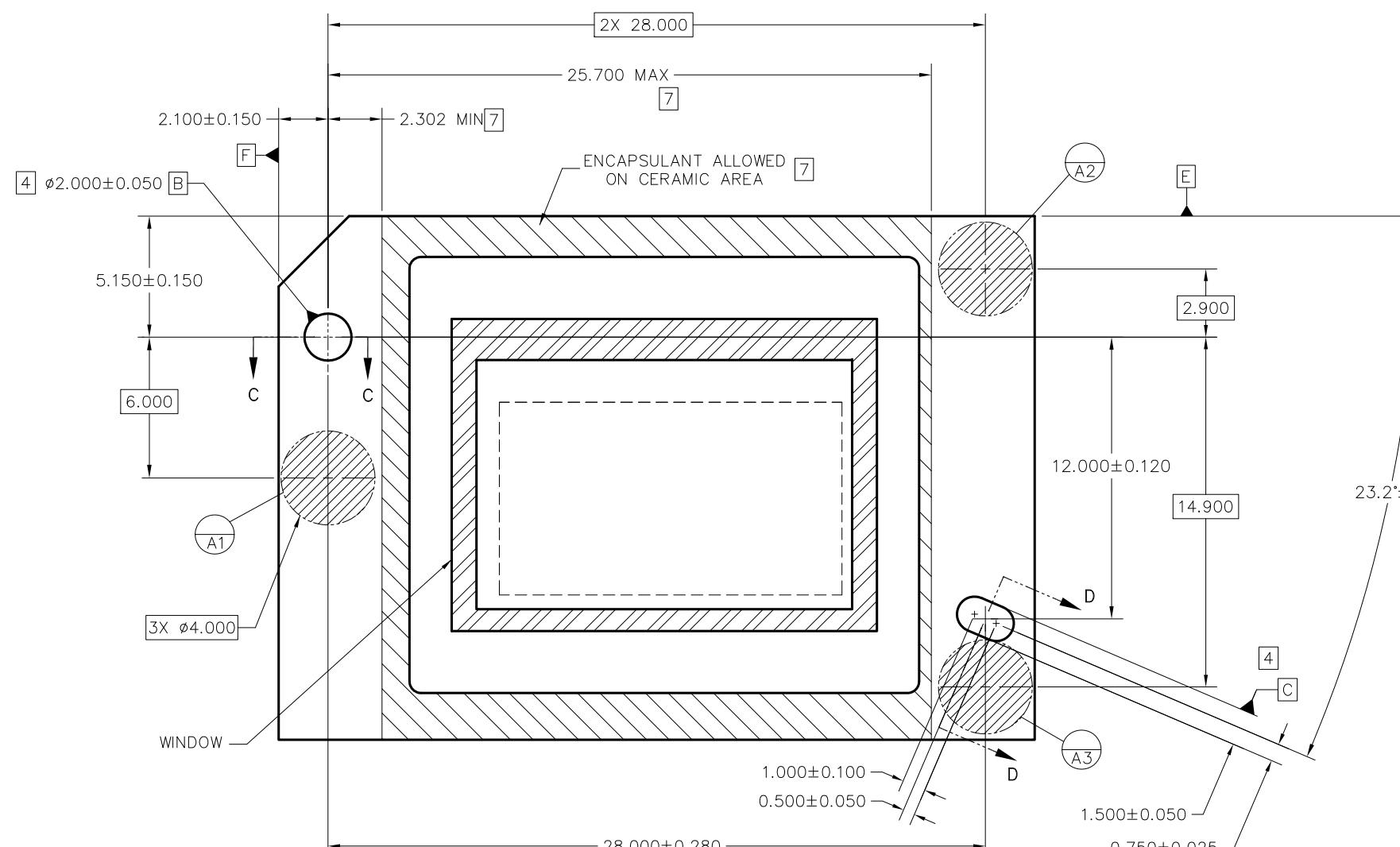
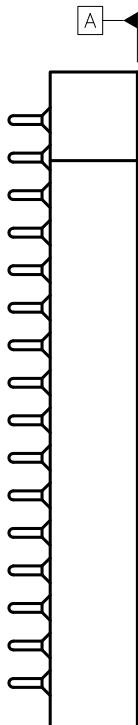


SECTION A-A
SCALE 20/1

| -1 | ITEM QTY | PART OR IDENTIFYING NUMBER | NOMENCLATURE OR DESCRIPTION | NOTES |
|------------|----------|----------------------------|---|--|
| PARTS LIST | | | | |
| | | | UNLESS OTHERWISE SPECIFIED • DIMENSIONS ARE IN MILLIMETERS • TOLERANCES: ANGLES ± 1° • 2 PLACE DECIMALS ± 0.25 • 3 PLACE DECIMALS ± 0.05 • REMOVE ALL BURRS AND SHARP EDGES • INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994 • DIMENSIONAL LIMITS APPLY BEFORE PROCESSES • PARENTHETICAL INFO FOR REF ONLY | |
| | | | ENGR: F. ARMSTRONG 04/04/19 | TEXAS INSTRUMENTS Dallas, Texas |
| | | | QA: S. HUDGENS 04/12/2019 | ICD, MECHANICAL, DMD .65 1080p / UHD HSSI SERIES 450 (FYP PACKAGE) |
| | | | COE: M. DORAK 04/12/2019 | SIZE: D DRAWING NO: 2516609 REV: A |
| | | | SCALE: 4/1 | SHEET: 1 OF 4 |

D

D



D

D

C

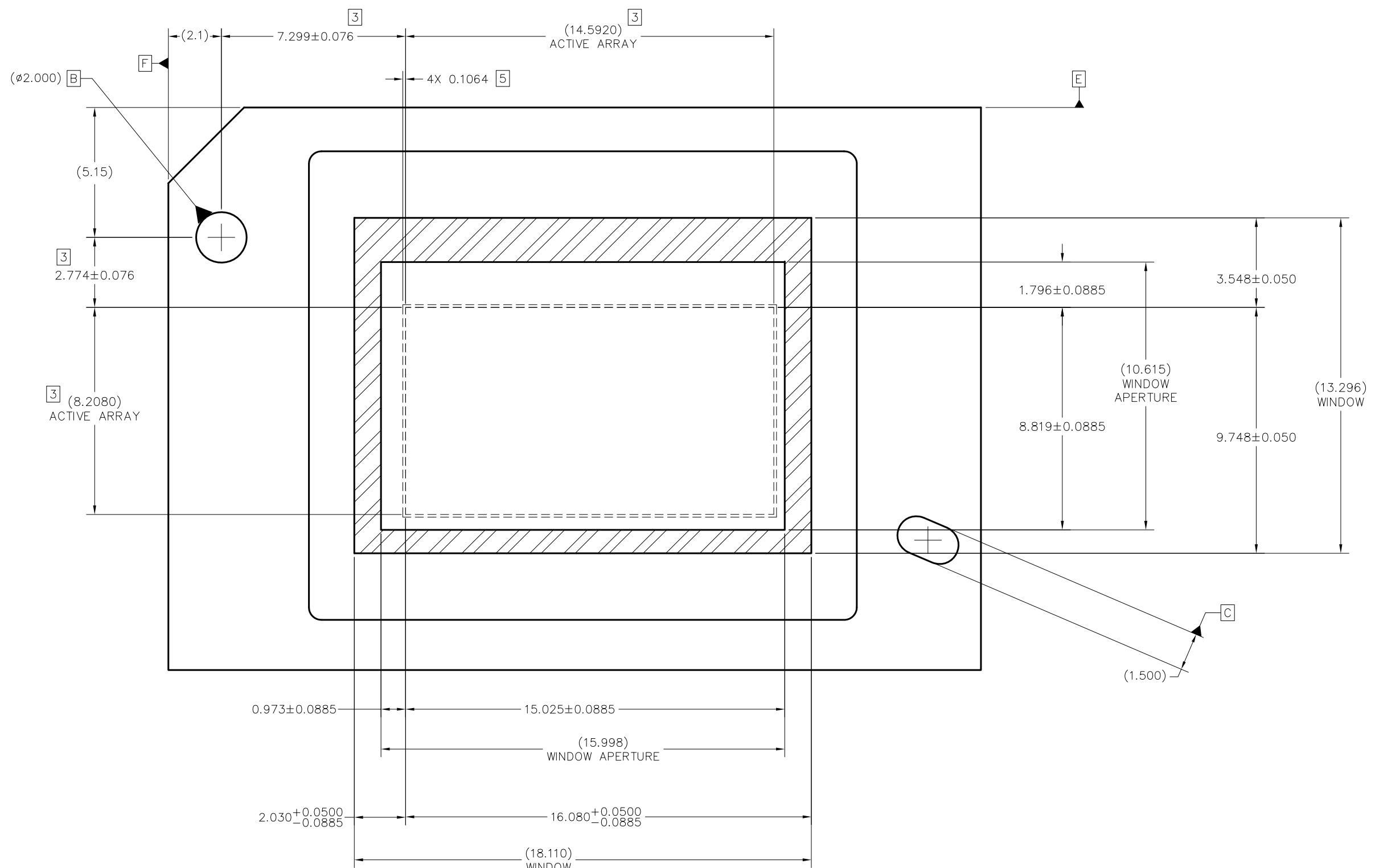
C

B

B

A

A



VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12/1

| TEXAS INSTRUMENTS Dallas, Texas | DATE ISSUE DATE | SIZE D | DRAWING NO 2516609 | REV A |
|------------------------------------|--------------------|-----------|-----------------------|----------|
| | | SCALE 4/1 | | sheet 3 |

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025