

## DLPA300 Driver for DLP Digital Micromirror Devices

### 1 Features

- Designed for the DLP® 9- $\mu$ m pixel digital micromirror devices (DMDs)
  - DLP780NE
  - DLP780TE
  - DLP800RE
  - DLP781NE
  - DLP781TE
  - DLP801RE
  - DLP801XE
- Generates the micromirror clocking pulses the 9- $\mu$ m pixel DMDs require
- Generates specialized voltage levels required for micromirror clocking pulses

### 2 Applications

- Enterprise projector
- Smart projector
- Laser TV
- Digital signage
- Large venue projector
- ProAV projector

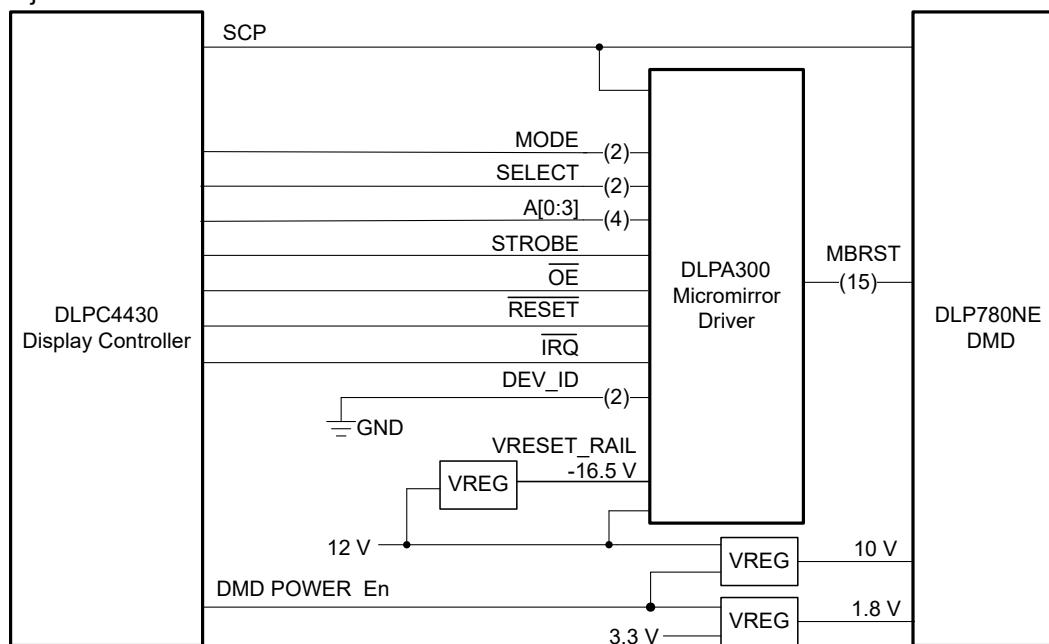
### 3 Description

The DLPA300 device is a micromirror driver for the DLP 9- $\mu$ m pixel, high-efficiency digital micromirror devices (DMDs), which include the DLP780NE, DLP780TE, DLP800RE, DLP781NE, DLP781TE, DLP801RE, and DLP801XE DMDs. A part of these DMD chipsets, the DLPA300 micromirror driver generates the  $V_{OFFSET}$  and  $V_{BIAS}$  voltages. It also switches  $V_{OFFSET}$ ,  $V_{BIAS}$ , and an externally generated  $V_{RESET}$  to create the micromirror clocking pulses for the DLP DMDs. Either the TI DLPC4420 or DLPC4430 display controller manages the timing of this waveform.

#### Device Information

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE
DLPA300	HTQFP (80)	14.00 mm × 14.00 mm

(1) For all available packages, see the orderable addendum at the end of this data sheet.



Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2021) to Revision A (June 2023)	Page
• Updated <a href="#">Features</a> for new DMDs.....	<a href="#">1</a>
• Updated <a href="#">Applications</a> .....	<a href="#">1</a>
• Updated <a href="#">Description</a> for new DMDs.....	<a href="#">1</a>
• Added minimum value to $V_{IN}$ in <a href="#">Absolute Maximum Ratings</a> .....	<a href="#">6</a>
• Updated $F_{SW}$ in <a href="#">Bias Voltage Boost Converter</a> .....	<a href="#">8</a>
• Deleted Discharge time constant in <a href="#">V<sub>OFFSET</sub> Regulator</a> .....	<a href="#">9</a>
• Added Discharge current sink in <a href="#">V<sub>OFFSET</sub> Regulator</a> .....	<a href="#">9</a>
• Updated <a href="#">Overview</a> .....	<a href="#">12</a>
• Updated drawing for proper logic polarity in <a href="#">Functional Block Diagram</a> .....	<a href="#">13</a>
• Updated switching frequency in <a href="#">Bias Voltage Boost Converter</a> .....	<a href="#">14</a>
• Updated <a href="#">Bias Voltage Boost Converter</a> for new DMDs.....	<a href="#">14</a>
• Updated <a href="#">V<sub>OFFSET</sub> Regulator</a> for new DMDs.....	<a href="#">15</a>
• Updated <a href="#">Application Information</a> .....	<a href="#">17</a>
• Updated <a href="#">Typical Application</a> .....	<a href="#">17</a>
• Updated <a href="#">Design Requirements</a> .....	<a href="#">18</a>
• Corrected minor typos in <a href="#">Detailed Design Procedure</a> .....	<a href="#">19</a>

## 5 Pin Configuration and Functions

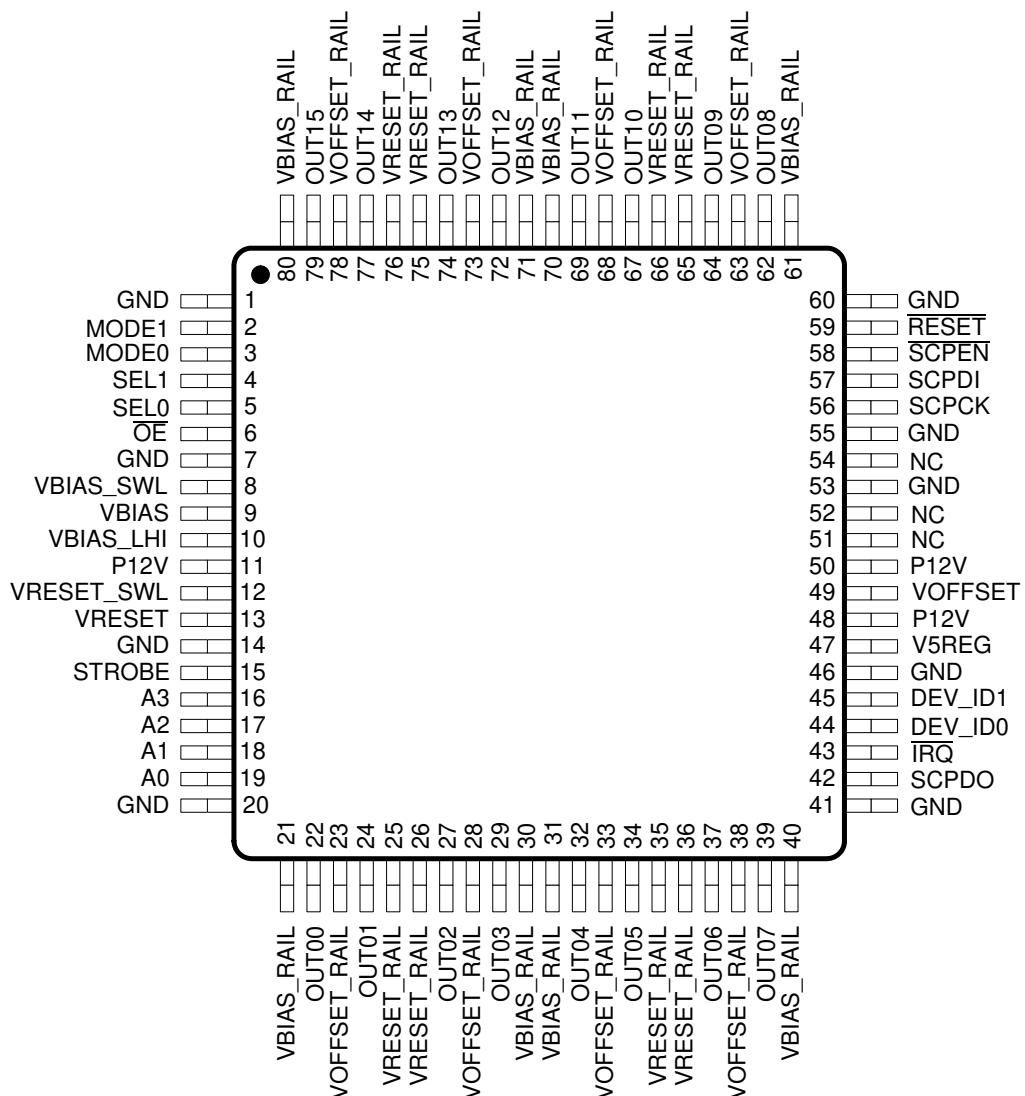


Figure 5-1. PFP Package 80-Pin HTQFP Top View

**Table 5-1. Package Pinout**

PIN		I/O (INPUT DEFAULT)	DESCRIPTION
NAME	NO.		
OUT00	22	Output	16 micromirror clocking waveform outputs (enabled by $\overline{OE} = 0$ )
OUT01	24	Output	
OUT02	27	Output	
OUT03	29	Output	
OUT04	32	Output	
OUT05	34	Output	
OUT06	37	Output	
OUT07	39	Output	
OUT08	62	Output	
OUT09	64	Output	
OUT10	67	Output	
OUT11	69	Output	
OUT12	72	Output	
OUT13	74	Output	
OUT14	77	Output	
OUT15	79	Output	
A0	19	Input (pulldown)	Output Address. Used to select which OUTxx pin is active at a given time
A1	18	Input (pulldown)	
A2	17	Input (pulldown)	
A3	16	Input (pulldown)	
MODE0	3	Input (pulldown)	Mode Select. Used to determine the operating mode of the DLPA300
MODE1	2	Input (pulldown)	
SEL0	5	Input (pulldown)	Output Voltage Select. Used to switch the voltage applied to the addressed OUTxx pin
SEL1	4	Input (pulldown)	
STROBE	15	Input (pulldown)	A rising edge on STROBE latches in the control signals after a tristate delay
$\overline{OE}$	6	Input (pullup)	Asynchronous input controls whether the 16 OUTxx pins are active or are in a high-impedance state. $\overline{OE} = 0$ : Enabled. $\overline{OE} = 1$ : High Z
RESET	59	Input (pullup)	Resets the DLPA300 internal logic. Active low. Asynchronous
SCPEN	58	Input (pullup)	Enables serial bus data transfers. Active low
SCPDI	57	Input (pull down)	Serial bus data input. Clocked in on the falling edge of SCPCK
SCPCK	56	Input (pull down)	Serial bus clock. Provided by chipset controller
SCPDO	42	Output	Serial bus data output (open drain). Clocked out on the rising edge of SCPCK. A 1-k $\Omega$ pullup resistor to the chip-set controller $V_{DD}$ supply is recommended.
IRQ	43	Output	Interrupt request output to the chipset Controller. Active low. A 1-k $\Omega$ pullup resistor to the chip-set controller $V_{DD}$ supply is recommended.
DEV_ID1	45	Input (pullup)	Serial bus device address: 00 = all; 01 = device 1; 10 = device 2; 11 = device 3
DEV_ID0	44	Input (pullup)	
VBIAS	9	Output	One of three specialized voltages the DLPA300 generates
VBIAS_LHI	10	Input	Current limiter output for VBIAS supply (also the VBIAS switching inductor input)
VBIAS_SWL	8	Input	Connection point for VBIAS supply switching inductor
VBIAS_RAIL	21, 30, 31, 40, 61, 70, 71, 80	Input	The internally used VBIAS supply rail. Internally isolated from VBIAS
VRESET	13	No Connect	This pin is unused by the DLPA300.

**Table 5-1. Package Pinout (continued)**

PIN		I/O (INPUT DEFAULT)	DESCRIPTION
NAME	NO.		
VRESET_SWL	12	No Connect	This pin is unused by the DLPA300.
VRESET_RAIL <sup>(1)</sup>	25, 26, 35, 36, 65, 66, 75, 76	Input	The internally-used VRESET supply rail. Internally isolated from VRESET. The external VRESET supply is connected to this pin. The package thermal pad is tied to this voltage level. <sup>(1)</sup>
VOFFSET	49	Output	One of three specialized voltages the DLPA300 generates
VOFFSET_RAIL	23, 28, 33, 38, 63, 68, 73, 78	Input	The internally-used VOFFSET supply rail. Internally isolated from VOFFSET
GND	1, 7, 14, 20, 41, 46, 53, 55, 60	GND	Common ground
V5REG	47	Output	The 5-V logic supply output
P12V	11, 48, 50	Input	The main power input to the DLPA300
NC	51, 52, 54	No Connect	No connect

(1) Exposed thermal pad is internally connected to VRESET\_RAIL.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
<b>ELECTRICAL</b>					
P12V	Load supply voltage			14	V
VRESET_SWL	Reset supply switching inductor connection point	(VRESET_SWL-VRESET_RAIL)		-1	V
VBIAS_RAIL	Internally-used V <sub>BIAS</sub> supply rail	(VBIAS_RAIL-VRESET_RAIL)		60	V
VOFFSET_RAIL	Internally-used V <sub>OFFSET</sub> supply rail	(VOFFSET_RAIL-VRESET_RAIL)		40.5	V
V <sub>IN</sub>	Logic inputs		-0.3	7	V
V <sub>OUT</sub>	Open drain logic outputs			7	V
<b>ENVIRONMENTAL</b>					
T <sub>J(max)</sub>	Maximum junction temperature			125	°C
T <sub>A</sub>	Operating temperature		0	75	°C
T <sub>stg</sub>	Storage temperature		-55	150	°C

(1) Stresses beyond those listed under [Section 6.1](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM) <sup>(1)</sup>	±2000	V
		Charged device model (CDM) <sup>(2)</sup>	800	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

at T<sub>A</sub> = 25°C, P12V = 10.8 V to 13.2 V (unless otherwise noted)<sup>(2)</sup>

		POWER	MIN	NOM	MAX	UNIT
I <sub>P12V1</sub>	P12V supply current <sup>(1)</sup>	Global shadow at 50 kHz, OUT load = 39 Ω and 410 pF, V <sub>5REG</sub> = 30 mA, V <sub>BIAS</sub> = 21 V at 5 mA, V <sub>OFFSET</sub> = 10 V at 30 mA		200		mA
		Outputs disabled and no external loads, V <sub>BIAS</sub> = 21 V, V <sub>OFFSET</sub> = 4.5 V		22		mA
T <sub>JTSDR</sub>	Thermal shutdown temperature	With device temperature rising	145	160	175	°C
		Hysteresis	5	10	15	°C
T <sub>JTWR</sub>	Thermal warning temperature		5	10	15	°C
		With device temperature rising	125	140	155	°C
		Hysteresis	5	10	15	°C

(1) During power up the inrush power supply current can be as high as 1 A for a momentary period of time.

(2) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DLPA300	UNIT
		PFP (HTQFP)	
		80 PINS	
$R_{c-j}$	Thermal resistance	3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics Control Logic

$T_A = 25^\circ\text{C}$ ,  $\text{P12V} = 10.8 \text{ V}$  to  $13.2 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL}$ Low-level logic input voltage				0.8	V
$V_{IH}$ High-level logic input voltage			1.97		V
$I_{IH}$ High-level logic input current	$V_{IN} = 5 \text{ V}$ , input with pulldown. See terminal functions table.		40	50	$\mu\text{A}$
$I_{IL}$ Low-level logic input current	$V_{IN} = 0 \text{ V}$ , input with pullup. See terminal functions table.	-50	-40		$\mu\text{A}$
$I_{IH}$ High-level logic input leakage current	$V_{IN} = 0 \text{ V}$ , input with pulldown	-1		1	$\mu\text{A}$
$I_{IL}$ Low-level logic input leakage current	$V_{IN} = 5 \text{ V}$ , input with pullup	-1		1	$\mu\text{A}$
$V_{OL}$ Open drain logic outputs	$I = 4 \text{ mA}$			0.4	V
$I_{OL}$ Logic output leakage current	$V = 3.3 \text{ V}$			1	$\mu\text{A}$

## 6.6 5-V Linear Regulator

$T_A = 25^\circ\text{C}$ ,  $\text{P12V} = 10.8\text{ V}$  to  $13.2\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{5\text{REG}}$	Output voltage	Average voltage, $I_{\text{OUT}} = 4\text{ mA}$ to $50\text{ mA}$	4.75	5	5.25	V
$I_{\text{IL}}$	Output current: internal logic		4		20	mA
$I_{\text{IE}}$	Output current: external circuitry		0		30	mA
$I_{\text{CL5}}$	Current limit		80			mA
$V_{\text{UV5}}$	Undervoltage threshold	$I_{\text{OUT}} = 50\text{ mA}$	V5REG voltage increasing, $\text{P12V} = 5.4\text{ V}$	4.1		V
			V5REG voltage falling, $\text{P12V} = 5.2\text{ V}$	3.9		
$V_{\text{RIP}}$	Output ripple voltage <sup>(1)</sup>			200		mVpk-pk
$V_{\text{OS5}}$	Voltage overshoot at start up			2		%V5REG
$t_{\text{ss}}$	Power up	Measured between 10 to 90% of V5REG		1		ms

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

## 6.7 Bias Voltage Boost Converter

$T_A = 25^\circ\text{C}$ ,  $\text{P12V} = 10.8\text{ V}$  to  $13.2\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{\text{RL}}$	Output current: reset outputs	Load = $400\text{pF}$ , $39\text{ }\Omega$ , repetition frequency = $50\text{ kHz}$	0		18	mA
$I_{\text{QL}}$	Output current: quiescent / drivers	Load = $400\text{ pF}$ , $39\text{ }\Omega$ , repetition frequency = $50\text{ kHz}$			3	mA
$I_{\text{DL}}$	Output current: DMD load		0		5	mA
$I_{\text{CLFB}}$	Current limit flag	Corresponding current on output at $\text{P12V} = 10.8\text{ V}$	30			mA
$I_{\text{CLB}}$	Current limit	Measured on input	330	376	460	mA
$V_{\text{BIAS}}$	Output voltage		20.5	21	21.5	V
$V_{\text{UVB}}$	$V_{\text{BIAS}}$ undervoltage threshold	Bias voltage falling	50		92	%VBIAS
$V_{\text{UVLHI}}$	$V_{\text{BIAS\_LHI}}$ undervoltage threshold	$V_{\text{BIAS\_LHI}}$ voltage increasing		8		V
		$V_{\text{BIAS\_LHI}}$ voltage falling		6.5		V
$R_{\text{DS}}$	Boost switch $R_{\text{DS(on)}}$	$T_J = 25^\circ\text{C}$		2		$\Omega$
$V_{\text{RIP}}$	Output ripple voltage <sup>(1)</sup>			200		mVpk-pk
$F_{\text{SW}}$	Switching frequency		1.1	1.3	1.5	MHz
$V_{\text{OSB}}$	Voltage overshoot at start up			2		%VBIAS
$t_{\text{ss}}$	Power up	$C_{\text{OUT}} = 3.3\text{ }\mu\text{F}$ , Measured between 10 to 90% of target $V_{\text{BIAS}}$		1		ms
$t_{\text{dis}}$	Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

## 6.8 Reset Voltage Buck-Boost Converter

This is feature is not used in the DLPA300.

## 6.9 $V_{OFFSET}$ Regulator

$T_A = 25^\circ\text{C}$ ,  $\text{P12V} = 10.8\text{ V}$  to  $13.2\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{RL}$ Output current: reset outputs	Load = 400 pF, 39 $\Omega$ , repetition frequency = 50 kHz	0		12.2	mA
$I_{QL}$ Output current: quiescent / drivers	Load = 400 pF, 39 $\Omega$ , repetition frequency = 50 kHz			3	mA
$I_{DL}$ Output current		0		30	mA
$I_{CLO}$ Current limit		100			mA
$V_{OFFSET}$ Output Voltage		9.75	10	10.25	V
$V_{UVO}$ Undervoltage threshold	$V_{OFFSET}$ voltage falling	50		92	% $V_{OFFSET}$
$V_{RIP}$ Output ripple voltage <sup>(1)</sup>			100		mVpk-pk
$V_{OSO}$ Voltage overshoot at start-up			2		% $V_{OFFSET}$
$t_{ss}$ Power up	$C_{OUT} = 4.7\text{ }\mu\text{F}$ , Measured between 10 to 90% of target $V_{OFFSET}$		1		ms
$I_{dis}$ Discharge current sink		400			mA

(1) Output ripple voltage relies on suitable external components being selected and good printed circuit board layout practice.

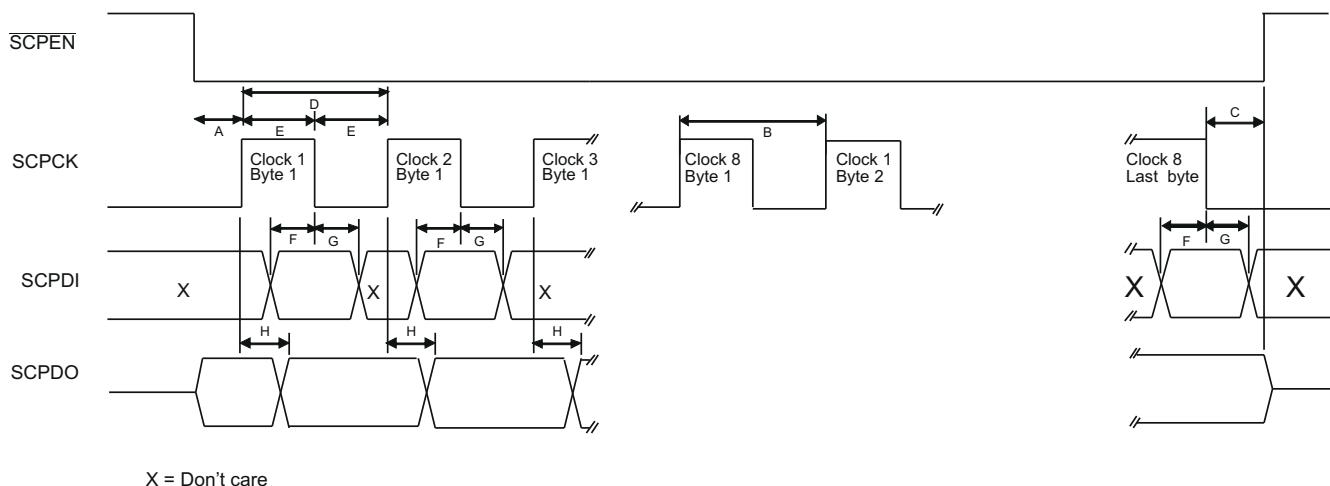
## 6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SERIAL COMMUNICATION PORT INTERFACE</b>					
A <sup>(1)</sup>	Setup SCPEN low to SCPCK	360			ns
B <sup>(1)</sup>	Byte to byte delay	1.9			μs
C <sup>(1)</sup>	Setup SCPDI to SCPEN high	360			ns
D <sup>(1)</sup>	SCPCK frequency <sup>(2)</sup>	0	526		kHz
	SCPCK period	1.9	2		μs
E <sup>(1)</sup>	SCPCK high or low time	300			ns
F <sup>(1)</sup>	SCPDI set-up time	300			ns
G <sup>(1)</sup>	SCPDI hold time	300			ns
H <sup>(1)</sup>	SCPDO propagation delay	300			ns
	SCPEN, SCPCK, SCPDI, RESET filter (pulse reject)	150			ns
<b>OUTPUT MICROMIRROR CLOCKING PULSES</b>					
F <sub>PREP</sub>	Phased reset repetition frequency each output pin (non-overlapping)		50		kHz
F <sub>GREP</sub>	Global reset repetition frequency all output pins		50		kHz
I <sub>RLK</sub>	V <sub>RESET</sub> output leakage current	OE = 1, V <sub>RESET_RAIL</sub> = -28.5V	-1	-10	μA
I <sub>BLK</sub>	V <sub>BIAS</sub> output leakage current	OE = 1, V <sub>BIAS_RAIL</sub> = 28.5V	1	10	μA
I <sub>OLK</sub>	V <sub>OFFSET</sub> output leakage current	OE = 1, V <sub>OFFSET_RAIL</sub> = 10.25V	1	10	μA
<b>OUTPUT MICROMIRROR CLOCKING PULSE CONTROLS</b>					
t <sub>SPW</sub>	STROBE pulse width		10		ns
t <sub>SP</sub>	STROBE period		20		ns
t <sub>OHz</sub>	Output time to high impedance	OE Pin = High		100	ns
t <sub>OEN</sub>	Output enable time from high impedance	OE Pin = Low		100	ns
t <sub>SUS</sub>	Set-up time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8		ns
t <sub>HOS</sub>	Hold time	From A[3:0], MODE[1:0], and SEL[1:0] to STROBE edge	8		ns
t <sub>PBR</sub>	Propagation time	From STROBE to V <sub>BIAS</sub> /V <sub>RESET</sub> edge 50% point.	80	200	ns
t <sub>PRO</sub>		From STROBE to V <sub>RESET</sub> /V <sub>OFFSET</sub> edge 50% point.	80	200	ns
t <sub>POB</sub>		From STROBE to V <sub>OFFSET</sub> /V <sub>BIAS</sub> edge 50% point.	80	200	ns
t <sub>DEL</sub>	Edge-to-edge propagation delta	Maximum difference between the slowest and fastest propagation times for any given reset output.		40	ns
t <sub>CHCH</sub>	Output channel-to-channel propagation delta	Maximum difference between the slowest and fastest propagation times for any two outputs for any given edge.		20	ns

(1) See [Figure 6-1](#)

(2) There is no minimum speed for the serial port. It can be written to statically for diagnostic purposes.



**Figure 6-1. Serial Interface Timing**

## 7 Detailed Description

### 7.1 Overview

The DLPA300 is a micromirror driver for the 9- $\mu$ m pixel family of DMDs. These include the DLP780NE, DLP800RE, DLP780TE, DLP781NE, DLP781TE, DLP801RE and DLP801XE DMDs. The DLPA300 micromirror driver generates  $V_{OFFSET}$  and  $V_{BIAS}$  voltages required by the DMD.  $V_{RESET}$  for the DMDs is generated by an external voltage regulator. Under the control of the DLPC4430 (or DLPC4420) display controller, the DLPA300 micromirror driver switches these three voltage supplies to control the micromirror reset waveform via the MBRST pins on the DMD.

Reliable function and operation of the DLPA300 micromirror driver require that it is used as part of the family of 9- $\mu$ m pixel DMD chipsets. For LED and RGB direct laser illumination, the DLPA100 can be replaced by discrete power supply ICs and a power supply sequencer.

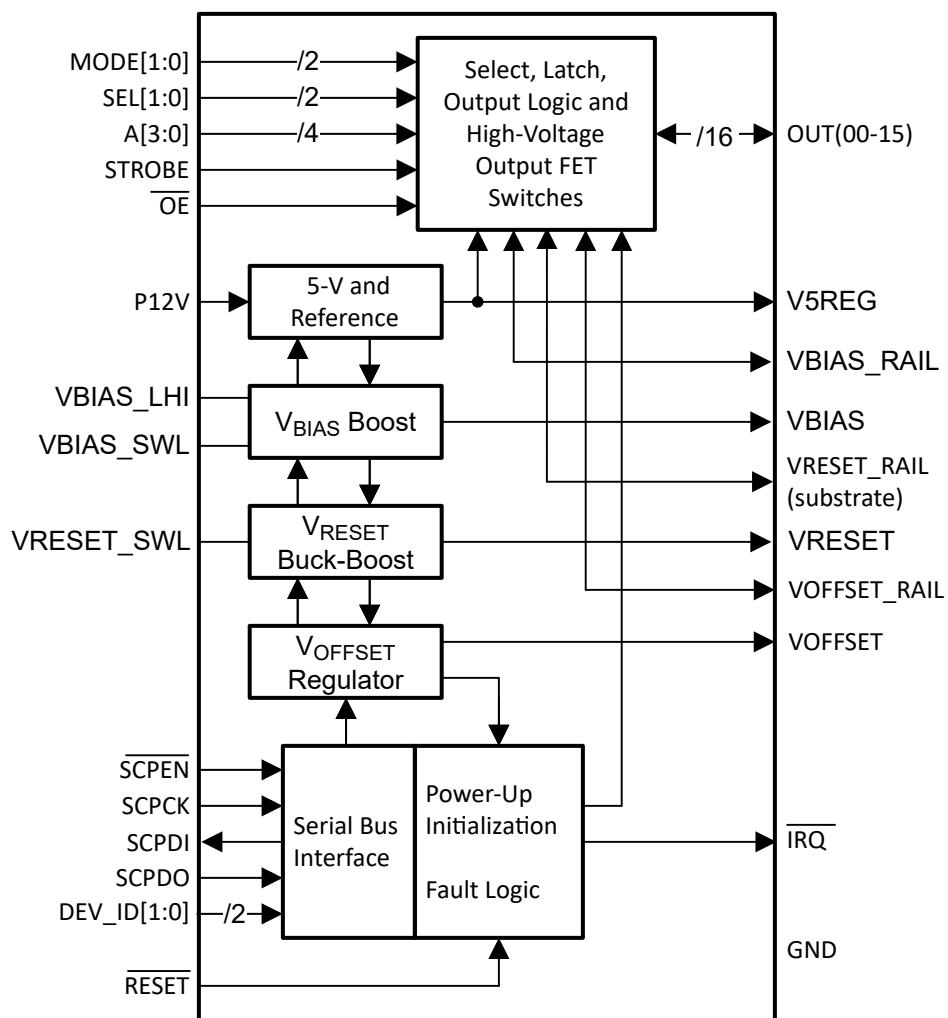
The DLPA300 consists of three functional blocks: a high-voltage power supply function, a DMD micromirror clock generation function, and a serial communication (SCP) function.

The high-voltage power supply function generates two specialized voltage levels:  $V_{BIAS}$  (21-V) and  $V_{OFFSET}$  (10-V). The exact values are controlled by the DLPC4430 or DLPC4420 display controller.  $V_{RESET}$  is generated by external voltage regulator.

The micromirror clock generation function uses the two voltages generated by the high-voltage power supply function and the one generated by the external voltage regulator to create the fifteen micromirror clock pulses (output the OUT[0:14] pins of the DLPA300). OUT15 is unused.

The serial communication function allows the display controller to control the generation of  $V_{BIAS}$ ,  $V_{RESET}$ , and  $V_{OFFSET}$ ; control the generation of the micromirror clock pulses; and control the general operation of the DLPA300 micromirror driver.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 5-V Linear Regulator

The 5-V linear regulator supplies the 5-V needed for the internal logic of the DLPA300 micromirror driver. It can also provide 5-V, up to 30 mA, for external peripherals.

Figure 7-1 shows the block diagram of this module. The input decoupling capacitors are shared with other internal DLPA300 modules. See Section 8.2.2.1 for recommended component values.

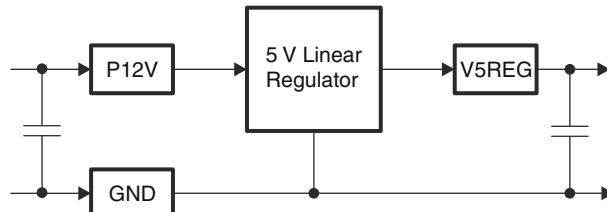


Figure 7-1. 5-Volt Linear Regulator Block Diagram

### 7.3.2 Bias Voltage Boost Converter

The bias voltage converter is a switching supply that operates at 1.3 MHz. The converter supplies the internal bias voltage for the high voltage FET switches. The  $V_{BIAS}$  voltage level for the 9- $\mu$ m pixel family of DMDs is 21V. The  $V_{BIAS}$  voltage level is configured by the DLP display controller chip over the serial communication port (SCP). Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for under-voltage ( $V_{UV}$ ) and current-limit ( $C_L$ ) conditions.

Figure 7-2 shows the block diagram of this module. The input decoupling capacitors are shared with other internal DLPA300 modules. See Section 8.2.2.1 for recommended component values.

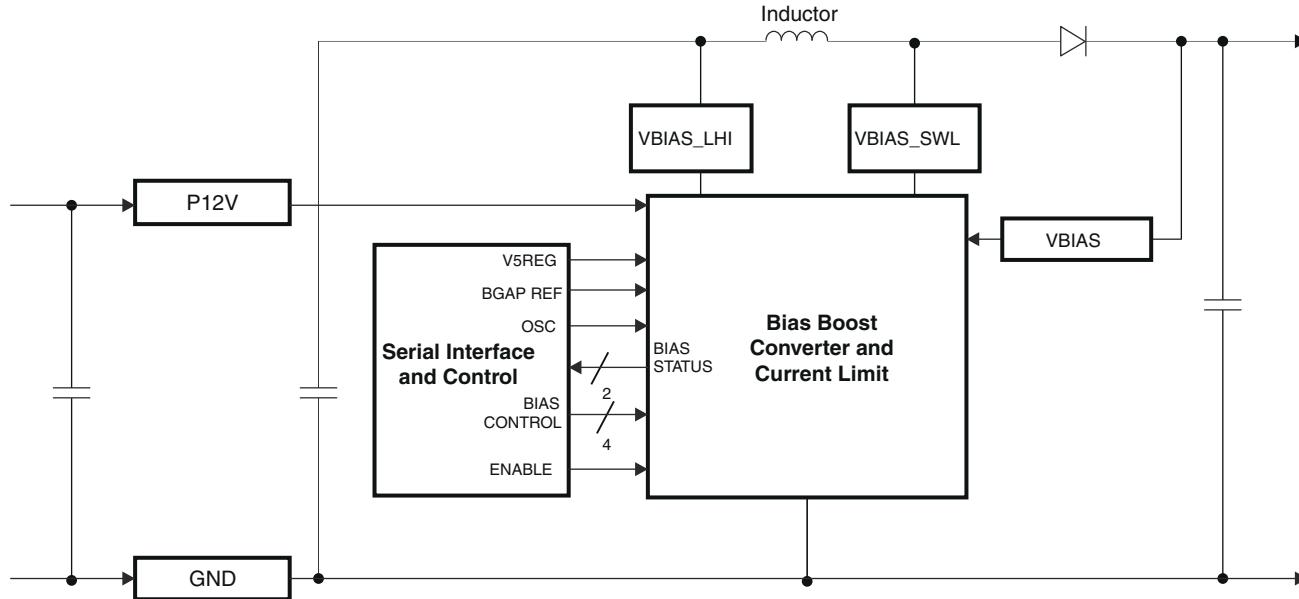


Figure 7-2. Bias Voltage Boost Converter Block Diagram

### 7.3.3 Reset Voltage Buck-Boost Converter

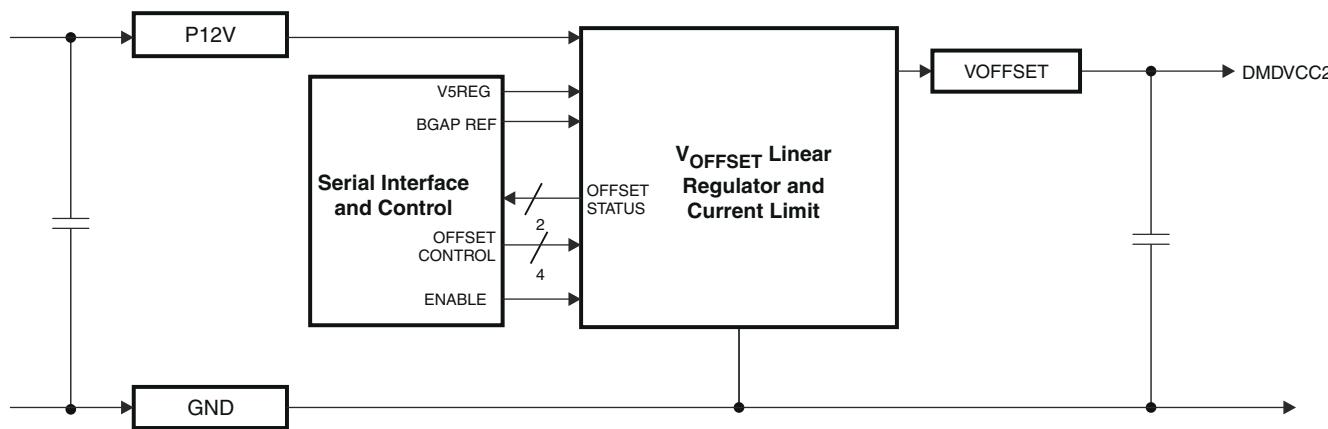
The internal reset voltage buck-boost converter in the DLPA300 is unused. An external voltage regulator is used to generate the -16.5-V for  $V_{RESET}$ . The output of this regulator is connected to the  $V_{RESET\_RAIL}$  pin on the DLPA300 micromirror driver.

The external voltage regulator provide reset voltage level for the high voltage FET switches. The internal reset voltage buck-boost converter is disabled by the DLP display controller over the serial communication port.

### 7.3.4 $V_{OFFSET}$ Regulator

The  $V_{OFFSET}$  regulator supplies the internal  $V_{OFFSET}$  voltage for the high voltage FET switches. The  $V_{OFFSET}$  voltage level for the 9- $\mu$ m pixel family of DMDs is 10-V during normal operation and 4.5-V during power down. The  $V_{OFFSET}$  voltage level is configured by the DLP controller chip over the serial communication port. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides two status bits to indicate latched and unlatched status bits for undervoltage ( $V_{UV}$ ) and current-limit ( $C_L$ ) conditions.

Figure 7-3 shows the block diagram of this module. The input decoupling capacitors are shared with other DLPA300 modules. See [Section 8.2.2.1](#) for recommended component values.



**Figure 7-3. Offset Voltage Boost Convertor Block Diagram**

### 7.3.5 Serial Communications Port (SCP)

The SCP is a full duplex, synchronous, character-oriented (byte) port that allows exchange of data between the DLPC4430 or DLPC4420 display controller, and the DLPA300 micromirror driver (and other DLP devices). The display controller is the primary on the SCP bus. The DLPA300 micromirror driver is the secondary on the SCP bus.

**Table 7-1. Serial Communications Port Signal Definitions**

SIGNAL	I/O	FROM/TO	TYPE	DESCRIPTION
SCPCK	I	SCP bus primary to secondary	LVTTL compatible	SCP bus serial transfer clock. The host processor (primary) generates this clock.
SCPEN	I	SCP bus primary to secondary	LVTTL compatible	SCP bus access enable (low true). When high, secondary resets to the idle state, and SCPDO output is tristated. Pulling SCPEN low initiates a read or write access. SCPEN must remain low for an entire read/write access, and must be pulled high after the last data cycle. To abort a read or write cycle, pull SCPEN high at any point.
SCPDI	I	SCP bus primary to secondary	LVTTL compatible	SCP bus serial data input. Data bits are valid and must be clocked in on the falling edge of SCPCK.
SCPDO	O	SCP bus secondary to primary	LVTTL, open drain w/tristate	SCP bus serial data output. Data bits must be clocked out on the rising edge of SCPCK. A 1-kΩ pullup resistor to the 3.3-V display controller supply is required.
IRQ	O	SCP bus secondary to primary	LVTTL, open drain	Not part of the SCP bus definition. Asynchronous interrupt signal from secondary to request service from the primary. A 1-kΩ pullup resistor to the 3.3-V display controller supply is required.

### 7.4 Device Functional Modes

At power up, the DLPC4430 or DLPC4420 display controller configures the DLPA300 over the SCP bus. There are two device functional modes. When  $\overline{OE}$  is high, OUT[0:14] are tristated. When  $\overline{OE}$  is low, the OUT[0:14] are active under the control of the display controller.

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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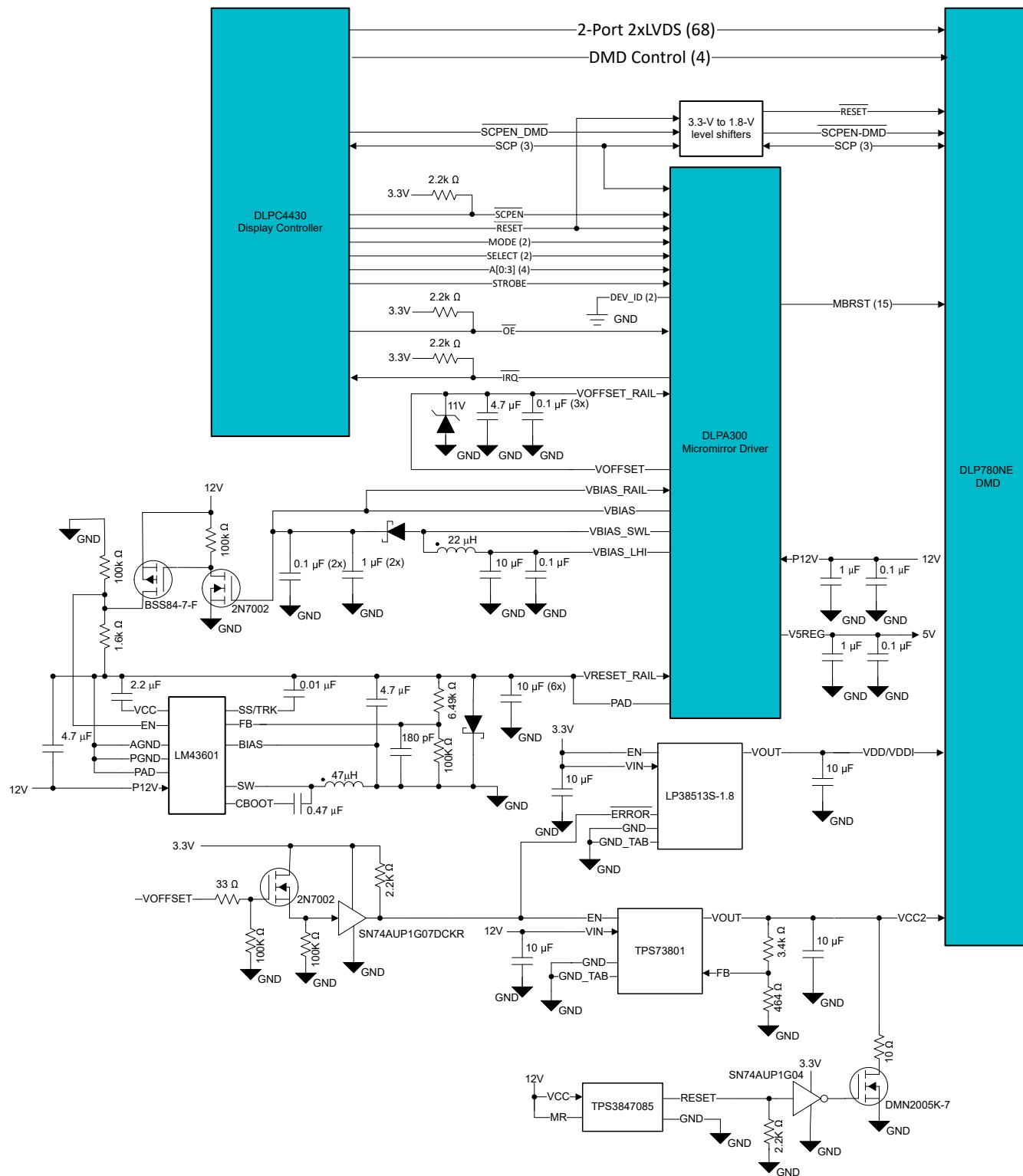
### 8.1 Application Information

DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLP display controller. Typical applications using the DLP780NE, DLP800RE and DLP780TE chipsets include laserTVs, smart projectors, enterprise projectors and digital signage. The DLP781NE, DLP781TE, DLP801RE and DLP801XE are used in higher brightness applications such as ProAV and large venue projectors.

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller through the DLPA300. Refer to *Power Supply Recommendations* section in the DLP780NE, DLP780TE, DLP800RE, DLP781NE, DLP781TE, DLP801RE and DLP801XE datasheets for power-up and power-down specifications. To ensure reliable operation, the DLP780NE, DLP800RE, DLP781NE and DLP801RE DMDs must always be used with DLPC4430 display controller, a DLPA100 power management and motor driver and a DLPA300 micromirror driver. The DLP780TE, DLP781TE and DLP801XE DMDs must always be used with the DLPC4420 display controller, the DLPA100 power management and motor driver and a DLPA300 micromirror driver. For LED and RGB direct laser illumination, the DLPA100 power management and motor driver can be replaced with discrete power supplies that are sequenced to meet the display controller power supply sequencing.

### 8.2 Typical Application

The DLPA300 micromirror driver controls the switching of the bias, offset and reset voltage levels on the MBRST pins to assure correct DMD operation. It is controlled by a DLP display controller which synchronizes the display data sent to the DMD with the correct sequencing of the bias, offset and reset voltage levels by the DLPA300 micromirror driver. The typical application shown in [Figure 8-1](#) is a Full-HD display using the DLP780NE chipset. The application is the same for the DLP800RE, DLP781NE or DLP801RE/DLPC4430 chipsets and the DLP780TE, DLP781TE or DLP801XE/dual-DLPC4420 chipsets. The DLPA300 micromirror driver creates  $V_{BIAS}$  and  $V_{OFFSET}$  with internal voltage regulators.  $V_{RESET}$  is created by an external regulator. These voltages are switched by the DLPA300 micromirror driver on the OUT[0:14] pins which are connected to the MBRST pins on the DMD.



**Figure 8-1. DLPA300 Typical Application**

### 8.2.1 Design Requirements

For the correct operation of a display system based on the 9- $\mu$ m pixel family of DMDs, the DLPA300 micromirror driver must be controlled by the DLPC4420 or DLPC4430 display controller. The embedded software in the DLPC4430 or DLPC4420 display controller coordinates the video data to the DMD and the bias, offset and reset

waveforms created by the DLPA300 micromirror driver that are input to the MBRST pins on the DMD. This results in the highest possible image quality and system efficiency.

The key design requirements are power supply sequencing for power up and power down. The 9- $\mu$ m family of DMDs require that the VCC2 supply be turned on after the 1.8-V supply is full on and stable. Similarly, on power down, the DMDs require that the VCC2 supply be full off before the 1.8-V supply begins its power off ramp.

The DLPA300 micromirror driver imparts one power supply sequencing constraint. Because  $V_{RESET}$  is generated by an external supply, the DLPC4430 display controller cannot control this supply directly by software. Therefore, it is necessary to use the  $V_{BIAS}$  supply to control the power up and power down of the external  $V_{RESET}$  power supply.

These power supply sequencing requirements necessitate external circuitry to control the  $V_{RESET}$  and VCC2 power supply sequencing, as seen in [Figure 8-1](#).

### 8.2.2 Detailed Design Procedure

The DLPC4430 or DLPC4420 display controller configures the  $V_{BIAS}$  and  $V_{OFFSET}$  voltage regulators in the DLPA300 micromirror driver through the SCP bus.  $V_{BIAS}$  is then used to generate the enable signal for the  $V_{RESET}$  external voltage regulator, LM43601 step-down voltage converter. When the  $V_{BIAS}$  is enabled, it turns on the two-transistor buffer amplifier. The 2N7002 and BSS84-7-F FETs isolate  $V_{BIAS}$  from the  $V_{RESET\_RAIL}$  and shift the voltage reference to  $V_{RESET\_RAIL}$ .

The thermal pad on the DLPA300 micromirror controller and the LM43601 step-down voltage converter are electrically connected to the  $V_{RESET\_RAIL}$ . Furthermore, the AGND and PGND pins on the LM43601 step-down voltage converter are also connected to the  $V_{RESET\_RAIL}$ . Therefore, the logic levels and analog voltage levels for LM43601 step-down voltage converter are referenced to the -16.5-V  $V_{RESET\_RAIL}$ .

The LM43601 data sheet provides details for the component selection for the components in the voltage regulator circuit connected to the  $V_{RESET\_RAIL}$ . The output of the regulator is set to the  $V_{RESET}$  value of -16.5 V. The selection of the resistors in the resistor divider sets the output voltages, 6.49 k $\Omega$  and 100 k $\Omega$ .

The DLP780NE power sequencing requires that the VCC2 power supply ramps up after the 1.8-V supply is powered on and stable, and  $V_{OFFSET}$  is powered up and stable. The two conditions are met by the wired-or of the ERROR signal from the LP38513-1.8 ultra-low dropout linear regulator and an enable signal generated from  $V_{OFFSET}$ . The 2N7002 enhancement mode FET acts as an inverter and level shifter from  $V_{OFFSET}$  to a 3.3-V logic level.

In the event of a power supply failure (such as a pull-the-plug event), VCC2 must be driven low before the 1.8-V supply starts to drop voltage. To achieve this, the TPS3847 12-V voltage monitor triggers a shunt-to-ground power FET to pull VCC2 to ground.

#### 8.2.2.1 Component Selection Guidelines

**Table 8-1. 5-V Regulator**

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
P12V filter capacitor	10 to 33 $\mu$ F, 20 VDC, 1 $\Omega$ max ESR	Tantalum or ceramic	Positive Terminal: P12V, pin 11 (locate near pin 11)	Negative Terminal: Ground
P12V bypass capacitor	0.1 $\mu$ F, 50 VDC, 0.1 $\Omega$ max ESR	Ceramic	P12V, pin 11 (locate near pin 11)	Ground
V5REG filter capacitor	0.1 <sup>(1)</sup> to 1.0 $\mu$ F, 10 VDC, 2.5 $\Omega$ max ESR	Tantalum or ceramic	Positive Terminal: V5REG, pin 47 (locate near pin 47)	Negative Terminal: Ground
V5REG bypass capacitor	0.1 $\mu$ F <sup>(1)</sup> , 16 VDC, 0.1 $\Omega$ max ESR	Ceramic	V5REG, pin 47 (locate near pin 47)	Ground

(1) To ensure stability of the linear regulator, use a capacitance with a value not less than 0.1  $\mu$ F.

**Table 8-2. Bias Voltage Boost Converter**

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
LHI filter capacitor	10 $\mu$ F, 20 VDC, 1- $\Omega$ max ESR	Tantalum or ceramic	Positive Terminal: VBIAS_LHI, pin 10 (locate near pin 10)	Negative Terminal: Ground
LHI bypass capacitor	0.1 $\mu$ F, 50 VDC, 0.1- $\Omega$ max ESR	Ceramic	VBIAS_LHI, pin 10 (locate near pin 10)	Ground
VBIAS_RAIL filter capacitor (2 required)	1 $\mu$ F, 50 VDC, 0.1- $\Omega$ max ESR	Ceramic	VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71)	Ground
VBIAS_RAIL bypass capacitors (2 required)	0.1 $\mu$ F, 50 VDC, 0.1 $\Omega$ max ESR	Ceramic	VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71)	Ground
Inductor	22 $\mu$ H, 0.5 A, 160 m $\Omega$ ESR	Coil Craft DT1608C-223 (or equivalent)	VBIAS_LHI, pin 10	VBIAS_SWL, pin 8
Schottky diode	0.5 A, 40 V (minimum)	OnSemi MBR0540T1G or STMicroelectronics STPS0540Z, STPS0560Z (or equivalent)	Anode: VBIAS_SWL, pin 8	Cathode: VBIAS, pin 9

**Table 8-3. Offset Voltage Regulator**

COMPONENT	VALUE	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
VOFFSET filter capacitors	1 <sup>(1)</sup> to 4.7 <sup>(2)</sup> $\mu$ F, 35 VDC, 1 $\Omega$ max ESR	Tantalum or ceramic	Positive Terminal: VOFFSET, pin 49 (1st Cap near pin 49) Positive Terminal: DMDVCC2 pins (2nd Cap at DMD)	Negative Terminal: Ground at DLPA300 Negative Terminal: VSS (Ground) at DMD
VOFFSET bypass capacitors (3 required)	0.1 $\mu$ F, 50 VDC, 0.1 $\Omega$ max ESR	Ceramic	VOFFSET, pin 49 (locate 1 near pin 49)	Ground at DLPA300 Ground at DMD
Zener Diode	11V 3W	Micro Commercial Components 3SMBJ5926B-TP or equivalent	VOFFSET	Ground

(1) To ensure stability of the linear regulator, the absolute minimum output capacitance must not be less than 1.0  $\mu$ F.  
 (2) Recommended value is 3.3  $\mu$ F each. Different values are acceptable, provided that the sum of the two is 6.8  $\mu$ F maximum.

**Table 8-4. Pullup Resistors**

COMPONENT	VALUE (k $\Omega$ )	TYPE OR PART NUMBER	CONNECTION 1	CONNECTION 2
Resistor	2.2		SCPDO, pin 42	Chipset controller 3.3-V V <sub>DD</sub>
Resistor	2.2		IRQ, pin 43	Chipset Controller 3.3-V V <sub>DD</sub>
Resistor (optional)	2.2		OE, pin 6	Chipset Controller 3.3-V V <sub>DD</sub>

### 8.2.3 Application Curves

The power supply sequencing for V<sub>BIAS</sub>, V<sub>OFFSET</sub> and V<sub>RESET</sub> are shown in [Figure 8-2](#) and [Figure 8-3](#). On power-up, the turn on of V<sub>BIAS</sub> enables the external V<sub>RESET</sub> voltage regulator. In power-down, when V<sub>BIAS</sub> powers off, it disables the V<sub>RESET</sub> regulator, which slowly decays to ground.

The power sequencing for VCC2 voltage regulator is shown in [Figure 8-4](#) and [Figure 8-5](#). The power up of V<sub>OFFSET</sub> enables the turn on of the VCC2 voltage regulator. As seen in the zoom out of [Figure 8-4](#), the 1.8-V supply is already on and stable. Similarly, the power down of V<sub>OFFSET</sub> disables the VCC2 voltage regulator. The 1.8-V supply powers down after both V<sub>OFFSET</sub> and VCC2 are powered down, as seen in the zoom out of [Figure 8-5](#).

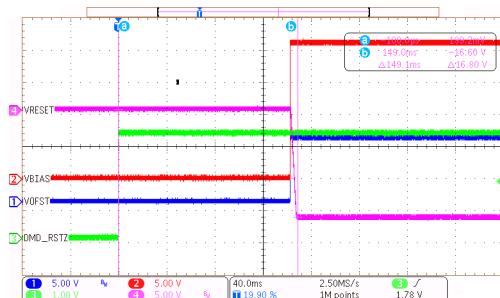


Figure 8-2. High Voltage Power-Up Sequence

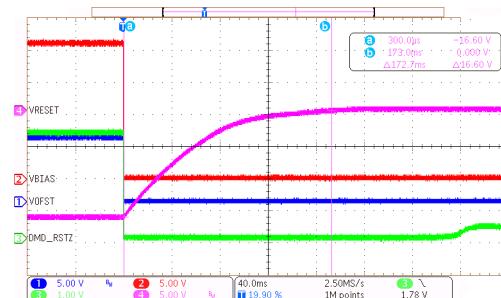


Figure 8-3. High Voltage Power-Down Sequence

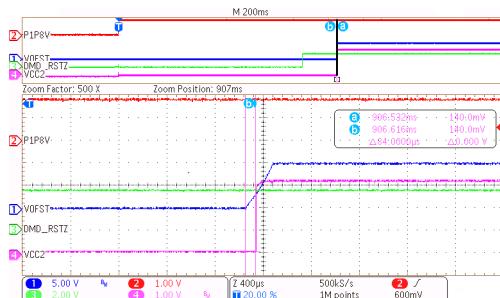


Figure 8-4. VCC2 Power-Up Sequence

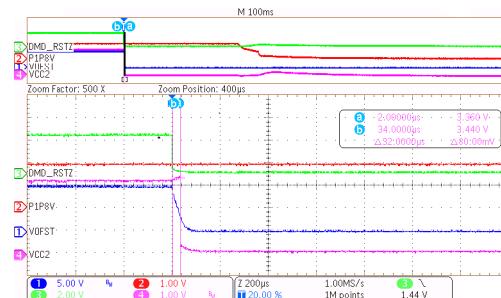


Figure 8-5. VCC2 Power-Down Sequence

## 9 Power Supply Recommendations

### 9.1 Power Supply Rail Guidelines

Table 8-1 through Table 8-4 provides discrete component selection guidelines.

- Ensure that the P12V filter and bypass capacitors are distributed and connected to pin 11 and pin 48 and pin 50. Place these capacitors as close to their respective pins as possible and if necessary, place on the bottom layer.
- The V5REG filter and bypass capacitors must be placed near and connected to pin 47.
- It is best to route the VBIAS\_RAIL etch runs in the following order: pin 40, pin 31, pin 30, pin 21, pin 80, pin 71, pin 70, and pin 61. Ensure that the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Locate the bypass capacitors near and connected to pin 30 and pin 71 to provide bypassing on both sides.
- The VBIAS\_LHI filter and bypass capacitors must be placed near and connected to pin 10.
- The VBIAS filter and bypass capacitors must be placed near and connected to pin 9.
- VBIAS pin 9 must also be connected (optionally with a 0-ohm resistor) to VBIAS\_RAIL at or between pins 21 and 80.
- Route the VRESET\_RAIL etch runs in the following order: pin 36, pin 35, pin 26, pin 25, pin 76, pin 75, pin 66, and pin 65. Ensure the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Bypass capacitors must be placed near and connected to pins 35 and 66 to provide bypassing on both sides.
- The VRESET filter and bypass capacitors must be located near and connected to pin 13. VRESET pin 13 must also be connected (optionally with a 0-Ω resistor) to VRESET\_RAIL at or between pin 25 and pin 76.
- Route the VOFFSET\_RAIL etch runs in the following order: pin 23, pin 28, pin 33, pin 38, pin 63, pin 68, pin 73, and pin 78. Ensure the etch runs are short and direct as they must carry 35 ns current spikes of up to 0.64 A (peak). Place the bypass capacitors near and connected to pin 28 and pin 73 to provide bypassing on both sides.
- The VOFFSET filter and bypass capacitors must be placed near and connected to pin 49.
- VOFFSET pin 49 must also be connected (optionally with a 0-Ω resistor) to VOFFSET\_RAIL at or between pin 38 and pin 63.

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#### Note

Aluminum electrolytic capacitors may not be suitable for the DLPA300 application. At the switching frequencies used in the DLPA300 (up to 1.5 MHz), aluminum electrolytic capacitors drop significantly in capacitance and increase in ESR resulting in voltage spikes on the power supply rails, which could cause the device to shut down or perform in an unreliable manner.

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## 10 Layout

### 10.1 Layout Guidelines

**CAUTION**

Board layout and routing guidelines must be followed explicitly and all external components used must be in the range of values and of the quality recommended for proper operation of the DLPA300.

**CAUTION**

Thermal pads must be tied to VRESET\_RAIL. Do not connect to ground.

Provide suitable Kelvin connections for the switching regulator feedback pins: V<sub>BIAS</sub> (pin 9) and V<sub>RESET</sub> (pin 13).

Make the PCB traces that connect the switching devices: V<sub>BIAS\_SWL</sub> (pin 8) and V<sub>RESET\_SWL</sub> (pin 12) as short and wide as possible to minimize leakage inductances. Make the PCB traces that connect the switching converter components (inductors, flywheel diodes and filtering capacitors) as short and wide as possible. Ensure that the electrical loops that these components form are as small and compact as possible, with the ground referenced components forming a star connection.

Due to the fast switching transitions appearing on the sixteen reset OUT<sub>x</sub> pins, it is recommended to keep these traces as short as possible. Also, to minimize potential cross-talk between outputs, it is advisable to maintain as much clearance between each of the output traces.

#### 10.1.1 Grounding Guidelines

Ensure that the PWB has an internal ground plane that extends under the DLPA300. All nine ground pins (1, 7, 14, 20, 41, 46, 53, 55, and 60) must be connected to the ground plane using the shortest possible runs and vias. All filter and bypass capacitors must be placed near the pin being filtered or bypassed for the shortest possible runs to the part and to the ground plane.

### 10.2 Thermal Considerations

Thermally bond or solder the DLPA300 package to an external thermal pad on the PWB surface. The recommended dimensions of the thermal pad are 10 mm × 10 mm centered under the device. The metal bottom of the package is tied internally to the substrate at the VRESET\_RAIL voltage level. Therefore, the thermal pad on the board must be isolated from any other extraneous circuit or ground and no circuit vias are allowed inside the pad area. Thermal pads are required on both sides of the PWB. Connect the thermal pads together through an array of 5 × 5 thermal vias, 0.5 mm in diameter.

**Thermal pads and the thermal vias are connected to VRESET\_RAIL and must be isolated from ground, or any other circuit.**

Locate an internal P12V plane directly underneath the top layer and have an isolated area under the DLPA300. This isolated area must be a minimum of 20 cm<sup>2</sup> and connect to the thermal pad of the DLPA300 through the thermal vias. The potential of the isolated area is also at VRESET\_RAIL. The internal ground plane must extend under the DLPA300 to help carry the heat away. Please refer to the PowerPAD Thermally Enhanced Package application report ([SLMA002](#)) for details on thermally efficient package design considerations.

Be careful to place the DLPA300 device away from local PWB hotspots. Heat generated from adjacent components may impact the DLPA300 thermal characteristics.

## 11 Device and Documentation Support

### 11.1 Third-Party Products Disclaimer

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### 11.2 Device Support

#### 11.2.1 Device Nomenclature

The device marking consists of the fields shown in [Figure 11-1](#).



#### PART MARKING CODES

LLLLLLL = Lot trace code or date code

e4 = Pb-Free NiPdAu terminal finish

● = Pin 1 designator

**Figure 11-1. Device Marking (Device Top View)**

### 11.3 Documentation Support

#### 11.3.1 Related Documentation

The following documents contain additional information related to the chipsets supported by the DLPA300 micromirror driver and used in the typical application.

- [DLP780NE data sheet](#)
- [DLP800RE data sheet](#)
- [DLP780TE data sheet](#)
- [DLP781NE data sheet](#)
- [DLP801RE data sheet](#)
- [DLP781TE data sheet](#)
- [DLP801XE data sheet](#)
- [DLPC4430 data sheet](#)
- [DLPC4420 data sheet](#)
- [DLPA100 data sheet](#)
- [LM43601 data sheet](#)
- [LP38513S data sheet](#)
- [TPS73801 data sheet](#)
- [TPS3847085 data sheet](#)

### 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLPA300PFP	Active	Production	HTQFP (PFP)   80	119   JEDEC TRAY (5+1)	Yes	Call TI	Call TI	0 to 70	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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