DP83TC814x-Q1 100BASE-T1 Automotive Ethernet PHY

1 Features

- Open Alliance and IEEE 802.3bw 100BASE-T1 compliant
  - Passes Level IV emissions with Integrated LPF
- SAE J2962-3 EMC compliant
- Configurable I/O voltages: 3.3V, 2.5V, and 1.8V
- MAC interfaces: MII, RMII, RGMII and SGMII
- Optional separate voltage rail for MAC interface pins (3.3V, 2.5V, 1.8V)
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C ambient operating temperature
  - ±8kV HBM ESD for pins 12 and 13
  - IEC61000-4-2 ESD classification level 4 for pins 12 and 13: ±8kV contact discharge
- IEEE 1588 SFD support
- TSN compliant with 802.3br frame pre-emption support
- Low active power operation: < 230mW
- Diagnostic tool kit
  - Signal Quality Indication (SQI)
  - Time Domain Reflectometry (TDR)
  - Electrostatic discharge sensor
  - Voltage sensor
  - PRBS Built-in Self-Test
  - Loopbacks
- VQFN, wettable flank packaging
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design

2 Applications

- ADAS
- Gateway and Body Control
- Telematics

3 Description

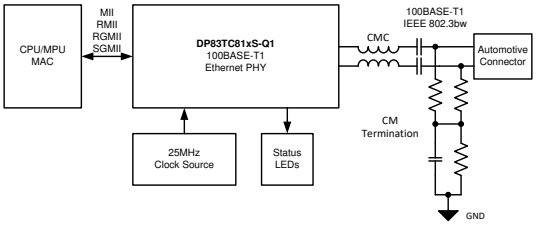
The DP83TC814-Q1 device is an IEEE 802.3bw-compliant automotive PHYTER™ Ethernet physical layer transceiver which can work with Unshielded Twisted Pair cable. The PHY provides all physical layer functions needed to transmit and receive data over unshielded single twisted-pair cables. The device provides xMII flexibility with support for standard MII, RMII, RGMII, and SGMII MAC interfaces.The PHY also integrates a low pass filter on the MDI side to reduce emissions.

This device includes the Diagnostic Tool Kit, providing an extensive list of real-time monitoring tools, debug tools and test modes. Within the tool kit is the first integrated electrostatic discharge (ESD) monitoring tool. The device is capable of counting ESD events on MDI as well as providing real-time monitoring through the use of a programmable interrupt. Additionally, the DP83TC814S-Q1includes a pseudo random binary sequence (PRBS) frame generation tool, which is fully compatible with internal loopbacks, to transmit and receive data without the use of a MAC. The device is housed in a 6.00mm × 6.00mm, 36 pin VQFN wettable flank package. This device is pin-2-pin compatible with DP83TG720 (1000BASE-T1) and is also form factor compatible with DP83TC811. This allows for a single PCB layout to be used for DP83TC811, DP83TC812, DP83TC814, and DP83TG720.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
DP83TC814S-Q1	VQFN (36)	6.00mm × 6.00mm
DP83TC814R-Q1	VQFN (36)	6.00mm × 6.00mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

4 Device Comparison Table

PART NUMBER	SGMII SUPPORT	OPERATING TEMPERATURE
DP83TC814R-Q1	No	–40°C to 125°C
DP83TC814S-Q1	Yes	–40°C to 125°C

5 Pin Configuration and Functions

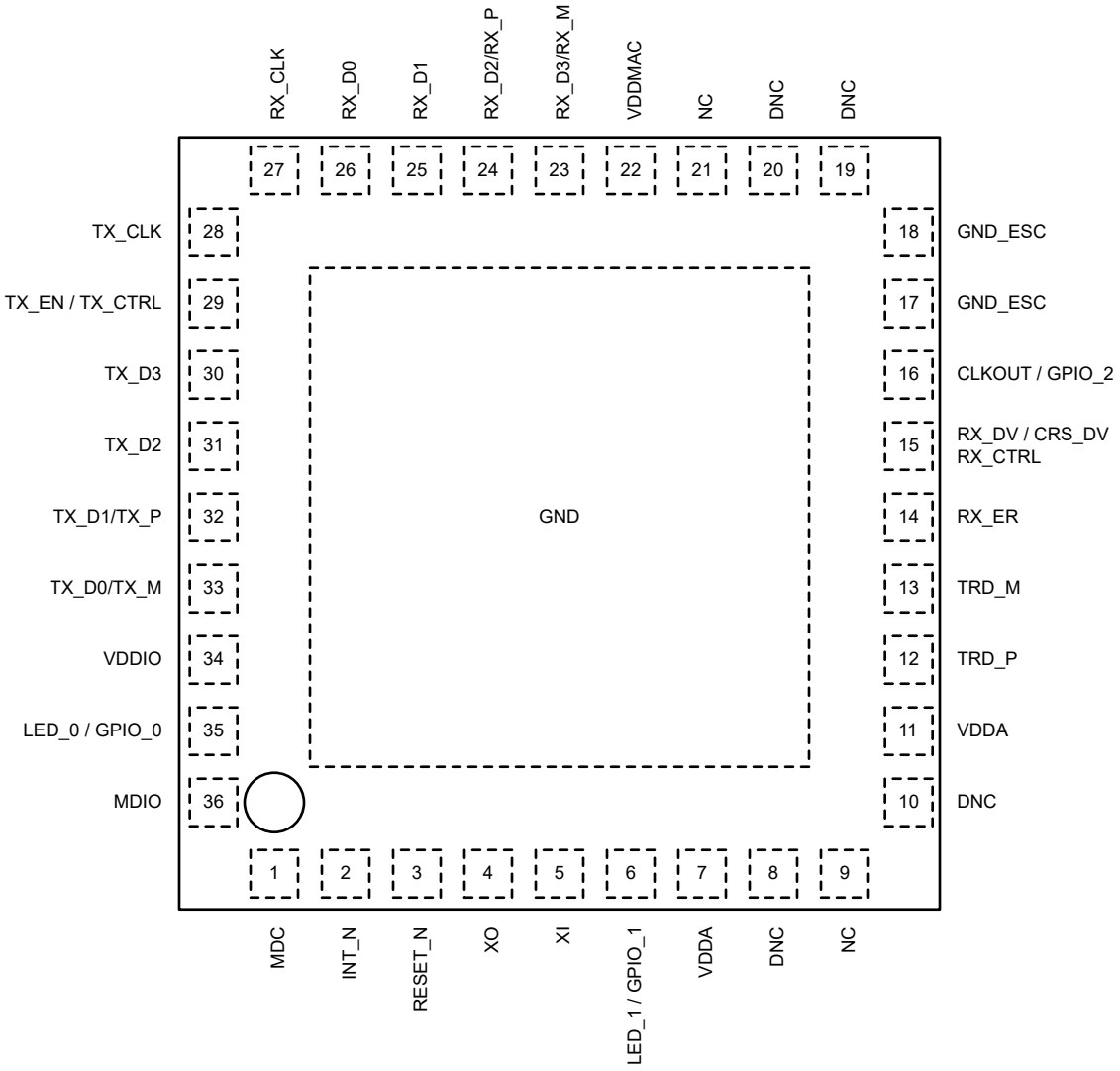


Figure 5-1. DP83TC814S-Q1 RHA Package
36-Pin VQFN

Top View

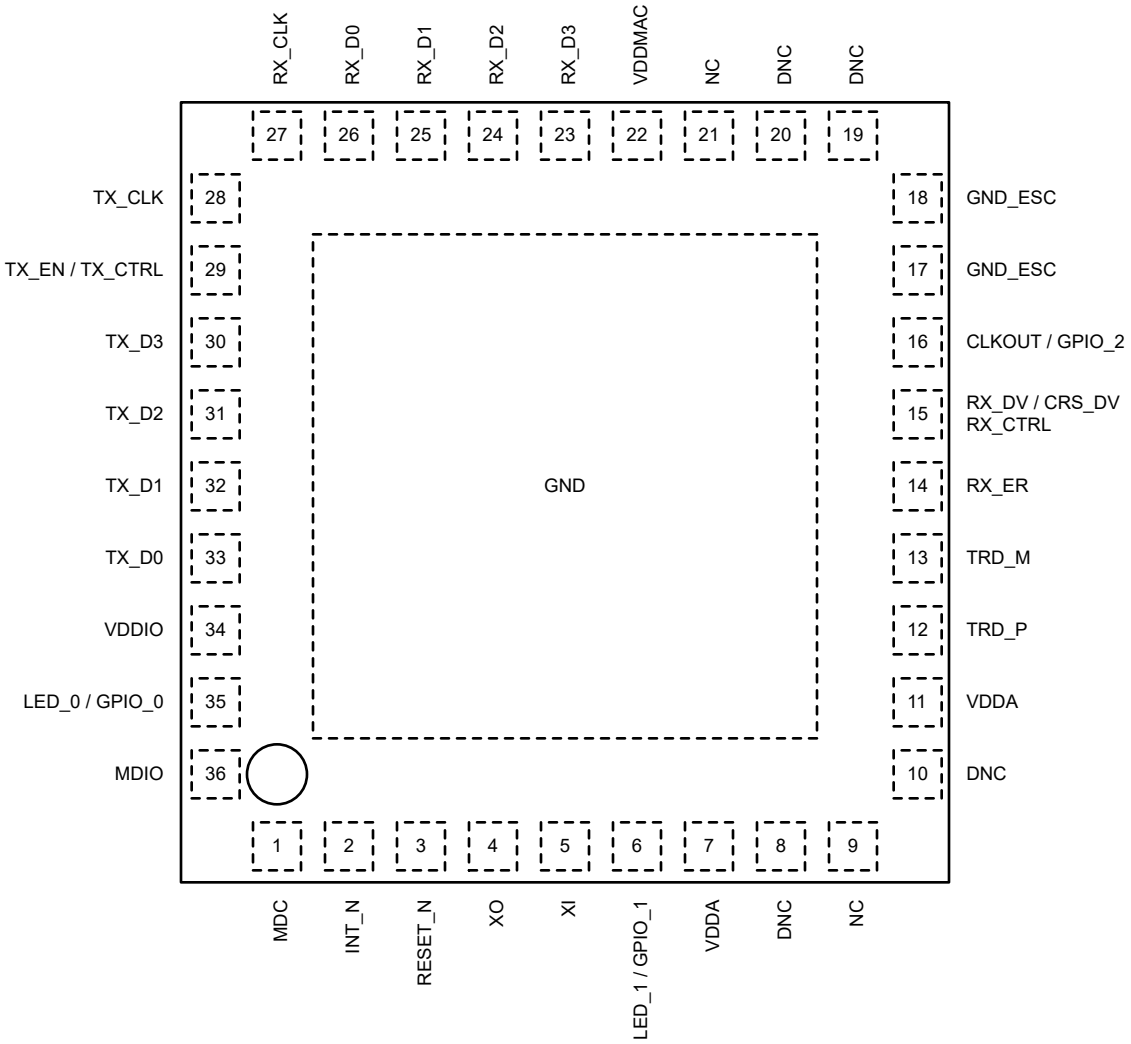


Figure 5-2. DP83TC814R-Q1 RHA Package
36-Pin VQFN
Top View

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME[2]	NO.		
MAC INTERFACE			
RX_D3 RX_M	23	S, PD, O	**Receive Data:** Symbols received on the cable are decoded and transmitted out of these pins synchronous to the rising edge of RX_CLK. Data is considered valid when RX_DV is asserted. A data nibble, RX_D[3:0], is transmitted in MII and RGMII modes. 2 bits; RX_D[1:0], are transmitted in RMII mode. RX_D[3:2] are not used when in RMII Follower mode. If the PHY is bootstrapped to RMII Leader mode, a 50MHz clock reference is automatically outputted on RX_D3. This clock must be fed to the MAC. **RX_M / RX_P:** Differential SGMII Data Output. These pins transmit data from the PHY to the MAC. Use the strap resistors in RX_D3 pin in SGMII mode.
RX_D2 RX_P	24		
RX_D1	25		
RX_D0	26		
RX_CLK	27	PD, O	**Receive Clock:** In MII and RGMII modes, the receive clock provides a 25MHz reference clock. **Unused in RMII and SGMII modes**
RX_ER	14	S, PD, O	**Receive Error:** In MII and RMII modes, this pin indicates a receive error symbol has been detected within a received packet. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required to be used by the MAC in MII or RMII because the PHY automatically corrupts data on a receive error. **Unused in RGMII and SGMII modes**
RX_DV CRS_DV RX_CTRL	15	S, PD, O	**Receive Data Valid:** This pin indicates when valid data is presented on RX_D[3:0] for MII mode. **Carrier Sense Data Valid:** This pin combines carrier sense and data valid into an asynchronous signal. When CRS_DV is asserted, data is presented on RX_D[1:0] in RMII mode. To set Pin 15 as CRS_DV, set 0x0551=0x0010 (Default). **RGMII Receive Control:** Receive control combines receive data valid indication and receive error indication into a single signal. RX_DV is presented on the rising edge of RX_CLK and RX_ER is presented on the falling edge of RX_CLK. To set Pin 15 as RX_DV, set 0x0551=0x0000. **Unused in SGMII mode**
TX_CLK	28	PD, I, O	**Transmit Clock:** In MII mode, the transmit clock is a 25MHz output (50Ω Driver) and has constant phase referenced to the reference clock. In RGMII mode, this clock is sourced from the MAC layer to the PHY. A 25MHz clock must be provided (not required to have constant phase to the reference clock unless synchronous RGMII is enabled) **Unused in RMII and SGMII modes**
TX_EN TX_CTRL	29	PD, I	**Transmit Enable:** In MII mode, transmit enable is presented prior to the rising edge of the transmit clock. TX_EN indicates the presence of valid data inputs on TX_D[3:0]. In RMII mode, transmit enable is presented prior to the rising edge of the reference clock. TX_EN indicates the presence of valid data inputs on TX_D[1:0]. **RGMII Transmit Control:** Transmit control combines transmit enable and transmit error indication into a single signal. TX_EN is presented prior to the rising edge of TX_CLK; TX_ER is presented prior to the falling edge of TX_CLK. **Unused in SGMII mode**
TX_D3	30	PD, I	**Transmit Data:** In MII and RGMII modes, the transmit data nibble, TX_D[3:0], is received from the MAC prior to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] is received from the MAC prior to the rising edge of the reference clock. TX_D[3:2] are not used in RMII mode. **TX_M / TX_P:** Differential SGMII Data Input. These pins receive data that is transmitted from the MAC to the PHY.
TX_D2	31		
TX_D1 TX_P	32		
TX_D0 TX_M	33		
SERIAL MANAGEMENT INTERFACE			
MDC	1	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input and output data. This clock can be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 20MHz. There is no minimum clock rate.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME[2]	NO.		
MDIO	36	OD, IO	**Management Data Input/Output:** Bidirectional management data signal that can be sourced by the management station or the PHY. This pin requires a pullup resistor. In systems with multiple PHYs using same MDIO-MDC bus, a single pull-up resistor must be used on MDIO line. Recommended to use a resistor between 2.2kΩ and 9kΩ. MDIO/MDC Access is required to pass Open Alliance Compliance. See Section 7.3.2

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME[2]	NO.		
CONTROL INTERFACE			
$\overline{\text{INT}}$	2	PU, OD, IO	**Interrupt:** Active-LOW output, which is asserted LOW when an interrupt condition occurs. This pin has a weak internal pullup. Register access is necessary to enable various interrupt triggers. Once an interrupt event flag is set, register access is required to clear the interrupt event. This pin can be configured as an Active-HIGH output using register *0x0011*. Interrupt status from Reg 12-13 is recommended to be read only when INT_N is LOW. This pin can also operate as Power-Down control where asserting this pin low puts the PHY in power down mode and asserting high puts the PHY in normal mode. This feature can also be enabled using the register *0x0011*.
$\overline{\text{RESET}}$	3	PU, I	**Reset:** Active-LOW input, which initializes or reinitializes the PHY. Asserting this pin LOW for at least 1µs forces a reset process to occur. All internal registers reinitializes to the default states as specified for each bit in the Register Maps section. All bootstrap pins are resampled upon deassertion of reset.
CLOCK INTERFACE			
XI	5	I	**Reference Clock Input (RMII):** Reference clock 50MHz CMOS-level oscillator in RMII Follower mode. Reference clock 25MHz crystal or oscillator in RMII Leader mode. **Reference Clock Input (Other MAC Interfaces):** Reference clock 25MHz crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only and XO left floating. This pin can also accept clock input from other devices like Ethernet MAC or another Ethernet PHY in daisy-chain operations.
XO	4	O	**Reference Clock Output:** XO pin is used for crystal only. This pin must be left floating when a CMOS-level oscillator is connected to XI.
LED/GPIO INTERFACE			
LED_0 / GPIO_0	35	S, PD, IO	**LED_0:** Link Status LED. This pin can also be used as LED or clock output via Register selection.
LED_1 / GPIO_1	6	S, PD, IO	**LED_1:** Link Status and BLINK for TX/RX Activity. This pin can also be used as LED or clock output via Strap/ Register selection.
CLKOUT / GPIO_2	16	IO	**Clock Output:** 25MHz reference clock in all modes except RMII Follower, which is 50MHz instead. This pin can also be used as LED or GPIO via Strap/Register selection. Program register<0x045F>=0x000F and register<0x0453>=0x0003 to disable switching on CLKOUT pin
MEDIUM DEPENDENT INTERFACE			
TRD_M	13	IO	**Differential Transmit and Receive:** Bidirectional differential signaling configured for 100BASE-T1 operation, IEEE 802.3bw compliant.
TRD_P	12		
GROUND ESCAPE			
GND_ESC	17		**Ground Escape:** Optional ground escape pins. These pins can be connected to ground to optimize PCB layout. These pins are not substitute for power ground connection to DAP. DAP must always be connected to power ground. This pin can be left unconnected if not used.
GND_ESC	18		**Ground Escape:** Optional ground escape pins. These pins can be connected to ground to optimize PCB layout. These pins are not substitute for power ground connection to DAP. DAP must always be connected to power ground. This pin can be left unconnected if not used.
POWER CONNECTIONS			
VDDA	11	SUPPLY	**Core Supply:** 3.3V Recommend using 0.47µF and 0.01µF ceramic decoupling capacitors; optional ferrite bead can be used.
VDDIO	34	SUPPLY	**IO Supply:** 1.8V, 2.5V, or 3.3V Recommend using ferrite bead, 0.47µF and 0.01µF ceramic decoupling capacitors.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME[2]	NO.		
VDDMAC	22	SUPPLY	**Optional MAC Interface Supply:** 1.8V, 2.5V, or 3.3V Optional separate supply for MAC interface pins. This pin supplies power to the MAC interface pins and can be kept at a different voltage level as compared to other IO pins. Recommend using 0.47µF, and 0.01µF ceramic decoupling capacitors and ferrite bead. When separate VDDMAC is not required in the system then the pin must be connected to VDDIO. When connecting to VDDIO, 0.47µF on the VDDIO can be removed. 0.47µF must still be connected close to VDDMAC. In this case, one common ferrite bead can be used between VDDIO and VDDMAC.
VDDA	7	SUPPLY	**VDDA Supply:** 3.3V Recommend using 0.1µF ceramic decoupling capacitors.
GROUND	DAP	GROUND	**Ground:** This must always be connected to power ground.
DO NOT CONNECT			
DNC	8		**DNC:** Do not connect (leave floating)
DNC	10		**DNC:** Do not connect (leave floating)
DNC	19		**DNC:** Do not connect (leave floating)
DNC	20		**DNC:** Do not connect (leave floating)
RECOMMENDED FOR FUTURE EMC ENHANCEMENTS			
Pin 9	9		Connect to Pin 21
Pin 21	21		Connect 2.2µF and 0.1µF ceramic capacitors from Pin 21 to GND

(1) Pin Type:
I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup
S = Bootstrap configuration pin (all configuration pins have weak internal pullups or pulldowns)

(2) When pins are unused, follow the recommended connection requirements provided in the table above. If pins do not have required termination, the pins can be left floating.

Table 5-2. Pin Domain

PIN NO	PIN NAME	VOLTAGE DOMAIN
1	MDC	VDDIO
2	INT_N	VDDIO
3	RESET_N	VDDIO
4	XO	VDDIO
5	XI	VDDIO
6	LED_1/GPIO_1	VDDIO
12	TRD_P	VDDA
13	TRD_M	VDDA
14	RX_ER	VDDMAC
15	RX_DV/CRS_DV/RX_CTRL	VDDMAC
16	CLKOUT/GPIO_2	VDDMAC
23	RX_D3/RX_M	VDDMAC
24	RX_D2/RX_P	VDDMAC
25	RX_D1	VDDMAC
26	RX_D0	VDDMAC
27	RX_CLK	VDDMAC
28	TX_CLK	VDDMAC
29	TX_EN/TX_CTRL	VDDMAC
30	TX_D3	VDDMAC
31	TX_D2	VDDMAC
32	TX_D1/TX_P	VDDMAC
33	TX_D0/TX_M	VDDMAC
35	LED_0/GPIO_0	VDDIO
36	MDIO	VDDIO

Table 5-3. Pin States - POWER-UP / RESET

PIN NO	PIN NAME	POWER-UP / RESET		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	I	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1	I	PD	9
7	VDDA	SUPPLY	none	none
8	DNC	I/O	PD	455
9	NC	FLOAT	none	none
10	DNC	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT	O	none	none
17	GND_ESC	FLOAT	none	none
18	GND_ESC	I	PD	50
19	DNC	FLOAT	none	none
20	DNC	FLOAT	none	none
21	NC	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	I	PD	9
24	RX_D2	I	PD	9
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	I	PD	9
36	MDIO	OD, IO	none	none

Table 5-4. Pin States - MAC ISOLATE and IEEE PWDN

PIN NO	PIN NAME	MAC ISOLATE			IEEE PWDN		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VDDA	SUPPLY	none	none	SUPPLY	none	none
8	DNC	IO	PD	455	IO	PD	455
9	NC	FLOAT	none	none	FLOAT	none	none
10	DNC	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	I	PD	6	I	PD	6
15	RX_DV	I	PD	6	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	GND_ESC	FLOAT	none	none	FLOAT	none	none
18	GND_ESC	FLOAT	none	none	FLOAT	none	none
19	DNC	FLOAT	none	none	FLOAT	none	none
20	DNC	FLOAT	none	none	FLOAT	none	none
21	DNC	FLOAT	none	none	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	I	PD	9	O	none	none
24	RX_D2	I	PD	9	O	none	none
25	RX_D1	I	PD	9	O	none	none
26	RX_D0	I	PD	9	O	none	none
27	RX_CLK	I	PD	9	O	none	none
28	TX_CLK	I	PD	9	I	none	none
29	TX_EN	I	PD	9	I	none	none
30	TX_D3	I	PD	9	I	none	none
31	TX_D2	I	PD	9	I	none	none
32	TX_D1	I	PD	9	I	none	none
33	TX_D0	I	PD	9	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

Table 5-5. Pin States - MII and RGMII

PIN NO	PIN NAME	MII			RGMII		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VDDA	SUPPLY	none	none	SUPPLY	none	none
8	DNC	IO	PD	455	IO	PD	455
9	NC	FLOAT	none	none	FLOAT	none	none
10	DNC	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	O	none	none	I	PD	6
15	RX_DV	O	none	none	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	GND_ESC	FLOAT	none	none	FLOAT	none	none
18	GND_ESC	FLOAT	none	none	FLOAT	none	none
19	DNC	FLOAT	none	none	FLOAT	none	none
20	DNC	FLOAT	none	none	FLOAT	none	none
21	DNC	FLOAT	none	none	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	O	none	none	O	none	none
24	RX_D2	O	none	none	O	none	none
25	RX_D1	O	none	none	O	none	none
26	RX_D0	O	none	none	O	none	none
27	RX_CLK	O	none	none	O	none	none
28	TX_CLK	O	none	none	I	none	none
29	TX_EN	I	none	none	I	none	none
30	TX_D3	I	none	none	I	none	none
31	TX_D2	I	none	none	I	none	none
32	TX_D1	I	none	none	I	none	none
33	TX_D0	I	none	none	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

Table 5-6. Pin States - RMII LEADER and RMII FOLLOWER

PIN NO	PIN NAME	RMII LEADER			RMII FOLLOWER		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VDDA	SUPPLY	none	none	SUPPLY	none	none
8	DNC	IO	PD	455	IO	PD	455
9	NC	FLOAT	none	none	FLOAT	none	none
10	DNC	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	O	none	none	O	none	none
15	RX_DV	O	none	none	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	GND_ESC	FLOAT	none	none	FLOAT	none	none
18	GND_ESC	FLOAT	none	none	FLOAT	none	none
19	DNC	FLOAT	none	none	FLOAT	none	none
20	DNC	FLOAT	none	none	FLOAT	none	none
21	DNC	FLOAT	none	none	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	O, 50MHz	none	none	I	PD	9
24	RX_D2	I	PD	9	I	PD	9
25	RX_D1	O	none	none	O	none	none
26	RX_D0	O	none	none	O	none	none
27	RX_CLK	I	PD	9	I	PD	9
28	TX_CLK	I	none	none	I	none	none
29	TX_EN	I	none	none	I	none	none
30	TX_D3	I	none	none	I	none	none
31	TX_D2	I	none	none	I	none	none
32	TX_D1	I	none	none	I	none	none
33	TX_D0	I	none	none	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

Table 5-7. Pin States - SGMII

PIN NO	PIN NAME	SGMII		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1	O	none	none
7	VDDA	SUPPLY	none	none
8	DNC	IO	PD	455
9	NC	FLOAT	none	none
10	DNC	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT	O	none	none
17	GND_ESC	FLOAT	none	none
18	GND_ESC	FLOAT	none	none
19	DNC	FLOAT	none	none
20	DNC	FLOAT	none	none
21	DNC	FLOAT	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	O	none	none
24	RX_D2	O	none	none
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	O	none	none
36	MDIO	OD, IO	none	none

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
Input Voltage	VDDA	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (3.3V)	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (2.5V)	–0.3		4	V
Input Voltage	VDDIO/VDDMAC (1.8V)	–0.3		4	V
Pins	MDI	–0.3		4	V
Pins	MAC interface	–0.3		VDDMAC + 0.3	V
Pins	MDIO, MDC, GPIO, XI, XO, INT, RESET, CLKOUT	–0.3		VDDIO + 0.3	V
DC Output Voltage	All Pins	–0.3		4	V
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
			TRD_N, TRD_P pins	±8000	
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±750	
		IEC 61000-4-2 contact discharge	TRD_N, TRD_P pins	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIO / VDDMAC	IO Supply Voltage, 1.8V operation	1.62	1.8	1.98	V
	IO Supply Voltage, 2.5V operation	2.25	2.5	2.75	
	IO Supply Voltage, 3.3V operation	2.97	3.3	3.63	
VDDA	Core Supply Voltage, 3.3V	2.97	3.3	3.63	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DP83TC814 RHA (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
100BASE-T1 PMA CONFORMANCE						
V_{OD-MDI}	Output Differential Voltage	$R_{L(diff)}$ = 100Ω			2.2	V
$R_{MDI-Diff}$	Integrated Differential Output Termination	TRD_P and TRD_M		100		Ω
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±10%, 2-level strap	0		0.8	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±10%, 2-level strap	2		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±10%, 2-level strap	0		0.7	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±10%, 2-level strap	1.5		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±10%, 2-level strap	0		0.35 × VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±10%, 2-level strap	0.65 × VDDIO		VDDIO	V
BOOTSTRAP DC CHARACTERISTICS (3 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0		0.18 × VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0.22 × VDDIO		0.42 × VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 3.3V ±10%, 3-level strap	0.46 × VDDIO		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0		0.19 × VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0.27 × VDDIO		0.41 × VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 2.5V ±10%, 3-level strap	0.58 × VDDIO		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0		0.35 × VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0.40 × VDDIO		0.75 × VDDIO	V

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 1.8V ±10%, 3-level strap	0.84 × VDDIO		VDDIO	V
IO CHARACTERISTICS						
V_{IH}	High Level Input Voltage	VDDIO = 3.3V ±10%	2			V
V_{IL}	Low Level Input Voltage	VDDIO = 3.3V ±10%			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±10%	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ±10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 2.5V ±10%	1.7			V
V_{IL}	Low Level Input Voltage	VDDIO = 2.5V ±10%			0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ±10%	2			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 2.5V ±10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 1.8V ±10%	0.65 × VDDIO			V
V_{IL}	Low Level Input Voltage	VDDIO = 1.8V ±10%			0.35 × VDDIO	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±10%	VDDIO-0.45			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ±10%			0.45	V
I_{IH}	Input High Current(1)	T_A = -40°C to 125°C, VIN=VDDIO, All pins except XI	-10		10	µA
I_{IH-XI}	Input High Current(1)	T_A = -40°C to 125°C, VIN=VDDIO, XI pin	-15		15	µA
I_{IL-XI}	Input Low Current(1)	T_A = -40°C to 125°C, VIN=GND, XI pin	-15		15	µA
I_{IL}	Input Low Current(1)	T_A = -40°C to 125°C, VIN=GND, All pins except XI pin	-10		10	µA
Iozh	Tri-state Output High Current	T_A = -40°C to 125°C, VIN=VDDIO, All pins except RX_CTRL and RX_ER	-10		10	µA
Iozh	Tri-state Output High Current	T_A = -40°C to 125°C, VIN=VDDIO, RX_CTRL and RX_ER	-52		52	µA
Iozl	Tri-state Output Low Current(2)	T_A = -40°C to 125°C, VOUT=GND	-10		10	µA
R_{pulldn}	Internal Pull Down Resistor	RX_D[3:0], RX_CLK, LED_0, LED_1	6.2	8.4	10.7	kΩ
R_{pulldn}	Internal Pull Down Resistor	RX_CTRL, RX_ER	4.725	5.8	7.2	kΩ
R_{pullup}	Internal Pull Up Resistor	INT, RESET	6.3	9	11.2	kΩ
XI V_{IH}	High Level Input Voltage		1.3		VDDIO	V
XI V_{IL}	Low Level Input Voltage				0.5	V
C_{IN}	Input Capacitance XI			1		pF
C_{IN}	Input Capacitance INPUT PINS			5		pF
C_{OUT}	Output Capacitance XO			1		pF

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output Capacitance OUTPUT PINS			5		pF
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK	35	50	65	Ω
POWER CONSUMPTION						
I(3V3)	MII	-40°C to 125°C		57	63	mA
I(3V3)	RMII	-40°C to 125°C		57	63	mA
I(3V3)	RGMII	-40°C to 125°C		57	63	mA
I(3V3)	SGMII	-40°C to 125°C		81	95	mA
I(VDDIO=3.3V)	MII	-40°C to 125°C, VDDIO = VDDMAC		19	24	mA
I(VDDIO=3.3V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		18	23	mA
I(VDDIO=3.3V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		13	21	mA
I(VDDIO=3.3V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		7	12	mA
I(VDDIO=2.5V)	MII	-40°C to 125°C, VDDIO = VDDMAC		12	18	mA
I(VDDIO=2.5V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		12	17	mA
I(VDDIO=2.5V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		12	16	mA
I(VDDIO=2.5V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		6	9	mA
I(VDDIO=1.8V)	MII	-40°C to 125°C, VDDIO = VDDMAC		9	13	mA
I(VDDIO=1.8V)	RMII	-40°C to 125°C, VDDIO = VDDMAC		9	13	mA
I(VDDIO=1.8V)	RGMII	-40°C to 125°C, VDDIO = VDDMAC		9	12	mA
I(VDDIO=1.8V)	SGMII	-40°C to 125°C, VDDIO = VDDMAC		4	6	mA
POWER CONSUMPTION (LOW POWER MODE)						
I(VDDA3V3)	IEEE Power Down	-40°C to 125°C, All interfaces		8	22	mA
I(VDDA3V3)	RESET	-40°C to 125°C, All interfaces		9	23	mA
I(VDDA3V3)	Standby	-40°C to 125°C, MII		15	33	mA
I(VDDA3V3)	Standby	-40°C to 125°C, RMII		15	30	mA
I(VDDA3V3)	Standby	-40°C to 125°C, RGMII		15	30	mA
I(VDDA3V3)	Standby	-40°C to 125°C, SGMII		15	30	mA
I(VDDIO=3.3V)	IEEE Power Down	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		15	23	mA
I(VDDIO=3.3V)	RESET	-40°C to 125°C, All interfaces, VDDIO=VDDMAC		15	23	mA

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, MII, VDDIO=VDDMAC		19	25	mA
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, RMII, VDDIO=VDDMAC		16	20	mA
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, RGMII, VDDIO=VDDMAC		14	20	mA
I(VDDIO=3.3V)	Standby	-40℃ to 125℃, SGMII, VDDIO=VDDMAC		14	16	mA
I(VDDIO=2.5V)	IEEE Power Down	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		10	16	mA
I(VDDIO=2.5V)	RESET	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		10	16	mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, MII, VDDIO=VDDMAC		14	18	mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, RMII, VDDIO=VDDMAC		11	14	mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, RGMII, VDDIO=VDDMAC		9	14	mA
I(VDDIO=2.5V)	Standby	-40℃ to 125℃, SGMII, VDDIO=VDDMAC		9	14	mA
I(VDDIO=1.8V)	IEEE Power Down	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		7	11	mA
I(VDDIO=1.8V)	RESET	-40℃ to 125℃, All interfaces, VDDIO=VDDMAC		7	11	mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, MII, VDDIO=VDDMAC		10	12	mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, RMII, VDDIO=VDDMAC		7	11	mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, RGMII, VDDIO=VDDMAC		6	11	mA
I(VDDIO=1.8V)	Standby	-40℃ to 125℃, SGMII, VDDIO=VDDMAC		6	11	mA
SGMII Input						
V_{IDTH}	Input differential voltage tolerance	SI_P and SI_N, AC coupled	0.1			V
$R_{IN-DIFF}$	Receiver differential input impedance (DC)		80		120	Ω
SGMII Output						
	Clock signal duty cycle	SO_P and SO_N, AC coupled, 0101010101 pattern	48		52	%
	Output Differential Voltage	SO_P and SO_N, AC coupled	150		400	mV
Voltage Sensor						
VDDA	VDDA Sensor Range	-40℃ to +125℃	2.7	3.3	4	V
	VDDA Sensor Resolution (LSB)	-40℃ to +125℃		8.8		mV
	VDDA Sensor Accuracy (voltage and temperature variation on single part)	-40℃ to +125℃	-120		120	mV
	VDDA Sensor Accuracy (part-part variation)	-40℃ to +125℃	-50		50	mV

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDIO / VDDMAC	VDDIO / VDDMAC Sensor Range	-40℃ to +125℃	1.44		3.9	V
	VDDIO / VDDMAC Sensor Resolution (LSB)	-40℃ to +125℃		16		mV
	VDDIO / VDDMAC Sensor Accuracy (voltage and temperature variation on single part)	-40℃ to +125℃	-144		144	mV
	VDDIO / VDDMAC Sensor Accuracy (part-part variation)	-40℃ to +125℃	-85		85	mV

(1) For pins: MDC, TX_CLK, TX_CTRL, TX_D[3:0], and RESET_N
(2) For pins: RX_D[3:0], RX_CLK, RX_CTRL, MDIO, INT_N, and XO.

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
MII TIMING						
T1.1	TX_CLK High / Low Time		16	20	24	ns
T1.2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK		10			ns
T1.3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK		0			ns
T2.1	RX_CLK High / Low Time		16	20	24	ns
T2.2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising		10		30	ns
RMII LEADER TIMING						
T3.1	RMII Leader Clock Period			20		ns
	RMII Leader Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to RMII Leader Clock		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from RMII Leader Clock		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from RMII Leader Clock rising edge		4	10	14	ns
RMII FOLLOWER TIMING						
T3.1	Input Reference Clock Period			20		ns
	Reference Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to XI Clock rising		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from XI Clock rising		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from XI Clock rising		4		14	ns
RGMII INPUT TIMING						
T_{cyc}	Clock Cycle Duration	TX_CLK	36	40	44	ns
$T_{setup(align)}$	TX_D[3:0], TX_CTRL Setup to TX_CLK (Align Mode)		1	2		ns
$T_{hold(align)}$	TX_D[3:0], TX_CTRL Hold from TX_CLK (Align Mode)		1	2		ns
RGMII OUTPUT TIMING						
$T_{skew(align)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Align Mode Enabled)	On PHY Pins	-750		750	ps
$T_{setup(shift)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled, default)	On PHY Pins	2			ns
T_{cyc}	Clock Cycle Duration	RX_CLK	36	40	44	ns
Duty_G	Duty Cycle	RX_CLK	45	50	55	%
Tr/Tf	Rise / Fall Time (20% to 80%)	C_{LOAD} = 5pF			1.2	ns
SMI TIMING						
T4.1	MDC to MDIO (Output) Delay Time	25pF load capacitance	0		40	ns
T4.2	MDIO (Input) to MDC Setup Time		10			ns
T4.3	MDIO (Input) to MDC Hold Time		10			ns
	MDC Frequency			2.5	20	MHz
POWER-UP TIMING						
T5.1	Supply ramp time: For all supplies (1)		0.2		8	ms
T5.3	XTAL Startup / Settling: Powerup to XI good/stabilized			0.35		ms
T5.4	Internal Oscillator stabilization time from power up				10	ms
	Last Supply power up To Reset Release				10	ms
T5.5	Post power-up to SMI ready: Post Power-up wait time required before MDC preamble can be sent for register access		10			ms

6.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
T5.6	Power-up to Strap latch-in				10	ms
T5.7	CLKOUT Startup/Settling: Powerup to CLKOUT good/stabilized				10	ms
T5.8	Power-up to idle stream				10	ms
RESET TIMING (RESET_N)						
T6.1	Reset Pulse Width: Minimum Reset pulse width to be able to reset		720			ns
T6.2	Reset to SMI ready: Post reset wait time required before MDC preamble can be sent for register access		1			ms
T6.3	Reset to Strap latch-in: Hardware configuration pins transition to output drivers			40		µs
T6.4	Reset to idle stream				1800	µs
TRANSMIT LATENCY TIMING						
	MII Rising edge TX_CLK with assertion TX_EN to SSD symbol on MD		205		233	ns
	Follower RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI		374		409	ns
	Leader RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI		382		408	ns
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI		370		390	ns
	First symbol of SGMII to SSD symbol on MDI		420		456	ns
RECEIVE LATENCY TIMING						
	SSD symbol on MDI to MII Rising edge of RX_CLK with assertion of RX_DV		467		491	ns
	SSD symbol on MDI to Follower RMII Rising edge of XI clock with assertion of CRS_DV		527		574	ns
	SSD symbol on MDI to Leader RMII Rising edge of Leader clock with assertion of CRS_DV		521		557	ns
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL		484		511	ns
	SSD symbol on MDI to first symbol of SGMII		708		788	ns
25MHz OSCILLATOR REQUIREMENTS						
	Frequency Tolerance		-100		+100	ppm
	Rise / Fall Time (10%-90%)				8	ns
	Jitter Tolerance (RMS)				25	ps
	XI Duty Cycle in external clock mode		40		60	%
50MHz OSCILLATOR REQUIREMENTS						
	Frequency			50		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Rise / Fall Time (10% - 90%)				4	ns
	Duty Cycle		35		65	%
25MHz CRYSTAL REQUIREMENTS						
	Frequency			25		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Equivalent Series Resistance				100	Ω
OUTPUT CLOCK TIMING (25 MHz)						
	Frequency (PPM)		-100		100	-

6.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Duty Cycle		40		60	%
	Rise Time				5000	ps
	Fall Time				5000	ps
	Jitter (Short Term)				1000	ps
	Frequency			25		MHz

(1) For supplies with ramp rate longer than 8ms, a RESET pulse is required after the last supply becomes stable.

6.7 Timing Diagrams

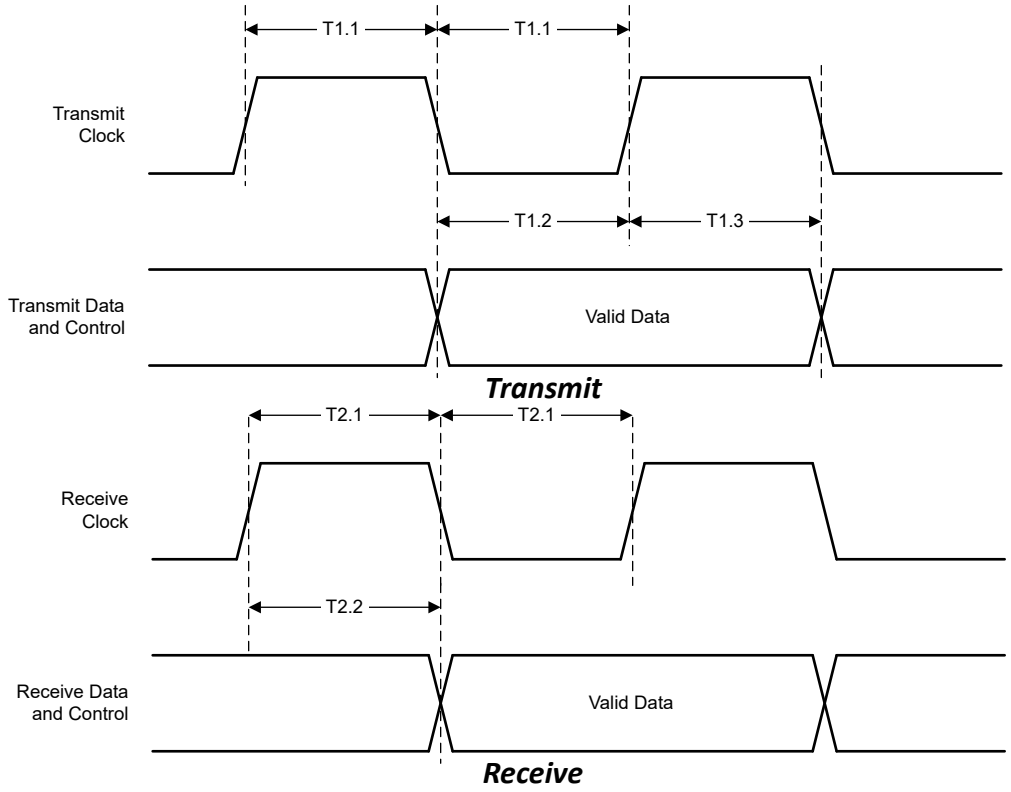


Figure 6-1. MII Timing

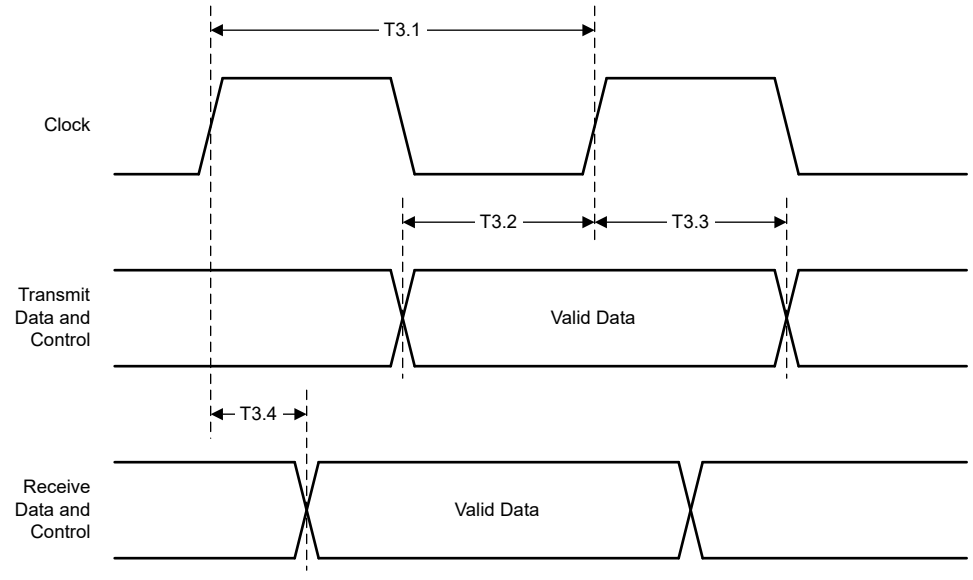


Figure 6-2. RMII Transmit and Receive Timing

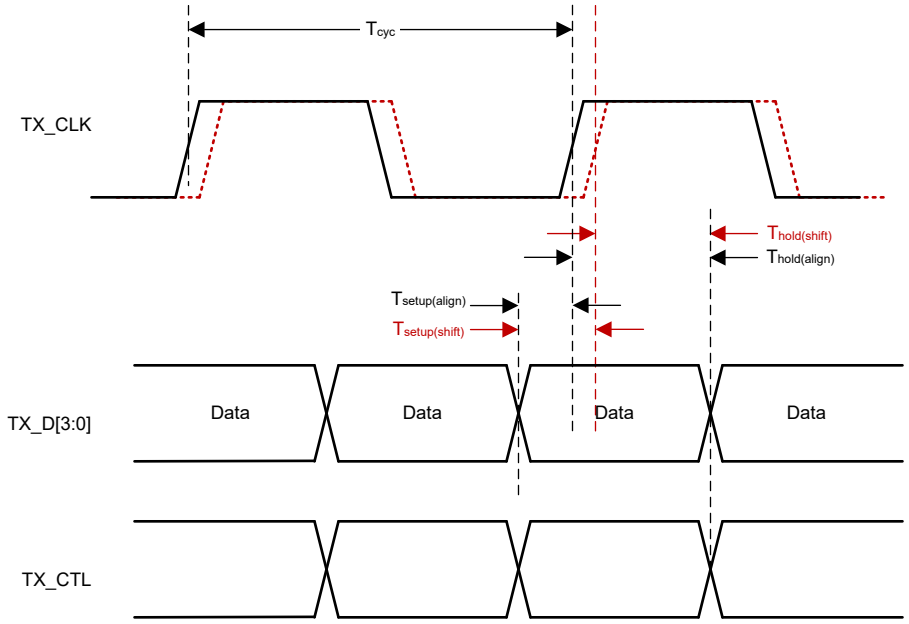


Figure 6-3. RGMII Transmit Timing

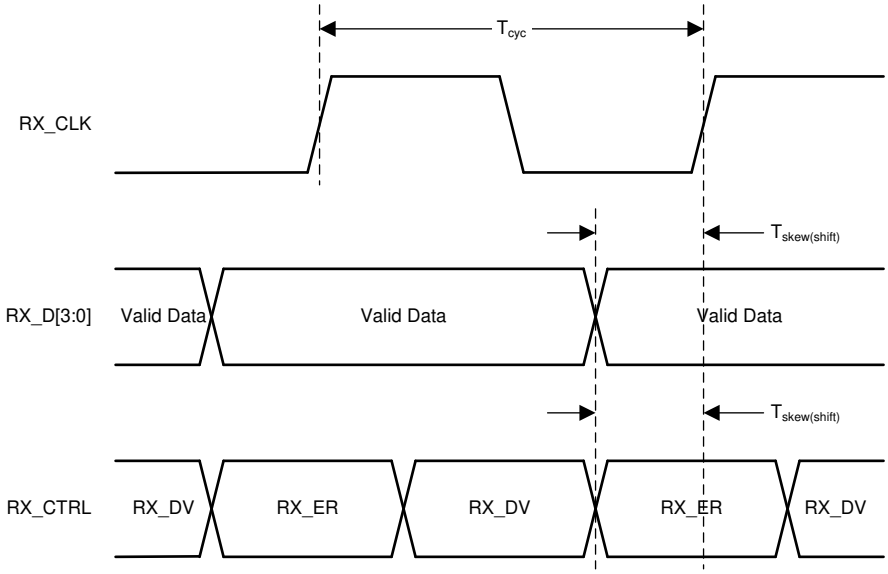


Figure 6-4. RGMII Receive Timing (Internal Delay Enabled)

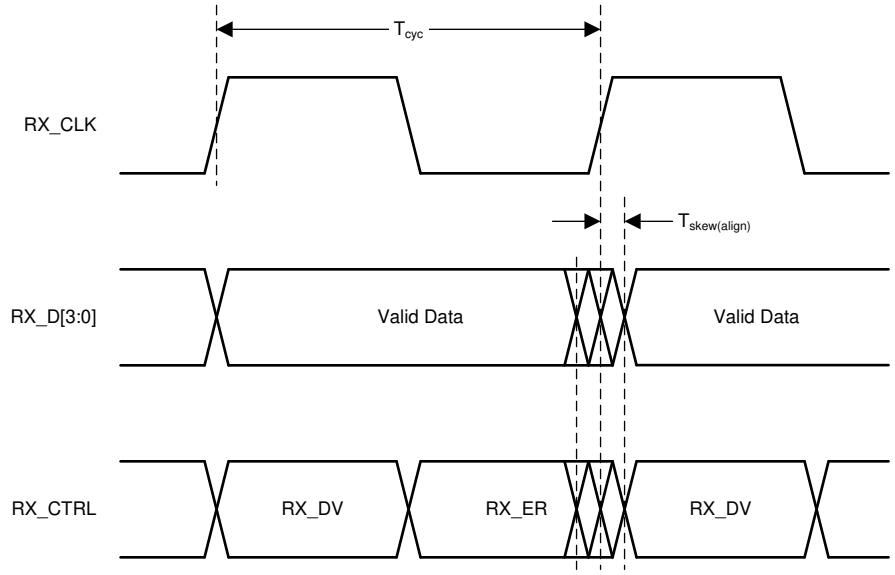


Figure 6-5. RGMII Receive Timing (Internal Delay Disabled)

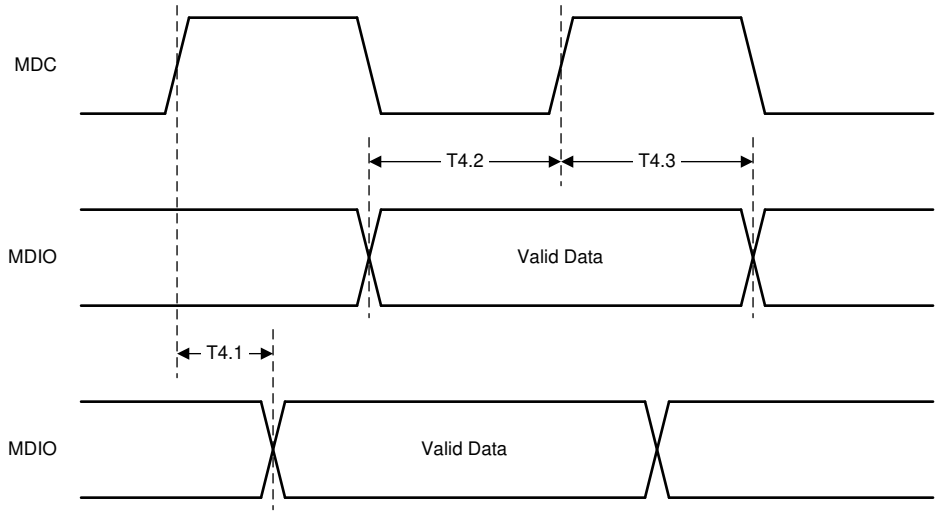


Figure 6-6. Serial Management Timing

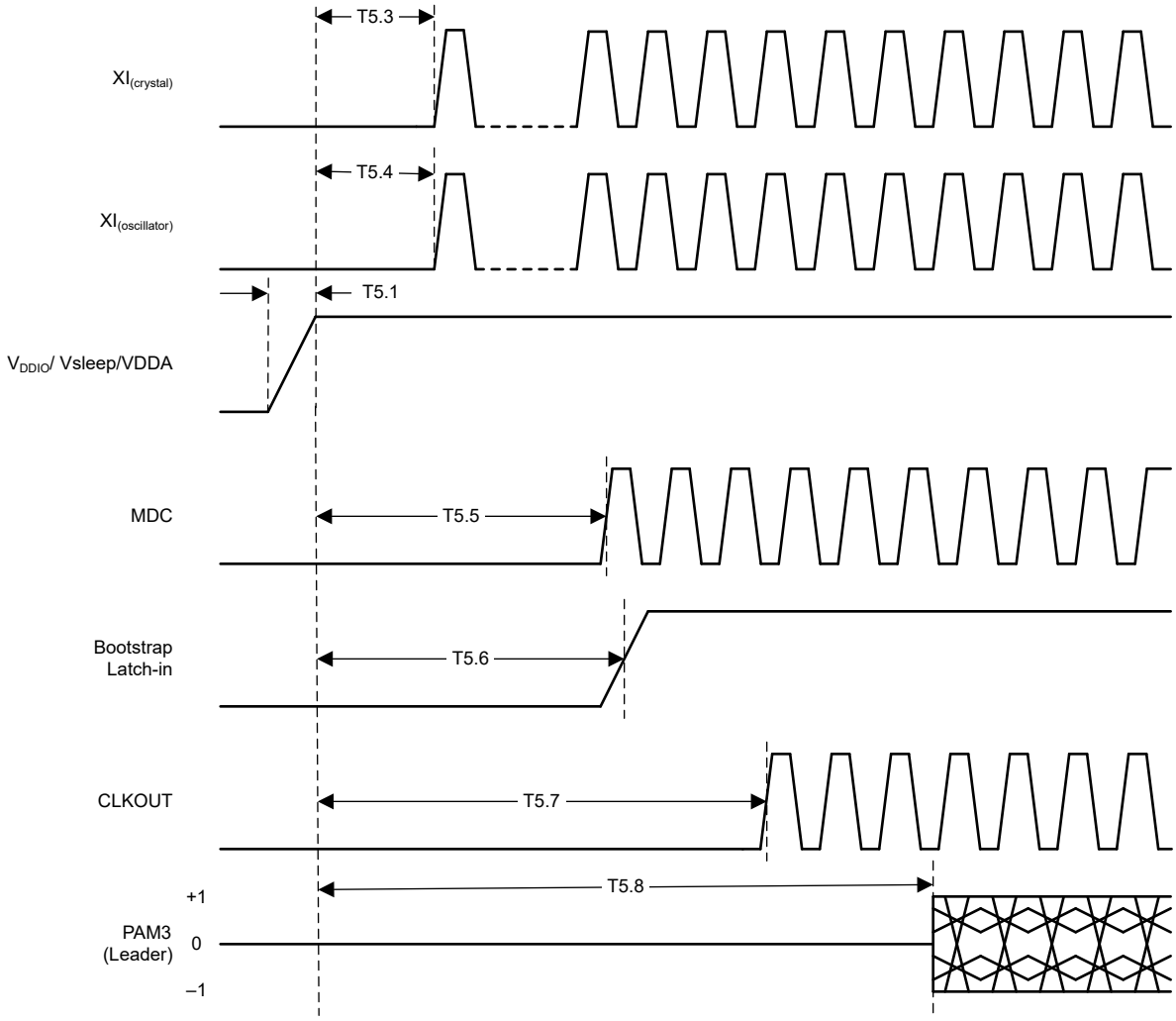


Figure 6-7. Power-Up Timing

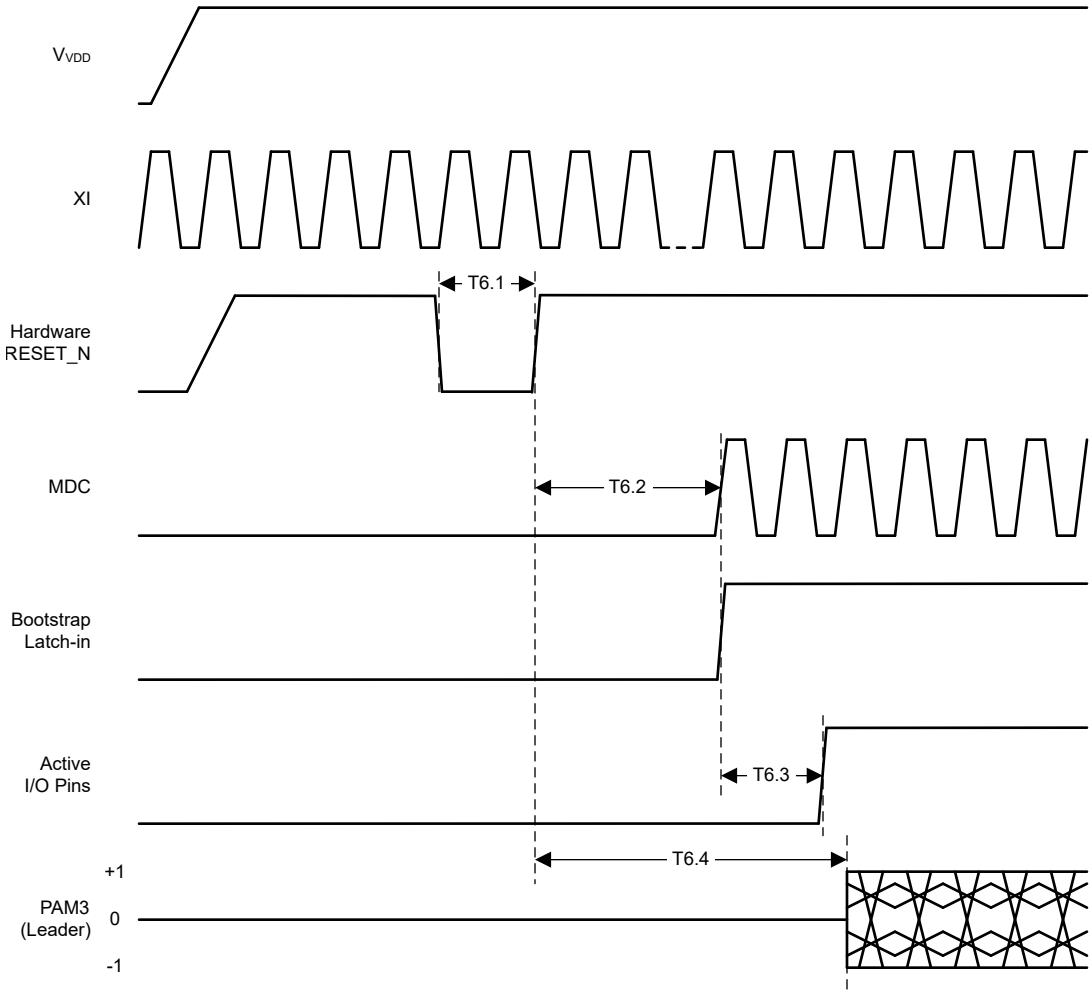
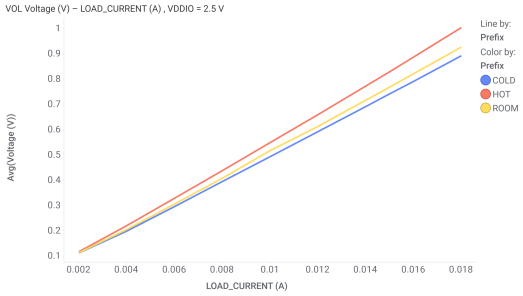


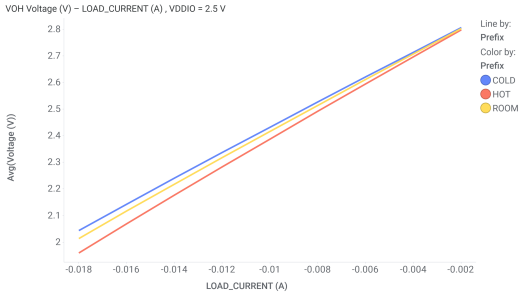
Figure 6-8. Reset Timing

6.8 Typical Characteristics



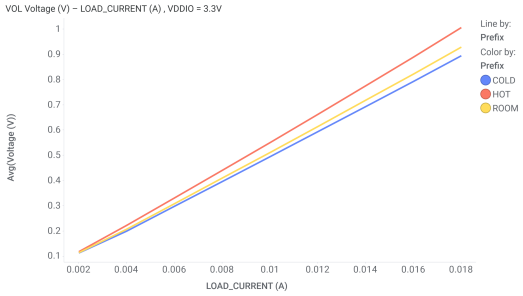
VDDIO = 2.5V

Figure 6-9. LED Pins VOL (2.5V)



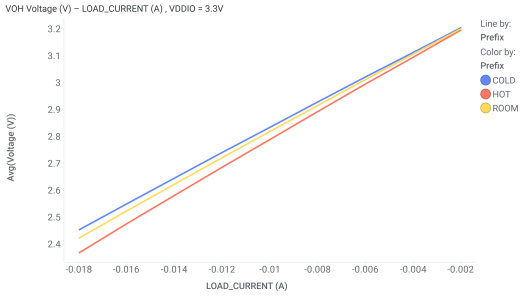
VDDIO = 2.5V

Figure 6-10. LED Pins VOH (2.5V)



VDDIO = 3.3V

Figure 6-11. LED Pins VOL (3.3V)



VDDIO = 3.3V

Figure 6-12. LED Pins VOH (3.3V)

7 Detailed Description

7.1 Overview

The DP83TC814S-Q1 is a 100BASE-T1 automotive Ethernet Physical Layer transceiver. The device is IEEE 802.3bw compliant and AEC-Q100 qualified for automotive applications. The DP83TC814S-Q1 is interoperable with both BroadR-Reach PHYs and 100BASE-T1 PHYs.

This device is specifically designed to operate at 100Mbps speed while meeting stringent automotive EMC limits. The DP83TC814S-Q1 transmits PAM3 ternary symbols at 66.667MHz over unshielded single twisted-pair cable. The device is application flexible; supporting MII, RMII, RGMII, and SGMII in a single 36-pin VQFN wettable flank package.

There is an extensive Diagnostic Tool Kit within the DP83TC814S-Q1 for both in-system use as well as debug, compliance and system prototyping for bring-up. The DP83TC814S-Q1 can meet IEC61000-4-2 Level 4 electrostatic discharge limits and the device also includes an on-chip ESD sensor for detecting ESD events in real-time.

7.2 Functional Block Diagram

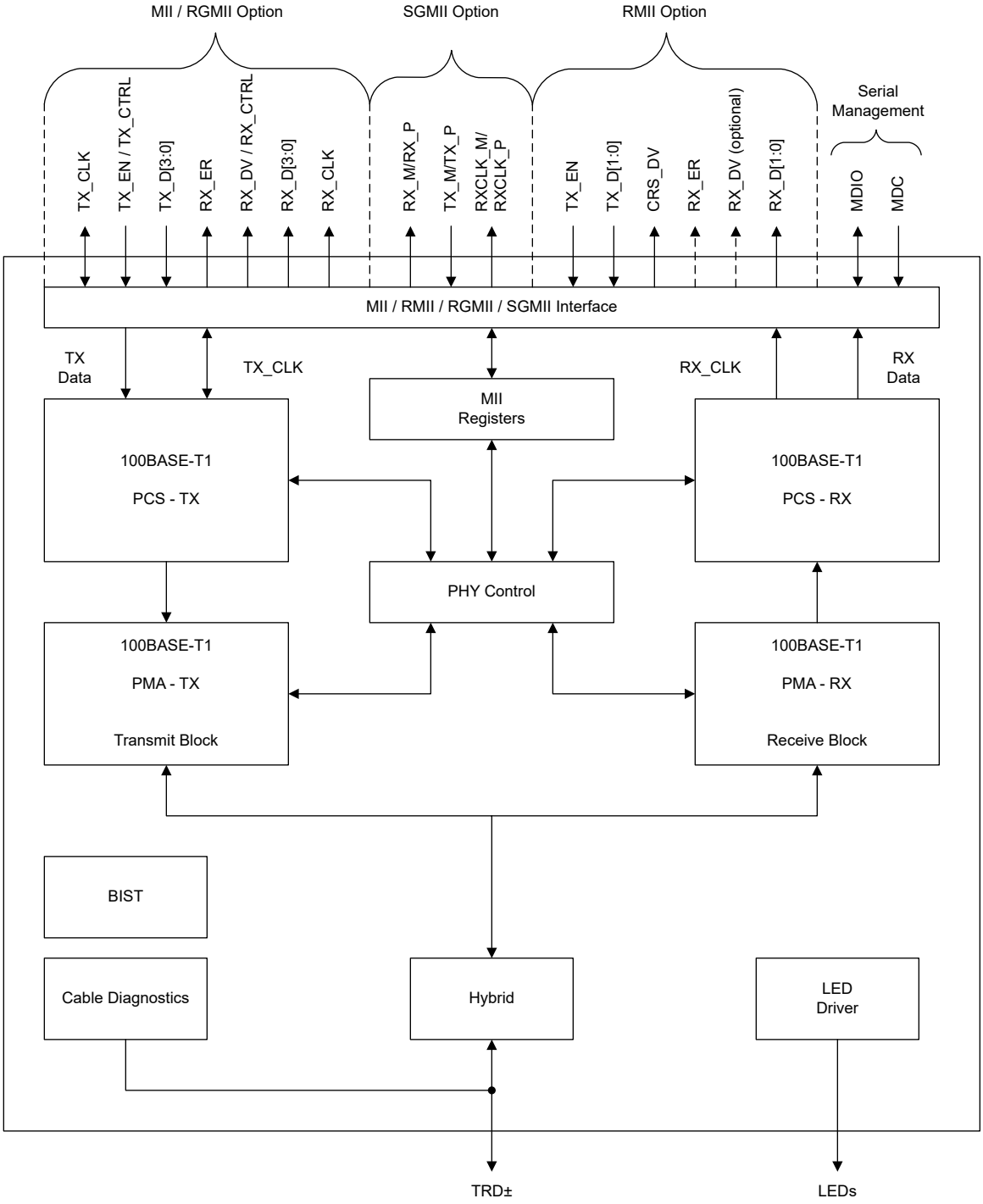


Figure 7-1. DP83TC814S-Q1

7.3 Feature Description

Note

Refer to the *DP83TC812, DP83TC813, and DP83TC814: Configuring for Open Alliance Specification Compliance* application note for more information about the register settings used for compliance testing. Use these register settings to achieve the same performance as observed during compliance testing.

7.3.1 Diagnostic Tool Kit

The DP83TC814 diagnostic tool kit provides mechanisms for monitoring normal operation, device-level debugging, system-level debugging, fault detection, and compliance testing. This tool kit includes a built-in self-test with PRBS data, various loopback modes, Signal Quality Indicator (SQI), Time Domain Reflectometry (TDR), undervoltage monitor, electrostatic discharge monitor, and IEEE 802.3bw test modes.

7.3.1.1 Signal Quality Indicator

When the DP83TC814S-Q1 is active, the Signal Quality Indicator can be used to determine the quality of link based on SNR readings made by the device. SQI is presented as a 8-level indication. Signal quality indication is accessible through register 0x871. SQI is continuously monitored by the PHY to allow for real-time link signal quality status.

Bits[3:1] in register 0x871 provide SQI value while bits [7:5] provide the worst SQI value since the last read. The SQI value reported in register 0x871[3:1] map directly to the SQI levels required by Open Alliance.

To get the most accurate SQI reporting, use the initialization routine explained in SNLA389 application note.

Table 7-1. Signal Quality Indicator

REG 0x871[3:1]	OPEN ALLIANCE SQI LEVEL	LINK QUALITY
0x0	0 (Worst)	Poor/ No Link
0x1	1	
0x2	2	
0x3	3	
0x4	4	Good / Excellent Link
0x5	5	
0x6	6	
0x7	7 (Best)	

7.3.1.2 Electrostatic Discharge Sensing

Electrostatic discharge is a serious issue for electronic circuits and if not properly mitigated can create short-term issues (signal integrity, link drops, packet loss) as well as long-term reliability faults. The DP83TC814 has robust integrated ESD circuitry and offers an ESD sensing architecture. ESD events can be detected on MDI pins independently for further analysis and debug.

Additionally, the DP83TC814 provides an interrupt status flag; *Register 0x12[11]* is set when an ESD event is logged. This interrupt can be routed to the INT_N pin using bit[3] of the same register. *Register 0x442[14:9]* store the number of ESD events that have occurred since power-up. Hardware and software resets are ignored by the ESDS register to prevent unwarranted clearing.

7.3.1.3 Time Domain Reflectometry

Time domain reflectometry helps determine the quality of the cable, connectors and terminations in addition to estimating OPEN and SHORT faults along a cable. The DP83TC814-Q1 transmits a test pulse down the attached twisted-pair cable. Transmitted pulses continue down the cable and reflect from each imperfection and fault, allowing the device to measure the time to return and strength (amplitude) of all reflections. This technique enables the DP83TC814-Q1 to identify cable OPENs and SHORTs.

TDR is activated by setting bit[15] in register 0x1E. The procedure is as follows.

- Configure the DP83TC814-Q1 as per the initialization settings from SNLA389 Application Note
- Verify that the Link Partner connected to the PHY is silent. Link is down during TDR execution.
- Run the Pre-TDR configuration settings as listed in SNLA389.
- Start TDR by setting register 0x1E[15] to '1'.
- Wait 100ms, read register 0x1E[1:0]
  - If the register reads 0b10 then TDR has executed successfully.
- If TDR executed successfully then read register 0x310 to get TDR results.
  - 0x310[7]: 0 = Cable fault not detected or 1 = Cable fault detected
  - 0x310[6]: 0 = Cable fault is SHORT or 1 = Cable fault is OPEN
  - If valid cable fault is detected then 0x310[5:0] stores the location value in meters.

7.3.1.4 Voltage Sensing

The DP83TC814 offers sensors for monitoring voltage at the supply pins. Undervoltage monitoring are always active in the DP83TC814 by default. If an undervoltage condition is detected, interrupt status flag is set in register 0x0013. These interrupts can also be optionally routed to the INT pin using the same register.

The following method must be used to read each sensor.

- Step 1: Program register 0x0467 = 0x6004 ; Initial configuration of monitors
- Step 2: Program register 0x046A = 0x00A3; Enable Monitors
- Step 3: Configure register 0x0468 with the corresponding setting to select the required sensor.
  - VDDA Sensor: Use 0x0468 = 0x0920
  - VSLEEP Sensor: Use 0x0468 = 0x1920
  - VDDMAC Sensor: Use 0x0468 = 0x2920
  - VDDIO Sensor: Use 0x0468 = 0x3920
- Step 4: Read register 0x047B[14:7] and convert this output code to decimal.
- Step 5: Use the output code in the following equations to get the absolute value of the sensor. Refer to Table 7-2 table for constant values for corresponding sensors.
  - vdda_value = 3.3 + (vdda_output_code - vdda_output_mean_code)*slope_vdda_sensor
  - vsleep_value = 3.3 + (vsleep_output_code - vsleep_output_mean_code)*slope_vsleep_sensor
  - vddmac_value = 3.3 + (vddmac_output_code - vddmac_output_mean_code)*slope_vddmac_sensor
  - vddio_value = 3.3 + (vddio_output_code - vddio_output_mean_code)*slope_vddio_sensor

Table 7-2. Sensors Constant Values

SENSOR	CONSTANT	VALUE
VDDA	vdda_output_mean_code	126
	slope_vdda_sensor	0.0088
VSLEEP	vsleep_output_mean_code	134
	slope_vsleep_sensor	0.0088
VDDMAC	vddmac_output_mean_code	205
	slope_vddmac_sensor	0.016
VDDIO	vddio_output_mean_code	205
	slope_vddio_sensor	0.016

7.3.1.5 BIST and Loopback Modes

DP83TC814 incorporates a data-path's Built-In-Self-Test (BIST) to check the PHY level and system level data-paths. BIST has following integrated features which make the system level data transfer tests (through-put etc) and diagnostics possible without relying on MAC or external data generator hardware/software.

The following features are available in the DP83TC814 which can be used for easy evaluation.

1. Loopback modes
2. Data Generator
   a. Customizable MAC packets generator
   b. Transmitted packet counter
   c. PRBS stream generator
3. Data Checker
   a. Received MAC packets error checker
   b. Received packet counter: Counts total packets received and packets received with errors
   c. PRBS lock and PRBS error checker

7.3.1.5.1 Data Generator and Checker

DP83TC814 supports inbuilt Pseudo-random data generator and checker which can be used in conjunction with Loopback modes to check the data path. Data generator can be programmed to generate either user defined MAC packets or PRBS stream.

Following parameters of generated MAC packets can be configured (refer to registers<0x061B>,register<0x061A> and register<0x0624> for required configuration):

- Packet Length
- Inter-packet gap
- Defined number of packets to be sent or continuous transmission
- Packet data-type: Incremental/Fixed/PRBS
- Number of valid bytes per packet

7.3.1.5.2 xMII Loopback

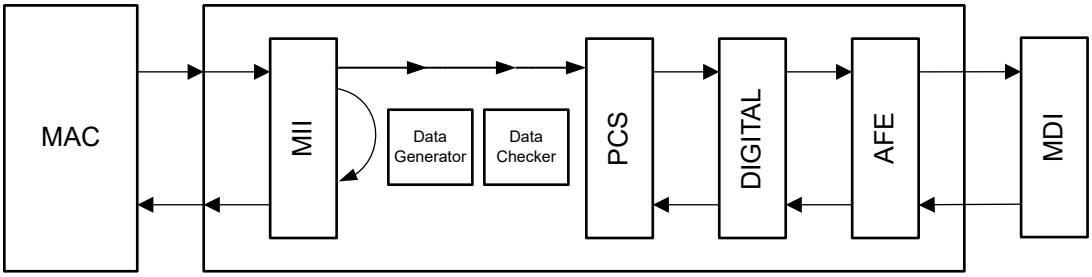


Figure 7-2. xMII Loopback Without Data Generator

xMII Loopback is the shallowest loop through the PHY. xMII Loopback is a useful test mode to validate communications between the MAC and the PHY. When in xMII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83TC814 to the RX pins where the device can be checked by the MAC. There is no link indication when in xMII loopback.

Enable Loopback

Write register 0x0000 = 0x6100

Enable Data Generator/checker for MAC Side

Data is generated externally on the MAC TX pins.

Use the following register settings to enable checker depending on the MAC interface mode.

- For RGMII, write register 0x0619 = 0x1004
- For SGMII, write register 0x0619 = 0x1114
- For RMII, write register 0x0619 = 0x1224
- For MII, write register 0x0619 = 0x1334

Check Incoming Data From MAC Side

Data can be verified at MAC interface RX pins.

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E. The registers must be read together and in this order.

Enable Data Generator/checker for Cable Side

Not applicable as data is generated externally on the MAC interface TX pins.

Check Data for Cable Side

Not applicable as PRBS stream checker works with only internal PRBS generator.

Other System Requirements

Generated data is going to cable side.

7.3.1.5.3 PCS Loopback

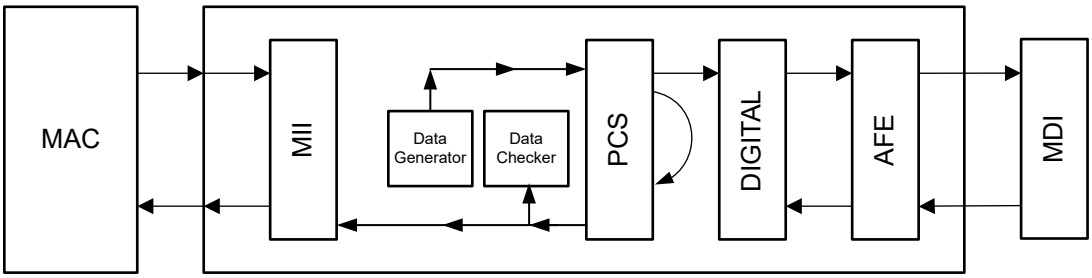


Figure 7-3. PCS Loopback With Data Generator

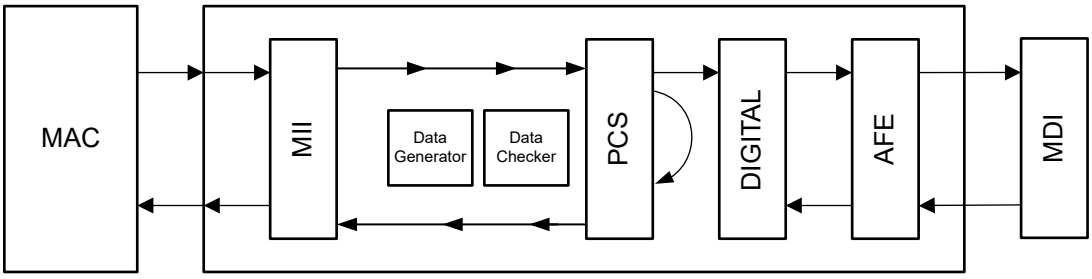


Figure 7-4. PCS Loopback Without Data Generator

PCS Loopback loops back data prior to exiting the PCS and entering the PMA. Data received from the MAC on the transmit path is brought through the digital block within the PHY where the data is then routed back to the MAC through the receive path. The DP83TC814 receive PMA circuitry is configured for isolation to prevent contention.

Enable Loopback

Write register 0x0016 = 0x0102

Enable Data Generator/Checker For MAC Side

Write register 0x0624 = 0x55BF

Write register 0x0619 = 0x1555

Check Incoming Data From MAC Side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E. The registers must be read together and in this order.

Enable Data Generator/Checker For Cable Side

Write register 0x0624 = 0x55BF

Write register 0x0619 = 0x0557

Check Data For Cable Side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other System Requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.1.5.4 Digital Loopback

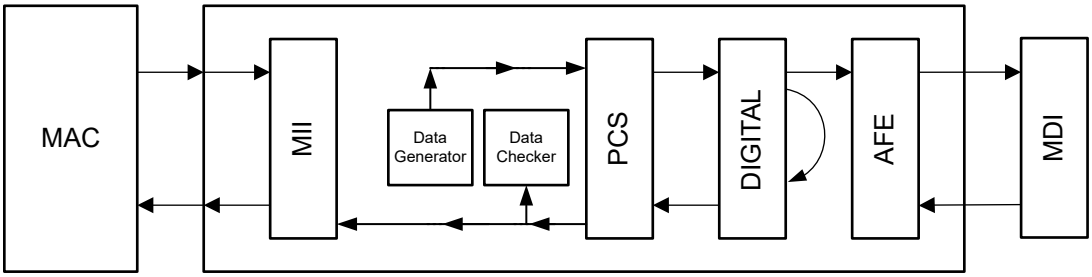


Figure 7-5. Digital Loopback With Data Generator

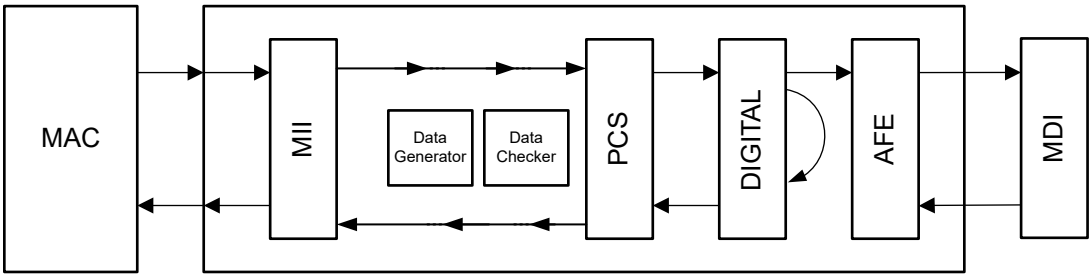


Figure 7-6. Digital Loopback Without Data Generator

Digital Loopback loops back data prior to exiting the Digital and entering the AFE. Data received from the MAC on the transmit path is brought through the digital block within the PHY where data is then routed back to the MAC through the receive path. The DP83TC814 receive Analog circuitry is configured for isolation to prevent contention.

Enable Loopback

Write register 0x0016 = 0x0104

Enable Data Generator/Checker for MAC Side

Write register 0x0624 = 0x55BF

Write register 0x0619 = 0x1555

Check Incoming Data From MAC Side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E. The registers must be read together and in this order.

Enable Data Generator/Checker for Cable Side

Write register 0x0624 = 0x55BF

Write register 0x0619 = 0x0557

Check Data for Cable Side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other System Requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.1.5.5 Analog Loopback

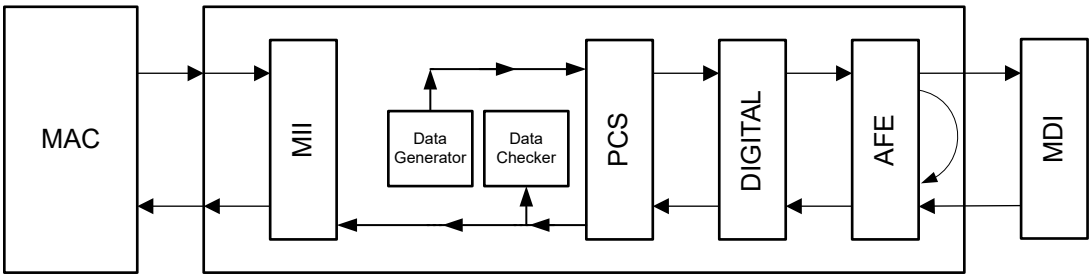


Figure 7-7. Analog Loopback With Data Generator

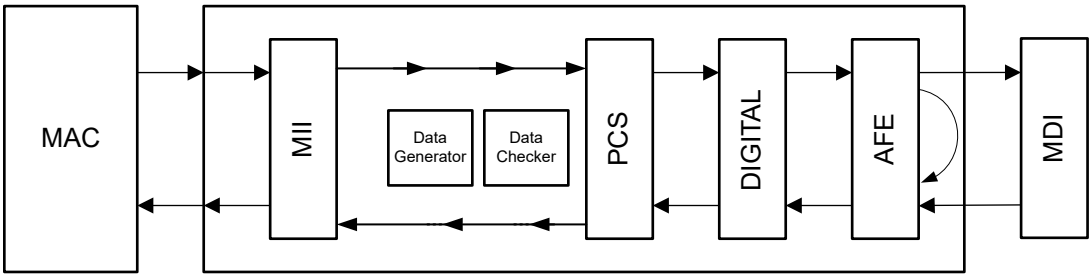


Figure 7-8. Analog Loopback Without Data Generator

Analog Loopback uses the echoed signals from the unterminated MDI and decodes these signals in the Hybrid to return the data to the MAC.

Enable Loopback

Write register 0x0016 = 0x0108

Enable Data Generator/checker For MAC Side

Write register 0x0624 = 0x55BF

Write register 0x0619 = 0x1555

Check Incoming Data From MAC Side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E. The registers must be read together and in this order.

Enable Data Generator/checker For Cable Side

Write register 0x0624 = 0x55BF

Write register 0x0619 = 0x0557

Check Data For Cable Side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other System Requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.1.5.6 Reverse Loopback

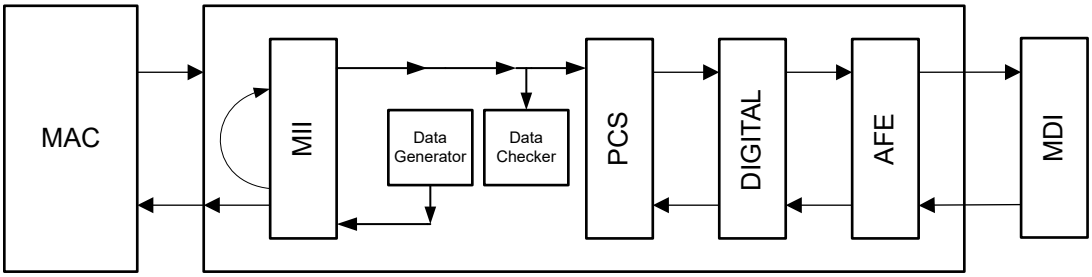


Figure 7-9. Reverse Loopback With Data Generator

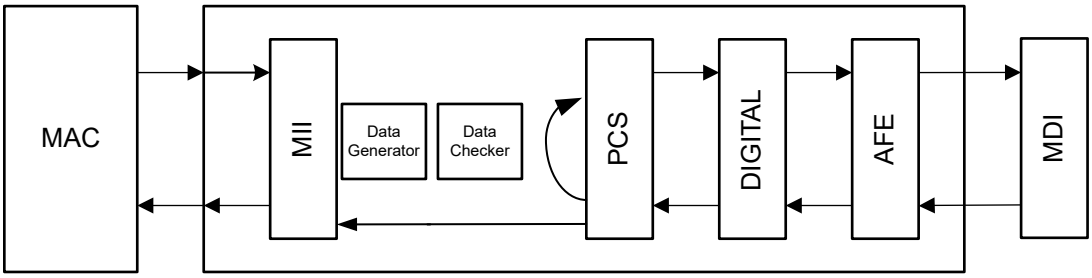


Figure 7-10. Reverse Loopback Without Data Generator

Reverse Loopback receives data on the MDI and passes data through the entire receive block where the data is then looped back within the PCS layer to the transmit block. The data is transmitted back out on the MDI to the attached Link Partner. To avoid contention, MAC transmit path is isolated.

Enable Loopback

Write register 0x0016 = 0x0110

Enable Data Generator/Checker For MAC Side

Write register 0x0624 = 0x55BF

Use the following register settings to enable checker depending on the MAC interface mode.

- For RGMII, write register 0x0619 = 0x1004
- For SGMII, write register 0x0619 = 0x1114
- For RMII, write register 0x0619 = 0x1224
- For MII, write register 0x0619 = 0x1334

Check Incoming Data From MAC Side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E. The registers must be read together and in this order.

Enable Data Generator/Checker For Cable Side

Write register 0x0624 = 0x55BF

Write register 0x0619 = 0x0557

Check Data For Cable Side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other System Requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.2 Compliance Test Modes

Note

Refer to SNLA389 Application Note for more information about the register settings used for compliance testing. Use these register settings to achieve the same performance as observed during compliance testing.

There are four PMA compliance test modes required in IEEE 802.3bw, sub-clause 96.5.2, which are all supported by the DP83TC814-Q1 . These compliance test modes include: transmitter waveform Power Spectral Density (PSD) mask, amplitude, distortion, 100BASE-T1 Leader jitter, 100BASE-T1 Follower jitter, droop, transmitter frequency, frequency tolerance, return loss, and mode conversion.

Any of the three GPIOs can be used to output TX_TCLK for the 100BASE-T1 Follower jitter measurement. For routing TX_TCLK to CLKOUT pin for 100BASE-T1 Follower Jitter measurement, write to register 0x045F = 0x000D. The device must be configured in Follower mode.

7.3.2.1 Test Mode 1

Test mode 1 evaluates transmitter droop. In test mode 1, the DP83TC814-Q1 transmits '+1' symbols for a minimum of 600ns followed by '–1' symbols for a minimum of 600ns. This pattern is repeated continuously until the test mode is disabled.

Test mode 1 is enabled by setting bits[15:13] = 0b001 in the MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.2.2 Test Mode 2

Test mode 2 evaluates the transmitter 100BASE-T1 Leader mode jitter. In test mode 2, the DP83TC814-Q1 transmits a {+1,-1} data symbol sequence. The transmitter synchronizes the transmitted symbols from the local reference clock.

Test mode 2 is enabled by setting bits[15:13] = 0b010 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.2.3 Test Mode 4

Test mode 4 evaluates the transmitter distortion. In test mode 4, the DP83TC814-Q1 transmits the sequence of symbols generated by Equation 1:

$$g(x) = 1 + x^9 + x^{11} \quad (1)$$

The bit sequences, x0n and x1n, are generated from combinations of the scrambler in accordance to Equation 2 and Equation 3:

$'x0_n = Scr_n[0]$ (2)

$x1_n = Scr_n[1] \wedge Scr_n[4]$ (3)

Example streams of the 3-bit nibbles are shown in Table 7-3.

Table 7-3. Transmitter Test Mode 4 Symbol Mapping

x1n	x0n	PAM3 SYMBOL
0	0	0
0	1	+1
1	0	0
1	1	–1

Test mode 4 is enabled by setting bits[15:13] = 0b100 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.2.4 Test Mode 5

Test mode 5 evaluates the transmitter PSD mask. In test mode 5, the DP83TC814-Q1 transmits a pseudo-random sequence of PAM3 symbols.

Test mode 5 is enabled by setting bits[15:13] = 0b101 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.4 Device Functional Modes

7.4.1 Power Down

When any of the supply rails are below the POR threshold (≅0.6V), the PHY is in a power-down state. All digital IOs remains in high impedance states and analog blocks are disabled. PMA termination is not present when powered down.

7.4.2 Reset

Reset is activated upon power-up, when $\overline{\text{RESET}}$ is pulled LOW (for the minimum reset pulse time) or if hardware reset is initiated by setting bit[15] in register 0x1F. All digital circuitry is cleared along with register settings during reset. Once reset completes, device bootstraps are re-sampled and associated bootstrap registers are set accordingly. PMA termination is not present in reset.

7.4.3 Standby

The device (100BASE-T1 Leader mode only) automatically enters into standby post power-up and reset so long that all supplies are available and the device is bootstrapped for managed operation.

In standby, all PHY functions are operational except for PCS and PMA blocks. The PMA termination is also not present. Link establishment is not possible in standby and data cannot be transmitted or received. SMI functions are operational and register configurations are maintained.

If the device is configured for autonomous operation through bootstrap setting, the PHY automatically switches to normal operation once POR is complete.

7.4.4 Normal

Normal mode can be entered from either autonomous or managed operation. When in autonomous operation, the PHY automatically attempts to establish a link with a valid Link Partner once POR is complete.

In managed operation, SMI access is required to allow the device to exit standby (100BASE-T1 Leader mode only); commands issued through the SMI allow the device to exit standby and enables both the PCS and PMA blocks. All device features are operational in normal mode.

Autonomous operation can be enabled through SMI access by setting register 0x18B[6] = '1'. Note that this bit is auto-cleared after link up.

7.4.5 Media Dependent Interface

7.4.5.1 100BASE-T1 Leader and 100BASE-T1 Follower Configuration

100BASE-T1 Leader and 100BASE-T1 Follower are configured using either hardware bootstraps or through register access.

LED_0 controls the 100BASE-T1 Leader and 100BASE-T1 Follower bootstrap configuration. By default, 100BASE-T1 Follower mode is configured because there is an internal pulldown resistor on the LED_0 pin. If 100BASE-T1 Leader mode configuration through hardware bootstrap is preferred, an external pullup resistor is required.

Additionally, bit[14] in the **MMD1_PMA_CTRL_2 Register (Address 0x1834)** controls the 100BASE-T1 Leader and 100BASE-T1 Follower configuration. When this bit is set, 100BASE-T1 Leader mode is enabled.

7.4.5.2 Auto-Polarity Detection and Correction

During the link training process, the DP83TC814-Q1 100BASE-T1 Follower device is able to detect polarity reversal and automatically corrects the error. If polarity reversal is detected, the 100BASE-T1 Follower self-inverts transmitted signals to account for the error and verifies compatibility with the 100BASE-T1 Leader. Polarity at the 100BASE-T1 Leader is always observed as correct because polarity detection and correction is handled entirely by the 100BASE-T1 Follower.

Auto-polarity correction can be disabled in cases the correction is not required. Disabling of auto-polarity correction is achieved using register 0x0553.

7.4.5.3 Jabber Detection

The jabber function prevents the PCS Receive state machine from locking up into a DATA state if the End-of-Stream Delimiters, ESD1 and ESD2, are never detected or received within the rcv_max_timer. When the maximum receive DATA state timer expires, the PCS Receive state machine is reset and transitions into IDLE state. IEEE 802.3bw specifies that jabber timeout be set to 1.08ms ±54µs. By default, jabber timeout in the DP83TC814 is set to 1.1ms. This timer is configurable in *Register 0x496[10:0]*.

7.4.5.4 Interleave Detection

The interleave function allows for the DP83TC814-Q1 to detect and de-interleave the serial stream from a connected link partner. The two possible interleave sequences of ternary symbols include: (TA_n, TB_n) or (TB_n, TA_n).

7.4.6 MAC Interfaces

7.4.6.1 Media Independent Interface

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2015 clause 22. The PHY has internal series termination resistors on MII output pins including TX_CLK output when the PHY is operating in MII mode. In this mode, do not leave the MII-TX pins floating or High-Z.

The MII signals are summarized in Table 7-4:

Table 7-4. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_EN, TX_ER
	RX_DV, RX_ER
Clock Signals	TX_CLK
	RX_CLK

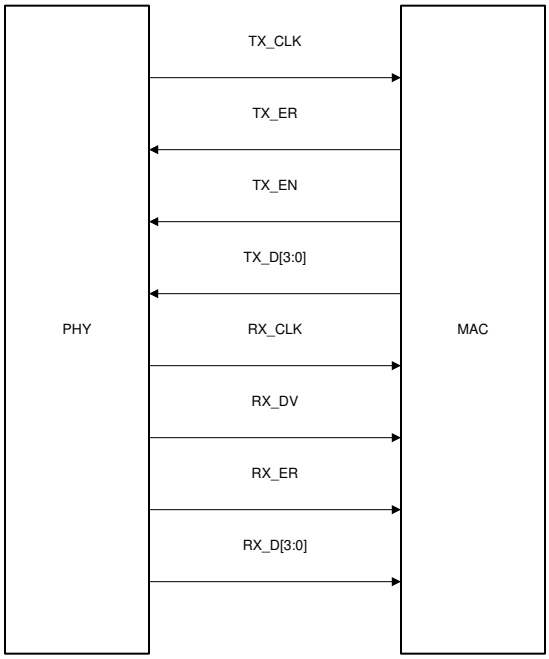


Figure 7-11. MII Signaling

Table 7-5. MII Transmit Encoding

TX_EN	TX_ER	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

Table 7-6. MII Receive Encoding

RX_DV	RX_ER	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000	Normal Inter-Frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

7.4.6.2 Reduced Media Independent Interface

The DP83TC814-Q1 incorporates the Reduced Media Independent Interface (RMII) as defined in the RMII Revision 1.2 and 1.0 from the RMII consortium. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3u MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII.

The DP83TC814-Q1 offers two types of RMII operations: RMII Follower and RMII Leader. In RMII Follower Mode, the DP83TC814-Q1 operates off a 50MHz CMOS-level oscillator, which is either provided by the MAC or synchronous to the MAC reference clock. In RMII Leader operation, the DP83TC814-Q1 operates off of either a 25MHz CMOS-level oscillator connected to XI pin or a 25MHz crystal connected across XI and XO pins. When bootstrapping to RMII Leader Mode, a 50MHz output clock automatically is enabled on RX_D3. This 50MHz output clock must be routed to the MAC.

The RMII specification has the following characteristics:

- Single clock reference shared between MAC and PHY
- Provides independent 2-bit wide transmit and receive data paths

In this mode, data transfers are two bits for every clock cycle using the 50MHz reference clock for both transmit and receive paths.

The RMII signals are summarized in Table 7-7:

Table 7-7. RMII Signals

FUNCTION	PINS
Data Signals	TX_D[1:0]
	RX_D[1:0]
Control Signals	TX_EN
	CRS_DV

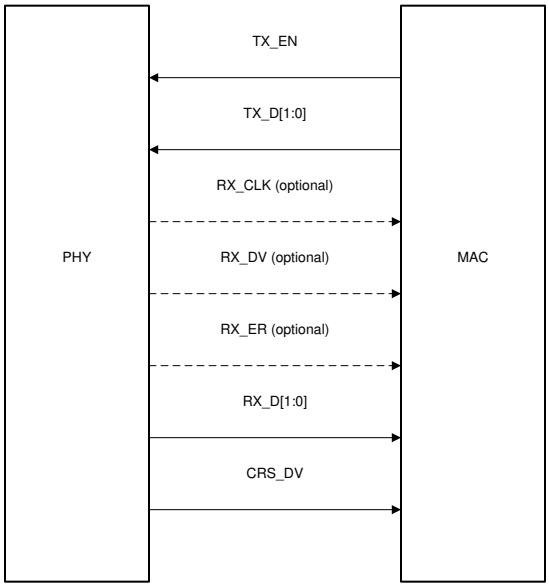


Figure 7-12. RMII Signaling

Table 7-8. RMII Transmit Encoding

TX_EN	TX_D[1:0]	DESCRIPTION
0	00 through 11	Normal Inter-Frame
1	00 through 11	Normal Data Transmission

Table 7-9. RMII Receive Encoding

CRS_DV	RX_ER	RX_D[1:0]	DESCRIPTION
0	0	00 through 11	Normal Inter-Frame
0	1	00	Normal Inter-Frame
0	1	01 through 11	Reserved
1	0	00 through 11	Normal Data Reception
1	1	00 through 11	Data Reception with Errors

RMII Follower: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the XI pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the XI pin.

RMII Leader: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the RX_D3 pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the RX_D3 pin.

The DP83TC814-Q1 RMII supplies an RX_DV signal, which provides a simpler method to recover receive data without the need to separate RX_DV from the CRS_DV indication. RX_ER is also supported even though RX_ER is not required by the RMII specification.

RMII includes a programmable FIFO to adjust for the frequency differences between the reference clock and the recovered clock. The programmable FIFO, located in the register 0x0011[9:8] and register 0x0648[9:7], minimizes internal propagation delay based on expected maximum packet size and clock accuracy.

Table 7-10. XI Clock PPM = ± 100ppm

Reg 0x0011 <9:8>	Reg 0x0648 <9:7>	INCREMENT PHY LATENCY	MAX PACKET LENGTH WITHOUT ERRORS
01	010	Default	2250
10	100	80ns	7250

7.4.6.3 Reduced Gigabit Media Independent Interface

The DP83TC814-Q1 also supports Reduced Gigabit Media Independent Interface (RGMII) as specified by RGMII version 2.0 with LVCMOS. RGMII is designed to reduce the number of pins required to connect MAC and PHY. To accomplish this goal, the control signals are multiplexed. Both rising and falling edges of the clock are used to sample the control signal pin on transmit and receive paths. Data is samples on just the rising edge of the clock. For 100Mbps operation, RX_CLK and TX_CLK operate at 25MHz.

The RGMII signals are summarized in Table 7-11:

Table 7-11. RGMII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_CTRL
	RX_CTRL
Clock Signals	TX_CLK
	RX_CLK

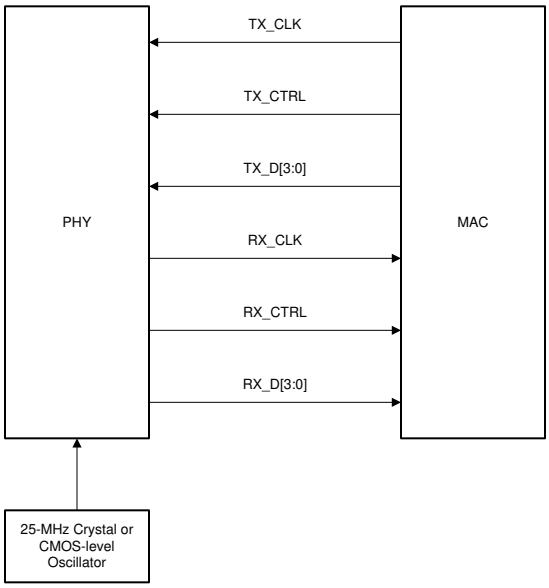


Figure 7-13. RGMII Connections

Table 7-12. RGMII Transmit Encoding

TX_CTRL (POSITIVE EDGE)	TX_CTRL (NEGATIVE EDGE)	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	1	0000 through 1111	Normal Data Transmission
1	0	0000 through 1111	Transmit Error Propagation

Table 7-13. RGMII Receive Encoding

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1101	Reserved
0	1	1110	False Carrier Indication

Table 7-13. RGMII Receive Encoding (continued)

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

During packet reception, RX_CLK can be stretched on either the positive or negative pulse to accommodate the transition from the internal free running clock to a recovered clock (data synchronous). Data can be duplicated on the falling edge of the clock because double data rate (DDR) is only required for 1Gbps operation, which is not supported by the DP83TC814-Q1.

The DP83TC814-Q1 supports in-band status indication to help simplify link status detection. Inter-frame signals on RX_D[3:0] pins as specified in Table 7-14.

Table 7-14. RGMII In-Band Status

RX_CTRL	RX_D3	RX_D[2:1]	RX_D0
00 **Note:** In-band status is only valid when RX_CTRL is low	**Duplex Status:** 0 = Half-Duplex 1 = Full-Duplex	**RX_CLK Clock Speed:** 00 = 2.5MHz 01 = 25MHz 10 = 125MHz 11 = Reserved	**Link Status:** 0 = Link not established 1 = Valid link established

7.4.6.4 Serial Gigabit Media Independent Interface

The Serial Gigabit Media Independent Interface (SGMII) provides a means for data transfer between MAC and PHY with significantly less signal pins (4 pins) compared to MII (14 pins), RMII (7 pins) or RGMII (12 pins). SGMII uses low-voltage differential signaling (LVDS) to reduce emissions and improve signal quality.

The DP83TC814 SGMII is capable of operating in 4-wire. SGMII is configurable through hardware bootstraps. In 4-wire operation, two differential pairs are used to transmit and receive data. Clock and data recovery are performed in the MAC and in the PHY.

Because the DP83TC814 operates at 100Mbps, the 1.25Gbps rate of the SGMII is excessive. The SGMII specification allows for 100Mbps operation by replicating each byte within a frame 10 times. Frame elongation takes place above the IEEE 802.3 PCS layer, which prevents the start-of-frame delimiter from appearing more than once.

Because the DP83TC814 only supports 100Mbps speed, SGMII Auto-Negotitation can be disabled by setting bit[0] = 0b0 in the *Register 0x608*.

The SGMII signals are summarized in Table 7-15.

Table 7-15. SGMII Signals

FUNCTION	PINS
Data Signals	TX_M, TX_P
	RX_M, RX_P

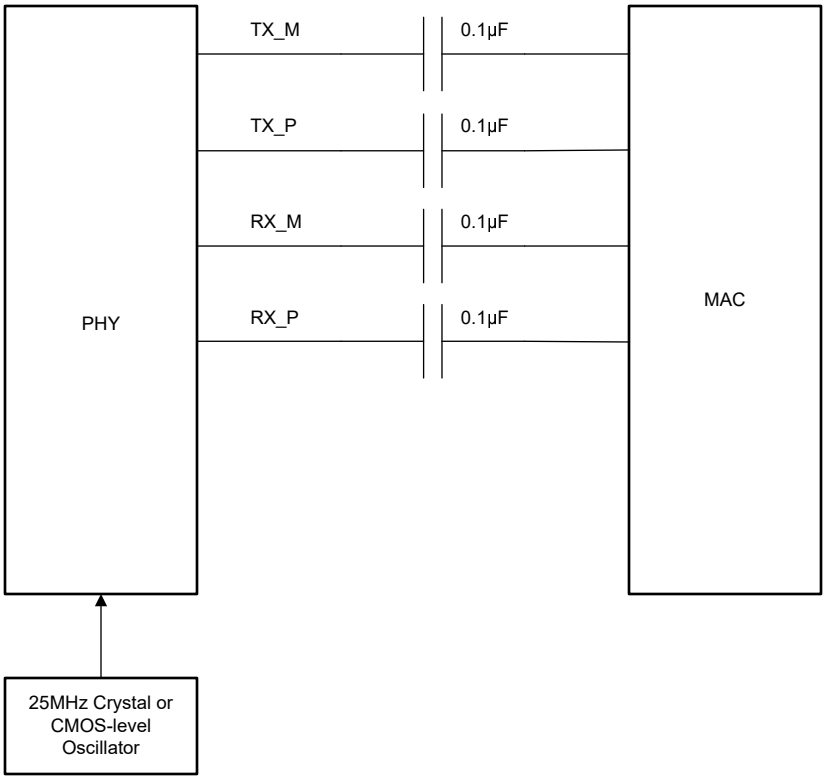


Figure 7-14. SGMII Connections

7.4.7 Serial Management Interface

The Serial Management Interface (SMI) provides access to the DP83TC814S-Q1 internal register space for status information and configuration. The SMI frames and base registers are compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TC814S-Q1 . Additionally, the DP83TC814S-Q1 includes control and status registers added to clause 45 as defined by IEEE 802.3bw. Access to clause 45 register field is achieved using clause 22 access.

The SMI includes the management clock (MDC) and the management input and output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 9 DP83TC814S-Q1 PHYs can share a common SMI bus. To distinguish between the PHYs, a 4-bit address is used. During power-up-reset, the DP83TC814S-Q1 latches the PHYAD[3:0] configuration pins to determine the address.

The management entity must not start an SMI transaction in the first cycle after power-up-reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device can actively drive the MDIO signal during the first bit of turnaround. The addressed

DP83TC814S-Q1 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TC814S-Q1 , thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 7-16. SMI Protocol Structure

SMI PROTOCOL	<idle> <start> <op code> <device address> <reg address> <turnaround> <data> <idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

7.4.7.1 Direct Register Access

Direct register access can be used for the first 31 registers (0x0 through 0x1F).

7.4.7.2 Extended Register Space Access

The DP83TC814S-Q1 's SMI function supports read or write access to the extended register set using registers REGCR (0x0D) and ADDAR (0x0E) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

Note

Registers with addresses above 0x001F require indirect access. For indirect access, a sequence of register writes must be followed. The MMD value defines the Device Address (DEVAD) of the register set. The DEVAD must be configured in the register 0x000D (REGCR) bits [4:0] for indirect access

The DP83TC814S-Q1 supports 3 MMD device addresses:
1. MMD1F (Vendor specific registers): DEVAD [4:0] = ‘11111’
2. MMD1 (IEEE 802.3az defined registers): DEVAD [4:0] = ‘00001’
3. MMD3 (IEEE 802.3az defined registers): DEVAD [4:0] = ‘00011’

Table 7-17. MMD Register Space Division

MMD Register Space	Register Address Setting
MMD1F	0x000 - 0x0EFD
MMD1	0x1000 - 0x1FFF
MMD3	0x3000 - 0x3001

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for MMD1F register accesses (DEVAD[4:0] = 11111).

7.4.7.3 Write Operation (No Post Increment)

To write a register in the extended register set:

Instruction	Example: Set reg 0x0170 = 0C50
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR (0x0D).	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR (0x0E).	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Write the content of the desired extended register set register to register ADDAR.	Write register 0x0E to value 0x0C50

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register is previously configured.

7.4.7.4 Read Operation (No Post Increment)

To read a register in the extended register set:

Instruction	Example: Read 0x0170
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Read the content of the desired extended register set register to register ADDAR.	Read register 0x0E

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register is previously configured.

7.4.7.5 Write Operation (Post Increment)

To write a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

Instruction	Example: Set reg 0x0170 = 0C50 & reg 0x0171 = 0x0011
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F
2. Write the register address from register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11. DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x801F
4. Write the content of the desired extended register set register to register ADDAR.	Write register 0x0E to value 0x0C50
5. Subsequent writes to register ADDAR (step 4) writes the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.	Write register 0x0E to value 0x0011

Step 4 Writes register 0x0170 to 0x0C50 and because post increment is enabled, Step 5 writes register 0x0171 to 0x0011.

7.4.7.6 Read Operation (Post Increment)

To read a register in the extended register set and automatically increment the address register to the next higher value following the read operation:

Instruction	Example: Read register 0x0170 & 0x0171
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F

Instruction	Example: Read register 0x0170 & 0x0171
2. Write the desired register address to register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x801F
4. Read the content of the desired extended register set register to register ADDAR.	Read register 0x0E
5. Subsequent reads to register ADDAR (step 4) reads the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.	Read register 0x0E

Step 4 Reads register 0x0170 and because post increment is enabled, Step 5 reads register 0x0171.

7.5 Programming

7.5.1 Strap Configuration

The DP83TC814S-Q1 uses functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up and hardware reset (through either the $\overline{\text{RESET}}$ pin or register access). Some strap pins support 3 levels and some strap pins support 2 levels, which are described in greater detail below. PHY address straps, RX_DV/RX_CTRL and RX_ER, are 3-level straps while all other straps are two levels. Configuration of the device can be done through strapping or through serial management interface.

Note

Because strap pins are functional pins after reset is deasserted, strap pins must not be connected directly to VDDIO or VDDMAC or GND. Either pullup resistors, pulldown resistors, or both are required for proper operation.

Note

When using VDDMAC and VDDIO separately, connect strap resistors to the correct voltage rail. The voltage domain of each pin is listed in the table below.

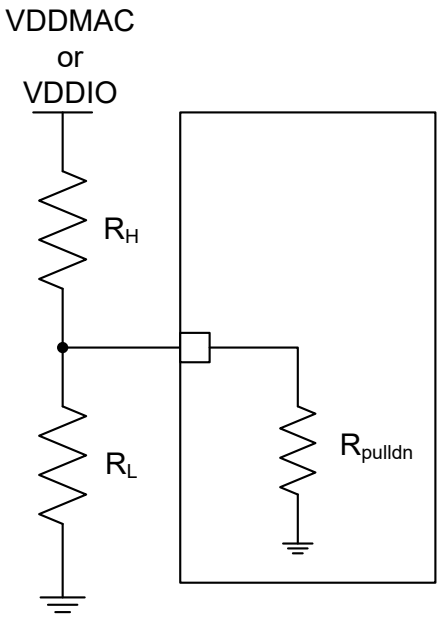


Figure 7-15. Strap Circuit

R_{pulldn} value is included in the Electrical Characteristics table of the data sheet.

Table 7-18. Recommended 3-Level Strap Resistor Ratios for PHY Address

MODE [3]	IDEAL RH (kΩ) (VDDIO = 3.3V) [1]	IDEAL RH (kΩ) (VDDIO = 2.5V) [2]	IDEAL RH (kΩ) (VDDIO = 1.8V) [1]
1	OPEN	OPEN	OPEN
2	13	12	4
3	4.5	2	0.8

1. Strap resistors with 10% tolerance.
2. Strap resistors with 1% tolerance.
3. RL is optional and can be added if voltage on bootstrap pins needs to be adjusted.

Table 7-19. Recommended 2-Level Strap Resistors

MODE	IDEAL RH (kΩ) (1), (2)
1	OPEN
2	2.49

(1) Strap resistors with up to 10% tolerance can be used.
(2) To gain more margin in customer application for 1.8V VDDIO, either 2.1kΩ +/-10% pull-up can be used or resistor accuracy of 2.49kΩ resistor can be limited to 1%.

The following table describes the PHY configuration bootstraps:

Table 7-20. Bootstraps

PIN NAME	PIN NO.	DOMAIN	DEFAULT MODE	STRAP FUNCTION			DESCRIPTION
RX_DV/ RX_CTRL	15	VDDMAC	1	**MODE**	**PHY_AD[0]**	**PHY_AD[2]**	PHY_AD: PHY Address ID
				1	0	0	
				2	0	1	
				3	1	1	
RX_ER	14	VDDMAC	1	**MODE**	**PHY_AD[1]**	**PHY_AD[3]**	PHY_AD: PHY Address ID
				1	0	0	
				2	0	1	
				3	1	1	
CLKOUT	16	VDDMAC	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable. This is a duplicate strap for LED_1. If CLKOUT pin is configured as LED_1 pin then the $\overline{\text{AUTO}}$strap functionality also moves to the CLKOUT pin.
				1	0		
				2	1		
RX_D0	26	VDDMAC	1	**MODE**	**MAC[0]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D1	25	VDDMAC	1	**MODE**	**MAC[1]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D2	24	VDDMAC	1	**MODE**	**MAC[2]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D3	23	VDDMAC	1	**MODE**	**CLKOUT_PIN**		CLKOUT_PIN: This strap determines which pin is used for output clock.
				1	0		
				2	1		
LED_0	35	VDDIO	1	**MODE**	**MS**		MS: 100BASE-T1 Leader & 100BASE-T1 Follower Selection
				1	0		
				2	1		
LED_1	6	VDDIO	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable This is the default strap pin for controlling $\overline{\text{AUTO}}$ feature. If this pin is configured as CLKOUT, the $\overline{\text{AUTO}}$ feature moves to pin 16.
				1	0		
				2	1		

Note

Refer to SNLA389 Application Note for more information about the register settings used for compliance testing. Use these register settings to achieve the same performance as observed during compliance testing. Managed mode strap option is recommended to prevent the link up process from initiating while the software configuration from SNLA389 is being executed. Once the software configuration is completed, the PHY can be removed from Managed mode by setting bit 0x018B[6] to '1'. This bit is auto-cleared after link up

RX_D3 strap pin has a special functionality of controlling the output status of CLKOUT (pin 16) and LED_1 (pin 6). The Table 7-21 table below shows how pin 16 and pin 6 is affected by RX_D3 strap status. Note that RX_D3 option only changes the pin functionality but not the voltage domains. Pin 16 is always in VDDMAC domain and Pin 6 is always in VDDIO domain. If VDDIO and VDDMAC are at separate voltage levels, VDDIO and VDDMAC must be verified that pin 16 and pin 6 are strapped to the respective voltage domains.

In clock output daisy chain applications, if VDDMAC and VDDIO are at different voltages then clock output must be routed to pin 6. Internal oscillator of the DP83TC814 operates in the VDDIO domain, so clock output must also be used on the pin in VDDIO domain, such as pin 6. In clock output daisy chain applications where VDDMAC and VDDIO are same, this requirement can be ignored. This requirement can also be ignored in applications where clock output is not being used.

Table 7-21. Clock Output Pin Selection

CLKOUT_PIN	DESCRIPTION
0	Pin 16 is Clock output, Pin 6 is LED_1 pin. $\overline{\text{AUTO}}$ is controlled by straps on pin 6.
1	Pin 6 is Clock output, Pin 16 is LED_1 pin. $\overline{\text{AUTO}}$ is controlled by straps on pin 16.

Table 7-22. 100BASE-T1 Leader and 100BASE-T1 Follower Selection Bootstrap

MS	DESCRIPTION
0	100BASE-T1 Follower Configuration
1	100BASE-T1 Leader Configuration

Table 7-23. Autonomous Mode Bootstrap

$\overline{\text{AUTO}}$	DESCRIPTION
0	Autonomous Mode, PHY able to establish link after power-up
1	Managed Mode, PHY must be allowed to establish link after power-up based on register write

Table 7-24. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire) (1)
0	0	1	MII
0	1	0	RMII Follower
0	1	1	RMII Leader
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Internal Delay Mode)
1	1	0	RGMII (TX and RX Internal Delay Mode)
1	1	1	RGMII (RX Internal Delay Mode)

(1) SGMII strap mode is only available on 'S' type device variant. For 'R' type device variant, this strap mode is RESERVED

Table 7-25. PHY Address Bootstraps

PHY_AD[3:0]	RX_CTRL STRAP MODE	RX_ER STRAP MODE	DESCRIPTION Section 7.5.1
0000	1	1	PHY Address: 0b00000 (0x0)

Table 7-25. PHY Address Bootstraps (continued)

PHY_AD[3:0]	RX_CTRL STRAP MODE	RX_ER STRAP MODE	DESCRIPTION Section 7.5.1
0001	-	-	NA
0010	-	-	NA
0011	-	-	NA
0100	2	1	PHY Address: 0b00100 (0x4)
0101	3	1	PHY Address: 0b00101 (0x5)
0110	-	-	NA
0111	-	-	NA
1000	1	2	PHY Address: 0b01000 (0x8)
1001	-	-	NA
1010	1	3	PHY Address: 0b01010 (0xA)
1011	-	-	NA
1100	2	2	PHY Address: 0b01100 (0xC)
1101	3	2	PHY Address: 0b01101 (0xD)
1110	2	3	PHY Address: 0b01110 (0xE)
1111	3	3	PHY Address: 0b01111 (0xF)

7.5.2 LED Configuration

The DP83TC814S-Q1 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2 (CLKOUT). Several functions can be multiplexed onto the LEDs for different modes of operation. LED operations are selected using register 0x0450. By default, Pin 14 of the DP83TC813 will output the CLKOUT signal. To instead have the LED1 signal on Pin 14, write the following registers:

Write register 0x045F = 0x000F

Write register 0x0452 = 0x0000

Write register 0x0451 = 0x0009

Because the LED output pins are also used as strap pins, external components required for strapping and the user must consider the LED usage to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding input upon power up or hardware reset.

Figure 7-16 shows the two proper ways of connecting LEDs directly to the DP83TC814S-Q1

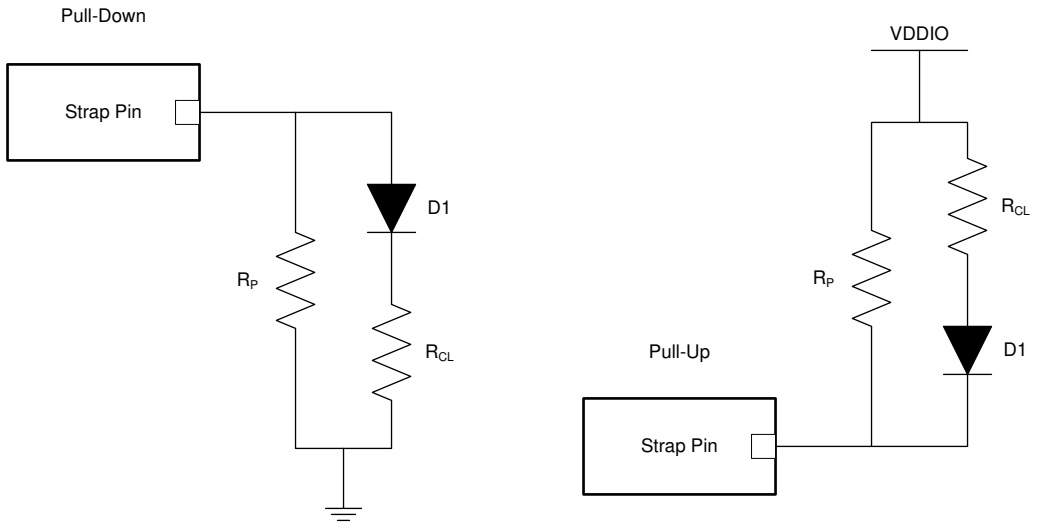


Figure 7-16. Example Strap Connections

7.5.3 PHY Address Configuration

The DP83TC814S-Q1 can be set to respond to any of 9 possible PHY addresses through bootstrap pins. The PHY address is latched into the device upon power-up or hardware reset. Each PHY on the serial management bus in the system must have a unique PHY address.

By default, DP83TC814S-Q1 latches to a PHY address of 0 (<0b00000>). This address can be changed by adding pullup resistors to bootstrap pins found in Section 7.5.3.

8 Register Maps

8.1 Register Access Summary

There are two different methods for accessing registers within the field. Direct register access method is only allowed for the first 31 registers (0x0 through 0x1F). Registers beyond 0x1F must be accessed by use of the Indirect Method (Extended Register Space) described in *Section 7.4.7.2*.

Table 8-1. MMD Register Space Division

MMD REGISTER SPACE	REGISTER ADDRESS RANGE
MMD1F	0x0000 - 0x0EFD
MMD1	0x1000 - 0x1FFF
MMD3	0x3000 - 0x3001

Note

For MMD1 and MMD3, the most significant nibble of the register address is used to denote the respective MMD space. This nibble must be ignored during actual register access operation. For example, to access register 0x1836, use 0x1 as the MMD indicator and 0x0836 as the register address.

Table 8-2. Register Access Summary

REGISTER FIELD	REGISTER ACCESS METHODS
0x0 through 0x1F	Direct Access
	Indirect Access, MMD1F = '11111' **Example:** to read register 0x17 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x17 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1F Field 0x20 - 0xFFF	Indirect Access, MMD1F = '11111' **Example:** to read register 0x462 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x462 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1 Field 0x0 - 0xFFF	Indirect Access, MMD1 = '00001' **Example:** to read register 0x7 in MMD1 field (register 0x1007) with no post increment Step 1) write 0x1 to register 0xD Step 2) write 0x7 to register 0xE Step 3) write 0x4001 to register 0xD Step 4) read register 0xE

8.2 DP83TC814 Registers

Table 8-3 lists the memory-mapped registers for the DP83TC814 registers. All register offset addresses not listed in Table 8-3 should be considered as reserved locations and the register contents should not be modified.

Table 8-3. DP83TC814 Registers

Offset	Acronym	Register Name	Section
0h	BMCR	IEEE Control Register	Section 8.2.1
1h	BMSR	IEEE Status Register	Section 8.2.2
2h	PHYIDR1	PHY Identification Register - 1	Section 8.2.3
3h	PHYIDR2	PHY Identification Register - 2	Section 8.2.4
10h	PHYSTS	PHY Status Register	Section 8.2.5
11h	PHYSCR	Software Control Register	Section 8.2.6
12h	MISR1	Interrupt Register -1	Section 8.2.7
13h	MISR2	Interrupt Register -2	Section 8.2.8
15h	RECR	RX Error Count Register	Section 8.2.9
16h	BISCR	BIST Control Register	Section 8.2.10
18h	MISR3	Interrupt Register -3	Section 8.2.11
19h	REG_19	PHY Address Status Register	Section 8.2.12
1Eh	CDCR	TDR Run Status Register	Section 8.2.13
1Fh	PHYRCR	Reset Control Register	Section 8.2.14
133h	Register_133	CnS Status Register	Section 8.2.15
18Bh	LPS_CFG2	Low Power Configuration Register - 2	Section 8.2.16
18Ch	LPS_CFG3	Low Power Configuration Register - 3	Section 8.2.17
18Eh	LPS_STATUS	Low Power Status Register	Section 8.2.18
300h	TDR_TX_CFG	TDR TX Configuration Register	Section 8.2.19
301h	TAP_PROCESS_CFG	Tap Process Configuration Register	Section 8.2.20
302h	TDR_CFG1	TDR Configuration Register - 1	Section 8.2.21
303h	TDR_CFG2	TDR Configuration Register - 2	Section 8.2.22
304h	TDR_CFG3	TDR Configuration Register - 3	Section 8.2.23
305h	TDR_CFG4	TDR Configuration Register - 4	Section 8.2.24
306h	TDR_CFG5	TDR Configuration Register - 5	Section 8.2.25
310h	TDR_TC1	TDR Status Register	Section 8.2.26
430h	A2D_REG_48	RGMII ID Control Register	Section 8.2.27
442h	A2D_REG_66	ESD Event Count Register - 1	Section 8.2.28
450h	LEDS_CFG_1	LED Configuration Register - 1	Section 8.2.29
451h	LEDS_CFG_2	LED Configuration Register - 2	Section 8.2.30
452h	IO_MUX_CFG_1	IO Multiplexing Register - 1	Section 8.2.31
453h	IO_MUX_CFG_2	IO Multiplexing Register - 2	Section 8.2.32
456h	IO_MUX_CFG	xMII Impedance Control Register	Section 8.2.33
45Dh	CHIP_SOR_1	Strap Status Register	Section 8.2.34
45Fh	LED1_CLKOUT_ANA_CTRL	CLKOUT and LED_1 Control Register	Section 8.2.35
489h	TX_INTER_CFG	Interleave Configuration Register	Section 8.2.36
496h	JABBER_CFG	Jabber Configuration Register	Section 8.2.37
553h	PG_REG_4	Auto-Polarity Correction Control Register	Section 8.2.38
560h	TC1_CFG_RW	TC1 Configuration Register	Section 8.2.39
561h	TC1_LINK_FAIL_LOSS	TC1 Link Fail Count Register	Section 8.2.40
562h	TC1_LINK_TRAINING_TIME	TC1 Link Training Time Register	Section 8.2.41

Table 8-3. DP83TC814 Registers (continued)

Offset	Acronym	Register Name	Section
563h	NO_LINK_TH		Section 8.2.42
600h	RGMII_CTRL	RGMII Control Register	Section 8.2.43
601h	RGMII_FIFO_STATUS	RGMII FIFO Status Register	Section 8.2.44
602h	RGMII_CLK_SHIFT_CTRL	RGMII Shift Control Register	Section 8.2.45
608h	SGMII_CTRL_1	SGMII Control Register - 1	Section 8.2.46
60Ah	SGMII_STATUS	SGMII Status Register	Section 8.2.47
60Ch	SGMII_CTRL_2	SGMII Control Register - 2	Section 8.2.48
60Dh	SGMII_FIFO_STATUS	SGMII FIFO Status Register	Section 8.2.49
618h	PRBS_STATUS_1	PRBS Status Register - 1	Section 8.2.50
619h	PRBS_CTRL_1	PRBS Control Register - 1	Section 8.2.51
61Ah	PRBS_CTRL_2	PRBS Control Register - 2	Section 8.2.52
61Bh	PRBS_CTRL_3	PRBS Control Register - 3	Section 8.2.53
61Ch	PRBS_STATUS_2	PRBS Status Register - 2	Section 8.2.54
61Dh	PRBS_STATUS_3	PRBS Status Register - 3	Section 8.2.55
61Eh	PRBS_STATUS_4	PRBS Status Register - 4	Section 8.2.56
620h	PRBS_STATUS_5	PRBS Status Register - 5	Section 8.2.57
622h	PRBS_STATUS_6	PRBS Status Register - 6	Section 8.2.58
623h	PRBS_STATUS_7	PRBS Status Register - 7	Section 8.2.59
624h	PRBS_CTRL_4	PRBS Control Register - 4	Section 8.2.60
625h	PATTERN_CTRL_1	BIST Pattern Control Register - 1	Section 8.2.61
626h	PATTERN_CTRL_2	BIST Pattern Control Register - 2	Section 8.2.62
627h	PATTERN_CTRL_3	BIST Pattern Control Register - 3	Section 8.2.63
628h	PMATCH_CTRL_1	BIST Match Control Register - 1	Section 8.2.64
629h	PMATCH_CTRL_2	BIST Match Control Register - 2	Section 8.2.65
62Ah	PMATCH_CTRL_3	BIST Match Control Register - 3	Section 8.2.66
639h	TX_PKT_CNT_1	xMII TX Packet Count Register - 1	Section 8.2.67
63Ah	TX_PKT_CNT_2	xMII TX Packet Count Register - 2	Section 8.2.68
63Bh	TX_PKT_CNT_3	xMII TX Packet Count Register - 3	Section 8.2.69
63Ch	RX_PKT_CNT_1	xMII RX Packet Count Register - 2	Section 8.2.70
63Dh	RX_PKT_CNT_2	xMII RX Packet Count Register - 2	Section 8.2.71
63Eh	RX_PKT_CNT_3	xMII RX Packet Count Register - 3	Section 8.2.72
648h	RMII_CTRL_1	RMII Control Register	Section 8.2.73
649h	RMII_STATUS_1	RMII FIFO Status Register	Section 8.2.74
871h	dsp_reg_71	SQI Register	Section 8.2.75
1000h	MMD1_PMA_CTRL_1		Section 8.2.76
1001h	MMD1_PMA_STATUS_1		Section 8.2.77
1007h	MMD1_PMA_STATUS_2		Section 8.2.78
100Bh	MMD1_PMA_EXT_ABILITY_1		Section 8.2.79
1012h	MMD1_PMA_EXT_ABILITY_2		Section 8.2.80
1834h	MMD1_PMA_CTRL_2		Section 8.2.81
1836h	MMD1_PMA_TEST_MODE_CTRL		Section 8.2.82
3000h	MMD3_PCS_CTRL_1		Section 8.2.83
3001h	MMD3_PCS_Status_1		Section 8.2.84

Complex bit access types are encoded to fit into small table cells. Table 8-4 shows the codes that are used for access types in this section.

Table 8-4. DP83TC814 Access Type Codes

Access Type	Code	Description
Read Type		
H	H	Set or cleared by hardware
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0S	W 0S	Write 0 to set
W1S	W 1S	Write 1 to set
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 BMCR Register (Offset = 0h) [Reset = 2100h]

BMCR is shown in Table 8-5.

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Table 8-5. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MII Reset	RH/W1S	0h	1b = Digital in reset and all MII regs (0x0 - 0xF) reset to default 0b = No reset This bit is auto-cleared
14	xMII Loopback	R/W	0h	1b = Enable MII loopback 0b = Disable MII loopback When xMII loopback mode is activated, the transmitted data presented on xMII TXD is looped back to xMII RXD internally. There is no LINK indication generated when xMII loopback is enabled.
13	Speed Select	R	1h	Speed Selection: Always 100-Mbps Speed
12	Auto-Negotiation Enable	R	0h	Auto-Negotiation: Not supported on this device
11	IEEE Power Down Enable	R/W	0h	This bit can be programmed to enter and exit IEEE power down mode This bit provide status when using INT_N as power down pin 0h = Normal mode 1h = Power down mode
10	Isolate	R/W	0h	Isolates the port from the xMII with the exception of the serial management interface 0h = Normal Mode 1h = Enable Isolate Mode
9	RESERVED	R	0h	Reserved
8	Duplex Mode	R	1h	0h = Half duplex 1h = Full duplex
7	RESERVED	R	0h	Reserved
6-0	RESERVED	R	0h	Reserved

8.2.2 BMSR Register (Offset = 1h) [Reset = 0061h]

BMSR is shown in Table 8-6.

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Table 8-6. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4	R	0h	0b = PHY doesn't support 100BASE-T4
14	100Base-X Full Duplex	R	0h	0h = PHY not able to perform full duplex 100Base-X 1h = PHY able to perform full duplex 100Base-X
13	100Base-X Half Duplex	R	0h	0h = PHY not able to perform half duplex 100Base-X 1h = PHY able to perform half duplex 100Base-X
12	10 Mbps Full Duplex	R	0h	0h = PHY not able to operate at 10Mbps in full duplex 1h = PHY able to operate at 10Mbps in full duplex
11	10 Mbps Half Duplex	R	0h	0h = PHY not able to operate at 10Mbps in half duplex 1h = PHY able to operate at 10Mbps in half duplex
10-7	RESERVED	R	0h	Reserved
6	MF Preamble Suppression	R	1h	0h = PHY does not accept management frames with preamble suppressed 1h = PHY accepts management frames with preamble suppressed
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	Auto-Negotiation Ability	R	0h	0h = PHY is not able to perform Auto-Negotiation 1h = PHY is able to perform Auto-Negotiation
2	Link status	R	0h	0h = Link is down 1h = Link is up
1	Jabber detect	H	0h	0h = No jabber condition detected 1h = Jabber condition detected
0	Extended Capability	R	1h	0h = Basic register set capabilities only 1h = Extended register capabilities

8.2.3 PHYIDR1 Register (Offset = 2h) [Reset = 2000h]

PHYIDR1 is shown in Table 8-7.

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Table 8-7. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally Unique Identifier 1	R	2000h	Unique Identifier for the part

8.2.4 PHYIDR2 Register (Offset = 3h) [Reset = A271h]

PHYIDR2 is shown in Table 8-8.

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Table 8-8. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Unique Identifier 2	R	28h	Unique Identifier for the part
9-4	Model Number	R	27h	Unique Identifier for the part
3-0	Revision Number	R	1h	Unique Identifier for the part

8.2.5 PHYSTS Register (Offset = 10h) [Reset = 0004h]

PHYSTS is shown in Table 8-9.

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Table 8-9. PHYSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	Descrambler Lock Status (Latch Low)	R/W0S	0h	0h = Descrambler is unlocked at least once 1h = Descrambler is locked
8	RESERVED	R	0h	Reserved
7	Interrupt Pin Status	H	0h	Interrupts pin status, cleared on reading 0x12 0h = Interrupt pin set 1h = Interrupt pin not set
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	MII Loopback Status	R	0h	0h = No MII loopback 1h = MII loopback
2	Duplex Mode Status	R	1h	0h = Half duplex 1h = Full duplex
1	RESERVED	R	0h	Reserved
0	Link Status (Latch Low) Non-Clear on Read	R	0h	Non-Clear on Read Latch Low link status Status is cleared on reading reg0x1 0h = Link is down atleast once 1h = Link is up

8.2.6 PHYSCR Register (Offset = 11h) [Reset = 010Bh]

PHYSCR is shown in Table 8-10.

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Table 8-10. PHYSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11	SGMII Soft Reset	R/WSC	0h	SGMII Digital Reset This bit is auto-cleared
10	MAC Isolate for PHY_ADDR 0x00	R/W	0h	MAC Isolate is enabled only if PHY address is 0x00 Reg0x0[10] works for all PHY addresses including 0x00 0h = Normal mode 1h = Isolate mode (No output from PHY to MAC)
9-8	RMII TX FIFO Depth	R/W	1h	0h = 4 nibbles 1h = 5 nibbles 2h = 6 nibbles
7	RESERVED	R	0h	Reserved
6-4	RESERVED	R	0h	Reserved
3	Interrupt Polarity	R/W	1h	0h = Active high 1h = Active low
2	Force Interrupt	R/W	0h	1h = Force interrupt pin
1	Interrupts Enable	R/W	1h	0h = Disable interrupts 1h = Enable interrupts
0	Interrupt Pin Configuration	R/W	1h	0h = Configure INT_N pin as power down input pin 1h = Configure INT_N pin is as interrupt output pin

8.2.7 MISR1 Register (Offset = 12h) [Reset = 0000h]

MISR1 is shown in Table 8-11.

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Table 8-11. MISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Energy Detect Change Status	H	0h	Status is changed to 1 when there is a change of MDI Energy detection output Status is cleared on read of this register
13	Link Status Change Status	H	0h	Status is changed to 1 when there is a change of link status Status is cleared on read of this register
12	Wake on LAN Status	H	0h	Status is changed to 1 when WOL is received Status is cleared on read of this register
11	ESD Fault Detected Status	H	0h	Status is changed to 1 when ESD fault is detected Status is cleared on read of this register
10	Training Done Status	H	0h	Status is changed to 1 when training is done Status is cleared on read of this register
9	RESERVED	R	0h	Reserved
8	RX Error Counter Half Full Status	H	0h	Status is changed to 1 when RX Error Counter in 0x15 is half full Status is cleared on read of this register
7	RESERVED	R	0h	Reserved
6	Energy Detect Change Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
5	Link Status Change Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
4	Wake on LAN Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
3	ESD Fault Detected Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
2	Link Training Completed Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
1	RESERVED	R	0h	Reserved
0	RX Error Counter Half Full Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set

8.2.8 MISR2 Register (Offset = 13h) [Reset = 0000h]

MISR2 is shown in Table 8-12.

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Table 8-12. MISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Under Voltage Status	H	0h	Status is changed to 1 when Under Voltage is detected Status is cleared on read of this register
14	Over Voltage Status	H	0h	Status is changed to 1 when Over Voltage is detected Status is cleared on read of this register
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	Sleep Mode Status	H	0h	Status is changed to 1 when sleep mode has changed Status is cleared on read of this register
9	Data Polarity Change Status	H	0h	Status is changed to 1 when MDI lines polarity change is detected Status is cleared on read of this register
8	Jabber Detect Status	H	0h	Status is changed to 1 when jabber is detected Status is cleared on read of this register
7	Under Voltage Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
6	Over Voltage Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	Data Polarity Change Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
0	Jabber Detect Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set

8.2.9 RECR Register (Offset = 15h) [Reset = 0000h]

RECR is shown in Table 8-13.

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Table 8-13. RECR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Error Count	RC	0h	RX_ER Counter: When a valid carrier is presented (only while RX_DV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in xMII loopback mode. The counter stops when at the maximum count (0xFFFF). When the counter exceeds half-full (0x7FFF), an interrupt is generated. This register is cleared on read.

8.2.10 BISCR Register (Offset = 16h) [Reset = 0100h]

BISCR is shown in Table 8-14.

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Table 8-14. BISCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	PRBS Lock Lost Latch Status	H	0h	0h = PRBS lock never lost 1h = PRBS lock lost at least once
9	RESERVED	R	0h	Reserved
8	Core Power Mode	R	1h	0h = Core is in power down or sleep mode 1h = Core is in normal power mode
7	RESERVED	R	0h	Reserved
6	Data Transmission to MDI in xMII Loopback	R/W	0h	0h = Transmit data on MDI during xMII loopback
5-2	Loopback Mode	R/W	0h	Enable Loopbacks other than PCS loopback. 0x16[1] must be 0 1h = Digital Loopback 2h = Analog Loopback 4h = Reverse Loopback 8h = External Loopback
1	PCS Loopback Enable	R/W	0h	0h = Disable PCS Loopback 1h = Enable PCS Loopback
0	RESERVED	R	0h	Reserved

8.2.11 MISR3 Register (Offset = 18h) [Reset = 00X5h]

MISR3 is shown in Table 8-15.

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Table 8-15. MISR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	No Link Status	H	0h	Status is changed to 1 when Link has not been observed within time programmed in 0x563 after training starts Status is cleared on read of this register
13	RESERVED	R	0h	Reserved
12	Power-On Reset Done Status	H	0h	Status is changed to 1 Power-On Reset is done after the the supplies are up Status is cleared on read of this register
11	No Frame Status	H	0h	Status is changed to 1 when No frame is detected until Status is cleared on read of this register
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	No Link Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
5	RESERVED	R	0h	Reserved
4	Power-On Reset Done Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
3	No Frame Indication	R/W	0h	0h = Indication is disabled 1h = Enable indication on INT_N pin if corresponding Interrupt Status is set
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2.12 REG_19 Register (Offset = 19h) [Reset = 0800h]

REG_19 is shown in Table 8-16.

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Table 8-16. REG_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-5	RESERVED	R	0h	Reserved
4-0	PHY Address	R	0h	PHY Address latched from straps

8.2.13 CDCR Register (Offset = 1Eh) [Reset = 0000h]

CDCR is shown in Table 8-17.

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Table 8-17. CDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TDR Start	RH/W1S	0h	Bit is cleared after TDR run is complete 1h = Start TDR
14	TDR Auto-Run Enable	R/W	0h	0h = Start TDR manually using 0x1E[15] 1h = Start TDR automatically on link down
13-2	RESERVED	R	0h	Reserved
1	TDR Done Status	R	0h	0h = TDR on-going or not initiated 1h = TDR done
0	TDR Fail Status	R	0h	When TDR Done Status is 1, this bit indicates if TDR ran successfully 0h = TDR ran successfully 1h = TDR run failed

8.2.14 PHYRCR Register (Offset = 1Fh) [Reset = 0000h]

PHYRCR is shown in Table 8-18.

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Table 8-18. PHYRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Hard Reset	RH/W1S	0h	Hardware Reset(Reset digital + register file) This bet is self clearing 0h = Normal Operation 1h = Resets PHY and clears registers. Does not resample the straps.
14	Soft Reset	RH/W1S	0h	0h = Normal Operation 1h = Restart PHY. Resets PHY but does not clear registers. Does not resample the straps. This bit is self cleared.
13	RESERVED	R	0h	Reserved
12-8	RESERVED	R	0h	Reserved
7	Standby Mode	R/W	0h	0h = Normal operation 1h = Standby mode enabled
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4-0	RESERVED	R	0h	Reserved

8.2.15 Register_133 (Offset = 133h) [Reset = 0000h]

Register_133 is shown in Table 8-19.

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Table 8-19. Register_133 Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Link Up Status	R	0h	Link Up status as defined by CnS
13	PHY Control In Send Data Mode	R	0h	PHY Control In Send Data Status
12	Link Status	R	0h	Link status set by link monitor
11-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	Descrambler Lock Status	R	0h	0h = Scrambler Not Locked 1h = Scrambler Locked
1	Local Receiver Status	R	0h	0h = Local PHY received link invalid 1h = Local PHY received link valid
0	Remote Receiver Status	R	0h	0h = Remote PHY received link invalid 1h = Remote PHY received link valid

8.2.16 LPS_CFG2 Register (Offset = 18Bh) [Reset = 1C4Bh]

LPS_CFG2 is shown in Table 8-20.

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Table 8-20. LPS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	Stop Sleep Negotiation on Link Down	R/W	1h	1b = Stop Sleep Negotiation if link goes down during negotiation
11	Stop Sleep Negotiation on Activity	R/W	1h	1b = Stop Sleep Negotiation when activity from MAC is observed in SLEEP_ACK state
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Ignore on read
6	Autonomous Mode	R/W	1h	1b = PHY entered normal mode on power up 0b = PHY entered standby mode on power up Default value is decided by LED_1 strap This bit is cleared post link up.
5	Transition To Standby	R/W	0h	1b = Enable normal to standby transition on over temperature/over voltage/under voltage 0b = Disable normal to standby transition on over temperature/over voltage/under voltage
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	LPS Sleep Enable	R/W	1h	Enable transition to Standby mode instead of Sleep mode after successful sleep negotiation (refered to as TC10_SBY) 0h = Enter standby after negotiated LPS 1h = Enter sleep after negotiated LPS
0	RESERVED	R	0h	Reserved

8.2.17 LPS_CFG3 Register (Offset = 18Ch) [Reset = 0000h]

LPS_CFG3 is shown in Table 8-21.

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Table 8-21. LPS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8-0	Power State Entry	RH/W1S	0h	1h = Normal command 10h = Standby command

8.2.18 LPS_STATUS Register (Offset = 18Eh) [Reset = 0000h]

LPS_STATUS is shown in Table 8-22.

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Table 8-22. LPS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6-0	Power State Status	R	0h	1h = Sleep 2h = Standby 4h = Normal

8.2.19 TDR_TX_CFG Register (Offset = 300h) [Reset = 2710h]

TDR_TX_CFG is shown in Table 8-23.

Return to the Summary Table.

Table 8-23. TDR_TX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TDR Transmit Duration	R/W	2710h	TDR transmit duration in µs Default : 10000µs

8.2.20 TAP_PROCESS_CFG Register (Offset = 301h) [Reset = 1703h]

TAP_PROCESS_CFG is shown in Table 8-24.

Return to the Summary Table.

Table 8-24. TAP_PROCESS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	End Tap Index	R/W	17h	End echo coefficient index for peak detect sweep during TDR
7-5	RESERVED	R	0h	Reserved
4-0	Start Tap Index	R/W	3h	Starting echo coefficient index for peak detect sweep during TDR

8.2.21 TDR_CFG1 Register (Offset = 302h) [Reset = 0045h]

TDR_CFG1 is shown in Table 8-25.

Return to the Summary Table.

Table 8-25. TDR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-4	Neighboring Taps Number	R/W	4h	Number of neighboring echo coefficient taps to be considered for calculating local maximum
3-2	Post-Silence State Timer	R/W	1h	0h = 0ms 1h = 10ms 2h = 100ms 3h = 1000ms
1-0	Pre-Silence State Timer	R/W	1h	0h = 0ms 1h = 10ms 2h = 100ms 3h = 1000ms

8.2.22 TDR_CFG2 Register (Offset = 303h) [Reset = 0419h]

TDR_CFG2 is shown in Table 8-26.

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Table 8-26. TDR_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	Tap Index Offset	R/W	4h	Tap index offset of dyamic peak equation, Start Tap Index + 1'b1
7-0	cfg_tdr_filt_init	R/W	19h	Value of peak_th at x=start_tap_index of dynamic peak threshold equation

8.2.23 TDR_CFG3 Register (Offset = 304h) [Reset = 0030h]

TDR_CFG3 is shown in Table 8-27.

Return to the Summary Table.

Table 8-27. TDR_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	cfg_tdr_filt_slope	R/W	30h	Slope of dynamic peak threshold equation (0.4)

8.2.24 TDR_CFG4 Register (Offset = 305h) [Reset = 0004h]

TDR_CFG4 is shown in Table 8-28.

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Table 8-28. TDR_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8-7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-4	hpf_gain_tdr	R/W	0h	HPF gain code during TDR
3-0	pga_gain_tdr	R/W	4h	PGA gain code during TDR

8.2.25 TDR_CFG5 Register (Offset = 306h) [Reset = 000Ah]

TDR_CFG5 is shown in Table 8-29.

Return to the Summary Table.

Table 8-29. TDR_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-0	cfg_cable_delay_num	R/W	Ah	Configure the propagation delay per meter of the cable in nanoseconds. This is used for the fault location estimation Valid values : 4 'd0 to 4 'd11 - [4.5:0.1:5.6]ns Default : 4 'd10 (5.5 ns)

8.2.26 TDR_TC1 Register (Offset = 310h) [Reset = 0000h]

TDR_TC1 is shown in Table 8-30.

Return to the Summary Table.

Table 8-30. TDR_TC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	Fault Detect Status	R	0h	0h = No Fault detected in cable 1h = Fault detected in cable
6	Fault Type	R	0h	0h = Short to GND, supply, or between MDI pins 1h = Open. Applicable to both 1-wire and 2-wire open faults
5-0	TDR Fault Location	R	0h	Fault location in meters (Valid only if Fault Detect Status = 1)

8.2.27 A2D_REG_48 Register (Offset = 430h) [Reset = 0770h]

A2D_REG_48 is shown in Table 8-31.

Return to the Summary Table.

Table 8-31. A2D_REG_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-8	RGMII TX Shift Delay	R/W	7h	Controls Internal Delay in RGMII mode in Steps of 312.5ps Delay = ((Bit[11:8] in decimal) + 1) × 312.5 ps
7-4	RGMII RX Shift Delay	R/W	7h	Controls Internal Delay in RGMII mode in Steps of 312.5ps Delay = ((Bit[7:4] in decimal) + 1) × 312.5 ps
3-0	RESERVED	R	0h	Reserved

8.2.28 A2D_REG_66 Register (Offset = 442h) [Reset = 0000h]

A2D_REG_66 is shown in Table 8-32.

Return to the Summary Table.

Table 8-32. A2D_REG_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-9	ESD Event Count	R	0h	Field gives the number of ESD events on the copper channel
8	RESERVED	R	0h	Reserved
7-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

8.2.29 LEDS_CFG_1 Register (Offset = 450h) [Reset = 2610h]

LEDS_CFG_1 is shown in Table 8-33.

Return to the Summary Table.

Table 8-33. LEDS_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Disable LED Stretching	R/W	0h	0h = LED pulses are stretched according to the blink rate in 'LED Blink Rate' field 1h = LED pulses are directly connected to RX_DV(for RX activity) and TX_CTRL(for TX Activity)
13-12	LED Blink Rate	R/W	2h	Blink Rate of the LED when configured for activity 0h = 20Hz (50 ms) 1h = 10Hz (100 ms) 2h = 5Hz (200 ms) 3h = 2Hz (500 ms)
11-8	LED_2 Options	R/W	6h	0h = Link OK 1h = Link OK + blink on TX/RX activity 2h = Link OK + blink on TX activity 3h = Link OK + blink on RX activity 4h = Link OK + 100Base-T1 Leader 5h = Link OK + 100Base-T1 Follower 6h = TX/RX activity with stretch option 7h = Reserved 8h = Reserved 9h = Link lost (remains on until register 0x1 is read) Ah = PRBS error (toggles on error) Bh = XMII TX/RX Error with stretch option
7-4	LED_1 Options	R/W	1h	0h = Link OK 1h = Link OK + blink on TX/RX activity 2h = Link OK + blink on TX activity 3h = Link OK + blink on RX activity 4h = Link OK + 100Base-T1 Leader 5h = Link OK + 100Base-T1 Follower 6h = TX/RX activity with stretch option 7h = Reserved 8h = Reserved 9h = Link lost (remains on until register 0x1 is read) Ah = PRBS error (toggles on error) Bh = XMII TX/RX Error with stretch option
3-0	LED_0 Options	R/W	0h	0h = Link OK 1h = Link OK + blink on TX/RX activity 2h = Link OK + blink on TX activity 3h = Link OK + blink on RX activity 4h = Link OK + 100Base-T1 Leader 5h = Link OK + 100Base-T1 Follower 6h = TX/RX activity with stretch option 7h = Reserved 8h = Reserved 9h = Link lost (remains on until register 0x1 is read) Ah = PRBS error (toggles on error) Bh = XMII TX/RX Error with stretch option

8.2.30 LEDS_CFG_2 Register (Offset = 451h) [Reset = 0049h]

LEDS_CFG_2 is shown in Table 8-34.

Return to the Summary Table.

Table 8-34. LEDS_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12-9	RESERVED	R	0h	Reserved
8	LED_2 Force Enable	R/W	0h	1h = Force 'LED_2 Force Value' on CLKOUT pin (when CLKOUT is configured as LED_2)
7	LED_2 Force Value	R/W	0h	When LED_2 Force Enable is set, this bit decides the output of LED_2 0h = Low 1h = High
6	LED_2 Polarity	R/W	1h	Polarity of LED_2: (When CLKOUT is used as LED_2) 0h = Active Low polarity 1h = Active High polarity
5	LED_1 Force Enable	R/W	0h	1h = Force 'LED_1 Force Value' on LED_1 pin
4	LED_1 Force Value	R/W	0h	When LED_1 Force Enable is set, this bit decides the output of LED_1 0h = Low 1h = High
3	LED_1 Polarity	R/W	1h	Polarity of LED_1: 0h = Active Low polarity 1h = Active High polarity Default value is decided by the strap on LED_1. If the strap is placed to supply, LED_1 polarity is 0, else LED_1 polarity is 1.
2	LED_0 Force Enable	R/W	0h	1h = Force 'LED_0 Force Value' on LED_0 pin
1	LED_0 Force Value	R/W	0h	When LED_0 Force Enable is set, this bit decides the output of LED_0 0h = Low 1h = High
0	LED_0 Polarity	R/W	1h	Polarity of LED_0: 0h = Active Low polarity 1h = Active High polarity Default value is decided by the strap on LED_0. If the strap is placed to supply, LED_0 polarity is 0, else LED_0 polarity is 1

8.2.31 IO_MUX_CFG_1 Register (Offset = 452h) [Reset = 0000h]

IO_MUX_CFG_1 is shown in Table 8-35.

Return to the Summary Table.

Table 8-35. IO_MUX_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10-8	LED_1 Configuration	R/W	0h	Controls the output of LED_1 IO: 2h = WoL 3h = Under-Voltage indication 6h = ESD 7h = Interrupt
7	RESERVED	R	0h	Reserved
6-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-0	LED_0 Configuration	R/W	0h	Controls the output of LED_0 IO: 2h = WoL 3h = Under-Voltage indication 6h = ESD 7h = Interrupt

8.2.32 IO_MUX_CFG_2 Register (Offset = 453h) [Reset = 0001h]

IO_MUX_CFG_2 is shown in Table 8-36.

Return to the Summary Table.

Table 8-36. IO_MUX_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Enable TX_ER on LED_1	R/W	0h	Configures LED_1 pin to TX_ER
14-9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-0	CLKOUT Configuration	R/W	1h	2h = WoL 3h = Under-Voltage indication 6h = ESD 7h = Interrupt

8.2.33 IO_MUX_CFG Register (Offset = 456h) [Reset = 0000h]

IO_MUX_CFG is shown in Table 8-37.

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Table 8-37. IO_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RX PUPD Value	R/W	0h	When RX pins PUPD force control is enabled, PUPD is controlled by this register 0h = No pull 1h = Pull up 2h = Pull down 3h = Reserved
13	RX PUPD Force Control	R/W	0h	Enables PUPD force control on RX MAC pins 0h = No force control 1h = enables force control
12-11	TX PUPD Value	R/W	0h	When TX pins PUPD force control is enabled, PUPD is controlled by this register 0h = No pull 1h = Pull up 2h = Pull down 3h = Reserved
10	TX PUPD Force Control	R/W	0h	Enables PUPD force control on TX MAC pins 0h = No force control 1h = Enables force control
9-6	RESERVED	R	0h	Reserved
5	Impedance Control - RX Pins	R/W	0h	This bit control the IO slew rate of the RX MAC interface pads in MII, RGMII, and RMII mode. Note: Impedance of driver is same regardless of value, RMII is not suitable for slow mode due to timing constraints 0h = Fast Mode (Default) 1h = Slow Mode
4-1	RESERVED	R	0h	Reserved
0	Impedance Control - TX_CLK	R/W	0h	This bit adjusts the slew rate of TX_CLK in MII mode. 0h = Fast Mode (Default) 1h = Slow Mode

8.2.34 CHIP_SOR_1 Register (Offset = 45Dh) [Reset = 0000h]

CHIP_SOR_1 is shown in Table 8-38.

Return to the Summary Table.

Table 8-38. CHIP_SOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	LED_1 Strap	R	0h	LED_1 strap sampled at power up
12	RX_D3 Strap	R	0h	RX_D3 strap sampled at power up
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	LED0_STRAP	R	0h	LED_0 strap sampled at power up or reset
8	RXD3 Strap	R	0h	RX_D3 strap sampled at reset
7	RXD2 Strap	R	0h	RX_D2 strap sampled at power up or reset
6	RXD1 Strap	R	0h	RX_D1 strap sampled at power up or reset
5	RXD0 Strap	R	0h	RX_D0 strap sampled at power up or reset
4	RXCLK Strap	R	0h	RX_CLK strap sampled at power up or reset
3-2	RXER Strap	R	0h	RX_ER strap sampled at power up or reset
1-0	RXDV Strap	R	0h	RX_DV strap sampled at power up or reset

8.2.35 LED1_CLKOUT_ANA_CTRL Register (Offset = 45Fh) [Reset = 000Ch]

LED1_CLKOUT_ANA_CTRL is shown in Table 8-39.

Return to the Summary Table.

Table 8-39. LED1_CLKOUT_ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-2	LED_1 Mux Control	R/W	3h	0h = 25MHz XI Clock for daisy chaining 1h = TX_TCLK for test modes 3h = Signal Selected by 'CLKOUT Configuration'
1-0	CLKOUT Mux Control	R/W	0h	0h = 25MHz XI Clock for daisy chaining 1h = TX_TCLK for test modes 3h = Signal Selected by 'CLKOUT Configuration'

8.2.36 TX_INTER_CFG Register (Offset = 489h) [Reset = 0001h]

TX_INTER_CFG is shown in Table 8-40.

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Table 8-40. TX_INTER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	Force Interleave	R/W	0h	Force interleave on TX
1	TX Interleave Enable	R/W	0h	Enable interleave on TX, if interleave detected on the RX 0h = Interleave on Tx disabled 1h = Interleave on Tx enabled if interleave detected on Rx
0	Interleave Detection Enable	R/W	1h	0h = Disable Interleave Detection 1h = Enable Interleave Detection

8.2.37 JABBER_CFG Register (Offset = 496h) [Reset = 044Ch]

JABBER_CFG is shown in Table 8-41.

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Table 8-41. JABBER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10-0	Jabber Timeout Count	R/W	44Ch	Jabber timeout count in µs

8.2.38 PG_REG_4 Register (Offset = 553h) [Reset = 0000h]

PG_REG_4 is shown in Table 8-42.

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Table 8-42. PG_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	Force Receive Polarity Force Enable	R/W	0h	Enable force on polarity 0h = Auto-polarity on MDI 1h = Force polarity on MDI
12	Receive Polarity Force Value	R/W	0h	Polarity force value. Only valid if bit [13] is 1. 0h = Forced Normal polarity 1h = Forced Inverted polarity
11-0	RESERVED	R	0h	Reserved

8.2.39 TC1_CFG_RW Register (Offset = 560h) [Reset = 07E4h]

TC1_CFG_RW is shown in Table 8-43.

Return to the Summary Table.

Table 8-43. TC1_CFG_RW Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12-11	Link Status Metric	R/W	0h	Selects following link up signals as defined by C&S 0h = link_up_c_and_s 1h = link_montor_status 2h = (phy_control = SEND_DATA) 3h = comm_ready from TC1 spec
10-5	Link Failure Scenario	R/W	3Fh	Each bit enables logging of link failure in the given scenario: Bit[5] - SQI greater than the value configured in the SQI Threshold register Bit[6] - RCV_JABBER_DET5 - BAD_SSD Bit[7] - LINK_FAILED Bit[8] - RX_ERROR Bit[9] - BAD_END Bit[10] - RESERVED
4-3	Comm Timer Value	R/W	0h	Selects the hysteresis timer value for TC1 comm ready 0h = 2ms 1h = 500µs 2h = 1ms 3h = 4ms
2-0	SQI Threshold	R/W	4h	SQI threshold used to increment Link Failure Count defined by TC1. Whenever SQI becomes worse than the threshold, link failure count (Register 0x0561 bit[9:0]) as defined by TC1 is incremented

8.2.40 TC1_LINK_FAIL_LOSS Register (Offset = 561h) [Reset = 0000h]

TC1_LINK_FAIL_LOSS is shown in Table 8-44.

Return to the Summary Table.

Table 8-44. TC1_LINK_FAIL_LOSS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Link Losses	R	0h	Number of Link Losses as defined in TC1 since last power cycle
9-0	Link Failures	R	0h	Link Failures as defined in TC1 Number of Link Failures (including RX errors, Bad SSD, Bad ESD, Bad SQI) not causing a link down

8.2.41 TC1_LINK_TRAINING_TIME Register (Offset = 562h) [Reset = 0000h]

TC1_LINK_TRAINING_TIME is shown in Table 8-45.

Return to the Summary Table.

Table 8-45. TC1_LINK_TRAINING_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Communication Ready	R	0h	Communication ready as defined in TC1 1h = PHY is ready for communication
14-8	RESERVED	R	0h	Reserved
7-0	Link Training Time	R	0h	Link Training Time measured in milliseconds measured from soft reset

8.2.42 NO_LINK_TH Register (Offset = 563h) [Reset = 0096h]

NO_LINK_TH is shown in Table 8-46.

Return to the Summary Table.

Table 8-46. NO_LINK_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	cfg_no_link_timer_th	R/W	96h	If link is not obtained within this amount of time(in milliseconds), interrupt is provided if enabled

8.2.43 RGMII_CTRL Register (Offset = 600h) [Reset = 0030h]

RGMII_CTRL is shown in Table 8-47.

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Table 8-47. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6-4	RGMII TX FIFO Half Full Threshold	R/W	3h	RGMII TX sync FIFO half full threshold
3	RGMII Enable	R/W	0h	0h = RGMII disable Default value is latched from straps 1h = RGMII enable
2	Invert RGMII TX Data Lines	R/W	0h	1h = Invert RGMII TXD[3:0] TX_D3 to TX_D0 TX_D2 to TX_D1 TX_D1 to TX_D2 TX_D0 to TX_D3
1	Invert RGMII RX Data Lines	R/W	0h	1h = Invert RGMII RXD[3:0] RX_D3 to RX_D0 RX_D2 to RX_D1 RX_D1 to RX_D2 RX_D0 to RX_D3
0	RESERVED	R	0h	Reserved

8.2.44 RGMII_FIFO_STATUS Register (Offset = 601h) [Reset = 0000h]

RGMII_FIFO_STATUS is shown in Table 8-48.

Return to the Summary Table.

Table 8-48. RGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	RGMII TX FIFO Full Error	R	0h	0h = No empty fifo error This bit is only cleared on device reset 1h = RGMII TX full error has been indicated
0	RGMII TX FIFO Empty Error	R	0h	0h = No empty fifo error This bit is only cleared on device reset 1h = RGMII TX empty error has been indicated

8.2.45 RGMII_CLK_SHIFT_CTRL Register (Offset = 602h) [Reset = 0000h]

RGMII_CLK_SHIFT_CTRL is shown in Table 8-49.

Return to the Summary Table.

Table 8-49. RGMII_CLK_SHIFT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	RGMII RX Shift	R/W	0h	0h = Clock and data are aligned 1h = Clock is internally delayed by value programmed in DLL RX Shift Delay in register 0x430
0	RGMII TX Shift	R/W	0h	0h = Clock and data are aligned 1h = Clock is internally delayed by value programmed in DLL TX Shift Delay in register 0x430

8.2.46 SGMII_CTRL_1 Register (Offset = 608h) [Reset = 007Bh]

SGMII_CTRL_1 is shown in Table 8-50.

Return to the Summary Table.

Table 8-50. SGMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SGMII TX Error Disable	R/W	0h	0h = Enable SGMII TX Error indication 1h = Disable SGMII TX Error indication
14	RESERVED	R	0h	Reserved
13-10	RESERVED	R	0h	Reserved
9	SGMII Enable	R/W	0h	1b = SGMII enable 0b = SGMII disable Default value is latched from straps If both SGMII and RGMII are enabled, SGMII take precedence
8	SGMII TX Polarity Invert	R/W	0h	1b = Invert SGMII RX_D[3:2] polarity
7	SGMII TX Polarity Invert	R/W	0h	1b = Invert SGMII TX_D[1:0] polarity
6-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-1	SGMII Auto Negotiation Timer	R/W	1h	Selects duration of SGMII Auto-Negotiation timer 0h = 1.6ms 1h = 2µs 2h = 800µs 3h = 11ms
0	SGMII Auto Negotiation Enable	R/W	1h	0h = Disable SGMII Auto-Negotiation 1h = Enable SGMII Auto-Negotaition

8.2.47 SGMII_STATUS Register (Offset = 60Ah) [Reset = 0000h]

SGMII_STATUS is shown in Table 8-51.

Return to the Summary Table.

Table 8-51. SGMII_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	SGMII Page Received	R	0h	0h = No new auto neg page received 1h = A new auto neg page received
11	SGMII Link Status	R	0h	0h = SGMII link is down 1h = SGMII link is up
10	SGMII Auto Negotiation Status	R	0h	1h = SGMII autoneg completed
9	Word Boundary Align Indication	R	0h	1h = Aligned
8	Word Boundary Sync Status	R	0h	0h = Sync not achieved 1h = Sync achieved
7-4	Word Boundary Index	R	0h	Word boundary index selection
3-0	RESERVED	R	0h	Reserved

8.2.48 SGMII_CTRL_2 Register (Offset = 60Ch) [Reset = 0024h]

SGMII_CTRL_2 is shown in Table 8-52.

Return to the Summary Table.

Table 8-52. SGMII_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	SGMII CDR Lock Value	R/W	0h	SGMII CDR lock force value
7	SGMII CDR Lock Force Enable	R/W	0h	SGMII CDR lock force enable
6	SGMII Auto Negotiation Restart	RH/W1S	0h	Restart SGMII auto negotiation
5-3	SGMII TX FIFO Half Full Threshold	R/W	4h	SGMII TX sync FIFO half full threshold
2-0	SGMII RX FIFO Half Full Threshold	R/W	4h	SGMII RX sync FIFO half full threshold

8.2.49 SGMII_FIFO_STATUS Register (Offset = 60Dh) [Reset = 0000h]

SGMII_FIFO_STATUS is shown in Table 8-53.

Return to the Summary Table.

Table 8-53. SGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	SGMII RX FIFO Full Error	H	0h	0h = No error indication 1h = SGMII RX fifo full error has been indicated
2	SGMII RX FIFO Empty Error	H	0h	0h = No error indication 1h = SGMII RX fifo empty error has been indicated
1	SGMII TX FIFO Full Error	H	0h	0h = No error indication 1h = SGMII TX fifo full error has been indicated
0	SGMII TX FIFO Empty Error	H	0h	0h = No error indication 1h = SGMII TX fifo empty error has been indicated

8.2.50 PRBS_STATUS_1 Register (Offset = 618h) [Reset = 0000h]

PRBS_STATUS_1 is shown in Table 8-54.

Return to the Summary Table.

Table 8-54. PRBS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	PRBS Error Overflow Counter	R	0h	Holds number of error counter overflow that received by the PRBS checker. Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. Counter stops on 0xFF. Note: when PRBS counters work in single mode, overflow counter is not active

8.2.51 PRBS_CTRL_1 Register (Offset = 619h) [Reset = 0574h]

PRBS_CTRL_1 is shown in Table 8-55.

Return to the Summary Table.

Table 8-55. PRBS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	Packet Generation Configuration	R/W	0h	0h = Transmit 1518 byte packets in packet generation mode 1h = Transmit 64 byte packets in packet generation mode
12	Send Packet	RH/W1S	0h	Enables generating MAC packet with fix/incremental data with CRC (pkt_gen_en has to be set and cfg_pkt_gen_prbs has to be clear) Cleared automatically when pkt_done is set
11	RESERVED	R	0h	Reserved
10-8	PRBS Check Select	R/W	5h	000b : Checker receives from RGMII TX 001b : Checker receives from SGMII TX 010b : Checker receives from RMII RX 011b : Checker receives from MII 101b : Checker receives from Cu RX 110b : Reserved 111b : Reserved
7	RESERVED	R	0h	Reserved
6-4	PRBS Transmit Select	R/W	7h	000b : PRBS transmits to RGMII RX 001b : PRBS transmits to SGMII RX 010b : PRBS transmits to RMII RX 011b : PRBS transmits to MII RX 101b : PRBS transmits to Cu TX 110b : Reserved 111b : Reserved
3	PRBS Count Mode	R/W	0h	0h = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting. 1h = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again
2	PRBS Checker Enable	R/W	1h	Enable PRBS checker (to receive data) To be enabled for counters in 0x63C, 0x63D, 0x63E to work 1h = Enable PRBS checker
1	PRBS Generation Enable	R/W	0h	If 0x619[0] is set, 0h = Transmits non-PRBS packet (PRBS checker is also disabled in this case) 1h = Transmits PRBS packet
0	PRBS or Packet Generation Enable	R/W	0h	0h = Disable packet/PRBS generator 1h = Enable packet/PRBS generator

8.2.52 PRBS_CTRL_2 Register (Offset = 61Ah) [Reset = 05DCh]

PRBS_CTRL_2 is shown in Table 8-56.

Return to the Summary Table.

Table 8-56. PRBS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Packet Length	R/W	5DCh	Sets packet length (in bytes) between the PRBS packets or nonPRBS packets generated

8.2.53 PRBS_CTRL_3 Register (Offset = 61Bh) [Reset = 007Dh]

PRBS_CTRL_3 is shown in Table 8-57.

Return to the Summary Table.

Table 8-57. PRBS_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	PRBS IPG	R/W	7Dh	Sets IPG (in bytes) between the PRBS packets or non-PRBS packets generated

8.2.54 PRBS_STATUS_2 Register (Offset = 61Ch) [Reset = 0000h]

PRBS_STATUS_2 is shown in Table 8-58.

Return to the Summary Table.

Table 8-58. PRBS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Checker Byte Count	R	0h	Holds number of total bytes that received by the PRBS checker. Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFF This counter is cleared if this counter is read after programming 0x620[1]=1

8.2.55 PRBS_STATUS_3 Register (Offset = 61Dh) [Reset = 0000h]

PRBS_STATUS_3 is shown in Table 8-59.

Return to the Summary Table.

Table 8-59. PRBS_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Checker Packet Count-1	R	0h	Holds Bits [15:0] of number of total packets received by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x61D,0x61E are read in the same order after programming 0x620[1]=1

8.2.56 PRBS_STATUS_4 Register (Offset = 61Eh) [Reset = 0000h]

PRBS_STATUS_4 is shown in Table 8-60.

Return to the Summary Table.

Table 8-60. PRBS_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Checker Packet Count-2	R	0h	Holds Bits [31:16] of number of total packets received by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x61D,0x61E are read in the same order after programming 0x620[1]=1

8.2.57 PRBS_STATUS_5 Register (Offset = 620h) [Reset = 0000h]

PRBS_STATUS_5 is shown in Table 8-61.

Return to the Summary Table.

Table 8-61. PRBS_STATUS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	MAC Packet Gen Done	R	0h	Set when all MAC packets with CRC are transmitted 0h = MAC packet transmission in progress 1h = MAC packets transmission completed
11	MAC Packet Gen Busy	R	0h	0h = Packet generator is not in process 1h = Packet generator is in process
10	PRBS Checker Packet Count Overflow Status	R	0h	If PRBS Checker Packet Count overflows, this status bit is set to 1 This overflow status is cleared after clearing PRBS byte counter using 0x620[1]
9	PRBS Checker Byte Count Overflow Status	R	0h	If PRBS Checker Byte Count overflows, this status bit is set to 1 This overflow status is cleared after clearing PRBS byte counter using 0x620[1]
8	PRBS Lock	R	0h	1h = PRBS checker is locked and synced with the received stream
7-0	PRBS Error Count	R	0h	Writing 1 to bit 0 locks all PRBS counters Writing 1 to bit1 locks all PRBS counters and clears the counters on read of those specific registers Bits [1:0] are self-cleared after write Reading Bits[7:0] after writing bit0/bit1, gives the number of error bits received by PRBS checker When PRBS Count Mode set to zero, count stops on 0xFF

8.2.58 PRBS_STATUS_6 Register (Offset = 622h) [Reset = 0000h]

PRBS_STATUS_6 is shown in Table 8-62.

Return to the Summary Table.

Table 8-62. PRBS_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Packer Error Count-1	R	0h	Holds Bits [15:0] of number of total packets received with error by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x622,0x623 are read in the same order after programming 0x620[1]=1

8.2.59 PRBS_STATUS_7 Register (Offset = 623h) [Reset = 0000h]

PRBS_STATUS_7 is shown in Table 8-63.

Return to the Summary Table.

Table 8-63. PRBS_STATUS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Packer Error Count-2	R	0h	Holds Bits [31:16] of number of total packets received with error by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x622,0x623 are read in the same order after programming 0x620[1]=1

8.2.60 PRBS_CTRL_4 Register (Offset = 624h) [Reset = 5511h]

PRBS_CTRL_4 is shown in Table 8-64.

Return to the Summary Table.

Table 8-64. PRBS_CTRL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Packet Data	R/W	55h	Fixed data to be sent when MAC Packet Mode is set to Fixed mode
7-6	MAC Packet Mode	R/W	0h	0h = Incremental 1h = Fixed 2h = PRBS 3h = PRBS
5-3	Pattern Length in MAC Packets	R/W	2h	Number of bytes of valid pattern in packet (Max - 6)
2-0	Packet Count for MAC Packets Mode	R/W	1h	0h = 1 packet 1h = 10 packets 2h = 100 packets 3h = 1000 packets 4h = 10000 packets 5h = 100000 packets 6h = 1000000 packets 7h = Continuous packets

8.2.61 PATTERN_CTRL_1 Register (Offset = 625h) [Reset = 0000h]

PATTERN_CTRL_1 is shown in Table 8-65.

Return to the Summary Table.

Table 8-65. PATTERN_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Pattern in MAC Packets [15:0]	R/W	0h	Bytes 0,1 of programmable pattern in MAC packets

8.2.62 PATTERN_CTRL_2 Register (Offset = 626h) [Reset = 0000h]

PATTERN_CTRL_2 is shown in Table 8-66.

Return to the Summary Table.

Table 8-66. PATTERN_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Pattern in MAC Packets [31:16]	R/W	0h	Bytes 2,3 of programmable pattern in MAC packets

8.2.63 PATTERN_CTRL_3 Register (Offset = 627h) [Reset = 0000h]

PATTERN_CTRL_3 is shown in Table 8-67.

Return to the Summary Table.

Table 8-67. PATTERN_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Pattern in MAC Packets [47:32]	R/W	0h	Bytes 4,5 of programmable pattern in MAC packets

8.2.64 PMATCH_CTRL_1 Register (Offset = 628h) [Reset = 0000h]

PMATCH_CTRL_1 is shown in Table 8-68.

Return to the Summary Table.

Table 8-68. PMATCH_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Destination Address in MAC Packets [15:0]	R/W	0h	Destination Address field in the generated MAC packets

8.2.65 PMATCH_CTRL_2 Register (Offset = 629h) [Reset = 0000h]

PMATCH_CTRL_2 is shown in Table 8-69.

Return to the Summary Table.

Table 8-69. PMATCH_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Destination Address in MAC Packets [31:16]	R/W	0h	Destination Address field in the generated MAC packets

8.2.66 PMATCH_CTRL_3 Register (Offset = 62Ah) [Reset = 0000h]

PMATCH_CTRL_3 is shown in Table 8-70.

Return to the Summary Table.

Table 8-70. PMATCH_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Destination Address in MAC Packets [47:32]	R/W	0h	Destination Address field in the generated MAC packets

8.2.67 TX_PKT_CNT_1 Register (Offset = 639h) [Reset = 0000h]

TX_PKT_CNT_1 is shown in Table 8-71.

Return to the Summary Table.

Table 8-71. TX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TX Packet Count [15:0]	RC	0h	Lower 16 bits of TX packets from MAC counter Note : Register is cleared when 0x639, 0x63A, 0x63B are read in sequence

8.2.68 TX_PKT_CNT_2 Register (Offset = 63Ah) [Reset = 0000h]

TX_PKT_CNT_2 is shown in Table 8-72.

Return to the Summary Table.

Table 8-72. TX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TX Packet Count [31:16]	RC	0h	Upper 16 bits of TX packets from MAC counter Note : Register is cleared when 0x639, 0x63A, 0x63B are read in sequence

8.2.69 TX_PKT_CNT_3 Register (Offset = 63Bh) [Reset = 0000h]

TX_PKT_CNT_3 is shown in Table 8-73.

Return to the Summary Table.

Table 8-73. TX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TX Error Packet Count	RC	0h	TX packets from MAC with CRC error counter Note : Register is cleared when 0x639, 0x63A, 0x63B are read in sequence

8.2.70 RX_PKT_CNT_1 Register (Offset = 63Ch) [Reset = 0000h]

RX_PKT_CNT_1 is shown in Table 8-74.

Return to the Summary Table.

Table 8-74. RX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Packet Count [15:0]	RC	0h	Lower 16 bits of RX packets received from MDI Note : Register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

8.2.71 RX_PKT_CNT_2 Register (Offset = 63Dh) [Reset = 0000h]

RX_PKT_CNT_2 is shown in Table 8-75.

Return to the Summary Table.

Table 8-75. RX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Packet Count [31:16]	RC	0h	Upper 16 bits of RX packets received from MDI Note : Register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

8.2.72 RX_PKT_CNT_3 Register (Offset = 63Eh) [Reset = 0000h]

RX_PKT_CNT_3 is shown in Table 8-76.

Return to the Summary Table.

Table 8-76. RX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Error Packet Count	RC	0h	Rx packet with error (CRC error) counter Note : Register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

8.2.73 RMII_CTRL_1 Register (Offset = 648h) [Reset = 0120h]

RMII_CTRL_1 is shown in Table 8-77.

Return to the Summary Table.

Table 8-77. RMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	RMII TXD Delay Disable	R/W	0h	If set, disables delay of TXD in RMII mode
9-7	RMII Half Full Threshold	R/W	2h	FIFO Half Full Threshold in nibbles for the RMII Rx FIFO
6	RMII Enable	R/W	0h	1h = RMII Enable
5	RESERVED	R	0h	Reserved
4	RMII Follower Enable	R/W	0h	Not recommended to configure this bit. Can be used as a status bit 1h = RMII Follower mode is enabled
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RMII Rev1.0 Enable	R/W	0h	1h = Enable RMII rev1.0
0	RMII Enhanced Mode Enable	R/W	0h	1h = Enable RMII Enhanced mode

8.2.74 RMII_STATUS_1 Register (Offset = 649h) [Reset = 0000h]

RMII_STATUS_1 is shown in Table 8-78.

Return to the Summary Table.

Table 8-78. RMII_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	RMII FIFO Empty Error	R	0h	Clear on read bit RMII FIFO underflow error status
0	RMII FIFO Full Error	R	0h	Clear on Read bit RMII FIFO overflow status

8.2.75 dsp_reg_71 Register (Offset = 871h) [Reset = 0000h]

dsp_reg_71 is shown in Table 8-79.

Return to the Summary Table.

Table 8-79. dsp_reg_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-5	Worst SQI	RC	0h	Worst SQI value since last read
4	RESERVED	R	0h	Reserved
3-1	SQI Value	R	0h	SQI value
0	RESERVED	R	0h	Reserved

8.2.76 MMD1_PMA_CTRL_1 Register (Offset = 1000h) [Reset = 0000h]

MMD1_PMA_CTRL_1 is shown in Table 8-80.

Return to the Summary Table.

Table 8-80. MMD1_PMA_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PMA Reset	R/W	0h	1h = PMA reset
14-1	RESERVED	R	0h	Reserved
0	PMA Loopback	R/W	0h	1h = PMA loopback set

8.2.77 MMD1_PMA_STATUS_1 Register (Offset = 1001h) [Reset = 0000h]

MMD1_PMA_STATUS_1 is shown in Table 8-81.

Return to the Summary Table.

Table 8-81. MMD1_PMA_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	Link Status	R	0h	1h = Link is up
1-0	RESERVED	R	0h	Reserved

8.2.78 MMD1_PMA_STATUS_2 Register (Offset = 1007h) [Reset = 003Dh]

MMD1_PMA_STATUS_2 is shown in Table 8-82.

Return to the Summary Table.

Table 8-82. MMD1_PMA_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5-0	PMA PMD Type Selection	R	3Dh	PMA or PMD type selection field 111101b = 100BASE-T1 PMA or PMD

8.2.79 MMD1_PMA_EXT_ABILITY_1 Register (Offset = 100Bh) [Reset = 0800h]

MMD1_PMA_EXT_ABILITY_1 is shown in Table 8-83.

Return to the Summary Table.

Table 8-83. MMD1_PMA_EXT_ABILITY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	Extended Abilities	R	1h	0h = PMA/PMD does not have extended abilities 1h = PMA/PMD has BASE-T1 extended abilities
10-0	RESERVED	R	0h	Reserved

8.2.80 MMD1_PMA_EXT_ABILITY_2 Register (Offset = 1012h) [Reset = 0001h]

MMD1_PMA_EXT_ABILITY_2 is shown in Table 8-84.

Return to the Summary Table.

Table 8-84. MMD1_PMA_EXT_ABILITY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	100BASE-T1 Ability	R	1h	0h = PMA/PMD does not support 100BASE-T1 1h = PMA/PMD supports 100BASE-T1

8.2.81 MMD1_PMA_CTRL_2 Register (Offset = 1834h) [Reset = 8000h]

MMD1_PMA_CTRL_2 is shown in Table 8-85.

Return to the Summary Table.

Table 8-85. MMD1_PMA_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Leader Follower Configuration	R/W	0h	0h = Configure PHY as follower 1h = Configure PHY as leader
13-4	RESERVED	R	0h	Reserved
3-0	Type Selection	R	0h	Type selection field 0h = 100BASE-T1

8.2.82 MMD1_PMA_TEST_MODE_CTRL Register (Offset = 1836h) [Reset = 0000h]

MMD1_PMA_TEST_MODE_CTRL is shown in Table 8-86.

Return to the Summary Table.

Table 8-86. MMD1_PMA_TEST_MODE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	Compliance Test Mode	R/W	0h	100BASE-T1 test mode control 000b = Normal mode operation 001b = Test mode 1 010b = Test mode 2 011b = Reserved 100b = Test mode 4 101b = Test mode 5 110b = Reserved 111b = Reserved
12-0	RESERVED	R	0h	Reserved

8.2.83 MMD3_PCS_CTRL_1 Register (Offset = 3000h) [Reset = 0000h]

MMD3_PCS_CTRL_1 is shown in Table 8-87.

Return to the Summary Table.

Table 8-87. MMD3_PCS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCS Reset	R/W	0h	Reset bit, Self Clear. When write to this bit 1: 1. Reset the registers (not vendor specific) at MMD3/MMD7. 2. Reset brk_top Please note: This register is WSC (write-self-clear) and not read-only
14	PCS Loopback	R/W	0h	This bit is cleared by PCS Reset
13-11	RESERVED	R	0h	Reserved
10	RX Clock Stoppable	R/W	0h	RW, reset value = 1. 1= PHY can stop receiving clock during LPI 0= Clock not stoppable Note: This flop implemented at glue logic
9-0	RESERVED	R	0h	Reserved

8.2.84 MMD3_PCS_Status_1 Register (Offset = 3001h) [Reset = 0000h]

MMD3_PCS_Status_1 is shown in Table 8-88.

Return to the Summary Table.

Table 8-88. MMD3_PCS_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	TX LPI Received	R	0h	0h = LPI not received 1h = Tx PCS has received LPI
10	RX LPI Received	R	0h	0h = LPI not received 1h = Rx PCS has received LPI
9	TX LPI Indication	R	0h	0h = PCS is not currently receiving LPI 1h = TX PCS is currently receiving LPI
8	RX LPI Indication	R	0h	0h = PCS is not currently receiving LPI 1h = RX PCS is currently receiving LPI
7	RESERVED	R	0h	Reserved
6	TX Clock Stoppable	R	0h	0h = Clock not stoppable 1h = The MAC can stop the clock during LPI
5-0	RESERVED	R	0h	Reserved

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DP83TC814 is a single-port 100Mbps Automotive Ethernet PHY. It supports IEEE 802.3bw and allows for connections to an Ethernet MAC through MII, RMII, RGMII, or SGMII. When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required connections.

Note

Refer to SNLA389 Application Note for more information about the register settings used for compliance testing. It is necessary to use these register settings to achieve the same performance as observed during compliance testing.

9.2 Typical Applications

Figure 9-2 through Figure 9-6 show some the typical applications for the DP83TC814x-Q1.

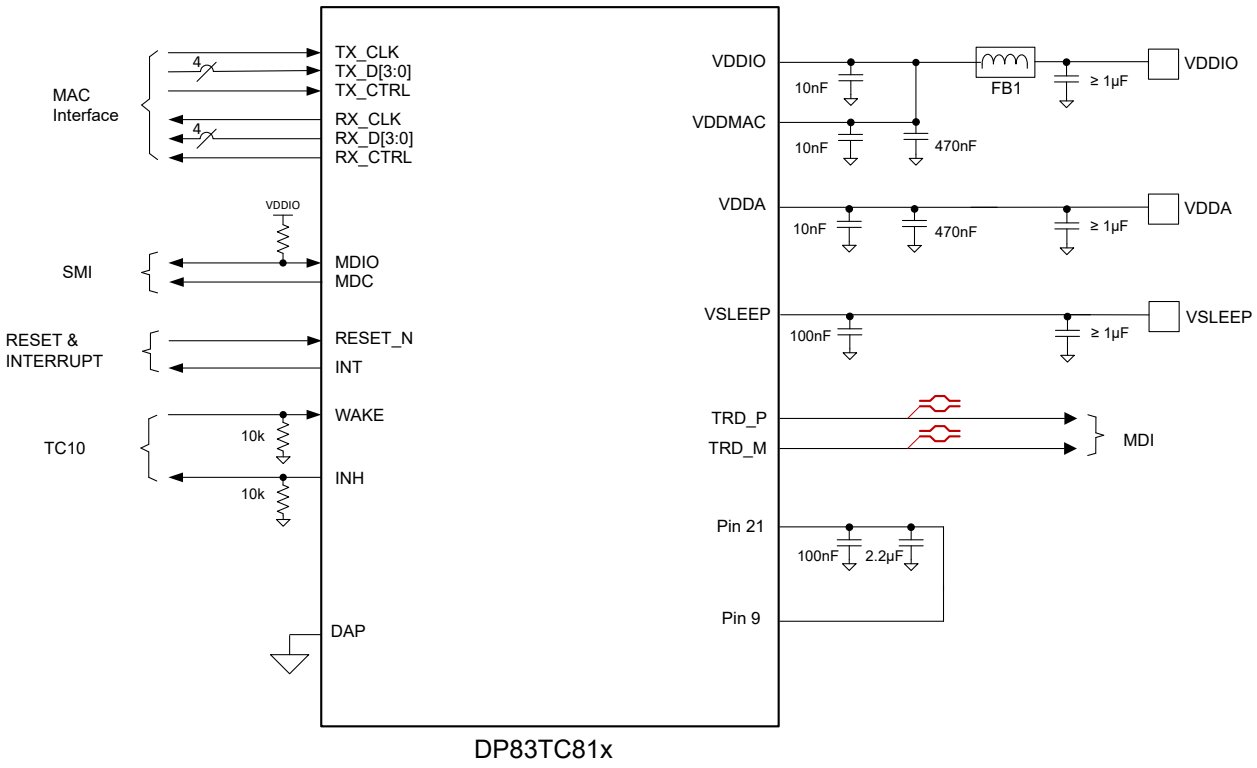

Figure 9-1. Typical Application (General)

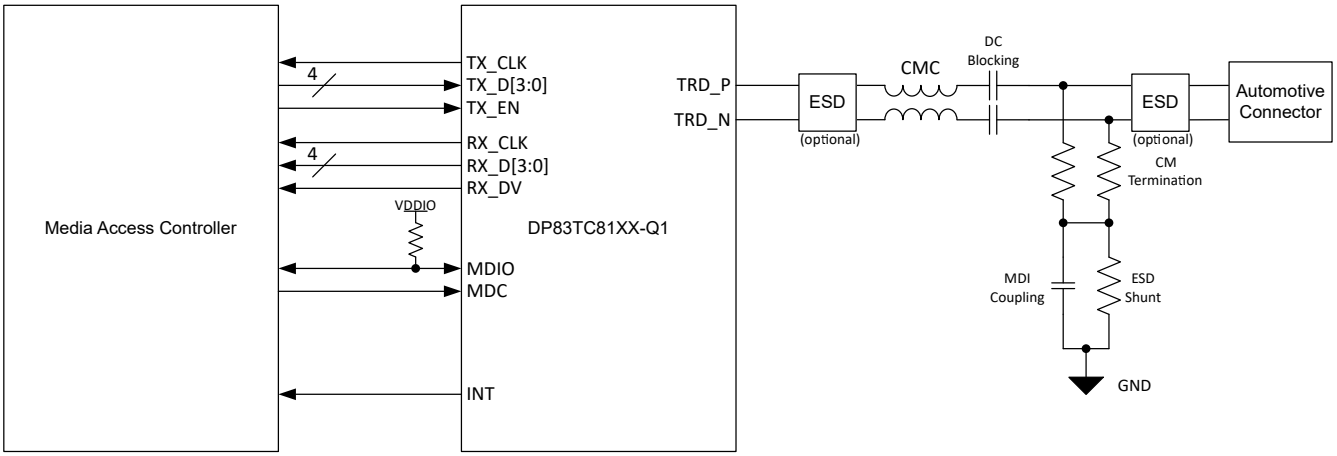

Figure 9-2. Typical Application (MII)

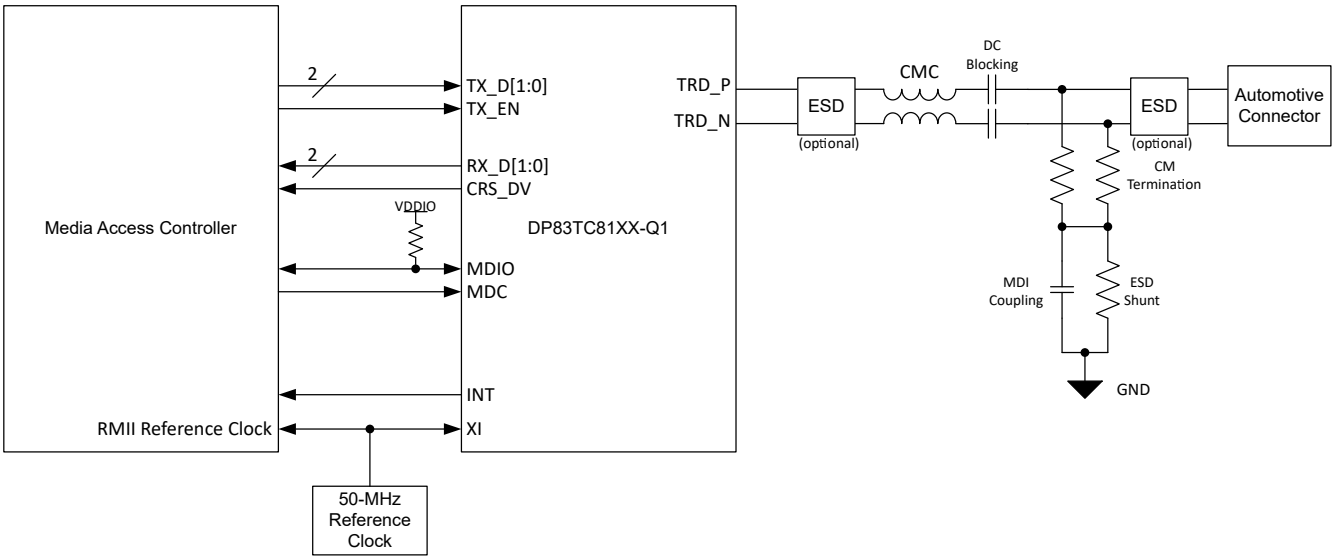

Figure 9-3. Typical Application (RMII Follower)

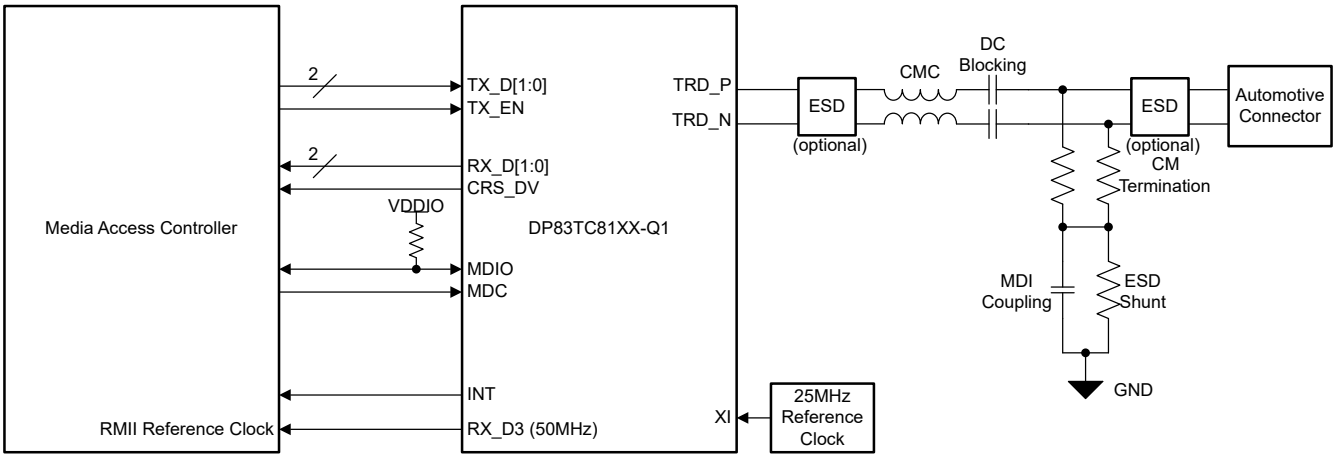

Figure 9-4. Typical Application (RMII Leader)

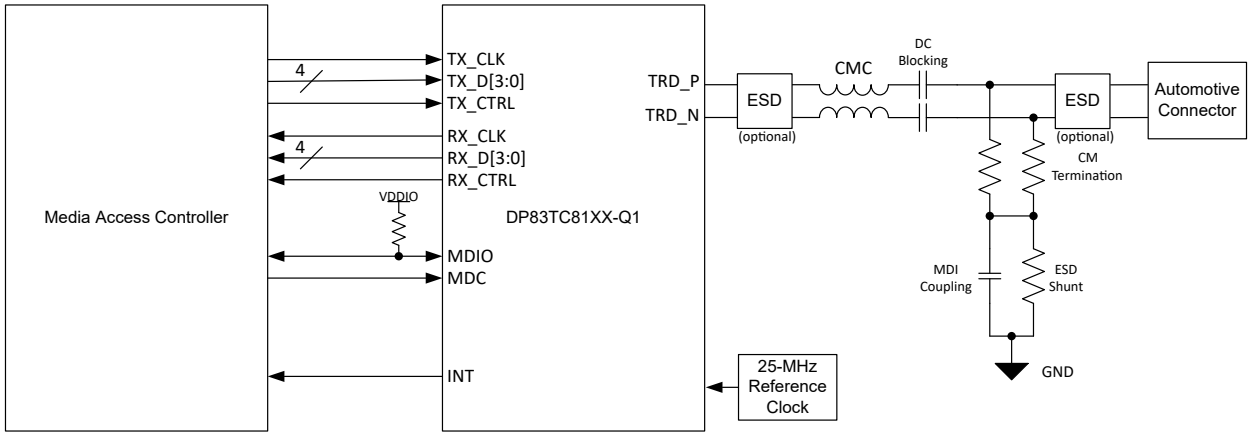

Figure 9-5. Typical Application (RGMII)

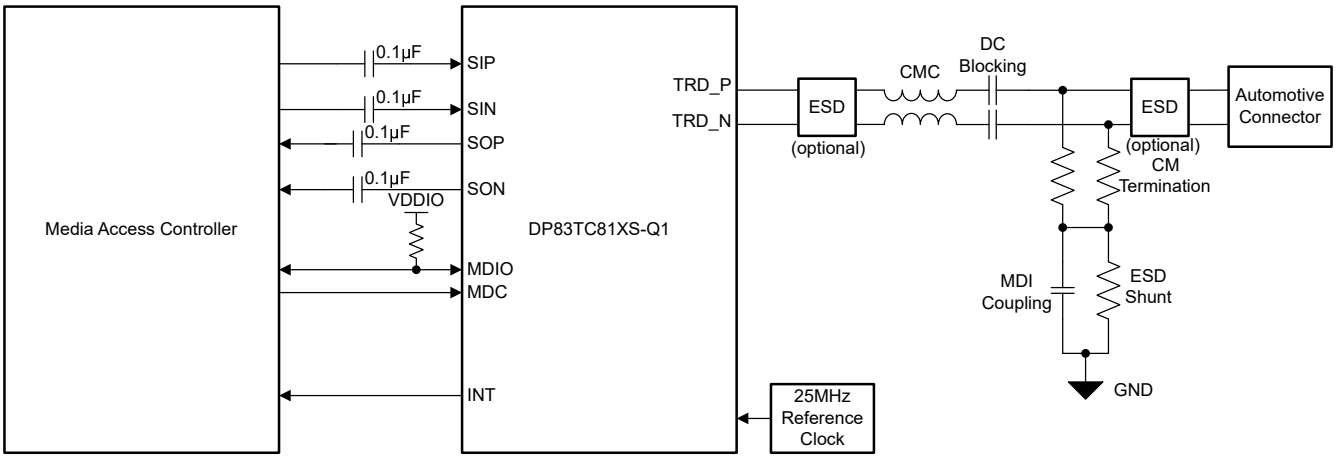

Figure 9-6. Typical Application (SGMII)

9.2.1 Design Requirements

For these typical applications, use the following as design parameters from the table below. Refer to *Power Supply Recommendations* section for detailed connection diagram.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8V, 2.5V, or 3.3V
V_{DDMAC}	1.8V, 2.5V, or 3.3V
V_{DDA}	3.3V
Decoupling capacitors V_{DDIO} (2) (3)	0.01µF
(Optional) ferrite bead for V_{DDIO} (3)	1kΩ at 100MHz (BLM18KG601SH1D)
Decoupling capacitors V_{DDMAC} (2)	0.01µF, 0.47µF
Ferrite bead for V_{DDMAC}	1kΩ at 100MHz (BLM18KG601SH1D)
Decoupling capacitors V_{DDA} (2)	0.01µF, 0.47µF
(Optional) ferrite bead for V_{DDA}	1kΩ at 100MHz (BLM18KG601SH1D)
Decoupling capacitors V_{DDA}(pin 7)	0.1µF
DC Blocking Capacitors (2)	0.1µF
Common-Mode Choke	200µH
Common Mode Termination Resistors(1)	1kΩ
MDI Coupling Capacitor (2)	4.7nF
ESD Shunt(2)	100kΩ
Reference Clock	25MHz

(1) 1% tolerance components are recommended.
(2) 10% tolerance components are recommended.
(3) If VDDIO is separate from VDDMAC then additional ferrite bead and 0.47µF capacitor is required on VDDIO.

9.2.1.1 Physical Medium Attachment

There must be no metal running beneath the common-mode choke. CMCs can inject noise into metal beneath them, which can affect the emissions and immunity performance of the system. Because the DP83TC814S-Q1 is a voltage mode line driver, no external termination resistors are required. The ESD shunt and MDI coupling capacitor must be connected to ground. Verify that the common mode termination resistors are 1% tolerance or better to improve differential coupling.

9.2.1.1.1 Common-Mode Choke Recommendations

The following CMCs are recommended for use with the DP83TC814S-Q1 :

Table 9-2. Recommended CMCs

MANUFACTURER	PART NUMBER
Pulse Electronics	AE2002
Murata	DLW43MH201XK2L
Murata	DLW32MH201XK2
TDK	ACT1210L-201

Table 9-3. CMC Electrical Specifications

PARAMETER	TYP	UNITS	CONDITIONS
Insertion Loss	–0.5	dB	1 – 30MHz
	–1.0	dB	30 – 60MHz
Return Loss	–26	dB	1 – 30MHz
	–20	dB	30 – 60MHz
Common-Mode Rejection	–24	dB	1MHz
	–42	dB	10 – 100MHz
	–25	dB	400MHz
Differential Common-Mode Rejection	–70	dB	1 – 10MHz
	–50	dB	100MHz
	–24	dB	1000MHz

9.2.2 Detailed Design Procedure

When creating a new system design with an Ethernet PHY, follow this schematic capture procedure:

1. Use the 'Strap Tool' tab from the Schematic Checklist to select the correct external bootstrap resistors.
2. Select desired PHY hardware configurations described in Section 7.5.1.
3. Go through and use the 'Pinwise Checklist' tab Schematic Checklist as a guide for your schematic design.
4. Use DP83TC812, DP83TC813, and DP83TC814: Configuring for Open Alliance Specification Complianceas a guide for selecting components for the MDI circuit connected to the TRD_M and TRD_P pins.

The following layout procedure must be followed:

1. Locate the PHY near the edge of the board so that short MDI traces can be routed to the desired connector.
2. Place the MDI external components: CMC, DC-blocking capacitors, CM termination, MDI-coupling capacitor, and ESD shunt.
3. Create metal pour keepout under the CMC on the top layer and at least one layer beneath the top later.
4. The MDI TRD_M and TRD_P traces are routed with 100Ω differential.
5. Place the clock source near the XI and XO pins.
6. In MII, RMII, or RGMII mode, the xMII pins are routed 50Ω and are single-ended with reference to ground.
7. The transmit path xMII pins are routed such that setup and hold timing does not violate the PHY requirements.
8. The receive path xMII pins are routed such that setup and hold timing does not violate the MAC requirements.
9. In SGMII mode, the xMII RX_P, RX_M, TX_P, and TX_M pins are routed 100Ω differential.
10. Place the MDIO pullup close to the PHY.
11. Go through 'Layout Checklist' tab from the Schematic Checklist to guide your design.

9.2.3 Application Curves

The following curves are obtained using the PHY evaluation module under nominal conditions.

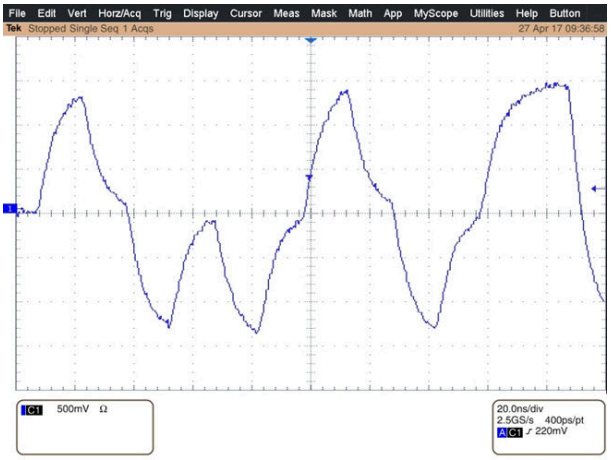

Figure 9-7. MDI IDLE Stream

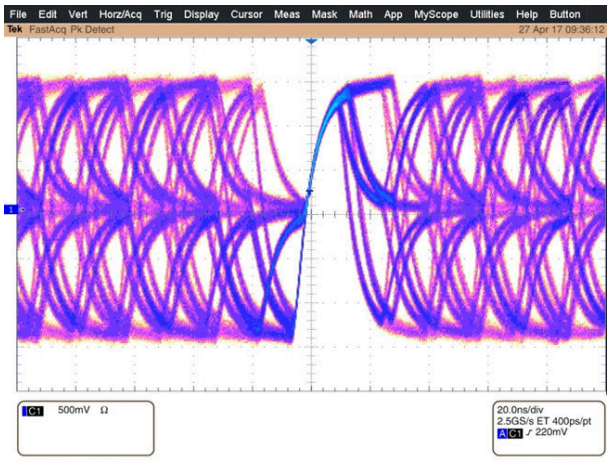

Figure 9-8. MDI IDLE Stream (Variable Persistence)

9.3 Power Supply Recommendations

The DP83TC814S-Q1 is capable of operating with a wide range of IO supply voltages (3.3V, 2.5V, or 1.8V). No power supply sequencing is required. Please note that inputs pins must not be driven until VDDA and VDDIO are stable. The recommended power supply de-coupling network is shown in the figure below. For improved conducted emissions, an optional ferrite bead can be placed between the supply and the PHY de-coupling network.

Typical application block diagram along with supply and peripherals is shown below.

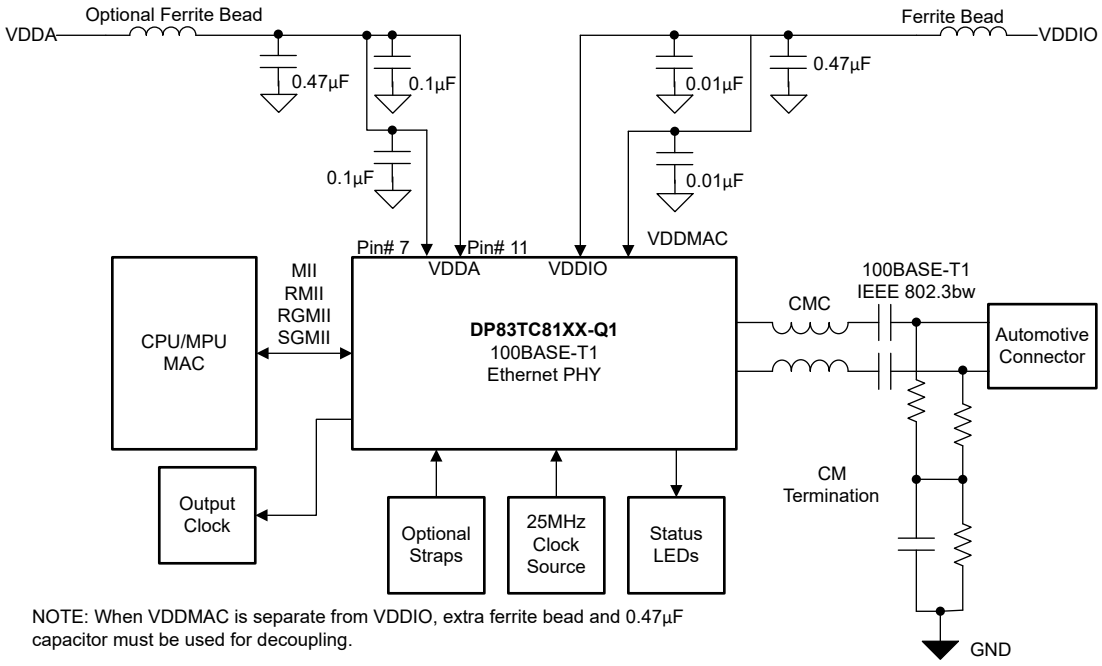

Figure 9-9. Typical Application With Peripherals

When VDDIO and VDDMAC are separate, both voltage rails must have a dedicated network of ferrite bead, 0.47µF, and 0.01µF capacitors.

Current Consumption Break-Down

The following table highlights the break down of power consumption in active mode for each supply rail, specifically highlighting the split between VDDMAC and VDDIO.

Table 9-4. Active Mode Current Consumption

VOLTAGE RAIL	VOLTAGE (V)	MAX CURRENT (mA) [1]
MII		
VDDA	3.3	63
VDDIO	3.3	4
	2.5	3
	1.8	2
VDDMAC	3.3	20
	2.5	15
	1.8	11
VDDA (pin #7)	3.3	2
RMII		
VDDA	3.3	63
VDDIO	3.3	6
	2.5	4
	1.8	3
VDDMAC	3.3	17
	2.5	13
	1.8	10
VDDA (pin #7)	3.3	2
RGMII		
VDDA	3.3	63
VDDIO	3.3	4
	2.5	3
	1.8	2
VDDMAC	3.3	17
	2.5	13
	1.8	10
VDDA (pin #7)	3.3	2
SGMII		
VDDA	3.3	95
VDDIO	3.3	4
	2.5	3
	1.8	2
VDDMAC	3.3	8
	2.5	6
	1.8	4
VDDA (pin #7)	3.3	2

1. Current consumption measured across voltage, temperature, and process with active data communication.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces must be 50Ω, single-ended impedance. Differential traces must be 50Ω single-ended and 100Ω differential. Make sure impedance is controlled throughout. Impedance discontinuities cause reflections leading to emissions and signal integrity issues. Stubs must be avoided on all signal traces, especially differential signal pairs.

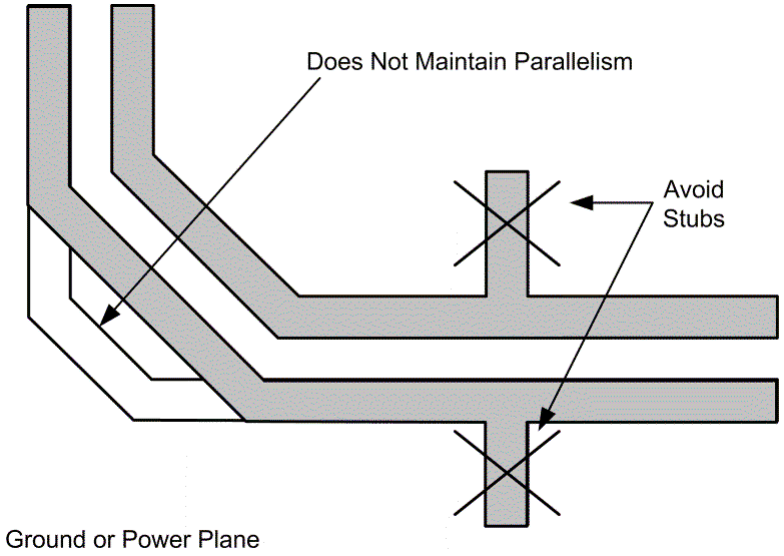

Figure 9-10. Differential Signal Trace Routing

Within the differential pairs, trace lengths must be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces must be length matched to each other and all receive signal traces must be length matched to each other. For SGMII differential traces, keep the skew mismatch below 20ps.

Ideally, there must be no crossover on signal path traces. High speed signal traces must be routed on internal layers to improved EMC performance. However, vias present impedance discontinuities and must be minimized when possible. Route trace pairs on the same layer. Signals on different layers must not cross each other without at least one return path plane between them. Differential pairs must always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

9.4.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces must be avoided at all cost. A signal crossing a split plane can cause unpredictable return path currents and can impact signal quality and result in emissions issues.

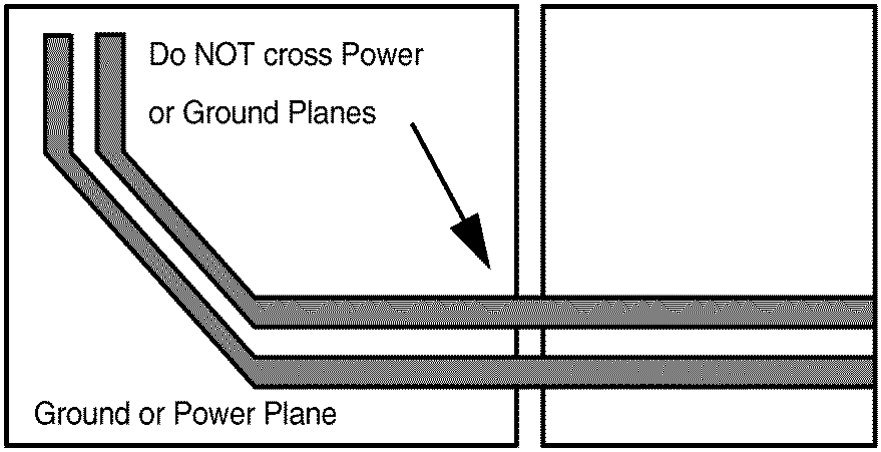

Figure 9-11. Power and Ground Plane Breaks

9.4.1.3 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

9.4.1.4 PCB Layer Stacking

To meet signal integrity and performance requirements, minimum four-layer PCB is recommended. However, a six-layer PCB and above must be used when possible.

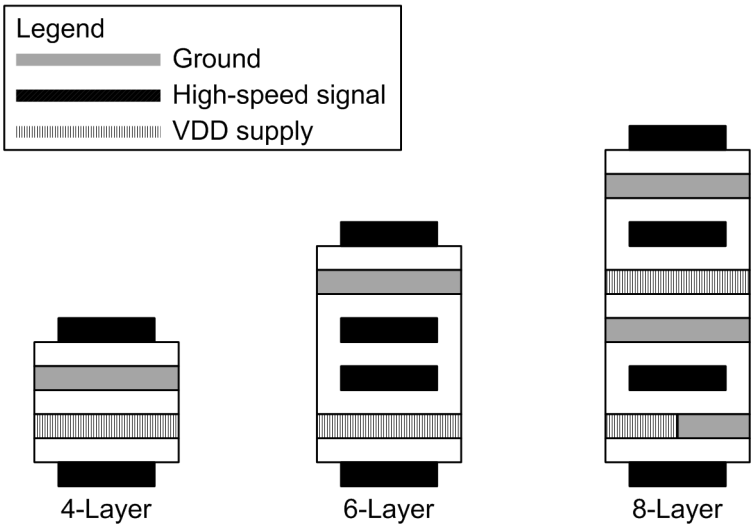

Figure 9-12. Recommended PCB Layer Stack-Up

9.4.2 Layout Example

There is an evaluation board references for the DP83TC814-Q1 . The DP83TC812EVM-MC is a media converter board which can be used for interoperability and bit error rate testing.

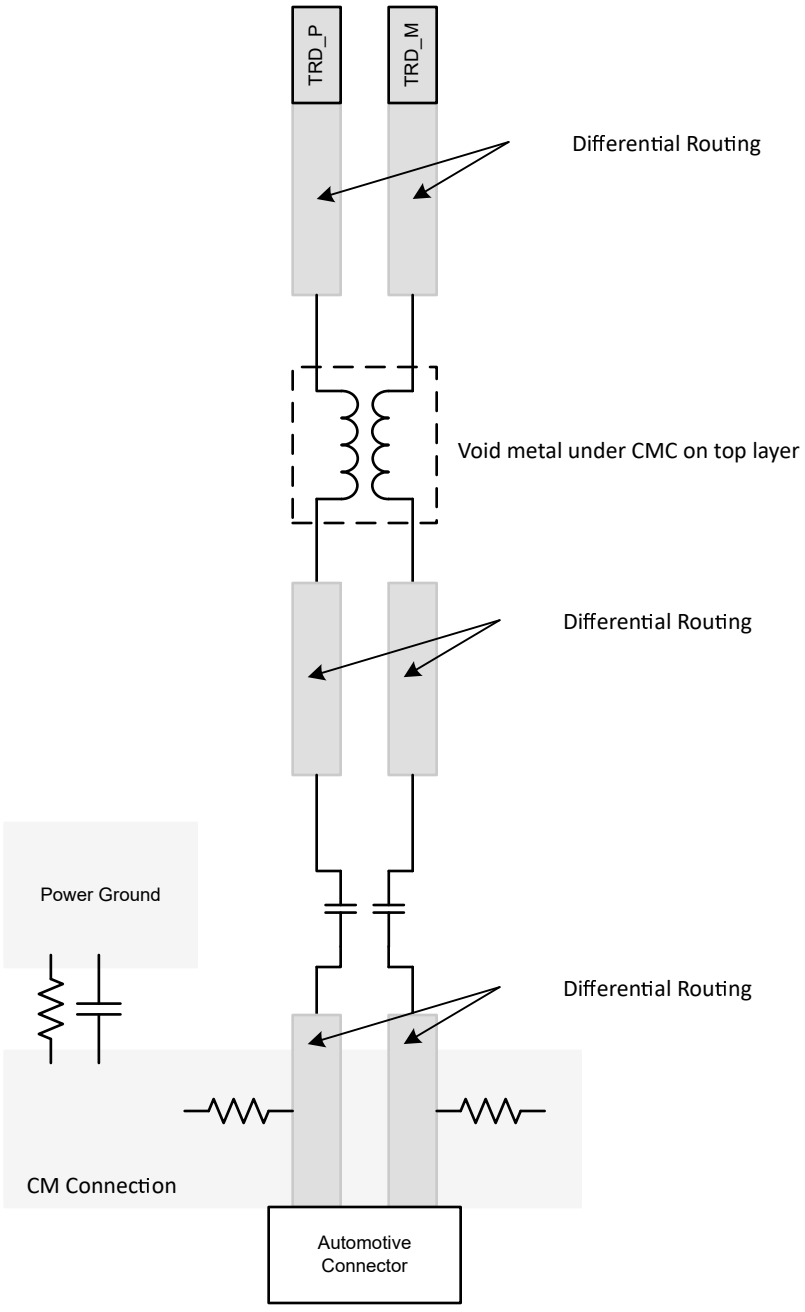

Figure 9-13. MDI Low-Pass Filter Layout Recommendation

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2021) to Revision A (December 2025)	Page
• Updated the CLKOUT frequency to be 50MHz in RMII Follower mode in the Pin Configuration and Functions section	4
• Added line to CLKOUT/GPIO2 description about which registers to program to disable switching in the *Pin Configuration and Functions* section	4
• Added line to INT pin description, "Reg 12-13 is recommended to be read only when INT_N is LOW", in the *Pin Configuration and Functions* section	4
• Added corrections for maximum clock rate in MDC description of the *Pin Functions* table	4
• Updated MDIO pin description to include link to Compliance Test Modes section in the *Pin Configuration and Functions* section	16
• Removed supply ramp delay offset for all supplies in the *Timing Requirements* section	16
• Updated Iozh to clarify mapping of Rx_Ctrl and Rx_ER pins in the *Electrical Characteristics* table	16
• Added corrections to the TDR description and deleted Register 0x310, Bit 8 in the *Time Domain Reflectometry* section	33
• Updated and corrected order of register writes for packet generation in the BIST and Loopback Modes section	35
• Clarified register reads for checking incoming data on the MAC side	37
• Added corrections to the RGMII Transmit Encoding table for Normal Data Transmission and Transmit Error Propagation	45
• Added corrections to the RGMII Transmit Encoding table for Normal Data Transmission and Transmit Error Propagation	47
• Added correction to note referring to SNLA389 Application Note	53

- Updated PHY Address Bootstraps: Binary values corrected to match hex settings 58
- Clarified and updated Bit Descriptions throughout the *Registers* 58
- Updated RMII Follower typical application diagram for correct XI configuration in the *Typical Applications* section 146
- Updated Typical Application (General) Diagram in the *Typical Applications* 146
- Updated RGMII Typical Application diagram to include 25MHz input..... 146

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83TC814RRHARQ1	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	814R
DP83TC814RRHARQ1.A	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	814R
DP83TC814RRHATQ1	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	814R
DP83TC814RRHATQ1.A	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	814R
DP83TC814SRHARQ1	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	814S
DP83TC814SRHARQ1.A	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	814S
DP83TC814SRHATQ1	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	814S
DP83TC814SRHATQ1.A	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	-	NIPDAU	Level-3-260C-168 HR	-40 to 125	814S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

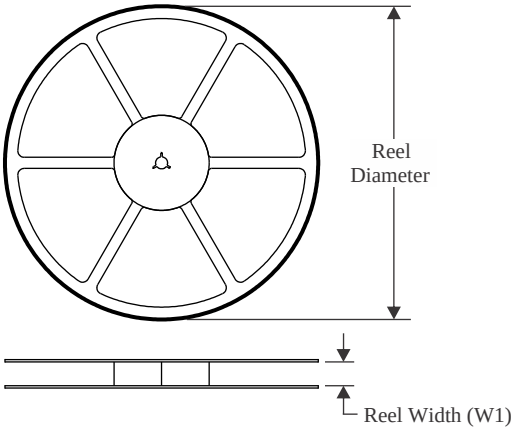
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

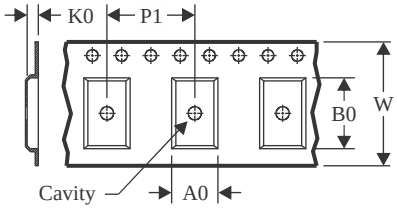
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

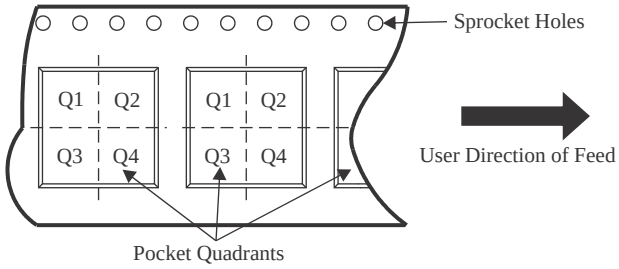


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

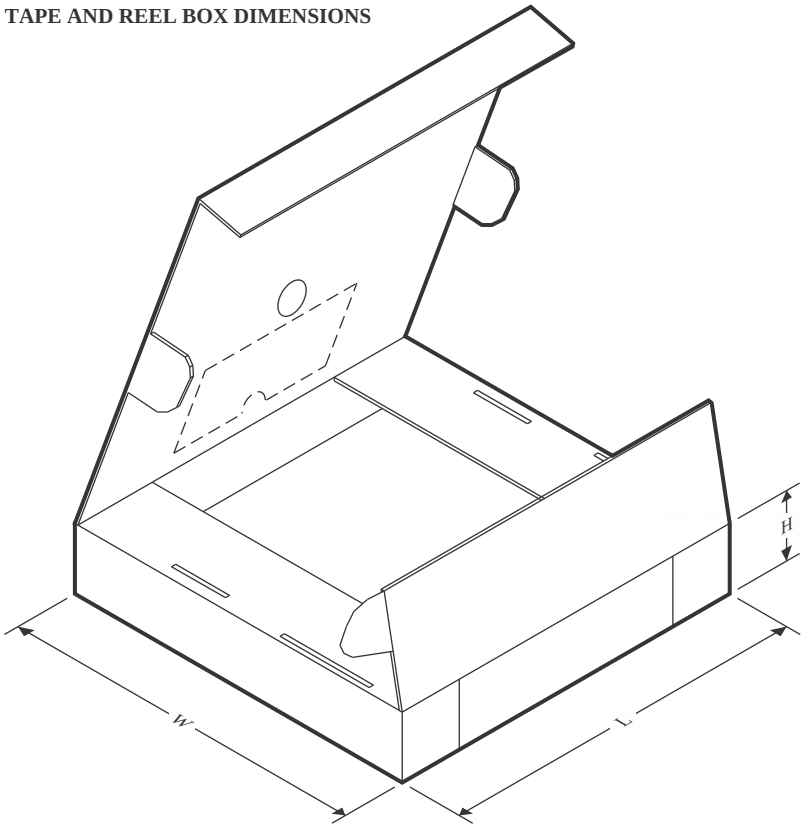
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83TC814RRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC814RRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC814SRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC814SRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83TC814RRHARQ1	VQFN	RHA	36	2500	367.0	367.0	35.0
DP83TC814RRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0
DP83TC814SRHARQ1	VQFN	RHA	36	2500	367.0	367.0	35.0
DP83TC814SRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

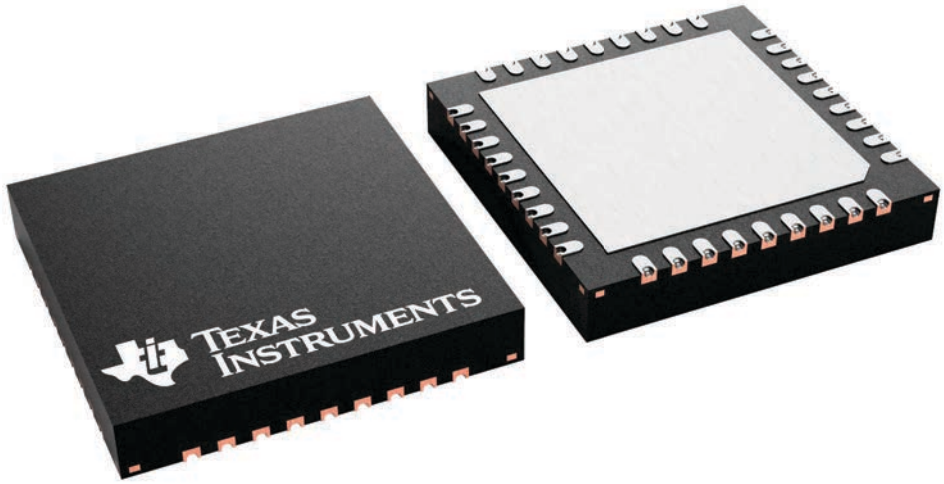
RHA 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



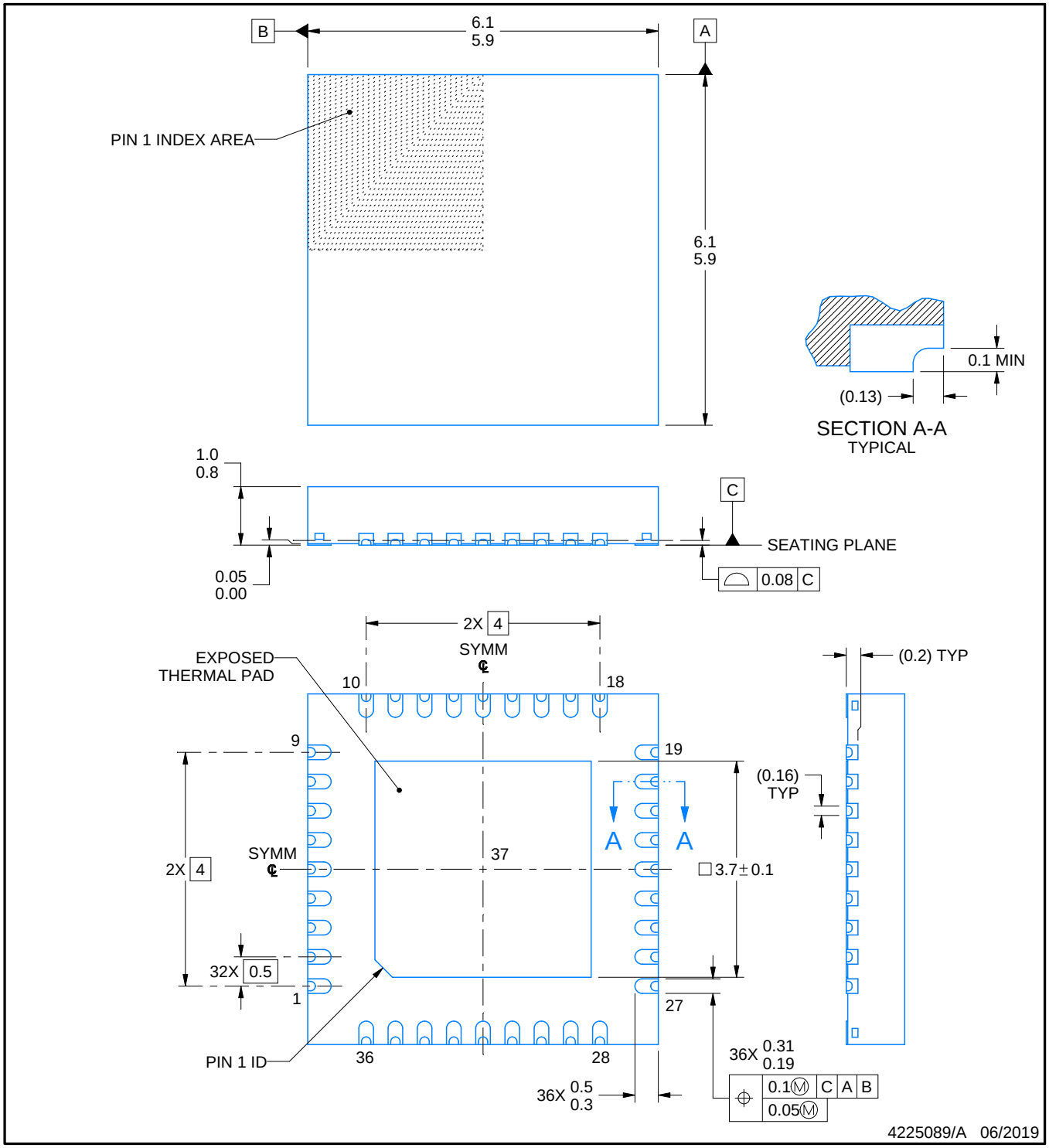
4228438/A

PACKAGE OUTLINE

RHA0036A

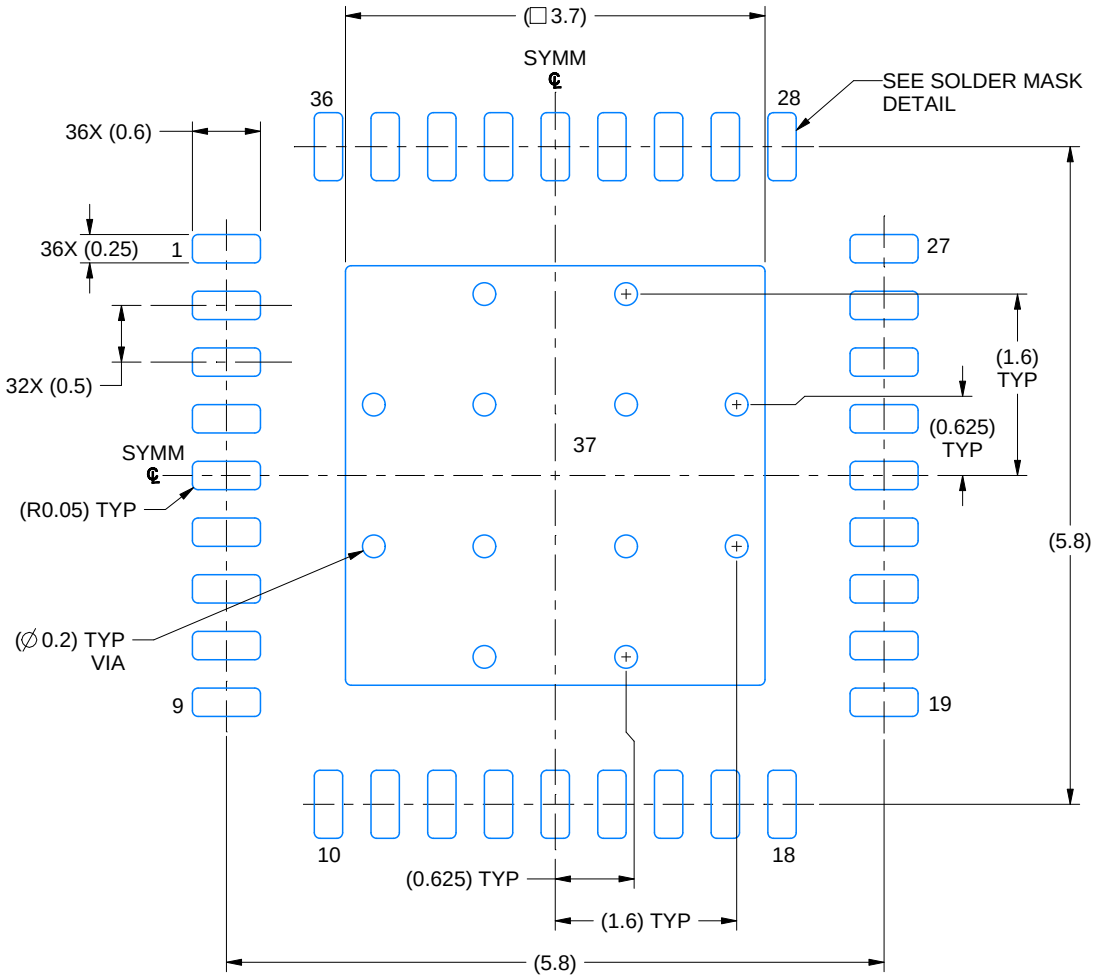
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

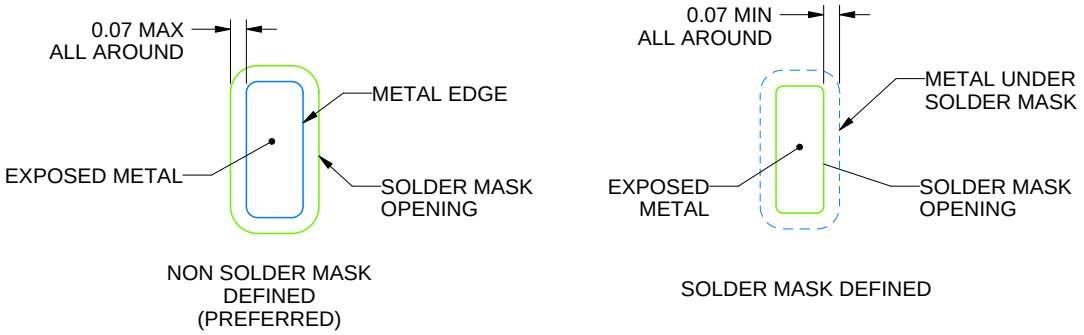


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

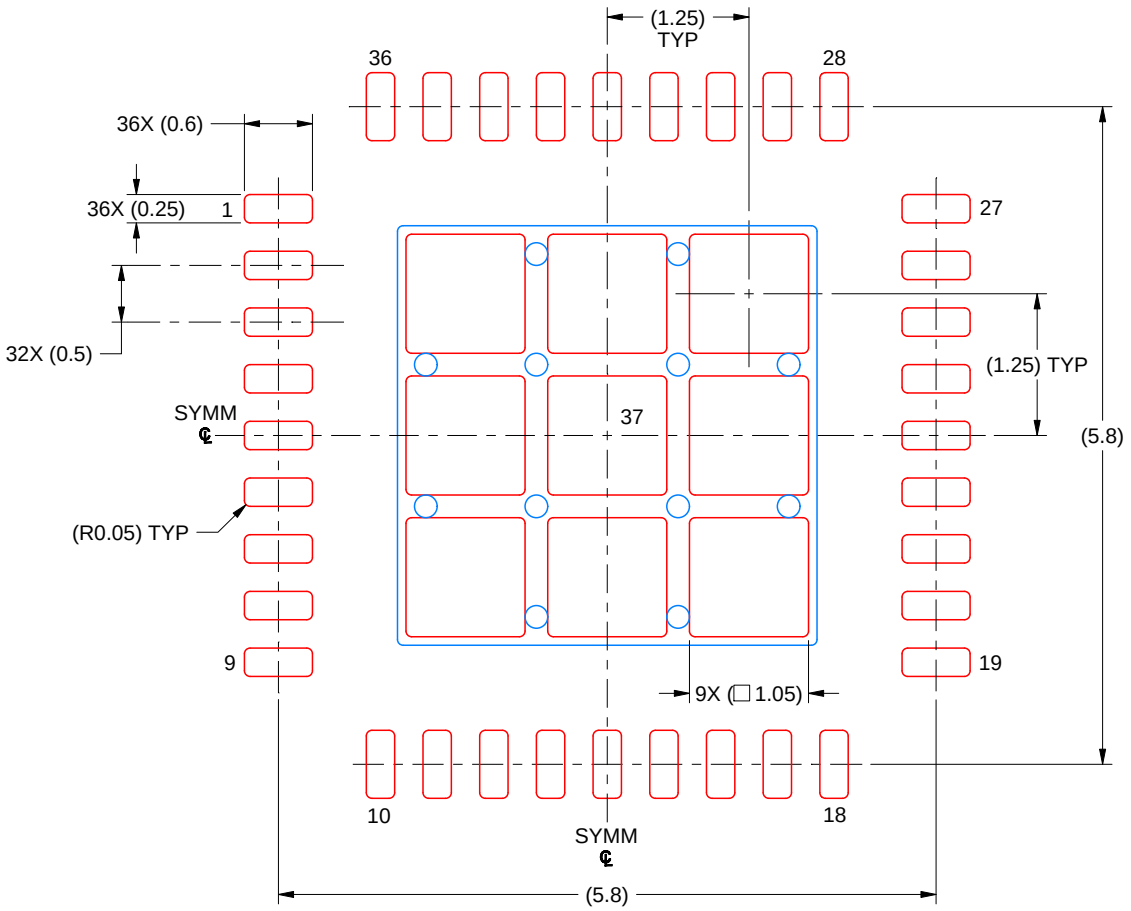


SOLDER MASK DETAILS

4225089/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225089/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025