DP83TC815-Q1 100Base-T1 Automotive Ethernet PHY Transceiver With IEEE802.1AS and TC10 Sleep-Wake

1 Features

- IEEE802.3bw compliant 100BASE-T1 PHY
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- IEEE 802.1AS time synchronization
  - Highly accurate 1pps signal
    - Synchronization jitter: < ±15ns (options to reduce to ±1ns)
    - Synchronization offset: < ±30ns
  - Multiple IOs for event capture and trigger
- OA TC-10 compliant sleep, wake up
- Robust EMC performance
  - IEC62228-5, OA EMC compliant
  - IEC61000-4-2 ESD level 4 MDI: ±8kV CD
  - SAE J2962-3 EMC compliant
  - 39dBm DPI immunity with ±5% asymmetry
  - < 4dBµV radiated emissions in GPS and glonass bands
  - Stripline emissions: class-II compliant
- MAC Interfaces: MII, RMII, RGMII, SGMII
- Footprint compatible with TI's 100BASE-T1, 1000BASE-T1 PHY - with BOM options
- 48V ready: VBAT transients to MDI up to +/– 70V
- Diagnostic tool kit
  - Signal quality indication (SQI) and time domain reflectometry (TDR)
  - Voltage, temperature, and ESD sensors
  - PPM monitor: provides external clock ppm drift (up to ±100ppb accuracy)
- Single 3.3V supply capability

2 Applications

- ADAS
  - Radar synchronization
- Body electronics and lighting
  - Body control module
  - Zone control module
- Telematics

3 Description

The DP83TC815-Q1 is an IEEE 802.3bw and Open Alliance (OA) compliant automotive qualified 100Base-T1 Ethernet physical layer transceiver. The device provides all physical layer functions needed to transmit and receive data over unshielded, shielded single twisted-pair cables with xMII interface flexibility.

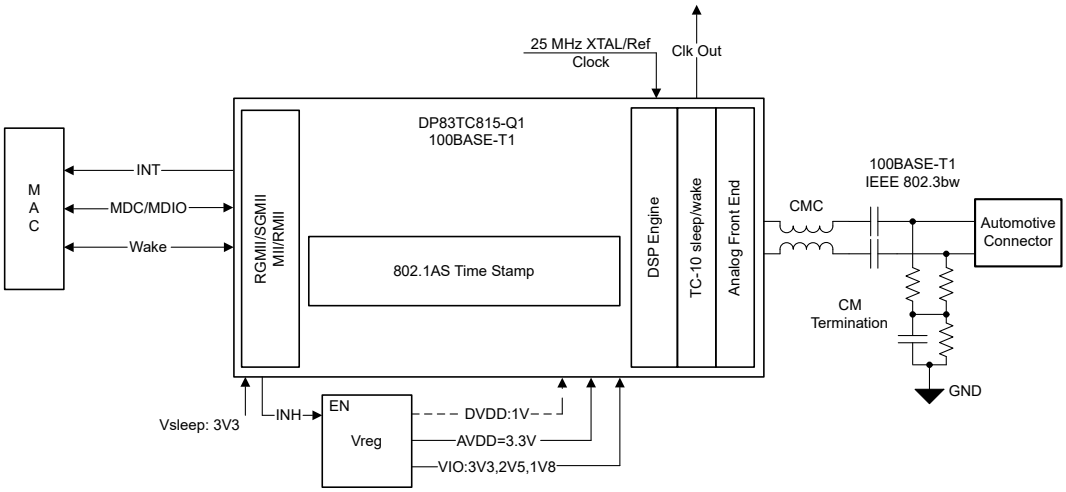
The DP83TC815-Q1 integrates IEEE802.1AS / IEEE1588v2 to enable highly accurate time synchronization and hardware time stamping for time-sensitive, real-time controlled applications.

The DP83TC815-Q1 supports OA TC-10 low power sleep feature with wake forwarding for reduced system power consumption when communication is not required.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DP83TC815-Q1	RHA (VQFN, 36)	6.00mm × 6.00mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematics

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4 Device Comparison Table

PART NUMBER	TC10?	MACsec?	802.1AS?	AVB CLOCKS?	FOOTPRINT COMPATIBLE?
DP83TC812x-Q1	Yes	No	No	No	Yes
DP83TC814x-Q1	No	No	No	No	Yes
DP83TC815-Q1	Yes	No	Yes	No	Yes
DP83TC816-Q1	Yes	No	Yes	Yes	Yes
DP83TC817S-Q1	Yes	Yes	Yes	No	Yes
DP83TC818S-Q1	Yes	Yes	Yes	Yes	Yes

5 Pin Configuration and Functions

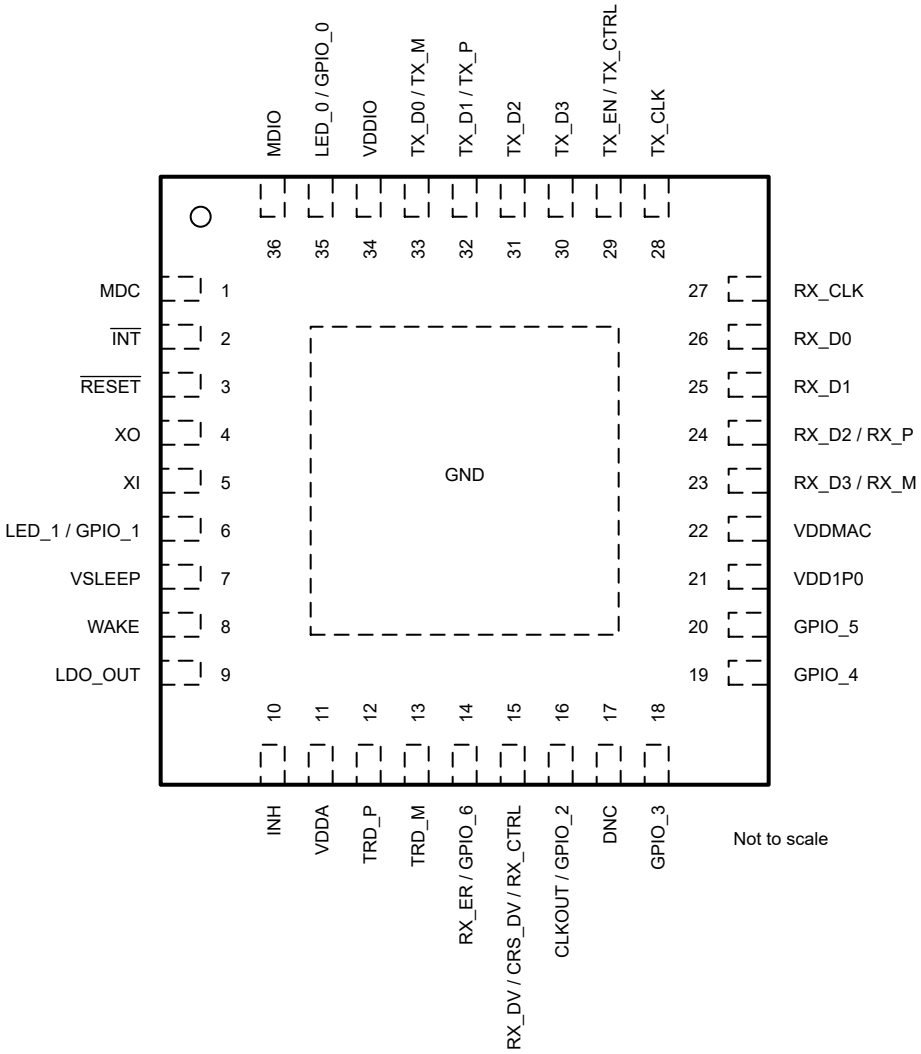


Figure 5-1. DP83TC815-Q1 RHA Package 36-Pin VQFN Top View

Table 5-1. Pin Functions

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
MAC INTERFACE			
RX_CLK	27	S, PD, O	**Receive Clock:** In MII and RGMII modes, the receive clock provides a 25MHz reference clock. **Unused in RMII and SGMII modes**
RX_D0	26	S, PD, O	**Receive Data:** Symbols received on the cable are decoded and transmitted out of these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A data nibble, RX_D[3:0], is transmitted in MII and RGMII modes. 2 bits; RX_D[1:0], are transmitted in RMII mode. If the PHY is bootstrapped to RMII Leader mode, a 50MHz clock reference is automatically outputted on RX_D3. This clock must be fed to the MAC. **RX_M / RX_P:** Differential SGMII Data Output. These pins transmit data from the PHY to the MAC.
RX_D1	25		
RX_D2 / RX_P	24		
RX_D3 / RX_M	23		
RX_DV / CRS_DV / RX_CTRL	15	S, PD, O	**Receive Data Valid:** This pin indicates when valid data is presented on RX_D[3:0] for MII mode. **Carrier Sense Data Valid:** This pin combines carrier sense and data valid into an asynchronous signal. When CRS_DV is asserted, data is presented on RX_D[1:0] in RMII mode. **RGMII Receive Control:** Receive control combines receive data valid indication and receive error indication into a single signal. RX_DV is presented on the rising edge of RX_CLK and RX_ER is presented on the falling edge of RX_CLK. **Unused in SGMII mode**
RX_ER / GPIO_6	14	S, PD, O	**Receive Error:** In MII and RMII modes, this pin indicates a receive error symbol has been detected within a received packet. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is **optional** in MII or RMII because the PHY automatically corrupts data on a receive error. **Unused in RGMII and SGMII modes** **This pin can be used as GPIO_6.**
TX_CLK	28	PD, I, O	**Transmit Clock:** In MII mode, the transmit clock is a 25MHz output (50 ohm Driver). In RGMII mode, this clock is sourced from the MAC layer to the PHY. A 25MHz clock must be provided in RGMII mode to meet the RGMII timing requirements mentioned in *Timing Requirements*. **Unused in RMII and SGMII modes**
TX_D0 / TX_M	33	PD, I	**Transmit Data:** In MII and RGMII modes, the transmit data nibble, TX_D[3:0], is received from the MAC prior to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] is received from the MAC prior to the rising edge of the reference clock. TX_D[3:2] are not used in RMII mode. **TX_M / TX_P:** Differential SGMII Data Input. These pins receive data that is transmitted from the MAC to the PHY.
TX_D1 / TX_P	32		
TX_D2	31		
TX_D3	33		
TX_EN / TX_CTRL	29	PD, I	**Transmit Enable:** In MII mode, transmit enable is presented prior to the rising edge of the transmit clock. TX_EN indicates the presence of valid data inputs on TX_D[3:0]. In RMII Leader mode, transmit enable is presented prior to the rising edge of RX_D3. TX_EN indicates the presence of valid data inputs on TX_D[1:0]. **RGMII Transmit Control:** Transmit control combines transmit enable and transmit error indication into a single signal. TX_EN is presented prior to the rising edge of TX_CLK; TX_ER is presented prior to the falling edge of TX_CLK. **Unused in SGMII mode**
SERIAL MANAGEMENT INTERFACE			
MDC	1	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input and output data. This clock can be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 20MHz. There is no minimum clock rate.
MDIO	36	OD, IO	**Management Data Input/Output:** Bidirectional management data signal that can be sourced by the management station or the PHY. This pin requires a pullup resistor. In systems with multiple PHYs using same MDIO-MDC bus, a single pull-up resistor must be used on MDIO line. Recommended to use a resistor between 2.2kΩ and 9kΩ. MDIO/MDC Access is required to pass Open Alliance Compliance. See Section 7.3.8.

Table 5-1. Pin Functions (continued)

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
CONTROL INTERFACE			
INH	10	O, OD	**INH:** Active-HIGH output. This pin is Hi-Z when the PHY is in TC-10 SLEEP. This pin is HIGH for all other PHY states. External pull down resistor in the range of 2kΩ - 10kΩ must be used when implementing TC-10 circuit. If multiple devices are sharing INH pin, then a single pull down resistor must be used.
$\overline{\text{INT}}$	2	PU, OD, IO	**Interrupt:** Active-LOW output, asserts LOW when an interrupt condition occurs. This pin has a weak internal pullup. Register access is necessary to enable various interrupt triggers. Once an interrupt event flag is set, register access is required to clear the interrupt event. This pin can be configured as an Active-HIGH output using register *0x0011*. Interrupt status from Reg 12-13 is recommended to be read only when INT_N is LOW. This pin can also operate as Power-Down control where asserting this pin low would put the PHY in power down mode and asserting high would put the PHY in normal mode. This feature can also be enabled through register *0x0011*.
$\overline{\text{RESET}}$	3	PU, I	**Reset:** Active-LOW input, which initializes or reinitializes the PHY. Asserting this pin LOW for at least 1µs forces a reset process to occur. All internal registers reinitialize to the default states as specified for each bit in the Register Maps section. All bootstrap pins are resampled upon deassertion of reset.
WAKE	8	PD, I/O	**WAKE:** Input/Output pin which is Active-HIGH input by default. As input, this pin wakes the PHY from TC-10 SLEEP. Asserting this pin HIGH at power-up brings the PHY out of SLEEP. External 10kΩ pull down resistor can be used when implementing TC-10 circuit to prevent accidental wake-up. This pin can be directly tied to VSLEEP or it can be pulled to VSLEEP through a resistor to wake the device. This pin also supports wake forwarding feature where a WAKE pulse generated by the PHY is then used to wake up other PHYs in the same system.
CLOCK INTERFACE			
XI	5	I	**Reference Clock Input (RMII):** Reference clock 25MHz crystal or oscillator in RMII Leader mode. **Reference Clock Input (Other MAC Interfaces):** Reference clock 25MHz crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only and XO left floating. This pin can also accept clock input from other devices like Ethernet MAC or another Ethernet PHY in daisy-chain operations. If using a crystal, connect a 100Ω resistor in series with the XI pin
XO	4	O	**Reference Clock Output:** XO pin is used for crystal only. This pin must be left floating when a CMOS-level oscillator is connected to XI.
LED/GPIO INTERFACE			
CLKOUT / GPIO_2	16	IO	**Clock Output:** 25MHz reference clock. This pin can also be used as LED or GPIO via Strap/Register selection. Program register<0x045F>=0x000F and register<0x0453>=0x0003 to disable switching on clkout pin
GPIO_3[3]	18	PD, IO	**General Purpose IO pins**
GPIO_4	19	S, PD, IO	
GPIO_5	20	PD, IO	
LED_0 / GPIO_0	35	S, PD, IO	**LED_0:** Link Status LED. This pin can also be used as LED or clock output through Register selection.
LED_1 / GPIO_1	6	S, PD, IO	**LED_1:** Link Status and BLINK for TX/RX Activity. This pin can also be used as LED or clock output via Strap/ Register selection.
MEDIUM DEPENDENT INTERFACE			
TRD_M	13	IO	**Differential Transmit and Receive:** Bidirectional differential signaling configured for 100BASE-T1 operation, IEEE 802.3bw compliant.
TRD_P	12		
POWER CONNECTIONS			
GND	GND	GROUND	**Ground:** This must always be connected to power ground.
LDO_OUT	9	SUPPLY	**1.0V LDO Out:** 1.0V Internal LDO Regulator Output 1.0V is generated internally from 3.3V VDDA Core supply. Connect to VDD1P0 (Pin 21) for Single Supply Mode. Leave floating for Dual Supply Mode

Table 5-1. Pin Functions (continued)

PIN		STATE[1]	DESCRIPTION
NAME[2]	NO.		
VDD1P0	21	SUPPLY	**VDD1P0 Supply:** 1.0V Connect to LDO_OUT (Pin 9) for Single Supply Mode. Connect to external regulator for Dual Supply Mode. In Dual Supply Mode, recommend using ferrite bead and 2.2µF and 0.1µF ceramic decoupling capacitors.
VDDA	11	SUPPLY	**Core Supply:** 3.3V Recommend using 0.47µF and 0.01µF ceramic decoupling capacitors; optional ferrite bead can be used.
VDDIO	34	SUPPLY	**IO Supply:** 1.8V, 2.5V, or 3.3V Recommend using ferrite bead, 0.47µF and 0.01µF ceramic decoupling capacitors.
VDDMAC	22	SUPPLY	**Optional MAC Interface Supply:** 1.8V, 2.5V, or 3.3V Optional separate supply for MAC interface pins. This pin supplies power to the MAC interface pins and can be kept at a different voltage level as compared to other IO pins. Recommend using 0.47µF, and 0.01µF ceramic decoupling capacitors and ferrite bead. When separate VDDMAC is not required in the system then it must be connected to VDDIO. When connecting to VDDIO, 0.47µF on the VDDIO can be removed. 0.47µF must still be connected close to VDDMAC. In this case, one common ferrite bead can be used between VDDIO and VDDMAC.
VSLEEP	7	SUPPLY	**VSLEEP Supply:** 3.3V Recommend using 0.1µF ceramic decoupling capacitors.
DO NOT CONNECT			
DNC	17	–	**DNC:** Do not connect (leave floating)

(1) Pin Type:
I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup
S = Bootstrap configuration pin (all configuration pins have weak internal pullups or pulldowns)

(2) When pins are unused, follow the recommended connection requirements provided in the table above. If pins do not have required termination, the pins can be left floating.

(3) Do not drive the GPIO_3 HIGH before power-up.

5.1 Pin Power Domain

Table 5-2. Pin Domain

PIN NO	PIN NAME	VOLTAGE DOMAIN
1	MDC	VDDIO
2	INT_N	VDDIO
3	RESET_N	VDDIO
4	XO	VDDIO
5	XI	VDDIO
6	LED_1/GPIO_1	VDDIO
8	WAKE	VSLEEP
10	INH	VSLEEP
12	TRD_P	VDDA
13	TRD_M	VDDA
14	RX_ER / GPIO_6	VDDMAC
15	RX_DV/CRS_DV/RX_CTRL	VDDMAC
16	CLKOUT/GPIO_2	VDDMAC
18	GPIO_3	VDDMAC
19	GPIO_4	VDDMAC
20	GPIO_5	VDDMAC
23	RX_D3/RX_M	VDDMAC
24	RX_D2/RX_P	VDDMAC
25	RX_D1	VDDMAC
26	RX_D0	VDDMAC
27	RX_CLK	VDDMAC
28	TX_CLK	VDDMAC
29	TX_EN/TX_CTRL	VDDMAC
30	TX_D3	VDDMAC
31	TX_D2	VDDMAC
32	TX_D1/TX_P	VDDMAC
33	TX_D0/TX_M	VDDMAC
35	LED_0/GPIO_0	VDDIO
36	MDIO	VDDIO

5.2 Pin States

Table 5-3. Pin States - POWER-UP / RESET

PIN NO	PIN NAME	POWER-UP / RESET		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1	I	PD	9
7	VSLEEP	SUPPLY	none	none
8	WAKE	I/O	PD	455
9	LDO_OUT	O	none	none
10	INH	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT	O	none	none
17	DNC	FLOAT	none	none
18	GPIO_3	I	PD	9
19	GPIO_4	I	PD	9
20	GPIO_5	I	PD	9
21	VDD1P0	SUPPLY	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	I	PD	9
24	RX_D2	I	PD	9
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	I	PD	9
36	MDIO	OD, IO	none	none

Table 5-4. Pin States - TC10 SLEEP

PIN NO	PIN NAME	TC10 SLEEP (All Supplies On)		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1 (1)	I	PD	9
7	VSLEEP	SUPPLY	none	none
8	WAKE	I/O	PD	455
9	LDO_OUT	O	none	none
10	INH	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT (2)	O	none	none
17	DNC	FLOAT	none	none
18	GPIO_3	I	PD	9
19	GPIO_4	I	PD	9
20	GPIO_5	I	PD	9
21	VDD1P0	SUPPLY	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	I	PD	9
24	RX_D2	I	PD	9
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	I	PD	9
36	MDIO	OD, IO	none	none

(1) If LED_1 is configured as CLKOUT, the TC10 Sleep IO state becomes: Output with no pull resistors
(2) If CLKOUT is configured as LED_1, the TC10 Sleep IO state becomes: Input, 9kΩ pull down

Table 5-5. Pin States - MAC ISOLATE and IEEE PWDN

PIN NO	PIN NAME	MAC ISOLATE			IEEE PWDN		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VSLEEP	SUPPLY	none	none	SUPPLY	none	none
8	WAKE	IO	PD	455	IO	PD	455
9	LDO_OUT	O	none	none	O	none	none
10	INH	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	I	PD	6	I	PD	6
15	RX_DV	I	PD	6	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	DNC	FLOAT	none	none	FLOAT	none	none
18	GPIO_3	I	PD	9	I	PD	9
19	GPIO_4	I	PD	9	I	PD	9
20	GPIO_5	I	PD	9	I	PD	9
21	VDD1P0	SUPPLY	none	none	SUPPLY	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	I	PD	9	O	none	none
24	RX_D2	I	PD	9	O	none	none
25	RX_D1	I	PD	9	O	none	none
26	RX_D0	I	PD	9	O	none	none
27	RX_CLK	I	PD	9	O	none	none
28	TX_CLK	I	PD	9	I	none	none
29	TX_EN	I	PD	9	I	none	none
30	TX_D3	I	PD	9	I	none	none
31	TX_D2	I	PD	9	I	none	none
32	TX_D1	I	PD	9	I	none	none
33	TX_D0	I	PD	9	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

Table 5-6. Pin States - MII and RGMII

PIN NO	PIN NAME	MII			RGMII		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)	PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9	I	PU	9
4	XO	O	none	none	O	none	none
5	XI	I	none	none	I	none	none
6	LED_1	O	none	none	O	none	none
7	VSLEEP	SUPPLY	none	none	SUPPLY	none	none
8	WAKE	IO	PD	455	IO	PD	455
9	LDO_OUT	O	none	none	O	none	none
10	INH	OD, O	none	none	OD, O	none	none
11	VDDA	SUPPLY	none	none	SUPPLY	none	none
12	TRD_P	IO	none	none	IO	none	none
13	TRD_M	IO	none	none	IO	none	none
14	RX_ER	O	none	none	I	PD	6
15	RX_DV	O	none	none	O	none	none
16	CLKOUT	O	none	none	O	none	none
17	DNC	FLOAT	none	none	FLOAT	none	none
18	GPIO_3	I	PD	9	I	PD	9
19	GPIO_4	I	PD	9	I	PD	9
20	GPIO_5	I	PD	9	I	PD	9
21	VDD1P0	SUPPLY	none	none	SUPPLY	none	none
22	VDDMAC	SUPPLY	none	none	SUPPLY	none	none
23	RX_D3	O	none	none	O	none	none
24	RX_D2	O	none	none	O	none	none
25	RX_D1	O	none	none	O	none	none
26	RX_D0	O	none	none	O	none	none
27	RX_CLK	O	none	none	O	none	none
28	TX_CLK	O	none	none	I	none	none
29	TX_EN	I	none	none	I	none	none
30	TX_D3	I	none	none	I	none	none
31	TX_D2	I	none	none	I	none	none
32	TX_D1	I	none	none	I	none	none
33	TX_D0	I	none	none	I	none	none
34	VDDIO	SUPPLY	none	none	SUPPLY	none	none
35	LED_0	O	none	none	O	none	none
36	MDIO	OD, IO	none	none	OD, IO	none	none

Table 5-7. Pin States - SGMII

PIN NO	PIN NAME	SGMII		
		PIN STATE (1)	PULL TYPE	PULL VALUE (kΩ)
1	MDC	I	none	none
2	$\overline{\text{INT}}$	OD, O	PU	9
3	$\overline{\text{RESET}}$	I	PU	9
4	XO	O	none	none
5	XI	I	none	none
6	LED_1	O	none	none
7	VSLEEP	SUPPLY	none	none
8	WAKE	IO	PD	455
9	LDO_OUT	O	none	none
10	INH	OD, O	none	none
11	VDDA	SUPPLY	none	none
12	TRD_P	IO	none	none
13	TRD_M	IO	none	none
14	RX_ER	I	PD	6
15	RX_DV	I	PD	6
16	CLKOUT	O	none	none
17	DNC	FLOAT	none	none
18	GPIO_3	I	PD	9
19	GPIO_4	I	PD	9
20	GPIO_5	I	PD	9
21	VDD1P0	SUPPLY	none	none
22	VDDMAC	SUPPLY	none	none
23	RX_D3	O	none	none
24	RX_D2	O	none	none
25	RX_D1	I	PD	9
26	RX_D0	I	PD	9
27	RX_CLK	I	PD	9
28	TX_CLK	I	none	none
29	TX_EN	I	none	none
30	TX_D3	I	none	none
31	TX_D2	I	none	none
32	TX_D1	I	none	none
33	TX_D0	I	none	none
34	VDDIO	SUPPLY	none	none
35	LED_0	O	none	none
36	MDIO	OD, IO	none	none

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup

5.3 Pin Multiplexing

Following table provides details of the different functions available on GPIO pins.

LED: Pin configured as LED indication.

CLKOUT: Pin configured as a clock output signal

Event Triggers/Capture: Pin configured to capture and trigger 802.1AS Time stamp generated events

PTP Interrupt: Pin configured to output 802.1AS/PTP specific interrupts

50/25MHz PTP Input: 50/25MHz Reference Clock for PTP

Sync Clock: Programmable Frequency Clock synchronous to PTP wall clock

PPM Monitor: Pin configured for external clock input to monitor PPM w.r.t internal clocks

Table 5-8. Pin Multiplexing

FIELD	PIN	Default	LED	CLKOUT 25MHz	Event Trigger / Capture
LED_0 / GPIO_0	35	LED_0	Yes		Yes
LED_1 / GPIO_1	6	LED_1	Yes	Yes	Yes
CLKOUT / GPIO_2	16	CLKOUT	Yes	Yes	Yes
GPIO_3	18	GPIO_3			Yes
GPIO_4	19	GPIO_4			Yes
GPIO_5	20	GPIO_5			Yes
RX_ER / GPIO_6	14	RX_ER			Yes

Table 5-9. Pin Multiplexing - PTP, Interrupts

FIELD	PIN	50/25MHz PTP Input	PTP Sync Clock	PTP Interrupt
LED_0 / GPIO_0	35	Yes		Yes
LED_1 / GPIO_1	6			Yes
CLKOUT / GPIO_2	16		Yes	Yes
GPIO_3	18		Yes	Yes
GPIO_4	19		Yes	Yes
GPIO_5	20	Yes		Yes
RX_ER / GPIO_6	14			Yes

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	TYP	MAX	UNIT
Input Voltage	VDDA	–0.3		4	V
Input Voltage	VDD1P0	–0.3		1.4	V
Input Voltage	VDDIO (3.3V)	–0.3		4	V
Input Voltage	VDDIO(2.5V)	–0.3		4	V
Input Voltage	VDDIO(1.8V)	–0.3		4	V
Input Voltage	VSLEEP	-0.3		4	V
Pins	MDI (TRD_M, TRD_P)	–0.3		4	V
Input Voltage	MDC, RESET, XI, LED_1, RX_ER, RX_CTRL, CLKOUT, RX_D[3:0], TX_CLK, TX_CTRL, TX_D[3:0], LED_0, MDIO, GPIO	–0.3		VDDIO + 0.3	V
Pins	MDIO, MDC, GPIO, XI, XO, INT, RESET, CLKOUT	–0.3		VDDIO + 0.3	V
Output Voltage	INH	–0.3		VSLEEP + 0.3	V
Input Voltage	WAKE	–0.3		VSLEEP + 0.3	V
Output Voltage	INT, LED_1, RX_CTRL, CLKOUT, RX_D[3:0], RX_CLK, LED_0, MDIO, GPIO	–0.3		4	V
T_J	Junction temperature	-40		150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
			TRD_N, TRD_P pins	±8000	
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
		IEC 61000-4-2 contact discharge	TRD_N, TRD_P pins	±8000	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIO / VDDMAC	IO Supply Voltage, 1.8V operation	1.665	1.8	1.935	V
	IO Supply Voltage, 2.5V operation	2.3125	2.5	2.6875	
	IO Supply Voltage, 3.3V operation	3.0525	3.3	3.5475	
VDDA	Core Supply Voltage, 3.3V	2.97	3.3	3.63	V
VDD1P0	Core Digital External Supply 1V	0.95	1.0	1.1	V
VSLEEP	Sleep Supply Voltage, 3.3V	2.97	3.3	3.63	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		RHA (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
100BASE-T1 PMA CONFORMANCE						
V_{OD-MDI}	Output Differential Voltage	$R_{L(diff)}$ = 100Ω			2.2	V
$R_{MDI-Diff}$	Integrated Differential Output Termination	TRD_P and TRD_M		100		Ω
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±7.5%, 2-level strap	0		0.8	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±7.5%, 2-level strap	2		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±7.5%, 2-level strap	0		0.7	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±7.5%, 2-level strap	1.7		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±7.5%, 2-level strap	0		0.35 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±7.5%, 2-level strap	0.65 x VDDIO		VDDIO	V
BOOTSTRAP DC CHARACTERISTICS (3 Level)						
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 3.3V ±7.5%, 3-level strap	0		0.18 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 3.3V ±7.5%, 3-level strap	0.22 x VDDIO		0.42 x VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 3.3V ±7.5%, 3-level strap	0.46 x VDDIO		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 2.5V ±7.5%, 3-level strap	0		0.25 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 2.5V ±7.5%, 3-level strap	0.29 x VDDIO		0.56 x VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 2.5V ±7.5%, 3-level strap	0.65 x VDDIO		VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range	VDDIO = 1.8V ±7.5%, 3-level strap	0		0.35 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range	VDDIO = 1.8V ±7.5%, 3-level strap	0.40 x VDDIO		0.75 x VDDIO	V

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{MODE3}	Mode 3 Strap Voltage Range	VDDIO = 1.8V ±7.5%, 3-level strap	0.84 x VDDIO		VDDIO	V
IO CHARACTERISTICS						
V_{IH}	High Level Input Voltage	VDDIO = 3.3V ±7.5%	2			V
V_{IL}	Low Level Input Voltage	VDDIO = 3.3V ±7.5%			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±7.5%	2.4			V
V_{OL}	Low Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±7.5%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 2.5V ±7.5%	1.7			V
V_{IL}	Low Level Input Voltage	VDDIO = 2.5V ±7.5%			0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ±7.5%	2			V
V_{OL}	Low Level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ±7.5%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 1.8V ±7.5%	0.65*VDDIO			V
V_{IL}	Low Level Input Voltage	VDDIO = 1.8V ±7.5%			0.35*VDDIO	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±7.5%	VDDIO-0.45			V
V_{OL}	Low Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±7.5%			0.45	V
I_{IH}	Input High Current(1)	VIN = VDDIO, All pins except XI and WAKE	-10		10	µA
I_{IH-XI}	Input High Current(1)	VIN = VDDIO, XI pin	-15		15	µA
I_{IL-XI}	Input Low Current(1)	VIN = GND, XI pin	-15		15	µA
I_{IL}	Input Low Current(1)	VIN = GND, All pins except XI, RESET_N pins	-10		10	µA
I_{IL-RST}	Input Low Current	VIN = GND, $\overline{\text{RESET}}$ pin	-500		0	µA
Iozh	Tri-state Output High Current(2)	VIN = VDDIO, All pins except RX_CTRL and RX_ER	-10		10	µA
Iozh	Tri-state Output High Current(2)	VIN = VDDIO, RX_CTRL and RX_ER	-52		52	µA
Iozl	Tri-state Output Low Current(2)	VOUT = GND	-10		10	µA
R_{pulldn}	Internal Pull Down Resistor	RX_D[3:0], RX_CLK, LED_0, LED_1, TX_CTRL	6.2	8.4	10.7	kΩ
R_{pulldn}	Internal Pull Down Resistor	RX_CTRL, RX_ER	4.725	5.8	7.2	kΩ
R_{pulldn}	Internal Pull Down Resistor	WAKE	320	455	590	kΩ
R_{pullup}	Internal Pull Up Resistor	INT, RESET	6.3	9	11.2	kΩ
XI V_{IH}	High Level Input Voltage		1.3		VDDIO	V
XI V_{IL}	Low Level Input Voltage				0.5	V
C_{IN}	Input Capacitance XI			1		pF

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance INPUT PINS			5		pF
C_{OUT}	Output Capacitance XO			1		pF
C_{OUT}	Output Capacitance OUTPUT PINS			5		pF
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK	35	50	65	Ω
Power Consumption VDDIO						
I(VDDIO=3.3V)	MII			20	25	mA
	RMII			19	25	mA
	RGMII			17	23	mA
	SGMII			10	14	mA
I(VDDIO=2.5V)	MII			14	18	mA
	RMII			13	18	mA
	RGMII			12	16	mA
	SGMII			6	9	mA
I(VDDIO=1.8V)	MII			10	13	mA
	RMII			9	13	mA
	RGMII			8	12	mA
	SGMII			4	6	mA
I(VDDIO=3.3V)	MII	802.1AS enabled		22	28	mA
	RMII			23	28	mA
	RGMII			20	28	mA
	SGMII			13	22	mA
I(VDDIO=2.5V)	MII			16	22	mA
	RMII			15	21	mA
	RGMII			14	19	mA
	SGMII			8	15	mA
I(VDDIO=1.8V)	MII			11	17	mA
	RMII			11	17	mA
	RGMII			8	17	mA
	SGMII			6	12	mA
Power Consumption : Core Supplies						
Single Supply: I(3V3)	xMII			71	172	mA
	SGMII			91	193	mA
Dual External Supply: I(3V3)	xMII			48	70	mA
	SGMII			68	91	mA
Dual External Supply: I(1V0)	xMII			23	102	mA
	SGMII			23	102	mA
Power Consumption : Core Supplies, 802.1AS enabled						

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Single Supply: I(3V3)	xMII	Sync Interval = 125ms		87	194	mA
	SGMII			107	215	mA
Dual External Supply: I(3V3)	xMII			60	83	mA
Dual External Supply: I(1V0)	xMII			27	111	mA
Dual External Supply: I(3V3)	SGMII			80	104	mA
Dual External Supply: I(1V0)	SGMII			27	111	mA
Power Consumption: Low Power Modes						
I(VDDA3V3)	RESET	Single supply		17	103	mA
I(VDDA3V3)		Dual supply		9	21	mA
I(DVDD1P0)		Dual supply		8	82	mA
I(VDDIO=3.3V)		VDDIO = VDDMAC		12	18	mA
I(VDDIO=2.5V)				8.5	14	mA
I(VDDIO=1.8V)				6	10	mA
I(VDDA3V3)	IEEE Power Down	Single supply		15	98	mA
I(VDDA3V3)		Dual supply		10	21	mA
I(VDDD1P0)		Dual supply		5	77	mA
I(VDDIO=3.3V)		VDDIO = VDDMAC		12	18	mA
I(VDDIO=1.8V)				8	11	mA
I(VDDIO=2.5V)				8	14	mA
I(VDDA3V3)	Standby	Single supply		31	119	mA
I(VDDA3V3)		Dual supply		22	37	mA
I(DVDD1P0)		Dual supply		9	82	mA
I(VDDIO=3.3V)		xMII, VDDIO = VDDMAC		15	22	mA
		SGMII, VDDIO = VDDMAC		12	15	mA
I(VDDIO=2.5V)		xMII, VDDIO = VDDMAC		11	16	mA
		SGMII, VDDIO = VDDMAC		8	13	mA
I(VDDIO=1.8V)		xMII, VDDIO = VDDMAC		8	13	mA
		SGMII, VDDIO = VDDMAC		6	8	mA
I(VSLEEP)	TC-10 Sleep	All other supplies are off		7	18	µA
		All other supplies are off, Fast Wake-up mode enabled		25	50	µA
I(VDDIO=3.3V)	TC-10 Sleep, supplies on	VDDIO = VDDMAC		12	16	mA
I(VDDIO=2.5V)				8.5	12	mA
I(VDDIO=1.8V)				6	9	mA
I(VDDA3V3)		Single supply		35	132	mA
I(VDDA3V3)		Dual Supply		28	50	mA
I(VDDD1P0)		Dual Supply		7	82	mA
SGMII Input						
V_{IDTH}	Input differential voltage tolerance	SI_P and SI_N, AC coupled	0.1			V
$R_{IN-DIFF}$	Receiver differential input impedance (DC)		80		120	ohm

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SGMII Output						
	Clock signal duty cycle	SO_P and SO_N, AC coupled, 0101010101 pattern	48		52	%
	Output Differential Voltage	SO_P and SO_N, AC coupled	150		400	mV
Voltage Sensor						
VDDA	VDDA Sensor Range		2.7	3.3	4	V
	VDDA Sensor Resolution (LSB)			8.8		mV
	VDDA Sensor Accuracy	Voltage and temperature variation on single part	-150		150	mV
	VDDA Sensor Accuracy	Part-part variation	-100		100	mV
VDDIO / VDDMAC	VDDIO / VDDMAC Sensor Range		1.44		3.9	V
	VDDIO / VDDMAC Sensor Resolution (LSB)			16		mV
	VDDIO / VDDMAC Sensor Accuracy	Voltage and temperature variation on single part	-200		200	mV
	VDDIO / VDDMAC Sensor Accuracy	Part-part variation	-100		100	mV
VSLEEP	VSLEEP Sensor Range	Part-part and VT variation	2.7	3.3	4	V
	VSLEEP Sensor Resolution (LSB)			8.8		mV
	VSLEEP Sensor Accuracy	Voltage and temperature variation on single part	-150		150	mV
	VSLEEP Sensor Accuracy	Part-part variation	-100		100	mV
VDD1P0	VDD1P0 Sensor Range		0.9	1	1.2	V
	VDD1P0 Sensor Resolution (LSB)			2.7		mV
	VDD1P0 Sensor Accuracy	With room temp offset callibration on each part	-60		60	mV
	VDD1P0 Sensor Accuracy	Part-to-part	-40		40	mV
Temperature Sensor						
Temp	Temp Sensor Range		-40		150	℃
Temp	Temp Sensor Resolution (LSB)			1.1		℃

(1) For pins: MDC, TX_CLK, TX_CTRL, TX_D[3:0], and RESET_N
(2) For pins: RX_D[3:0], RX_CLK, RX_CTRL, MDIO, INT_N, and XO.

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
MII TIMING						
T1.1	TX_CLK High / Low Time		16	20	24	ns
T1.2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK		10			ns
T1.3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK		0			ns
T2.1	RX_CLK High / Low Time		16	20	24	ns
T2.2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising		10		30	ns
RMII LEADER TIMING						
T3.1	RMII Leader Clock Period			20		ns
	RMII Leader Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to RMII Leader Clock		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from RMII Leader Clock		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from RMII Leader Clock rising edge		4	10	14	ns
RMII FOLLOWER TIMING						
T3.1	Input Reference Clock Period			20		ns
	Reference Clock Duty Cycle		35		65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to XI Clock rising		4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from XI Clock rising		2			ns
T3.4	RX_D[1:0], RX_ER, CRS_DV Delay from XI Clock rising		4		14	ns
RGMII INPUT TIMING						
T_{cyc}	Clock Cycle Duration	TX_CLK	36	40	44	ns
$T_{setup(align)}$	TX_D[3:0], TX_CTRL Setup to TX_CLK (Align Mode)		1	2		ns
$T_{hold(align)}$	TX_D[3:0], TX_CTRL Hold from TX_CLK (Align Mode)		1	2		ns
RGMII OUTPUT TIMING						
$T_{skew(align)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Align Mode Enabled)	On PHY Pins	-1.2		1.2	ns
$T_{setup(shift)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled, default)	On PHY Pins	2			ns
T_{cyc}	Clock Cycle Duration	RX_CLK	36	40	44	ns
Duty_G	Duty Cycle	RX_CLK	45	50	55	%
SMI TIMING						
T4.1	MDC to MDIO (Output) Delay Time	25pF load capacitance	0		40	ns
T4.2	MDIO (Input) to MDC Setup Time		10			ns
T4.3	MDIO (Input) to MDC Hold Time		10			ns
	MDC Frequency			2.5	20	MHz
POWER-UP TIMING						
T5.1	Supply ramp time: AVDD, DVDD, VDDIO (1)		0.2		8	ms
T5.1	Supply ramp time: Vsleep (1)		0.4		8	ms
T5.2	Supply ramp delay offset: For all supplies				10	ms
T5.3	XTAL Startup / Settling: Powerup to XI good/stabilized			1.5		ms
T5.4	Oscillator stabilization time from power up				10	ms
	Last Supply power up, stable Clock To Reset Release				10	ms

6.6 Timing Requirements (continued)

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
T5.5	Post power-up to SMI ready: Post Power-up wait time required before MDC preamble can be sent for register access		10			ms
T5.6	Power-up to Strap latch-in				10	ms
T5.7	CLKOUT Startup/Settling: Powerup to CLKOUT good/stabilized				10	ms
T5.8	Power-up to idle stream				10	ms
RESET TIMING (RESET_N)						
T6.1	Reset Pulse Width: Miminum Reset pulse width to be able to reset		100			µs
T6.2	Reset to SMI ready: Post reset wait time required before MDC preamble can be sent for register access		1			ms
T6.3	Reset to Strap latch-in: Hardware configuration pins transition to output drivers			80		µs
T6.4	Reset to idle stream				1800	µs
WAKE REQUEST AND WAKE PULSE TIMING						
T7.1	Local Wake-Up Pulse Duration		40			µs
T7.2	Local Wake-Up to INH Transition				40	µs
T7.3	Energy-detect-based Wake-Up Pulse Duration				0.7	ms
T7.4	Energy-detect-based Wake-Up to INH Transition				0.7	ms
T7.5	Energy-detect-based Wake-Up to WAKE forwarding pulse				1.4	ms
TRANSMIT LATENCY TIMING						
	MII Rising edge TX_CLK with assertion TX_EN to SSD symbol on MD		190		275	ns
	MII Rising edge TX_CLK with assertion TX_EN to SSD symbol on MD	with PTP enabled	170		275	ns
	Follower RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI		350		473	ns
	Leader RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI		340		462	ns
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI		340		493	ns
	First symbol of SGMII to SSD symbol on MDI		375		505	ns
RECEIVE LATENCY TIMING						
	SSD symbol on MDI to MII Rising edge of RX_CLK with assertion of RX_DV		420		530	ns
	SSD symbol on MDI to MII Rising edge of RX_CLK with assertion of RX_DV	With PTP enabled	450		600	ns
	SSD symbol on MDI to Follower RMII Rising edge of XI clock with assertion of CRS_DV		499		660	ns
	SSD symbol on MDI to Leader RMII Rising edge of Leader clock with assertion of CRS_DV		499		720	ns
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL		450		590	ns
	SSD symbol on MDI to first symbol of SGMII		727		884	ns
25 MHz OSCILLATOR REQUIREMENTS						
	Frequency Tolerance		-100		+100	ppm
	Rise / Fall Time (10%-90%)				8	ns
	Jitter Tolerance (RMS)				25	ps
	XI Duty Cycle in external clock mode		40		60	%

6.6 Timing Requirements (continued)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
50 MHz OSCILLATOR REQUIREMENTS						
	Frequency			50		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Rise / Fall Time (10% - 90%)				4	ns
	Duty Cycle		35		65	%
25 MHz CRYSTAL REQUIREMENTS						
	Frequency			25		MHz
	Frequency Tolerance and Stability Over temperature and aging		–100		100	ppm
	Equivalent Series Resistance				100	Ω
OUTPUT CLOCK TIMING (25 MHz)						
	Frequency (PPM)		-100		100	-
	Duty Cycle		40		60	%
	Rise Time				5000	ps
	Fall Time				5000	ps
	Jitter (Short Term)				1000	ps
	Frequency			25		MHz
802.1AS Synchronised Clock						
	802.1AS Synchronized Clock Frequency		1		50	MHz
	Duty Cycle		45		55	%
	Jitter (rms)				100	ps
	Jitter (period)				400	ps
	Jitter (cycle to cycle)				300	ps
1pps Output	Synchronization Accuracy (802.1AS Clock source: Internal PLL/NCO DDS) - with optimized settings	Offset Variation across Reset cycles	-30		30	ns
		Jitter for a single reset cycle	-15		15	ns
	Synchronization Accuracy (802.1AS Clock source: recovered Clock @200MHz) - with optimized settings	Offset Variation across Reset cycles	-30		30	ns
		Jitter for a single reset cycle	-1		1	ns

(1) For supplies with ramp rate longer than 8ms, a RESET pulse is required after the last supply becomes stable.

6.7 Timing Diagrams

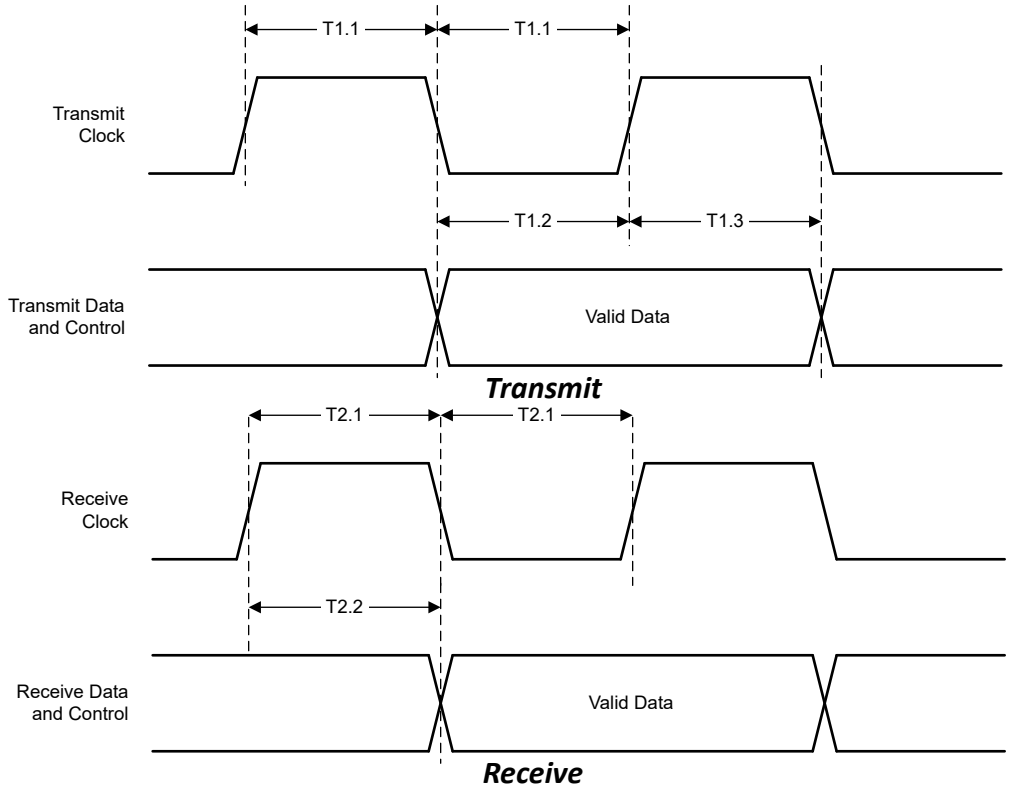


Figure 6-1. MII Timing

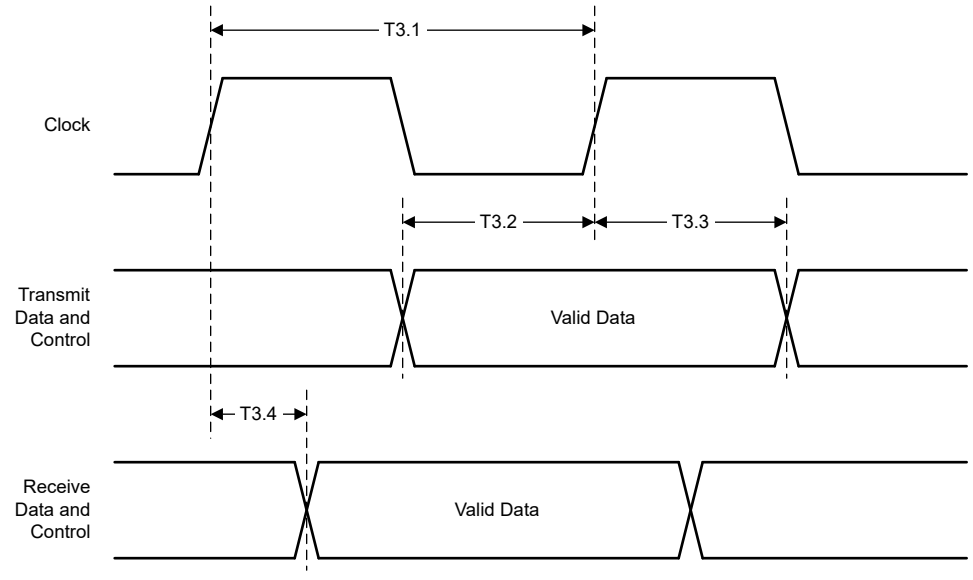


Figure 6-2. RMII Transmit and Receive Timing

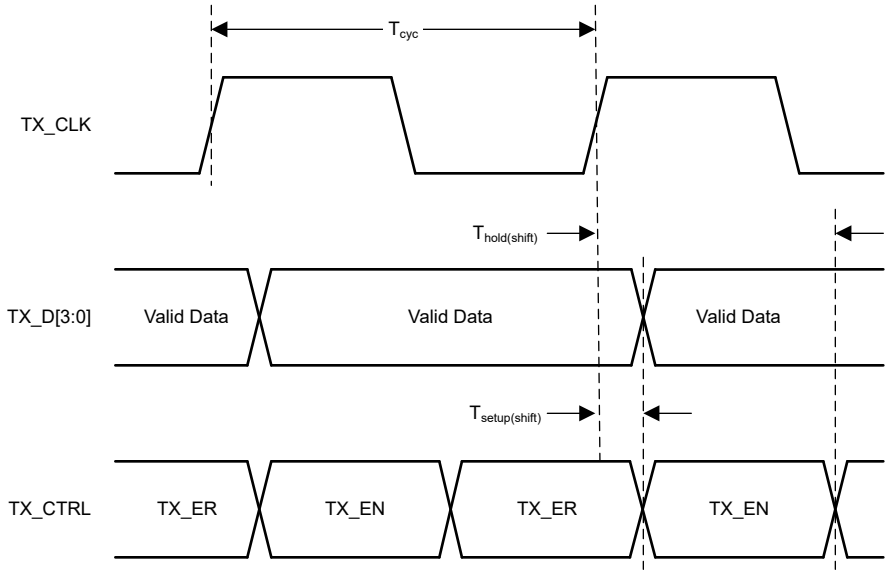


Figure 6-3. RGMII Transmit Timing (Internal Delay Enabled)

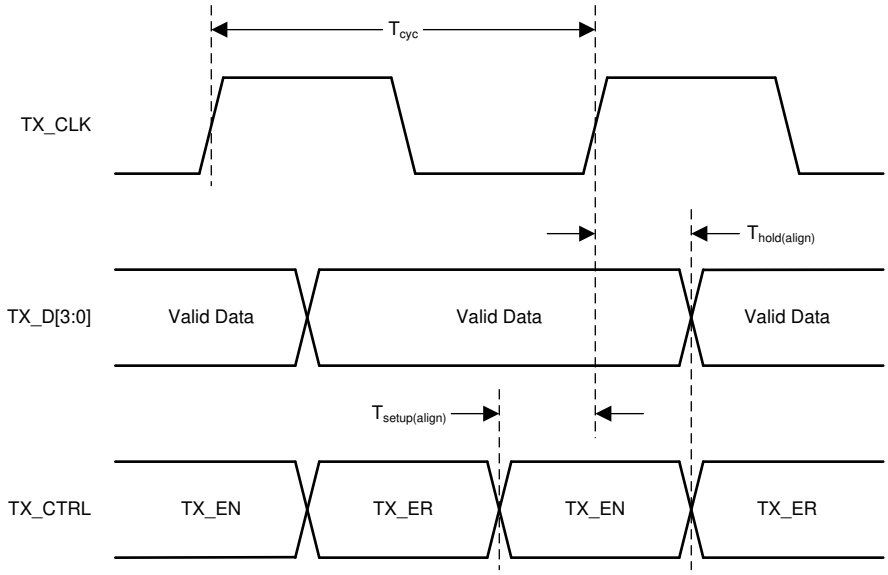


Figure 6-4. RGMII Transmit Timing (Internal Delay Disabled)

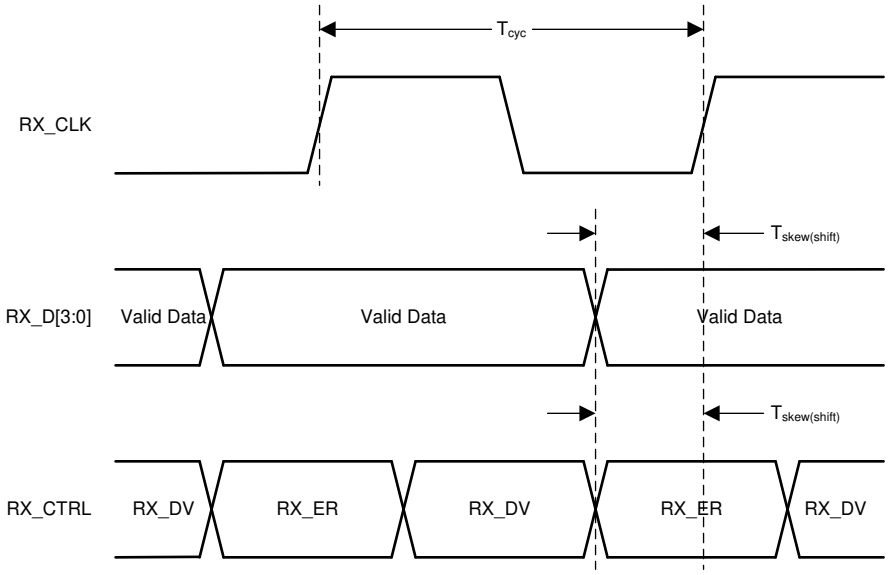


Figure 6-5. RGMII Receive Timing (Internal Delay Enabled)

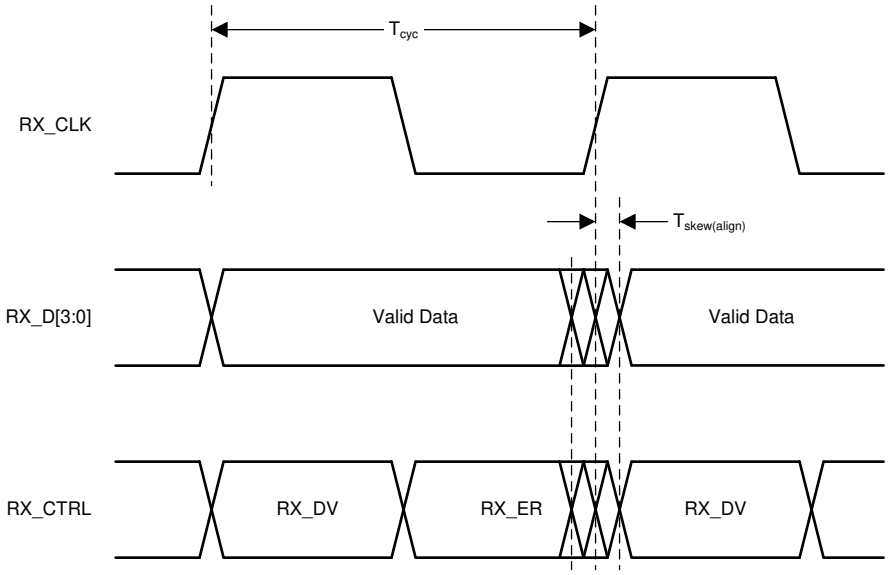


Figure 6-6. RGMII Receive Timing (Internal Delay Disabled)

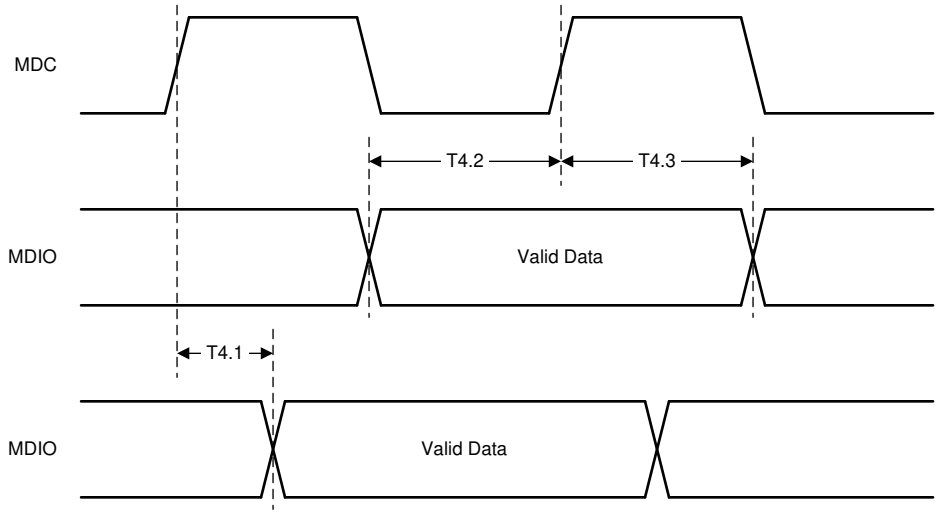


Figure 6-7. Serial Management Timing

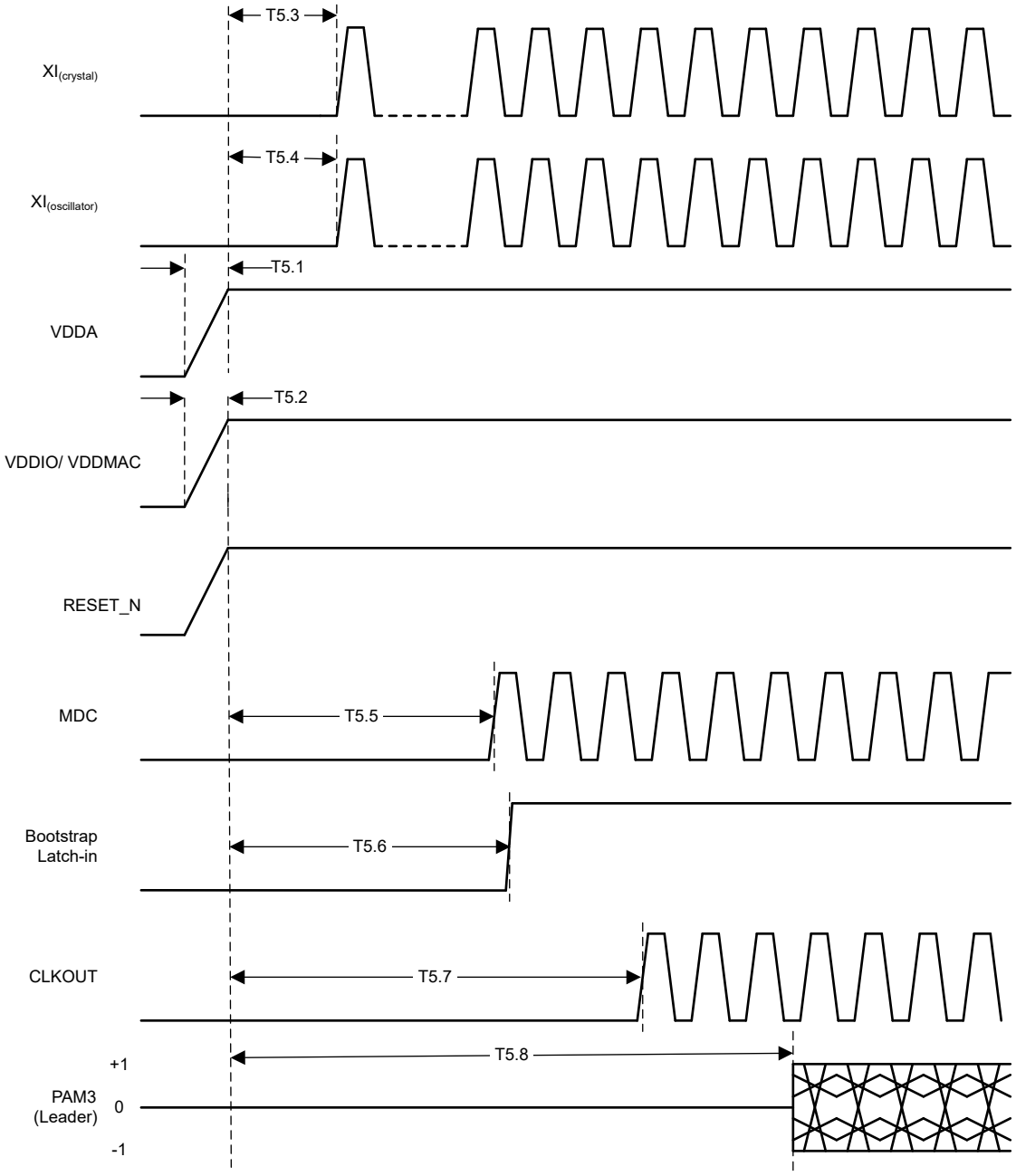


Figure 6-8. Power-Up Timing

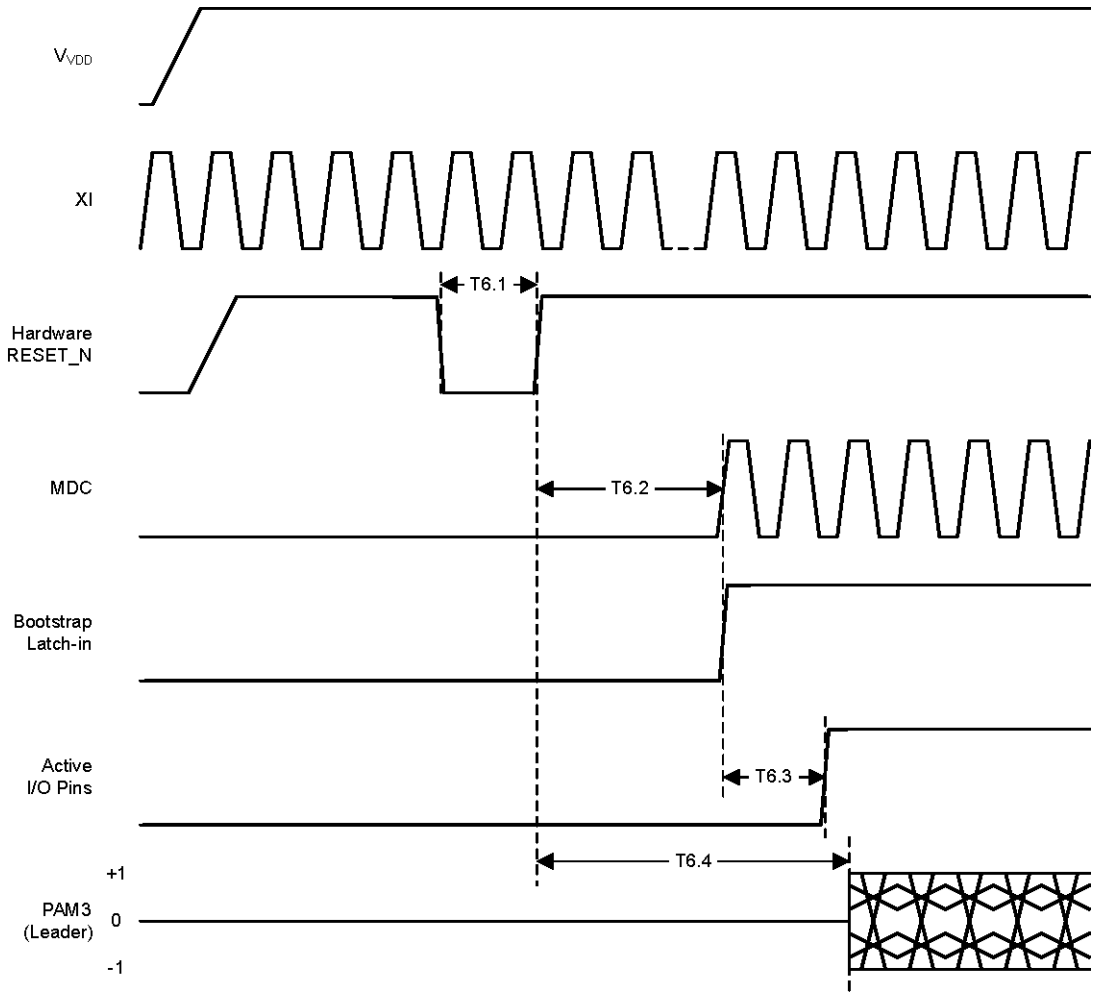


Figure 6-9. Reset Timing

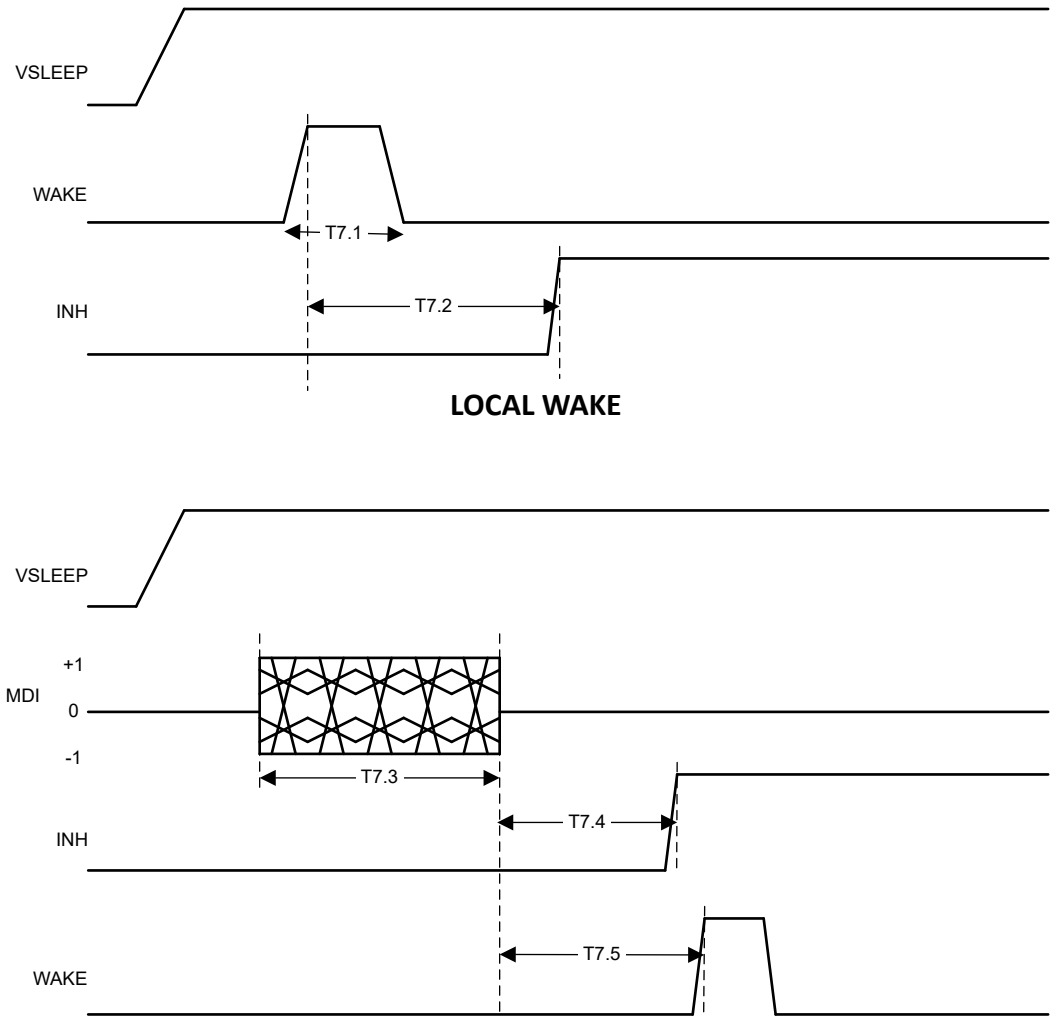


Figure 6-10. WAKE Timing

6.8 Typical Characteristics

Figure 6-11 and Figure 6-12 show typical characteristics of the MDI pins of the DP83TC815-Q1.

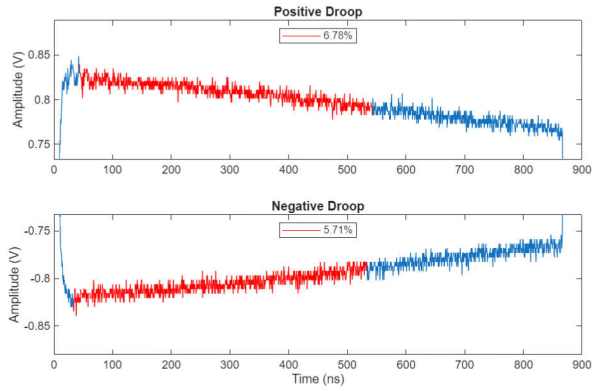


Figure 6-11. Typical Tx Droop

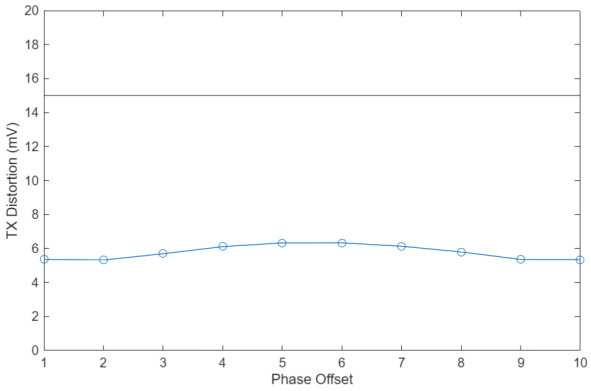


Figure 6-12. Typical Tx Distortion

7 Detailed Description

7.1 Overview

The DP83TC815-Q1 is a 100BASE-T1 automotive Ethernet PHY providing 100Mbps full-duplex communication. DP83TC815-Q1 is IEEE 802.3bw compliant and AEC-Q100 qualified for automotive applications.

This device is specifically designed to operate at 100Mbps speed while meeting stringent automotive EMC limits. The DP83TC815-Q1 transmits PAM3 ternary symbols at 66.667MHz over unshielded single twisted-pair cable. DP83TC815-Q1 is application-flexible, supporting MII, RMII, RGMII, and SGMII in a single 36-pin VQFN wettable flank package.

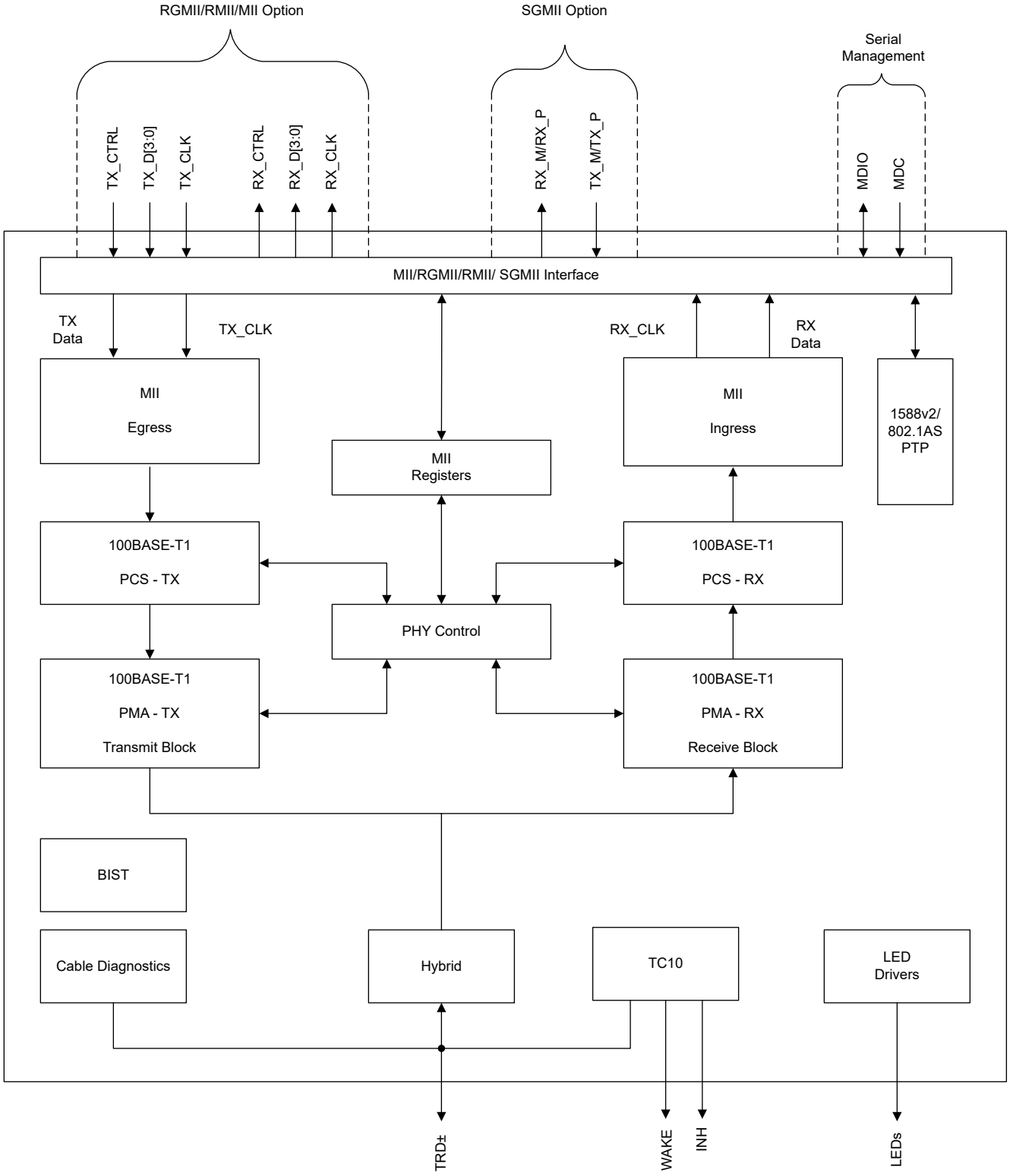
The PHY integrates 1588v2/802.1AS hardware time stamping, enabling highly accurate time synchronization.

The DP83TC815-Q1 supports Open Alliance TC-10 low power mode to enable lower power sleep/wake of ECU using Ethernet UTP and remove the need for additional wiring (for example, single-wire wake). The PHY also offers wake-forwarding without the need for link-up, enabling very fast wake-up of the network. The PHY supports WAKE and INH pins for implementing TC-10 functionality in the system. The DP83TC815-Q1 supports Fast-Wake up from Sleep where the PHY can wake-up and link-up even before the Host boots up, by retaining the PHY configuration during sleep.

There is an extensive Diagnostic Tool Kit within the DP83TC815-Q1 for both in-system use as well as debug, compliance, and system prototyping for bring-up. The DP83TC815-Q1 can meet IEC61000-4-2 Level 4 electrostatic discharge limits and also includes an on-chip ESD sensor for detecting ESD events in real-time.

The DP83TC815-Q1 is built for minimal thermal footprint with low active power as well as multiple low-power modes. DP83TC815-Q1 supports Wake-on-LAN Magic Packets, allowing upstream devices an option for entering into low-power state. Additionally, the device can enter into sleep state and remain until energy is detected on the MDI or locally woken through the WAKE pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEEE802.1AS Features

The DP83TC815-Q1 integrates IEEE 1588v2/802.1AS timestamping and other additional hardware engines to offer highly accurate synchronization with synchronization jitter of up to ±15ns (with options to reduce to up to ±1ns for point-to-point connections).

The DP83TC815-Q1 is also capable of providing a high quality time synchronized clock signal to achieve system level synchronization for ADAS sensor data synchronization, Corner RADAR Chirp synchronization, 1 pps signal for LiDAR, V2X, etc.

Note

The terms ***802.1AS*** , ***1588*** , ***1588v2*** , ***PTP*** are used interchangeably in the document.

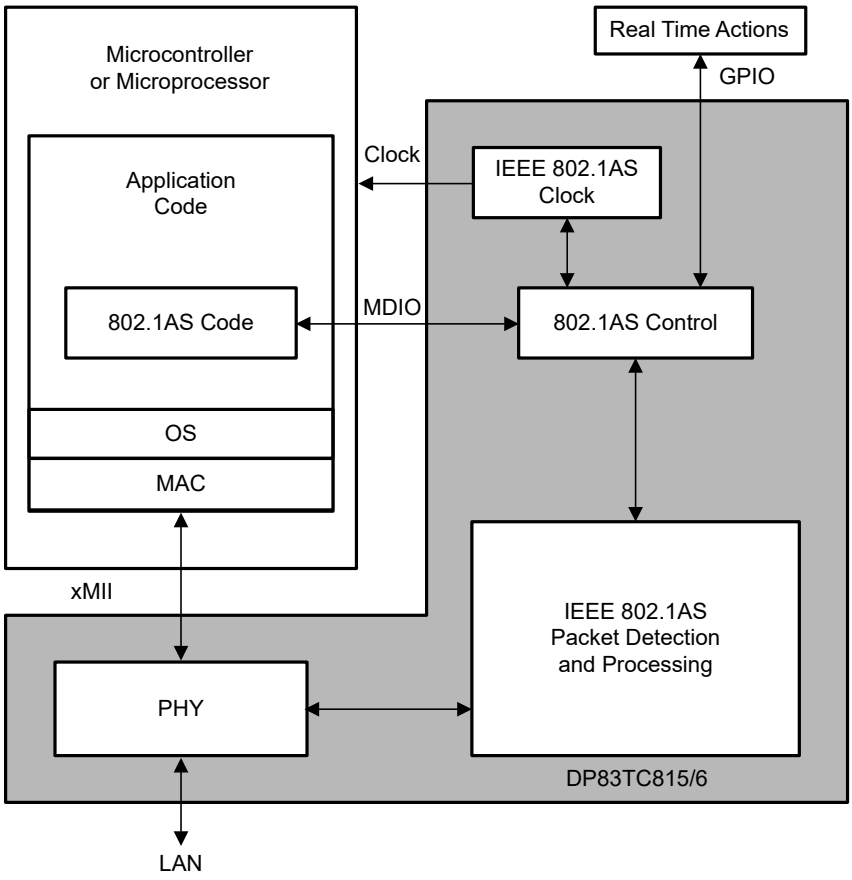


Figure 7-1. DP83TC815-Q1 Example PTP System Application

The PTP implementation consists of the following major function blocks:

- IEEE802.1AS Clock: This block provides an adjustable clock that is used as the time source for all PTP timestamp related functions.
- IEEE802.1AS PTP Timestamp: This block provides timestamping and packet modification functions.
- IEEE802.1AS Clock Events and GPIOs: This block provides clock events and GPIO functions for enabling timestamping of input events and for outputting clock comparison-based outputs/interrupt status.
- IEEE802.1AS Interrupt: This block provides interrupt generation, masking and status indication functions.
- IEEE802.1AS Registers: This block contains all configuration, control and status registers related information.

The range of register address used for IEEE802.1AS PTP implementation are listed below:

Table 7-1. IEEE802.1AS PTP Register Address

ADDRESS
0x0D00 to 0x0D0A
0x0D10 to 0x0D1D
0x0D20 to 0x0D2B
0x0D30 to 0x0D3F
0x0D40 to 0x0D4F
0x0D50 to 0x0D54
0x0DE0, 0x0DF0

Note

Before PTP is enabled through 0x0D00 or any PTP registers are accessed, bit 5 of register 0x05B7 must be toggled from 0->1->0. Additionally, to use recovered 200M and 100M as reference to PTP, set 0x05B7[5]=1.

IEEE802.1AS provides a time synchronization protocol, often referred to as the Precision Time Protocol (PTP), which synchronizes time across an Ethernet network. DP83TC815-Q1 supports IEEE802.1AS enabled Ethernet applications by providing hardware support for three time-critical elements.

- IEEE802.1AS synchronized clock generation
- Packet timestamps for clock synchronization
- Event triggering and timestamping through GPIO

7.3.1.1 PTP Clock Configuration

7.3.1.1.1 PTP Reference Clock

IEEE802.1AS clock can be run on the following different reference clocks selectable through register 0xD27

1. 250MHz/125MHz from PLL
2. 200MHz/100MHz recovered clock from MDI data
3. External reference clock
4. Clock output from Fractional (Frac) PLL (PTP_PLL)

For PTP applications, the IEEE802.1AS timer is recommended be run on the 250MHz PLL clock or the 200MHz recovered clock. Clock output from Frac PLL is recommended to be used only when clock output synchronous to IEEE802.1AS is needed on a GPIO.

7.3.1.1.2 PTP Synchronized Clock (Wall Clock)

The PTP time clock in DP83TC815-Q1 is a readable or writable time source for all IEEE802.1AS PTP related functions. PTP clock is a high accuracy oscillator and a counter that represents time in seconds and nanoseconds.

The clock consists of Seconds (32–bit field) and Nanoseconds (30–bit field). When the nanoseconds counter reaches 1 x 10^9, the nanoseconds counter reverts to zero and the seconds counter increments by 1. Additionally, a Fractional Nanoseconds (sub nanosecond - units of 2^{-32} ns) counter for time adjustment is available. PTP_RATE_DIR controls whether the device operates at a higher or lower frequency than the reference clock. The clock counter increment per cycle varies depending on the reference clock used and is equal to the period (in ns) corresponding to the PTP reference clock. A Frac PLL is used to generate non-integer synchronized clock output. Use of Frac PLL eliminates need for external VCXO.

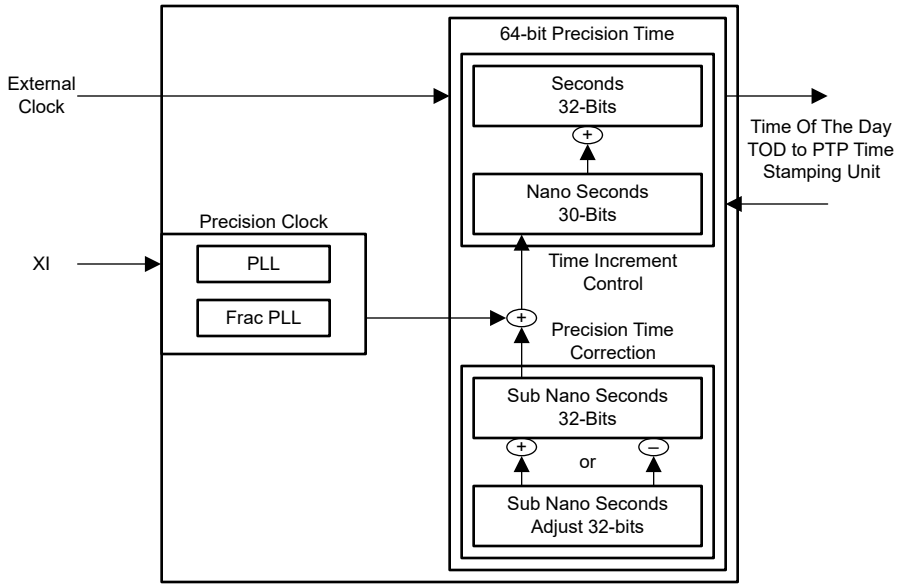


Figure 7-2. PTP Timestamping - Clock

The clock does not support negative time values. If negative time is required in the system, the host software has to make conversions from the PHY clock time to actual time.

The clock also does not support the upper 16-bits of the seconds field as defined by the specification (Version 2 specifies a 48-bit seconds field). If the upper 16-bits value is required to be greater than 0, it has to be handled by host software. The rollover of the seconds field only occurs every 136 years, minimizing burden to host software.

7.3.1.1.2.1 PTP Time Read or Write

The PTP Time Read or Write is done using the same register PTP_TDR. Since the time value is 62 bits, the register needs to be read/written 4 times to access the whole time value. The Setting time through the PTP Time Data Register involves writing all four time fields to the PTP_TDR and then issuing a 'Load PTP Clock' command through the PTP Control Register. The Time value can also be read using the PTP_TDR register by first setting the 'Read PTP Clock' command in the PTP Control Register and then reading all four time fields.

Writing a time value requires the following steps in the same order

1. Write Clock_time_ns[15:0] to PTP_TDR
2. Write Clock_time_ns[31:16] to PTP_TDR
3. Write Clock_time_sec[15:0] to PTP_TDR
4. Write Clock_time_sec[31:16] to PTP_TDR
5. Write to PTP_CTL with the 'Load PTP Clock' bit set

Read a time value requires the following steps in the same order

1. Write to PTP_CTL with the 'Read PTP Clock' bit set
2. Read Clock_time_ns[15:0] from PTP_TDR
3. Read Clock_time_ns[31:16] from PTP_TDR
4. Read Clock_time_sec[15:0] from PTP_TDR
5. Read Clock_time_sec[31:16] from PTP_TDR

7.3.1.1.2.2 PTP Clock Initialization

During software initialization when the device is powering-up, initialize the PTP clock in preparation for synchronizing to the leader clock. The PTP_CLKSRC register must be configured prior to enabling the IEEE802.1AS function to allow correct operation. During the initial synchronization attempt, the system time clock can be a little far apart from the PTP leader clock, so the system time clock most likely requires a

step-time adjustment to get the clock closer to the actual time. After that, the continuous time adjustment method or temporary time adjustment method can be the best options when the system time clock is close to being synchronized with the leader clock.

7.3.1.1.2.3 PTP Clock Adjustment

This section describes the available options to update the Clock time value. The DP83TC815-Q1 provides several mechanisms for updating the IEEE802.1AS clock based on the results of the synchronization protocol:

- Directly Read/Writable (Directly Setting or Reading the Time)
- Adjustable by Add/Subtract (Step-Time Adjustment)
- Frequency Scalable (Continuous Time Adjustment)
- Temporary Frequency Control (Temporary Time Adjustment)

Directly Read/Writable - Directly setting the system time clock to a value is accomplished by setting a new time in the clock registers (PTP_TDR). Initial setting of the clock/timer can require a direct write of a time value.

Adjustable by Add/Subtract - Time can also be adjusted by adding/subtracting a value to the present time value. For adding a value, the value has to be written to PTP_TDR register. For subtracting a value, the 32-bit 2's complement representations of both seconds and nanoseconds fields can be written to PTP_TDR register. To add/subtract the following registers have to be written in the same order

1. Write Clock_time_ns[15:0] to PTP_TDR
2. Write Clock_time_ns[31:16] to PTP_TDR
3. Write Clock_time_sec[15:0] to PTP_TDR
4. Write Clock_time_sec[31:16] to PTP_TDR
5. Write to PTP_CTL with the 'Step PTP Clock' bit set

Frequency Scalable- The system can be set up to perform continuous time adjustment to the IEEE802.1AS PTP clock. Frequency (clock/timer rate) can be adjusted via register control to match the frequency of the leader. This is also called **Permanent Rate Adjustment.** The clock can be programmed to operate at an adjusted frequency value by programming a rate adjustment value. The rate adjustment allows for correction on the order of 2^{-32} ns per reference clock cycle.

- **Rate Adjustment** - The clock can be programmed to operate at an adjusted frequency value by programming a rate adjustment value. The rate adjustment allows for correction on the order of 2^{-32} ns per reference clock cycle. The frequency adjustment allows the clock to correct the offset over time, avoiding any potential side-effects caused by a step adjustment in the time value.

Temporary Frequency (Time) Control : Allows time correction by running at a modified frequency for a period of time. This is also called **Temporary Rate Adjustment.** The clock can be programmed to operate at a temporary adjusted frequency value by programming a rate adjustment value and duration. The rate adjustment allows for correction on the order of 2^{-32} ns per reference clock cycle. The frequency adjustment allows the clock to correct the offset over time, avoiding any potential side-effects caused by a step adjustment in the time value. The clock can also be programmed to perform a temporary adjusted frequency value by including a rate adjustment duration.

Several mechanisms can be used to update the PHY's IEEE802.1AS clock, based on the results of the synchronization protocol. The method used to update the clock value can depend on the difference in the time values. For example, at the initial synchronization attempt, the clocks can be very far apart, and therefore require a Step Adjustment or a Direct Time Set. Later, when clocks are very close in value, the Temporary Rate Adjustment method can be the best option.

7.3.1.1.2.4 PTP Clock Output

The DP83TC815-Q1 provides a synchronized clock output signal for use by external devices. The output clock signal can be any frequency generated from reference clock divided by n, where n is an integer in the range of 2 to 255. This provides nominal frequencies from 125MHz down to 980.4kHz if the reference clock used is 250MHz.

The synchronized clock output is only supported when PTP Reference Clock used is PTP_PLL. The frequency of PTP_PLL is programmable.

The clock output signal frequency is controlled by the PTP_COC register. The output GPIO is controlled by the CLKOUT_MUX_CTL register. The output clock signal is generated using the rate information in the PTP_RATEH and PTP_RATEL registers and is therefore frequency accurate to the IEEE802.1AS clock time of the device. Note that any step adjustment in the IEEE802.1AS clock time cannot be accurately be represented on the 802.1AS clock output signal.

7.3.1.1.2.4.1 One Pulse Per Second (PPS) Output

The device can be programmed to output a PPS signal using the trigger functions in periodic mode. If a 50% duty cycle is acceptable, then any of the triggers can be used. If the PPS signal requires any other duty cycle (for example 200ms high time) then Trigger0 or Trigger1 must be used. The use of triggers is explained further in the following sections.

7.3.1.1.3 PTP Time Registers

Table 7-2. PTP Control and Time Registers

REGISTER NAME	REGISTER ADDRESS
PTP Control Register (PTP_CTL)	0x0D00
PTP Time Data Register (PTP_TDR)	0x0D01
PTP Clock Source Register (PTP_CLKSRC)	0x0D27
PTP Debug Select (PTP_DEBUG_SEL)	0x0DF0

Table 7-3. PTP Time Adjustment and Clock Output Control Registers

REGISTER NAME	REGISTER ADDRESS
PTP Temporary Rate Duration Low Register (PTP_TRDL)	0x0D1A
PTP Temporary Rate Duration High Register (PTP_TRDH)	0x0D1B
PTP Rate Low Register (PTP_RATEL)	0x0D04
PTP Rate High Register (PTP_RATEH)	0x0D05
Base frequency control(FREQ_CTL_1)	0x0D35
Base frequency control(FREQ_CTL_2)	0x0D36
Scheduler control(SCH_CTL_1)	0x0D33
Scheduler control(SCH_CTL_2)	0x0D34
PTP Clock Output Control Register (PTP_COC)	0x0D20
CLKOUT muxing control (CLKOUT_MUX_CTL)	0x0DA8

7.3.1.2 Packet Timestamps

This section provides details of:

- Available synchronizing clock options and operation modes
- IEEE802.1AS Transmit Packet Parser and Timestamp Unit
- IEEE802.1AS Receive Packet Parser and Timestamp Unit

7.3.1.2.1 Transmit (Egress) Packet Parser and Timestamp

The IEEE802.1AS PTP transmit parser monitors transmit packet data to detect IEEE802.1AS Event messages. The transmit parser can detect PTP Event messages transported directly in Layer2 Ethernet packets or PTP VLAN packets. Upon detection of a PTP Event Message, the device captures the transmit timestamp and provides the timestamp to host (MAC) for processing. In addition to PTP event based filtering, there is an option to filter and timestamp PTP event frames with a specific domain number.

Because the host (MAC) knows the order of packet transmission, only the timestamp is recorded (there is no need to record sequence number or other information). If required, the device has an option to record the 16-bit

SequenceId, the 4-bit messageType field, and generate a 12-bit hash value for octets 20-29 of the PTP event message. The device can buffer four timestamps.

If enabled, an interrupt can be generated upon a Transmit Timestamp Ready.

One-Step Operation:

In some cases, the transmitter can be set to operate in a One-Step mode. For Sync Messages, a One-Step device can automatically insert timestamp information in the outgoing packet. This eliminates the need for host(MAC) to read the timestamp and send a follow up message.

7.3.1.2.2 Receive (ingress) Packet Parser and Timestamp

The IEEE802.1AS/1588v2 receive parser monitors receive packet data to detect IEEE1588 Version 1 and Version 2 Event messages. The receive parser can detect PTP Event messages transported directly in Ethernet packets. Upon detection of a PTP Event message, the device captures the receive timestamp and provide the timestamp value to host (MAC). In addition to the timestamp, the device records the 16-bit SequenceId, the 4-bit messageType field, and generate a 12-bit hash value for octets 20-29 of the PTP event message. The device can buffer four timestamps.

If enabled, an interrupt is generated upon a Receive Timestamp Ready.

Receive Timestamp Insertion:

The DP83TC815-Q1 can deliver the timestamp to host (MAC) by inserting the timestamp in the received packet. This allows for a simple method to deliver the packet to software without having to match the timestamp to the correct packet. This also eliminates the need to read the receive timestamp through the Serial Management Interface.

7.3.1.2.3 PTP Transmit and Receive Timestamp Registers

Table 7-4. PTP Transmit and Receive Timestamp Registers

REGISTER NAME	REGISTER ADDRESS
PTP Transmit Configuration Register 0 (PTP_TXCFG0)	0x0D12
PTP Transmit Configuration Register 1 (PTP_TXCFG1)	0x0D13
PTP Receive Configuration Register 0 (PTP_RXCFG0)	0x0D15
Receive Configuration Register 1 (PTP_RXCFG1)	0x0D16
PTP Receive Configuration Register 2 (PTP_RXCFG2)	0x0D17
PTP Receive Configuration Register 3 (PTP_RXCFG3)	0x0D18
PTP Receive Configuration Register 4 (PTP_RXCFG4)	0x0D19
Event Timestamp Storage Configuration (PTP_EVNT_TSU_CFG)	0x0D1C
PTP Transmit Timestamp Register (PTP_TXTS)	0x0D08
PTP Receive Timestamp Register (PTP_RXTS)	0x0D09
PTP Offset Register (PTP_OFF)	0x0D29
PTP Receive Hash Register (PTP_RXHASH)	0x0D2B
PTP Ethernet Type Register (PTP_ETR)	0x0D28
PHY Status Frame Configuration Register 0 (PSF_CFG0)	0x0D14
PHY Status Frame Configuration Register 1 (PSF_CFG1)	0x0D21
PHY Status Frame Configuration Register 2 (PSF_CFG2)	0x0D22
PHY Status Frame Configuration Register 3 (PSF_CFG3)	0x0D23
PHY Status Frame Configuration Register 4 (PTP_PKTSTS4)	0x0D24
PTP ONESTEP OFFSET register(PTP_ONESTEP_OFF)	0x0D40
PTP Domain Filter Controls	0x0D49

7.3.1.3 Event Triggering and Timestamping

This section describes Input/Output functions used for implementing IEEE 802.1AS PTP Event Triggering and Event capture configuration.

7.3.1.3.1 Event Triggering (Output)

The DP83TC815-Q1 is capable of being programmed to generate a trigger signal on a GPIO configured as output pin based on the IEEE802.1AS time value. Each trigger can be programmed to generate a one-time rising or falling edge, a single pulse of programmable width. DP83TC815-Q1 can also be used to generate a Periodic Output signal.

For each trigger, the host (MAC) specifies the desired GPIO and trigger occurrence time. The trigger is generated when the internal PTP clock matches the programmed trigger activation time.

The device supports up to 8 trigger signals which can be output on any of the GPIO signal pins. Multiple triggers can be assigned to a single GPIO, allowing generation of more complex waveforms (that is, a sequence of varying width pulses). The trigger signals are OR'ed together to form a combined signal. The triggers are configured through the PTP Trigger Configuration Registers and enabled through the PTP Control register. The trigger time and width settings are controlled through the PTP Control and Time Data registers. Each trigger can be programmed to generate status on completion or on an error.

The DP83TC815-Q1 can be programmed to output a Pulse-Per-Second (PPS) signal using the trigger functions.

7.3.1.3.1.1 Trigger Initialization

To initialize a trigger, the trigger configuration can be set using the appropriate PTP Trigger Configuration Register. Arming a trigger consists of the following steps

1. Set the 'Trigger Load' bit in the PTP Control Register (PTP_CTL) along with the 'Trigger Select' setting for the trigger. This disables the trigger if the trigger was previously enabled.
2. Write to PTP_TDR: Start_time_ns[15:0]
3. Write to PTP_TDR: Initial state, Wait for Rollover, Start_time_ns[29:16] (Initial state is the stage of the GPIO before triggering starts) (If wait for rollover bit is set, the bit indicates that the trigger is not be armed until the seconds field of the clock time has rolled over from 0xFFFF_FFFF to 0.)
4. Write to PTP_TDR: Start_time_sec[15:0]
5. Write to PTP_TDR: Start_time_sec[31:16]
6. Write to PTP_TDR: Pulsewidth[15:0]
7. Write to PTP_TDR: Pulsewidth[31:16]
8. Write to PTP_TDR: Pulsewidth2[15:0]
9. Write to PTP_TDR: Pulsewidth2[31:16]
10. Set the 'Trigger Enable' bit in the PTP_CTL register along with the 'Trigger Select' setting for the trigger

For Edge type signals, Pulsewidth2 is interpreted as a 16-bit seconds field and Pulsewidth1 is a 30-bit nanoseconds field.

For Triggers 0 and 1, when used for Single or Periodic Pulse type signal, Pulsewidth controls the first pulse width and Pulsewidth2 value controls the second pulse width (total period is Pulsewidth + Pulsewidth2). For Pulsewidth and Pulsewidth2, bits[31:30] is the seconds field and bits[29:0] is the nanoseconds field.

For all other triggers in periodic mode, the high and low pulse widths are the same (period is twice Pulsewidth) and Pulsewidth2 is not used. For Pulsewidth, bits[31:30] is the seconds field and bits[29:0] is the nanoseconds field.

Step 10 is not necessary if all appropriate fields are written. If fields are not changing from previous settings, the latter writes to the PTP_TDR register can be skipped and step 10 can be excluded.

Reading the trigger control settings is similar to the process for writing these values.

1. Set the 'Trigger Read' bit in the PTP Control Register (PTP_CTL) along with the 'Trigger Select' setting for the trigger.

2. Read fields from PTP_TDR in same order as written above.

Note that for periodic signals, the time value being read back is the next programmed trigger time rather than the start trigger time (these can or can not be the same value). This capability is essential for diagnostic purposes only.

7.3.1.3.2 Event Timestamp (Input)

The DP83TC815-Q1 can be programmed to timestamp an event by monitoring the input signal. The event can be monitored for rising edge, falling edge, or either. The Event Timestamp Unit can monitor up to eight events which can be set to any of the GPIO signal pins. PTP event timestamps are stored in a queue which allows storage of up to eight timestamps. When an event timestamp is available, the device sets the 'Event Ready' bit in the PTP Status Register.

The PTP_ESTS provides detailed information on the available event timestamp, including information on the event number, rise/fall direction, and indication of events missed due to overflow of the device event queue. Event timestamp values must be **adjusted by 14ns** (3 times period of the IEEE802.1AS reference clock frequency of 250MHz + 2ns) to compensate for input path and synchronization delays. The time value compensated depends on the IEEE802.1AS reference clock frequency. The adjustment time depends on the reference frequency programmed and has to be adjusted based on the clock selected by the host. The Event Timestamp Unit is configured through the PTP Event Configuration Register (PTP_EVNT). External event inputs on the GPIO pins can be monitored and timestamped with the resolution of 4(8) ns. If event interrupts are enabled in the PTP Status Register, an interrupt is generated upon detection of the event.

Each event monitor can be placed in a single-event capture mode. In this mode, the event monitor captures a single event timestamp.

7.3.1.3.2.1 Timestamp Storage and Reading

PTP event timestamps are stored in a queue which allows storage of up to eight timestamps. The timestamp values can be read by the host through the PTP Event Data Register (PTP_EDATA). The process for reading event timestamps is as follows:

1. Read PTP_ESTS to determine if an event timestamp is available.
2. Read from PTP_EDATA: Extended Event Status[15:0] (available only if PTP_ESTS:'Multiple Events Detected' is 1)
3. Read from PTP_EDATA: Timestamp_ns[15:0]
4. Read from PTP_EDATA: Timestamp_ns[29:16] (upper 2 bits are always 0)
5. Read from PTP_EDATA: Timestamp_sec[15:0]
6. Read from PTP_EDATA: Timestamp_sec[31:16]
7. Repeat Steps 1-6 until PTP_ESTS = 0

If desired, software can skip reading all or a portion of the timestamp based on the value of the 'PTP_ESTS:Event Timestamp Change Length' field.

7.3.1.3.3 Event Capture and Output Trigger Registers

Table 7-5. Event Capture and Output Trigger Registers

REGISTER NAME	REGISTER ADDRESS
PTP Trigger Configuration Register (PTP_TRIG)	0x0D10
PTP Event Configuration Register (PTP_EVNT)	0x0D11
PTP Trigger Status Register (PTP_TSTS)	0x0D03
PTP Event GPIO selection (PTP_EVENT_GPIO_SEL)	0x0D30
PTP Event Status Register (PTP_ESTS)	0x0D0A
PTP Event Data Register (PTP_EDATA) : For Extended Event Status	0x0D0B
PTP Event Data Register (PTP_EDATA) : When Timestamping	0x0D0B

Table 7-5. Event Capture and Output Trigger Registers (continued)

REGISTER NAME	REGISTER ADDRESS
PTP Status Register (PTP_STS)	0x0D02

7.3.1.4 PTP Interrupts

The PTP module can interrupt the system using the INT_N pin on the device, shared with other interrupts from the PHY. As an alternative, the device can be programmed to use a GPIO (PTP_INTCTL) pin to generate PTP interrupts separate from other PHY interrupts.

Using the Shared Interrupt Pin:

Host (MAC) can use the INT_N pin and must configure which PTP functions generate interrupts using the interrupt enables in the PTP Status Register (PTP_STS).

Using a GPIO Pin:

To use a GPIO pin for interrupts, host (MAC) must program the PTP_INTCTL register with the GPIO pin to use for interrupts. The interrupt is an active high signal, implemented as an Open-Drain function (drive low, pulled high via an external pullup resistor). Software also must configure which PTP functions generate interrupts using the interrupt enables in the PTP Status Register (PTP_STS). This mechanism provides slightly simpler handling of PTP interrupts since there is no need to check the MISR for interrupts.

7.3.1.5 PTP I/O Configuration

The DP83TC815-Q1 features a set of general-purpose input/output (GPIO) pins that are configurable to meet various application needs. These GPIO pins can be used for input event monitoring, output pulse generation, or outputting unique serial bit streams.

When configured for PTP application the GPIOs work closely with the IEEE802.1AS PTP to generate and monitor precisely timed signals synchronous to the precision time clock. The GPIO output pins can be configured to initiate an output upon the occurrence of a specific time which is being kept by the on-board precision time clock. Likewise, the specific time of arrival of an input event can be captured and recorded with respect to the precision time clock.

In addition to timestamping PTP packets, the IEEE802.1AS Clock value can be saved into a set of clock capture registers based on the GPIO inputs. The GPIO output pins can be configured to initiate an output upon the occurrence of a specific time configured. If an LED pin is to be used as a GPIO, the LED function must be disabled prior to configuring the GPIO function.

Note: The IEEE802.1AS module supports up to 7 GPIO signals and details are summarized in the below table:

Table 7-6. DP83TC815-Q1 IEEE802.1AS PTP Function Mapping

FIELD	PIN	50/25MHz PTP INPUT	PTP SYNC CLOCK	PTP INTERRUPT	EVENT TRIGGER	EVENT CAPTURE
LED_0 / GPIO_0	35	Yes		Yes	Yes	Yes
LED_1 / GPIO_1	6			Yes	Yes	Yes
CLKOUT / GPIO_2	16		Yes	Yes	Yes	Yes
GPIO_3	18		Yes	Yes	Yes	Yes
GPIO_4	19		Yes	Yes	Yes	Yes
GPIO_5	20	Yes		Yes	Yes	Yes
RX_ER / GPIO_6	14			Yes	Yes	Yes

7.3.2 TC10 Sleep Wake-up

DP83TC815-Q1 is a 100BASE-T1 Ethernet PHY with TC-10 power saving feature with the following features.

- Open Alliance TC10 compliant
- 7µA (Typical, 27°C), 18µA (Maximum, 125°C) sleep current

- Wake forwarding feature for Ethernet network wake-up
- Fast Wake-up
- Open Alliance TC1 Interoperability and EMC compliant

This block diagram shows the system level integration of DP83TC815-Q1 to support the TC10 sleep/wake-up feature.

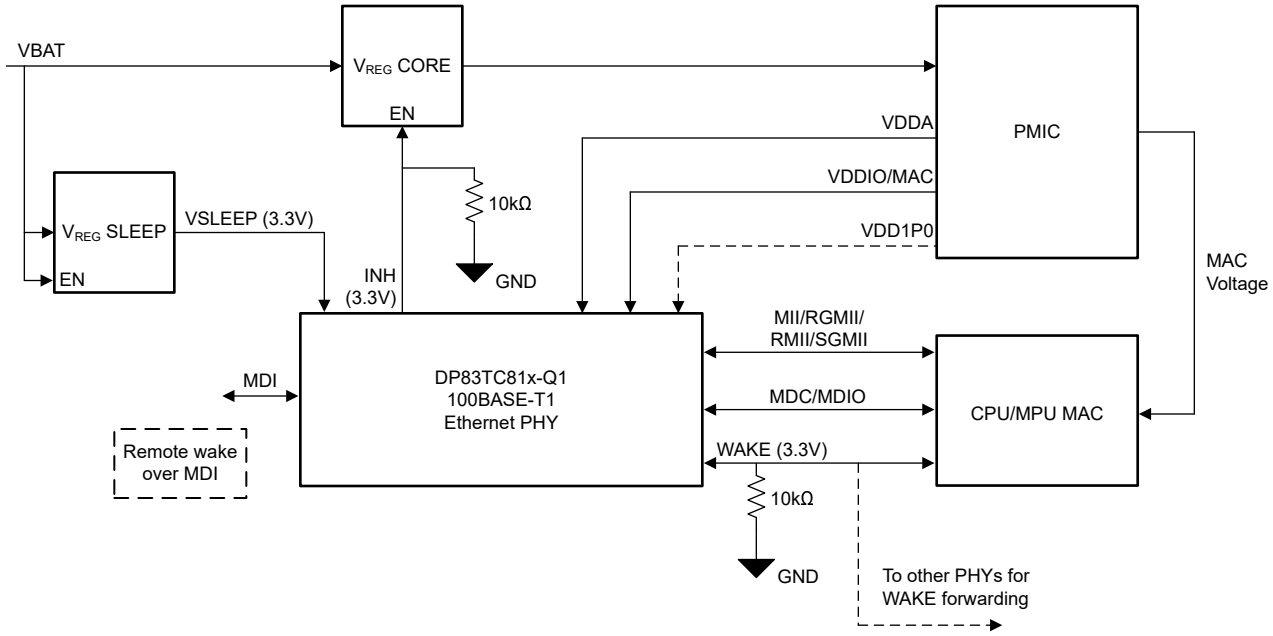


Figure 7-3. System Block Diagram

7.3.2.1 Functions of the PHY for TC10 Support

The following section describes in detail the primary functions of the ethernet PHY (DP83TC815-Q1) in supporting TC10.

7.3.2.1.1 Transition from Sleep to Wake-up Mode

7.3.2.1.1.1 Local Wake Detection

To wake-up the PHY locally (local wake), a pulse of width greater than 40µs is required to be forced on the WAKE pin. The detection circuit inside the PHY on the WAKE pin rejects any pulse of width less than 10µs and detects any pulse greater than 40µs reliably. The core power supplies (VDD1P0, VDDA, VDDIO/VDDMAC) are not needed for the PHY for local wake detection.

After the wake-up, PHY transitions from sleep to wake-up mode and pulls INH to high.

For local wake, it is assumed that some portion of the system is already active and the PHY is in TC10 sleep. As an example, the system can have a microcontroller in active mode to control the WAKE pin of the PHY. When the MCU wants to wake up the PHY from TC10 sleep, it raises the WAKE pin to 3.3V to send a wake pulse.

7.3.2.1.1.2 WUP Transmission and Reception

To wake-up the link partner remotely, the PHY needs to send a defined sequence of PAM3 symbols for 1 ms+/-0.3 ms. WUP transmission is done after a local wake-up without any manual intervention provided the device is strapped to autonomous mode and the pin RESET is not asserted. If the device is strapped to managed mode or if the device is in RESET state, WUP is transmitted only after the device transitions to normal mode.

During the sleep mode, to wake-up the PHY from sleep, remote link partner transmits WUP. The PHY detects the WUP and transitions from the sleep mode to functional mode. The core power supplies (VDDA, VDDIO/

VDDMAC, VDD1P0) are not needed for the PHY for WUP detection. The incoming WUP signal must be compliant to 100Base-T1 PMA signal PSD mask defined in IEEE802.3.

7.3.2.1.2 Wake Forwarding

Wake forwarding is a way to wake-up other PHYs connected to the same WAKE line, when one of the PHYs have woken up remotely. When PHY wakes-up from sleep on the reception of WUP (remote wake-up), the PHY transmits a pulse of width greater than 40µs on the WAKE line to wake-up other PHYs connected to the same wake-line without any manual intervention.

Wake forwarding can also be done by a PHY during active link upon reception of special WUR symbols. WUR can be initiated on one the PHYs by programming ***reg<0x018C> = 0x0080*** . The link partner PHY forwards WAKE pulse of width 40µs upon reception of those WUR symbols.

Note

Programming ***0x018C = 0x0080*** without the link-up makes the PHY initiate WUR immediately after the link is up.

7.3.2.1.3 Transition to Sleep - Sleep Negotiation

Sleep negotiation can be initiated from one of the two PHYs connected through link-up. Post the initiation, both of these PHYs go through negotiation and smoothly transition to sleep.

The sleep negotiation can be initiated (local sleep req) by programming ***reg<0x018C> = 0x0002*** on any of the PHYs.

Note

Sleep can only be initiated when there is active link between the PHYs. Programming ***0x018C = 0x0002*** without the link-up makes the PHY initiate sleep immediately after the link is up.

The states the PHYs go through in the negotiation are explained in detail below.

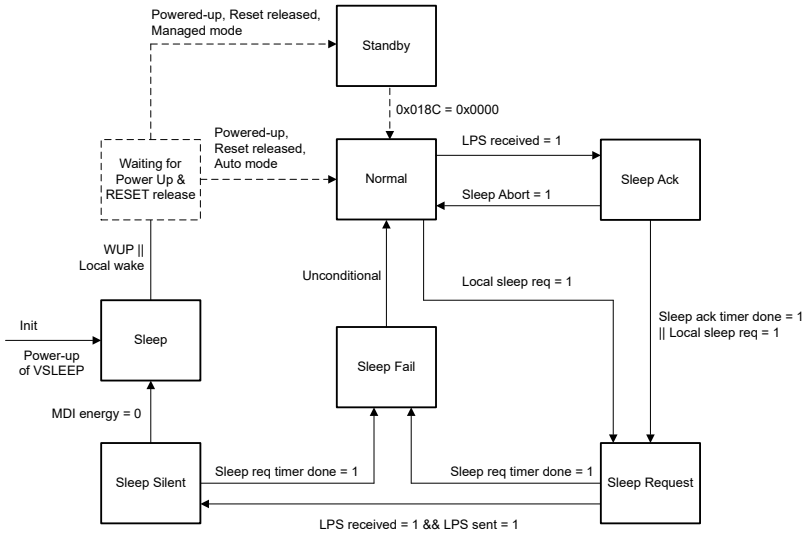


Figure 7-4. Sleep State Diagram

The MAC/controller intervention is only needed to initiate the sleep and abort the Sleep. All other state transitions happen though interaction between both the PHYs and need no external intervention and are explained below for information purpose only.

7.3.2.1.3.1 Sleep Ack

When a PHY receives LPS symbols from the link partner, the PHY transitions from Normal state (linked-up state) to Sleep ACK state.

During this transition, a timer of 8ms (sleep_ack_timer) is initialized and an interrupt is raised to indicate the MAC that the link partner is requesting sleep. The interrupt (LPS_int) is enabled by default (***reg<0x0018>[0]=1***).

The MAC can choose to abort the sleep by

- Programming ***reg<0x001B> = 0x0001*** (or)
- Drive a high pulse on LED_1 to abort the sleep (This feature is disabled by default and has to be enabled prior to sleep negotiation by programming ***reg<0x001B> = 0x0002***)

The PHY transitions back to Normal state if the MAC aborts the sleep. In case, the MAC chooses not to abort sleep before sleep_ack_timer lapses, the PHY transitions to Sleep Request state.

7.3.2.1.3.2 Sleep Request

The PHY which initiated the sleep (locally initiated), transitions from Normal to Sleep Request state. When the PHY transitions to Sleep Request, a timer of 16 ms (sleep_req_timer) is initialized and LPS symbols are transmitted (at least 64 bits). The PHY then waits for the link partner to send back the LPS symbols. After LPS symbols are received back from the link partner, the PHY transitions to Sleep Silent state. In case the LPS symbols are not received before sleep_req_timer lapses, the PHY transitions to Sleep Fail state.

The PHY for which sleep is initiated remotely, the PHY transitions from Normal to Sleep ACK to Sleep Request provided the MAC chose not to abort the sleep. When the PHY transitions to Sleep Request, a timer of 16 ms (sleep_req_timer) is initialized and LPS symbols are transmitted (at least 64 bits). After LPS symbols are transmitted, the PHY transitions to Sleep Silent state.

7.3.2.1.3.3 Sleep Silent

The PHY transitions to Sleep Silent from the Sleep Request state and waits for the line to go silent. If the line goes silent, the PHY transition from Sleep Silent to the Sleep state. In case the PHY does not go silent before sleep_req_timer lapses (16ms timer initialized when the PHY moved to Sleep Request state).

7.3.2.1.3.4 Sleep Fail

The PHY transitions to Sleep Fail if LPS symbols are not received before sleep_req_timer lapses or if the line is not silent before sleep_req_timer lapses, the PHY transitions to Sleep Fail state. When the PHY goes through this state, sleep fail interrupt flag (0x0018[13]) is set. Indication of this flag on INT_N pin can enabled through 0x0018[5].

After this transition, the PHY unconditionally transitions to Normal state.

7.3.2.1.3.5 Sleep

The PHY transitions to Sleep state after the negotiation is successful. In the Sleep mode, the INH transitions from High to Low. To get the lowest power consumption, the core power supplies (VDD1P0, VDDA, VDDIO/ VDDMAC) can be cut off. In Single Supply Mode, VDD1P0 is cut-off internal to the PHY and no external power switch is required.

In this Sleep state, the PHY waits for local wake or remote wake to eventually transition to Normal state.

After the first power-up, the PHY comes up in this sleep state until activity is observed on WAKE pin or MDI lines.

Note

In this sleep state, TI recommends not to drive all the pins controlled by MAC/controller and to be left in a Hi-Z state. The pins must be made Hi-Z before the core power supplies are cutoff. 25MHz clock on XI is not needed by the PHY in the sleep mode and TI recommends MAC/controller not to drive. Crystal oscillator present on XI, XO pins internal to the PHY is also disabled in sleep mode.

7.3.2.1.3.6 Force Sleep

PHY can be placed into sleep by bypassing the sleep negotiation by programming ***reg<0x0444> = 0x000C*** .

For this forced sleep to work, WAKE must be driven low and MDI lines must be silent. To make MDI lines silent write ***0x523 = 0x0001*** . Else, the PHY transitions to functional state immediately after the sleep is forced.

7.3.2.2 Power Supply Networks for Sleep Applications

DP83TC815-Q1 does not have any restrictions with respect to supply sequencing of VDD1P0, VSLEEP, VDDA, VDDIO/VDDMAC. The sleep functionality in the PHY is active immediately after the VLSEEP supply ramp is complete. The core functionality of the PHY is active 10ms after the last core power supply ramp is complete or after the device transitions from sleep to functional state whichever happens later.

The core supplies can be cut off in a system which requires the lowest current consumption in sleep mode. In Single Supply Mode, VDD1P0 is cut-off internal to the PHY and no external switch is required.

The image below shows some of the configurations of supply networks.

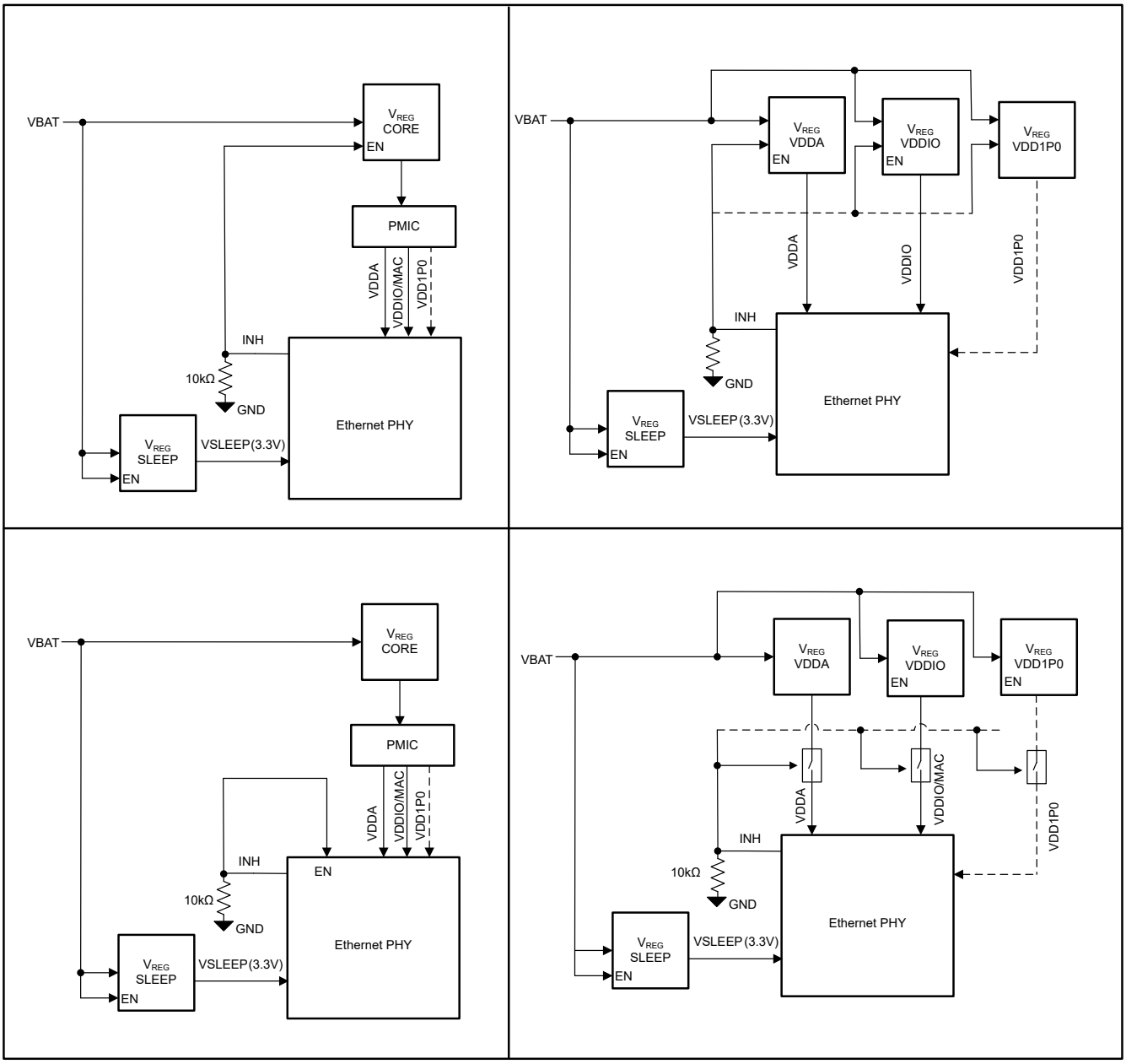


Figure 7-5. Core Supply Networks

The PHY doesn't malfunction even if the supplies are not cutoff. But, the current consumption of the PHY from the core supplies are high. The table below shows the current comparison in sleep mode when supplies are cut off and when the supplies are intact.

Table 7-7. Current Consumption Comparison

S.NO	SUPPLY	UNITS	CURRENT CONSUMPTION (Max)	
			SUPPLIES CUT-OFF	SUPPLIES INTACT
1	VSLEEP	mA	0.018	0.018
2	VDDA	mA	0	50
3	VDDIO/VDDMAC (3.3V)	mA	0	23
4	Total Current	mA	0.018	73

Many power supply networks share the PMIC between different PHYs available on the same PCB board to reduce the number of components and the board area.

In this case, the INH of the different PHYs can be connected together and this signal functions are Wired-OR (due to the open drain configuration of INH). The power supplies are cut-off only after all the PHYs are in sleep mode. Hence, there is high current consumption from the supplies even though one or some of the PHYs are in sleep. The functionality of the PHYs in sleep is affected during this case. To achieve the lowest power consumption in the above case, PMIC must be separated for both the PHYs.

The figure below shows one of the supply network examples where two PHYs share the same PMIC.

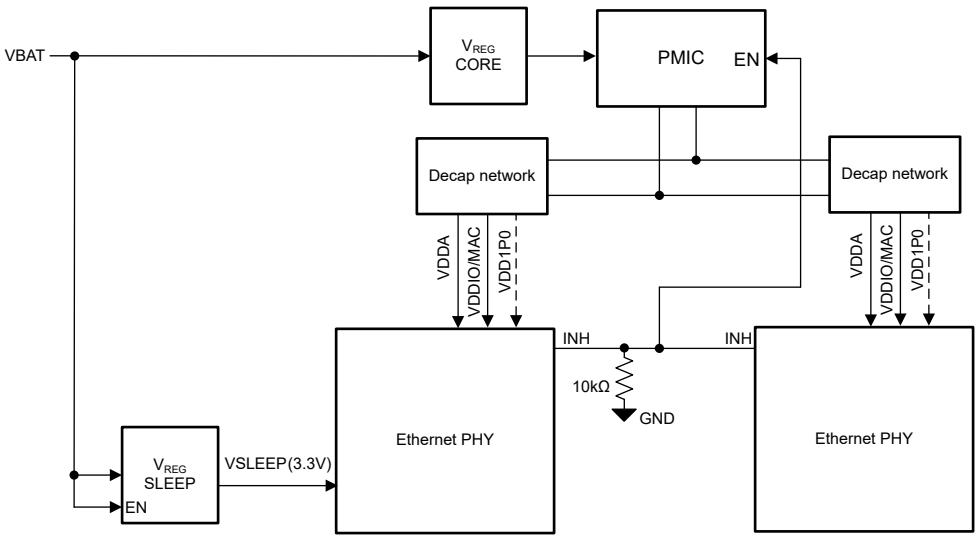


Figure 7-6. Power Network With Shared Core Supplies

7.3.2.3 Configuration for Non-TC10 Applications

The following configuration is recommended for DP83TC815-Q1 in applications where TC10 sleep/wake-up functionality is not required.

Hardware Configuration

The below hardware configurations must be followed even if *'TC10 Disable'* strap is used.

- VSLEEP pin can be connected to VDDA (or any 3.3V supply source).
- WAKE pin must be pulled up to corresponding VSLEEP supply connection directly or through a resistor lower than 10kΩ. WAKE pin cannot be pulled up to VDDIO/VDDMAC supply.
- INH can be left floating.

Software Configuration

To disable the TC10 functionality, an additional setting ***reg<0x018B>[8] = 1*** must be programmed along with the other initialization settings. This additional configuration is not required if *'TC10 Disable'* strap is mounted accordingly to disable TC10.

7.3.2.4 Miscellaneous Sleep Features

WUR Initiation Through WAKE Pin

As mentioned in *'WAKE forwarding'* section, WUR can be initiated through a register write. Apart from the register option, WUR can also be initiated from a PHY if a pulse of >40µs is driven on the WAKE pin of the PHY. To enable this feature, reg<0x017F>[15] = 1 must be programmed.

Programmable Wake-Forward Pulse Width

The width of the pulse forwarded on the WAKE pin when a PHY receives WUR is programmable. Table 7-8 shows the register write needed for each of the pulse width options available.

Table 7-8. WUR Wake Pulse Width

S. NO	WIDTH OF PULSE	REGISTER WRITE
1	50µs	0x0184[3:2] = 2'b00
2	500µs	0x0184[3:2] = 2'b01
3	2ms	0x0184[3:2] = 2'b10
4	20ms	0x0184[3:2] = 2'b11

The forwarded wake-pulse when the device wakes up from sleep through WUP is not programmable.

7.3.2.5 Fast Wake-up

In a typical Sleep-Wake cycle of an ECU, post wake-up, SoC/Host takes a long time to boot up. The PHY which needs registers to be programmed to link-up, doesn't start the link-up process until SoC completes the boot-up phase. The link-up process of Ethernet PHY takes 100ms, before the link is ready for communication which adds up to the delay.

DP83TC815-Q1 supports custom Fast Wake-up feature to reduce the time delay from wake-up to communication ready. The image below shows the timing differences from wake-up to link-up, with and without Fast-Wake feature.

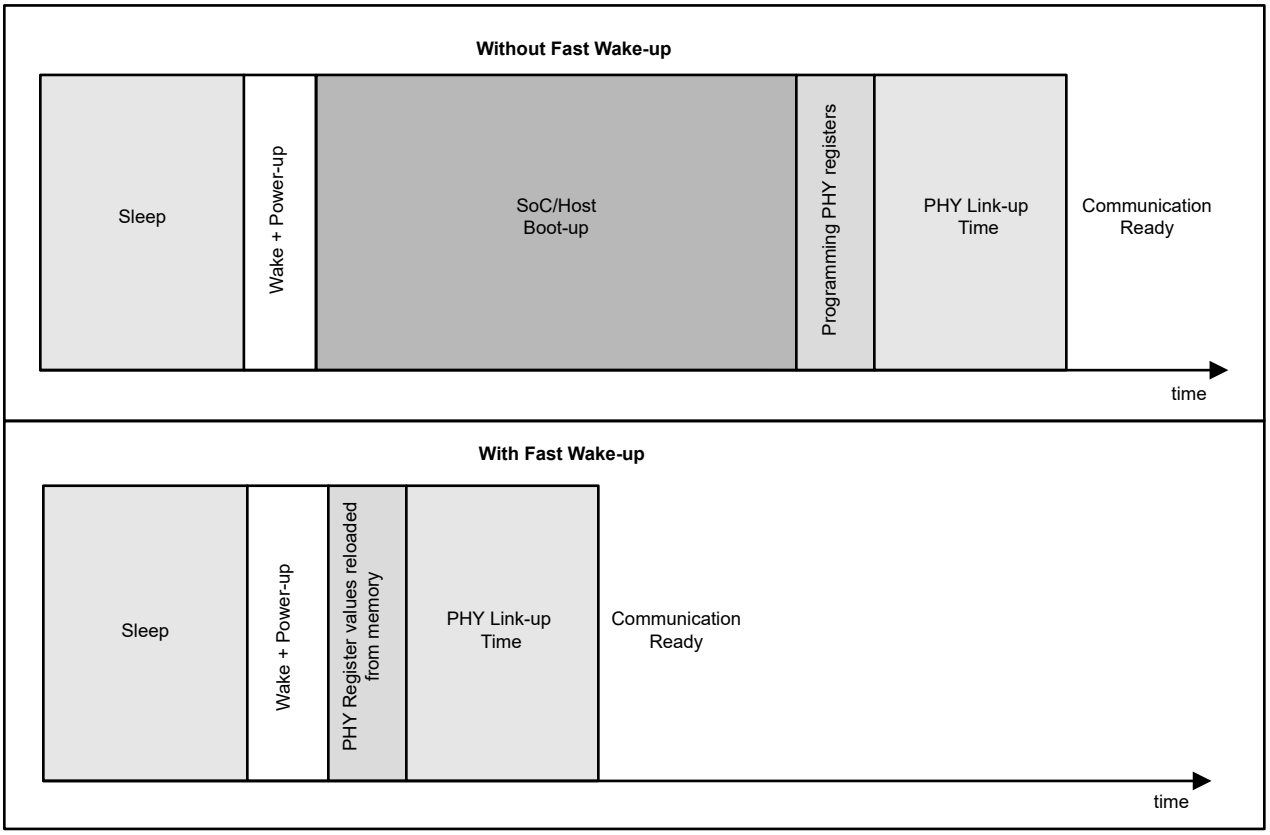


Figure 7-7. Fast Wake-Up Timing Block Diagram

DP83TC815-Q1 integrates low power consuming memory required to store register information across sleep and wake cycle. The register values stored in the memory are loaded automatically post wake and core power-up

of the PHY. Since SoC/Host is not needed to program the registers, the PHY can be communication ready independently, thereby reducing the delay from wake to communication ready significantly.

The memory integrated in the VSLEEP domain so that the information is intact even when the core power supplies (VDDA, VDD1P0, VDDMAC/VDDIO) are turned-off during the sleep state. This memory is volatile and erased when VSLEEP power supply is turned-off.

Note

Register Memory is cleared on assertion of pin RESET. RESET_N must not be asserted during sleep-wake cycles unless the intention is to clear Register Memory.

The register values to be stored in the memory, must be programmed at least once when the core power supplies are turned-on. This means that the delay reduction can be seen only from the second sleep-wake cycle. The state transition diagram below illustrates the same.

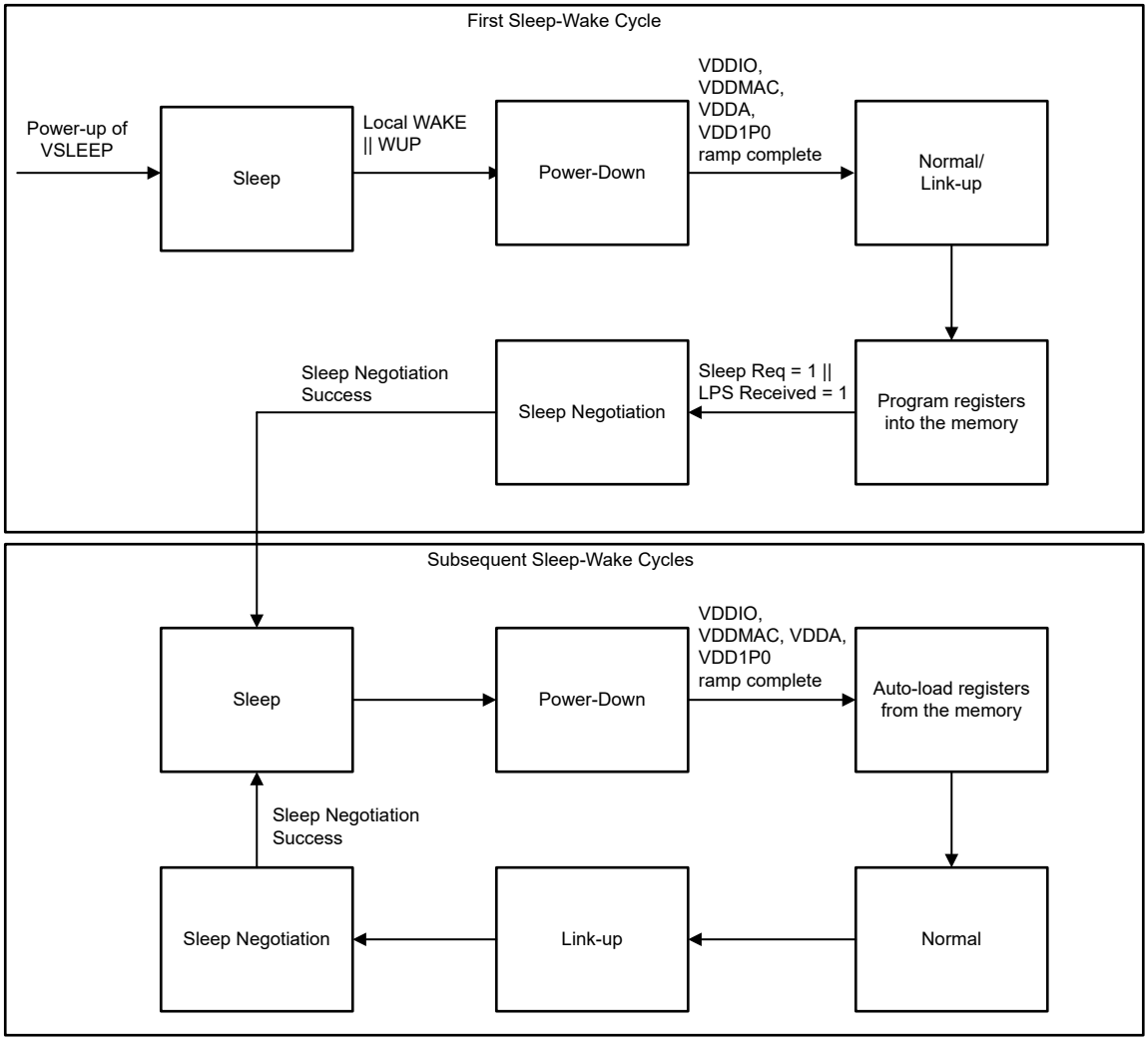


Figure 7-8. Fast Wake-Up State Machine

Programming registers into the memory can be done any time before next sleep-negotiation either during link-up, standby mode, normal mode or during communication. Programming registers into the memory can be done even during subsequent sleep-wake cycles.

Procedure To Program The Memory:

- Power-Up VSLEEP. PHY goes into sleep state.
- Let the PHY wake-up from sleep using local or remote wake.
- Power-up core power supplies (VDDIO, VDDMAC, VDDA, VDD1P0)
- Let SoC boot-up.
- Program registers of the PHY and let the PHY link-up.
- Program register into the memory (any time during link-up or communication) by following the below sequence
  - Program the below registers in the same order to enable Fast Wake
    - 0x523 = 0x0001
    - 0x01D2 = 0x0004
    - 0x01D2 = 0x0014
    - 0x01D2 = 0x0004
    - Wait for at least 200 us
    - 0x01BE = 0x0560
  - For each register value to be stored, carry out the following sequence
    - 0x01BC = <Register Address to be stored>
    - 0x01BD = <Register Data to be stored>
    - 0x01BE = 0x0760
    - Wait for at least 200 us
- The memory is loaded and registers values are auto-loaded from the next wake cycle.

To clear the Memory at any point, assert pin reset (RESET_N = LOW) or program register 0x01BE = 0x0060.

7.3.3 PPM Monitor

DP83TC815-Q1 has an in-built PPM monitor to calculate frequency offset between any two internal clock sources or between an external clock source and any internal clock source. The PPM monitor is a continuous monitor which provides real-time frequency offset between the two clock sources.

PPM Monitor takes in a reference clock and compares the frequency offset with a monitor clock. Both reference clock and monitor clock can be selected from options of:

- 25MHz XI clock input
- Internal Leader transmit clock of 200MHz
- MDI Recovered clock of 200MHz
- External Clock input on GPIOs (LED_0, GPIO_5)
- PTP Trigger 0 Output
- SGMII Recovered Clock
- PLL clk of 250Mhz

Note

Highest Frequency Clock out of the two clock sources used for comparison, must be chosen as monitor clock. Max ratio between monitor clock frequency and reference clock frequency can be 5 (lesser the ratio, higher the accuracy). Minimum allowed frequency for Monitor CLK is 12.5Mhz.

Following software sequence can be used to read out frequency offset

- Step-1: Disable PPM monitor before configuring settings in below steps, by programming 0x01AF[13]= 0
- Step-2: Select Reference Clock and Monitor Clock by programming register fields 0x01AF[12:9], 0x01AF[8:5], 0x01AF[15:14]
- Step-3: Select refresh period of the ppm monitor (for example, 1ms, 10ms, 100ms, and so forth.) Monitor accuracy increases with refresh period. Refresh period must be Common Multiple of monitor clock period and reference clock period.
- Step-4: Program monitor clock count and reference clock count
  - {0x01A4, 0x01A3} = refresh period/monitor clock period
  - {0x01A6, 0x01A5} = refresh period/reference clock period

- Step-5: Enable PPM monitor by programming 0x01AF[13] = 1
- Step-6: Wait for at least one refresh period to complete, write 0x01AF[4] = 1 to latch the ppm monitor values and read status registers {0x01AE, 0x01AD}
  - If 0x01AE[15] = 0, ppm offset is negative, if 0x01AE[15] = 1, ppm offset is positive.
  - PPM offset of monitor clock = {0x01AE[14:0],0x01AD[15:0]}/ {0x01A4, 0x01A3}

Example - Configuring PPM Monitor:

Calculating PPM offset between 12.5MHz external clock (on GPIO5), XI input clock of 25MHz for a refresh period of 10ms

Table 7-9. Example Sequence for Configuring PPM Monitor

STEP	DESCRIPTION	PROGRAMMING	NOTES
1	Disable PPM Monitor	0x01AF = 0x0000	
2	Selecting reference clock (GPIO5 input) and monitor clock (XI clock input)	0x01AF = 0xC800	Enable PPM monitor and clock selection use the same register. Care must be taken not to overwrite other fields of the register
3	Select refresh period = 10ms	-	
4	Program monitor clock count and reference clock count	0x01A4 = 0x0003 0x01A3 = 0xD090 0x01A6 = 0x0001 0x01A5 = 0xE848	For 10ms refresh period, count for • 25MHz is 250000 • 12.5MHz is 125000
5	Enable PPM monitor	0x01AF = 0xE800	Enable PPM monitor and clock selection use the same register. Take care not to overwrite other fields of the register
6	Latch PPM value after at least one refresh period	0x01AF = 0xE810	To latch the PPM value to read registers.
7	Read PPM offset value registers	Read 0x01AE,0x01AD	For external clock of 12.5MHz + 0ppm, XI input of 25MHz+ 100ppm, read out values are 0x01AE = 0x8000 and 0x01AD = 0x0019
8	Calculate PPM offset	-	PPM offset = 0x0019/0x0003D090 = 1e-4 (100ppm)

Configuring Interrupt for PPM Monitor Unlock:

PPM monitor can also be used to give an unlock interrupt if the PPM of the monitor clock goes beyond configured thresholds.

Following software sequence can be used to configure interrupt thresholds

- Step-1: Disable PPM monitor before configuring settings in below steps, by programming 0x01AF[13]= 0
- Step-2: Choose PPM thresholds beyond interrupt has to be indicated
- Step-3: Calculate counter register thresholds
  - Threshold = Monitor clock count (value loaded in register 0x01A4, 0x01A3) * PPM threshold
- Step-4: Load values into the registers
  - Load positive PPM threshold in registers {0x01A8, 0x01A7} = Monitor Clock Count * positive PPM beyond which interrupt is flagged
  - Load negative PPM threshold in registers {0x01AA,0x01A9} = Monitor clock count - (Monitor Clock Count * negative PPM beyond which interrupt is flagged
- Step-5: (Optional) Enable interrupt indication on INT_N pin by programming 0x0017 = 0x0008. Status is available in bit 11 of register 0x0017 irrespective of whether indication on INT_N is enabled
- Step-6: Enable PPM monitor by programming 0x01AF[13] = 1
- Step-7: Wait for at least 1 refresh period and read status from 0x0017[11]

Example - Configuring PPM Monitor Interrupt:

Enabling Interrupt for previous example in Table 7-9 with PPM threshold chosen as 200ppm

Table 7-10. Example Sequence for Configuring PPM Monitor Interrupt

STEP	DESCRIPTION	PROGRAMMING	NOTES
1	Disable PPM Monitor	0x01AF[13] = 0	
2	Choose PPM threshold	-	Choosing 200ppm for this example
3	Calculate counter register threshold	-	Counter register threshold = $200*10^{-6}*$ 250000 = 50
4	Program clock counter register thresholds	0x01A8 = 0x0000 0x01A7 = 0x0032 0x01AA = 0x0003 0x01A9 = 0xD090	Loading counter threshold in registers {0x01A8,0x01A7} and {0x01AA,0x01A9}
5	Enable PPM interrupt indication on INT_N pin	0x0017 = 0x0008	
6	Enable PPM Monitor	0x01AF[13] =1	
7	Wait for at least 1 refresh period and read status	Read 0x0017[11]	

7.3.4 Clock Dithering

To reduce the emissions from clock and data switching, DP83TC815-Q1 supports clock dithering on internal system clocks and MAC interface clock, data pins. The frequency of clocks is modulated with time to spread out the signal energy and reduce emissions. Figure 7-9 shows the example of dithered clock frequency using triangular and sawtooth profile, with time.

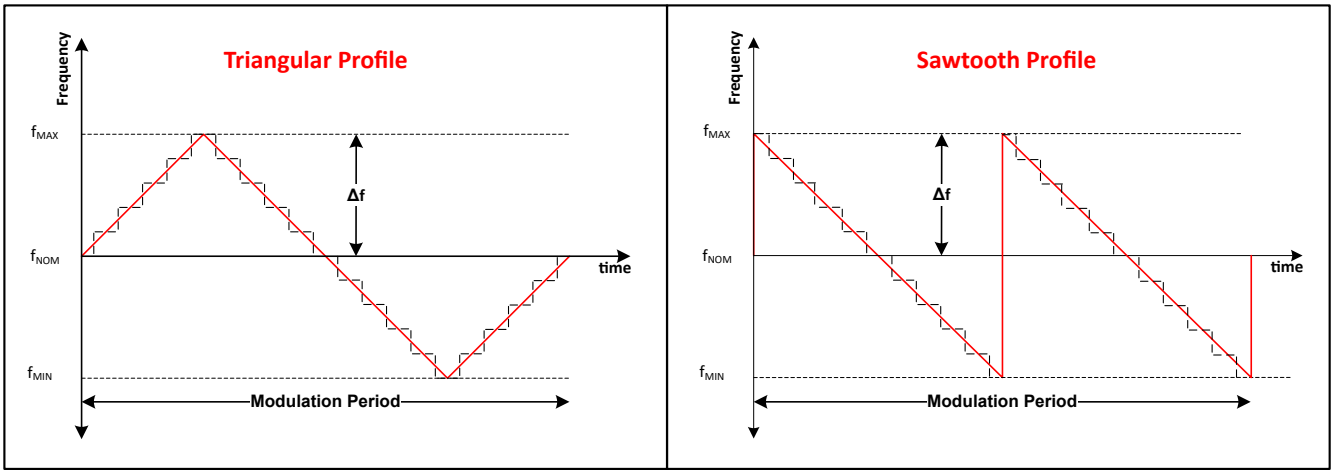


Figure 7-9. Clock Dithering Frequency Profiles

Dithering can be enabled and disabled using register 0x05A8. Separate options are available for enabling dithering of internal core clocks and MAC interface.

Note

Note: MAC interface dithering is only available for MII, RMII and RGMII interfaces. SGMII MAC interface outputs cannot be dithered.

To tweak the EMC performance, the following dithering options are available on DP83TC815-Q1

- **Dithering Profile:**
  - Triangular and Sawtooth profiles are available
- **Dithering Modulation Period:** Cycle time across which average of Δ(f) is 0.

  - EMC performance has higher improvement with higher modulation period.
- **Dithering Maximum Frequency Offset (Δ(f)):** Configure maximum ratio of frequency offset w.r.t average frequency of the clock
  - EMC performance has higher improvement with higher Δ(f)

The above options are available from programming using registers 0x05A1 and 0x05A8

Impact of Dithering MAC Interface:

Dithering of clocks results in shrinkage and elongation of clock period of MAC interface signals over the modulation period. This causes the Inter-Packet Gap between packets to shrink or elongate. The output clock period of MAC interface reference clock also shrinks or elongates. Table 7-11 shows the comparison of Inter-Packet Gap and RGMII MAC interface period.

Table 7-11. IPG and Clock Period Variation with Dithering

S.NO	Δf/f	DITHER MODULATION TIME	25MHz CYCLE SLIPs	IPG VARIATION	25MHz CLOCK PERIOD VARIATION
Sawtooth/Triangular					
1	1%	8.33 us	±1	±0.5 byte	±0.4ns
2	2%	8.33 us	±2	±1 byte	±0.8ns
3	2%	16.66 us	±4	±2 byte	±0.8ns

When MAC interface dithering is enabled, the compliance of Ethernet MAC to IPG shrinkage and Clock period variation must be made sure.

7.3.5 Output Slew Control

DP83TC815-Q1 provides options to control the slew rate of MAC interface output pins and GPIOs. Table below shows the options available for each of these output pins.

Table 7-12. Output Slew Control Options

S.NO	PINS	SLEW RATE OPTIONS	CONTROL REGISTER
1	RX_CLK RX_D0 RX_D1 RX_D2 RX_D3 RX_CTRL RX_ER	Slew Mode -1 (Slowest) Slew Mode - 2 Slew Mode - 3 Slew Mode - 4 Slew Mode - 5 Slew Mode - 6 Slew Mode - 7 (Fastest)	0x0456[9:5]
2	TX_CLK		0x0456[4:0]
3	CLKOUT		0x0460[12:8]
4	GPIO_3		0x0461[4:0]
5	GPIO_4		0x0461[12:8]
6	LED_1		0x0460[4:0]
7	LED_0 GPIO_5	Fast Mode Slow Mode	0x455[13:9]

Table 7-13 - Table 7-15 illustrate how typical Rise/Fall Time changes for varying Slew Mode, CLOAD, and VDDIO.

Table 7-13. Rise/Fall time vs Slew Mode for CLOAD = 5pF, VDDIO = 3.3V

Slew Mode	Rise/Fall Time
1	4.1ns

Table 7-13. Rise/Fall time vs Slew Mode for CLOAD = 5pF, VDDIO = 3.3V (continued)

Slew Mode	Rise/Fall Time
2	3.5ns
3	3.0ns
4	2.7ns
5	2.4ns
6	2.0ns
7	1.6ns

Table 7-14. Rise/Fall time vs CLOAD for CLOAD = 5pF, Slew Mode = 4

CLOAD	Rise/Fall Time
5pF	2.7ns
15pF	3.4ns
25pF	4.2ns

Table 7-15. Rise/Fall time vs VDDIO for CLOAD = 5pF, Slew Mode = 4

VDDIO	Rise/Fall Time
3.3V	2.7ns
2.5V	2.4ns
1.8V	2.2ns

7.3.6 Diagnostic Tool Kit

The DP83TC815-Q1 diagnostic tool kit provides mechanisms for monitoring normal operation, device-level debugging, system-level debugging, fault detection, and compliance testing. This tool kit includes a built-in self-test with PRBS data, various loopback modes, Signal Quality Indicator (SQI), Time Domain Reflectometry (TDR), undervoltage monitor, overtemperature monitor, electrostatic discharge monitor, and IEEE 802.3bw test modes.

7.3.6.1 Signal Quality Indicator

When the DP83TC815-Q1 is active, the Signal Quality Indicator can be used to determine the quality of link based on SNR readings made by the device. SQI is presented as a 8-level indication. Signal quality indication is accessible through register 0x871. SQI is continuously monitored by the PHY to allow for real-time link signal quality status.

Bits[3:1] in register 0x871 provide SQI value while bits [7:5] provide the worst SQI value since the last read. The SQI value reported in register 0x871[3:1] map directly to the SQI levels required by Open Alliance.

Table 7-16. Signal Quality Indicator

REG 0x871[3:1]	OPEN ALLIANCE SQI LEVEL	LINK QUALITY
0x0	0 (Worst)	Poor/ No Link
0x1	1	
0x2	2	
0x3	3	
0x4	4	Good / Excellent Link
0x5	5	
0x6	6	
0x7	7 (Best)	

7.3.6.2 Electrostatic Discharge Sensing

Electrostatic discharge is a serious issue for electronic circuits and if not properly mitigated can create short-term issues (signal integrity, link drops, packet loss) as well as long-term reliability faults. The DP83TC815-Q1 has

robust integrated ESD circuitry and offers an ESD sensing architecture. ESD events can be detected on MDI pins independently for further analysis and debug.

Additionally, the DP83TC815-Q1 provides an interrupt status flag; *Register 0x12[11]* is set when an ESD event is logged. This interrupt can be routed to the INT_N pin using bit[3] of the same register. *Register 0x442[14:9]* store the number of ESD events that have occurred since power-up. Hardware and software resets are ignored by the ESDS register to prevent unwarranted clearing.

7.3.6.3 Time Domain Reflectometry

Time domain reflectometry helps determine the quality of the cable, connectors and terminations in addition to estimating OPEN and SHORT faults along a cable. The DP83TC815-Q1 transmits a test pulse down the attached twisted-pair cable. Transmitted pulses continue down the cable and reflect from each imperfection and fault, allowing the device to measure the time to return and strength (amplitude) of all reflections. This technique enables the DP83TC815-Q1 to identify cable OPENs and SHORTs.

TDR is activated by setting bit[15] in register 0x1E. The procedure is outlined in Table 7-17. Note that the Link Partner connected to the PHY must be silent. Link is down during TDR execution.

Table 7-17. TDR Run Procedure

SEQUENCE	DESCRIPTION	REGISTER READ/WRITE
Step 1: For DP83TC815-Q1 as leader	Force the link-down by writing register and enable link-partner to go silent. In case of valid open and short cable faults, TDR still functions well without step 1. For good cable case, TDR register 0x001E can show *Fail* on bypassing this step.	Write Reg[0x1834] = 0x8001 To make leader go silent.
Step 1: ForDP83TC815-Q1as follower	Force the link-down by writing register and enable link-partner to go silent. In case of valid open and short cable faults, TDR still works fine without step 1. For good cable case, TDR register 0x001E can show *Fail* on bypassing this step.	If DP83TC815-Q1 is link partner, write reg[0x1834] = 0x8001 on the link partner to make it silent. If other PHY is used, contact the vendor for register write to make link partner silent
Step 2	TDR configuration: Pre-run	Reg[0x0523] = 0x0001 Reg[0x04DF] = 0x0003 Reg[0x0827] = 0x3800 Reg[0x0301] = 0x1700 Reg[0x0302] = 0x0045 Reg[0x0303] = 0x042D Reg[0x0304] = 0x0026 Reg[0x0305] = 0x0015 Reg[0x001F] = 0x4000 Reg[0x0523] = 0x0000 Reg[0x001F] = 0x0000 Reg[0x001E]= 0x8000
Step 3	Start TDR	Reg[0x001E(15)] = 1
Step 4	Wait for 100ms (must be sufficient for TDR to converge for maximum cable length)	
Step 5	Read 0x001E[1:0] = [TDR done : TDR fail]. Value must be [1,0]. Fault type and locations are valid only if this correct value is read. Value other than [1,0] means that there is some noise on the line which is causing TDR to fail.	

Table 7-17. TDR Run Procedure (continued)

SEQUENCE	DESCRIPTION	REGISTER READ/WRITE	
Step 6	Fault type and location is read.	Read Reg 0x0310 for fault status and fault type. For fault types:	
		TDR_TC-1 Reg 0x0310[7] = peak_detect	
		0b	Fault not detected
		1b	Fault detected
		TDR_TC-1 Reg 0x0310[6] = peak_sign	
		0b	short
		1b	open
		**peak_sign only valid if Fault detected in cable. If a valid fault detected: register 0x0310[5:0] = is the fault location in meters.	

7.3.6.4 Voltage Sensing

Voltage Sensing Steps Summary

The DP83TC815-Q1 offers sensors for monitoring voltage at the supply pins. Undervoltage monitoring are always active in the DP83TC815-Q1 by default. If an undervoltage condition is detected, interrupt status flag is set in register 0x0013. These interrupts can also be optionally routed to the INT pin using the same register.

- Step 1: Program register 0x0469 = 0x8324 ; Initial configuration of monitor
- Step 2: Program register 0x046A = 0x0096 and then 0x46A=0x0093; Enables and refreshes monitor
- Step 3: Program register 0x0013 = 0x00C0, Enable over voltage and under voltage interrupts
- Step 4: Configure register 0x0468 with the corresponding setting to select the required sensor.

Table 7-18. Voltage Sensor Register Selection

SENSOR	0x0468 REGISTER SETTING
VDDA	0x0920
VSLEEP	0x1920
VDDMAC	0x2920
VDDIO	0x3920
VDD1P0	0x5920

- Step 5: Read register 0x047B[14:7] and convert this output code to decimal.
- Step 6: Use the output code in the following equations to get the absolute value of the sensor. Refer to Table 7-19 table for constant values for corresponding sensors.
  - vdda_value = 3.3 + (vdda_output_code – vdda_output_mean_code)*slope_vdda_sensor
  - vsleep_value = 3.3 + (vsleep_output_code – vsleep_output_mean_code)*slope_vsleep_sensor
  - vddmac_value = 3.3 + (vddmac_output_code – vddmac_output_mean_code)*slope_vddmac_sensor
  - vddio_value = 3.3 + (vddio_output_code – vddio_output_mean_code)*slope_vddio_sensor
  - vdd1p0_value = 1.0 + (vdd1_output_code – vdd1_output_mean_code)*slope_vdd1_sensor

Table 7-19. Voltage Sensors Constant Values

SENSOR	CONSTANT	VALUE
VDDA/VSLEEP	vdda_output_mean_code	125.13
	slope_vdda_sensor	0.00869
VDDMAC/VDDIO	vddio_output_mean_code	201.62
	slope_vddio_sensor	0.015387

Table 7-19. Voltage Sensors Constant Values (continued)

SENSOR	CONSTANT	VALUE
VDD1P0	vdd1_output_mean_code	125.17
	slope_vdd1_sensor	0.00263

Over and Undervoltage Thresholds

There are two over voltage thresholds, *over_up_th* and *over_low_th*. When the monitor read value goes above *over_up_th,* the interrupt is asserted high. After the interrupt is asserted high, the interrupt is asserted low only if the monitor read value goes below *over_low_th* .

There are two under voltage thresholds, *under_up_th* and under_low_th. When the monitor read value goes below *under_low_th,* the interrupt is asserted high. After the interrupt is asserted high, the interrupt is asserted low only if the monitor read value goes above *under_up_th*

Table 7-20. Over Voltage Register Thresholds

MONITOR	over_up_th	over_low_th	under_up_th	under_low_th
VDD1P0	0x057A<7:0>	0x057A<15:8>	0x057B<7:0>	0x057B<15:8>
VDDMAC 1.8V	0x0483<7:0>	0x0483<15:8>	0x0484<7:0>	0x0484<15:8>
VDDMAC 2.5V	0x0481<7:0>	0x0481<15:8>	0x0482<7:0>	0x0482<15:8>
VDDMAC 3.3V	0x046F<7:0>	0x046F<15:8>	0x0470<7:0>	0x0470<15:8>
VDDIO 1.8V	0x047F<7:0>	0x047F<15:8>	0x0480<7:0>	0x0480<15:8>
VDDIO 2.5V	0x047D<7:0>	0x047D<15:8>	0x047E<7:0>	0x047E<15:8>
VDDIO 3.3V	0x0471<7:0>	0x0471<15:8>	0x0472<7:0>	0x0472<15:8>
VSLEEP	0x046D<7:0>	0x046D<15:8>	0x046E<7:0>	0x046E<15:8>
VDDA	0x046B<7:0>	0x046B<15:8>	0x046C<7:0>	0x046C<15:8>

7.3.6.5 Temperature Sensing

Temperature Sensing Steps Summary

The DP83TC815-Q1 offers sensors for monitoring temperature at the supply pins. Over temperature monitoring is always active in the DP83TC815-Q1 by default. If an over temperature condition is detected, interrupt status flag is set in register 0x0013. These interrupts can also be optionally routed to the INT pin using the same register.

- Step 1: Program register 0x469=0x8324; Initial configuration of monitor.
- Step 2: Program registers 0x046A = 0x0096, 0x046A = 0x0093; Enable Monitors
- Step 3: Configure over temperature interrupt settings. See the Interrupt Overtemperature Thresholds section for more details. (optional)
- Step 4: Program register 0x0013=0x008; Enable over temperature interrupt (optional)
- Step 5: Set register 0x468=0x4920 to select the temperature sensor.
- Step 6: Read register 0x047B[14:7] and convert this output code to decimal.
- Step 7: Use the output code in the following equation to get the absolute value of the sensor:

  temp_value = 25 + (temp_output_code – temp_output_mean_code) × slope_temp_sensor

Table 7-21. Temperature Sensors Constant Values

SENSOR	CONSTANT	VALUE
Temperature	temp_output_mean_code	90
	slope_temp_sensor	1.0839

  – To detect over temperature use the interrupt register, continuously read 0x13[11].

– Pin 2 can also be configured as an interrupt pin through register 0x11. When configured correctly, pin 2 is asserted LOW when the over temperature condition occurs.0x13[11].

Over Temperature Threshold Register

The over temperature threshold register has two fields, *over_up_th* and *over_low_th*. When the monitor read value goes above *over_up_th,* the interrupt is asserted high. After the interrupt is asserted high, the interrupt is asserted low only if the monitor read value goes below *over_low_th* .

Table 7-22. Over Temperature Register Thresholds

MONITOR	over_up_th	over_low_th
Temperature	0x0473<7:0>	0x0473<15:8>

Example of How to Configure Over Temperature Threhsholds

- Step 1: Decide *over_up_th* and *over_low_th* temperatures.
- over_up temperature: 130°C
- over_low temperature: 140°C
- Step 2: Subsitute the temperature values into the equation and solve for temp_output_code.
  - temp_value = 25 + (temp_output_code – temp_output_mean_code) × slope_temp_sensor
  - 130^{o}C = 25 + (temp_output_code_130 – 81.26) × 1.0839
  - 140^{o}C = 25 + (temp_output_code _140 – 81.26) × 1.0839
  - temp_output_code_130 = 187
  - temp_output_code_140 = 178
- Step 3: Set the register bits *over_up_th* to 187 and *over_low_th* to 178.

Note

The DP83TC815-Q1 does not inlude a hardware calibration. Accuracy of the temperature sensor is about ±25°C for a part and ±11°C across parts.

7.3.7 BIST and Loopback Modes

DP83TC815-Q1 incorporates a data-path's Built-In-Self-Test (BIST) to check the PHY level and system level data-paths. BIST has following integrated features which make the system level data transfer tests (through-put etc) and diagnostics possible without relying on MAC or external data generator hardware/software.

The following features are available in the DP83TC815-Q1 which can be used for easy evaluation.

1. Loopback modes
2. Data Generator
   a. Customizable MAC packets generator
   b. Transmitted packet counter
   c. PRBS stream generator
3. Data Checker
   a. Received MAC packets error checker
   b. Received packet counter: Counts total packets received and packets received with errors
   c. PRBS lock and PRBS error checker

7.3.7.1 Data Generator and Checker

DP83TC815-Q1 supports inbuilt Pseudo-random data generator and checker which can be used in conjunction with Loopback modes to check the data path. Data generator can be programmed to generate either user defined MAC packets or PRBS stream.

Following parameters of generated MAC packets can be configured (refer to registers<0x061B>, register<0x061A>, and register<0x0624> for required configuration):

- Packet Length

- Inter-packet gap
- Defined number of packets to be sent or continuous transmission
- Packet data-type: Incremental/Fixed/PRBS
- Number of valid bytes per packet

7.3.7.2 xMII Loopback

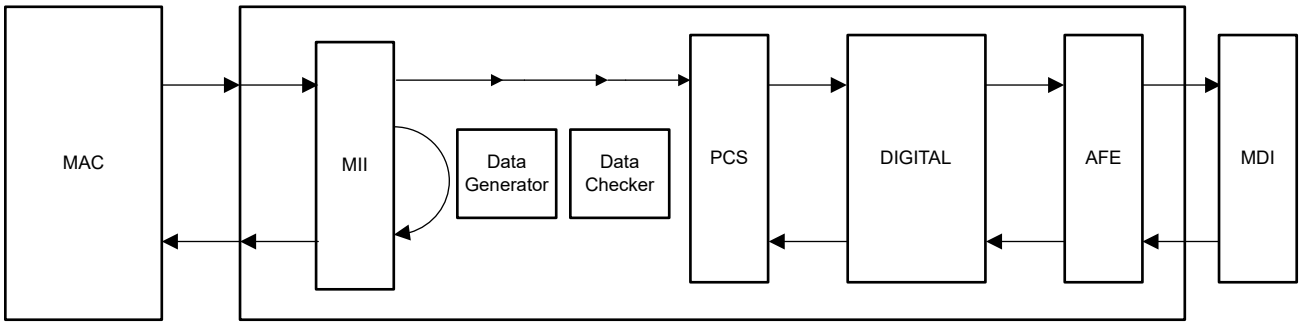


Figure 7-10. xMII Loopback Without Data Generator

xMII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in xMII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83TC815-Q1 to the RX pins where it can be checked by the MAC. There is no link indication when in xMII loopback.

Enable Loopback

Write register 0x0000 = 0x6100

Enable data generator/checker for MAC side

Data is generated externally on the MAC TX pins.

Use the following register settings to enable checker depending on the MAC interface mode.

- For RGMII, write register 0x0619 = 0x1004
- For SGMII, write register 0x0619 = 0x1114
- For RMII, write register 0x0619 = 0x1224
- For MII, write register 0x0619 = 0x1334

Check incoming data from MAC side

Data can be verified at MAC interface RX pins.

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Not applicable as data is generated externally on the MAC interface TX pins.

Check data for Cable side

Not applicable as PRBS stream checker works with only internal PRBS generator.

Other system requirements

Generated data is going to cable side.

7.3.7.3 PCS Loopback

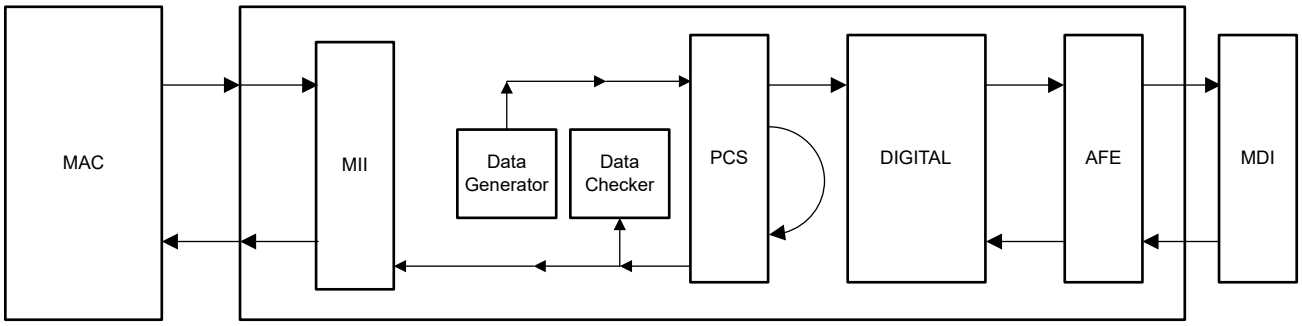


Figure 7-11. PCS Loopback With Data Generator

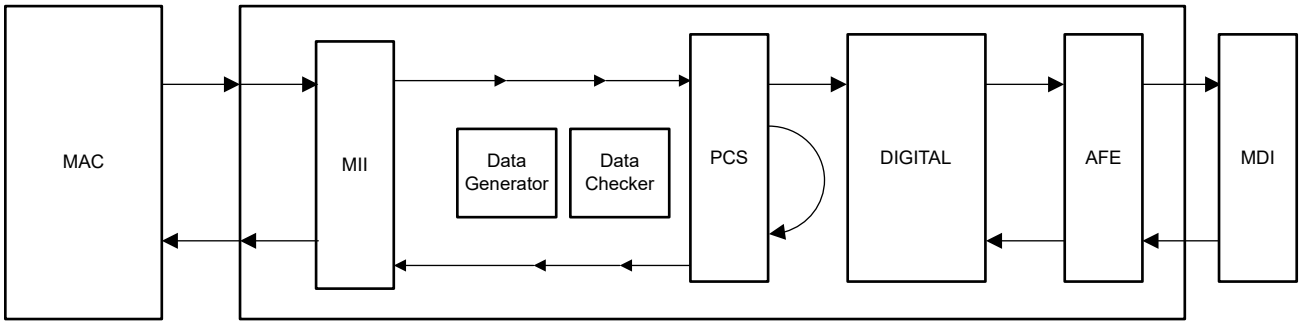


Figure 7-12. PCS Loopback Without Data Generator

PCS Loopback loops back data prior to the data exiting the PCS and entering the PMA. Data received from the MAC on the transmit path is brought through the digital block within the PHY where the data is then routed back to the MAC through the receive path. The DP83TC815-Q1 receive PMA circuitry is configured for isolation to prevent contention.

Enable Loopback

Write register 0x0552 = 0x0000

Write register 0x0016 = 0x0102

Enable data generator/checker for MAC side

Write register 0x0619 = 0x1555

Write register 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Write register 0x0619 = 0x0557

Write register 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1

2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other system requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.7.4 Digital Loopback

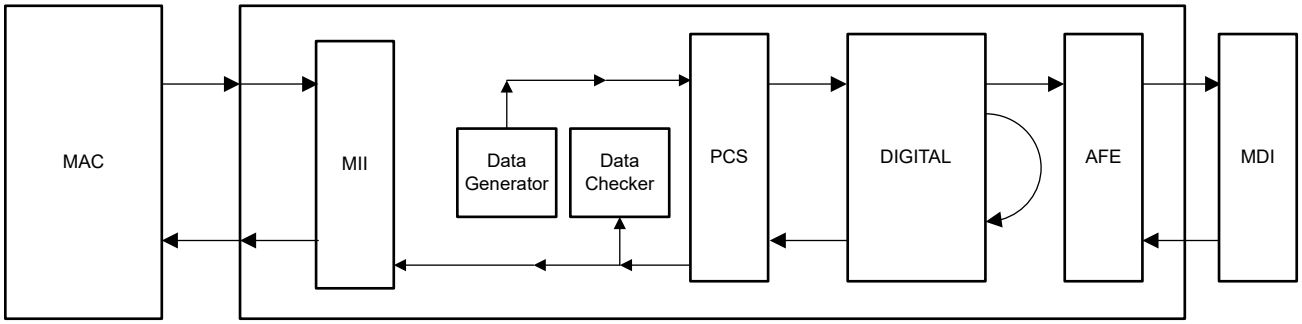


Figure 7-13. Digital Loopback With Data Generator

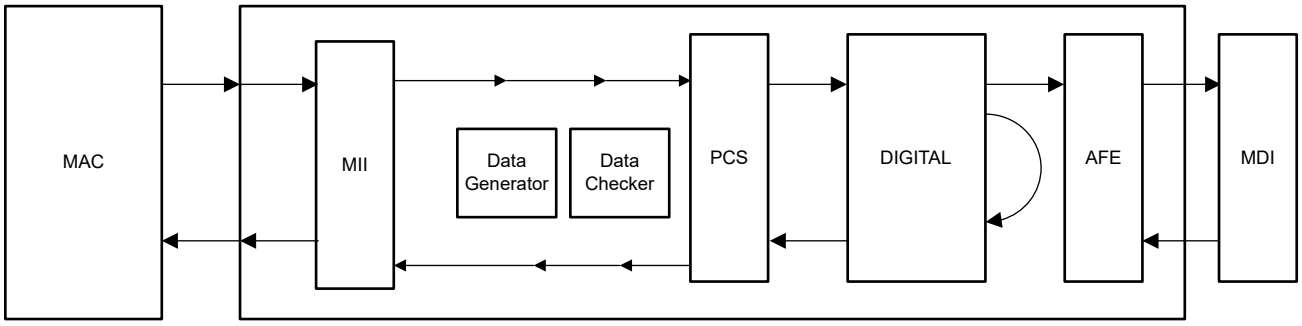


Figure 7-14. Digital Loopback Without Data Generator

Digital Loopback loops back data prior to exiting the Digital and entering the AFE. Data received from the MAC on the transmit path is brought through the digital block within the PHY where the data is then routed back to the MAC through the receive path. The DP83TC815-Q1 receive Analog circuitry is configured for isolation to prevent contention.

Enable Loopback

Write register 0x0868 = 0x085A

Write register 0x04DF = 0x0006

Write register 0x0016 = 0x0104

Enable data generator/checker for MAC side

Write register 0x0619 = 0x1555

Write register 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Write register 0x0619 = 0x0557

Write register 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other system requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.7.5 Analog Loopback

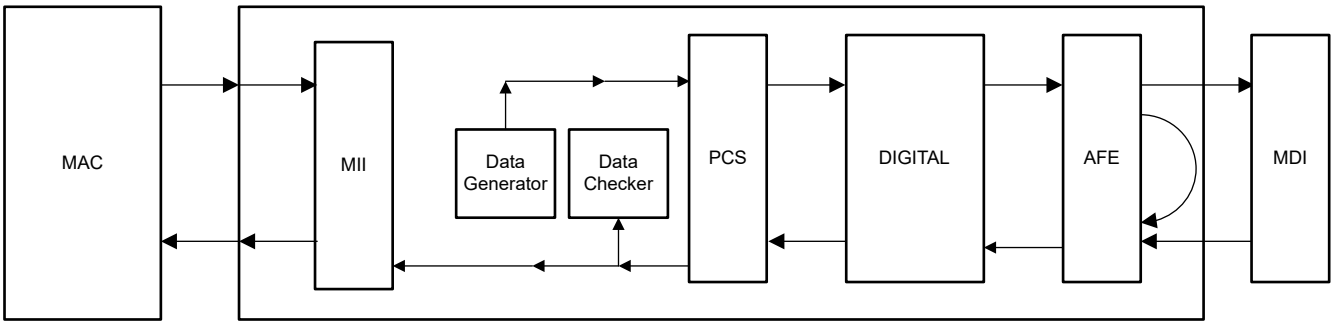


Figure 7-15. Analog Loopback With Data Generator

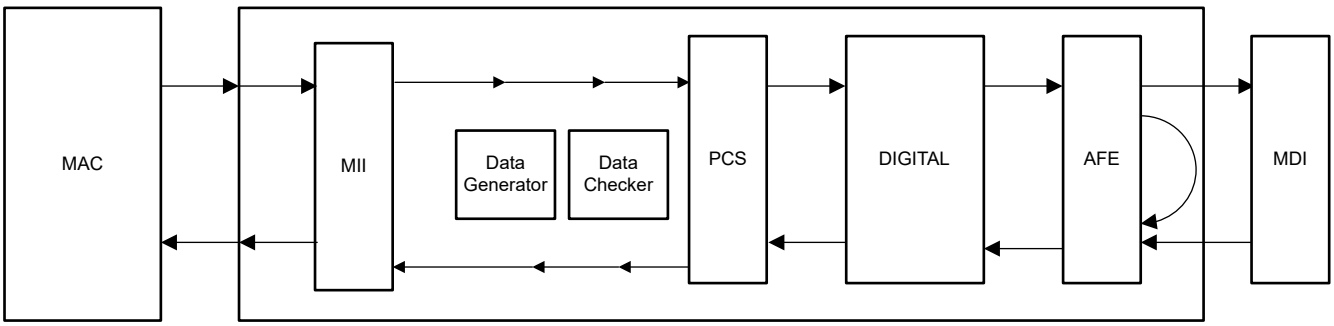


Figure 7-16. Analog Loopback Without Data Generator

Analog Loopback uses the echoed signals from the unterminated MDI and decodes these signals in the Hybrid to return the data to the MAC.

Enable Loopback

Write registers:

- 0x0868 = 0x085A
- 0x04DF = 0x0006

- 0x0016 = 0x0108
- 0x0802 = 0x4A47
- 0x001F = 0x4000

Enable data generator/checker for MAC side

Write registers:

- 0x0619 = 0x1555
- 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Write registers:

- 0x0619 = 0x0557
- 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other system requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.7.6 Reverse Loopback

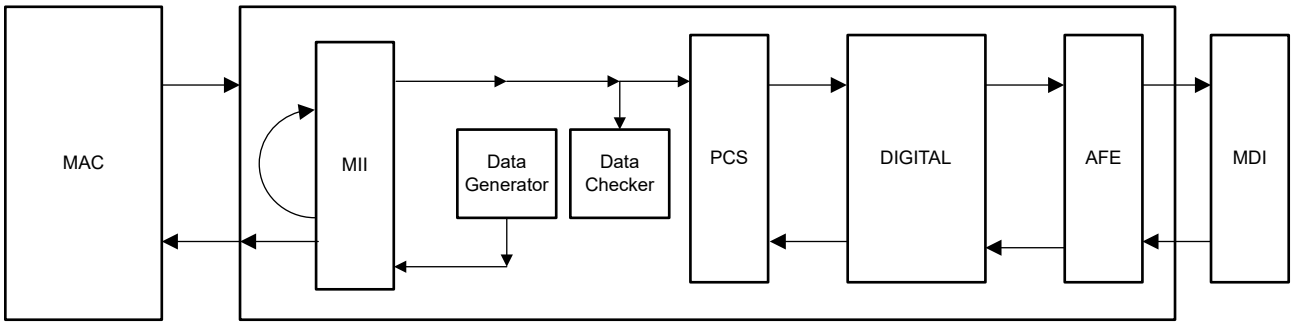


Figure 7-17. Reverse Loopback With Data Generator

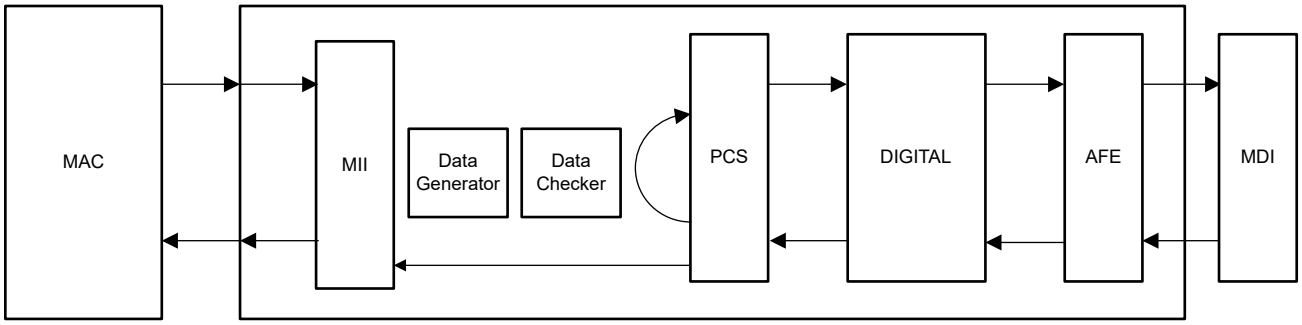


Figure 7-18. Reverse Loopback Without Data Generator

Reverse Loopback receives data on the MDI and passes the data through the entire receive block where the data is then looped back within the PCS layer to the transmit block. The data is transmitted back out on the MDI to the attached Link Partner. To avoid contention, MAC transmit path is isolated.

Enable Loopback

Write register 0x0016 = 0x0110

Enable data generator/checker for MAC side

Use the following register settings to enable checker depending on the MAC interface mode.

- For RGMII, write register 0x0619 = 0x1004
- For SGMII, write register 0x0619 = 0x1114
- For RMII, write register 0x0619 = 0x1224
- For MII, write register 0x0619 = 0x1334

Write register 0x0624 = 0x55BF

Check incoming data from MAC side

Data can also be checked internally by reading registers 0x063C, 0x063D, 0x063E

Enable data generator/checker for Cable side

Write register 0x0619 = 0x0557

Write register 0x0624 = 0x55BF

Check data for Cable side

1. Write register 0x0620[1] = 1'b1
2. Read register 0x620
   a. Bit [7:0] = Number of errors bytes received
   b. Bit [8] = PRBS checker lock status on incoming data (1'b1 indicates lock)

Repeat steps 1 and 2 to continuously check error status of incoming data stream.

Other system requirements

Data generate by the internal PRBS is transmitted over the MDI and the MAC interface.

7.3.8 Compliance Test Modes

Note

It is necessary to use the register settings outlined in TI Application Note SDAA127 to achieve desired OA compliance performance. To obtain the Application Note contact TI.

There are four PMA compliance test modes required in IEEE 802.3bw, sub-clause 96.5.2, which are all supported by the DP83TC815-Q1. These compliance test modes include: transmitter waveform Power Spectral Density (PSD) mask, amplitude, distortion, 100BASE-T1 Leader jitter, 100BASE-T1 Follower jitter, droop, transmitter frequency, frequency tolerance, return loss, and mode conversion.

TX_TCLK can be routed to CLKOUT/LED_1 pin for 100BASE-T1 Follower Jitter measurement. This can be enabled via register 0x45F. The device must be configured in Follower mode.

7.3.8.1 Test Mode 1

Test mode 1 evaluates transmitter droop. In test mode 1, the DP83TC815-Q1 transmits '+1' symbols for a minimum of 600ns followed by '–1' symbols for a minimum of 600ns. This pattern is repeated continuously until the test mode is disabled.

Test mode 1 is enabled by setting bits[15:13] = 0b001 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.8.2 Test Mode 2

Test mode 2 evaluates the transmitter 100BASE-T1 Leader mode jitter. In test mode 2, the DP83TC815-Q1 transmits a {+1,-1} data symbol sequence. The transmitter synchronizes the transmitted symbols from the local reference clock.

Test mode 2 is enabled by setting bits[15:13] = 0b010 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.8.3 Test Mode 4

Test mode 4 evaluates the transmitter distortion. In test mode 4, the DP83TC815-Q1 transmits the sequence of symbols generated by Equation 1:

$$g(x) = 1 + x^9 + x^{11} \quad (1)$$

The bit sequences, x0n and x1n, are generated from combinations of the scrambler in accordance to Equation 2 and Equation 3:

$$'x0_n = Scr_n[0] \quad (2)$$

$$x1_n = Scr_n[1] \wedge Scr_n[4] \quad (3)$$

Example streams of the 3-bit nibbles are shown in Table 7-23.

Table 7-23. Transmitter Test Mode 4 Symbol Mapping

x1n	x0n	PAM3 SYMBOL
0	0	0
0	1	+1
1	0	0
1	1	–1

Test mode 4 is enabled by setting bits[15:13] = 0b100 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.3.8.4 Test Mode 5

Test mode 5 evaluates the transmitter PSD mask. In test mode 5, the DP83TC815-Q1 transmits a pseudo-random sequence of PAM3 symbols.

Test mode 5 is enabled by setting bits[15:13] = 0b101 in MMD1_PMA_TEST_MODE_CTRL Register (0x1836).

7.4 Device Functional Modes

7.4.1 Power Modes

DP83TC815-Q1 supports different Power Modes including functional modes and low power modes like Stand-by Mode, TC10 Sleep, IEEE Power down. The following figure shows the state transition diagram between these power modes.

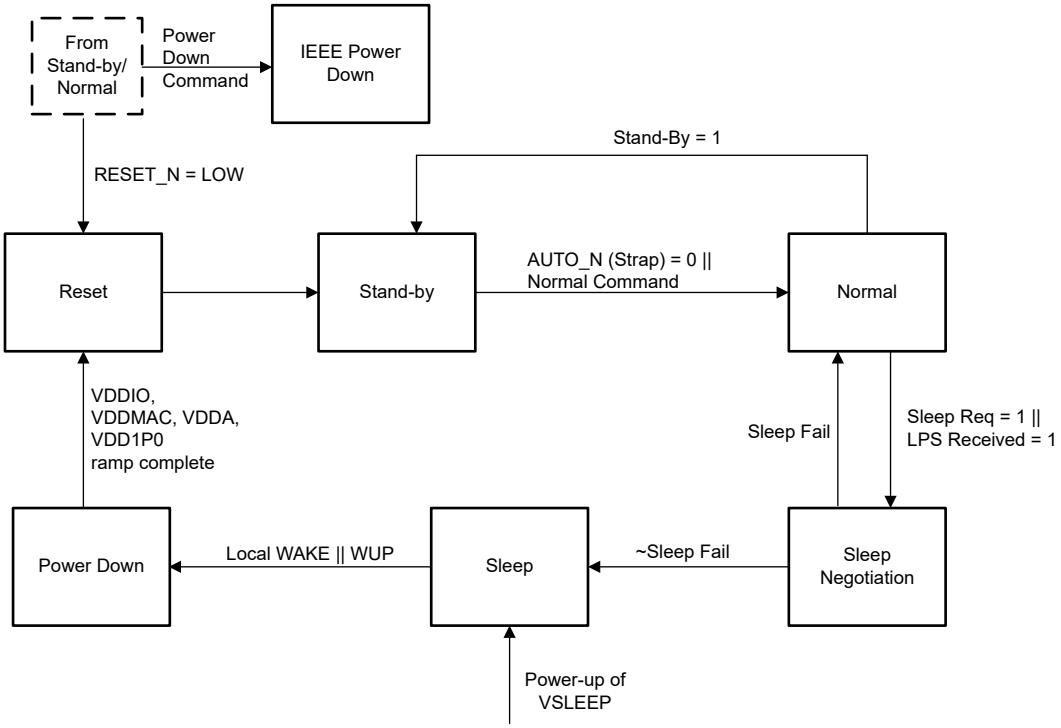


Figure 7-19. Power State Diagram

7.4.1.1 Power Down

When any of the supply rails are below the POR threshold, the PHY is in a power-down state. All digital IOs remain in high impedance states and analog blocks are disabled. PMA termination is not present when powered down.

Table 7-24. POR Thresholds

SUPPLY	POR THRESHOLD
VDDA/VDDMAC/VDDIO/VSLEEP	0.6V
VDD1P0	0.25V

7.4.1.2 Reset

Reset is activated upon power-up, when $\overline{\text{RESET}}$ is pulled LOW (for the minimum reset pulse time) or if hardware reset is initiated by setting bit[15] in register 0x1F. All digital circuitry is cleared along with register settings during reset. Once reset completes, device bootstraps are re-sampled and associated bootstrap registers are set accordingly. PMA termination is not present in reset.

7.4.1.3 Standby

The device (100BASE-T1 Leader mode only) automatically enters into standby post power-up and reset so long that all supplies including VSLEEP are available and the device is bootstrapped for managed operation.

In standby, all PHY functions are operational except for PCS and PMA blocks. The PMA termination is also not present. Link establishment is not possible in standby and data cannot be transmitted or received. SMI functions are operational and register configurations are maintained.

If the device is configured for autonomous operation through bootstrap setting, the PHY automatically switches to normal operation once POR is complete.

7.4.1.4 Normal

Normal mode can be entered from either autonomous or managed operation. When in autonomous operation, the PHY automatically tries to establish a link with a valid Link Partner once POR is complete.

In managed operation, SMI access is required to allow the device to exit standby, commands issued through the SMI allow the device to exit standby and enables both the PCS and PMA blocks. All device features are operational in normal mode.

Autonomous operation can be enabled through SMI access by setting register 0x18B[6] = '1'. Note that this bit is auto-cleared after link up.

7.4.1.5 Sleep

Once in sleep mode, all PHY blocks are disabled except for energy detection. All register configurations are lost in sleep mode. No link can be established, data cannot be transmitted or received and SMI access is not available when in sleep mode.

It is recommended to cut-off all power supplies except VSLEEP when in sleep mode to achieve lowest power consumption.

7.4.2 Media Dependent Interface

7.4.2.1 100BASE-T1 Leader and 100BASE-T1 Follower Configuration

100BASE-T1 Leader and 100BASE-T1 Follower are configured using either hardware bootstraps or through register access.

LED_0 controls the 100BASE-T1 Leader and 100BASE-T1 Follower bootstrap configuration. By default, 100BASE-T1 Follower mode is configured because there is an internal pulldown resistor on LED_0 pin. If 100BASE-T1 Leader mode configuration through hardware bootstrap is preferred, an external pullup resistor is required.

Additionally, bit[14] in the MMD1_PMA_CTRL_2 Register (Address 0x1834) controls the 100BASE-T1 Leader and 100BASE-T1 Follower configuration. When this bit is set, 100BASE-T1 Leader mode is enabled.

7.4.2.2 Auto-Polarity Detection and Correction

During the link training process, the DP83TC815-Q1 100BASE-T1 Follower device is able to detect polarity reversal and automatically corrects the error. If polarity reversal is detected, the 100BASE-T1 Follower inverts its own transmitted signals to account for the error and ensure compatibility with the 100BASE-T1 Leader. Polarity at the 100BASE-T1 Leader is always observed as correct because polarity detection and correction is handled entirely by the 100BASE-T1 Follower.

Auto-polarity correction can be disabled in cases where it is not required. Disabling of auto-polarity correction is achieved through register 0x0553.

7.4.2.3 Jabber Detection

The jabber function prevents the PCS Receive state machine from locking up into a DATA state if the End-of-Stream Delimiters, ESD1 and ESD2, are never detected or received within the rcv_max_timer. When the maximum receive DATA state timer expires, the PCS Receive state machine is reset and transitions into IDLE state. IEEE 802.3bw specifies that jabber timeout be set to 1.08 ms ± 54 µs. By default, jabber timeout in the DP83TC815-Q1 is set to 1.1 ms. This timer is configurable in Register 0x496[10:0].

7.4.2.4 Interleave Detection

The interleave function allows for the DP83TC815-Q1 to detect and de-interleave the serial stream from a connected link partner. The two possible interleave sequences of ternary symbols include: (TA_n, TB_n) or (TB_n, TA_n).

7.4.3 MAC Interfaces

7.4.3.1 Media Independent Interface

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2015 clause 22. The PHY has internal series termination resistors on MII output pins including TX_CLK output when the PHY is operating in MII mode. In this mode, it is recommended to not leave the MII-TX pins floating or High-Z.

The MII signals are summarized in Table 7-25:

Table 7-25. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_EN, TX_ER
	RX_DV, RX_ER
Clock Signals	TX_CLK
	RX_CLK

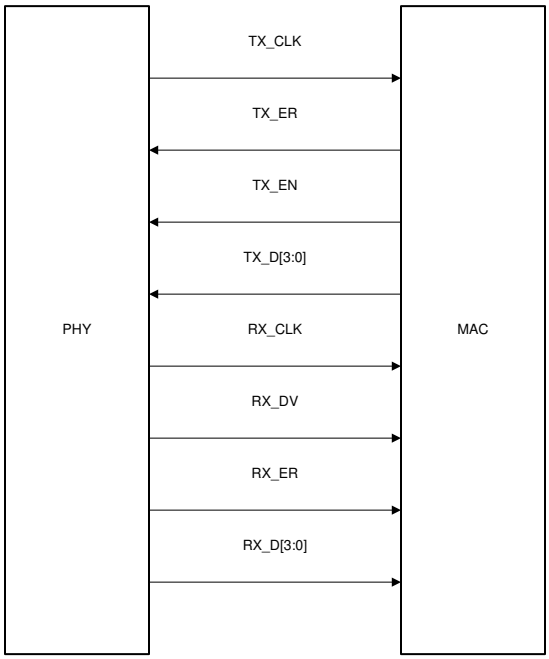


Figure 7-20. MII Signaling

Table 7-26. MII Transmit Encoding

TX_EN	TX_ER	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

Table 7-27. MII Receive Encoding

RX_DV	RX_ER	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000	Normal Inter-Frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

7.4.3.2 Reduced Media Independent Interface

The DP83TC815-Q1 incorporates the Reduced Media Independent Interface (RMII) as defined in the RMII Revision 1.2 and 1.0 from the RMII consortium. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3u MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII.

The DP83TC815-Q1 offers two types of RMII operations: RMII Follower and RMII Leader. In RMII Follower Mode, the DP83TC815-Q1 operates off a 50MHz CMOS-level oscillator, which is either provided by the MAC or synchronous to the MAC reference clock. In RMII Leader operation, the DP83TC815-Q1 operates off of either a 25MHz CMOS-level oscillator connected to XI pin or a 25MHz crystal connected across XI and XO pins. When bootstrapping to RMII Leader Mode, a 50MHz output clock is automatically enabled on RX_D3. This 50MHz output clock must be routed to the MAC.

RMII Leader mode can be configured through straps or by programming register 0x0648. RMII Follower mode can only be configured through straps on RX_D[2:0] pins. For RMII Follower Mode, besides placing appropriate strap resistors, program register 0x0432 to value 0x0004 as well.

The RMII specification has the following characteristics:

- Single clock reference shared between MAC and PHY
- Provides independent 2-bit wide transmit and receive data paths

In this mode, data transfers are two bits for every clock cycle using the 50MHz reference clock for both transmit and receive paths.

The RMII signals are summarized in Table 7-28:

Table 7-28. RMII Signals

FUNCTION	PINS
Data Signals	TX_D[1:0]
	RX_D[1:0]
Control Signals	TX_EN
	CRS_DV

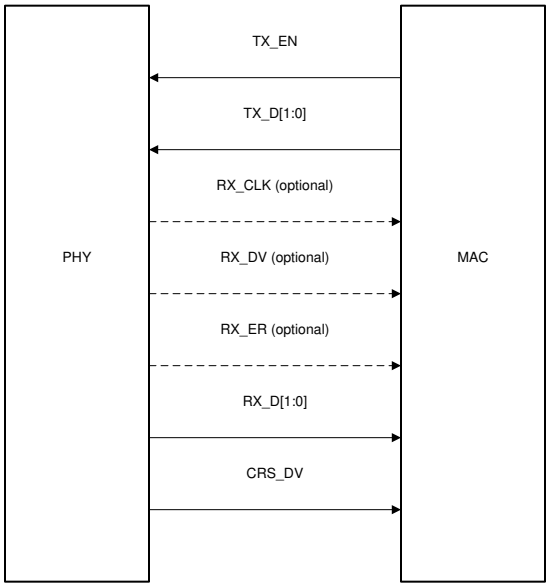


Figure 7-21. RMII Signaling

Table 7-29. RMII Transmit Encoding

TX_EN	TX_D[1:0]	DESCRIPTION
0	00 through 11	Normal Inter-Frame
1	00 through 11	Normal Data Transmission

Table 7-30. RMII Receive Encoding

CRS_DV	RX_ER	RX_D[1:0]	DESCRIPTION
0	0	00 through 11	Normal Inter-Frame
0	1	00	Normal Inter-Frame
0	1	01 through 11	Reserved
1	0	00 through 11	Normal Data Reception
1	1	00 through 11	Data Reception with Errors

RMII Follower: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the XI pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the XI pin.

RMII Leader: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the RX_D3 pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the RX_D3 pin.

The DP83TC815-Q1 RMII supplies an RX_DV signal, which provides a simpler method to recover receive data without the need to separate RX_DV from the CRS_DV indication. RX_ER is also supported even though it is not required by the RMII specification.

RMII includes a programmable FIFO to adjust for the frequency differences between the reference clock and the recovered clock. The programmable FIFO, located in the register 0x0011[9:8] and register 0x0648[9:7], minimizes internal propagation delay based on expected maximum packet size and clock accuracy.

Table 7-31. XI Clock PPM = ±100ppm

Reg 0x0011 <9:8>	Reg 0x0648 <9:7>	INCREMENT PHY LATENCY	MAX PACKET LENGTH WITHOUT ERRORS
01	010	Default	2250
10	100	80ns	7250

7.4.3.3 Reduced Gigabit Media Independent Interface

The DP83TC815-Q1 also supports Reduced Gigabit Media Independent Interface (RGMII) as specified by RGMII version 2.0 with LVCMOS. RGMII is designed to reduce the number of pins required to connect MAC and PHY. To accomplish this goal, the control signals are multiplexed. Both rising and falling edges of the clock are used to sample the control signal pin on transmit and receive paths. Data is sampled on just the rising edge of the clock. For 100Mbps operation, RX_CLK and TX_CLK operate at 25MHz.

The RGMII signals are summarized in Table 7-32:

Table 7-32. RGMII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_CTRL
	RX_CTRL
Clock Signals	TX_CLK
	RX_CLK

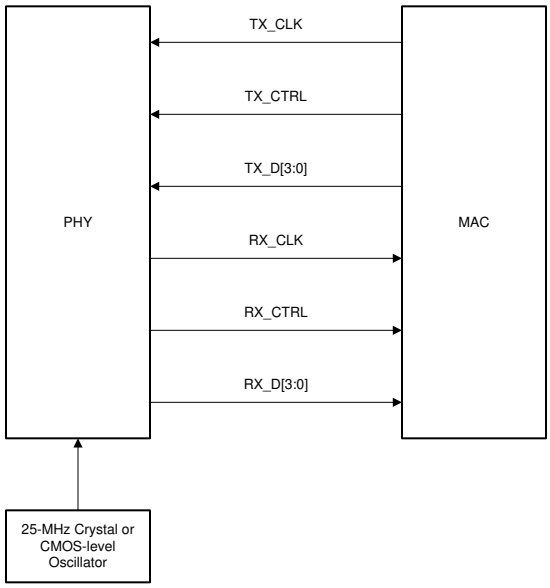


Figure 7-22. RGMII Connections

Table 7-33. RGMII Transmit Encoding

TX_CTRL (POSITIVE EDGE)	TX_CTRL (NEGATIVE EDGE)	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

Table 7-34. RGMII Receive Encoding

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

During packet reception, RX_CLK can be stretched on either the positive or negative pulse to accommodate the transition from the internal free running clock to a recovered clock (data synchronous). Data can be duplicated on the falling edge of the clock because double data rate (DDR) is only required for 1Gbps operation, which is not supported by the DP83TC815-Q1.

The DP83TC815-Q1 supports in-band status indication to help simplify link status detection. Inter-frame signals on RX_D[3:0] pins as specified in Table 7-35.

Table 7-35. RGMII In-Band Status

RX_CTRL	RX_D3	RX_D[2:1]	RX_D0
00 **Note:** In-band status is only valid when RX_CTRL is low	**Duplex Status:** 0 = Half-Duplex 1 = Full-Duplex	**RX_CLK Clock Speed:** 00 = 2.5MHz 01 = 25MHz 10 = 125MHz 11 = Reserved	**Link Status:** 0 = Link not established 1 = Valid link established

7.4.3.4 Serial Gigabit Media Independent Interface

The Serial Gigabit Media Independent Interface (SGMII) provides a means for data transfer between MAC and PHY with significantly less signal pins (4 pins) compared to MII (14 pins), RMII (7 pins) or RGMII (12 pins). SGMII uses low-voltage differential signaling (LVDS) to reduce emissions and improve signal quality.

The DP83TC815-Q1 SGMII is capable of operating in 4-wire. SGMII is configurable through hardware bootstraps. In 4-wire operation, two differential pairs are used to transmit and receive data. Clock and data recovery are performed in the MAC and in the PHY.

Because the DP83TC815-Q1 operates at 100Mbps, the 1.25-Gbps rate of the SGMII is excessive. The SGMII specification allows for 100Mbps operation by replicating each byte within a frame 10 times. Frame elongation takes place above the IEEE 802.3 PCS layer, which prevents the start-of-frame delimiter from appearing more than once.

The DP83TC815-Q1 only supports 100Mbps speed, therefore SGMII Auto-Negotiation can be disabled by setting bit[0] = 0b0 in the *Register 0x608*.

The SGMII signals are summarized in Table 7-36.

Table 7-36. SGMII Signals

FUNCTION	PINS
Data Signals	TX_M, TX_P
	RX_M, RX_P

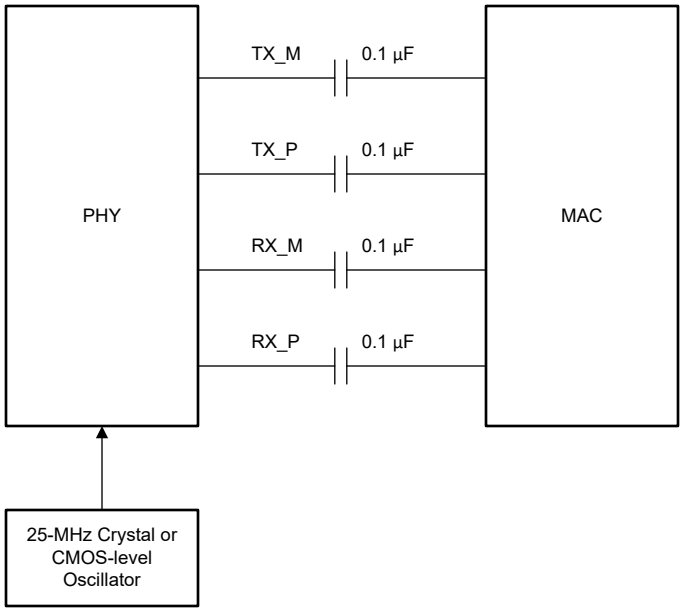


Figure 7-23. SGMII Connections

7.4.4 Serial Management Interface

The Serial Management Interface (SMI) provides access to the DP83TC815-Q1 internal register space for status information and configuration. The SMI frames and base registers are compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TC815-Q1. Additionally, the DP83TC815-Q1 includes control and status registers added to clause 45 as defined by IEEE 802.3bw. Access to clause 45 register field is achieved using clause 22 access.

The SMI includes the management clock (MDC) and the management input and output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 9 DP83TC815-Q1 PHYs can share a common SMI bus. To distinguish between the PHYs, a 4-bit address is used. During power-up-reset, the DP83TC815-Q1 latches the PHYAD[3:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up-reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device can actively drive the MDIO signal during the first bit of turnaround. The addressed DP83TC815-Q1 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TC815-Q1, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

Table 7-37. SMI Protocol Structure

SMI PROTOCOL	<idle> <start> <op code> <device address> <reg address> <turnaround> <data> <idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

7.4.4.1 Extended Register Space Access

The SMI function of the DP83TC815-Q1 supports read or write access to the extended register set using registers REGCR (0x0D) and ADDAR (0x0E) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

Note

Registers with addresses above 0x001F require indirect access. For indirect access, a sequence of register writes must be followed. The MMD value defines the Device Address (DEVAD) of the register set. The DEVAD must be configured in the register 0x000D (REGCR) bits [4:0] for indirect access

The DP83TC815-Q1 supports 3 MMD device addresses:

1. MMD1F (Vendor specific registers): DEVAD [4:0] = ‘11111’
2. MMD1 (IEEE 802.3az defined registers): DEVAD [4:0] = ‘00001’
3. MMD3 (IEEE 802.3az defined registers): DEVAD [4:0] = ‘00011’

Table 7-38. MMD Register Space Division

MMD REGISTER SPACE	REGISTER ADDRESS SETTING
MMD1F	0x000 - 0x0DF0
MMD1	0x1000 - 0x1836
MMD3	0x3000 - 0x3001

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for MMD1F register accesses (DEVAD[4:0] = 11111).

7.4.4.2 Write Operation (No Post Increment)

To write a register in the extended register set:

INSTRUCTION	EXAMPLE: Set reg 0x0170 = 0C50
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR (0x0D).	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR (0x0E).	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Write the content of the desired extended register set register to register ADDAR.	Write register 0x0E to value 0x0C50

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.4.3 Read Operation (No Post Increment)

To read a register in the extended register set:

INSTRUCTION	EXAMPLE: Read 0x0170
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x401F
4. Read the content of the desired extended register set register to register ADDAR.	Read register 0x0E

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.4.4 Write Operation (Post Increment)

To write a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

INSTRUCTION	EXAMPLE: Set reg 0x0170 = 0C50 & reg 0x0171 = 0x0011
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F
2. Write the register address from register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11. DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x801F
4. Write the content of the desired extended register set register to register ADDAR.	Write register 0x0E to value 0x0C50
5. Subsequent writes to register ADDAR (step 4) writes the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.	Write register 0x0E to value 0x0011

Step 4 Writes register 0x0170 to 0x0C50 and because post increment is enabled, Step 5 writes register 0x0171 to 0x0011.

7.4.4.5 Read Operation (Post Increment)

To read a register in the extended register set and automatically increment the address register to the next higher value following the read operation:

INSTRUCTION	EXAMPLE: Read register 0x0170 & 0x0171
1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x001F
2. Write the desired register address to register ADDAR.	Write register 0x0E to value 0x0170
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) to register REGCR.	Write register 0x0D to value 0x801F
4. Read the content of the desired extended register set register to register ADDAR.	Read register 0x0E
5. Subsequent reads to register ADDAR (step 4) reads the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.	Read register 0x0E

Step 4 Reads register 0x0170 and because post increment is enabled, Step 5 reads register 0x0171.

7.5 Programming

7.5.1 Strap Configuration

The DP83TC815-Q1 uses functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up and hardware reset (through either the $\overline{\text{RESET}}$ pin or register access). Some strap pins support 3 levels and some strap pins support 2 levels, which are described in greater detail below. PHY address straps, RX_DV/RX_CTRL and RX_ER, are 3-level straps while all other straps are two levels. Configuration of the device can be done through strapping or through serial management interface.

Note

Because strap pins are functional pins after reset is deasserted, they must not be connected directly to VDDIO or VDDMAC or GND. Either pullup resistors, pulldown resistors, or both are required for proper operation.

Note

When using VDDMAC and VDDIO separately, it is important to connect strap resistors to the correct voltage rail. Each pin voltage domain is listed in the table below.

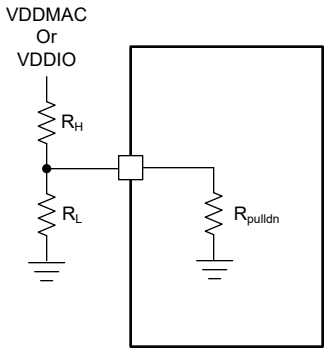


Figure 7-24. Strap Circuit

R_{pulldn} value is included in the Electrical Characteristics table of the data sheet.

Table 7-39. Recommended 3-Level Strap Resistor Ratios for PHY Address

MODE [3]	IDEAL RH (kΩ) (VDDIO = 3.3V) [1]	IDEAL RH (kΩ) (VDDIO = 2.5V) [2]	IDEAL RH (kΩ) (VDDIO = 1.8V) [1]
1	OPEN	OPEN	OPEN
2	13	12	4
3	4.5	2	0.8

1. Strap resistors with 10% tolerance.
2. Strap resistors with 1% tolerance.
3. RL is optional and can be added if voltage on bootstrap pins needs to be adjusted.

Table 7-40. Recommended 2-Level Strap Resistors

MODE	IDEAL RH (kΩ) [1, 2]
1	OPEN
2	2.49

1. Strap resistors with up to 10% tolerance can be used.
2. To gain more margin in customer application for 1.8V VDDIO, either 2.1kΩ ±10% pullup can be used or resistor accuracy of 2.49kΩ resistor can be limited to 1%.

The following table describes the PHY configuration bootstraps:

Table 7-41. Bootstraps

PIN NAME	PIN NO.	DOMAIN	DEFAULT MODE	STRAP FUNCTION			DESCRIPTION
RX_DV/ RX_CTRL	15	VDDMAC	1	**MODE**	**PHY_AD[0]**	**PHY_AD[2]**	PHY_AD: PHY Address ID
				1	0	0	
				2	0	1	
				3	1	1	
RX_ER	14	VDDMAC	1	**MODE**	**PHY_AD[1]**	**PHY_AD[3]**	PHY_AD: PHY Address ID
				1	0	0	
				2	0	1	
				3	1	1	
CLKOUT	16	VDDMAC	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable. This is a duplicate strap for LED_1. If CLKOUT pin is configured as LED_1 pin then the $\overline{\text{AUTO}}$strap functionality also moves to the CLKOUT pin.
				1	0		
				2	1		
RX_D0	26	VDDMAC	1	**MODE**	**MAC[0]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D1	25	VDDMAC	1	**MODE**	**MAC[1]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D2	24	VDDMAC	1	**MODE**	**MAC[2]**		MAC: MAC Interface Selection
				1	0		
				2	1		
RX_D3	23	VDDMAC	1	**MODE**	**CLKOUT_PIN**		CLKOUT_PIN: This strap determines which pin is used for output clock.
				1	0		
				2	1		
LED_0	35	VDDIO	1	**MODE**	**MS**		MS: 100BASE-T1 Leader & 100BASE-T1 Follower Selection
				1	0		
				2	1		
LED_1	6	VDDIO	1	**MODE**	**$\overline{\text{AUTO}}$**		$\overline{\text{AUTO}}$: Autonomous Disable This is the default strap pin for controlling $\overline{\text{AUTO}}$ feature. If this pin is configured as CLKOUT, the $\overline{\text{AUTO}}$ feature moves to pin 16.
				1	0		
				2	1		
GPIO_4	19	VDDMAC	1	**MODE**	**RESERVED**		Reserved. Leave unconnected.
				1	0		
				2	1		
RX_CLK	27	VDDMAC	1	**MODE**	**$\overline{\text{TC10}}$**		TC10 Disable: This pin strap decides whether TC10 is enabled or disabled
				1	0		
				2	1		

Note

Refer to open alliance application note, which provides the register configs for compliance testing. It is necessary to use these register settings to achieve the same performance as observed during compliance testing. Managed mode strap option is recommended to prevent the link up process from initiating while the software configuration from Errata is being executed. When the software configuration is completed, the PHY can be removed from Managed mode by setting bit 0x018B[6] to '1'. This bit is auto-cleared after link up

RX_D3 strap pin has a special functionality of controlling the output status of CLKOUT (pin 16) and LED_1 (pin 6). The Table 7-42 table below shows how pin 16 and pin 6 are affected by RX_D3 strap status. Note that RX_D3 option only changes the pin functionality but not the voltage domains. Pin 16 is always in VDDMAC domain and Pin 6 is always in VDDIO domain. If VDDIO and VDDMAC are at separate voltage levels, it must be ensured that pin 16 and pin 6 are strapped to the respective voltage domains.

In clock output daisy chain applications, if VDDMAC and VDDIO are at different voltages then clock output must be routed to pin 6. Internal oscillator of the DP83TC815-Q1 operates in the VDDIO domain, so clock output must also be used on the pin in VDDIO domain, that is, pin 6. In clock output daisy chain applications where VDDMAC and VDDIO are same, this requirement can be ignored. This requirement can also be ignored in applications where clock output is not being used.

Table 7-42. Clock Output Pin Selection

CLKOUT_PIN	DESCRIPTION
0	Pin 16 is Clock output, Pin 6 is LED_1 pin. $\overline{\text{AUTO}}$ is controlled by straps on pin 6.
1	Pin 6 is Clock output, Pin 16 is LED_1 pin. $\overline{\text{AUTO}}$ is controlled by straps on pin 16.

Table 7-43. 100BASE-T1 Leader and 100BASE-T1 Follower Selection Bootstrap

MS	DESCRIPTION
0	100BASE-T1 Follower Configuration
1	100BASE-T1 Leader Configuration

Table 7-44. Autonomous Mode Bootstrap

$\overline{\text{AUTO}}$	DESCRIPTION
0	Autonomous Mode, PHY able to establish link after power-up
1	Managed Mode, PHY must be allowed to establish link after power-up based on register write

Table 7-45. TC10 Disable Bootstrap

$\overline{\text{TC10}}$	DESCRIPTION
0	TC10 is enabled
1	TC10 is disabled. This strap prevents PHY from transition to sleep mode.

Table 7-46. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire) (1)
0	0	1	MII
0	1	0	RMII Follower (2)
0	1	1	RMII Leader
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Internal Delay Mode)
1	1	0	RGMII (TX and RX Internal Delay Mode)
1	1	1	RGMII (RX Internal Delay Mode)

(1) SGMII strap mode is only available on 'S' type device variant. For 'R' type device variant, this strap mode is RESERVED
(2) RMII Follower mode can only be configured through straps. Configure the straps and program register 0x0432 = 0x0004.

Table 7-47. PHY Address Bootstraps

PHY_AD[3:0]	RX_CTRL STRAP MODE	RX_ER STRAP MODE	DESCRIPTION Section 7.5.1
0000	1	1	PHY Address: b0000 (0x0)
0001	-	-	NA
0010	-	-	NA
0011	-	-	NA
0100	2	1	PHY Address: b0100 (0x4)
0101	3	1	PHY Address: b0101 (0x5)
0110	-	-	NA
0111	-	-	NA
1000	1	2	PHY Address: b1000 (0x8)
1001	-	-	NA
1010	1	3	PHY Address: b1010 (0xA)
1011	-	-	NA
1100	2	2	PHY Address: b1010 (0xC)
1101	3	2	PHY Address: b1011 (0xD)
1110	2	3	PHY Address: b1110 (0xE)
1111	3	3	PHY Address: b1111 (0xF)

7.5.1.1 LED Configuration

DP83TC815-Q1 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2 (CLKOUT). Several functions can be multiplexed onto the LEDs for different modes of operation. LED operations are selected using registers 0x0450.

Because the LED output pins are also used as strap pins, external components required for strapping and the user must consider the LED usage to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding input upon power up or hardware reset.

Figure 7-25 shows the two proper ways of connecting LEDs directly to the DP83TC815-Q1.

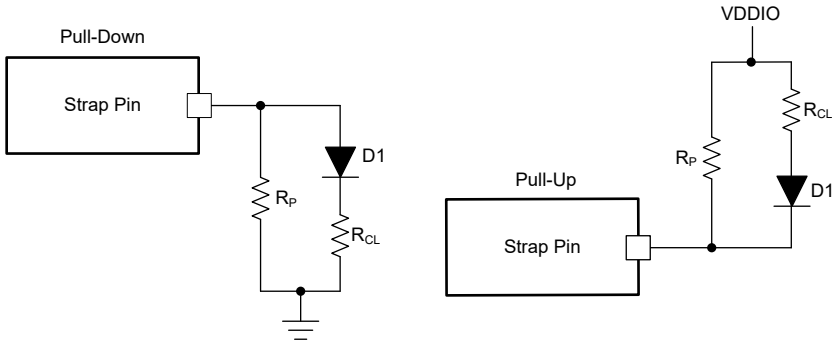


Figure 7-25. Example Strap Connections

8 Register Maps

8.1 Register Access Summary

There are two different methods for accessing registers within the field. Direct register access method is only allowed for the first 32 registers (0x0 through 0x1F). Registers beyond 0x1F must be accessed by use of the Indirect Method (Extended Register Space) described in Section 7.4.4.1.

Table 8-1. MMD Register Space Division

MMD REGISTER SPACE	REGISTER ADDRESS RANGE
MMD1F	0x0000 - 0x0DF0
MMD1	0x1000 - 0x1836
MMD3	0x3000 - 0x3001

Note

For MMD1 and MMD3, the most significant nibble of the register address is used to denote the respective MMD space. This nibble must be ignored during actual register access operation. For example, to access register 0x1836, use 0x1 as the MMD indicator and 0x0836 as the register address.

Table 8-2. Register Access Summary

REGISTER FIELD	REGISTER ACCESS METHODS
0x0 through 0x1F	Direct Access
	Indirect Access, MMD1F = '11111' **Example:** to read register 0x17 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x17 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1F Field 0x20 - 0xFFF	Indirect Access, MMD1F = '11111' **Example:** to read register 0x462 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x462 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1 Field 0x0 - 0xFFF	Indirect Access, MMD1 = '00001' **Example:** to read register 0x7 in MMD1 field (register 0x1007) with no post increment Step 1) write 0x1 to register 0xD Step 2) write 0x7 to register 0xE Step 3) write 0x4001 to register 0xD Step 4) read register 0xE

8.2 DP83TC815 Registers

Table 8-3 lists the memory-mapped registers for the DP83TC815 registers. All register offset addresses not listed in Table 8-3 must be considered as reserved locations and the register contents must not be modified.

Table 8-3. DP83TC815 Registers

Offset	Acronym	Register Name	Section
0h	BMCR	IEEE Control Register	Section 8.2.1
1h	BMSR	IEEE Status Register	Section 8.2.2
2h	PHYIDR1	PHY Identification Register - 1	Section 8.2.3
3h	PHYIDR2	PHY Identification Register - 2	Section 8.2.4
10h	PHYSTS	PHY Status Register	Section 8.2.5
11h	PHYSCR	Software Control Register	Section 8.2.6
12h	MISR1	Interrupt Register -1	Section 8.2.7
13h	MISR2	Interrupt Register -2	Section 8.2.8
15h	RECR	RX Error Count Register	Section 8.2.9
16h	BISCR	BIST Control Register	Section 8.2.10
17h	MISR4	Interrupt Register -4	Section 8.2.11
18h	MISR3	Interrupt Register -3	Section 8.2.12
19h	REG_19	PHY Address Status Register	Section 8.2.13
1Ah	REG_1A	Receive Symbol Status Register	Section 8.2.14
1Bh	TC10_ABORT_REG	TC10 Abort Register	Section 8.2.15
1Eh	CDCR	TDR Run Status Register	Section 8.2.16
1Fh	PHYRCR	Reset Control Register	Section 8.2.17
3Eh	Register_3E	Register_3E	Section 8.2.18
133h	Register_133	CnS Status Register	Section 8.2.19
17Fh	Register_17F	WUR WUP Configuration Register	Section 8.2.20
181h	Register_181	LPS Received Count Register	Section 8.2.21
182h	Register_182	WUR Received Count Register	Section 8.2.22
184h	LPS_CFG	Low Power Configuration Register - 0	Section 8.2.23
18Bh	LPS_CFG2	Low Power Configuration Register - 2	Section 8.2.24
18Ch	LPS_CFG3	Low Power Configuration Register - 3	Section 8.2.25
18Dh	LINK_FAIL_CNT	Link Fail Count Register	Section 8.2.26
18Eh	LPS_STATUS	Low Power Status Register	Section 8.2.27
1A0h	PCF	PHY Control Frame Configuration Register	Section 8.2.28
1A2h	MISC1	SA DA Configuration Register	Section 8.2.29
1A3h	PPM0	PPM Monitor Config Register - 0	Section 8.2.30
1A4h	PPM1	PPM Monitor Config Register - 1	Section 8.2.31
1A5h	PPM2	PPM Monitor Config Register - 2	Section 8.2.32
1A6h	PPM3	PPM Monitor Config Register - 3	Section 8.2.33
1A7h	PPM4	PPM Monitor Config Register - 4	Section 8.2.34
1A8h	PPM5	PPM Monitor Config Register - 5	Section 8.2.35
1A9h	PPM6	PPM Monitor Config Register - 6	Section 8.2.36
1AAh	PPM7	PPM Monitor Config Register - 7	Section 8.2.37
1ADh	PPM10	PPM Monitor Config Register - 10	Section 8.2.38
1AEh	PPM11	PPM Monitor Config Register - 11	Section 8.2.39
1AFh	PPM12	PPM Monitor Config Register - 12	Section 8.2.40
1BEh	fwu_reg_3	Fast Wake Up Register - 3	Section 8.2.41

Table 8-3. DP83TC815 Registers (continued)

Offset	Acronym	Register Name	Section
1D2h	spare_reg_tc10	Fast Wake Up Spare Register	Section 8.2.42
310h	TDR_TC1	TDR Status Register	Section 8.2.43
402h	ANA_LD_CTRL_3	VDDIO Level Status Register	Section 8.2.44
430h	A2D_REG_48	RGMII ID Control Register	Section 8.2.45
440h	A2D_REG_64	ESD Event Count Register - 0	Section 8.2.46
442h	A2D_REG_66	ESD Event Count Register - 1	Section 8.2.47
444h	A2D_REG_68	TC10 Force Control Register	Section 8.2.48
450h	LEDS_CFG_1	LED Configuration Register - 1	Section 8.2.49
451h	LEDS_CFG_2	LED Configuration Register - 2	Section 8.2.50
452h	IO_MUX_CFG_1	IO Multiplexing Register - 1	Section 8.2.51
453h	IO_MUX_CFG_2	IO Multiplexing Register - 2	Section 8.2.52
455h	IO_CONTROL_2	IO Control Register - 2	Section 8.2.53
456h	IO_MUX_CFG	xMII Impedance Control Register	Section 8.2.54
45Dh	CHIP_SOR_1	Strap Status Register	Section 8.2.55
45Fh	LED1_CLKOUT_ANA_CTRL	CLKOUT and LED_1 Control Register	Section 8.2.56
460h	IMPEDANCE_CTRL_0	Impedance Control Register - 0	Section 8.2.57
461h	IMPEDANCE_CTRL_1	Impedance Control Register - 1	Section 8.2.58
4DFh	RX_FIFO_CONFIG	RX_FIFO_CONFIG	Section 8.2.59
4EEh	LINKUP_TIMER_1	Link Up Timer Register - 1	Section 8.2.60
4EFh	LINKUP_TIMER_2	Link Up Timer Register - 2	Section 8.2.61
523h	TX_PR_FILT_CTRL	MDI Transmit Force Register	Section 8.2.62
551h	PG_REG_1	CRS_DV Control Register	Section 8.2.63
552h	PG_REG_3	PG_REG_3	Section 8.2.64
553h	PG_REG_4	Auto-Polarity Correction Control Register	Section 8.2.65
561h	TC1_LINK_FAIL_LOSS	TC1 Link Fail Count Register	Section 8.2.66
562h	TC1_LINK_TRAINING_TIME	TC1 Link Training Time Register	Section 8.2.67
563h	NO_LINK_TH	No Link Interrupt TimeThreshold Register	Section 8.2.68
5A0h	DITH_CTRL_0	Dithering Control Register - 0	Section 8.2.69
5A1h	DITH_CTRL_1	Dithering Control Register - 1	Section 8.2.70
5A8h	DITH_RFI_EN_CTRL	Dithering Enable Register	Section 8.2.71
5B2h	CFG_PCF_DMAC_ADDR	Configurable Last Two Bytes of PCF DMAC	Section 8.2.72
5B7h	SPARE_IN_FROM_DIG_SL_1	Register With Configurable Bits For Analog	Section 8.2.73
5B8h	CONTROL_REG_1	Dithering Disable Control	Section 8.2.74
600h	RGMII_CTRL	RGMII Control Register	Section 8.2.75
601h	RGMII_FIFO_STATUS	RGMII FIFO Status Register	Section 8.2.76
602h	RGMII_CLK_SHIFT_CTRL	RGMII Shift Control Register	Section 8.2.77
608h	SGMII_CTRL_1	SGMII Control Register - 1	Section 8.2.78
60Ah	SGMII_STATUS	SGMII Status Register	Section 8.2.79
60Ch	SGMII_CTRL_2	SGMII Control Register - 2	Section 8.2.80
60Dh	SGMII_FIFO_STATUS	SGMII FIFO Status Register	Section 8.2.81
618h	PRBS_STATUS_1	PRBS Status Register - 1	Section 8.2.82
619h	PRBS_CTRL_1	PRBS Control Register - 1	Section 8.2.83
61Ah	PRBS_CTRL_2	PRBS Control Register - 2	Section 8.2.84
61Bh	PRBS_CTRL_3	PRBS Control Register - 3	Section 8.2.85
61Ch	PRBS_STATUS_2	PRBS Status Register - 2	Section 8.2.86

Table 8-3. DP83TC815 Registers (continued)

Offset	Acronym	Register Name	Section
61Dh	PRBS_STATUS_3	PRBS Status Register - 3	Section 8.2.87
61Eh	PRBS_STATUS_4	PRBS Status Register - 4	Section 8.2.88
620h	PRBS_STATUS_5	PRBS Status Register - 5	Section 8.2.89
622h	PRBS_STATUS_6	PRBS Status Register - 6	Section 8.2.90
623h	PRBS_STATUS_7	PRBS Status Register - 7	Section 8.2.91
624h	PRBS_CTRL_4	PRBS Control Register - 4	Section 8.2.92
625h	PATTERN_CTRL_1	BIST Pattern Control Register - 1	Section 8.2.93
626h	PATTERN_CTRL_2	BIST Pattern Control Register - 2	Section 8.2.94
627h	PATTERN_CTRL_3	BIST Pattern Control Register - 3	Section 8.2.95
628h	PMATCH_CTRL_1	BIST Match Control Register - 1	Section 8.2.96
629h	PMATCH_CTRL_2	BIST Match Control Register - 2	Section 8.2.97
62Ah	PMATCH_CTRL_3	BIST Match Control Register - 3	Section 8.2.98
638h	PKT_CRC_STAT	BIST CRC Status Register	Section 8.2.99
639h	TX_PKT_CNT_1	xMII TX Packet Count Register - 1	Section 8.2.100
63Ah	TX_PKT_CNT_2	xMII TX Packet Count Register - 2	Section 8.2.101
63Bh	TX_PKT_CNT_3	xMII TX Packet Count Register - 3	Section 8.2.102
63Ch	RX_PKT_CNT_1	xMII RX Packet Count Register - 1	Section 8.2.103
63Dh	RX_PKT_CNT_2	xMII RX Packet Count Register - 2	Section 8.2.104
63Eh	RX_PKT_CNT_3	xMII RX Packet Count Register - 3	Section 8.2.105
648h	RMII_CTRL_1	RMII Control Register	Section 8.2.106
649h	RMII_STATUS_1	RMII FIFO Status Register	Section 8.2.107
D00h	PTP_CTL	PTP Control Register	Section 8.2.108
D01h	PTP_TDR	PTP Time Data Register	Section 8.2.109
D02h	PTP_STS	PTP Status Register	Section 8.2.110
D03h	PTP_TSTS	PTP Trigger Status Register	Section 8.2.111
D04h	PTP_RATEL	PTP Rate Low Register	Section 8.2.112
D05h	PTP_RATEH	PTP Rate High Register	Section 8.2.113
D08h	PTP_TXTS	PTP Transmit Timestamp Register	Section 8.2.114
D09h	PTP_RXTS	PTP Receive Timestamp Register	Section 8.2.115
D0Ah	PTP_ESTS	PTP Event Status Register	Section 8.2.116
D10h	PTP_TRIG	PTP Trigger Configuration Register	Section 8.2.117
D11h	PTP_EVNT	PTP Event Configuration Register	Section 8.2.118
D12h	PTP_TXCFG0	PTP Transmit Configuration Register 0	Section 8.2.119
D13h	PTP_TXCFG1	PTP Transmit Configuration Register 1	Section 8.2.120
D14h	PSF_CFG0	PHY Status Frame Configuration Register 0	Section 8.2.121
D15h	PTP_RXCFG0	PTP Receive Configuration Register 0	Section 8.2.122
D16h	PTP_RXCFG1	PTP Receive Configuration Register 1	Section 8.2.123
D17h	PTP_RXCFG2	PTP Receive Configuration Register 2	Section 8.2.124
D18h	PTP_RXCFG3	PTP Receive Configuration Register 3	Section 8.2.125
D19h	PTP_RXCFG4	PTP Receive Configuration Register 4	Section 8.2.126
D1Ah	PTP_TRDL	PTP Temporary Rate Duration Low Register	Section 8.2.127
D1Bh	PTP_TRDH	PTP Temporary Rate Duration High Register	Section 8.2.128
D1Ch	PTP_EVNT_TSU_CFG	Event Timestamp Storage Configuration	Section 8.2.129
D1Dh	PSF_TRIG_TS_EN	Trigger Timestamp PHY Status Frame Enable	Section 8.2.130
D20h	PTP_COC	PTP Clock Output Control Register	Section 8.2.131

Table 8-3. DP83TC815 Registers (continued)

Offset	Acronym	Register Name	Section
D21h	PSF_CFG1	Phy Status Frame Configuration Register 1	Section 8.2.132
D22h	PSF_CFG2	Phy Status Frame Configuration Register 2	Section 8.2.133
D23h	PSF_CFG3	Phy Status Frame Configuration Register 3	Section 8.2.134
D24h	PSF_CFG4	Phy Status Frame Configuration Register 4	Section 8.2.135
D26h	PTP_INTCTL	PTP Interrupt Control Register	Section 8.2.136
D27h	PTP_CLKSRC	PTP Clock Source Register	Section 8.2.137
D28h	PTP_ETYPE	PTP Ethernet Type Register	Section 8.2.138
D29h	PTP_OFF	PTP Offset Register	Section 8.2.139
D2Bh	PTP_RXHASH	PTP Receive Hash Register	Section 8.2.140
D30h	PTP_EVENT_GPIO_SEL	PTP Event GPIO selection	Section 8.2.141
D32h	TX_SMD_GPIO_CTL	TX path SMD detection and GPIO control	Section 8.2.142
D33h	SCH_CTL_1	Scheduler control 1	Section 8.2.143
D34h	SCH_CTL_2	Scheduler control 2	Section 8.2.144
D35h	FREQ_CTL_1	Base frequency control 1	Section 8.2.145
D36h	FREQ_CTL_2	Base frequency control 2	Section 8.2.146
D37h	PTP_RATEL_ACC_ONLY	PTP Rate ACC only LSB Register	Section 8.2.147
D38h	PTP_RATEH_ACC_ONLY	PTP Rate ACC only MSB Register and enable	Section 8.2.148
D39h	PTP_PLL_CTL	PTP_PLL control register	Section 8.2.149
D3Ah	PTP_PLL_RD_1	PTP timestamp read register 1	Section 8.2.150
D3Bh	PTP_PLL_RD_2	PTP timestamp read register 2	Section 8.2.151
D3Ch	PTP_PLL_RD_3	PTP timestamp read register 3	Section 8.2.152
D3Dh	PTP_PLL_RD_4	PTP timestamp read register 4	Section 8.2.153
D3Eh	PTP_PLL_RD_5	PTP timestamp read register 5	Section 8.2.154
D3Fh	PTP_PLL_RD_6	PTP timestamp read register 6	Section 8.2.155
D40h	PTP_ONESTEP_OFF	PTP ONESTEP OFFSET register	Section 8.2.156
D45h	PTP_PSF_VLAN_CFG_1	PSF VLAN Configuration 1	Section 8.2.157
D46h	PTP_PSF_VLAN_CFG_2	PSF VLAN Configuration 2	Section 8.2.158
D47h	PTP_PSF_VLAN_CFG_3	PSF VLAN Configuration 3	Section 8.2.159
D48h	MAX_IPV4_LENGTH	PSF IPv4 Packet Length	Section 8.2.160
D49h	PTP_TXCFG_2	PTP Domain Filter Controls	Section 8.2.161
D4Ah	PSF_DMAC_1	PSF DMAC Address 1	Section 8.2.162
D4Bh	PSF_DMAC_2	PSF DMAC Address 2	Section 8.2.163
D4Ch	PSF_DMAC_3	PSF DMAC Address 3	Section 8.2.164
D4Dh	PSF_SMAC_1	PSF SMAC Address 1	Section 8.2.165
D4Eh	PSF_SMAC_2	PSF SMAC Address 2	Section 8.2.166
D4Fh	PSF_SMAC_3	PSF SMAC Address 3	Section 8.2.167
D50h	PSF_ETYPE	PSF Ether Type	Section 8.2.168
D51h	IPV4_DA_1	PSF Destination Address 1	Section 8.2.169
D52h	IPV4_DA_2	PSF Destination Address 2	Section 8.2.170
D53h	PSF_SOURCE_UDP_PORT	PSF UDP Source Port Address	Section 8.2.171
D54h	PSF_DESTINATION_UDP_PORT	PSF UDP Destination Port Address	Section 8.2.172
DE0h	PTP_LAT_COMP_CTRL	PTP Latency Compensation Control	Section 8.2.173
DF0h	PTP_DEBUG_SEL	PTP Debug Select	Section 8.2.174
1000h	MMD1_PMA_CTRL_1	PMA Control 1	Section 8.2.175
1001h	MMD1_PMA_STATUS_1	PMA Status 1	Section 8.2.176

Table 8-3. DP83TC815 Registers (continued)

Offset	Acronym	Register Name	Section
1007h	MMD1_PMA_STAUS_2	PMA Status 2	Section 8.2.177
100Bh	MMD1_PMA_EXT_ABILITY_1	PMA Extended 1	Section 8.2.178
1012h	MMD1_PMA_EXT_ABILITY_2	PMA Extended 2	Section 8.2.179
1834h	MMD1_PMA_CTRL_2	PMA Control 2	Section 8.2.180
1836h	MMD1_PMA_TEST_MODE_CTRL	PMA Test	Section 8.2.181
3000h	MMD3_PCS_CTRL_1	PCS Control	Section 8.2.182
3001h	MMD3_PCS_Status_1	PCS Status	Section 8.2.183

Complex bit access types are encoded to fit into small table cells. Table 8-4 shows the codes that are used for access types in this section.

Table 8-4. DP83TC815 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WSC	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 BMCR Register (Offset = 0h) [Reset = 2100h]

BMCR is shown in Table 8-5.

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Table 8-5. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MII Reset	R-0/W1S	0h	1b = Digital in reset and all MII regs (0x0 - 0xF) reset to default 0b = No reset This bit is auto-cleared
14	MII Loopback Enable	R/W	0h	1b = Enable MII loopback 0b = Disable MII loopback When xMII loopback mode is activated, the transmitted data presented on xMII TXD is looped back to xMII RXD internally. There is no LINK indication generated when xMII loopback is enabled.
13	Speed Select	R	1h	1b= 1000 Mb/s 0b = Reserved
12	Auto-Negotiation Enable	R	0h	Auto-Negotiation: Not supported on this device

Table 8-5. BMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	IEEE Power Down Enable	R/W	0h	This bit can be programmed to enter and exit IEEE power down mode This bit provide status when using INT_N as power down pin 1b = Power down mode 0b = Normal mode
10	MAC Isolate Enable	R/W	0h	1b = Isolate mode (No output from PHY to MAC) 0b = Normal mode
9	RESERVED	R	0h	Reserved
8	Duplex Mode Select	R	1h	1b = Full duplex 0b = Half duplex
7	RESERVED	R	0h	Reserved
6-0	RESERVED	R	0h	Reserved

8.2.2 BMSR Register (Offset = 1h) [Reset = 0061h]

BMSR is shown in Table 8-6.

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Table 8-6. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	100Base-T4 Support	R	0h	0b = PHY does not support 100BASE-T4
14	100Base-X Full Duplex Support	R	0h	0b = PHY does not support full duplex 100BASE-X
13	100Base-X Half Duplex Support	R	0h	0b = PHY does not support half duplex 100BASE-X
12	10 Mbps Full Duplex Support	R	0h	0b = PHY does not support 10 Mb/s in full duplex mode
11	10 Mbps Half Duplex Support	R	0h	0b = PHY does not support 10 Mb/s in half duplex mode
10-7	RESERVED	R	0h	Reserved
6	SMI Preamble Suppression	R	1h	1b = PHY accepts management frames with preamble suppressed. 0b = PHY does not accept management frames with preamble suppressed
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	Auto-Negotiation Ability	R	0h	0b = PHY does not Auto-Negotiation
2	Link status (Latch Low)	RH	0h	1b = Link is up 0b = Link is down at least once
1	Jabber detect	RC	0h	1b = Jabber condition detected 0b = No Jabber condition detected
0	Extended register Capability	R	1h	1b = Extended register capabilities 0b = Basic register set capabilities only

8.2.3 PHYIDR1 Register (Offset = 2h) [Reset = 2000h]

PHYIDR1 is shown in Table 8-7.

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Table 8-7. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Organizationally Unique Identifier 1	R	2000h	Unique Identifier for the part

8.2.4 PHYIDR2 Register (Offset = 3h) [Reset = A2E0h]

PHYIDR2 is shown in Table 8-8.

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Table 8-8. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Unique Identifier 2	R	28h	Unique Identifier for the part
9-4	Model Number	R	2Eh	Unique Identifier for the part
3-0	Revision Number	R	0h	Unique Identifier for the part

8.2.5 PHYSTS Register (Offset = 10h) [Reset = 0004h]

PHYSTS is shown in Table 8-9.

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Table 8-9. PHYSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	Descrambler Lock Status (Latch Low)	RH	0h	1b = Descrambler is locked 0b = Descrmabler is unlocked at least once
8	RESERVED	R	0h	Reserved
7	Interrupt Pin Status	R	0h	Interrupts pin status, cleared on reading 0x12 1b = Interrupts pin not set 0b = Interrupt pin had been set
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	MII Loopback Status	R	0h	1b = MII loopback enabled 0b = MII loopback Disabled
2	Duplex Mode Status	R	1h	1b = Full duplex 0b = Half duplex
1	RESERVED	R	0h	Reserved
0	Link Status (Latch Low) Non-Clear on Read	R	0h	Non-Clear on Read Latch Low link status 1b = link is up 0b = link is down at least once Status is cleared on reading reg0x1

8.2.6 PHYSCR Register (Offset = 11h) [Reset = 010Bh]

PHYSCR is shown in Table 8-10.

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Table 8-10. PHYSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13-12	RESERVED	R	0h	Reserved
11	SGMII Soft Reset	R/WSC	0h	SGMII Digital Reset This bit is auto-cleared
10	MAC Isolate for PHY_ADDR 0x00	R/W	0h	MAC Isolate is enabled only if PHY address is 0x00 Reg0x0[10] works for all PHY addresses including 0x00 1b = Isolate mode (No output from PHY to MAC) 0b = Normal mode
9-8	RMII TX FIFO Depth	R/W	1h	00b = 4 nibbles 01b = 5 nibbles 10b = 6 nibbles 11b = 8 nibbles
7	RESERVED	R	0h	Reserved
6-4	RESERVED	R	0h	Reserved
3	Interrupt Polarity	R/W	1h	1b = Active low 0b = Active high
2	Force Interrupt	R/W	0h	1b = Force interrupt pin
1	Interrupts Enable	R/W	1h	1b = Enable interrupts 0b = Disable interrupts
0	Interrupt Pin Configuration	R/W	1h	1b = Configure INT_N pin is as interrupt output pin 0b = Configure INT_N pin as power down input pin

8.2.7 MISR1 Register (Offset = 12h) [Reset = 0000h]

MISR1 is shown in Table 8-11.

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Table 8-11. MISR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Energy Detect Change Status	RC	0h	Status is changed to 1 when there is a change of MDI Energy detection output Status is cleared on read of this register
13	Link Status Change Status	RC	0h	Status is changed to 1 when there is a change of link status Status is cleared on read of this register
12	Wake on LAN Status	RC	0h	Status is changed to 1 when WOL is received Status is cleared on read of this register
11	ESD Fault Detected Status	RC	0h	Status is changed to 1 when ESD fault is detected Status is cleared on read of this register
10	Training Done Status	RC	0h	Status is changed to 1 when training is done Status is cleared on read of this register
9	RESERVED	R	0h	Reserved
8	RX Error Counter Half Full Status	RC	0h	Status is changed to 1 when RX Error Counter in 0x15 is half full Status is cleared on read of this register
7	RESERVED	R	0h	Reserved
6	Energy Detect Change Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled

Table 8-11. MISR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Link Status Change Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
4	Wake on LAN Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
3	ESD Fault Detected Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
2	Training Done Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
1	RESERVED	R	0h	Reserved
0	RX Error Counter Half Full Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled

8.2.8 MISR2 Register (Offset = 13h) [Reset = 0000h]

MISR2 is shown in Table 8-12.

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Table 8-12. MISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Under Voltage Status	RC	0h	Status is changed to 1 when Under Voltage is detected Status is cleared on read of this register
14	Over Voltage Status	RC	0h	Status is changed to 1 when Over Voltage is detected Status is cleared on read of this register
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	Over Temperature Status	RC	0h	Status is changed to 1 when Over Temperature is detected Status is cleared on read of this register
10	RESERVED	R	0h	Reserved
9	Data Polarity Change Status	RC	0h	Status is changed to 1 when MDI lines polarity change is detected Status is cleared on read of this register
8	Jabber Detect Status	RC	0h	Status is changed to 1 when jabber is detected Status is cleared on read of this register
7	Under Voltage Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
6	Over Voltage Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	Data Polarity Change Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled

Table 8-12. MISR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Jabber Detect Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled

8.2.9 RECR Register (Offset = 15h) [Reset = 0000h]

RECR is shown in Table 8-13.

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Table 8-13. RECR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Error Count	RC	0h	RX_ER Counter: When a valid carrier is presented (only while RX_DV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in xMII loopback mode. The counter stops when it reaches its maximum count (0xFFFF). When the counter exceeds half-full (0x7FFF), an interrupt is generated. This register is cleared on read.

8.2.10 BISCR Register (Offset = 16h) [Reset = 0100h]

BISCR is shown in Table 8-14.

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Table 8-14. BISCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	Data Transmission to MDI in xMII Loopback	R/W	0h	0b = Suppress data to MDI during xMII loopback 1b = Transmit data to MDI during xMII loopback
5-2	Loopback Mode	R/W	0h	Enable Loopbacks other than PCS loopback. 0x16[1] must be 0 0001b = Digital Loopback 0010b = Analog Loopback 0100b = Reverse Loopback 1000b = External Loopback
1	PCS Loopback Enable	R/W	0h	0b = Disable PCS Loopback 1b = Enable PCS Loopback
0	RESERVED	R	0h	Reserved

8.2.11 MISR4 Register (Offset = 17h) [Reset = 0000h]

MISR4 is shown in Table 8-15.

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Table 8-15. MISR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved

Table 8-15. MISR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	PPM Monitor Unlock Status	R	0h	Status is changed to 1 when PPM Monitor unlocks Status is cleared on read of this register
10-7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	PPM Monitor Unlock Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
2-0	RESERVED	R	0h	Reserved

8.2.12 MISR3 Register (Offset = 18h) [Reset = 0035h]

MISR3 is shown in Table 8-16.

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Table 8-16. MISR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	No Link Status	RC	0h	Status is changed to 1 when Link has not been observed within time programmed in 0x562 after training starts Status is cleared on read of this register
13	Sleep Fail Status	RC	0h	Status is changed to 1 when Sleep Negotiation Fails Status is cleared on read of this register
12	Power-On Reset Done Status	RC	0h	Status is changed to 1 Power-On Reset is done after the supplies are up Status is cleared on read of this register
11	No Frame Status	RC	0h	Status is changed to 1 when No frame is detected until Status is cleared on read of this register
10	WUR Received Status	RC	0h	Status is changed to 1 when WUR command is received from link partner Status is cleared on read of this register
9	Remote Wake-up Indication	RC	0h	Status is 1 after power-up if device is woken-up remotely Status is cleared on read of this register
8	LPS Received Status	RC	0h	Status is changed to 1 when LPS command is received from link partner Status is cleared on read of this register
7	RESERVED	R	0h	Reserved
6	No Link Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
5	Sleep Fail Indication	R/W	1h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
4	Power-On Reset Done Indication	R/W	1h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
3	No Frame Indication	R/W	0h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled

Table 8-16. MISR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	WUR Received Indication	R/W	1h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled
1	RESERVED	R	0h	Reserved
0	LPS Received Indication	R/W	1h	1b = Enable indication on INT_N pin if corresponding Interrupt Status is set 0b = Indication is Disabled

8.2.13 REG_19 Register (Offset = 19h) [Reset = 0800h]

REG_19 is shown in Table 8-17.

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Table 8-17. REG_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-5	RESERVED	R	0h	Reserved
4-0	PHY Address	R	0h	PHY Address latched from straps

8.2.14 REG_1A Register (Offset = 1Ah) [Reset = 0000h]

REG_1A is shown in Table 8-18.

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Table 8-18. REG_1A Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	Data Polarity Status	R	0h	0b = Normal Polarity 1b = Reverse Polarity
3-1	RESERVED	R	0h	Reserved
0	Jabber Detect Disable	R/W	0h	0b = Jabber detection is enabled 1b =Jabber detection is Disabled

8.2.15 TC10_ABORT_REG Register (Offset = 1Bh) [Reset = 0000h]

TC10_ABORT_REG is shown in Table 8-19.

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Table 8-19. TC10_ABORT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	Sleep Abort through GPIO	R/W	0h	Sleep can be aborted by driving high on GPIO 1b = Use LED_1/CLKOUT for Sleep Abort (depending on which GPIO is configured as LED_1) 0b = GPIO is not used for Sleep Abort

Table 8-19. TC10_ABORT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Sleep Abort	R/W	0h	This bit to be set 1 to abort the sleep Cleared on transition to normal mode

8.2.16 CDCR Register (Offset = 1Eh) [Reset = 0000h]

CDCR is shown in Table 8-20.

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Table 8-20. CDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TDR Start	RH/W1S	0h	1b = Start TDR Bit is cleared after TDR run is complete
14	TDR Auto-Run Enable	R/W	0h	1b = Start TDR automatically on link down 0b = Start TDR manually using 0x1E[15]
13-2	RESERVED	R	0h	Reserved
1	TDR Done Status	R	0h	1b = TDR done 0b = TDR on-going or not initiated
0	TDR Fail status	R	0h	When TDR Done Status is 1, this bit indicates if TDR ran successfully 1b = TDR run failed 0b = TDR ran successfully

8.2.17 PHYRCR Register (Offset = 1Fh) [Reset = 0000h]

PHYRCR is shown in Table 8-21.

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Table 8-21. PHYRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Hard Reset	R-0/W1S	0h	Resets Digital Core and register File This bet is self clearing
14	Soft Reset	R-0/W1S	0h	Resets Digital Core but register File is not reset This bit is self clearing
13	Soft Reset 2	R-0/W1S	0h	Resets register File This bit is self clearing
12	RESERVED	R	0h	Reserved
11-7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4-0	RESERVED	R	0h	Reserved

8.2.18 Register_3E (Offset = 3Eh) [Reset = 0000h]

Register_3E is shown in Table 8-22.

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Table 8-22. Register_3E Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved

Table 8-22. Register_3E Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	cfg_leader_scr_rst_on_dsp_fail	R/W	0h	Enable Reset of scrambler on DSP fallback when phy is configured as Leader
4	cfg_follower_scr_rst_on_dsp_fail	R/W	0h	Enable Reset of scrambler on DSP fallback when phy is configured as Follower
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2.19 Register_133 (Offset = 133h) [Reset = 0000h]

Register_133 is shown in Table 8-23.

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Table 8-23. Register_133 Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Link Up Status	R	0h	Link Up status as defined by CnS
13	PHY Control In Send Data Mode	R	0h	PHY Control In Send Data Status
12	Link Status	R	0h	Link Status set by Link Monitor
11-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	Descrambler Lock Status	R	0h	Descrambler lock status
1	Local Receiver Status	R	0h	Local receiver status
0	Remote Receiver Status	R	0h	Remote receiver status

8.2.20 Register_17F (Offset = 17Fh) [Reset = 4028h]

Register_17F is shown in Table 8-24.

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Table 8-24. Register_17F Field Descriptions

Bit	Field	Type	Reset	Description
15	WUR from WAKE pin	R/W	0h	Enable WUR transmission when a pulse is transmitted on WAKE pin 1b = Enable sending WUR Threshold of WAKE pulse width can be configured through 0x17F[7:0]
14	WUP Enable	R/W	1h	Enable WUP transmission after local wake 1b = WUP transmission is enabled 0b = WUP transmission is Disabled This option can be effectively used when PHY powers-up in Standby mode through strap
13-8	RESERVED	R	0h	Reserved

Table 8-24. Register_17F Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	Wake Pulse Threshold	R/W	28h	Width of WAKE pulse in microseconds required to initiate WUR during an active link

8.2.21 Register_181 (Offset = 181h) [Reset = 0000h]

Register_181 is shown in Table 8-25.

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Table 8-25. Register_181 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	RX LPS Count	R	0h	Indicates number of LPS codes received

8.2.22 Register_182 (Offset = 182h) [Reset = 0000h]

Register_182 is shown in Table 8-26.

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Table 8-26. Register_182 Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	RX WUR Count	R	0h	Indicates number of WUR codes received

8.2.23 LPS_CFG Register (Offset = 184h) [Reset = 0203h]

LPS_CFG is shown in Table 8-27.

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Table 8-27. LPS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8-7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	Wake Forward Force	R/W	0h	1b = Force pulse on WAKE pin Pulse Width is configurable by bits [3:2] The bit is self-cleared
3-2	Wake Forward Pulse Width	R/W	0h	Configures the pulse width on WAKE pin for wake-forwarding 00b = 50us 01b = 500us 10b = 2ms 11b = 20ms
1	Wake Forward Enable	R/W	1h	Enable Wake Forwarding on WAKE pin on reception of WUR Command 0b = Enable Wake forwarding 1b = Disable Wake forwarding

Table 8-27. LPS_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0h	Reserved

8.2.24 LPS_CFG2 Register (Offset = 18Bh) [Reset = 1C4Bh]

LPS_CFG2 is shown in Table 8-28.

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Table 8-28. LPS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	Stop Sleep Negotiation on Link Down	R/W	1h	1b = Stop Sleep Negotiation if link goes down during negotiation
11	Stop Sleep Negotiation on Activity	R/W	1h	1b = Stop Sleep Negotiation when activity from MAC is observed in SLEEP_ACK state
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	TC10 Disable	R/W	0h	0b = Enable TC10 1b = Disable TC10 Default value is decided by RX_CLK strap
7	RESERVED	R	0h	Reserved
6	Autonomous Mode	R/W	1h	1b = PHY entered normal mode on power up 0b = PHY entered standby mode on power up Default value is decided by LED_1 strap This bit is cleared post link up.
5	Transition To Standby	R/W	0h	1b = Enable normal to standby transition on over temperature/over voltage/under voltage 0b = Disable normal to standby transition on over temperature/over voltage/under voltage
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2.25 LPS_CFG3 Register (Offset = 18Ch) [Reset = 0000h]

LPS_CFG3 is shown in Table 8-29.

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Table 8-29. LPS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8-0	Power State Entry	RH/W1S	0h	00000001b = Normal command 00000010b = Sleep request 00010000b = Standby command 10000000b = WUR command

8.2.26 LINK_FAIL_CNT Register (Offset = 18Dh) [Reset = 0000h]

LINK_FAIL_CNT is shown in Table 8-30.

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Table 8-30. LINK_FAIL_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	Link Losses Count	R	0h	TI Custom Link Loss Counter: Count incremented on fall edge of Link Status Count cleared on read of this register

8.2.27 LPS_STATUS Register (Offset = 18Eh) [Reset = 0000h]

LPS_STATUS is shown in Table 8-31.

Return to the Summary Table.

Table 8-31. LPS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6-0	Power State Status	R	0h	00000001b = Sleep Mode 00000010b = Standby Mode 00000100b = Normal Mode 00001000b = Sleep Ack 00010000b = Sleep Req 00100000b = Sleep Fail 01000000b = Sleep Silent

8.2.28 PCF Register (Offset = 1A0h) [Reset = 0000h]

PCF is shown in Table 8-32.

Return to the Summary Table.

Table 8-32. PCF Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	PHY Control Frames Error Status	R	0h	Indicates an error was detected in a PCF Frame since the last read of this register. This bit is cleared on read.
13	PHY Control Frames Ok Status	R	0h	Indicates a PCF Frame has completed without error since the last read of this register. This bit is cleared on read.
12-9	RESERVED	R	0h	Reserved
8	PHY Control Frames Destination Address	R/W	0h	Select MAC Destination Address for Phy Control Frames: 0: Use Mac Address [08 00 17 0B 6B 0F] 1: Use Mac Address [08 00 17 00 00 00] The device also recognizes packets with the above address with the Multicast bit set (that is 09 00 17)
7-6	PHY Control Frames Interrupt	R/W	0h	PCF Interrupt Control and Status: Bit 7 - Enable indication of PCF Frame Error Status on INT_N pin Bit 6 - Enable indication of PCF Frame OK Status on INT_N pin Status is available in 0x1A0[14:13]
5	PHY Control Frames Broadcast Disable	R/W	0h	By default, the device accepts broadcast Phy Control Frames which have a Phy address field of 0x1F. If this bit is set to a 1, the Phy Control Frame must have a Phy Address field that exactly matches the device Phy Address.

Table 8-32. PCF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-1	PHY Control Frames Buffer Size	R/W	0h	Determines the buffer size for transmit to allow Phy Control Frame detection. All packets are delayed as they pass through this buffer. If set to 0, packets are not be delayed and Phy Control frames are truncated after the Destination Address field
0	PHY Control Frames Enable	R/W	0h	Enables register writes using Phy Control Frames

8.2.29 MISC1 Register (Offset = 1A2h) [Reset = 0002h]

MISC1 is shown in Table 8-33.

Return to the Summary Table.

Table 8-33. MISC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6	Swap DA SA	R/W	0h	1b = Swap Destination Address and Source Address fields of the packet for debug
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

8.2.30 PPM0 Register (Offset = 1A3h) [Reset = F423h]

PPM0 is shown in Table 8-34.

Return to the Summary Table.

Table 8-34. PPM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Monitor Clock Count [15:0]	R/W	F423h	Lower 16 bits of Monitor clock counter in PPM Monitor Monitor Clock Count = Refresh period/monitor clock period Refresh period can be any common multiple of monitor and reference clock periods

8.2.31 PPM1 Register (Offset = 1A4h) [Reset = 0000h]

PPM1 is shown in Table 8-35.

Return to the Summary Table.

Table 8-35. PPM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Monitor Clock Count [31:16]	R/W	0h	Higher 16 bits of Monitor clock counter in PPM Monitor Monitor Clock Count = Refresh period/monitor clock period Refresh period can be any common multiple of monitor and reference clock periods

8.2.32 PPM2 Register (Offset = 1A5h) [Reset = 30D3h]

PPM2 is shown in Table 8-36.

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Table 8-36. PPM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Reference Clock Count [15:0]	R/W	30D3h	Lower 16 bits of Reference clock counter in PPM Monitor Reference Clock Count = Refresh period/reference clock period Refresh period can be any common multiple of monitor and reference clock periods

8.2.33 PPM3 Register (Offset = 1A6h) [Reset = 0000h]

PPM3 is shown in Table 8-37.

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Table 8-37. PPM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Reference Clock Count [31:16]	R/W	0h	Higher 16 bits of Reference clock counter in PPM Monitor Reference Clock Count = Refresh period/reference clock period Refresh period can be any common multiple of monitor and reference clock periods

8.2.34 PPM4 Register (Offset = 1A7h) [Reset = 0000h]

PPM4 is shown in Table 8-38.

Return to the Summary Table.

Table 8-38. PPM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PPM Monitor Interrupt Threshold Count - 1 [15:0]	R/W	0h	Lower 16 bits of PPM Monitor Interrupt Threshold Count - 1: PPM Monitor Interrupt Threshold Count 1 = Monitor Clock Count PPM beyond which interrupt must be flagged

8.2.35 PPM5 Register (Offset = 1A8h) [Reset = 0000h]

PPM5 is shown in Table 8-39.

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Table 8-39. PPM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PPM Monitor Interrupt Threshold Count - 1 [31:16]	R/W	0h	Higher 16 bits of PPM Monitor Interrupt Threshold Count -1: PPM Monitor Interrupt Threshold Count 1 = Monitor Clock Count PPM beyond which interrupt must be flagged

8.2.36 PPM6 Register (Offset = 1A9h) [Reset = 0000h]

PPM6 is shown in Table 8-40.

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Table 8-40. PPM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PPM Monitor Interrupt Threshold Count - 2 [15:0]	R/W	0h	Lower 16 bits of PPM Monitor Interrupt Threshold Count - 2: PPM Monitor Interrupt Threshold Count 2 = Monitor clock count - (Monitor Clock Count negative PPM beyond which interrupt must be flagged)

8.2.37 PPM7 Register (Offset = 1AAh) [Reset = 0000h]

PPM7 is shown in Table 8-41.

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Table 8-41. PPM7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PPM Monitor Interrupt Threshold Count - 2 [31:16]	R/W	0h	Higher 16 bits of PPM Monitor Interrupt Threshold Count -2: PPM Monitor Interrupt Threshold Count 2 = Monitor clock count - (Monitor Clock Count negative PPM beyond which interrupt must be flagged)

8.2.38 PPM10 Register (Offset = 1ADh) [Reset = 0000h]

PPM10 is shown in Table 8-42.

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Table 8-42. PPM10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PPM Monitor Output [15:0]	R/W	0h	PPM Monitor output If 0x01AE[15] = 0, ppm offset is negative, if 0x01AE[15] = 1, ppm offset is positive PPM offset of monitor clock = {0x01AE[14:0],0x01AD[15:0]}/ {0x01A4, 0x01A3}

8.2.39 PPM11 Register (Offset = 1AEh) [Reset = 0000h]

PPM11 is shown in Table 8-43.

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Table 8-43. PPM11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PPM Monitor Output [31:16]	R/W	0h	PPM Monitor output If 0x01AE[15] = 0, ppm offset is negative, if 0x01AE[15] = 1, ppm offset is positive PPM offset of monitor clock = {0x01AE[14:0],0x01AD[15:0]}/ {0x01A4, 0x01A3}

8.2.40 PPM12 Register (Offset = 1AFh) [Reset = 0000h]

PPM12 is shown in Table 8-44.

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Table 8-44. PPM12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	PPM Monitor External Clock Select	R/W	0h	Selects GPIO pin for External Clock Input of PPM Monitor: 2h = LED_0 3h = GPIO5
13	PPM Monitor Enable	R/W	0h	Enable for PPM monitor: 0h = Disable PPM Monitor 1h = Enable PPM Monitor
12-9	Reference Clock Select for PPM Monitor	R/W	0h	Selects the reference clock for the PPM monitor 0h = XI Input 1h = 200MHz Recovered Clock 2h = PLL CLK of 250MHz 3h = PTP PLL 4h = External Clock Input 5h = 200MHz Leader Transmit Clock 6h = SGMII Recovered Clock 7h = PTP Trigger 0
8-5	Monitor Clock Select for PPM Monitor	R/W	0h	Selects the monitor clock for the PPM monitor 0h = XI Input 1h = 200MHz Recovered Clock 2h = PLL CLK of 250Mhz 3h = PTP PLL 4h = External Clock Input 5h = 200MHz Leader Transmit Clock 6h = SGMII Recovered Clock 7h = PTP Trigger 0
4	Latch PPM Monitor Value	R/W	0h	Latches the ppm monitor value to a shadow register 0h = Disable PPM Status Read 1h = Enable PPM Status Read
3-2	RESERVED	R	0h	Reserved
1-0	RESERVED	R	0h	Reserved

8.2.41 fwu_reg_3 Register (Offset = 1BEh) [Reset = 0158h]

fwu_reg_3 is shown in Table 8-45.

Return to the Summary Table.

Table 8-45. fwu_reg_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	Fast Wake-Up Memory Load Enable	R/W	0h	Program this bit to 1 to enable loading register address and data into the memory
9	Fast Wake-Up Load Trigger	R/W	0h	Program this bit to 1 after programming register Address and Data in 0x1BC and 0x1BD This bit is auto-clearing
8	Fast Wake-Up Memory Reset	R/W	1h	0h = Reset Memory
7-2	RESERVED	R	0h	Reserved
1-0	RESERVED	R	0h	Reserved

8.2.42 spare_reg_tc10 Register (Offset = 1D2h) [Reset = 0000h]

spare_reg_tc10 is shown in Table 8-46.

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Table 8-46. spare_reg_tc10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Configure Fast Wake-Up	R/W	0h	To enable fast wake-up Memory program 0x01D2 = 0x0004 0x01D2 = 0x0014 0x01D2 = 0x0004

8.2.43 TDR_TC1 Register (Offset = 310h) [Reset = 0000h]

TDR_TC1 is shown in Table 8-47.

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Table 8-47. TDR_TC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7	Fault Detect Status	R	0h	1b = Fault detected in cable 0b = No Fault detected in cable
6	Fault Type	R	0h	0b = Short to GND, supply, or between MDI pins 1b = Open. Applicable to both 1-wire and 2-wire open faults
5-0	TDR Fault Location	R	0h	Fault location in meters (Valid only if Fault Detect Status = 1)

8.2.44 ANA_LD_CTRL_3 Register (Offset = 402h) [Reset = 0000h]

ANA_LD_CTRL_3 is shown in Table 8-48.

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Table 8-48. ANA_LD_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	VDDIO Supply Level	R	0h	VDDIO Level Detected by the PHY: 00b = 1.8V VDDIO 01b = 2.5V VDDIO 11b = 3.3V VDDIO
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11-10	VDDMAC Supply Level	R	0h	VDDIO Level Detected by the PHY: 00b = 1.8V VDDMAC 01b = 2.5V VDDMAC 11b = 3.3V VDDMAC
9-8	RESERVED	R	0h	Reserved
7-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-0	RESERVED	R	0h	Reserved

8.2.45 A2D_REG_48 Register (Offset = 430h) [Reset = 0AA0h]

A2D_REG_48 is shown in Table 8-49.

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Table 8-49. A2D_REG_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved

Table 8-49. A2D_REG_48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RESERVED	R	0h	Reserved
11-8	RGMII TX Shift Delay	R/W	Ah	Controls Internal Delay in RGMII mode in Steps of 312.5ps Delay = ((Bit[7:4] in decimal) + 1) x 312.5 ps
7-4	RGMII RX Shift Delay	R/W	Ah	Controls Internal Delay in RGMII mode in Steps of 312.5ps Delay = ((Bit[7:4] in decimal) + 1) x 312.5 ps
3-0	RESERVED	R	0h	Reserved

8.2.46 A2D_REG_64 Register (Offset = 440h) [Reset = 0001h]

A2D_REG_64 is shown in Table 8-50.

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Table 8-50. A2D_REG_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	ESD Event Counter Disable	R/W	1h	1b = Disable ESD Counter 0b = Enable ESD Counter Toggle this bit to clear the ESD counter

8.2.47 A2D_REG_66 Register (Offset = 442h) [Reset = 0000h]

A2D_REG_66 is shown in Table 8-51.

Return to the Summary Table.

Table 8-51. A2D_REG_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-9	ESD Event Count	R	0h	Field gives the number of ESD events on the copper channel
8	RESERVED	R	0h	Reserved
7-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

8.2.48 A2D_REG_68 Register (Offset = 444h) [Reset = 0000h]

A2D_REG_68 is shown in Table 8-52.

Return to the Summary Table.

Table 8-52. A2D_REG_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	Sleep Force Value	R/W	0h	1b = Force Sleep when Sleep Force Enable is set to 1
2	Sleep Force Enable	R/W	0h	1b = Sleep Force Enable (Sleep Force Value has to be set)

Table 8-52. A2D_REG_68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	WAKE pin Force Value	R/W	0h	Force value on WAKE pin when WAKE pin Force Enable is set 1b = High 0b = Low
0	WAKE pin Force Enable	R/W	0h	1b = Enable Force control of WAKE pin

8.2.49 LEDS_CFG_1 Register (Offset = 450h) [Reset = 2610h]

LEDS_CFG_1 is shown in Table 8-53.

Return to the Summary Table.

Table 8-53. LEDS_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Disable LED Stretching	R/W	0h	0b = LED pulses are stretched according to the blink rate in 'LED Blink Rate' field 1b = LED pulses are directly connected to RX_DV(for RX activity) and TX_CTRL(for TX Activity)
13-12	LED Blink Rate	R/W	2h	Blink Rate of the LED when configured for activity 00b = 20Hz (50 ms) 01b = 10Hz (100 ms) 10b = 5Hz (200 ms) 11b = 2Hz (500 ms)
11-8	LED_2 Options	R/W	6h	0x0 : link OK 0x1 : link OK + blink on TX/RX activity 0x2 : link OK + blink on TX activity 0x3 : link OK + blink on RX activity 0x4 : link OK + 100Base-T1 Leader 0x5 : link OK + 100Base-T1 Follower 0x6 : TX/RX activity with stretch option 0x7 : Reserved 0x8 : Reserved 0x9 : Link lost (remains on until register 0x1 is read) 0xB : xMII TX/RX Error with stretch option
7-4	LED_1 Options	R/W	1h	0x0 : link OK 0x1 : link OK + blink on TX/RX activity 0x2 : link OK + blink on TX activity 0x3 : link OK + blink on RX activity 0x4 : link OK + 100Base-T1 Leader 0x5 : link OK + 100Base-T1 Follower 0x6 : TX/RX activity with stretch option 0x7 : Reserved 0x8 : Reserved 0x9 : Link lost (remains on until register 0x1 is read) 0xB : xMII TX/RX Error with stretch option
3-0	LED_0 Options	R/W	0h	0x0 : link OK 0x1 : link OK + blink on TX/RX activity 0x2 : link OK + blink on TX activity 0x3 : link OK + blink on RX activity 0x4 : link OK + 100Base-T1 Leader 0x5 : link OK + 100Base-T1 Follower 0x6 : TX/RX activity with stretch option 0x7 : Reserved 0x8 : Reserved 0x9 : Link lost (remains on until register 0x1 is read) 0xB : xMII TX/RX Error with stretch option

8.2.50 LEDS_CFG_2 Register (Offset = 451h) [Reset = 0009h]

LEDS_CFG_2 is shown in Table 8-54.

Return to the Summary Table.

Table 8-54. LEDS_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12-9	RESERVED	R	0h	Reserved
8	LED_2 Force Enable	R/W	0h	1b = Force 'LED_2 Force Value' on CLKOUT pin (when CLKOUT is configured as LED_2)
7	LED_2 Force Value	R/W	0h	When LED_2 Force Enable is set, this bit decides the output of LED_2 0b = Low 1b = High
6	LED_2 Polarity	R/W	0h	Polarity of LED_2: (When CLKOUT is used as LED_2) 0b = Active Low polarity 1b = Active High polarity
5	LED_1 Force Enable	R/W	0h	1b = Force 'LED_1 Force Value' on LED_1 pin
4	LED_1 Force Value	R/W	0h	When LED_1 Force Enable is set, this bit decides the output of LED_1 0b = Low 1b = High
3	LED_1 Polarity	R/W	1h	Polarity of LED_1: 0b = Active Low polarity 1b = Active High polarity Default value is decided by the strap on LED_1. If the strap is placed to supply, LED_1 polarity is 0, else LED_1 polarity is 1.
2	LED_0 Force Enable	R/W	0h	1b = Force 'LED_0 Force Value' on LED_0 pin
1	LED_0 Force Value	R/W	0h	When LED_0 Force Enable is set, this bit decides the output of LED_0 0b = Low 1b = High
0	LED_0 Polarity	R/W	1h	Polarity of LED_0: 0b = Active Low polarity 1b = Active High polarity Default value is decided by the strap on LED_0. If the strap is placed to supply, LED_0 polarity is 0, else LED_0 polarity is 1

8.2.51 IO_MUX_CFG_1 Register (Offset = 452h) [Reset = 0000h]

IO_MUX_CFG_1 is shown in Table 8-55.

Return to the Summary Table.

Table 8-55. IO_MUX_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10-8	LED_1 Configuration	R/W	0h	000b = (default: LINK) 010b = WoL 011b = Under-Voltage indication 110b = ESD 111b = interrupt

Table 8-55. IO_MUX_CFG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-0	LED_0 Configuration	R/W	0h	000b = (default: LINK) 010b = WoL 011b = Under-Voltage indication 110b = ESD 111b = interrupt

8.2.52 IO_MUX_CFG_2 Register (Offset = 453h) [Reset = 0001h]

IO_MUX_CFG_2 is shown in Table 8-56.

Return to the Summary Table.

Table 8-56. IO_MUX_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Enable TX_ER on LED_1	R/W	0h	Configures LED_1 pin to TX_ER
14-9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-0	CLKOUT Configuration	R/W	1h	000b = (default: LINK) 010b = WoL 011b = Under-Voltage indication 110b = ESD 111b = interrupt

8.2.53 IO_CONTROL_2 Register (Offset = 455h) [Reset = 0000h]

IO_CONTROL_2 is shown in Table 8-57.

Return to the Summary Table.

Table 8-57. IO_CONTROL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-9	Impedance Control - LED_0, GPIO_5	R/W	0h	00000b - Fast Mode (Default) 00001b - Slow Mode
8-7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4-2	RESERVED	R	0h	Reserved
1-0	RESERVED	R	0h	Reserved

8.2.54 IO_MUX_CFG Register (Offset = 456h) [Reset = 0021h]

IO_MUX_CFG is shown in Table 8-58.

Return to the Summary Table.

Table 8-58. IO_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12-11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-5	Impedance Control - RX pins	R/W	1h	Impedance control for RX_CLK, RX_D[3:0], RX_CTRL, RX_ER 1h = Slew Mode -1 2h = Slew Mode -2 3h = Slew Mode -3 4h = Slew Mode -4 5h = Slew Mode -5 6h = Slew Mode -6 7h = Slew Mode -7
4-0	Impedance Control - TX_CLK	R/W	1h	1h = Slew Mode -1 2h = Slew Mode -2 3h = Slew Mode -3 4h = Slew Mode -4 5h = Slew Mode -5 6h = Slew Mode -6 7h = Slew Mode -7

8.2.55 CHIP_SOR_1 Register (Offset = 45Dh) [Reset = 0000h]

CHIP_SOR_1 is shown in Table 8-59.

Return to the Summary Table.

Table 8-59. CHIP_SOR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	GPIO_4 Strap	R	0h	GPIO_4 strap sampled at power up or reset
14	RESERVED	R	0h	Reserved
13	LED_1 Strap	R	0h	LED_1 strap sampled at power up
12	RX_D3 Strap	R	0h	RX_D3 strap sampled at power up
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	LED0 Strap	R	0h	LED_0 strap sampled at power up or reset
8	RXD3 Strap	R	0h	RX_D3 strap sampled at reset
7	RXD2 Strap	R	0h	RX_D2 strap sampled at power up or reset
6	RXD1 Strap	R	0h	RX_D1 strap sampled at power up or reset
5	RXD0 Strap	R	0h	RX_D0 strap sampled at power up or reset
4	RXCLK Strap	R	0h	RX_CLK strap sampled at power up or reset
3-2	RXER Strap	R	0h	RX_ER strap sampled at power up or reset
1-0	RXDV Strap	R	0h	RX_DV strap sampled at power up or reset

8.2.56 LED1_CLKOUT_ANA_CTRL Register (Offset = 45Fh) [Reset = 000Ch]

LED1_CLKOUT_ANA_CTRL is shown in Table 8-60.

Return to the Summary Table.

Table 8-60. LED1_CLKOUT_ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved

Table 8-60. LED1_CLKOUT_ANA_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RESERVED	R	0h	Reserved
13-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-2	LED_1 Mux Control	R/W	3h	00b = 25MHz XI Clock for daisy chaining 01b = TX_TCLK for test modes 11b = Signal Selected by CLKOUT Configuration
1-0	CLKOUT Mux Control	R/W	0h	00b = 25MHz XI Clock for daisy chaining 01b = TX_TCLK for test modes 11b = Signal Selected by CLKOUT Configuration

8.2.57 IMPEDANCE_CTRL_0 Register (Offset = 460h) [Reset = 0101h]

IMPEDANCE_CTRL_0 is shown in Table 8-61.

Return to the Summary Table.

Table 8-61. IMPEDANCE_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	Impedance Control - CLK_OUT	R/W	1h	1h = Slew Mode -1 2h = Slew Mode -2 3h = Slew Mode -3 4h = Slew Mode -4 5h = Slew Mode -5 6h = Slew Mode -6 7h = Slew Mode -7
7-5	RESERVED	R	0h	Reserved
4-0	Impedance Control - LED_1	R/W	1h	1h = Slew Mode -1 2h = Slew Mode -2 3h = Slew Mode -3 4h = Slew Mode -4 5h = Slew Mode -5 6h = Slew Mode -6 7h = Slew Mode -7

8.2.58 IMPEDANCE_CTRL_1 Register (Offset = 461h) [Reset = 0101h]

IMPEDANCE_CTRL_1 is shown in Table 8-62.

Return to the Summary Table.

Table 8-62. IMPEDANCE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	Impedance Control - GPIO_4	R/W	1h	1h = Slew Mode -1 2h = Slew Mode -2 3h = Slew Mode -3 4h = Slew Mode -4 5h = Slew Mode -5 6h = Slew Mode -6 7h = Slew Mode -7
7-5	RESERVED	R	0h	Reserved

Table 8-62. IMPEDANCE_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	Impedance Control - GPIO_3	R/W	1h	1h = Slew Mode -1 2h = Slew Mode -2 3h = Slew Mode -3 4h = Slew Mode -4 5h = Slew Mode -5 6h = Slew Mode -6 7h = Slew Mode -7

8.2.59 RX_FIFO_CONFIG Register (Offset = 4DFh) [Reset = 0003h]

RX_FIFO_CONFIG is shown in Table 8-63.

Return to the Summary Table.

Table 8-63. RX_FIFO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	cfg_sync_fifo_wr_cnt_rst_val	R/W	3h	

8.2.60 LINKUP_TIMER_1 Register (Offset = 4EEh) [Reset = 0000h]

LINKUP_TIMER_1 is shown in Table 8-64.

Return to the Summary Table.

Table 8-64. LINKUP_TIMER_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Link Up Timer [15:0]	R	0h	Link Up timer calculated from Power-up or Soft Reset or Link Down whichever comes later Link Up time (in ns) = Link Up Timer [31:0]*40

8.2.61 LINKUP_TIMER_2 Register (Offset = 4EFh) [Reset = 0000h]

LINKUP_TIMER_2 is shown in Table 8-65.

Return to the Summary Table.

Table 8-65. LINKUP_TIMER_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Link Up Timer [31:16]	R	0h	Link Up timer calculated from Power-up or Soft Reset or Link Down whichever comes later Link Up time (in ns) = Link Up Timer [31:0]*40

8.2.62 TX_PR_FILT_CTRL Register (Offset = 523h) [Reset = 0000h]

TX_PR_FILT_CTRL is shown in Table 8-66.

Return to the Summary Table.

Table 8-66. TX_PR_FILT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	MDI Polarity Invert	R/W	0h	1b = Invert polarity on MDI transmit side

Table 8-66. TX_PR_FILT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MDI Transmit Disable	R/W	0h	1b = Disable Transmit on MDI 0b = Enable Transmit on MDI

8.2.63 PG_REG_1 Register (Offset = 551h) [Reset = 0010h]

PG_REG_1 is shown in Table 8-67.

Return to the Summary Table.

Table 8-67. PG_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	RMII CRS_DV Config	R/W	1h	Configure Pin 15 as RX_DV or CRS_DV: 1b = Pin15 is CRS_DV 0b = Pin 15 is RX_DV
3-0	RESERVED	R	0h	Reserved

8.2.64 PG_REG_3 Register (Offset = 552h) [Reset = 0008h]

PG_REG_3 is shown in Table 8-68.

Return to the Summary Table.

Table 8-68. PG_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

8.2.65 PG_REG_4 Register (Offset = 553h) [Reset = 0000h]

PG_REG_4 is shown in Table 8-69.

Return to the Summary Table.

Table 8-69. PG_REG_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	Force Receive Polarity Force Enable	R/W	0h	0x0553[13:12] = 2'b10 : Disable Auto-Polarity Correction and force no polarity inversion 0x0553[13:12] = 2'b11 : Disable Auto-Polarity Correction and force polarity inversion
12	Receive polarity Force Value	R/W	0h	0x0553[13:12] = 2'b10 : Disable Auto-Polarity Correction and force no polarity inversion 0x0553[13:12] = 2'b11 : Disable Auto-Polarity Correction and force polarity inversion
11-0	RESERVED	R	0h	Reserved

8.2.66 TC1_LINK_FAIL_LOSS Register (Offset = 561h) [Reset = 0000h]

TC1_LINK_FAIL_LOSS is shown in Table 8-70.

Return to the Summary Table.

Table 8-70. TC1_LINK_FAIL_LOSS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	Link Losses	R	0h	Number of Link Losses as defined in TC1 since last power cycle
9-0	Link Failures	R	0h	Link Failures as defined in TC1 Number of Link Failures (including RX errors, Bad SSD, Bad ESD, Bad SQI) not causing a link down

8.2.67 TC1_LINK_TRAINING_TIME Register (Offset = 562h) [Reset = 0000h]

TC1_LINK_TRAINING_TIME is shown in Table 8-71.

Return to the Summary Table.

Table 8-71. TC1_LINK_TRAINING_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Communication Ready	R	0h	Communication ready as defined in TC1 1b = PHY is ready for communication
14-8	RESERVED	R	0h	Reserved
7-0	Link Training Time	R	0h	Link Training Time measured in milliseconds measured from soft reset

8.2.68 NO_LINK_TH Register (Offset = 563h) [Reset = 0096h]

NO_LINK_TH is shown in Table 8-72.

Return to the Summary Table.

Table 8-72. NO_LINK_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	No Link Timer Threshold	R/W	96h	Time Threshold in milliseconds for No Link Interrupt

8.2.69 DITH_CTRL_0 Register (Offset = 5A0h) [Reset = 3042h]

DITH_CTRL_0 is shown in Table 8-73.

Return to the Summary Table.

Table 8-73. DITH_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	Dithering Direction	R/W	0h	Selects type of Sawtooth profile 0h = Reverse Sawtooth profile 1h = Increasing Sawtooth profile
7-4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

8.2.70 DITH_CTRL_1 Register (Offset = 5A1h) [Reset = 640Dh]

DITH_CTRL_1 is shown in Table 8-74.

Return to the Summary Table.

Table 8-74. DITH_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Dithering Frequency Step	R/W	64h	Configure the maximum frequency offset for dithering 0x05A1[15:8] = (Required (delta(f)/f) *2^{17})/(0x5A1[7:0]) Default delta(f)/f = 1% Keep delta(f)/f limited to ≤ 2%
7-0	Dithering Modulation Period	R/W	Dh	Configures the modulation period for dithering 0x5A1[7:0] = Dithering Modulation Period / 640 ns) Default Modulation Period = 13*640ns = 8.34 us

8.2.71 DITH_RFI_EN_CTRL Register (Offset = 5A8h) [Reset = 0D07h]

DITH_RFI_EN_CTRL is shown in Table 8-75.

Return to the Summary Table.

Table 8-75. DITH_RFI_EN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Dithering Profile	R/W	0h	Select Dithering Frequency Profile 0h = Sawtooth 1h = Triangular
13	RESERVED	R	0h	Reserved
12	Dithering Enable	R/W	0h	1b = Enable Clock Dithering Engine
11	MAC Interface Dithering Enable	R/W	1h	1b = Enable dithering of RMII, RGMII, MII MAC Interface Outputs
10	Core Clocks Dithering Enable	R/W	1h	1b = Enable dithering for Internal Digital clocks
9-0	RESERVED	R	0h	Reserved

8.2.72 CFG_PCF_DMAC_ADDR Register (Offset = 5B2h) [Reset = 0F6Bh]

CFG_PCF_DMAC_ADDR is shown in Table 8-76.

Return to the Summary Table.

Table 8-76. CFG_PCF_DMAC_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	cfg_pcf_dmac_addr	R/W	F6Bh	Configurable last two bytes of PCF DMAC

8.2.73 SPARE_IN_FROM_DIG_SL_1 Register (Offset = 5B7h) [Reset = 0043h]

SPARE_IN_FROM_DIG_SL_1 is shown in Table 8-77.

Return to the Summary Table.

Table 8-77. SPARE_IN_FROM_DIG_SL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reads zero
11-0	spare_in_fromdig_sl_1	R/W	43h	register with configurable bits for analog

8.2.74 CONTROL_REG_1 Register (Offset = 5B8h) [Reset = 0001h]

CONTROL_REG_1 is shown in Table 8-78.

Return to the Summary Table.

Table 8-78. CONTROL_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5	cfg_dith_dis_till_linkup	R/W	0h	1b = Dithering is Disabled till linkup 0b = Dithering enabled before linkup
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2.75 RGMII_CTRL Register (Offset = 600h) [Reset = 002Xh]

RGMII_CTRL is shown in Table 8-79.

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Table 8-79. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0h	Reserved
6-4	RGMII TX FIFO Half Full Threshold	R/W	2h	RGMII TX sync FIFO half full threshold
3	RGMII Enable	R/W	0h	1b = RGMII enable 0b = RGMII Disable Default value is latched from straps
2	Invert RGMII TX Data Lines	R/W	0h	1b = Invert RGMII TXD[3:0] TX_D3 to TX_D0 TX_D2 to TX_D1 TX_D1 to TX_D2 TX_D0 to TX_D3
1	Invert RGMII RX Data Lines	R/W	0h	1b = Invert RGMII RXD[3:0] RX_D3 to RX_D0 RX_D2 to RX_D1 RX_D1 to RX_D2 RX_D0 to RX_D3
0	RESERVED	R	0h	Reserved

8.2.76 RGMII_FIFO_STATUS Register (Offset = 601h) [Reset = 0000h]

RGMII_FIFO_STATUS is shown in Table 8-80.

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Table 8-80. RGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	RGMII TX FIFO Full Error	R	0h	1b = RGMII TX full error has been indicated 0b = No empty fifo error This bit is only cleared on device reset

Table 8-80. RGMII_FIFO_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RGMII TX FIFO Empty Error	R	0h	1b = RGMII TX empty error has been indicated 0b = No empty fifo error This bit is only cleared on device reset

8.2.77 RGMII_CLK_SHIFT_CTRL Register (Offset = 602h) [Reset = 000Xh]

RGMII_CLK_SHIFT_CTRL is shown in Table 8-81.

Return to the Summary Table.

Table 8-81. RGMII_CLK_SHIFT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	RGMII RX Shift	R/W	0h	0b = clock and data are aligned 1b = clock is internally delayed by value programmed in DLL RX Shift Delay
0	RGMII TX Shift	R/W	0h	0b = clock and data are aligned 1b = clock is internally delayed by value programmed in DLL TX Shift Delay

8.2.78 SGMII_CTRL_1 Register (Offset = 608h) [Reset = 0X7Bh]

SGMII_CTRL_1 is shown in Table 8-82.

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Table 8-82. SGMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SGMII TX Error Disable	R/W	0h	1b = Disable SGMII TX Error indication 0b = Enable SGMII TX Error indication
14	RESERVED	R	0h	Reserved
13-10	RESERVED	R	0h	Reserved
9	SGMII Enable	R/W	0h	1b = SGMII enable 0b = SGMII Disable Default value is latched from straps If both SGMII and RGMII are enabled, SGMII take precedence
8	SGMII TX polarity Invert	R/W	0h	1b = Invert SGMII RX_D[3:2] polarity
7	SGMII TX polarity Invert	R/W	0h	1b = Invert SGMII TX_D[1:0] polarity
6-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2-1	RESERVED	R	0h	Reserved
0	SGMII Auto Negotiation Enable	R/W	1h	1b = Enable SGMII Auto-Negotaition 0b = Disable SGMII Auto-Negotiation

8.2.79 SGMII_STATUS Register (Offset = 60Ah) [Reset = 0000h]

SGMII_STATUS is shown in Table 8-83.

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Table 8-83. SGMII_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	SGMII Page Received	R	0h	1b = A new auto neg page received 0b = No new auto neg page received
11	SGMII Link Status	R	0h	1b = SGMII link up 0b = SGMII link down
10	SGMII Auto Negotiation Status	R	0h	1b = SGMII autoneg completed
9	Word Boundary Align Indication	R	0h	1b = Aligned
8	Word Boundary Sync Status	R	0h	1b = sync achieved 0b = sync not achieved
7-4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

8.2.80 SGMII_CTRL_2 Register (Offset = 60Ch) [Reset = 0044h]

SGMII_CTRL_2 is shown in Table 8-84.

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Table 8-84. SGMII_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-4	SGMII TX FIFO Half Full Threshold	R/W	4h	SGMII TX sync FIFO half full threshold
3-0	SGMII RX FIFO Half Full Threshold	R/W	4h	SGMII RX sync FIFO half full threshold

8.2.81 SGMII_FIFO_STATUS Register (Offset = 60Dh) [Reset = 0000h]

SGMII_FIFO_STATUS is shown in Table 8-85.

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Table 8-85. SGMII_FIFO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3	SGMII RX FIFO Full Error	RC	0h	1b = SGMII RX fifo full error has been indicated 0b = No error indication
2	SGMII RX FIFO Empty Error	RC	0h	1b = SGMII RX fifo empty error has been indicated 0b = No error indication
1	SGMII TX FIFO Full Error	RC	0h	1b = SGMII TX fifo full error has been indicated 0b = No error indication
0	SGMII TX FIFO Empty Error	RC	0h	1b = SGMII TX fifo empty error has been indicated 0b = No error indication

8.2.82 PRBS_STATUS_1 Register (Offset = 618h) [Reset = 0000h]

PRBS_STATUS_1 is shown in Table 8-86.

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Table 8-86. PRBS_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	PRBS Error Overflow Counter	R	0h	Holds number of error counter overflow that received by the PRBS checker. Value in this register is locked when write is done to register prbs_status_6 bit[0] or bit[1]. Counter stops on 0xFF. Note: when PRBS counters work in single mode, overflow counter is not active

8.2.83 PRBS_CTRL_1 Register (Offset = 619h) [Reset = 0574h]

PRBS_CTRL_1 is shown in Table 8-87.

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Table 8-87. PRBS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	0h	Reserved
12	Send Packet	R-0/W1S	0h	Enables generating MAC packet with fix/incremental data with CRC (0x619[0] has to be set and 0x619[1] has to be clear) Cleared automatically when pkt_done is set 1b = Transmit MAC packet with CRC 0b = Stop MAC packet
11	RESERVED	R	0h	Reserved
10-8	PRBS Check Select	R/W	5h	Selects the direction of PRBS checker reception 000b = Checker receives from RGMII TX 001b = Checker receives SGMII TX 101b = Checker receives from MDI RX
7	RESERVED	R	0h	Reserved
6-4	PRBS Transmit Select	R/W	7h	Selects the direction of PRBS transmission 000b = PRBS transmits to RGMII RX 001b = PRBS transmits to SGMII RX 101b = PRBS transmits to MDI TX
3	PRBS Count Mode	R/W	0h	1b = Continuous mode, when one of the PRBS counters reaches max value, pulse is generated and counter starts counting from zero again 0b = Single mode, When one of the PRBS counters reaches max value, PRBS checker stops counting.
2	PRBS Checker Enable	R/W	1h	Enable PRBS checker (to receive data) To be enabled for counters in 0x63C, 0x63D, 0x63E to work 1b = Enable PRBS checker
1	PRBS Generation Enable	R/W	0h	If 0x619[0] is set, 1b = Transmits PRBS packet 0b = Transmits non-PRBS packet (PRBS checker is also Disabled in this case)
0	PRBS or Packet Generation Enable	R/W	0h	1b = Enable packet/PRBS generator 0b = Disable packet/PRBS generator

8.2.84 PRBS_CTRL_2 Register (Offset = 61Ah) [Reset = 05DCh]

PRBS_CTRL_2 is shown in Table 8-88.

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Table 8-88. PRBS_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Packet Length	R/W	5DCh	Sets packet length (in bytes) between the PRBS packets or non-PRBS packets generated

8.2.85 PRBS_CTRL_3 Register (Offset = 61Bh) [Reset = 007Dh]

PRBS_CTRL_3 is shown in Table 8-89.

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Table 8-89. PRBS_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	PRBS IPG	R/W	7Dh	Sets IPG (in bytes) between the PRBS packets or non-PRBS packets generated

8.2.86 PRBS_STATUS_2 Register (Offset = 61Ch) [Reset = 0000h]

PRBS_STATUS_2 is shown in Table 8-90.

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Table 8-90. PRBS_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Checker Byte Count	R	0h	Holds number of total bytes that received by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFF This counter is cleared if this counter is read after programming 0x620[1]=1

8.2.87 PRBS_STATUS_3 Register (Offset = 61Dh) [Reset = 0000h]

PRBS_STATUS_3 is shown in Table 8-91.

Return to the Summary Table.

Table 8-91. PRBS_STATUS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Checker Packet Count-1	R	0h	Holds Bits [15:0] of number of total packets received by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x61D,0x61E are read in the same order, after programming 0x620[1]=1

8.2.88 PRBS_STATUS_4 Register (Offset = 61Eh) [Reset = 0000h]

PRBS_STATUS_4 is shown in Table 8-92.

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Table 8-92. PRBS_STATUS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Checker Packet Count-2	R	0h	Holds Bits [31:16] of number of total packets received by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x61D,0x61E are read in the same order, after programming 0x620[1]=1

8.2.89 PRBS_STATUS_5 Register (Offset = 620h) [Reset = 0000h]

PRBS_STATUS_5 is shown in Table 8-93.

Return to the Summary Table.

Table 8-93. PRBS_STATUS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	MAC Packet Gen Done	R	0h	Set when all MAC packets with CRC are transmitted 1b = MAC packets transmission completed 0b = MAC packet transmission in progress
11	MAC Packet Gen Busy	R	0h	1b = Packet generator is in process 0b = Packet generator is not in process
10	PRBS Checker Packet Count Overflow Status	R	0h	If PRBS Checker Packet Count overflows, this status bit is set to 1 This overflow status is cleared after clearing PRBS byte counter using 0x620[1]
9	PRBS Checker Byte Count Overflow Status	R	0h	If PRBS Checker Byte Count overflows, this status bit is set to 1 This overflow status is cleared after clearing PRBS byte counter using 0x620[1]
8	PRBS Lock	R	0h	1b = PRBS checker is locked and synced with the received stream
7-0	PRBS Error Count	R	0h	Writing 1 to bit0 locks all PRBS counters Writing 1 to bit1 locks all PRBS counters and clears the counters on read of those specific registers Bits [1:0] are self-cleared after write Reading Bits[7:0] after writing bit0/bit1, gives the number of error bits received by PRBS checker When PRBS Count Mode set to zero, count stops on 0xFF

8.2.90 PRBS_STATUS_6 Register (Offset = 622h) [Reset = 0000h]

PRBS_STATUS_6 is shown in Table 8-94.

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Table 8-94. PRBS_STATUS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Packer Error Count-1	R	0h	Holds Bits [15:0] of number of total packets received with error by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x622,0x623 are read in the same order, after programming 0x620[1]=1

8.2.91 PRBS_STATUS_7 Register (Offset = 623h) [Reset = 0000h]

PRBS_STATUS_7 is shown in Table 8-95.

Return to the Summary Table.

Table 8-95. PRBS_STATUS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS Packer Error Count-2	R	0h	Holds Bits [31:16] of number of total packets received with error by the PRBS checker Value in register is locked when 0x620[0] or 0x620[1] are written When PRBS Count Mode set to zero, count stops on 0xFFFFFFFF This counter is cleared if 0x622,0x623 are read in the same order, after programming 0x620[1]=1

8.2.92 PRBS_CTRL_4 Register (Offset = 624h) [Reset = 5511h]

PRBS_CTRL_4 is shown in Table 8-96.

Return to the Summary Table.

Table 8-96. PRBS_CTRL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	MAC Packet Data	R/W	55h	Fixed data to be sent when MAC Packet Mode is set to Fixed mode
7-6	MAC Packet Mode	R/W	0h	00b = Incremental 01b = Fixed 10b = PRBS 11b = PRBS
5-3	Pattern Length in MAC Packets	R/W	2h	MAC Packets have Destination Address, Source Address, Programmed Pattern, PRBS/Fixed/Incremental Data The length of Programmed Pattern can be confgured through this register. Pattern can be programmed through 0x625,0x626,0x627 000b = 6 bytes 001b = 1 bytes 010b = 2 bytes 011b = 3 bytes 100b = 4 bytes 101b = 5 bytes 110b = 6 bytes 111b = 6 bytes
2-0	Packet Count for MAC packets Mode	R/W	1h	000b = 1 packet 001b = 10 packets 010b = 100 packets 011b = 1000 packets 100b = 10000 packets 101b = 100000 packets 110b = 1000000 packets 111b = Continuous packets

8.2.93 PATTERN_CTRL_1 Register (Offset = 625h) [Reset = 0000h]

PATTERN_CTRL_1 is shown in Table 8-97.

Return to the Summary Table.

Table 8-97. PATTERN_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Pattern in MAC Packets [15:0]	R/W	0h	Bytes 0,1 of programmable pattern in MAC packets

8.2.94 PATTERN_CTRL_2 Register (Offset = 626h) [Reset = 0000h]

PATTERN_CTRL_2 is shown in Table 8-98.

Return to the Summary Table.

Table 8-98. PATTERN_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Pattern in MAC Packets [31:16]	R/W	0h	Bytes 2,3 of programmable pattern in MAC packets

8.2.95 PATTERN_CTRL_3 Register (Offset = 627h) [Reset = 0000h]

PATTERN_CTRL_3 is shown in Table 8-99.

Return to the Summary Table.

Table 8-99. PATTERN_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Pattern in MAC Packets [47:32]	R/W	0h	Bytes 4,5 of programmable pattern in MAC packets

8.2.96 PMATCH_CTRL_1 Register (Offset = 628h) [Reset = 0000h]

PMATCH_CTRL_1 is shown in Table 8-100.

Return to the Summary Table.

Table 8-100. PMATCH_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Destination Address in MAC Packets [15:0]	R/W	0h	Destination Address field in the generated MAC packets

8.2.97 PMATCH_CTRL_2 Register (Offset = 629h) [Reset = 0000h]

PMATCH_CTRL_2 is shown in Table 8-101.

Return to the Summary Table.

Table 8-101. PMATCH_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Destination Address in MAC Packets [31:16]	R/W	0h	Destination Address field in the generated MAC packets

8.2.98 PMATCH_CTRL_3 Register (Offset = 62Ah) [Reset = 0000h]

PMATCH_CTRL_3 is shown in Table 8-102.

Return to the Summary Table.

Table 8-102. PMATCH_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Destination Address in MAC Packets [47:32]	R/W	0h	Destination Address field in the generated MAC packets

8.2.99 PKT_CRC_STAT Register (Offset = 638h) [Reset = 0000h]

PKT_CRC_STAT is shown in Table 8-103.

Return to the Summary Table.

Table 8-103. PKT_CRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	RX Bad CRC	R	0h	1b = CRC error detected in the packet received from the MDI receiver
0	TX Bad CRC	R	0h	1b = CRC error detected in the packet transmitted on MDI transmitter

8.2.100 TX_PKT_CNT_1 Register (Offset = 639h) [Reset = 0000h]

TX_PKT_CNT_1 is shown in Table 8-104.

Return to the Summary Table.

Table 8-104. TX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TX Packet Count [15:0]	R	0h	Lower 16 bits of TX packets from MAC counter Note : register is cleared when 0x639, 0x63A, 0x63B are read in sequence

8.2.101 TX_PKT_CNT_2 Register (Offset = 63Ah) [Reset = 0000h]

TX_PKT_CNT_2 is shown in Table 8-105.

Return to the Summary Table.

Table 8-105. TX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TX Packet Count [31:16]	R	0h	Upper 16 bits of TX packets from MAC counter Note : register is cleared when 0x639, 0x63A, 0x63B are read in sequence

8.2.102 TX_PKT_CNT_3 Register (Offset = 63Bh) [Reset = 0000h]

TX_PKT_CNT_3 is shown in Table 8-106.

Return to the Summary Table.

Table 8-106. TX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TX Error Packet Count	R	0h	TX packets from MAC with CRC error counter Note : register is cleared when 0x639, 0x63A, 0x63B are read in sequence

8.2.103 RX_PKT_CNT_1 Register (Offset = 63Ch) [Reset = 0000h]

RX_PKT_CNT_1 is shown in Table 8-107.

Return to the Summary Table.

Table 8-107. RX_PKT_CNT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Packet Count [15:0]	R	0h	Lower 16 bits of RX packets received from MDI Note : register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

8.2.104 RX_PKT_CNT_2 Register (Offset = 63Dh) [Reset = 0000h]

RX_PKT_CNT_2 is shown in Table 8-108.

Return to the Summary Table.

Table 8-108. RX_PKT_CNT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Packet Count [31:16]	R	0h	Upper 16 bits of RX packets received from MDI Note : register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

8.2.105 RX_PKT_CNT_3 Register (Offset = 63Eh) [Reset = 0000h]

RX_PKT_CNT_3 is shown in Table 8-109.

Return to the Summary Table.

Table 8-109. RX_PKT_CNT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX Error Packet Count	R	0h	Rx packet w error (CRC error) counter Note : register is cleared when 0x63C, 0x63D, 0x63E are read in sequence

8.2.106 RMII_CTRL_1 Register (Offset = 648h) [Reset = 01X0h]

RMII_CTRL_1 is shown in Table 8-110.

Return to the Summary Table.

Table 8-110. RMII_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9-7	RMII Half Full Threshold	R/W	2h	FIFO Half Full Threshold in nibbles for the RMII Rx FIFO
6	RMII Enable	R/W	0h	1b = RMII Enable
5	RESERVED	R	0h	Reserved
4	RMII Follower Enable	R/W	0h	1b = RMII Follower mode is enabled Not recommended to configure this bit. Can be used as a status bit
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RMII Rev1.0 Enable	R/W	0h	1b = Enable RMII rev1.0
0	RMII Enhanced Mode Enable	R/W	0h	1b = Enable RMII Enhanced mode

8.2.107 RMII_STATUS_1 Register (Offset = 649h) [Reset = 0000h]

RMII_STATUS_1 is shown in Table 8-111.

Return to the Summary Table.

Table 8-111. RMII_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved

Table 8-111. RMII_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RMII FIFO Empty Error	R	0h	Clear on read bit RMII fifo underflow error status
0	RMII FIFO Full Error	R	0h	Clear on Read bit RMII fifo overflow status

8.2.108 PTP_CTL Register (Offset = D00h) [Reset = 0000h]

PTP_CTL is shown in Table 8-112.

Return to the Summary Table.

This register provides basic controls for the PTP 802.1AS operation

Table 8-112. PTP_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-10	Trigger Select	R/W	0h	PTP Trigger Select: This field selects the Trigger for loading control information or for enabling the Trigger. 000b = Trigger-0 001b = Trigger-1 010b = Trigger-2 011b = Trigger-3 100b = Trigger-4 101b = Trigger-5 110b = Trigger-6 111b = Trigger-7
9	Trigger Disable	R/W	0h	Disable PTP Trigger: Setting this bit disables the selected Trigger. This bit does not indicate Disable status for Triggers. Use the PTP Trigger Status register to determine Trigger Status. This bit is self-clearing and always reads back as 0. Disabling a Trigger does not disconnect it from a GPIO pin. The Trigger value is still driven to the GPIO if the Trigger is assigned to a GPIO.
8	Trigger Enable	R/W	0h	Enable PTP Trigger: Setting this bit enables the selected Trigger. This bit does not indicate Enable status for Triggers. Use the PTP Trigger Status register to determine Trigger Status. This bit is self-clearing and always reads back as 0.
7	Trigger Read	R/W	0h	Read PTP Trigger: Setting this bit begins the Trigger Read process. The Trigger is selected based on the setting of the 'Trigger Select' bits in this register. Upon setting this bit, subsequent reads of the PTP_TDR register returns the Trigger Control values. This bit is self-clearing and always reads back as 0.
6	Trigger Load	R/W	0h	Load PTP Trigger: Setting this bit disables the selected Trigger and begin the Trigger load process. The Trigger is selected based on the setting of the 'Trigger Select' bits in this register. Upon setting this bit, subsequent writes to the PTP_TDR sets the Trigger Control fields for the selected Trigger. The Trigger Load is completed after all fields have been written, or the 'Trigger Enable' bit has been set in this register. This bit is self-clearing and reads back as 0 when the Trigger Load is completed either by writing all Trigger Control fields, or by setting the Trigger Enable.

Table 8-112. PTP_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Read PTP Clock	WSC	0h	Read PTP Clock: Setting this bit causes the device to sample the PTP Clock time value. The time value is made available for reading through the PTP_TDR register. This bit is self-clearing and always reads back as 0.
4	Load PTP Clock	WSC	0h	Load PTP Clock: Setting this bit causes the device to load the PTP Clock time value from data previously written to the PTP_TDR register. This bit is self-clearing and always reads back as 0.
3	Step PTP Clock	R/W	0h	Step PTP Clock: Setting this bit causes the device to add a value to the PTP Clock. The value to be added is the value previously written to the PTP_TDR register. This bit is self-clearing and always reads back as 0.
2	PTP Enable	R/W	0h	Enable PTP Clock: Setting this bit enables the PTP Clock. Reading this bit returns the current enabled value. Writing a 0 to this bit has no effect.
1	PTP Disable	R/W	0h	Disable PTP Clock: Setting this bit disables the PTP Clock. Writing a 0 to this bit has no effect. This bit is self-clearing and always reads back as 0.
0	PTP Reset	R/W	0h	Reset PTP Clock: Setting this bit resets the PTP Clock and associated logic. In addition, the 802.1AS registers are reset, with the exception of the PTP_COC and PTP_CLKSRC registers. Unlike other bits in this register, this bit is not self-clearing and must be written to 0 to release the clock and logic from reset.

8.2.109 PTP_TDR Register (Offset = D01h) [Reset = 0000h]

PTP_TDR is shown in Table 8-113.

Return to the Summary Table.

This register provides a mechanism for reading and writing the 802.1AS Time and Trigger Control values. The function of this register is determined by controls in the PTP control register

Table 8-113. PTP_TDR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Time Data	R/W	0h	Time Data: On Reads, successively returns 16-bit values of the Clock time or Trigger Control information as selected by controls in the PTP Control register. Additional reads beyond the available fields always returns 0. On Writes, successively stores the 16-bit values of Clock time or Trigger Control Information as selected by controls in the PTP Control register.

8.2.110 PTP_STS Register (Offset = D02h) [Reset = 0000h]

PTP_STS is shown in Table 8-114.

Return to the Summary Table.

This register provides basic status and interrupt control for the 802.1AS PTP operation.

Table 8-114. PTP_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved

Table 8-114. PTP_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TX Timestamp Ready	R	0h	Transmit Timestamp Ready: A Transmit Timestamp is available for an outbound PTP Message. This bit is cleared upon read of the Transmit Timestamp if no other timestamps are ready.
10	RX Timestamp Ready	R	0h	Receive Timestamp Ready: A Receive Timestamp is available for an inbound PTP Message. This bit is cleared upon read of the Receive Timestamp if no other timestamps are ready.
9	Trigger Done	R	0h	PTP Trigger Done: A PTP Trigger has occurred. This bit is cleared upon read. This bit is only set if Trigger Notification is turned on for the Trigger through the Trigger Configuration registers. Note that if periodic trigger is set, this interrupt does not get asserted unless the programmed trigger has resulted in a erroneous condition. If TRIG_IF_LATE bit is set, even an erroneous condition does not give out an interrupt
8	Event Ready	R	0h	PTP Event Timestamp Ready: A PTP Event Timestamp is available. This bit is cleared upon read of the PTP Event Status register if no other event timestamps are ready.
7-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	TX Timestamp Ready Interrupt Enable	R/W	0h	Enable Transmit Timestamp Interrupt: Enable Interrupt on Transmit Timestamp Ready.
2	RX Timestamp Ready Interrupt Enable	R/W	0h	Enable Receive Timestamp Interrupt: Enable Interrupt on Receive Timestamp Ready.
1	Trigger Done Interrupt Enable	R/W	0h	Enable Trigger Interrupt: Enable Interrupt on Trigger Completion.
0	Event Ready Enable	R/W	0h	Enable Event Interrupt: Enable Interrupt on Event Timestamp Ready.

8.2.111 PTP_TSTS Register (Offset = D03h) [Reset = 0000h]

PTP_TSTS is shown in Table 8-115.

Return to the Summary Table.

This register provides status of the 802.1AS PTP Triggers. The bits in this register indicate the current status for each of the Trigger modules. The error bits are set if the associated notification enable (TRIG_NOTIFY) is set in the PTP Trigger Configuration Registers

Table 8-115. PTP_TSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Trigger-7 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
14	Trigger-7 Active Status	R	0h	This bit indicates that the Trigger is enabled and has not completed.
13	Trigger-6 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
12	Trigger-6 Active Status	R	0h	This bit indicates that the Trigger is enabled and has not completed.
11	Trigger-5 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
10	Trigger-5 Active Status	R	0h	This bit indicates that the Trigger is enabled and has not completed.

Table 8-115. PTP_TSTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	Trigger-4 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
8	Trigger-4 Active Status	R	0h	This bit indicates that the Trigger is enabled and has not completed.
7	Trigger-3 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
6	Trigger-3 Active Status	R	0h	This bit indicates that the Trigger is enabled and has not completed.
5	Trigger-2 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
4	Trigger-2 Active Status	R	0h	This bit indicates that the Trigger is enabled and has not completed.
3	Trigger-1 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
2	Trigger-1 Active Status	R	0h	This bit indicates the Trigger is enabled and has not completed.
1	Trigger-0 Error Indication	R	0h	This bit indicates that the Trigger was improperly programmed to trigger at a time prior to the current time. This bit is cleared when the Trigger is Disabled and/ or rearmed.
0	Trigger-0 Active Status	R	0h	This bit indicates that the Trigger is enabled and has not completed.

8.2.112 PTP_RATEL Register (Offset = D04h) [Reset = 0000h]

PTP_RATEL is shown in Table 8-116.

Return to the Summary Table.

This register contains the low 16-bits of the PTP Rate control. The PTP Rate Control indicates a positive or negative adjustment to the reference clock period in units of 2^{-32} ns. On each reference clock cycle, the PTP Clock is adjusted by adding ref_clk_period +/- PTP_Rate. Write the PTP Rate as PTP_RATEH, followed by PTP_RATEL. The rate takes effect on the write to the PTP_RATEL register

Table 8-116. PTP_RATEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Rate Control Low	R/W	0h	PTP Rate Control Low 16-bits: Writing to this register sets the low 16-bits of the Rate Control value. The Rate Control value is in units of 2^{-32} ns. Upon writing to this register, the full Rate Control value is loaded to the device.

8.2.113 PTP_RATEH Register (Offset = D05h) [Reset = 0000h]

PTP_RATEH is shown in Table 8-117.

Return to the Summary Table.

This register contains the upper 10-bits of the 26-bit PTP Rate control. In addition, it contains a direction control to indicate whether the device is operating faster or slower than the reference clock frequency. When setting the PTP Rate, write this register first, followed by a write to the PTP_RATEL register. The rate takes effect on the write to the PTP_RATEL register.

Table 8-117. PTP_RATEH Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PTP Rate Direction	R/W	0h	The setting of this bit controls whether the device operates at a higher or lower frequency than the reference clock. 0h = The PTP RATE value is added to the clock on every cycle indicating Lower Frequency 1h = The PTP RATE value is subtracted from the clock on every cycle indicating Higher Frequency
14	Temporary Rate Enable	R/W	0h	PTP Temporary Rate: Setting this bit causes the rate to be applied to the clock for the duration set in the PTP Temporary Rate Duration register (PTP_TRD). 0h = Normal Rate 1h = Temporary Rate
13-10	RESERVED	R	0h	Reserved
9-0	PTP Rate Control High	R/W	0h	PTP Rate Control High 10-bits: Writing to this register sets the high 10-bits of the Rate Control value. The Rate Control value is in units of 2^{-32} ns.

8.2.114 PTP_TXTS Register (Offset = D08h) [Reset = 0000h]

PTP_TXTS is shown in Table 8-118.

Return to the Summary Table.

This register provides a mechanism for reading the Transmit Timestamp. The fields are read in the following order:
Timestamp_ns [15:0];
Overflow_cnt[1:0], Timestamp_ns[29:16];
Timestamp_sec[15:0],
Timestamp_sec[31:16]
The Overflow_cnt value indicates if timestamps were dropped due to an overflow of the Transmit Timestamp queue. The overflow counter sticks at a value of three if additional timestamps were missed.
Note:
Each Transmit Timestamp information consists of Four reads. TXTS_RDY status (0xD02, Bit-11) is required to be read to access the next available Transmit Timestamp information.

Table 8-118. PTP_TXTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP TX Timestamp	R	0h	PTP Transmit Timestamp: Reading this register returns the Transmit Timestamp in four 16-bit reads.

8.2.115 PTP_RXTS Register (Offset = D09h) [Reset = 0000h]

PTP_RXTS is shown in Table 8-119.

Return to the Summary Table.

This register provides a mechanism for reading the Receive Timestamp and identification information. The fields are read in the following order:
Timestamp_ns [15:0]
Overflow_cnt[1:0], Timestamp_ns[29:16]
Timestamp_sec[15:0]
Timestamp_sec[31:16]
sequenceId[15:0]
messageType[3:0], source_hash[11:0]

The Overflow_cnt value indicates if timestamps were dropped due to an overflow of the Transmit Timestamp queue. The overflow counter sticks at a value of three if additional timestamps were missed.
Note:
Each Receive Timestamp information consists of Six reads. RXTS_RDY status (0xD02, Bit-12) is required to be read to access the next available Receive Timestamp information.

Table 8-119. PTP_RXTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP RX Timestamp	R	0h	PTP Receive Timestamp: Reading this register returns the Receive Timestamp and identification information in successive 16-bit reads.

8.2.116 PTP_ESTS Register (Offset = D0Ah) [Reset = 0000h]

PTP_ESTS is shown in Table 8-120.

Return to the Summary Table.

This register provides Status for the Event Timestamp unit. Reading this register provides status for the next Event Timestamp contained in the Event Data Register. If this register is 0, no Event Timestamp is available in the Event Data Register. Reading this register automatically moves to the next Event in the queue.

Table 8-120. PTP_ESTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10-8	Events Missed Counter	R	0h	Number of Events Missed: Indicates number of events have been missed prior to this timestamp for the EVNT_NUM indicated. This count value sticks at 7 if more than 7 events are missed.
7-6	Event Timestamp Change Length	R	0h	Event Timestamp Length: Indicates length of the Timestamp field in 16-bit words minus 1. Although all fields are available, this indicates how many of the fields contain data different from the previous Event Timestamp. This allows software to avoid reading more significant fields if they have not changed since the previous timestamp. This field is valid for both single and multiple events. The following shows the number of least significant fields which have new data for each setting 0h = One 16-bit field is new (Timestamp_ns[15:0]) 1h = Two 16-bit fields are new 2h = Three 16-bit fields are new 3h = All four 16-bit fields are new
5	Event Edge Detected	R	0h	Event edge configuration: Indicates whether the event is a rise or falling event. If the 'Multiple Event Detected' bit is set to 1, this bit indicates the Rise/Fall direction for the event indicated by EVNT_NUM. 0h = Falling edge detected 1h = Rising edge detected
4-2	Event Number Detected	R	0h	Event Number: Indicates Event Timestamp Unit which detected an event. If the 'Multiple Event Detected' bit is 1, this indicates the lowest event number captured. If events have been missed prior to this timestamp, it indicates the lowest event number captured which had at least one missed event.
1	Multiple Events Detected	R	0h	Multiple Event Detect: Indicates multiple events were detected at the same time. If multiple events are detected, an extended event status field is available as the first data read from the Event Data register. 0h = Single event detected 1h = Multiple events detected

Table 8-120. PTP_ESTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PTP Event Detected	R	0h	Indicates an Event has been detected by one of the Event Timestamp Units

8.2.117 PTP_TRIG Register (Offset = D10h) [Reset = 0000h]

PTP_TRIG is shown in Table 8-121.

Return to the Summary Table.

This register provides basic configuration for IEEE 802.1AS Triggers. To write configuration to a trigger, set the TRIG_WR bit along with the TRIG_SEL and other control information. To read configuration from a trigger, set the TRIG_SEL encoding to the trigger desired, and set the TRIG_WR bit to 0. The subsequent read of the PTP_TRIG register returns the configuration information.
Note:
A Pulse is seen in case toggle trigger is set with trig_if_late condition.
In trig_if_late condition, pulse trigger doesnt give pulse of the configured width.

Table 8-121. PTP_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Trigger Pulse Select	R/W	0h	Trigger Pulse: Setting this bit causes the trigger to generate a pulse rather than a single rising or falling edge.
14	Trigger Periodic Enable	R/W	0h	Trigger Periodic: Setting this bit causes the trigger to generate a periodic signal. If this bit is 0, the trigger generates a single Pulse or Edge depending on the Trigger Control settings.
13	Trigger If Late	R/W	0h	Trigger-if-late Control: Setting this bit allows an immediate trigger in the event the trigger is programmed to a time value which is less than the current time. This provides a mechanism for generating an immediate trigger or to immediately begin generating a periodic signal. For a periodic signal, no notification is generated if this bit is set and a late trigger occurs. Only use this function for Trigger 0 or Trigger 1. This bit has to be programmed before loading the trigger (loading the timestamp).
12	Trigger Notification Enable	R/W	0h	Trigger Notification Enable: Setting this bit enables trigger status to be reported on completion of a trigger or on an error detection due to late trigger. If trigger interrupts are enabled, the notification also results in an interrupt being generated.
11-8	Trigger GPIO Select	R/W	0h	GPIO trigger output configuration: Setting this field to a non-zero value connects the trigger to the associated GPIO pin. 0h = No GPIO is selected 1h = LED_0 2h = LED_1 3h = RX_ER 4h = CLKOUT 5h = GPIO_3 6h = GPIO_4 7h = GPIO_5
7	Trigger Toggle Mode	R/W	0h	Trigger Toggle mode enable: Setting this bit puts the trigger into toggle mode. In toggle mode, the initial value is ignored and the trigger output is toggled at the trigger time.
6-4	RESERVED	R	0h	Reserved
3-1	Trigger Select	R/W	0h	Trigger Configuration Select: This field selects the trigger for configuration read or write.

Table 8-121. PTP_TRIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Trigger Configuration Write	R/W	0h	Trigger Configuration Write: Setting this bit generates a Configuration Write to the selected trigger. This bit is self-clear bit and always reads back as 0.

8.2.118 PTP_EVNT Register (Offset = D11h) [Reset = 0000h]

PTP_EVNT is shown in Table 8-122.

Return to the Summary Table.

This register provides basic configuration for IEEE 802.1AS Events. To write configuration to an Event Timestamp Unit, set the EVNT_WR bit along with the EVNT_SEL and other control information. To read configuration from an Event Timestamp Unit, set the EVNT_SEL encoding to the Event desired, and set the EVNT_WR bit to 0. The subsequent read of the PTP_EVNT register returns the configuration information.

Table 8-122. PTP_EVNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Event Rise Detect Enable	R/W	0h	Event Rise Detect Enable: Enable detection of a rising edge transition on the selected event input.
13	Event Fall Detect Enable	R/W	0h	Event Fall Detect Enable: Enable detection of a falling edge transition on the selected event input.
12	Single Event Capture	R/W	0h	Single Event Capture: Setting this bit to a 1 enables single event capture operation. The EVNT_RISE and EVNT_FALL are cleared upon a valid event timestamp capture.
11-8	Event GPIO Select	R/W	0h	GPIO event capture configuration: Setting this field to a non-zero value connects the event to the associated GPIO pin. This field can also be used to capture events based on trigger outputs or AVB clock outputs 0h = No GPIO is selected 1h = LED_0 2h = LED_1 3h = RX_ER 4h = CLKOUT 5h = GPIO_3 6h = GPIO_4 7h = GPIO_5 8h = Media Clock 9h = Codec Clock Ah = Bit Clock Bh = Trigger 0 Ch = Trigger 1
7-4	RESERVED	R	0h	Reserved
3-1	Event Select	R/W	0h	Event Select: This field selects the Event Timestamp Unit for configuration read or write. 000b = Event-0 001b = Event-1 010b = Event-2 011b = Event-3 100b = Event-4 101b = Event-5 110b = Event-6 111b = Event-7

Table 8-122. PTP_EVNT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Event Configuration Write	R/W	0h	Event Configuration Write: Setting this bit generates a Configuration Write to the selected Event Timestamp Unit.

8.2.119 PTP_TXCFG0 Register (Offset = D12h) [Reset = 0000h]

PTP_TXCFG0 is shown in Table 8-123.

Return to the Summary Table.

This register provides configuration for IEEE 802.1AS Transmit Timestamp operation.

Table 8-123. PTP_TXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Sync Message One-Step Enable	R/W	0h	Sync Message One-Step Enable: Enable automatic insertion of timestamp into transmit Sync Messages. Device automatically parses message and insert the timestamp in the correct location. UDP checksum and CRC fields is regenerated.
14	TX TimeStamp Info Enable	R/W	0h	Enable latching of message type, hash value, sequence id along with Timestamp for transmit event packets and transmit these fields through PSF
13	Insert Delay Request	R/W	0h	Insert Delay_Req timestamp in Delay_Resp: If this bit is set to a 1, the device inserts the timestamp for transmitted Delay_Req messages into inbound Delay_Resp messages. The most recent timestamp is used for any inbound Delay_Resp message. The receive timestamp insertion logic must be enabled through the PTP Receive Configuration registers.
12	NTP Timestamp Enable	R/W	0h	Enable Timestamping of NTP Packets: If this bit is set to 0, the device checks the UDP protocol field for a PTP Event message (value 319). If this bit is set to 1, the device checks the UDP protocol field for an NTP message (value 123). This setting applies to the transmit and receive packet parsing engines.
11	Ignore Two-Step Flag	R/W	0h	Ignore Two_Step flag for One-Step operation: If this bit is set to a 0, the device does not insert a timestamp if the Two_Step bit is set in the flags field of the PTP header. If this bit is set to 1, the device inserts a timestamp independent of the setting of the Two_Step flag.
10	Disable CRC One-Step	R/W	0h	Disable checking of CRC for One-Step operation: If this bit is set to a 0, the device forces a CRC error for One-Step operation if the incoming frame has a CRC error. If this bit is set to a 1, the device sends the One-Step frame with a valid CRC, even if the incoming CRC is invalid.
9	Checksum Correction One-Step	R/W	0h	Enable UDP Checksum correction for One-Step Operation: Enables correction of the UDP checksum for messages which include insertion of the timestamp. The checksum is corrected by modifying the last two bytes of the UDP data. The last two bytes must be transmitted by the MAC as 0s. This control must be set for proper IPv6/UDP One-Step operation. This control has no effect for Layer2 Ethernet messages.
8	IP Address Filter	R/W	0h	Enable IEEE 802.1AS defined IP address filter: Enable filtering of UDP/IP Event messages using the IANA assigned IP Destination addresses. If this bit is set to 1, packets with IP Destination addresses which do not match the IANA assigned addresses is not timestamped. This field affects operation for both IPv4 and IPv6. If this field is set to 0, IP destination addresses is ignored.

Table 8-123. PTP_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	Layer2 Timestamp Enable	R/W	0h	Layer2 Timestamp Enable: Enables detection of IEEE 802.3/Ethernet encapsulated PTP event messages.
6	IPv6 Timestamp Enable	R/W	0h	IPv6 Timestamp Enable: Enables detection of UDP/IPv6 encapsulated PTP event messages.
5	IPv4 Timestamp Enable	R/W	0h	IPv4 Timestamp Enable: Enables detection of UDP/IPv4 encapsulated PTP event messages.
4-1	PTP Version	R/W	0h	PTP Version: Enable Timestamp capture for a specific version of the IEEE 802.1AS specification. This field can be programmed to any value between 1 and 15 and allows support for future versions of the IEEE 802.1AS specification. A value of 0 disables version checking (not recommended).
0	Transmit Timestamp Enable	R/W	0h	Transmit Timestamp Enable: Enable Timestamp capture for Transmit.

8.2.120 PTP_TXCFG1 Register (Offset = D13h) [Reset = 0000h]

PTP_TXCFG1 is shown in Table 8-124.

Return to the Summary Table.

This register provides data and mask fields to filter the first byte in a PTP Message. This function is disabled if all the mask bits are set to 0.

Table 8-124. PTP_TXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Transmit Byte0 Mask	R/W	0h	Byte0 Mask: Bit mask to be used for matching Byte0 of the PTP Message. A one in any bit enables matching for the associated data bit. If no matching is required, set all bits of the mask to 0
7-0	Transmit Byte0 Data	R/W	0h	Byte0 Data: Data to be used for matching Byte0 of the PTP Message.

8.2.121 PSF_CFG0 Register (Offset = D14h) [Reset = 4700h]

PSF_CFG0 is shown in Table 8-125.

Return to the Summary Table.

This register provides configuration for the Phy Status Frame function.

Table 8-125. PSF_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	PSF Termination Field Addition Enable	R/W	1h	1b = Enable addition of termination field for PSF packets
13	RESERVED	R	0h	Reserved
12-11	PSF MAC Source Address	R/W	0h	Phy Status Frame Mac Source Address: 0h = Use Mac Address [08 00 17 0B 6B 0F] 1h = Use Mac Address [08 00 17 00 00 00] 2h = Use Mac Multicast Dest Address 3h = Use Mac Address [00 00 00 00 00 00]
10-8	PSF Minimum Preamble	R/W	7h	Phy Status Frame minimum preamble: Determines the minimum preamble bytes required for sending packets on the MII interface. TI recommends that this be set to the smallest value the MAC tolerates.

Table 8-125. PSF_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PSF Endian Control	R/W	0h	Phy Status Frame Endian control: For each 16-bit field in a Status Message, the data is normally be presented in network byte order (Most significant byte first). If this bit is set to a 1, the byte data fields is reversed so that the least significant byte is first.
6	PSF Packet Type	R/W	0h	This bit controls the type of packet used for Phy Status Frames: 0h = Layer2 Ethernet packets 1h = IPv4 packets.
5	PSF Delivery Enable	R/W	0h	Phy Control Frame Read Phy Status Frame enable: Enable Phy Status Frame delivery of Phy Control Frame read data. Data read through a Phy Control Frame returns in a Phy Status Frame.
4	PSF Error Delivery Enable	R/W	0h	PSF Error Phy Status Frame enable: Enable Phy Status Frame delivery of Phy Status Frame Errors. This bit does not independently enable Phy Status Frame operation. One of the other enable bits must be set for Phy Status Frames to be generated.
3	PSF TX Timestamp Enable	R/W	0h	Transmit Timestamp Phy Status Frame enable: Enable Phy Status Frame delivery of Transmit Timestamps.
2	PSF RX Timestamp Enable	R/W	0h	Receive Timestamp Phy Status Frame enable: Enable Phy Status Frame delivery of Receive Timestamps.
1	PSF Trigger Enable	R/W	0h	Trigger Phy Status Frame enable: Enable Phy Status Frame delivery of Trigger Status.
0	PSF Event Enable	R/W	0h	Event Phy Status Frame enable: Enable Phy Status Frame delivery of Event Timestamps.

8.2.122 PTP_RXCFG0 Register (Offset = D15h) [Reset = 0000h]

PTP_RXCFG0 is shown in Table 8-126.

Return to the Summary Table.

This register provides configuration for IEEE 802.1AS Receive Timestamp operation.

Table 8-126. PTP_RXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Domain Match Enable	R/W	0h	Domain Match Enable: If set to 1, the Receive Timestamp unit requires the domain Number field (octet 4) of the PTP Header to match the value programmed in the PTP_DOMAIN field of the PTP_RXCFG3 register. If set to 0, the Receive Timestamp ignores the PTP_DOMAIN field.
14	Alternate Leader Timestamp Enable	R/W	0h	Alternate Leader Timestamp Disable: Disables Timestamp generation if the Alternate_Leader flag is set. 0h = Ignore Alternate_Leader flag 1h = Do not generate Timestamp if Alternate_Leader is 1
13	IP Address Data Select	R/W	0h	IP Address data select: Selects portion of IP address accessible through the PTP_RXCFG2 register. 0h = Two Most Significant Octets 1h = Two Least Significant Octets
12	User Programmed IP Address Filter Enable	R/W	0h	Enable User-programmed IP address filter: Enable detection of UDP/IP Event messages using a programmable IP address. The IP Address is set using the PTP_RXCFG2 register.

Table 8-126. PTP_RXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	PTP Receive Follower Only	R/W	0h	Receive Follower Only: By default, the Receive Timestamp Unit provides Timestamps for event messages meeting other requirements. Setting this bit to a 1 prevents Delay_Req messages from being Timestamped by requiring that the Control Field (offset 32 in the PTP message) be set to a value other than 1.
10-8	IP Address Filters Enable	R/W	0h	Enable IEEE 802.1AS defined IP address filters: Enable detection of UDP/IP Event messages using the IANA assigned IP Destination addresses. This field affects operation for both IPv4 and IPv6. A Timestamp is captured for the PTP message if the IP destination address matches the following: bxx1 : Dest IP address is 224.0.1.129 bx1x : Dest IP address is 224.0.1.130 - 132 b1xx : Dest IP address is 224.0.0.107
7	L2 Timetamp Enable	R/W	0h	Layer2 Timestamp Enable: Enables detection of IEEE 802.3/Ethernet encapsulated PTP event messages.
6	IPv6 Timestamp Enable:	R/W	0h	IPv6 Timestamp Enable: Enables detection of UDP/IPv6 encapsulated PTP event messages.
5	IPv4 Timestamp Enable:	R/W	0h	IPv4 Timestamp Enable: Enables detection of UDP/IPv4 encapsulated PTP event messages.
4-1	RX PTP Version	R/W	0h	PTP Version: Enable Timestamp capture for a specific version of the IEEE 802.1AS specification. This field can be programmed to any value between 1 and 15 and allows support for future versions of the IEEE 802.1AS specification. A value of 0 disables version checking (not recommended).
0	Receive Timestamp Enable	R/W	0h	Receive Timestamp Enable: Enable Timestamp capture for Receive.

8.2.123 PTP_RXCFG1 Register (Offset = D16h) [Reset = 0000h]

PTP_RXCFG1 is shown in Table 8-127.

Return to the Summary Table.

This register provides data and mask fields to filter the first byte in a PTP Message. This function is disabled if all the mask bits are set to 0.

Table 8-127. PTP_RXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	Receive Byte0 Mask	R/W	0h	Byte0 Mask: Bit mask to be used for matching Byte0 of the Receive PTP Message. A one in any bit enables matching for the associated data bit. If no matching is required, set all bits of the mask to 0.
7-0	Receive Byte0 Data	R/W	0h	Byte0 Data: Data to be used for matching Byte0 of the Receive PTP Message.

8.2.124 PTP_RXCFG2 Register (Offset = D17h) [Reset = 0000h]

PTP_RXCFG2 is shown in Table 8-128.

Return to the Summary Table.

This register provides for programming an IP address to be used for filtering packets to detect PTP Event Messages. Since the IPv4 address is 32-bits, to write an IP address, software must write two 16-bit values. The

USER_IP_SEL bit in the PTP_RXCFG0 register selects which octect of the IP address are accessible through this register.
For example, to write an IP address of 224.0.1.129, software must do the following:
1. Set USER_IP_SEL bit in PTP_RXCFG0 register to 0
2. Write 0xE000 (224.00) to PTP_RXCFG2
3. Set USER_IP_SEL bit in the PTP_RXCFG0 register to 1
4. Write 0x0181 (01.129) to PTP_RXCFG2
Reading this register returns the IP address field selected by USER_IP_SEL.

Table 8-128. PTP_RXCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Receive IP Address Data	R/W	0h	Receive IP Address Data: 16-bits of the IP Address field to be read or written. The 'IP Address Data Select' bit in the PTP_RXCFG0 register selects the portion of the IP address is to be read or written. - 'IP Address Data Select' in RX_CFG0 == 0 -> set MSB 2 bytes of IPv4/IPv6 Addr in PTP_RXCFG2 register in the normal byte format. - 'IP Address Data Select' in RX_CFG0 == 1 -> set LSB 2 bytes of IPv4/IPv6 Address in PTP_RXCFG2 register in the normal byte format. When IPv4, the complete ip address can be set, when IPv6 only MSB 2 bytes of the 16 byte address and LSB 2 bytes of the 16 byte address are compared.

8.2.125 PTP_RXCFG3 Register (Offset = D18h) [Reset = C000h]

PTP_RXCFG3 is shown in Table 8-129.

Return to the Summary Table.

This register provides extended configuration for IEEE 802.1AS Receive Timestamp operation.

Table 8-129. PTP_RXCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RX Minimum IFG after Timestamp	R/W	Ch	Minimum Inter-frame Gap: When a Timestamp is appended to a PTP Message, the length of the packet can get extended. This could reduce the Inter-frame Gap (IFG) between packets by as much as 8-byte times (6400 ns at 10 Mb, 640 ns at 100 Mb, 64 ns at 1G). This field sets a minimum on the IFG between packets in number of byte times. If the IFG is set larger than the actual IFG, Preamble bytes of the subsequent packet gets dropped. Set this value to the lowest possible value that the attached MAC can support.
11	Timestamp on Checksum Error	R/W	0h	Record Timestamp if UDP Checksum Error: By default, Timestamps is discarded for packets with UDP Checksum errors. If this bit is set, the Timestamp is made available in the normal manner.
10	Timestamp on CRC Error	R/W	0h	Record Timestamp if CRC Error: By default, Timestamps is discarded for packets with CRC errors. If this bit is set, the Timestamp is made available in the normal manner.
9	RESERVED	R	0h	Reserved
8	Insert Timestamp	R/W	0h	Enable Timestamp Insertion: Enables Timestamp insertion into a packet containing a PTP Event Message. If this bit is set, the Timestamp does not available through the PTP Receive Timestamp register.

Table 8-129. PTP_RXCFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	PTP Domain Matching Value	R/W	0h	PTP Domain Value: Value of the PTP Message domainNumber field. If PTP_RXCFG0:DOMAIN_EN is set to 1, the Receive Timestamp unit only captures a Timestamp if the domainNumber in the receive PTP message matches the value in this field. If the DOMAIN_EN bit is set to 0, the domainNumber field is ignored.

8.2.126 PTP_RXCFG4 Register (Offset = D19h) [Reset = 0000h]

PTP_RXCFG4 is shown in Table 8-130.

Return to the Summary Table.

This register provides extended configuration for IEEE 802.1AS Receive Timestamp operation. Disable Timestamp insertion using (through PTP_RXCFG3[8]) prior to changing any of the fields in this register.

Table 8-130. PTP_RXCFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	IPV4 UDP Checksum Modify	R/W	0h	Enable IPV4 UDP modification: When timestamp insertion is enabled, this bit controls how UDP checksums are handled for IPV4 PTP event messages. If set to a 0, the device clears the UDP checksum. If a UDP checksum error is detected the device forces a CRC error. If set to a 1, the device does not clear the UDP checksum. Instead it generates a 2-byte value to correct the UDP checksum and append this immediately following the PTP message. If an incoming UDP checksum error is detected, the device causes a UDP checksum error in the modified field. Only use this function if the incoming packets contain two extra bytes of UDP data following the PTP message. Do not enable this for systems using version 1 of the IEEE 802.1AS specification.
14	Seconds Timestamp Enable	R/W	0h	Enable Timestamp Seconds: Setting this bit to a 1 enables inserting a seconds field when Timestamp Insertion is enabled. If set to 0, only the nanoseconds portion of the Timestamp is inserted in the packet. This bit is ignored if 'Insert Timestamp' is 0. This bit is applicable for insertion of timestamps into PTP.
13-12	Seconds Timestamp Length	R/W	0h	Inserted Timestamp Seconds Length: For a PTP message, this field indicates the length of the Seconds field to be inserted in the PTP message. This field is ignored if 'Insert Timestamp' is 0 or if TS_SEC_EN is 0. 0h = Least Significant Byte only of Seconds field 1h = Two Least Significant Bytes of Seconds field 2h = Three Least Significant Bytes of Seconds field 3h = All four Bytes of Seconds field
11-6	RX Timestamp nanosec Field Offset	R/W	0h	Receive Timestamp Nanoseconds offset: This field provides an offset to the Nanoseconds field when inserting a Timestamp into a received PTP message. The offset indicates the byte offset from the beginning of the PTP message. This field is ignored if 'Insert Timestamp' is 0.
5-0	RX Timestamp sec Field Offset	R/W	0h	Receive Timestamp Seconds offset: This field provides an offset to the Seconds field when inserting a Timestamp into a received PTP message. The offset indicates the byte offset from the beginning of the PTP message. This field is ignored if 'Insert Timestamp' is 0.

8.2.127 PTP_TRDL Register (Offset = D1Ah) [Reset = 0000h]

PTP_TRDL is shown in Table 8-131.

Return to the Summary Table.

This register contains the low 16-bits of the duration in clock cycles to use the Temporary Rate as programmed in the PTP_RATEH and PTP_RATEL registers. Since the Temporary Rate takes affect upon writing the PTP_RATEL register, program this register before setting the Temporary Rate. This register does not need to be reprogrammed for each use of the Temporary Rate registers.

Table 8-131. PTP_TRDL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Temporary Rate Duration [15:10]	R/W	0h	PTP Temporary Rate Duration Low 16-bits: This register sets the duration for the Temporary Rate in number of clock cycles. The actual Time duration is dependent on the value of the Temporary Rate.

8.2.128 PTP_TRDH Register (Offset = D1Bh) [Reset = 0000h]

PTP_TRDH is shown in Table 8-132.

Return to the Summary Table.

This register contains the high 10-bits of the duration in clock cycles to use the Temporary Rate as programmed in the PTP_RATEH and PTP_RATEL registers. Since the Temporary Rate takes affect upon writing the PTP_RATEL register, program this register before setting the Temporary Rate. This register does not need to be reprogrammed for each use of the Temporary Rate registers.

Table 8-132. PTP_TRDH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-0	Temporary Rate Duration [25:16]	R/W	0h	PTP Temporary Rate Duration High 10-bits: This register sets the duration for the Temporary Rate in number of clock cycles. The actual Time duration is dependent on the value of the Temporary Rate.

8.2.129 PTP_EVNT_TSU_CFG Register (Offset = D1Ch) [Reset = 0002h]

PTP_EVNT_TSU_CFG is shown in Table 8-133.

Return to the Summary Table.

This register provides configuration of storage of Event Timestamps and the transmission to Host using PSF

Table 8-133. PTP_EVNT_TSU_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	Full Trigger Timestamp Storage Enable	R/W	1h	1b = Enable storing of full timestamp for triggers independent of the change from the previous event timestamp
0	Full Event Timestamp Storage Enable	R/W	0h	1b = Enable storing of full timestamp for events independent of the change from the previous event timestamp

8.2.130 PSF_TRIG_TS_EN Register (Offset = D1Dh) [Reset = 0000h]

PSF_TRIG_TS_EN is shown in Table 8-134.

Return to the Summary Table.

This register enables PHY Status Frame delivery of timestamp corresponding to edges of the generated trigger.

Table 8-134. PSF_TRIG_TS_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	Trigger Timestamp PHY Status Frame Enable	R/W	0h	This enables PHY Status Frame delivery of timestamp corresponding to edges of the generated trigger. Every bit corresponds to an enable for 1 trigger unit as: 8'b00000001: Enables PSF delivery for trigger0 edge timestamp 8'b00000010: Enables PSF delivery for trigger1 edge timestamp 8'b00000100: Enables PSF delivery for trigger2 edge timestamp 8'b00001000: Enables PSF delivery for trigger3 edge timestamp 8'b00010000: Enables PSF delivery for trigger4 edge timestamp 8'b00100000: Enables PSF delivery for trigger5 edge timestamp 8'b01000000: Enables PSF delivery for trigger6 edge timestamp 8'b10000000: Enables PSF delivery for trigger7 edge timestamp

8.2.131 PTP_COC Register (Offset = D20h) [Reset = 000Ah]

PTP_COC is shown in Table 8-135.

Return to the Summary Table.

This register provides configuration for the PTP clock-synchronized output divide-by-N clock.

Table 8-135. PTP_COC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	PTP Clock Output Division Value	R/W	Ah	PTP Clock output Divide-by Value: This field sets the divide-by value for the 802.1AS sync output clock. The 802.1AS sync clock output is derived by dividing output clock of PTP_PLL. Valid values range from 2 to 255 (0x02 to 0xFF), giving a nominal output frequency range of 125 MHz down to 980.4 kHz. Divide-by values of 0 and 1 are not valid and stops the output clock.

8.2.132 PSF_CFG1 Register (Offset = D21h) [Reset = 0000h]

PSF_CFG1 is shown in Table 8-136.

Return to the Summary Table.

This register provides configuration for the Phy Status Frame function. Specifically, the 16-bit value in this register is used as the first 16-bits of the PTP Header data for the Phy Status Frame.

Table 8-136. PSF_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	PTP v2 reserved field: This field contains the reserved 4-bit field (at offset 1) to be sent in status packets from the Phy to the local MAC using the MII receive data interface.
11-8	PTP Version Field	R/W	0h	PTP v2 versionPTP field: This field contains the versionPTP field to be sent in status packets from the Phy to the local MAC using the MII receive data interface.
7-4	PTP TransportSpecific Field	R/W	0h	PTP v2 Header transportSpecific field: This field contains the transportSpecific field to be sent in status packets from the Phy to the local MAC using the MII receive data interface.
3-0	PTP Message Type Field	R/W	0h	PTP v2 messageType field: This field contains the messageType field to be sent in status packets from the Phy to the local MAC using the MII receive data interface.

8.2.133 PSF_CFG2 Register (Offset = D22h) [Reset = 0000h]

PSF_CFG2 is shown in Table 8-137.

Return to the Summary Table.

This register provides configuration for the Phy Status Frame function. Specifically, the 16-bit value in this register is used as the first 16-bits of the IP Source address for an IPv4 Phy Status Frame.

Table 8-137. PSF_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	IP Source Address 1	R/W	0h	Second byte of IP source address: This field contains the second byte of the IP source address.
7-0	IP Source Address 0	R/W	0h	First byte of IP source address: This field contains the most significant byte of the IP source address.

8.2.134 PSF_CFG3 Register (Offset = D23h) [Reset = 0000h]

PSF_CFG3 is shown in Table 8-138.

Return to the Summary Table.

This register provides configuration for the Phy Status Frame function. Specifically, the 16-bit value in this register is used as the second 16-bits of the IP Source address for an IPv4 Phy Status Frame.

Table 8-138. PSF_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	IP Source Address 3	R/W	0h	Fourth byte of IP source address: This field contains the fourth byte of the IP source address.
7-0	IP Source Address 2	R/W	0h	Third byte of IP source address: This field contains the third byte of the IP source address.

8.2.135 PSF_CFG4 Register (Offset = D24h) [Reset = 0000h]

PSF_CFG4 is shown in Table 8-139.

Return to the Summary Table.

This register provides configuration for the Phy Status Frame function. Specifically, the 16-bit value in this register is used to assist in computation of the IP checksum for an IPv4 Phy Status Frame.

Table 8-139. PSF_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IP Checksum	R/W	0h	IP Checksum: This field contains a precomputed value of ones-complement addition of all fixed values in the IP Header. The device adds the Total Length and Identification values to generate the final checksum.

8.2.136 PTP_INTCTL Register (Offset = D26h) [Reset = 0000h]

PTP_INTCTL is shown in Table 8-140.

Return to the Summary Table.

This register provides configuration for the IEEE 802.1AS interrupt function, allowing the PTP Interrupt to use any of the GPIO pins.

Table 8-140. PTP_INTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-0	PTP Interrupt GPIO Select	R/W	0h	PTP Interrupt GPIO select: To enable interrupts on a GPIO pin, set this field to the required GPIO. 0h = INT_N 1h = LED_0 2h = LED_1 3h = RX_ER 4h = CLKOUT 5h = GPIO_3 6h = GPIO_4 7h = GPIO_5

8.2.137 PTP_CLKSRC Register (Offset = D27h) [Reset = 0084h]

PTP_CLKSRC is shown in Table 8-141.

Return to the Summary Table.

This register provides configuration for the reference clock source driving the IEEE 802.1AS hardware logic. The source clock period is also used by the 802.1AS nanoseconds clock adder to add the proper value every reference clock cycle.

Table 8-141. PTP_CLKSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	PTP Clock Reference Select-1	R/W	0h	PTP Clock Source Select: Selects among possible sources for the PTP reference clock Mapping of {PTP Clock Reference Select-1, PTP Clock Reference Select-2} is as follows: b1000 : External reference from LED_0 b1010 : External reference from GPIO_5 b0000 : PLL 250M b0100 : PLL 125M b0010 : Clock from PTP_PLL b0001 : Recovered 200M b0101 : Recovered 100M
13	PTP Ref Clock Division Enable	R/W	0h	Clock division enable: If set to 1, enables division of the PTP reference clock by a factor of value programmed in CLK_DIV_VAL.
12-11	PTP Clock Reference Select-2	R/W	0h	PTP Clock Source Select: Selects among possible sources for the PTP reference clock Mapping of {PTP Clock Reference Select-1, PTP Clock Reference Select-2} is as follows: b1000 : External reference from LED_0 b1010 : External reference from GPIO_5 b0000 : PLL 250M b0100 : PLL 125M b0010 : Clock from PTP_PLL b0001 : Recovered 200M b0101 : Recovered 100M
10-7	PTP Ref Clock Division Value	R/W	1h	Clock division divider value: When the clock source selection is the Divide-by-N using 'PTP Ref Clock Division Enable', these bits are used as the N value.
6-0	PTP Clock Source Period	R/W	4h	PTP Clock Source Period: This field configures the PTP clock source period in nanoseconds. Program the clock source period as > 2

8.2.138 PTP_ETYPE Register (Offset = D28h) [Reset = F788h]

PTP_ETYPE is shown in Table 8-142.

Return to the Summary Table.

This register provides the Ethernet Type (Ethertype) field for PTP transport over Ethernet (Layer2).

Table 8-142. PTP_ETYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP EtherType	R/W	F788h	PTP EtherType: This field contains the Ethernet Type field used to detect PTP messages transported over Ethernet layer 2. Program this register in reverse byte format. For example, the ethertype expected from PTP packets is 0x88F7 so 0xF788 is made as default value.

8.2.139 PTP_OFF Register (Offset = D29h) [Reset = 0000h]

PTP_OFF is shown in Table 8-143.

Return to the Summary Table.

This register provides the byte offset to the PTP message in a Layer2 Ethernet frame.

Table 8-143. PTP_OFF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	PTP Message Field Offset	R/W	0h	PTP Message Offset: This field contains the offset in bytes to the PTP Message from the preceding header. For Layer2, this the offset from the Ethernet Type Field. For UDP/IP, it is the offset from the end of the UDP Header.

8.2.140 PTP_RXHASH Register (Offset = D2Bh) [Reset = 0000h]

PTP_RXHASH is shown in Table 8-144.

Return to the Summary Table.

This register provides configuration for the source identity hash filter of the PTP receive packet parser. If enabled, the receive parse logic delivers a receive timestamp only if the hash function on the ten octet sourcePortIdentity field correctly matches the programmed value. The source identity hash filter does not affect timestamp insertion.

Table 8-144. PTP_RXHASH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	Receive Hash Enable	R/W	0h	Receive Hash Enable: Enables filtering of PTP messages based on the hash function on the ten octet sourcePortIdentity field.
11-0	Receive Hash	R/W	0h	Receive Hash: This field contains the expected source identity hash value for incoming PTP event messages.

8.2.141 PTP_EVENT_GPIO_SEL Register (Offset = D30h) [Reset = 0000h]

PTP_EVENT_GPIO_SEL is shown in Table 8-145.

Return to the Summary Table.

This register provides controls to make which IOs as inputs to enable event timestamping on them.

Table 8-145. PTP_EVENT_GPIO_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4-0	GPIO Event Enable	R/W	0h	GPIO Enable for PTP Event timestamping: Writing to these registers enables GPIOs for event timestamping by making them inputs Bit[0] = 1 : LED_0 is set as input Bit[1] = 1 : LED_1 is set as input Bit[2] = 1 : RX_ER is set as input Bit[3] = 1 : CLKOUT is set as input Bit[4] = 1 : GPIO_3 is set as input Bit[5] = 1 : GPIO_4 is set as input Bit[6] = 1 : GPIO_5 is set as input

8.2.142 TX_SMD_GPIO_CTL Register (Offset = D32h) [Reset = 001Fh]

TX_SMD_GPIO_CTL is shown in Table 8-146.

Return to the Summary Table.

This register controls the parsing of PTP frames with Dual VLAN Tag.

Table 8-146. TX_SMD_GPIO_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Dual VLAN Tag Parse Enable	R/W	0h	1b = Enable parsing of received packets with Dual VLAN tag
14	RESERVED	R	0h	Reserved
13-9	RESERVED	R	0h	Reserved
8-5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	Reserved

8.2.143 SCH_CTL_1 Register (Offset = D33h) [Reset = 0000h]

SCH_CTL_1 is shown in Table 8-147.

Return to the Summary Table.

Contains LSB 16-bits of step rate used by scheduler for scheduling large PPM adjustments.

Table 8-147. SCH_CTL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Scheduler Step Rate [15:0]	R/W	0h	Scheduler step rate for scheduling large PPM adjustment lower 16-bits: Bit 15:0 of 24-bit rate step used by scheduler (applicable only during permanent rate change and micro scheduler is used for rate change in small steps), resolution is 2^{-32} ns. Calculate clock period from mr_base_freq[31:0] and then using desired step rate value in ppm, calculate step rate in ns. Scale the value by 2^{-32} to obtain value to programmed to mr_step_rate.

8.2.144 SCH_CTL_2 Register (Offset = D34h) [Reset = 0300h]

SCH_CTL_2 is shown in Table 8-148.

Return to the Summary Table.

Contains MSB 8-bits of step rate used by scheduler for scheduling large PPM adjustments along with bypass options for PTP_PLL and accumulator.

Table 8-148. SCH_CTL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	Bypass Scheduler for PTP PLL	R/W	1h	Bypass scheduler for PTP_PLL: Bypass scheduler controlled rate going to PTP_PLL (applicable only during permanent rate change). When this Bit is set and Bit 8 is not set, scheduler controlled rate adjustment is applied to the timer but PTP_PLL gets total PTP rate adjustment. When this bit as well as Bit 8 is set, scheduler based adjustment is bypassed.
8	Bypass Scheduler for Timer	R/W	1h	Bypass scheduler for Timer: Bypass scheduler controlled rate going to timer (applicable only during permanent rate change). When this Bit is set and Bit 9 is not set, scheduler controlled rate adjustment is applied to PTP_PLL but timer gets total PTP rate adjustment. When this bit as well as Bit 9 is set, scheduler based adjustment is bypassed.
7-0	Scheduler Step Rate [23:16]	R/W	0h	Scheduler step rate for scheduling large PPM adjustment MSB 8-bits: Bit 23:16 of 24-Bit rate step used by scheduler (applicable only during permanent rate change and when micro scheduler is used for rate change in small steps), resolution is 2^{-32} ns. Calculate clock period from mr_base_freq[31:0]. Using desired step rate value in ppm, calculate step rate in ns. Scale the value by 2^{-32} to obtain value to be programmed to mr_step_rate.

8.2.145 FREQ_CTL_1 Register (Offset = D35h) [Reset = CCCDh]

FREQ_CTL_1 is shown in Table 8-149.

Return to the Summary Table.

Contains LSB 16-bits of Base frequency programmable for PTP_PLL.

Table 8-149. FREQ_CTL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Base Frequency for PTP_PLL [15:0]	R/W	CCCDh	Base frequency programmable for PTP_PLL LSB word: Bit 15:0 of 32-bit programmable base frequency which is generated by PTP_PLL. 1 LSB represents 0.07275957614 Hz. Note Frequency value is modified only when 0xD35 and 0xD36 are written in sequence. This config decides the default clock frequency for PTP_PLL.

8.2.146 FREQ_CTL_2 Register (Offset = D36h) [Reset = CCCCh]

FREQ_CTL_2 is shown in Table 8-150.

Return to the Summary Table.

Contains MSB 16-bits of Base frequency programmable for PTP_PLL.

Table 8-150. FREQ_CTL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	Base Frequency for PTP_PLL [31:16]	R/W	CCCCh	Base frequency programmable for PTP_PLL MSB word: Bit 31:16 of 32-bit programmable base frequency which is generated by PTP_PLL. 1 LSB represents 0.07275957614 Hz. Note: Frequency value is modified only when 0xD35 and 0xD36 are written in sequence. This config decides the default clock frequency for PTP_PLL.

8.2.147 PTP_RATEL_ACC_ONLY Register (Offset = D37h) [Reset = 0000h]

PTP_RATEL_ACC_ONLY is shown in Table 8-151.

Return to the Summary Table.

Contains LSB 16 bits of accumulator only rate adjustment value.

Table 8-151. PTP_RATEL_ACC_ONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Accumulator Rate Control [15:0]	R/W	0h	Rate Control value for PTP accumulator: Writing to this register sets the bits 15:0 of the Rate Control value for PTP accumulator when 0xD38[14] is set. The Rate Control value is in units of 2^{-32} ns. This rate adjustment is not applied to PTP_PLL. PTP_PLL rate adjustment can still be controlled from registers 0xD04 and 0xD05.

8.2.148 PTP_RATEH_ACC_ONLY Register (Offset = D38h) [Reset = 0000h]

PTP_RATEH_ACC_ONLY is shown in Table 8-152.

Return to the Summary Table.

Contains MSB 10 bits of accumulator only rate adjustment value. Also contains enable and direction of accumulator only rate adjustment.

Table 8-152. PTP_RATEH_ACC_ONLY Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PTP Accumulator Direction	R/W	0h	PTP Rate ACC only Direction: The setting of this bit controls whether the device operates at a higher or lower frequency than the reference clock. This direction is applied along with 0xD37 and 0xD38[9:0] only if bit 0xD38[14] is set. 0 : Higher Frequency. The 'PTP Accumulator Rate Control' value is added to the clock on every cycle 1 : Lower Frequency. The 'PTP Accumulator Rate Control' value is subtracted from the clock on every cycle
14	PTP Accumulator Mode Enable	R/W	0h	PTP Accumulator mode: Setting this bit makes the PTP accumulator to be incremented according to registers 0xD37 and 0xD38[9:0] every clock cycle. 0h = accumulation value from 0xD04, 0xD05 1h = accumulation value from 0xD37, 0xD38[9:0]
13	PTP Accumulator Trate Enable	R/W	0h	PTP Temporary Rate Enable in Accumulator Mode: Setting this bit applies the temporary rate adjustments to the PTP Accumulator too (apart from the PTP PLL) 0h = Temporary Rate Adjustments are not applied to PTP Accumulator when Accumulator mode is enabled 1h = Temporary Rate Adjustments are applied to PTP Accumulator when Accumulator mode is enabled
12-10	RESERVED	R	0h	Reserved
9-0	PTP Accumulator Rate Control [25:16]	R/W	0h	PTP Rate ACC only high 10-bits: Writing to this register sets the bits 25:16 of the Rate Control value for PTP accumulator when 0xD38[14] is set. The Rate Control value is in units of 2^{-32} ns. This rate adjustment does not applied to PTP_PLL. PTP_PLL rate adjustment is still controlled from registers 0xD04 and 0xD05.

8.2.149 PTP_PLL_CTL Register (Offset = D39h) [Reset = 0025h]

PTP_PLL_CTL is shown in Table 8-153.

Return to the Summary Table.

Register to configure PTP_PLL settling time and enables storing of PTP timestamp.

Table 8-153. PTP_PLL_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9	Half Rate Enable	R	0h	PTP_PLL set half rate: Set half rate for the NCO when in PLL_125M as ref clock mode.
8	PTP PLL Phase word [32]	R	0h	PTP_PLL phase word bit-32: Bit 32 of PTP_PLL phase word
7	Capture PTP Time	R/W	0h	Capture PTP time and PTP_PLL word: Used to capture the current 33-bit PTP_PLL word along with 64-bit PTP time. Setting this trigger stores PTP clock timestamp (32-bit seconds accumulator, 32-bit nanosecond accumulator) and 33-bit PTP_PLL word simultaneously which can be read through 0xD39 - 0xD3F. This bit is self clearing.
6-0	PTP Scheduler Settle Timer	R/W	25h	PTP_PLL scheduler settle timer: No of cycles taken by PTP_PLL to provide jitter free output for any change in rate, defines the latency of rate change going to PTP_PLL. Used in scheduler every time the value of the PTP_PLL is changed.

8.2.150 PTP_PLL_RD_1 Register (Offset = D3Ah) [Reset = 0000h]

PTP_PLL_RD_1 is shown in Table 8-154.

Return to the Summary Table.

PTP timer nanosec counter readout value.

Table 8-154. PTP_PLL_RD_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Timestamp [15:0]	R	0h	PTP time nano seconds LSB word: Bit 15 - 0 of PTP timer nano seconds counter.

8.2.151 PTP_PLL_RD_2 Register (Offset = D3Bh) [Reset = 0000h]

PTP_PLL_RD_2 is shown in Table 8-155.

Return to the Summary Table.

PTP timer nanosec counter readout value.

Table 8-155. PTP_PLL_RD_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Timestamp [31:16]	R	0h	PTP time nano seconds MSB word: Bit 31 - 16 of PTP timer nano seconds counter.

8.2.152 PTP_PLL_RD_3 Register (Offset = D3Ch) [Reset = 0000h]

PTP_PLL_RD_3 is shown in Table 8-156.

Return to the Summary Table.

PTP timer seconds counter readout value.

Table 8-156. PTP_PLL_RD_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Timestamp [47:32]	R	0h	PTP time seconds LSB word: Bit 15 - 0 of PTP timer seconds counter.

8.2.153 PTP_PLL_RD_4 Register (Offset = D3Dh) [Reset = 0000h]

PTP_PLL_RD_4 is shown in Table 8-157.

Return to the Summary Table.

PTP timer seconds counter readout value.

Table 8-157. PTP_PLL_RD_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Timestamp [63:48]	R	0h	PTP time seconds MSB word: Bit 31 - 16 of PTP timer seconds counter.

8.2.154 PTP_PLL_RD_5 Register (Offset = D3Eh) [Reset = 0000h]

PTP_PLL_RD_5 is shown in Table 8-158.

Return to the Summary Table.

PTP_PLL phase word read out value.

Table 8-158. PTP_PLL_RD_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Timestamp [79:64]	R	0h	PTP_PLL phase LSB word: Bit 15 - 0 of PTP_PLL phase word.

8.2.155 PTP_PLL_RD_6 Register (Offset = D3Fh) [Reset = 0000h]

PTP_PLL_RD_6 is shown in Table 8-159.

Return to the Summary Table.

PTP_PLL phase word read out value.

Table 8-159. PTP_PLL_RD_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PTP Timestamp [95:80]	R	0h	PTP_PLL phase MSB word: Bit 31 - 16 of PTP_PLL phase word.

8.2.156 PTP_ONESTEP_OFF Register (Offset = D40h) [Reset = 0000h]

PTP_ONESTEP_OFF is shown in Table 8-160.

Return to the Summary Table.

Controls offset value of onestep timestamp being inserted into the PTP packet.

Table 8-160. PTP_ONESTEP_OFF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	PTP Accumulator Rate Control [31:26]	R/W	0h	PTP accumulator Rate Control value: Writing to this register sets bits 31:26 of the Rate Control value for PTP accumulator only when 0xD38[14] is set. The Rate Control value is in units of 2^{-32} ns. This rate adjustment is not be applied to PTP_PLL. PTP_PLL rate adjustment is still controlled from registers 0xD04 and 0xD05.
9	PTP One-step Timestamp Offset Addition Enable	R/W	0h	PTP one-step timestamp offset addition enable: Setting this bit enables addition of the offset (loaded in 0xD40[8:0]) to the timestamp being inserted into the PTP packet during one-step timestamp insertion

Table 8-160. PTP_ONESTEP_OFF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-0	PTP One-step Timestamp Offset	R/W	0h	PTP one-step timestamp offset: This offset value is added to the timestamp that is being inserted during one-step operation when 0xD40[9] is enabled.

8.2.157 PTP_PSF_VLAN_CFG_1 Register (Offset = D45h) [Reset = 0000h]

PTP_PSF_VLAN_CFG_1 is shown in Table 8-161.

Return to the Summary Table.

Configuration of VLAN tags for PSF packets

Table 8-161. PTP_PSF_VLAN_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	Dual VLAN Tag Enable for PSF	R/W	0h	1b = Enable addition of dual VLAN tag for PSF packets
0	VLAN Tag Enable for PSF	R/W	0h	1b = Enable addition of VLAN tag for PSF packet

8.2.158 PTP_PSF_VLAN_CFG_2 Register (Offset = D46h) [Reset = 0000h]

PTP_PSF_VLAN_CFG_2 is shown in Table 8-162.

Return to the Summary Table.

Configuration of VLAN tags for PSF packets

Table 8-162. PTP_PSF_VLAN_CFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VLAN Tag 1 for PSF	R/W	0h	VLAN Tag 1 added to PSF packets when 0x0D45[0]=1

8.2.159 PTP_PSF_VLAN_CFG_3 Register (Offset = D47h) [Reset = 0000h]

PTP_PSF_VLAN_CFG_3 is shown in Table 8-163.

Return to the Summary Table.

Configuration of VLAN tags for PSF packets

Table 8-163. PTP_PSF_VLAN_CFG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VLAN Tag 2 for PSF	R/W	0h	VLAN Tag 2 added to PSF packets when 0x0D45[1]=1

8.2.160 MAX_IPV4_LENGTH Register (Offset = D48h) [Reset = 0724h]

MAX_IPV4_LENGTH is shown in Table 8-164.

Return to the Summary Table.

Table 8-164. MAX_IPV4_LENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11-6	mr_ipv4_length_2	R/W	1Ch	Configure max packet length for PSF IPV4. Maximum value of IPv4 packet length is 0x3E

Table 8-164. MAX_IPV4_LENGTH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	mr_ipv4_length_1	R/W	24h	Configure max packet length for PSF IPV4. Maximum value of IPv4 packet length is 0x3E

8.2.161 PTP_TXCFG_2 Register (Offset = D49h) [Reset = 0000h]

PTP_TXCFG_2 is shown in Table 8-165.

Return to the Summary Table.

Table 8-165. PTP_TXCFG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-2	mr_ptp_domain_tx	R/W	0h	Sets ptp domain filtering for Tx packet
1	mr_pkt_cfg_en	R/W	0h	Sets whether configurability is enabled for DMAC/SMAC in PSF or not
0	tx_domain_en	R/W	0h	1b = Enable domain filtering on PTP TX 0b=Disable domain filtering on PTP TX

8.2.162 PSF_DMAC_1 Register (Offset = D4Ah) [Reset = 1B01h]

PSF_DMAC_1 is shown in Table 8-166.

Return to the Summary Table.

Table 8-166. PSF_DMAC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_dmac	R/W	1B01h	PSF DMAC byte_1 and byte_2 with bytes reversed (byte_2, byte_1)

8.2.163 PSF_DMAC_2 Register (Offset = D4Bh) [Reset = 0019h]

PSF_DMAC_2 is shown in Table 8-167.

Return to the Summary Table.

Table 8-167. PSF_DMAC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_dmac	R/W	19h	PSF DMAC byte_3 and byte_4 with bytes reversed (byte_4, byte_3)

8.2.164 PSF_DMAC_3 Register (Offset = D4Ch) [Reset = 0000h]

PSF_DMAC_3 is shown in Table 8-168.

Return to the Summary Table.

Table 8-168. PSF_DMAC_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_dmac	R/W	0h	PSF DMAC byte_5 and byte_6 with bytes reversed (byte_6, byte_5)

8.2.165 PSF_SMAC_1 Register (Offset = D4Dh) [Reset = 0008h]

PSF_SMAC_1 is shown in Table 8-169.

Return to the Summary Table.

Table 8-169. PSF_SMAC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_smac	R/W	8h	PSF SMAC byte_1 and byte_2 with bytes reversed (byte_2, byte_1)

8.2.166 PSF_SMAC_2 Register (Offset = D4Eh) [Reset = 0B17h]

PSF_SMAC_2 is shown in Table 8-170.

Return to the Summary Table.

Table 8-170. PSF_SMAC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_smac	R/W	B17h	PSF SMAC byte_3 and byte_4 with bytes reversed (byte_4, byte_3)

8.2.167 PSF_SMAC_3 Register (Offset = D4Fh) [Reset = 0F6Bh]

PSF_SMAC_3 is shown in Table 8-171.

Return to the Summary Table.

Table 8-171. PSF_SMAC_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_smac	R/W	F6Bh	PSF SMAC byte_5 and byte_6 with bytes reversed (byte_6, byte_5)

8.2.168 PSF_ETYPE Register (Offset = D50h) [Reset = F788h]

PSF_ETYPE is shown in Table 8-172.

Return to the Summary Table.

Table 8-172. PSF_ETYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_etype	R/W	F788h	PSF ether type byte_1, byte_2 for L2 packet with bytes reversed (byte_2, byte1)

8.2.169 IPV4_DA_1 Register (Offset = D51h) [Reset = 00E0h]

IPV4_DA_1 is shown in Table 8-173.

Return to the Summary Table.

Table 8-173. IPV4_DA_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_da	R/W	E0h	PSF DA byte_1, byte_2 with bytes reversed (byte_2, byte_1)

8.2.170 IPV4_DA_2 Register (Offset = D52h) [Reset = 8101h]

IPV4_DA_2 is shown in Table 8-174.

Return to the Summary Table.

Table 8-174. IPV4_DA_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_ipv4_da	R/W	8101h	PSF DA byte_3, byte_4 with bytes reversed (byte_4, byte_3)

8.2.171 PSF_SOURCE_UDP_PORT Register (Offset = D53h) [Reset = 3F01h]

PSF_SOURCE_UDP_PORT is shown in Table 8-175.

Return to the Summary Table.

Table 8-175. PSF_SOURCE_UDP_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_udp_s_port	R/W	3F01h	PSF S_PORT byte1, byte2 with byte reversed (byte_2, byte_1)

8.2.172 PSF_DESTINATION_UDP_PORT Register (Offset = D54h) [Reset = 3F01h]

PSF_DESTINATION_UDP_PORT is shown in Table 8-176.

Return to the Summary Table.

Table 8-176. PSF_DESTINATION_UDP_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	mr_pkt_sts_udp_d_port	R/W	3F01h	PSF D_PORT byte1, byte2 with byte reversed (byte_2, byte_1)

8.2.173 PTP_LAT_COMP_CTRL Register (Offset = DE0h) [Reset = C000h]

PTP_LAT_COMP_CTRL is shown in Table 8-177.

Return to the Summary Table.

Table 8-177. PTP_LAT_COMP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	Dithering Latency Compensation Enable - Receive path	R/W	0h	Enable fixed latency compensation on the Rx side, when dithering is enabled, for 2-step PTP time stamping
2	Dithering Latency Compensation Enable - Transmit path	R/W	0h	Enable fixed latency compensation on the Tx side, when dithering is enabled, for 2-step PTP time stamping
1	Latency Compensation Enable - Receive path	R/W	0h	Enable fixed latency compensation on the Rx side, for 2-step PTP time stamping
0	Latency Compensation Enable - Transmit path	R/W	0h	Enable fixed latency compensation on the Tx side, for 2-step PTP time stamping

8.2.174 PTP_DEBUG_SEL Register (Offset = DF0h) [Reset = 0000h]

PTP_DEBUG_SEL is shown in Table 8-178.

Return to the Summary Table.

Table 8-178. PTP_DEBUG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	PTP External Reference Support Enable	R/W	0h	In PTP external reference clock mode, by the default minimum frequency supported is >35 MHz. Set this bit to support lower frequencies (up to 25MHz)

8.2.175 MMD1_PMA_CTRL_1 Register (Offset = 1000h) [Reset = 0000h]

MMD1_PMA_CTRL_1 is shown in Table 8-179.

Return to the Summary Table.

Table 8-179. MMD1_PMA_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PMA Reset	R/W	0h	1b = PMA reset
14-1	RESERVED	R	0h	Reserved
0	PMA Loopback	R/W	0h	1b = PMA loopback set

8.2.176 MMD1_PMA_STATUS_1 Register (Offset = 1001h) [Reset = 0000h]

MMD1_PMA_STATUS_1 is shown in Table 8-180.

Return to the Summary Table.

Table 8-180. MMD1_PMA_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0h	Reserved
2	Link Status	R	0h	1b = Link is up
1-0	RESERVED	R	0h	Reserved

8.2.177 MMD1_PMA_STAUS_2 Register (Offset = 1007h) [Reset = 003Dh]

MMD1_PMA_STAUS_2 is shown in Table 8-181.

Return to the Summary Table.

Table 8-181. MMD1_PMA_STAUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-6	RESERVED	R	0h	Reserved
5-0	PMA PMD Type Selection	R	3Dh	PMA or PMD type selection field 111101b = 100BASE-T1 PMA or PMD

8.2.178 MMD1_PMA_EXT_ABILITY_1 Register (Offset = 100Bh) [Reset = 0800h]

MMD1_PMA_EXT_ABILITY_1 is shown in Table 8-182.

Return to the Summary Table.

Table 8-182. MMD1_PMA_EXT_ABILITY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	Extended Abilities	R	1h	1b = PMA/PMD has BASE-T1 extended abilities 0b = PMA/PMD does not have BASE-T1 extended abilities
10-0	RESERVED	R	0h	Reserved

8.2.179 MMD1_PMA_EXT_ABILITY_2 Register (Offset = 1012h) [Reset = 0001h]

MMD1_PMA_EXT_ABILITY_2 is shown in Table 8-183.

Return to the Summary Table.

Table 8-183. MMD1_PMA_EXT_ABILITY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	0h	Reserved
0	100BASE-T1 Ability	R	1h	1b = PMA/PMD supports 100BASE-T1 0b = PMA/PMD does not support 100BASE-T1

8.2.180 MMD1_PMA_CTRL_2 Register (Offset = 1834h) [Reset = X000h]

MMD1_PMA_CTRL_2 is shown in Table 8-184.

Return to the Summary Table.

Table 8-184. MMD1_PMA_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	Leader Follower Configuration	R/W	0h	1b = Configure PHY as LEADER 0b = Configure PHY as FOLLOWER
13-4	RESERVED	R	0h	Reserved
3-0	type selection	R	0h	type selection field 0000b = 100Base-T1

8.2.181 MMD1_PMA_TEST_MODE_CTRL Register (Offset = 1836h) [Reset = 0000h]

MMD1_PMA_TEST_MODE_CTRL is shown in Table 8-185.

Return to the Summary Table.

Table 8-185. MMD1_PMA_TEST_MODE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	Compliance Test Mode	R/W	0h	100BASE-T1 test mode control 000b = Normal mode operation 001b = Test mode 1 010b = Test mode 2 011b = Reserved 100b = Test mode 4 101b = Test mode 5 110b = Reserved 111b = Reserved
12-0	RESERVED	R	0h	Reserved

8.2.182 MMD3_PCS_CTRL_1 Register (Offset = 3000h) [Reset = 0000h]

MMD3_PCS_CTRL_1 is shown in Table 8-186.

Return to the Summary Table.

Table 8-186. MMD3_PCS_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCS Reset	R/W	0h	Reset bit, Self Clear. When write to this bit 1: 1. reset the registers (not vendor specific) at MMD3/MMD7. 2. Reset brk_top Please notice: This register is WSC (write-self-clear) and not read-only!
14	PCS Loopback	R/W	0h	This bit is cleared by PCS_Reset
13-11	RESERVED	R	0h	Reserved

Table 8-186. MMD3_PCS_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX Clock Stoppable	R/W	0h	RW, reset value = 1. 1= PHY can stop receive clock during LPI 0= Clock not stoppable Note: this flop implemented at glue logic
9-0	RESERVED	R	0h	Reserved

8.2.183 MMD3_PCS_Status_1 Register (Offset = 3001h) [Reset = 0000h]

MMD3_PCS_Status_1 is shown in Table 8-187.

Return to the Summary Table.

Table 8-187. MMD3_PCS_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved
11	TX LPI Received	RC	0h	1= Tx PCS hs received LPI 0= LPI not received
10	RX LPI Received	RC	0h	1= Rx PCS hs received LPI 0= LPI not received
9	TX LPI Indication	R	0h	1= TX PCS is currently receiving LPI 0= PCS is not currently receiving LPI
8	RX LPI Indication	R	0h	1= RX PCS is currently receiving LPI 0= PCS is not currently receiving LPI
7	RESERVED	R	0h	Reserved
6	TX Clock Stoppable	R	0h	1= the MAC can stop the clock during LPI 0= Clock not stoppable
5-0	RESERVED	R	0h	Reserved

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DP83TC815-Q1 is a single-port 100Mbps Automotive Ethernet PHY. It supports IEEE 802.3bw and allows for connections to an Ethernet MAC through MII, RMII, RGMII, or SGMII. When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required connections.

Note

It is necessary to use the register settings outlined in TI Application Note SDAA127 to achieve desired OA compliance performance. To obtain the Application Note contact TI.

9.2 Typical Applications

Figure 9-1 through Figure 9-5 show some the typical applications for the DP83TC815-Q1.

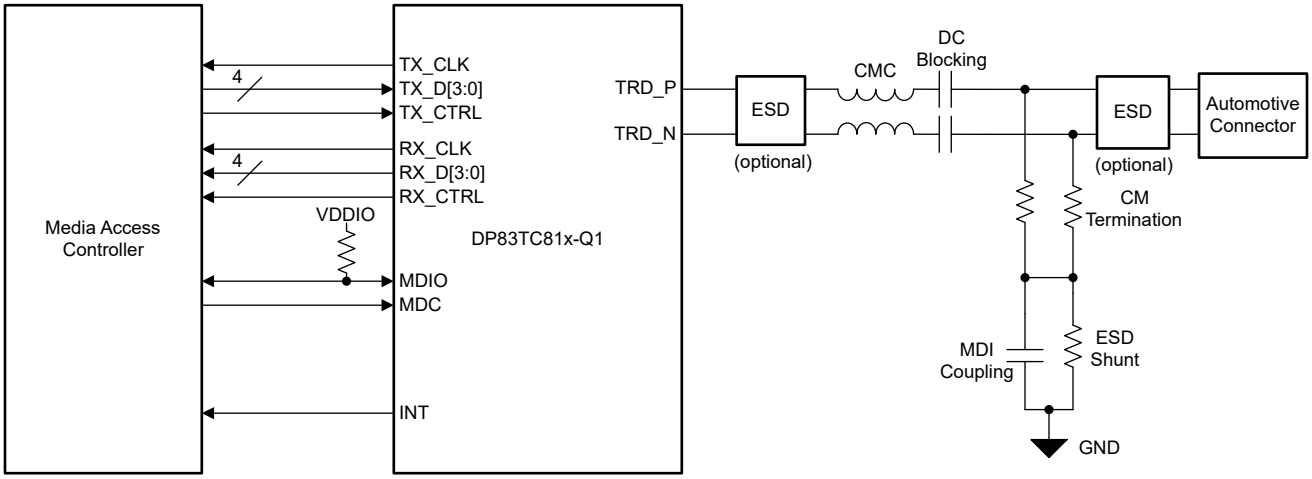

Figure 9-1. Typical Application (MII)

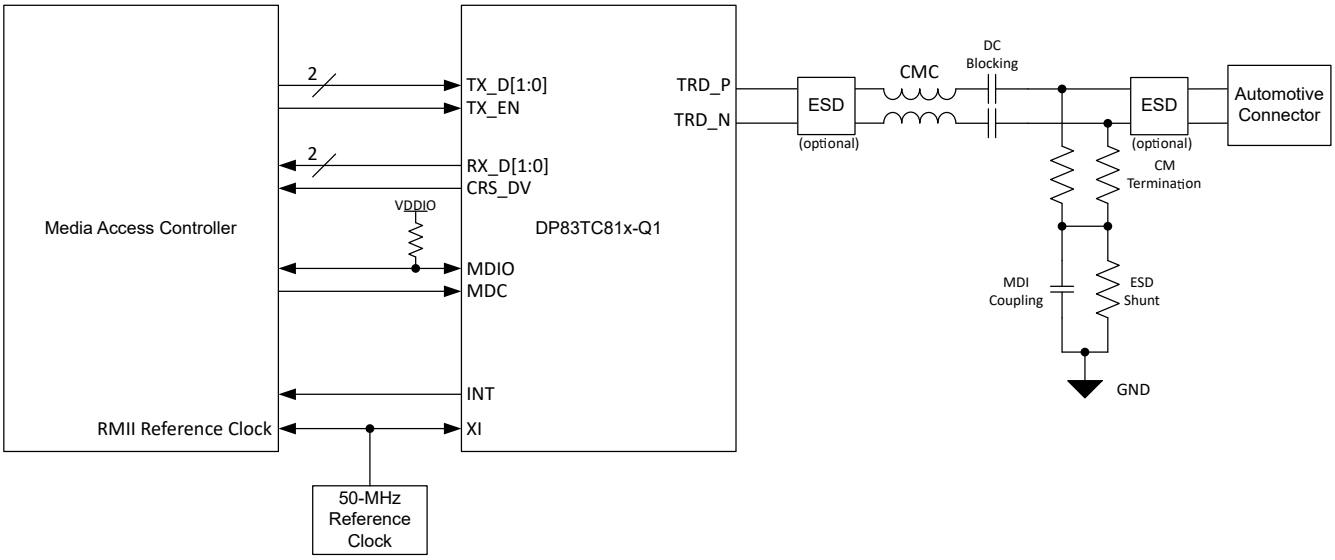

Figure 9-2. Typical Application (RMII Follower)

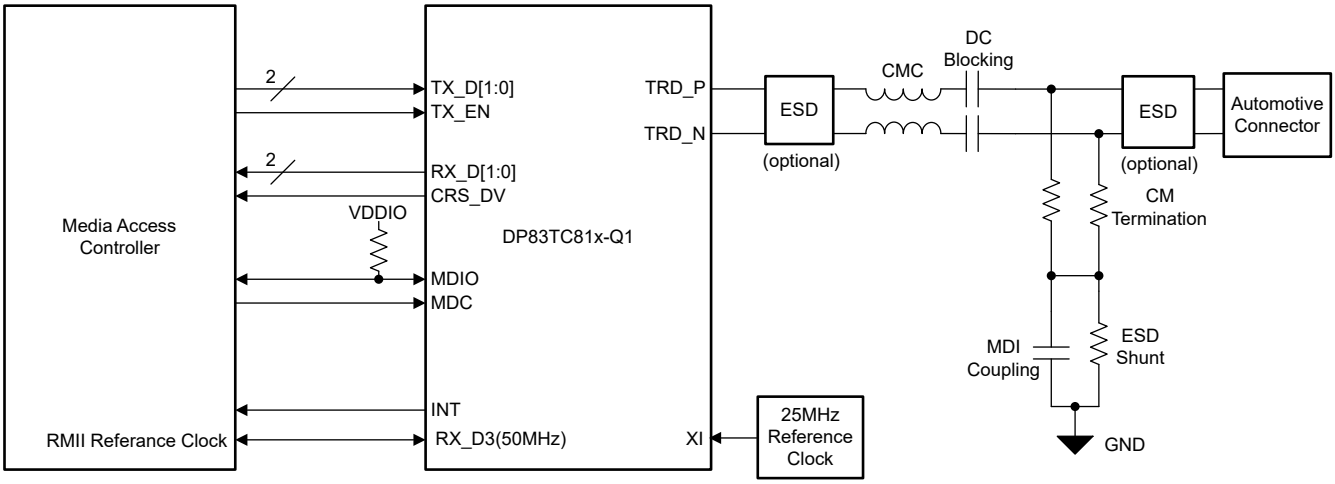

Figure 9-3. Typical Application (RMII Leader)

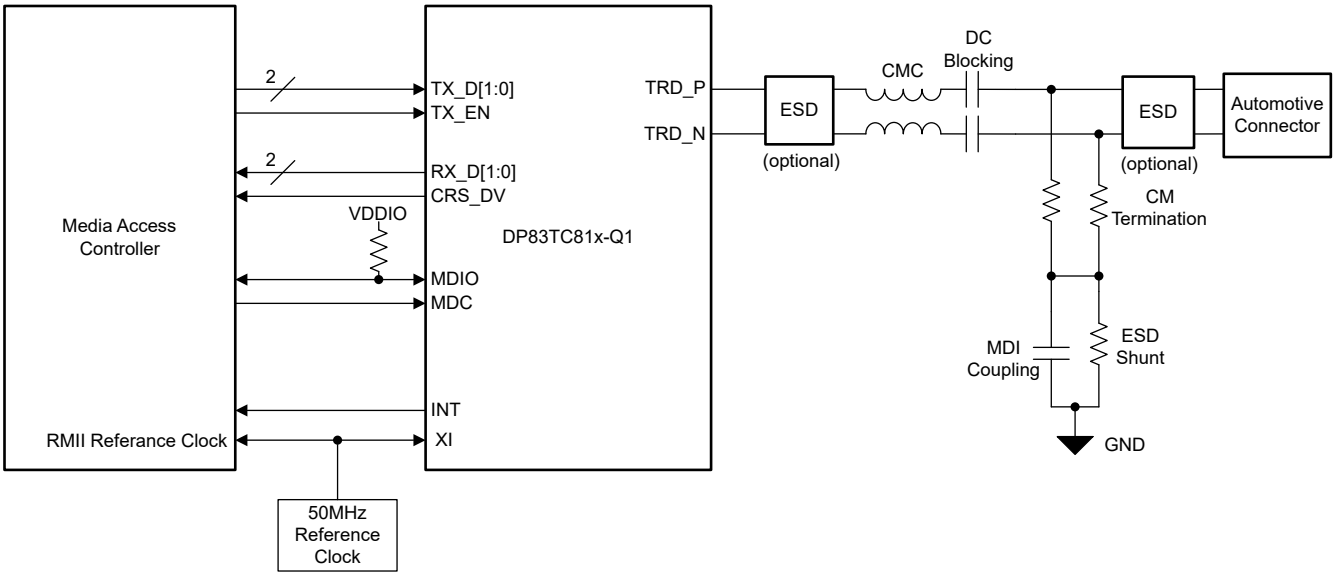

Figure 9-4. Typical Application (RGMII)

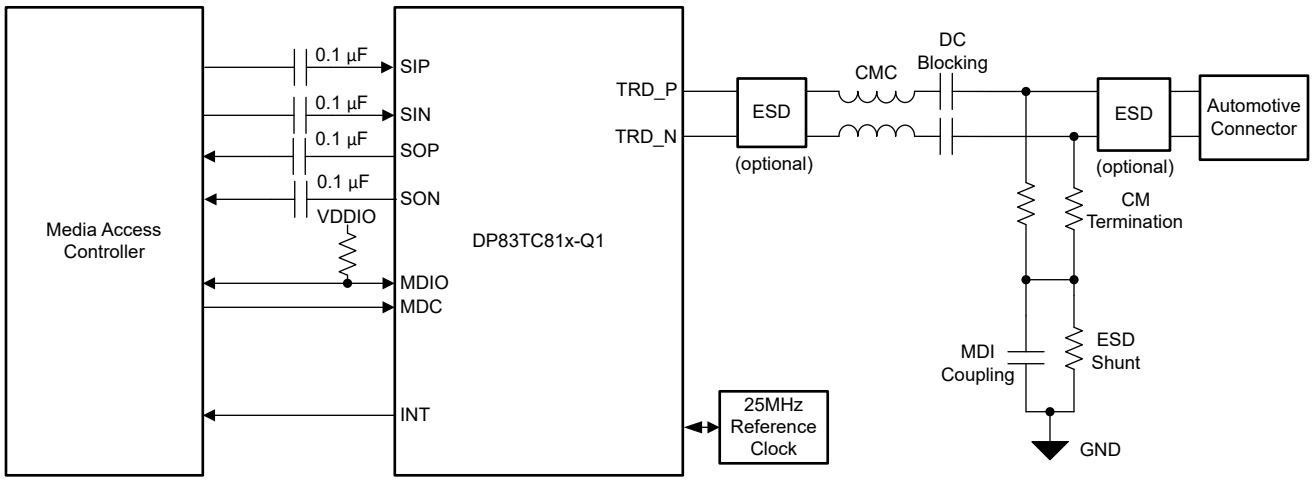

Figure 9-5. Typical Application (SGMII)

9.2.1 Design Requirements

For these typical applications, use the following as design parameters from the table below. Refer to Section 9.3 section for detailed connection diagram.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8V, 2.5V, or 3.3V
V_{DDMAC}	1.8V, 2.5V, or 3.3V
V_{DDA}	3.3V
V_{SLEEP}	3.3V
(Optional) V_{DD1P0}	1.0V
Decoupling capacitors V_{DDIO} (2) (3)	0.01 µF
(Optional) ferrite bead for V_{DDIO} (3)	1 kΩ at 100MHz (BLM18KG601SH1D)
Decoupling capacitors V_{DDMAC} (2)	0.01 µF, 0.47 µF
Ferrite bead for V_{DDMAC}	1 kΩ at 100MHz (BLM18KG601SH1D)

Table 9-1. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Decoupling capacitors V_{DDA} (2)	0.01 µF, 0.47 µF
(Optional) ferrite bead for V_{DDA}	1 kΩ at 100MHz (BLM18KG601SH1D)
Decoupling capacitors V_{SLEEP}	0.1 µF
Decoupling capacitors V_{DD1P0} (2)	0.1 µF, 2.2 µF
(Optional) Ferrite bead for V_{DD1P0}	1 kΩ at 100MHz (BLM18KG601SH1D)
DC Blocking Capacitors (2)	0.1 µF
Common-Mode Choke	200 µH
Common Mode Termination Resistors(1)	1 kΩ
MDI Coupling Capacitor (2)	4.7 nF
ESD Shunt(2)	100kΩ
Reference Clock	25MHz

(1) 1% tolerance components are recommended.
(2) 10% tolerance components are recommended.
(3) If VDDIO is separate from VDDMAC then additional ferrite bead and 0.47µF capacitor are required on VDDIO.

9.2.1.1 Physical Medium Attachment

There must be no metal running beneath the common-mode choke. CMCs can inject noise into metal beneath them, which can affect the emissions and immunity performance of the system. Because the DP83TC815-Q1 is a voltage mode line driver, no external termination resistors are required. The ESD shunt and MDI coupling capacitor must be connected to ground. Ensure that the common-mode termination resistors are 1% tolerance or better to improve differential coupling.

9.2.1.1.1 Common-Mode Choke Recommendations

The following CMCs are recommended for use with the DP83TC815-Q1:

Table 9-2. Recommended CMCs

MANUFACTURER	PART NUMBER
Pulse Electronics	AE2002
Murata	DLW43MH201XK2L
Murata	DLW32MH201XK2
TDK	ACT1210L-201

Table 9-3. CMC Electrical Specifications

PARAMETER	TYP	UNITS	CONDITIONS
Insertion Loss	–0.5	dB	1 – 30MHz
	–1.0	dB	30 – 60MHz
Return Loss	–26	dB	1 – 30MHz
	–20	dB	30 – 60MHz
Common-Mode Rejection	–24	dB	1 MHz
	–42	dB	10 – 100MHz
	–25	dB	400MHz
Differential Common-Mode Rejection	–70	dB	1 – 10MHz
	–50	dB	100MHz
	–24	dB	1000MHz

9.2.2 Detailed Design Procedure

When creating a new system design with an Ethernet PHY, follow this schematic capture procedure:

1. Select desired PHY hardware configurations in table Table 7-41.
2. Use the Electrical Characteristics table, the Table 7-39 table and the Table 7-40 table to select the correct external bootstrap resistors.
3. If using LEDs, ensure the correct external circuit is applied as shown in Figure 7-25.
4. Select an appropriate clock source that adheres to either the CMOS-level oscillator or crystal resonator requirements within the Electrical Characteristics table.
5. Select a CMC, a list of recommended CMCs are located in Table 9-2.
6. Add common-mode termination, DC-blocking capacitors, an MDI-coupling capacitor, and an ESD shunt found in Table 9-1.
7. Ensure that there is sufficient supply decoupling on VDDIO and VDDA supply pins.
8. Add an external pullup resistor (tie to VDDIO) on MDIO line.
9. If operating with SGMII, place 0.1µF, DC-blocking capacitors between the MAC and PHY SGMII pins.
10. If sleep modes are not desired, WAKE pin must be tied to VSLEEP directly or through an external pullup resistor.

The following layout procedure must be followed:

1. Locate the PHY near the edge of the board so that short MDI traces can be routed to the desired connector.
2. Place the MDI external components: CMC, DC-blocking capacitors, CM termination, MDI-coupling capacitor, and ESD shunt.
3. Create metal pour keepout under the CMC on the top layer and at least one layer beneath the top later.
4. Ensure that the MDI TRD_M and TRD_P traces are routed such that they are 100-Ω differential.
5. Place the clock source near the XI and XO pins.
6. Ensure that when configured for MII, RMII, or RGMII operation, the xMII pins are routed 50-Ω and are single-ended with reference to ground.
7. Ensure that transmit path xMII pins are routed such that setup and hold timing does not violate the PHY requirements.
8. Ensure that receive path xMII pins are routed such that setup and hold timing does not violate the MAC requirements.
9. Ensure that when configured for SGMII operation, the xMII RX_P, RX_M, TX_P, and TX_M pins are routed 100-Ω differential.
10. Place the MDIO pullup close to the PHY.

9.2.3 Application Curves

The following curves are obtained using the PHY evaluation module under nominal conditions.

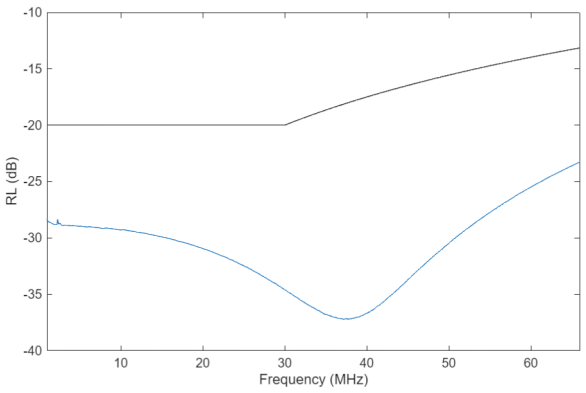

Figure 9-6. MDI Return Loss

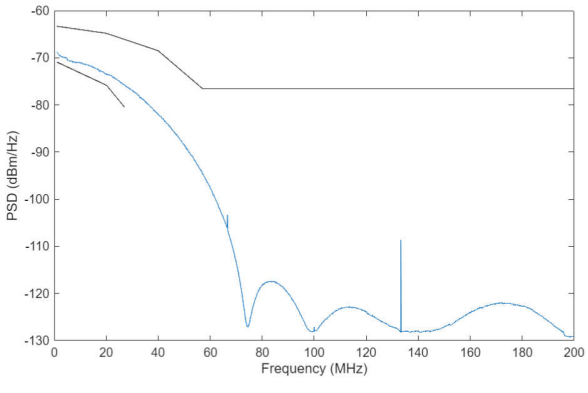

Figure 9-7. MDI PSD

9.3 Power Supply Recommendations

The DP83TC815-Q1 supports two Power Supply Modes; Single Supply Mode and Dual Supply Mode.

In Single Supply Mode, VDD1P0 can be fed from an LDO internal to DP83TC815-Q1. Connect LDO_OUT (pin 9) to VDD1P0 (Pin 21) through decoupling network of 2.2uF and 0.1uF. Ferrite bead on VDD1P0 is not supported in Single Supply Mode.

In Dual Supply Mode, VDD1P0 can be fed from an external voltage regulator. The voltage rail must have a ferrite bead, 2.2uF, and 0.1uF.

Recommendations for other supplies are the same between Single Supply Mode and Dual Supply Mode.

The DP83TC815-Q1 is capable of operating with a wide range of IO supply voltages (3.3V, 2.5V, or 1.8V). No power supply sequencing is required. The recommended power supply de-coupling network is shown in the figure below. For improved conducted emissions, an optional ferrite bead can be placed between the supply and the PHY de-coupling network.

Typical TC-10 application block diagram along with supply and peripherals is shown below. TPS7B81-Q1 is the recommended part number to be used as 3.3V LDO for the VSLEEP rail. The low quiescent current of this LDO is designed TC-10 applications. Some example power distribution networks for TC10 applications are explained in the Section 7.3.2.

When VDDIO and VDDMAC are separate, both voltage rails must have a dedicated network of ferrite bead, 0.47µF, and 0.01µF capacitors. VSLEEP can also be connected to VDDA for non-TC10 applications, and the 0.1µF capacitor must be retained in this configuration.

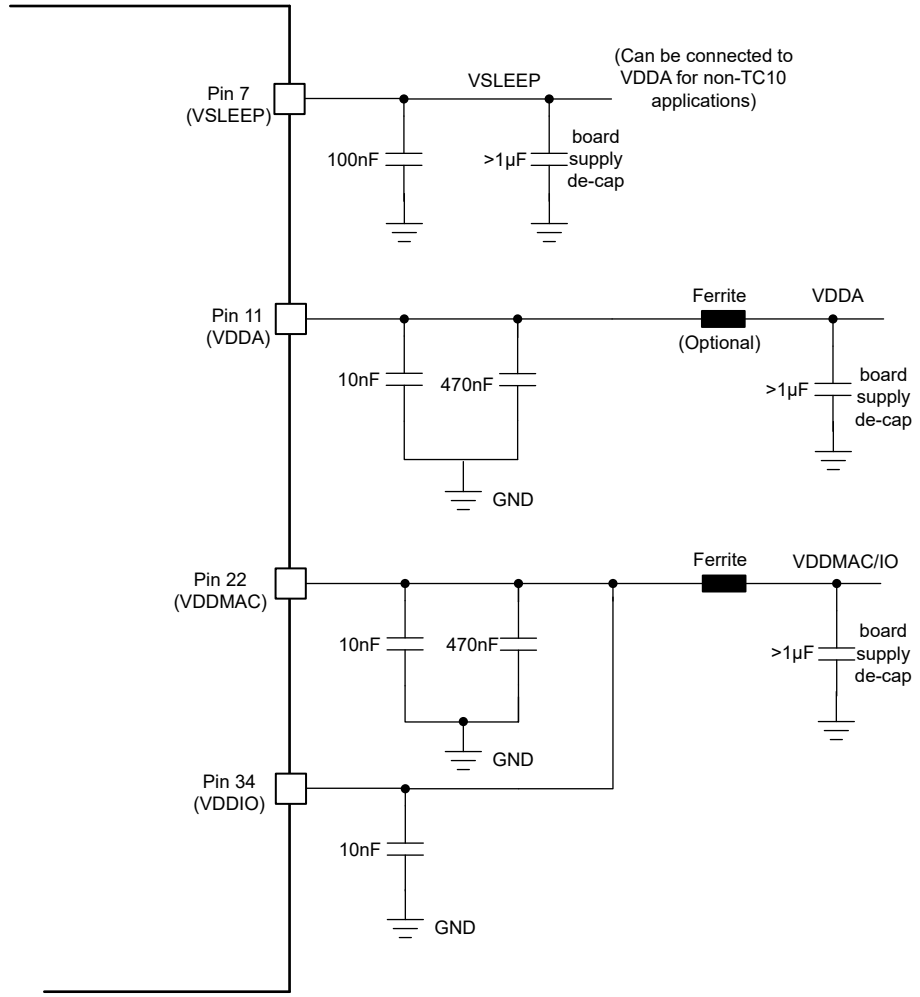

Figure 9-8. Decoupling Network - VDDA, VDDMAC, VDDIO, VSLEEP

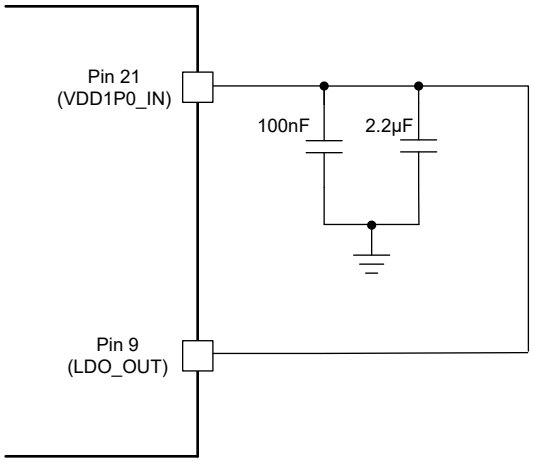

Figure 9-9. Decoupling Network - VDD1P0 (Single Supply Mode)

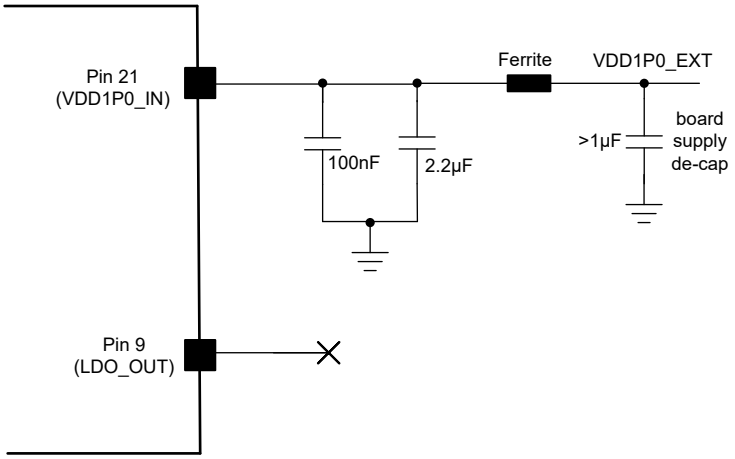

Figure 9-10. Decoupling Network - VDD1P0 (Dual Supply Mode)

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces must be 50Ω, single-ended impedance. Differential traces must be 50Ω single-ended and 100-Ω differential. Take care to ensure impedance is controlled throughout. Impedance discontinuities cause reflections leading to emissions and signal integrity issues. Stubs must be avoided on all signal traces, especially differential signal pairs.

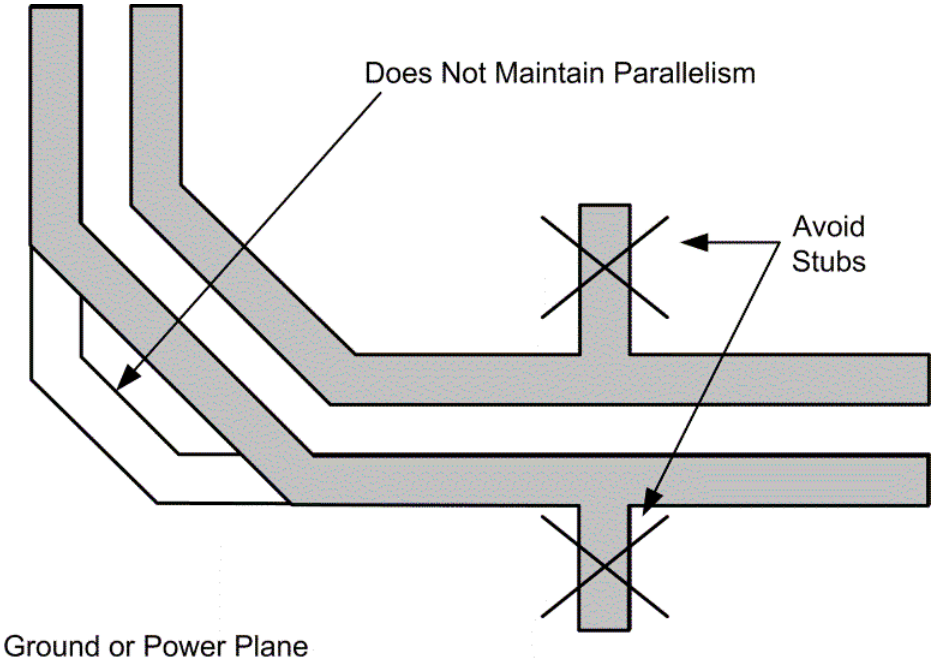

Figure 9-11. Differential Signal Trace Routing

Within the differential pairs, trace lengths must be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces must be length matched to each other and all receive signal traces must be length matched to each other. For SGMII differential traces, it is recommended to keep the skew mismatch below 20ps.

Ideally, there must be no crossover on signal path traces. High speed signal traces must be routed on internal layers to improved EMC performance. However, vias present impedance discontinuities and must be minimized when possible. Route trace pairs on the same layer. Signals on different layers must not cross each other without at least one return path plane between them. Differential pairs must always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

9.4.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces must be avoided at all cost. A signal crossing a split plane can cause unpredictable return path currents and could impact signal quality and result in emissions issues.

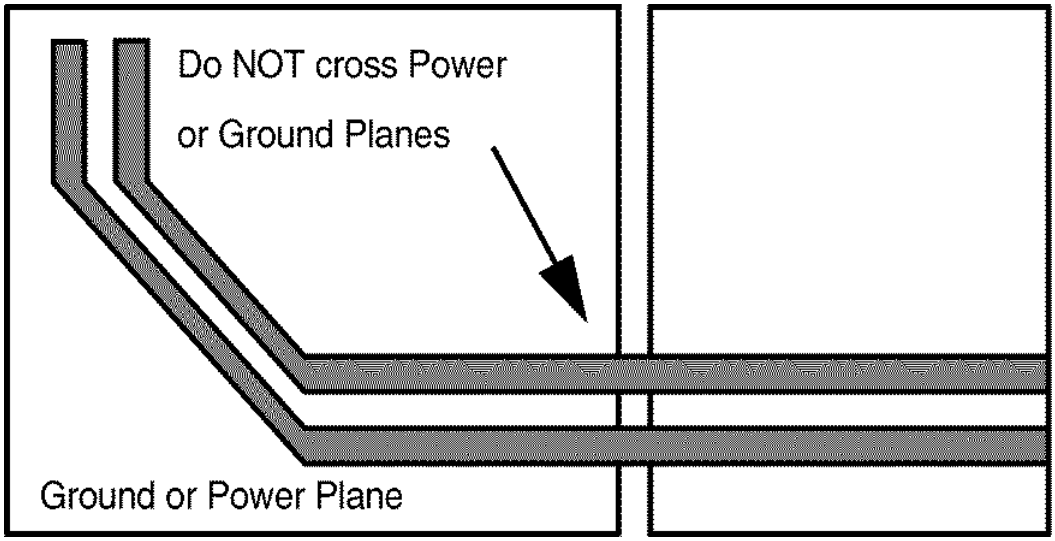

Figure 9-12. Power and Ground Plane Breaks

9.4.1.3 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

9.4.1.4 PCB Layer Stacking

To meet signal integrity and performance requirements, a minimum four-layer PCB is recommended. However, use a six-layer or above PCB when possible.

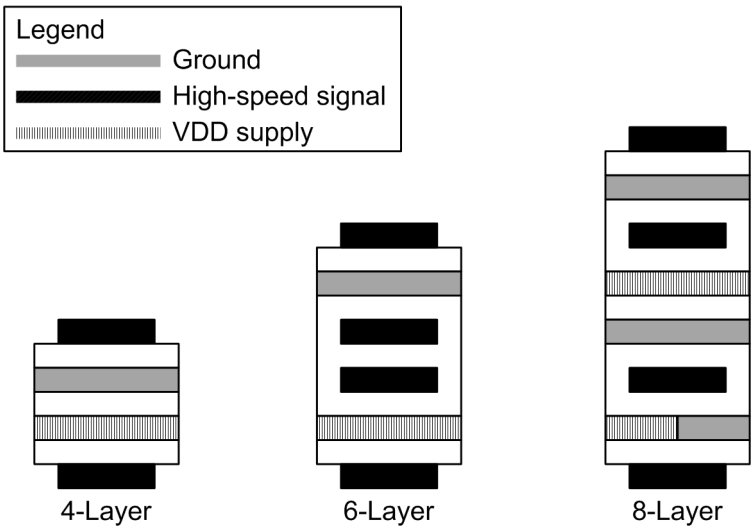

Figure 9-13. Recommended PCB Layer Stack-Up

9.4.2 Layout Example

There is an evaluation board reference for the DP83TC815-Q1. The DP83TC815EVM-MC is a media converter board which can be used for interoperability and bit error rate testing.

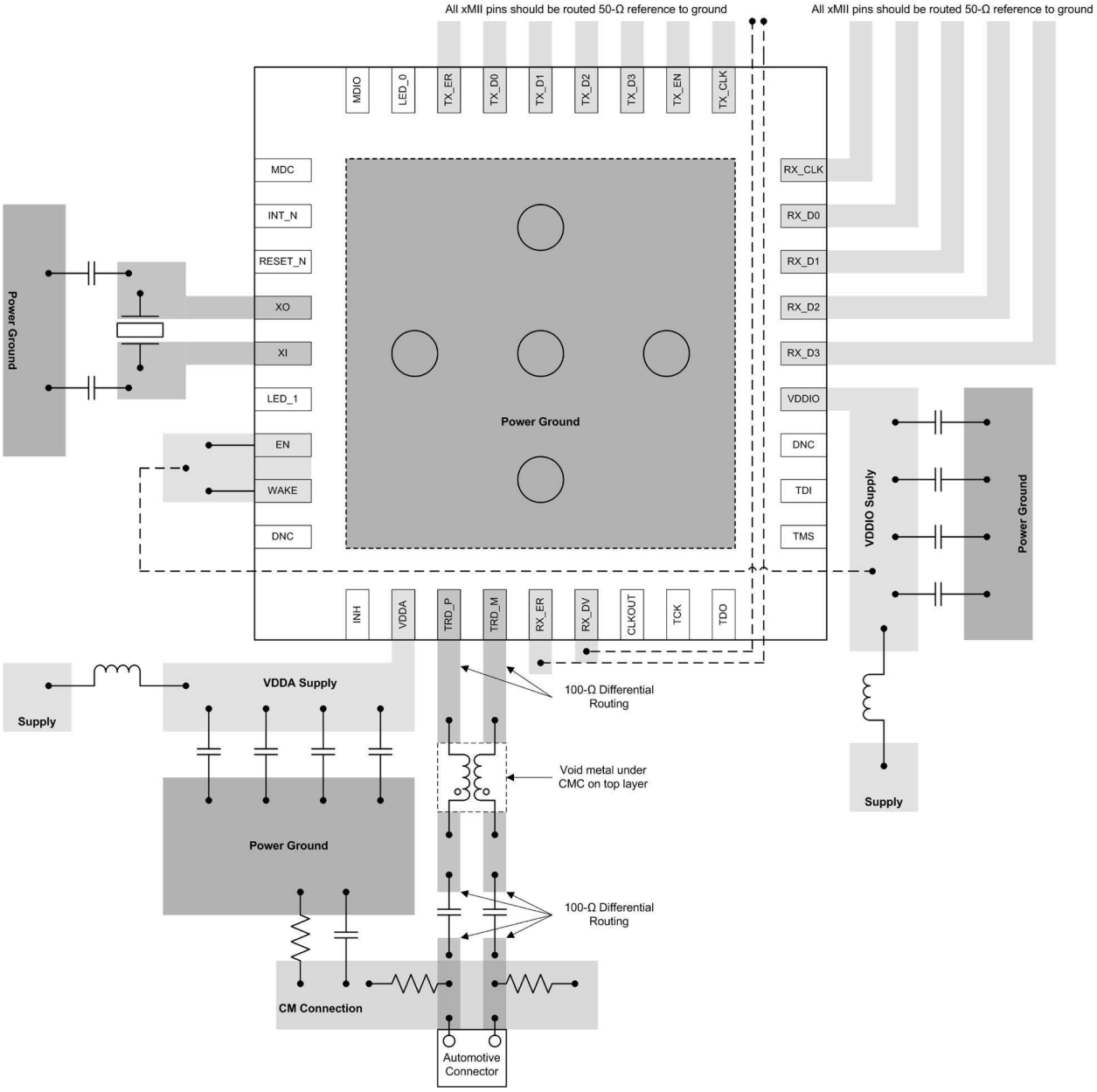

Figure 9-14. DP83TC815-Q1 MII / RMII / RGMII Layout Recommendation

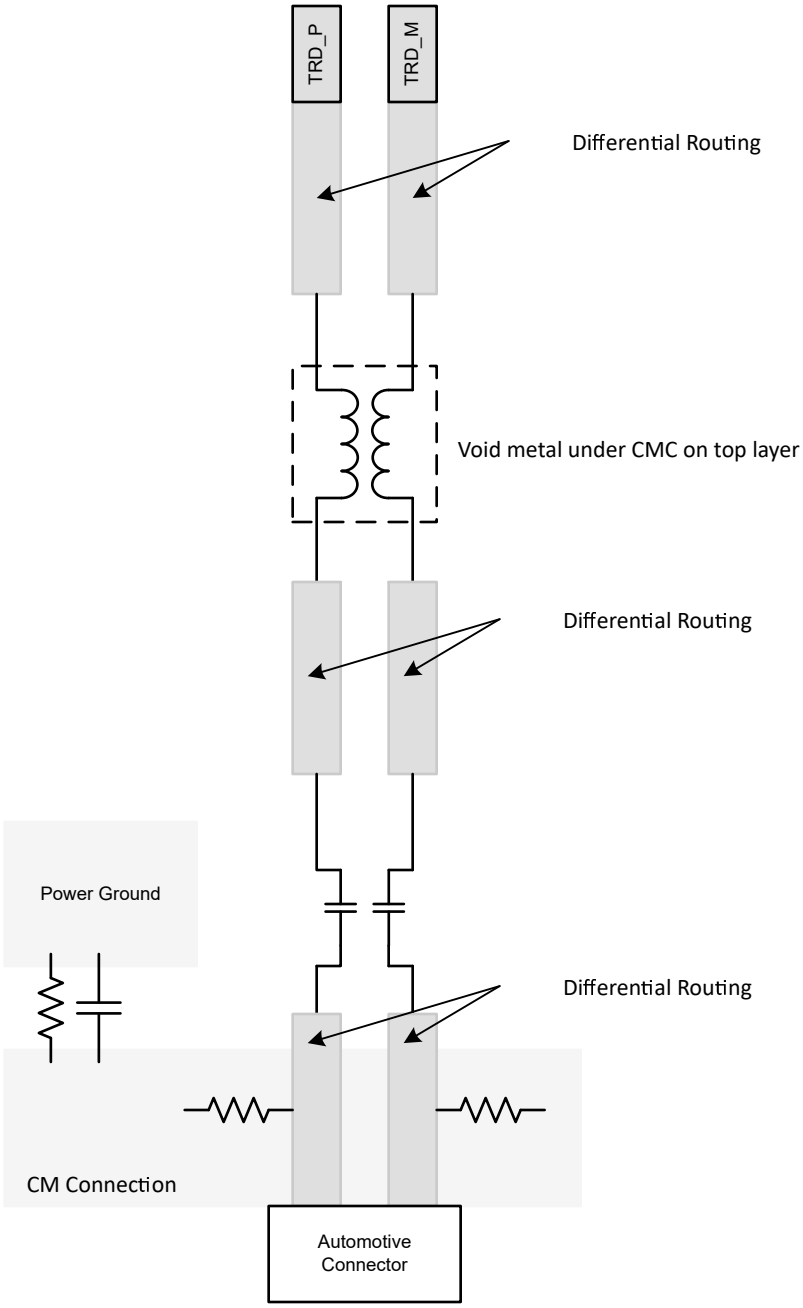

Figure 9-15. MDI Low-Pass Filter Layout Recommendation

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (November 2025)	Page
• First public release of the full data sheet	1
• Changed the document status from Advance Information to Production Data	1
• Updated all instance of legacy terminology to leader and follower throughout the document	1
• Updated accuracy, details, and style throughout the document	1
• Updated electrical parameters throughout the document to reflect product silicon	1
• Added the *Typical Characteristics* section	31
• Updated the *Register Maps* section	82
• Added the *Application Curves* section	160
• Added the *Layout Example* section	166

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83TC815RHARQ1	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	815

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

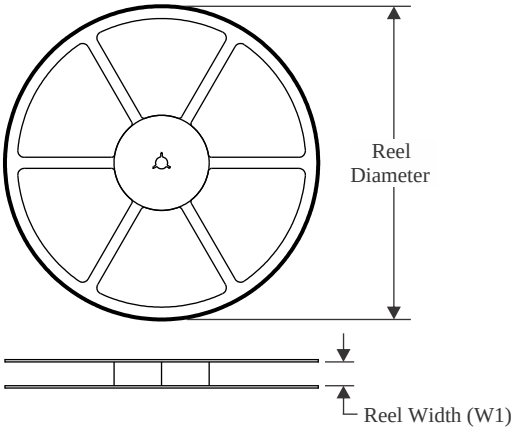
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

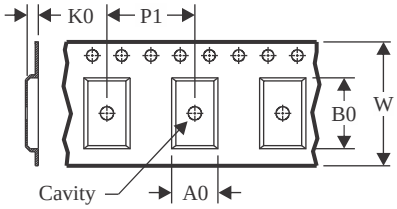
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

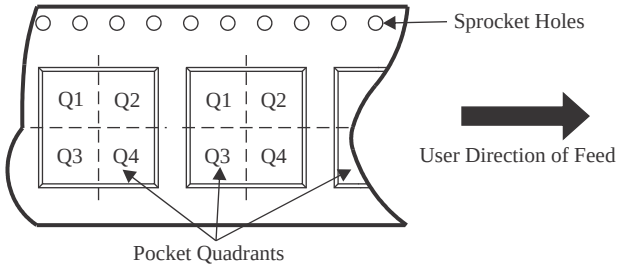


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

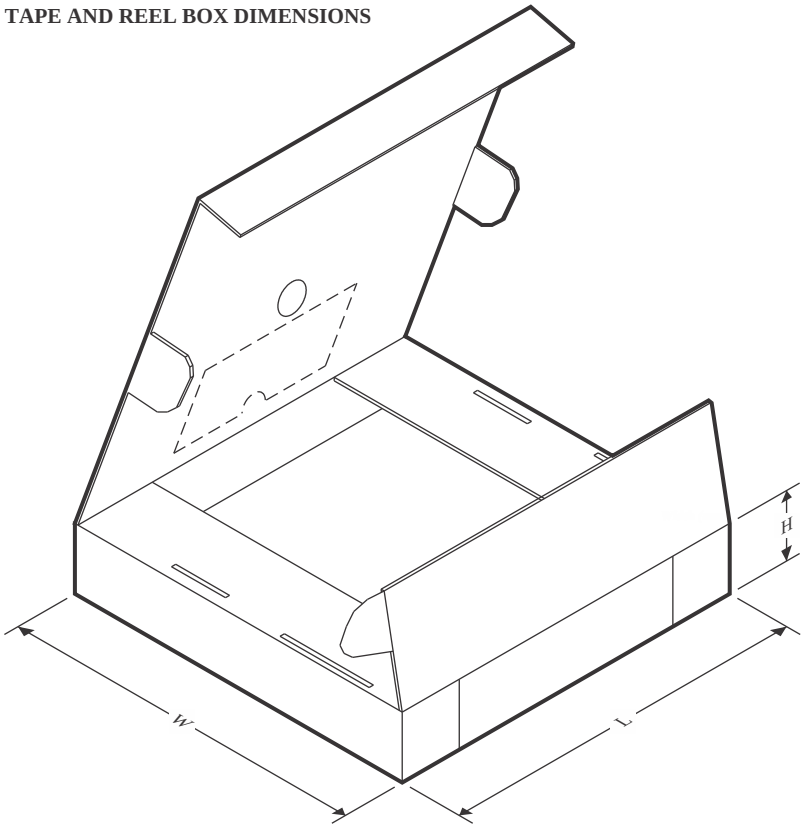
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83TC815RHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83TC815RHARQ1	VQFN	RHA	36	2500	360.0	360.0	36.0

GENERIC PACKAGE VIEW

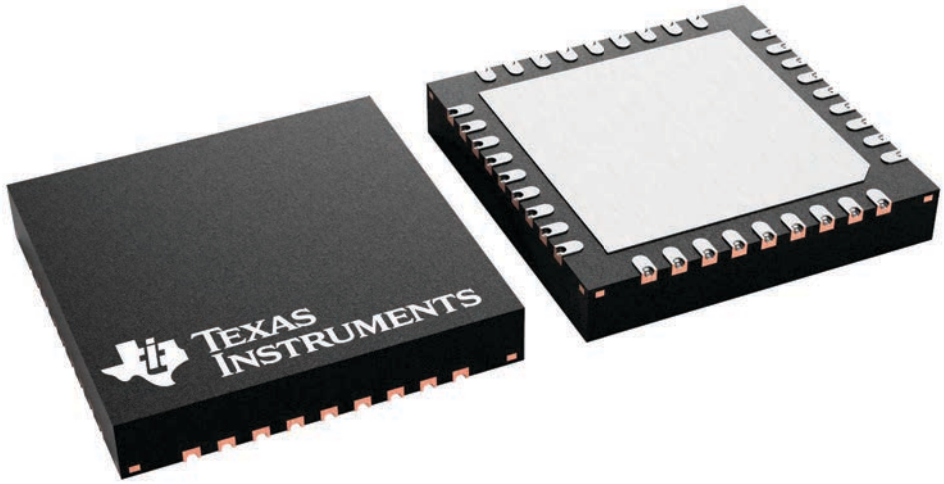
RHA 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



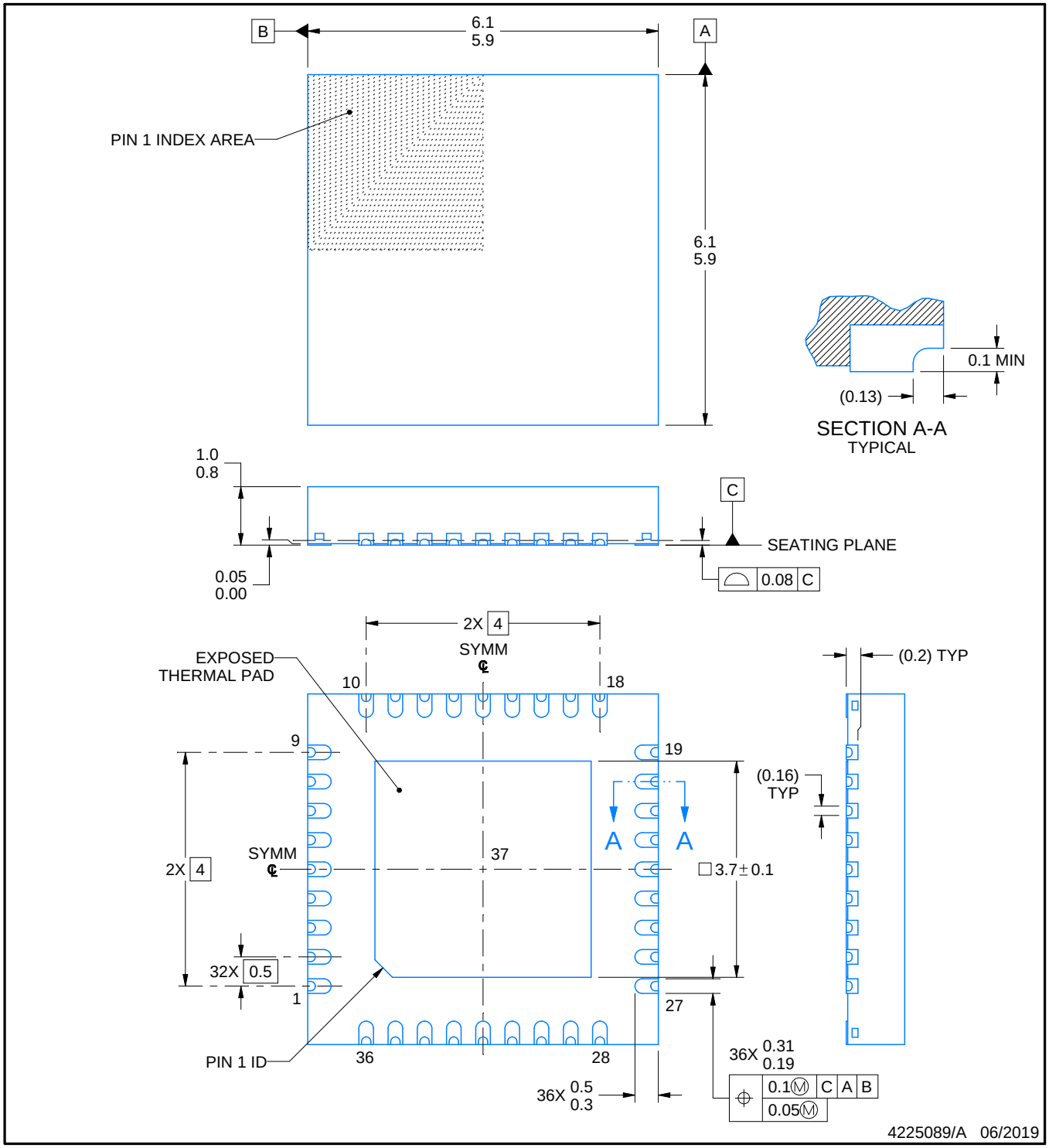
4228438/A

PACKAGE OUTLINE

RHA0036A

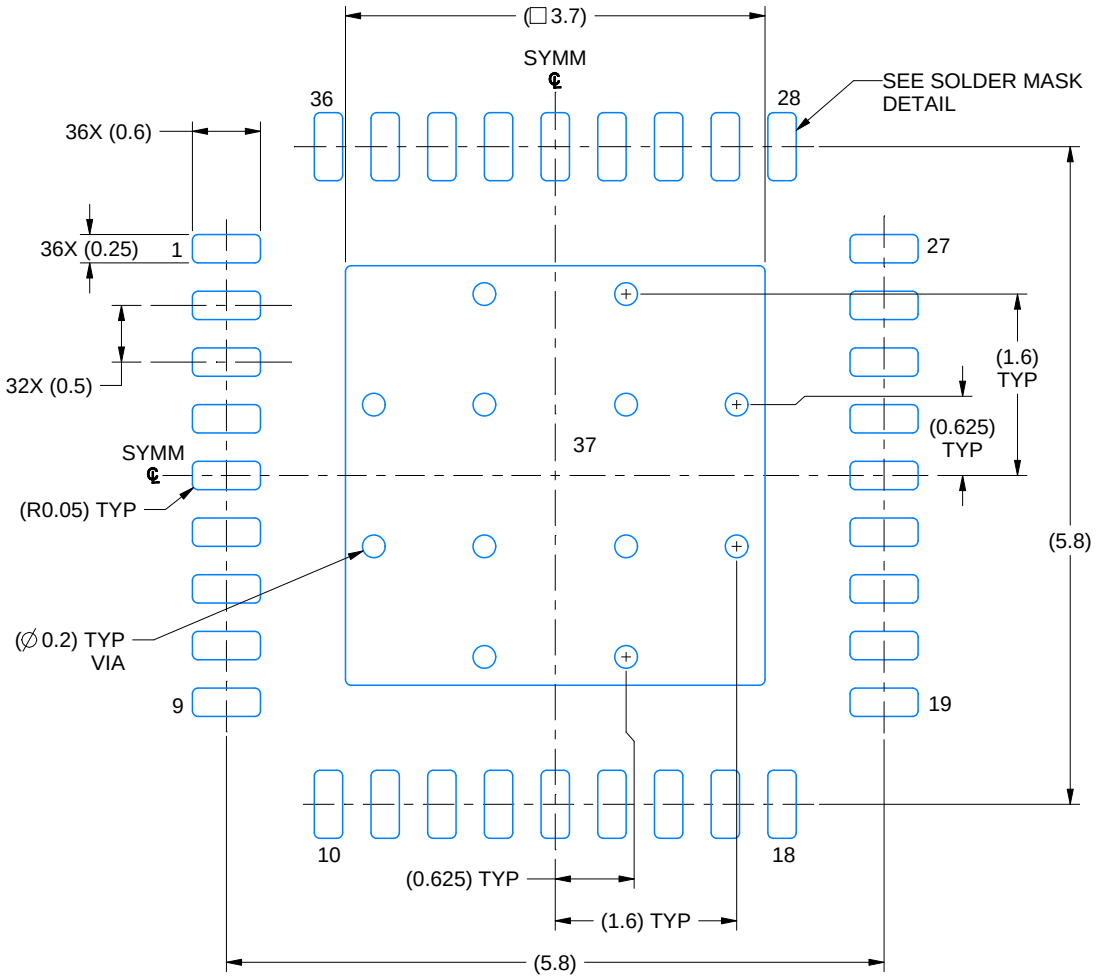
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

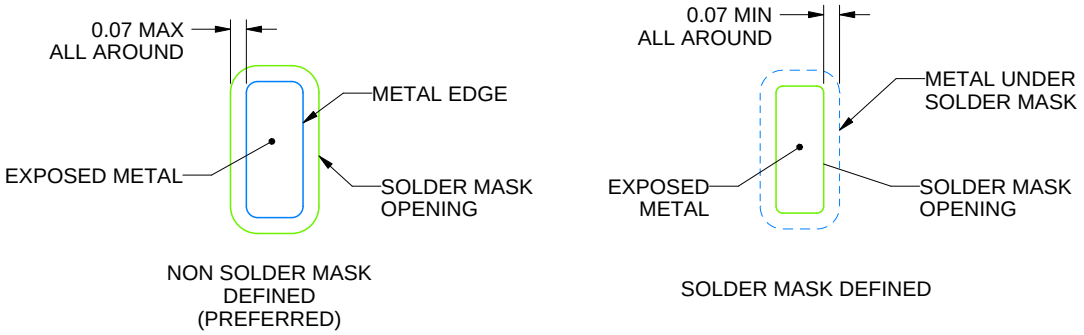


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

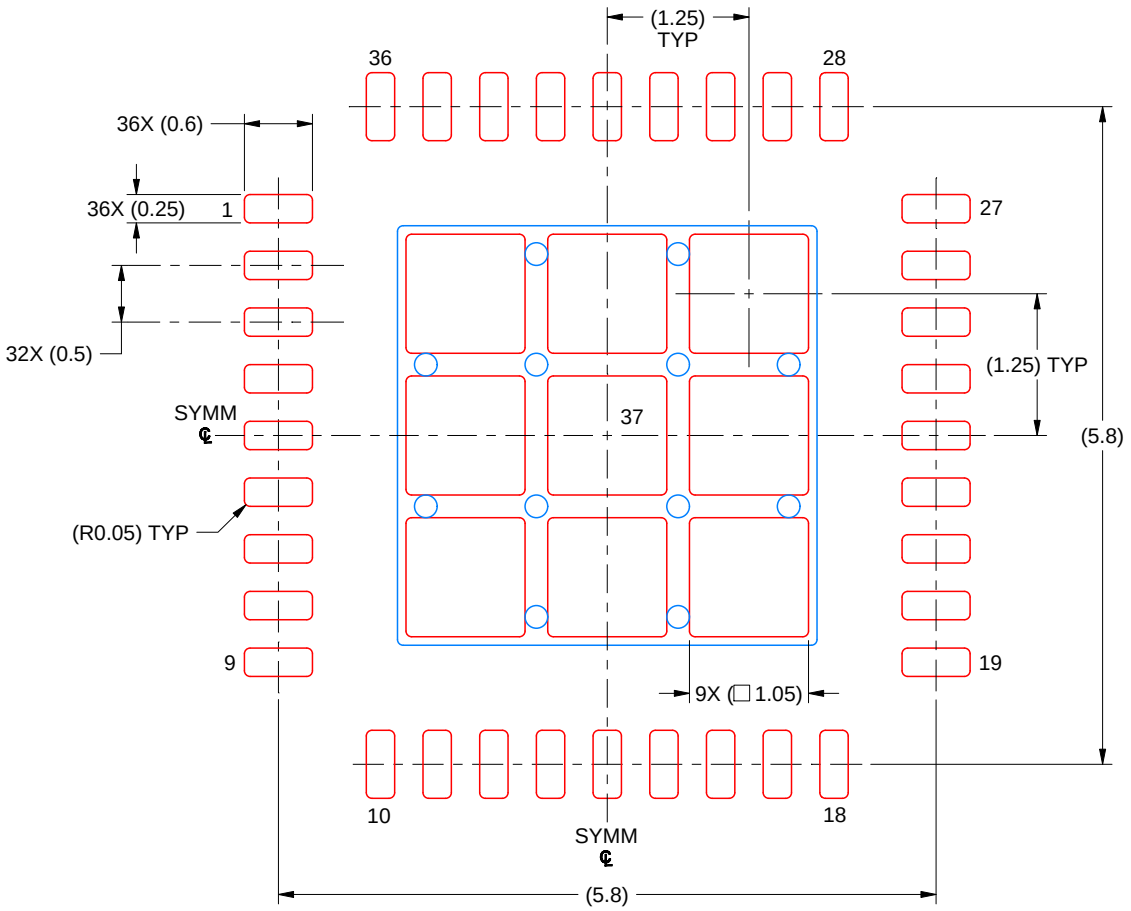


SOLDER MASK DETAILS

4225089/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225089/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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