ESD2CANFD24W-Q1 24V, 2-Channel ESD Protection Diode in DFN1110 Industry Standard Package for In-Vehicle Networks

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±23kV contact discharge
  - ±23kV air-gap discharge
- ISO 10605 (330 pF, 330 Ω) ESD protection:
  - ±18kV contact discharge
  - ±18kV air-gap discharge
- Tested in compliance to IEC 61000-4-5
- 24V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD protection with single component
- Low clamping voltage protects downstream components
- AEC-Q101 qualified
- I/O capacitance = 2pF (typical)
- DFN1110 (DXA) small, standard, common footprint

2 Applications

- Automotive in-vehicle networks:
  - Controller area network (CAN)
  - Controlled area network flexible data-rate (CAN-FD)
  - Low, fault tolerant CAN
  - High-speed CAN
- Industrial control networks:
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4

3 Description

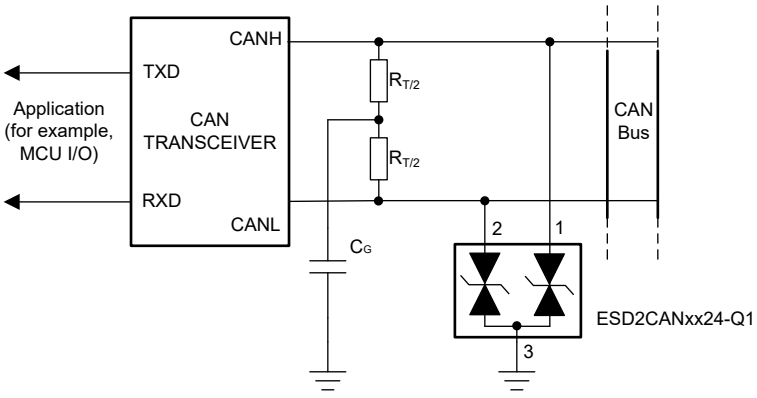
ESD2CANFD24W-Q1 is a bidirectional ESD protection diode for Controller Area Network (CAN) interface protection. ESD2CANFD24W-Q1 is rated to dissipate contact ESD strikes specified in the ISO 10605 automotive standard. The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key as automotive systems require a high level of robustness and reliability for safety applications.

This device features a low IO capacitance per channel and a pin-out to suit two automotive CAN bus lines (CANH and CANL) from the damage caused by ElectroStatic Discharge (ESD) and other transients. Additionally, the 2pF (typical) line capacitance of ESD2CANFD24W-Q1 is designed for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10Mbps.

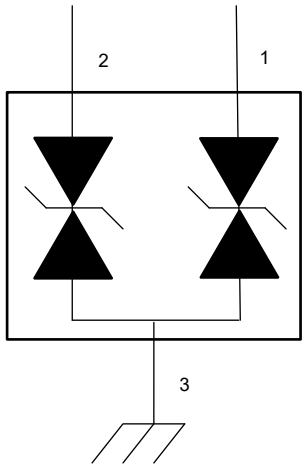
Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
ESD2CANFD24W-Q1	DXA (DFN1110, 3)	1.1mm × 1.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



ESD2CANxx24-Q1 Typical Application



Functional Block Diagram

Table of Contents

4 Pin Configuration and Functions

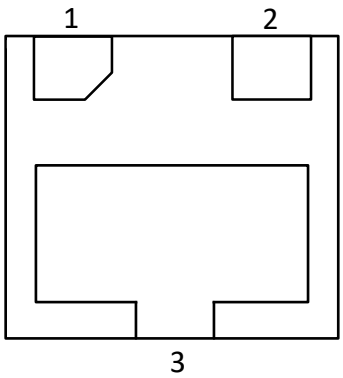


Figure 4-1. DXA Package, 3-Pin DFN-1110 (Bottom View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20µs) at 25°C		133	W
	IEC 61000-4-5 current (t_p - 8/20µs) at 25°C		3	A
T_A	Operating free-air temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001	± 2500	V
		Charged device model (CDM), per AEC Q101-005	± 1000	

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±23000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±23000	

5.4 ESD Ratings - ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605, 150pF, 330Ω, IO	Contact discharge	± 23000	V
			Air-gap discharge	± 23000	
		ISO 10605, 330pF, 330Ω, IO	Contact discharge	± 18000	
			Air-gap discharge	± 18000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC[1]		ESD2CANFD24W-Q1 DXA (DFN1110-3) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	318.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	164.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	26.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	163.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.7 Electrical Characteristics

over T_A = 25°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		–24		24	V
V_{BR}	Breakdown voltage	I_{IO} = 10mA, both Positive and Negative	25.5		35.5	V
I_{LEAK}	Leakage current, any IO pin to GND	V_{IO} = ±24V	-20	1	20	nA
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 3A, t_p = 8/20µs, from IO to GND		37		V
	Clamping voltage(3)	I_{PP} = 16A, TLP, from IO to GND		42		
R_{DYN}	Dynamic resistance(3)	IO to GND		0.61		Ω
		GND to IO		0.61		
C_L	Line capacitance, any IO to GND	V_{IO} = 0V, f = 1MHz, V_{p-p} = 30mV		2		pF

(1) Measurements made on both IO channels
(2) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

6 Typical Characteristics

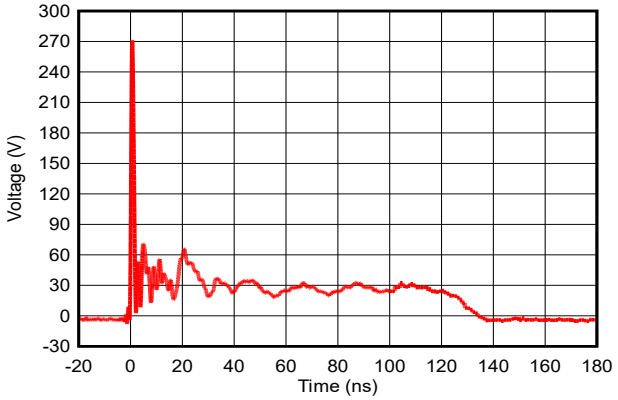


Figure 6-1. +8kV Clamped IEC Waveform

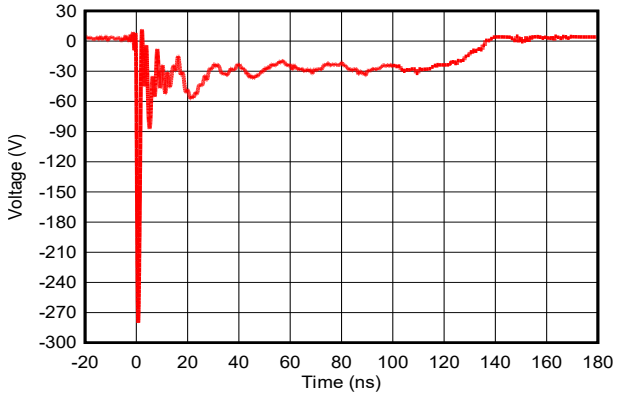


Figure 6-2. -8kV Clamped IEC Waveform

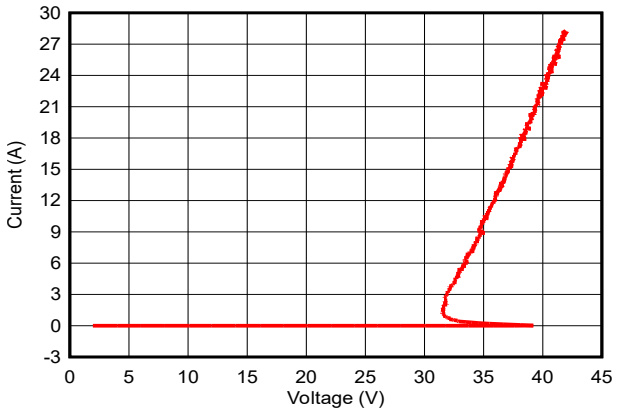


Figure 6-3. Positive TLP Curve

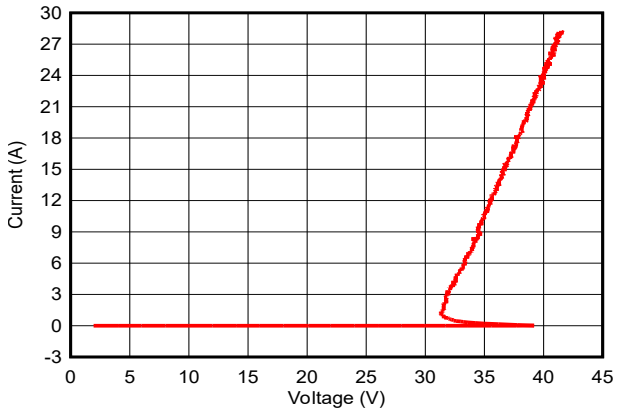


Figure 6-4. Negative TLP Curve

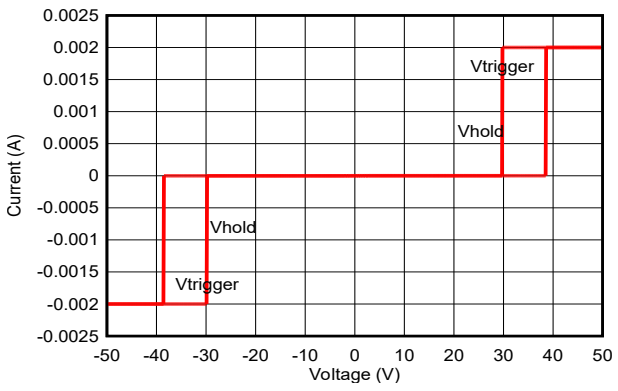


Figure 6-5. DC I-V Curve

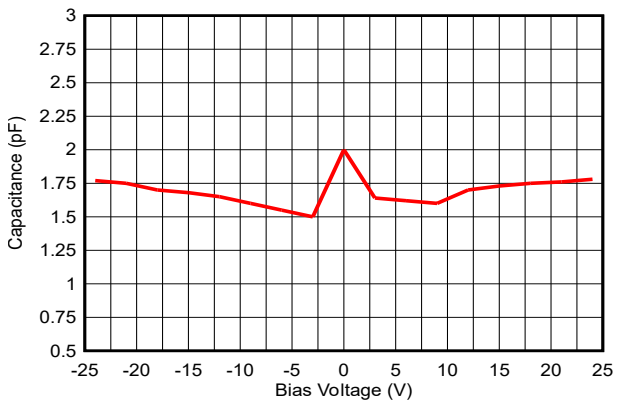


Figure 6-6. Bias Voltage vs. Capacitance

6 Typical Characteristics (continued)

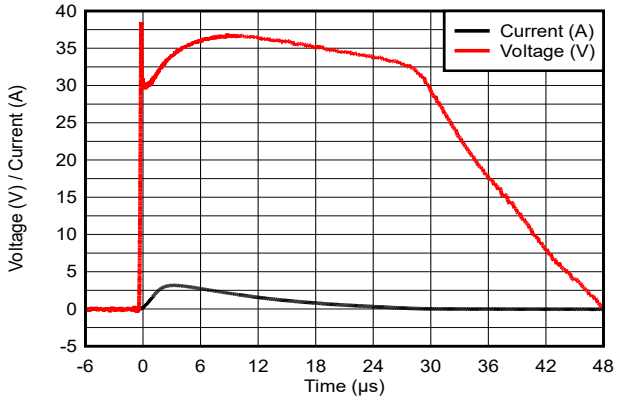


Figure 6-7. 8/20µs Surge Response

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD2CANFD24WDXARQ1	Active	Production	USON (DXA) | 3	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	1VO

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

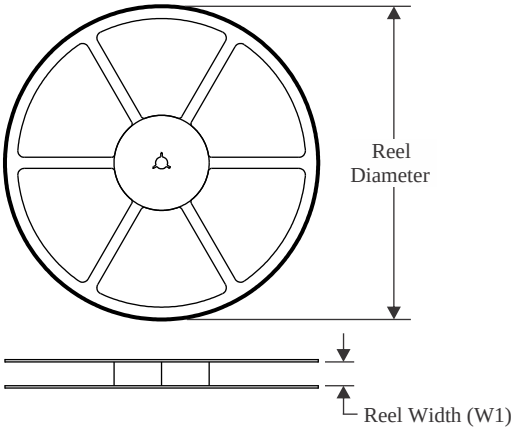
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

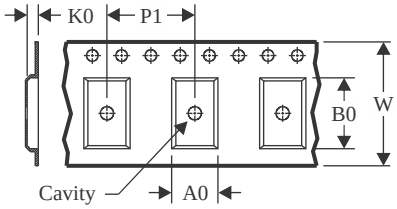
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

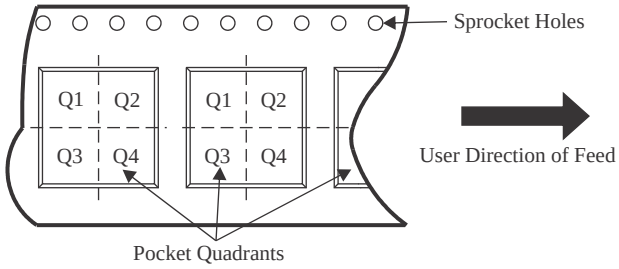


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

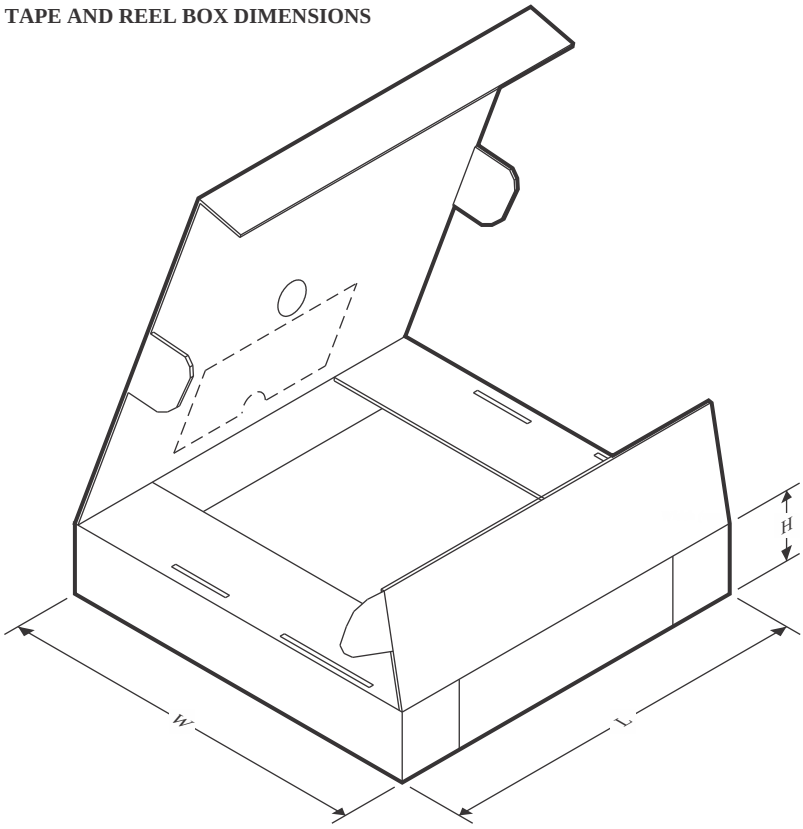
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CANFD24WDXARQ1	USON	DXA	3	3000	180.0	8.4	1.2	1.3	0.65	4.0	8.0	Q1

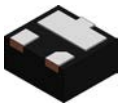
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CANFD24WDXARQ1	USON	DXA	3	3000	210.0	185.0	35.0

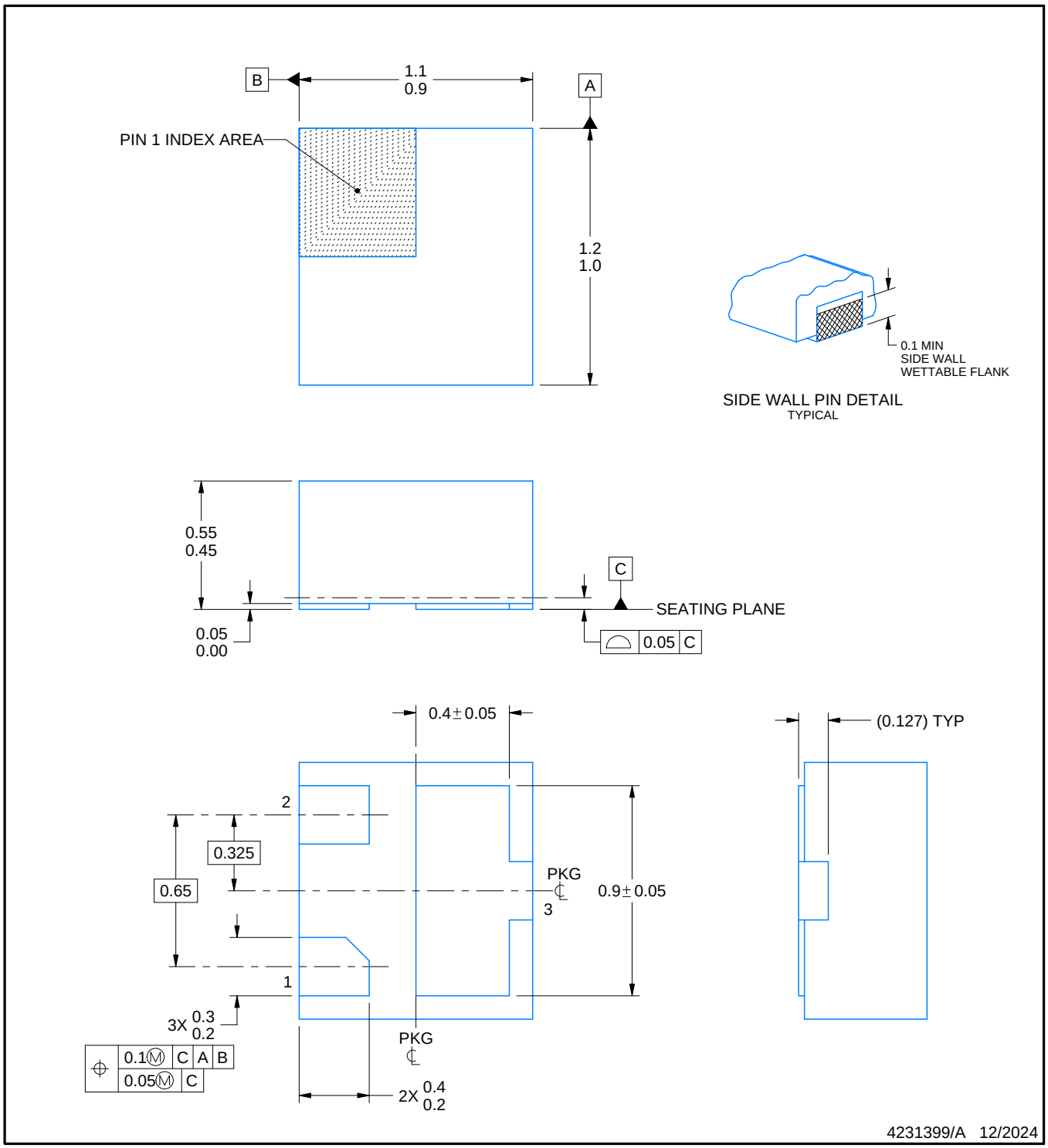
DXA0003A



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

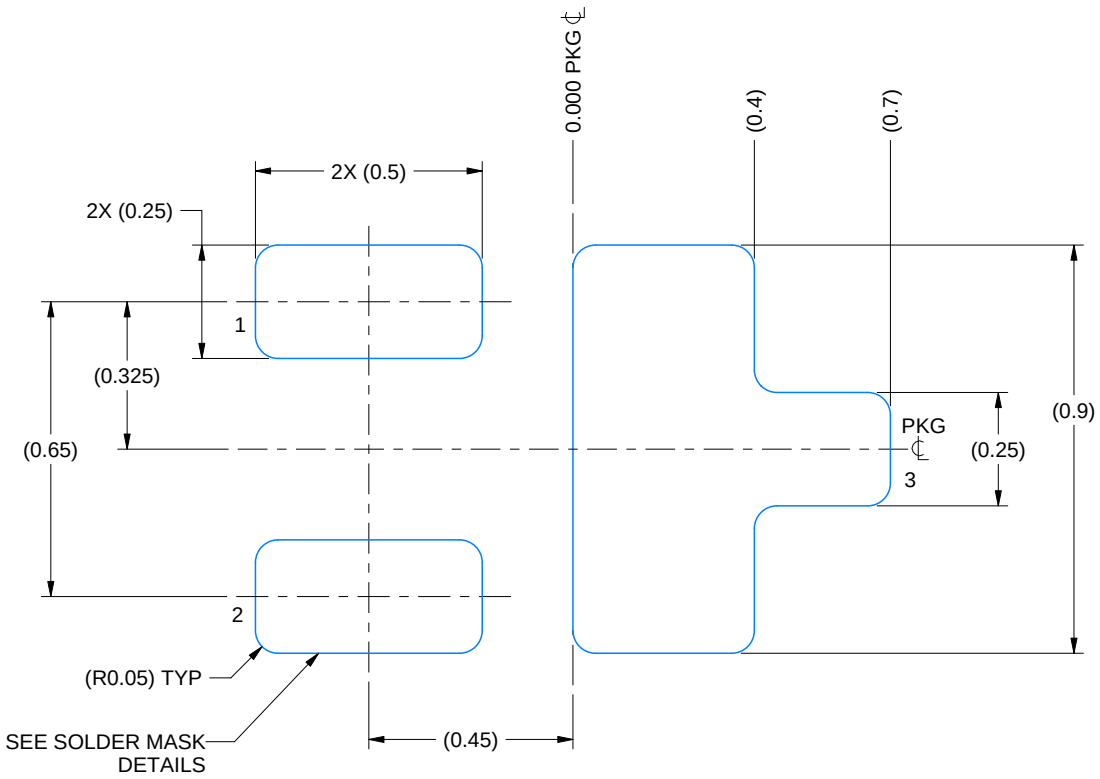
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

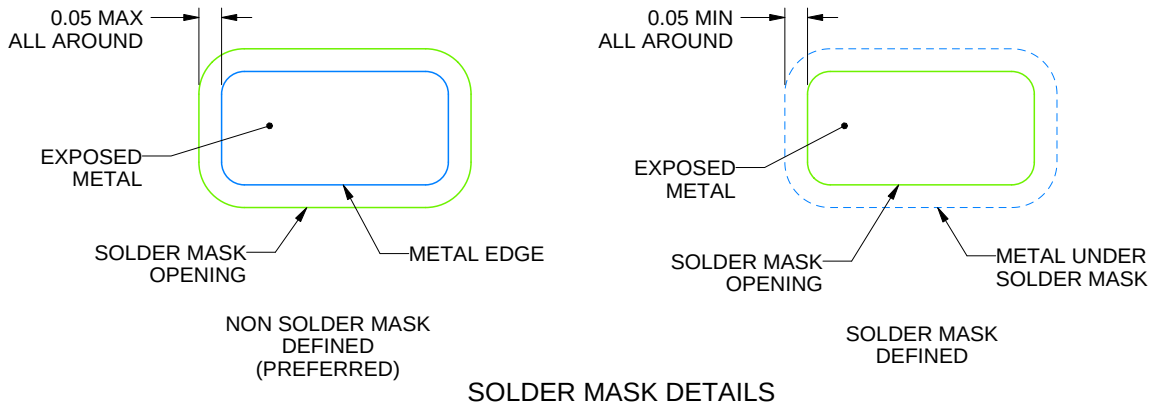
DXA0003A

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 60X



SOLDER MASK DETAILS

4231399/A 12/2024

NOTES: (continued)

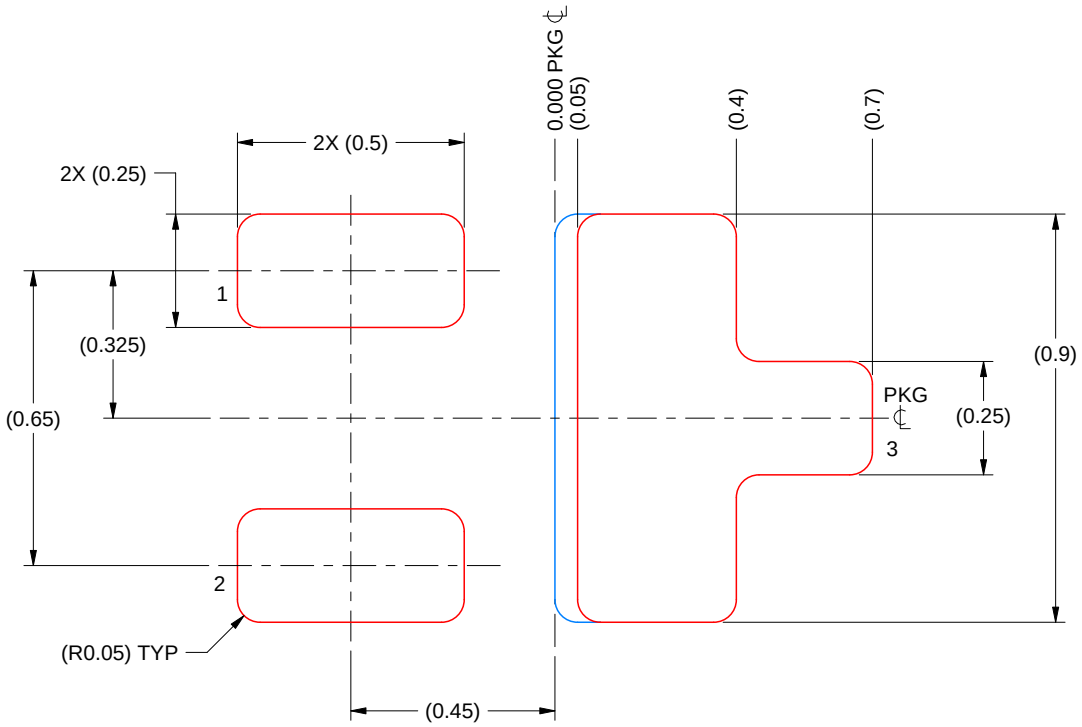
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DXA0003A

USON - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 60X

EXPOSED PAD 3
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231399/A 12/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025