

# ESD762 24V, 2-Channel, ESD Protection With 2.5A of 8/20μs Surge Protection in a SOT-23 Package

## 1 Features

- Robust surge protection:
  - IEC 61000-4-5 (8/20μs): 2.5A
- IEC 61000-4-2 level 4 ESD protection:
  - ±18kV contact discharge
  - ±18kV air-gap discharge
- 24V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD and surge protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 1.7pF (typical)
- SOT-23 (DBZ) small, standard, common footprint
- Leaded packages used for automatic optical inspection (AOI)

## 2 Applications

- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- [Industrial control networks](#):
  - Smart distribution system (SDS)
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4
  - 4/20mA circuits
  - PLC surge protection
  - ADC surge protection

## 3 Description

ESD762 is a bidirectional ESD protection diode for USB power delivery (USB-PD) and industrial interfaces. ESD762 is rated to dissipate contact ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 level 4 standard (±18kV contact and ±18kV airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

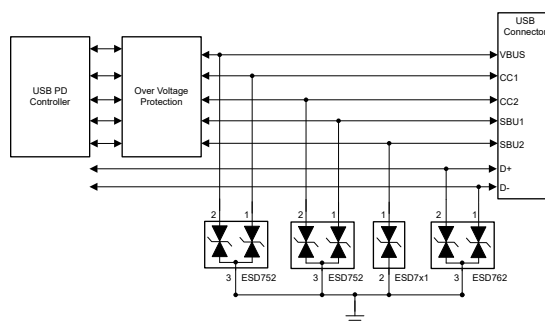
These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The  $I_{PP} = 2.5A$  (8/20μs surge waveform) capability of the ESD762 makes it suitable for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 1.7pF line capacitance of the ESD762 is suitable for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

The ESD762 are offered in the SOT-23 package for easy flow through routing.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM) |
|-------------|------------------------|-----------------|
| ESD762      | DBZ (SOT-23, 3)        | 2.92mm × 2.37mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



USB Power Delivery Application

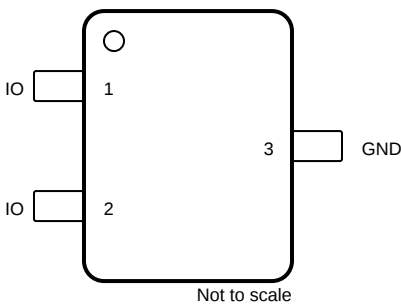
### USB Power Delivery Typical Application



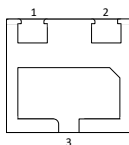
## Table of Contents

|   |          |  |           |
|---|----------|--|-----------|
| <b>1 Features</b> .....                         | <b>1</b> | <b>7 Application and Implementation</b> .....          | <b>11</b> |
| <b>2 Applications</b> .....                     | <b>1</b> | 7.1 Application Information.....                       | 11        |
| <b>3 Description</b> .....                      | <b>1</b> | 7.2 Typical Application.....                           | 11        |
| <b>4 Pin Configuration and Functions</b> .....  | <b>3</b> | <b>8 Power Supply Recommendations</b> .....            | <b>12</b> |
| <b>5 Specifications</b> .....                   | <b>4</b> | <b>9 Layout</b> .....                                  | <b>13</b> |
| 5.1 Absolute Maximum Ratings.....               | 4        | 9.1 Layout Guidelines.....                             | 13        |
| 5.2 ESD Ratings—JEDEC Specification.....        | 4        | 9.2 Layout Example.....                                | 13        |
| 5.3 ESD Ratings—IEC Specification.....          | 4        | <b>10 Device and Documentation Support</b> .....       | <b>14</b> |
| 5.4 Recommended Operating Conditions.....       | 4        | 10.1 Documentation Support.....                        | 14        |
| 5.5 Thermal Information.....                    | 4        | 10.2 Receiving Notification of Documentation Updates.. | 14        |
| 5.6 Electrical Characteristics.....             | 5        | 10.3 Support Resources.....                            | 14        |
| 5.7 Typical Characteristics – ESD762 (DBZ)..... | 6        | 10.4 Trademarks.....                                   | 14        |
| 5.8 Typical Characteristics – ESD762 (DXA)..... | 7        | 10.5 Electrostatic Discharge Caution.....              | 14        |
| <b>6 Detailed Description</b> .....             | <b>9</b> | 10.6 Glossary.....                                     | 14        |
| 6.1 Overview.....                               | 9        | <b>11 Revision History</b> .....                       | <b>15</b> |
| 6.2 Functional Block Diagram.....               | 9        | <b>12 Mechanical, Packaging, and Orderable</b>         |           |
| 6.3 Feature Description.....                    | 9        | <b>Information</b> .....                               | <b>15</b> |
| 6.4 Device Functional Modes.....                | 10       |  |           |

## 4 Pin Configuration and Functions



**Figure 4-1. DBZ Package, 3-Pin SOT-23 (Top View)**



**Figure 4-2. DXA Package, 3-Pin DFN1110-3 (Bottom View)**

**Table 4-1. Pin Functions**

| PIN  |      | TYPE <sup>(1)</sup> | DESCRIPTION        |
|------|------|---------------------|--------------------|
| NAME | NO.  |                     |                    |
| IO   | 1, 2 | I/O                 | ESD protected IO   |
| GND  | 3    | G                   | Connect to ground. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

| PARAMETER        |   | MIN | MAX | UNIT |
|------------------|---|-----|-----|------|
| P <sub>pp</sub>  | IEC 61000-4-5 Power (t <sub>p</sub> – 8/20μs) at 25°C   |     | 90  | W    |
| I <sub>pp</sub>  | IEC 61000-4-5 current (t <sub>p</sub> – 8/20μs) at 25°C |     | 2.5 | A    |
| T <sub>A</sub>   | Operating free-air temperature                          | -55 | 150 | °C   |
| T <sub>J</sub>   | Junction temperature                                    | -55 | 150 | °C   |
| T <sub>stg</sub> | Storage temperature                                     | -65 | 155 | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings—JEDEC Specification

| PARAMETER          |                         | TEST CONDITION  | VALUE  | UNIT |
|--------------------|-------------------------|---|--------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>         | ± 2500 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JS-002 <sup>(2)</sup> | ± 1000 |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 ESD Ratings—IEC Specification

over T<sub>A</sub> = 25°C (unless otherwise noted)

| PARAMETER          |                         | TEST CONDITION                            | VALUE  | UNIT |
|--------------------|-------------------------|---|--------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | IEC 61000-4-2 Contact Discharge, all pins | ±18000 | V    |
|                    |                         | IEC 61000-4-2 Air Discharge, all pins     | ±18000 | V    |

### 5.4 Recommended Operating Conditions

| PARAMETER       |                                | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|-----|------|
| V <sub>IN</sub> | Input voltage                  | -24 |     | 24  | V    |
| T <sub>A</sub>  | Operating free-air temperature | -55 |     | 150 | °C   |

### 5.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ESD762       | UNIT |
|-------------------------------|--|--------------|------|
|                               |  | DBZ (SOT-23) |      |
|                               |  | 3 PINS       |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 325.3        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 178.8        | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 165.5        | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 52.4         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 164.4        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A          | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.6 Electrical Characteristics

over  $T_A = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER   |  | TEST CONDITIONS   | PACKAGE        | MIN   | TYP  | MAX   | UNIT     |
|-------------|--|---|----------------|-------|------|-------|----------|
| $V_{RWM}$   | Reverse stand-off voltage                |   | All Packages   | -24   |      | 24    | V        |
| $V_{BRF}$   | Forward breakdown voltage <sup>(2)</sup> | $I_{IO} = 10\text{mA}$ , IO to GND                                | All Packages   | 25.5  |      | 35.5  | V        |
| $V_{BRR}$   | Reverse breakdown voltage <sup>(2)</sup> | $I_{IO} = -10\text{mA}$ , IO to GND                               | All Packages   | -35.5 |      | -25.5 | V        |
| $V_{CLAMP}$ | Clamping voltage <sup>(3)</sup>          | $I_{PP} = 2.5\text{A}$ , $t_p = 8/20\mu\text{s}$ , from IO to GND | All Packages   |       | 36   |       | V        |
|             | Clamping voltage <sup>(4)</sup>          | $I_{PP} = 16\text{A}$ , TLP, IO to GND or GND to IO               | SOT-23 & SC-70 |       | 38   |       | V        |
|             |  |   | DFN1110-3      |       | 42   |       | V        |
| $I_{LEAK}$  | Leakage current                          | $V_{IO} = \pm 24\text{V}$ , IO to GND                             | All Packages   | -50   | 5    | 50    | nA       |
| $R_{DYN}$   | Dynamic resistance <sup>(4)</sup>        | IO to GND and GND to IO   | SOT-23 & SC-70 |       | 0.57 |       | $\Omega$ |
|             |  |   | DFN1110-3      |       | 0.68 |       | $\Omega$ |
| $C_L$       | Line capacitance <sup>(5)</sup>          | $V_{IO} = 0\text{V}$ , $f = 1\text{MHz}$ , $V_{pp} = 30\text{mV}$ | All Packages   |       | 1.7  | 2.8   | pF       |

(1) Measurements made on each IO channel.

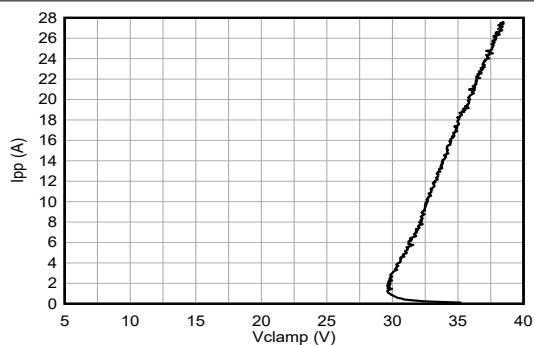
(2)  $V_{BRF}$  and  $V_{BRR}$  are defined as the voltage when +/- 10mA is applied in the positive or negative direction respectively, before the device latches into the snapback state.

(3) Device stressed with 8/20 $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.

(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

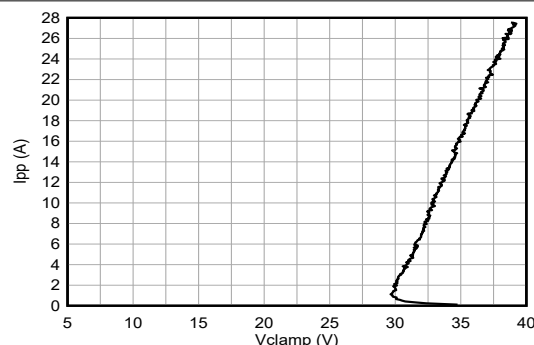
(5) Measured from IO to GND on each channel.

## 5.7 Typical Characteristics – ESD762 (DBZ)



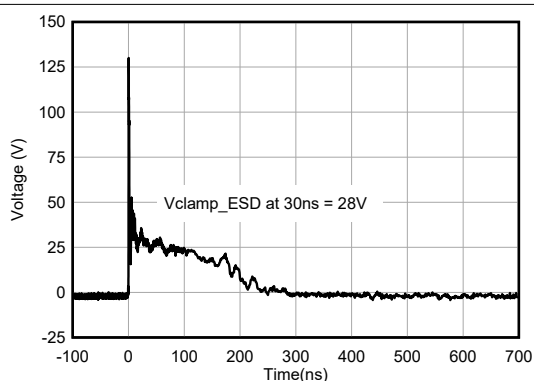
tp = 100 ns, Transmission Line Pulse (TLP)

**Figure 5-1. Positive TLP Curve**

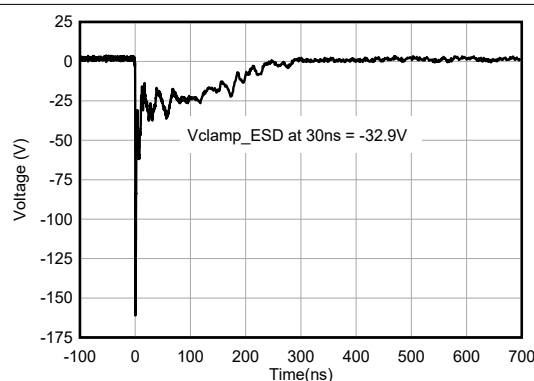


tp = 100 ns, Transmission Line Pulse (TLP)

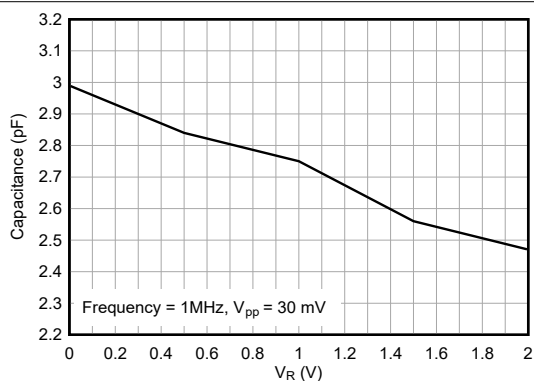
**Figure 5-2. Negative TLP Curve**



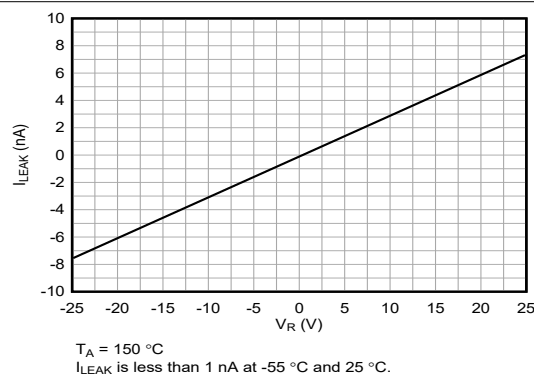
**Figure 5-3. +8-kV Clamped IEC Waveform**



**Figure 5-4. -8-kV Clamped IEC Waveform**



**Figure 5-5. Capacitance vs. Bias Voltage**



**Figure 5-6. Leakage Current vs. Bias Voltage Across Temperature**

## 5.7 Typical Characteristics – ESD762 (DBZ) (continued)

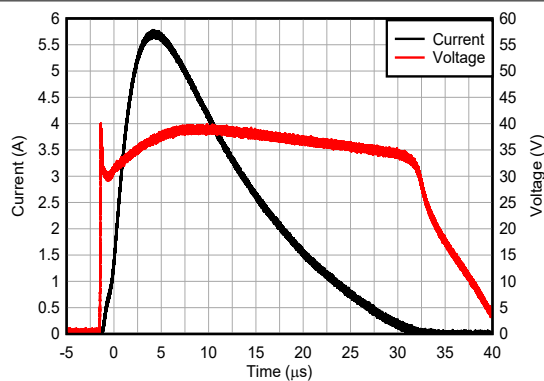


Figure 5-7. 8/20  $\mu$ s Surge Response at 5.7A

## 5.8 Typical Characteristics – ESD762 (DXA)

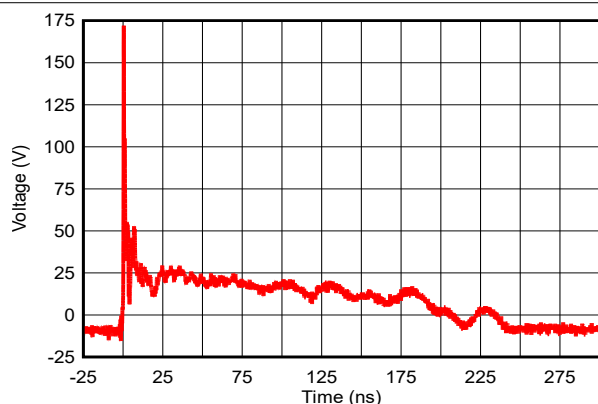


Figure 5-8. +8kV Clamped IEC Waveform

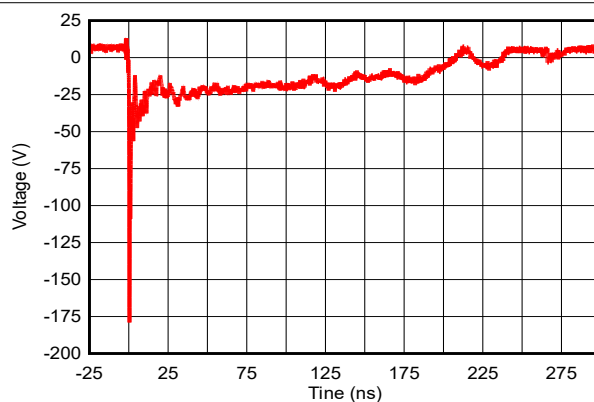


Figure 5-9. -8kV Clamped IEC Waveform

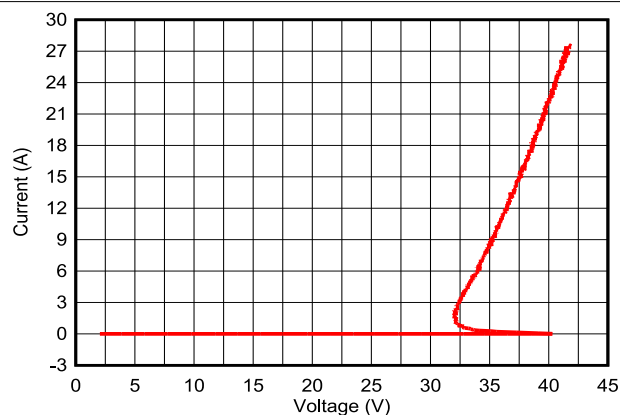


Figure 5-10. Positive TLP Curve

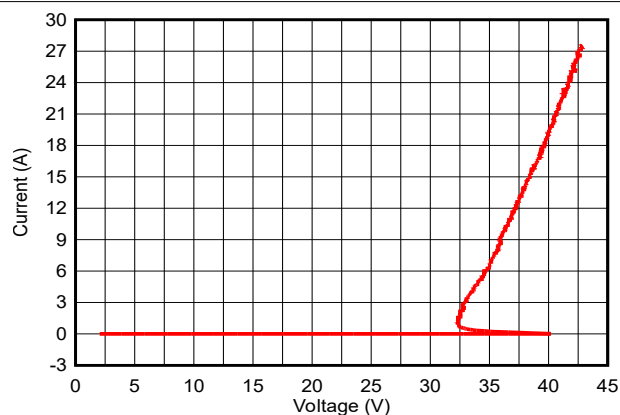


Figure 5-11. Negative TLP Curve

## 5.8 Typical Characteristics – ESD762 (DXA) (continued)

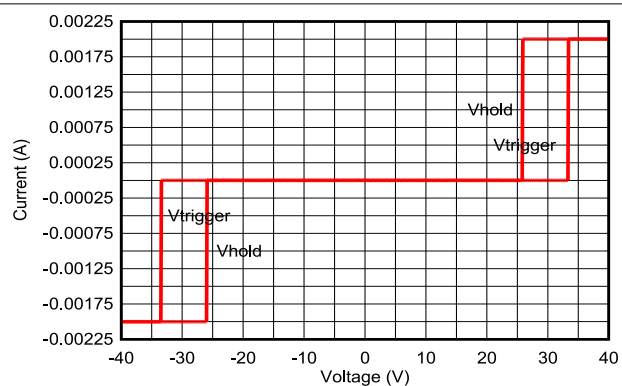


Figure 5-12. DC-IV Characteristics

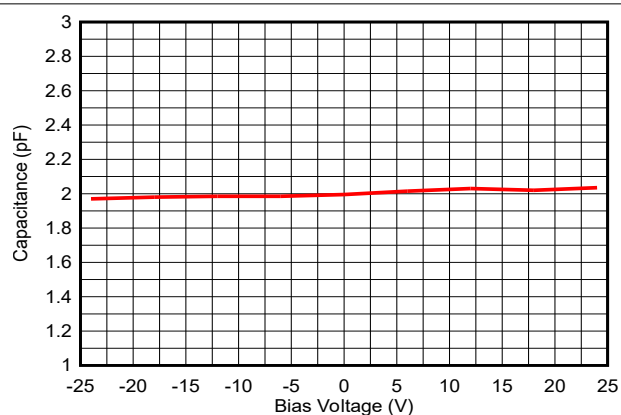


Figure 5-13. Capacitance vs. Bias Voltage

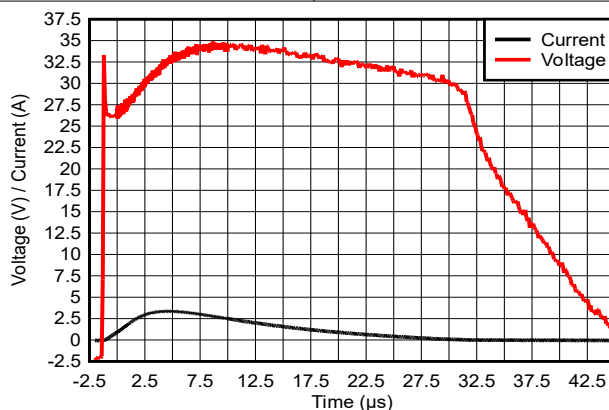


Figure 5-14. 8/20µs Surge Response



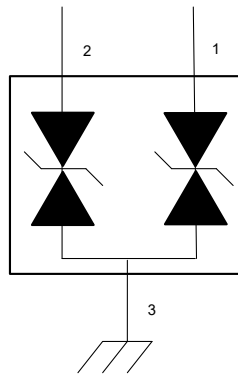
## 6 Detailed Description

### 6.1 Overview

ESD762 is a dual-channel ESD TVS diode in a SOT-23 leaded package which is convenient for automatic optical inspection. This product offers IEC 61000-4-2  $\pm 18\text{kV}$  contact & air-gap ESD protection respectively, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support.

A typical application of this product is the ESD protection for USB-PD slower speed signals (CC1, CC2, SBU1, SBU2, D+, and D-). The  $I_{PP} = 2.5\text{A}$  (8/20 $\mu\text{s}$  surge waveform) capability of the ESD762 makes it suitable for protecting VBUS. ESD762 is also a good fit for protecting industrial IOs requiring 2.5A or less of surge current protection. The 1.7pF line capacitance of this ESD protection diode is suitable for USB-PD slower speed signals and industrial IO applications.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

ESD762 is a bidirectional TVS diodes with a high ESD protection level. This device protects the circuit from ESD strikes up to  $\pm 18\text{kV}$  contact and  $\pm 18\text{kV}$  air-gap as specified in the IEC 61000-4-2 standard. The ESD762 can also handle up to 2.5A of surge current (IEC 61000-4-5 8/20  $\mu\text{s}$ ). The I/O capacitance of 1.7pF (typical) are suitable for USB power delivery slower speed signals and industrial applications. This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits.

For example, the ESD762 clamping voltage is only 36V when the device is taking 2.5A transient current. The breakdown is bidirectional so these protection devices are a good fit for applications requiring positive and negative polarity protection. Low leakage allows these diodes to conserve power when working below the  $V_{RWM}$ . The temperature range of  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 package is good for applications requiring automatic optical inspection (AOI).

#### 6.3.1 Temperature Range

These devices are qualified to operate from  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ .

#### 6.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 2.5A (8/20 $\mu\text{s}$  waveform) for the ESD762. An ESD-surge clamp diverts this current to ground.

#### 6.3.3 IO Capacitance

The capacitance between the I/O pins is 1.7pF for the ESD762. These capacitances are designed for USB power delivery slower speed signals and industrial applications.

#### 6.3.4 Dynamic Resistance

The IO pins feature an ESD clamp that has a low  $R_{DYN}$  of  $0.57\Omega$  for the SOT-23 package, and  $0.68\Omega$  for the DFN1110-3 package, which prevents system damage during ESD events.

### 6.3.5 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of  $\pm 25.5\text{V}$ . This protects sensitive equipment is protected from surges above the reverse standoff voltage of  $\pm 24\text{V}$ .

### 6.3.6 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 50nA (maximum) with a bias of  $\pm 24\text{V}$ .

### 6.3.7 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 36V ( $I_{PP} = 2.5\text{A}$  for 8/20 $\mu\text{s}$  surge waveform), 38V ( $I_{PP} = 16\text{A}$  for TLP, SOT-23 package), and 42V ( $I_{PP} = 16\text{A}$  for TLP, DFN1110-3 package).

### 6.3.8 Industry Standard Leaded Packages

These devices feature industry standard SOT-23 (DBZ) and DFN1110-3 packages for automatic optical inspection (AOI).

## 6.4 Device Functional Modes

The ESD762 are dual channel passive clamp devices that have low leakage during normal operation when the voltage between IO and GND is below  $V_{RWM}$ , and activate when the voltage between IO and GND goes above  $V_{BR}$ . During IEC 61000-4-2 ESD events, transient voltages as high as  $\pm 18\text{kV}$  can be clamped on either channel. When the voltages on the protected lines fall below the  $V_{HOLD}$ , the device reverts back to the low leakage passive state.

## 7 Application and Implementation

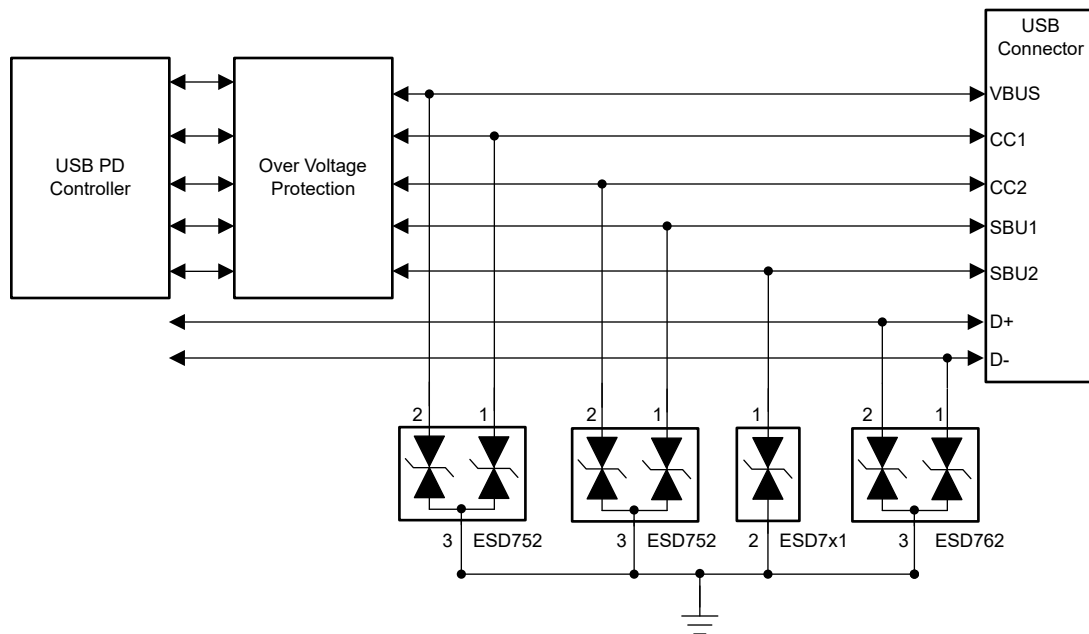
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

ESD762 is a dual channel TVS diode which is used to provide a path to ground for dissipating ESD events on USB-PD or industrial IO signal lines. As the current from the ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC.

### 7.2 Typical Application



USB Power Delivery Application

**Figure 7-1. USB Power Delivery Typical Application**

#### 7.2.1 Design Requirements

For this design example, the ESD762 are used to provide ESD protection on a USB-PD connector. [Table 7-1](#) lists the known design parameters for this application.

**Table 7-1. Design Parameters for the USB Power Delivery Typical Application**

| Design Parameter                | Value         |
|---------------------------------|---------------|
| Diode configuration             | Bidirectional |
| VBUS Voltage                    | + 20V         |
| $V_{IO}$ signal range           | + 3.3V        |
| $V_{RWM}$                       | $\pm 24V$     |
| Short to VBUS event on $V_{IO}$ | $\pm 20V$     |
| Data rate                       | Up to 480Mbps |

### 7.2.2 Detailed Design Procedure

The ESD762 has a  $V_{RWM}$  of  $\pm 24V$  to prevent the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic protects both positive and negative polarity. The low 1.7pF capacitance of the ESD762 device enables data rates up to 480Mbps, which allows the designer to meet the requirements for the D+ and D- signals. The ESD762 has an  $I_{PP} = 2.5A$  (8/20 $\mu s$ ) surge current capability making it suitable for protecting the VBUS power rail.

### 7.2.3 Application Curves

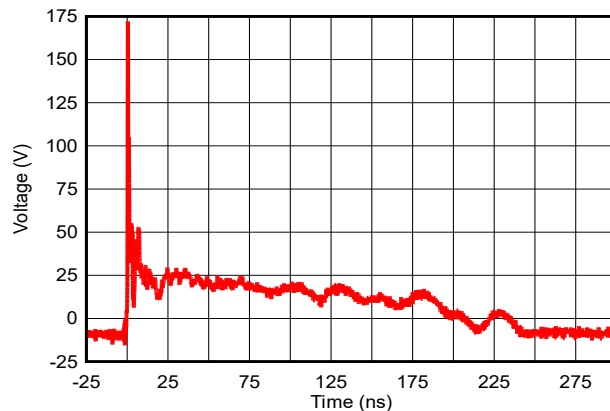


Figure 7-2. +8kV Clamped IEC Waveform

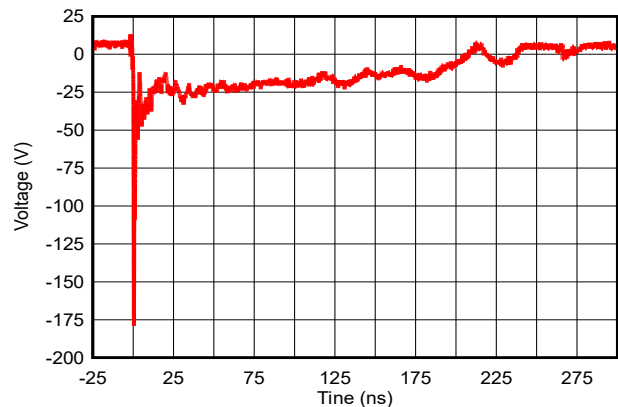


Figure 7-3. -8kV Clamped IEC Waveform

## 8 Power Supply Recommendations

These are passive TVS diode-based ESD protection devices; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

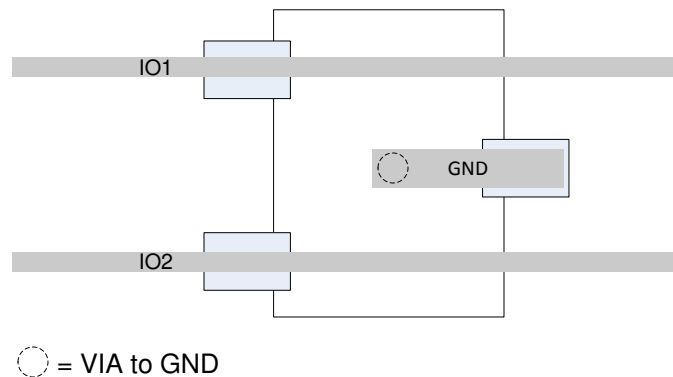
## 9 Layout

### 9.1 Layout Guidelines

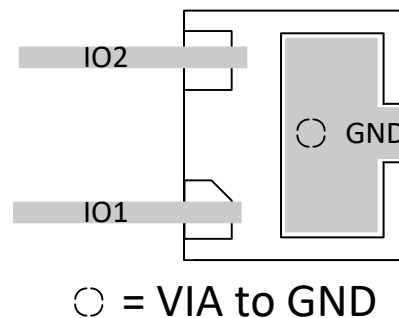
- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

### 9.2 Layout Example

This is a typical example of a dual channel IO routing.



**Figure 9-1. Routing with DBZ Package**



**Figure 9-2. Routing with DXA Package**

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD and Surge Protection for USB Interfaces application note](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision B (November 2022) to Revision C (December 2025) Page

- Removed ESD752 specifications from the data sheet..... 1
- Added DFN1110-3 package to device package options..... 1

### Changes from Revision A (August 2022) to Revision B (November 2022) Page

- Added ESD762 Specifications to the data sheet..... 1

### Changes from Revision \* (May 2022) to Revision A (August 2022) Page

- Changed the status of the data sheet from: *Advanced Information* to: *Production Data* ..... 1

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">ESD762DBZR</a> | Active        | Production           | SOT-23 (DBZ)   3 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 150   | 2RK8                |
| ESD762DBZR.B               | Active        | Production           | SOT-23 (DBZ)   3 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 150   | 2RK8                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

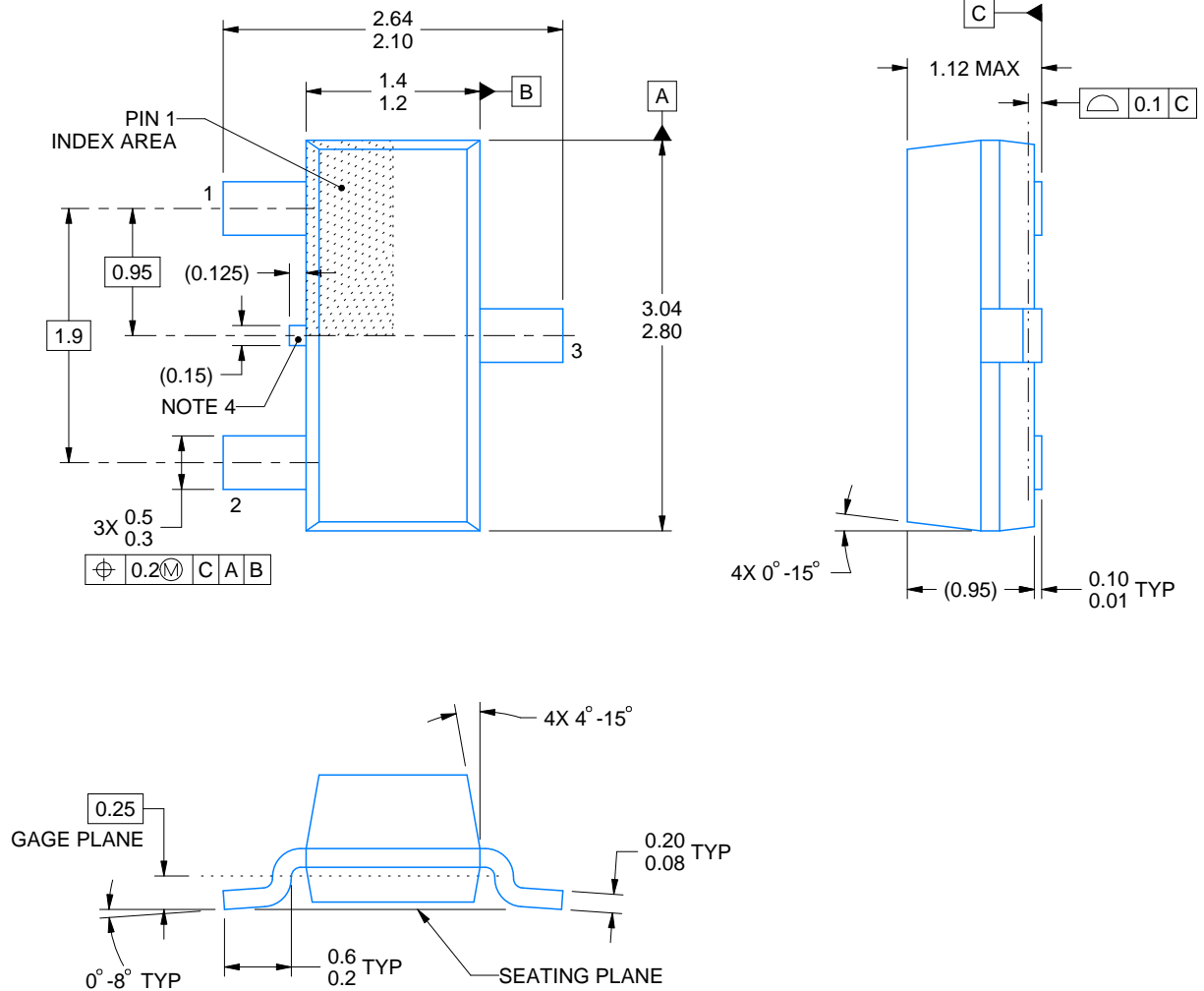
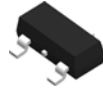
| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ESD762DBZR | SOT-23       | DBZ             | 3    | 3000 | 180.0              | 8.4                | 2.9     | 3.35    | 1.35    | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ESD762DBZR | SOT-23       | DBZ             | 3    | 3000 | 210.0       | 185.0      | 35.0        |



4214838/F 08/2024

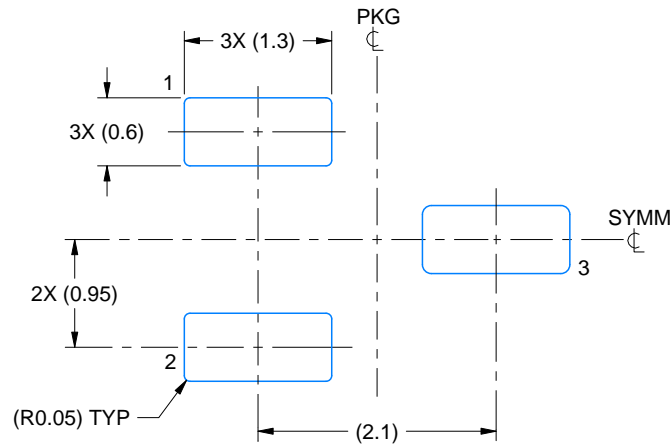
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

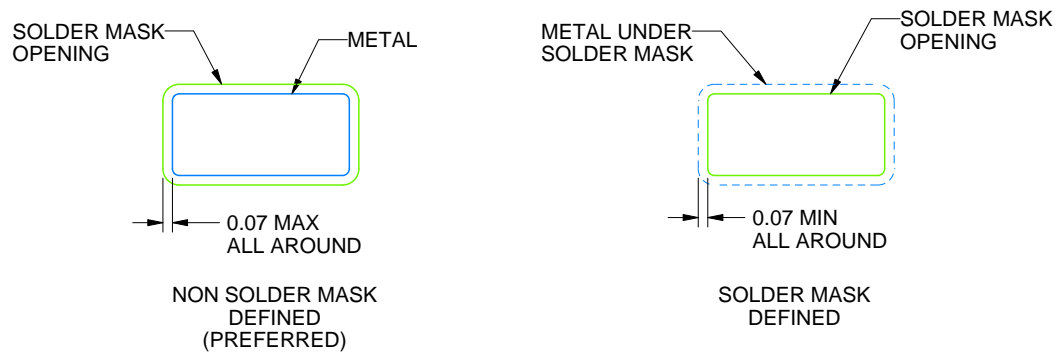
**DBZ0003A**

**SOT-23 - 1.12 mm max height**

## SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



## SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

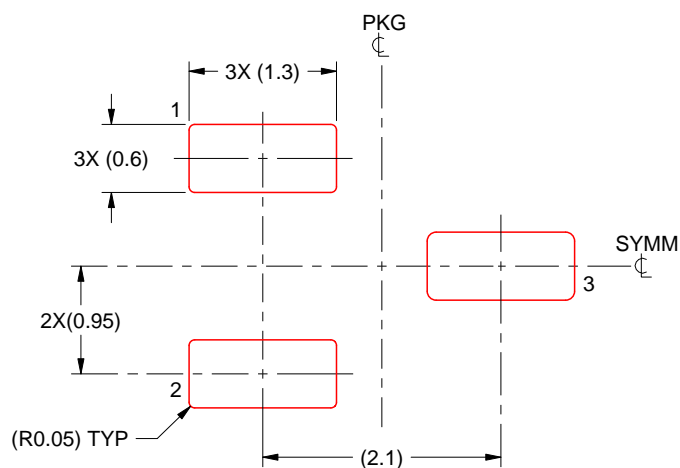
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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