

# ISO774xT-Q1 High-Speed, Reinforced Quad-Channel Digital Isolators With Integrated Transformer Driver

## 1 Features

- Qualified for automotive applications AEC-Q100
- Device temperature Grade 1: –40°C to 125°C ambient operating temperature
- [Functional Safety-Capable](#)
  - Documentation available to aid ISO 26262 system design
- 100Mbps data rate
- Robust isolation barrier:
  - >30-year projected lifetime at 1500V<sub>RMS</sub> working voltage
  - 5000V<sub>RMS</sub> rating
  - Up to 12.8kV surge capability
  - ±150kV/μs typical CMTI for digital isolator
- Wide supply range: 2.25V to 5.5V
- 2.25V to 5.5V level translation
- Default output *high* (ISO774xT) and *low* (ISO774xFT) options
- Low power consumption, typical 1.5mA per channel at 1Mbps
- Low propagation delay: typical 10.7ns at 5V
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
- Push-pull driver for transformers
- High output drive: max 0.7A at 5V supply
- Low R<sub>ON</sub> 0.4Ω max at 4.5V supply
- Spread spectrum clocking
- Typical 1.75A Current-limit for Transformer driver at 5V supply.
- Safety-related certifications (Pending):
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 61010-1, IEC 62368-1, IEC 60601-1, and GB 4943.1 certifications

## 2 Applications

[Hybrid, electric and powertrain system \(EV/HEV\)](#)

- [Battery management system \(BMS\)](#)
- [On-board charger](#)
- [Traction inverter and motor control](#)
- [DC/DC converter](#)

[Body electronics](#)

- [Automotive parking heater module](#)
- [HVAC control module](#)

## 3 Description

The ISO774xT-Q1 is a grade 1, high-performance, quad-channel digital isolator with integrated transformer driver with 5000V<sub>RMS</sub> isolation ratings per UL 1577. This reinforced insulation ratings according to VDE, CSA, TUV and CQC.

The ISO774xT-Q1 device provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO<sub>2</sub>) insulation barrier. If the input power or signal is lost, default output is *high* for devices without suffix F and *low* for devices with suffix F. See the [Device Functional Modes](#) section for further details.

The ISO774xT-Q1 has a low-noise, low-EMI push-pull transformer driver, specifically designed for small form factor, isolated power supplies. The device drives low-profile, center-tapped transformers from a 2.25V to 5.5V DC power supply. Very low noise and EMI are achieved by slew rate control of the output switch voltage and through Spread Spectrum Clocking (SSC). The ISO774xT-Q1 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive ground-referenced N-channel power switches. The device includes two 0.7A Power-MOSFET switches to provide start-up under heavy loads. The internal protection features include a 1.75A current limiting, under-voltage lockout, thermal shutdown, and break-before-make circuitry. ISO774xT-Q1 include a soft-start feature that prevents high inrush current during power up with large load capacitors. ISO774xTA-Q1 has a 160kHz internal oscillator for applications that need to minimize emissions whereas ISO774xTB-Q1 has a 420kHz internal oscillators for applications that require higher efficiency and smaller transformer size.

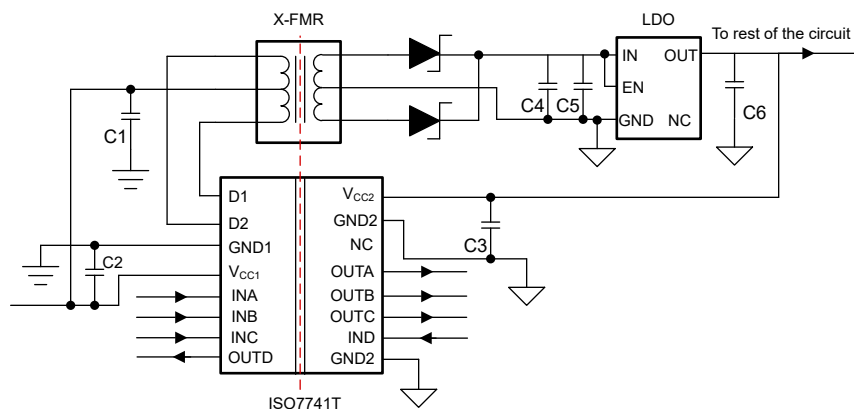
The ISO774xT-Q1 is available in a 16-pin DW package. The device operation is characterized for a temperature range from –40°C to 125°C.



## Package Information

| PART NUMBER   | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)  | PACKAGE SIZE <sup>(2)</sup> |
|---------------|------------------------|------------------|-----------------------------|
| ISO7741Tx-Q1  | DW (SOIC, 16)          | 10.30mm × 7.50mm | 10.30mm × 10.30mm           |
| ISO7741FTx-Q1 | DW (SOIC, 16)          | 10.30mm × 7.50mm | 10.30mm × 10.30mm           |
| ISO7742Tx-Q1  | DW (SOIC, 16)          | 10.30mm × 7.50mm | 10.30mm × 10.30mm           |
| ISO7742FTx-Q1 | DW (SOIC, 16)          | 10.30mm × 7.50mm | 10.30mm × 10.30mm           |

- (1) For all available packages, see [Section 11](#).  
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

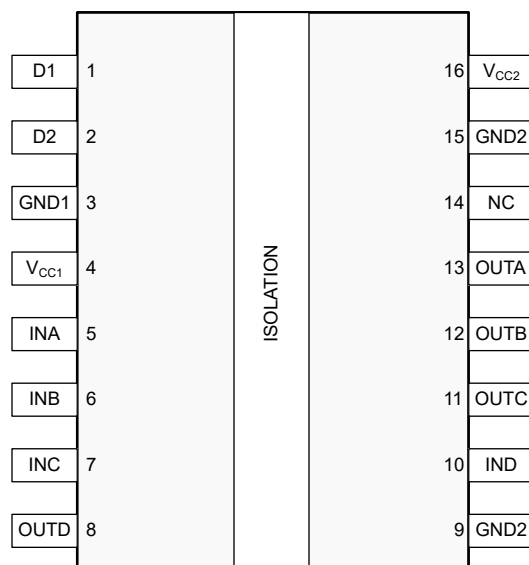


**Simplified Schematic**

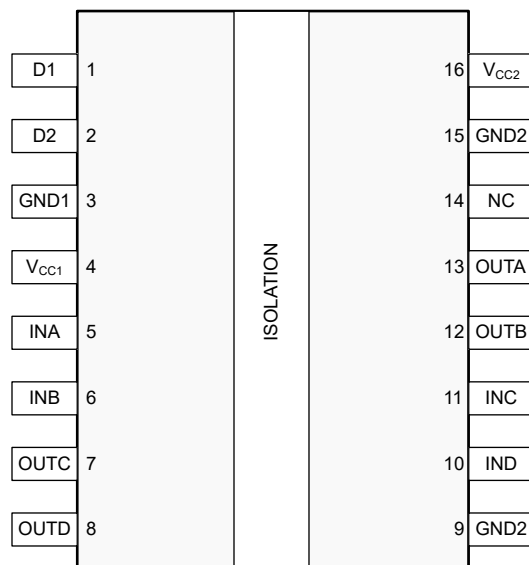
## Table of Contents

|                                                      |          |                                                                  |           |
|------------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                              | <b>1</b> | 5.19 Insulation Characteristics Curves.....                      | <b>21</b> |
| <b>2 Applications</b> .....                          | <b>1</b> | 5.20 Typical Characteristics.....                                | <b>22</b> |
| <b>3 Description</b> .....                           | <b>1</b> | <b>6 Parameter Measurement Information</b> .....                 | <b>25</b> |
| <b>4 Pin Configuration and Functions</b> .....       | <b>4</b> | <b>7 Detailed Description</b> .....                              | <b>27</b> |
| Pin Functions.....                                   | 5        | 7.1 Overview.....                                                | 27        |
| <b>5 Specifications</b> .....                        | <b>6</b> | 7.2 Functional Block Diagram.....                                | 28        |
| 5.1 Absolute Maximum Ratings.....                    | 6        | 7.3 Feature Description.....                                     | 29        |
| 5.2 ESD Ratings.....                                 | 6        | 7.4 Device Functional Modes.....                                 | 30        |
| 5.3 Recommended Operating Conditions.....            | 7        | <b>8 Application and Implementation</b> .....                    | <b>32</b> |
| 5.4 Thermal Information.....                         | 8        | 8.1 Application Information.....                                 | 32        |
| 5.5 Power Ratings.....                               | 8        | 8.2 Typical Application.....                                     | 32        |
| 5.6 Insulation Specifications.....                   | 9        | 8.3 Power Supply Recommendations.....                            | 41        |
| 5.7 Safety-Related Certifications.....               | 10       | 8.4 Layout.....                                                  | 41        |
| 5.8 Safety Limiting Values.....                      | 10       | <b>9 Device and Documentation Support</b> .....                  | <b>43</b> |
| 5.9 Electrical Characteristics Transformer.....      | 11       | 9.1 Documentation Support.....                                   | 43        |
| 5.10 Electrical Characteristics—5V Supply.....       | 12       | 9.2 Receiving Notification of Documentation Updates.....         | 43        |
| 5.11 Supply Current Characteristics—5V Supply.....   | 13       | 9.3 Support Resources.....                                       | 43        |
| 5.12 Electrical Characteristics—3.3V Supply.....     | 14       | 9.4 Trademarks.....                                              | 43        |
| 5.13 Supply Current Characteristics—3.3V Supply..... | 15       | 9.5 Electrostatic Discharge Caution.....                         | 43        |
| 5.14 Electrical Characteristics—2.5V Supply.....     | 16       | 9.6 Glossary.....                                                | 43        |
| 5.15 Supply Current Characteristics—2.5V Supply..... | 17       | <b>10 Revision History</b> .....                                 | <b>43</b> |
| 5.16 Switching Characteristics—5V Supply.....        | 18       | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>44</b> |
| 5.17 Switching Characteristics—3.3V Supply.....      | 19       | 11.1 Tape and Reel Information.....                              | 48        |
| 5.18 Switching Characteristics—2.5V Supply.....      | 20       |                                                                  |           |

## 4 Pin Configuration and Functions



**Figure 4-1. ISO7741T DW Package Top View**



**Figure 4-2. ISO7742T DW Package Top View**

## Pin Functions

| NAME             | PIN                      |                          | Type <sup>(1)</sup> | DESCRIPTION                                                                                                                                                                                                      |
|------------------|--------------------------|--------------------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | ISO7741Tx/<br>ISO7741FTx | ISO7742Tx/<br>ISO7742FTx |                     |                                                                                                                                                                                                                  |
| D1               | 1                        | 1                        | O                   | Open drain output of the first power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, the external traces must be kept short.  |
| D2               | 2                        | 2                        | O                   | Open drain output of the second power MOSFETs. Typically connected to the outer terminals of the center tap transformer. Because large currents flow through these pins, the external traces must be kept short. |
| GND1             | 3                        | 3                        | —                   | Ground connection for V <sub>CC1</sub>                                                                                                                                                                           |
| GND2             | 9                        | 9                        | —                   | Ground connection for V <sub>CC2</sub>                                                                                                                                                                           |
|                  | 15                       | 15                       |                     |                                                                                                                                                                                                                  |
| INA              | 5                        | 5                        | I                   | Input, channel A                                                                                                                                                                                                 |
| INB              | 6                        | 6                        | I                   | Input, channel B                                                                                                                                                                                                 |
| INC              | 7                        | 11                       | I                   | Input, channel C                                                                                                                                                                                                 |
| IND              | 10                       | 10                       | I                   | Input, channel D                                                                                                                                                                                                 |
| NC               | 14                       | 14                       | —                   | Not connected                                                                                                                                                                                                    |
| OUTA             | 13                       | 13                       | O                   | Output, channel A                                                                                                                                                                                                |
| OUTB             | 12                       | 12                       | O                   | Output, channel B                                                                                                                                                                                                |
| OUTC             | 11                       | 7                        | O                   | Output, channel C                                                                                                                                                                                                |
| OUTD             | 8                        | 8                        | O                   | Output, channel D                                                                                                                                                                                                |
| V <sub>CC1</sub> | 4                        | 4                        | —                   | Power supply, side 1                                                                                                                                                                                             |
| V <sub>CC2</sub> | 16                       | 16                       | —                   | Power supply, side 2                                                                                                                                                                                             |

(1) I = Input, O = Output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

See<sup>(1)</sup>

|                          |                               | MIN  | MAX                            | UNIT |
|--------------------------|-------------------------------|------|--------------------------------|------|
| $V_{CC1}, V_{CC2}$       | Supply voltage <sup>(2)</sup> | -0.5 | 6                              | V    |
| V                        | Voltage at INx, OUTx          | -0.5 | $V_{CCX} + 0.5$ <sup>(3)</sup> | V    |
| D1, D2                   | Output switch voltage         |      | 16                             | V    |
| $I_{(D1)PK}, I_{(D2)PK}$ | Peak output switch current    |      | 2.4                            | A    |
| $I_O$                    | Output current                | -15  | 15                             | mA   |
| $T_J$                    | Junction temperature          | -40  | 150                            | °C   |
| $T_{stg}$                | Storage temperature           | -65  | 150                            | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6V.

### 5.2 ESD Ratings

|             |                         |                                                                                         | VALUE | UNIT |
|-------------|-------------------------|-----------------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 HBM ESD Classification Level 3A <sup>(1)</sup> | ±6000 | V    |
|             |                         | Charged-device model (CDM), per AEC Q100-011 V CDM ESD Classification Level C6          | ±1500 | V    |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                    |                                               |                               | MIN                                 | NOM                  | MAX       | UNIT |
|--------------------|-----------------------------------------------|-------------------------------|-------------------------------------|----------------------|-----------|------|
| $V_{CC1}, V_{CC2}$ | Supply Voltage                                |                               | 2.25                                |                      | 5.5       | V    |
| $V_{CC(UVLO+)}$    | UVLO threshold when supply voltage is rising  |                               |                                     | 2                    | 2.25      | V    |
| $V_{CC(UVLO-)}$    | UVLO threshold when supply voltage is falling |                               | 1.7                                 | 1.8                  |           | V    |
| $V_{HYS(UVLO)}$    | Supply voltage UVLO hysteresis                |                               | 100                                 | 200                  |           | mV   |
| $I_{D1}, I_{D2}$   | Output switch current - Primary side          | $2.25V \leq V_{CC} \leq 2.8V$ |                                     |                      | 0.7       | A    |
| $I_{D1}, I_{D2}$   | Output switch current - Primary side          | $2.8V < V_{CC} \leq 5.5V$     |                                     |                      | 0.7       | A    |
| $I_{OH}$           | High level output current                     | $V_{CCO} = 5V$ <sup>(1)</sup> | -4                                  |                      |           | mA   |
|                    |                                               | $V_{CCO} = 3.3V$              | -2                                  |                      |           |      |
|                    |                                               | $V_{CCO} = 2.5V$              | -1                                  |                      |           |      |
| $I_{OL}$           | Low level output current                      | $V_{CCO} = 5V$                |                                     |                      | 4         | mA   |
|                    |                                               | $V_{CCO} = 3.3V$              |                                     |                      | 2         |      |
|                    |                                               | $V_{CCO} = 2.5V$              |                                     |                      | 1         |      |
| $V_{IH}$           | High level Input voltage                      |                               | $0.7 \times V_{CCI}$ <sup>(1)</sup> |                      | $V_{CCI}$ | V    |
| $V_{IL}$           | Low level Input voltage                       |                               | 0                                   | $0.3 \times V_{CCI}$ |           | V    |
| DR                 | Data Rate <sup>(2)</sup>                      |                               | 0                                   |                      | 100       | Mbps |
| $T_A$              | Ambient temperature                           |                               | -40                                 | 25                   | 125       | °C   |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

(2) 100Mbps is the maximum specified data rate, although higher data rates are possible.

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | ISO7741T-Q1 | UNIT |
|-------------------------------|----------------------------------------------|-------------|------|
|                               |                                              | DW (SOIC)   |      |
|                               |                                              | 16 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 64.0        | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 25.2        | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 33.3        | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 8.4         | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 32.7        | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | NA          | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Power Ratings

| PARAMETER          |                                        | TEST CONDITIONS                                                                                                                      | MIN | TYP | MAX | UNIT |
|--------------------|----------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| <b>ISO7741T-Q1</b> |                                        |                                                                                                                                      |     |     |     |      |
| $P_D$              | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5V$ , $T_J = 150^\circ C$ , $C_L = 15pF$ , Input a 50MHz 50% duty cycle square wave, $I_{D1}, I_{D2} = 700mA$ |     |     | 401 | mW   |
| $P_{D1}$           | Maximum power dissipation (side-1)     | $V_{CC1} = 5.5V$ , $T_J = 150^\circ C$ , $C_L = 15pF$ , Input a 50MHz 50% duty cycle square wave, $I_{D1}, I_{D2} = 700mA$           |     |     | 266 | mW   |
| $P_{D2}$           | Maximum power dissipation (side-2)     | $V_{CC2} = 5.5V$ , $T_J = 150^\circ C$ , $C_L = 15pF$ , Input a 50MHz 50% duty cycle square wave, $I_{D1}, I_{D2} = 700mA$           |     |     | 135 | mW   |
| <b>ISO7742T-Q1</b> |                                        |                                                                                                                                      |     |     |     |      |
| $P_D$              | Maximum power dissipation (both sides) | $V_{CC1} = V_{CC2} = 5.5V$ , $T_J = 150^\circ C$ , $C_L = 15pF$ , Input a 50MHz 50% duty cycle square wave, $I_{D1}, I_{D2} = 700mA$ |     |     | 411 | mW   |
| $P_{D1}$           | Maximum power dissipation (side-1)     | $V_{CC1} = 5.5V$ , $T_J = 150^\circ C$ , $C_L = 15pF$ , Input a 50MHz 50% duty cycle square wave, $I_{D1}, I_{D2} = 700mA$           |     |     | 309 | mW   |
| $P_{D2}$           | Maximum power dissipation (side-2)     | $V_{CC2} = 5.5V$ , $T_J = 150^\circ C$ , $C_L = 15pF$ , Input a 50MHz 50% duty cycle square wave, $I_{D1}, I_{D2} = 700mA$           |     |     | 102 | mW   |

## 5.6 Insulation Specifications

| PARAMETER                                        |                                                     | TEST CONDITIONS                                                                                                                                                                                                                                                                                     | VALUE             | UNIT             |
|--------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------------------|
|                                                  |                                                     |                                                                                                                                                                                                                                                                                                     | DW-16             |                  |
| CLR                                              | External clearance <sup>(1)</sup>                   | Shortest terminal-to-terminal distance through air                                                                                                                                                                                                                                                  | >8                | mm               |
| CPG                                              | External creepage <sup>(1)</sup>                    | Shortest terminal-to-terminal distance across the package surface                                                                                                                                                                                                                                   | >8                | mm               |
| DTI                                              | Distance through the insulation                     | Minimum internal gap (internal clearance)                                                                                                                                                                                                                                                           | >17               | µm               |
| CTI                                              | Comparative tracking index                          | DIN EN 60112 (VDE 0303-11); IEC 60112                                                                                                                                                                                                                                                               | >600              | V                |
|                                                  | Material group                                      | According to IEC 60664-1                                                                                                                                                                                                                                                                            | I                 |                  |
|                                                  | Overvoltage category per IEC 60664-1                | Rated mains voltage ≤ 300V <sub>RMS</sub>                                                                                                                                                                                                                                                           | I-IV              |                  |
|                                                  |                                                     | Rated mains voltage ≤ 600V <sub>RMS</sub>                                                                                                                                                                                                                                                           | I-IV              |                  |
|                                                  |                                                     | Rated mains voltage ≤ 1000V <sub>RMS</sub>                                                                                                                                                                                                                                                          | I-III             |                  |
| DIN EN IEC 60747-17 (VDE 0884-17) <sup>(2)</sup> |                                                     |                                                                                                                                                                                                                                                                                                     |                   |                  |
| V <sub>IORM</sub>                                | Maximum repetitive peak isolation voltage           | AC voltage (bipolar)                                                                                                                                                                                                                                                                                | 2121              | V <sub>PK</sub>  |
| V <sub>IOWM</sub>                                | Maximum working isolation voltage                   | AC voltage; Time dependent dielectric breakdown (TDDb) Test                                                                                                                                                                                                                                         | 1500              | V <sub>RMS</sub> |
|                                                  |                                                     | DC voltage                                                                                                                                                                                                                                                                                          | 2121              | V <sub>DC</sub>  |
| V <sub>IOTM</sub>                                | Maximum transient isolation voltage                 | V <sub>TEST</sub> = V <sub>IOTM</sub> ,<br>t = 60s (qualification);<br>V <sub>TEST</sub> = 1.2 x V <sub>IOTM</sub> ,<br>t= 1s (100% production)                                                                                                                                                     | 7071              | V <sub>PK</sub>  |
| V <sub>IMP</sub>                                 | Maximum impulse voltage <sup>(3)</sup>              | Tested in air, 1.2/50-µs waveform per IEC 62368-1                                                                                                                                                                                                                                                   | 8000              | V <sub>PK</sub>  |
| V <sub>IOSM</sub>                                | Maximum surge isolation voltage <sup>(4)</sup>      | V <sub>IOSM</sub> ≥ 1.3 x V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1                                                                                                                                                                                  | 12800             | V <sub>PK</sub>  |
| q <sub>pd</sub>                                  | Apparent charge <sup>(5)</sup>                      | Method a, After Input output safety test subgroup 2/3,<br>V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s;<br>V <sub>pd(m)</sub> = 1.2 x V <sub>IORM</sub> , t <sub>m</sub> = 10s                                                                                                     | ≤5                | pC               |
|                                                  |                                                     | Method a, After environmental tests subgroup 1,<br>V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s;<br>V <sub>pd(m)</sub> = 1.3 x V <sub>IORM</sub> , t <sub>m</sub> = 10s                                                                                                            | ≤5                |                  |
|                                                  |                                                     | Method b: At routine test (100% production);<br>V <sub>ini</sub> = 1.2 x V <sub>IOTM</sub> , t <sub>ini</sub> = 1s;<br>V <sub>pd(m)</sub> = 1.875 x V <sub>IORM</sub> , t <sub>m</sub> = 1s (method b1) or<br>V <sub>pd(m)</sub> = V <sub>ini</sub> , t <sub>m</sub> = t <sub>ini</sub> (method b2) | ≤5                |                  |
| C <sub>IO</sub>                                  | Barrier capacitance, input to output <sup>(6)</sup> | V <sub>IO</sub> = 0.4 x sin (2πft), f = 1MHz                                                                                                                                                                                                                                                        | ≅1                | pF               |
| R <sub>IO</sub>                                  | Isolation resistance <sup>(6)</sup>                 | V <sub>IO</sub> = 500V, T <sub>A</sub> = 25°C                                                                                                                                                                                                                                                       | >10 <sup>12</sup> | Ω                |
|                                                  |                                                     | V <sub>IO</sub> = 500V, 100°C ≤ T <sub>A</sub> ≤ 125°C                                                                                                                                                                                                                                              | >10 <sup>11</sup> |                  |
|                                                  |                                                     | V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C                                                                                                                                                                                                                                                    | >10 <sup>9</sup>  |                  |
|                                                  | Pollution degree                                    |                                                                                                                                                                                                                                                                                                     | 2                 |                  |
|                                                  | Climatic category                                   |                                                                                                                                                                                                                                                                                                     | 55/125/21         |                  |
| UL 1577                                          |                                                     |                                                                                                                                                                                                                                                                                                     |                   |                  |
| V <sub>ISO</sub>                                 | Maximum withstanding isolation voltage              | V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60s (qualification),<br>V <sub>TEST</sub> = 1.2 x V <sub>ISO</sub> , t = 1s (100% production)                                                                                                                                                            | 5000              | V <sub>RMS</sub> |

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-terminal device.

## 5.7 Safety-Related Certifications

| VDE                                                            | CSA                                                      | UL                                                                 | CQC                                    | TUV                                                    |
|----------------------------------------------------------------|----------------------------------------------------------|--------------------------------------------------------------------|----------------------------------------|--------------------------------------------------------|
| Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17) | Plan to certify according to IEC 62368-1 and IEC 60601-1 | Plan to certify according to UL 1577 Component Recognition Program | Plan to certify according to GB 4943.1 | Plan to certify according to EN 61010-1 and EN 62368-1 |
| Certificate planned                                            | Certificate planned                                      | Certificate planned                                                | Certificate planned                    | Certificate planned                                    |

## 5.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER            |                                         | TEST CONDITIONS                                                                                                                                         | MIN | TYP | MAX  | UNIT |
|----------------------|-----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| <b>DW-16 PACKAGE</b> |                                         |                                                                                                                                                         |     |     |      |      |
| I <sub>S</sub>       | Safety input, output, or supply current | R <sub>θJA</sub> = 64°C/W, V <sub>I</sub> = 5.5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, I <sub>L</sub> = 700mA see <a href="#">Figure 5-1</a>  |     |     | 319  | mA   |
|                      |                                         | R <sub>θJA</sub> = 64°C/W, V <sub>I</sub> = 3.6V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, I <sub>L</sub> = 700mA see <a href="#">Figure 5-1</a>  |     |     | 480  |      |
|                      |                                         | R <sub>θJA</sub> = 64°C/W, V <sub>I</sub> = 2.75V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, I <sub>L</sub> = 700mA see <a href="#">Figure 5-1</a> |     |     | 630  |      |
| P <sub>S</sub>       | Safety input, output, or total power    | R <sub>θJA</sub> = 64°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C see <a href="#">Figure 5-2</a>                                                 |     |     | 1953 | mW   |
| T <sub>S</sub>       | Maximum safety temperature              |                                                                                                                                                         |     |     | 150  | °C   |

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> must not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.  
 The junction-to-air thermal resistance, R<sub>θJA</sub>, is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:  
 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.  
 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum allowed junction temperature.  
 $P_S = I_S \times V_I$ , where V<sub>I</sub> is the maximum input voltage.

## 5.9 Electrical Characteristics Transformer

over full-range of recommended operating conditions, unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .

| PARAMETER                |                                                                     | TEST CONDITIONS                                             | MIN  | TYP  | MAX                    | UNIT             |
|--------------------------|---------------------------------------------------------------------|-------------------------------------------------------------|------|------|------------------------|------------------|
| <b>CLK</b>               |                                                                     |                                                             |      |      |                        |                  |
| $F_{SW}$                 | D1, D2 average switching Frequency (ISO774xTA-Q1)                   | $R_L = 50\Omega$ to $V_{CC1}$                               | 138  | 160  | 203                    | kHz              |
|                          | D1, D2 average switching Frequency (ISO774xTB-Q1)                   | $R_L = 50\Omega$ to $V_{CC1}$                               | 363  | 424  | 517                    | kHz              |
| <b>OUTPUT STAGE</b>      |                                                                     |                                                             |      |      |                        |                  |
| DMM                      | Average ON time mismatch between D1 and D2                          | $R_L = 50\Omega$                                            | 0%   |      |                        |                  |
| $R_{(ON)}$               | Output switch on resistance                                         | $V_{CC} = 4.5\text{V}$ , $I_{D1}$ , $I_{D2} = 700\text{mA}$ | 0.22 | 0.4  | $\Omega$               |                  |
|                          |                                                                     | $V_{CC} = 2.8\text{V}$ , $I_{D1}$ , $I_{D2} = 700\text{mA}$ | 0.24 | 0.45 | $\Omega$               |                  |
|                          |                                                                     | $V_{CC} = 2.25\text{V}$ , $I_{D1}$ , $I_{D2} = 0.5\text{A}$ | 0.26 | 0.5  | $\Omega$               |                  |
| $V_{(SLEW)}$             | Voltage slew rates on D1 and D2 for ISO774xTA-Q1                    | $R_L = 50\Omega$ to $V_{CC1}$                               | 48   |      | $\text{V}/\mu\text{s}$ |                  |
| $I_{(SLEW)}$             | Current slew rates at D1 and D2 for ISO774xTA-Q1                    | $R_L = 5\Omega$ through transformer                         | 11   |      | $\text{A}/\mu\text{s}$ |                  |
| $V_{(SLEWHF)}$           | Voltage slew rates on D1 and D2 for ISO774xTB-Q1                    | $R_L = 50\Omega$ to $V_{CC1}$                               | 152  |      | $\text{V}/\mu\text{s}$ |                  |
| $I_{(SLEWHF)}$           | Current slew rates at D1 and D2 for ISO774xTB-Q1                    | $R_L = 5\Omega$ through transformer                         | 41   |      | $\text{A}/\mu\text{s}$ |                  |
| $I_{LIM}$                | Current clamp limit ( $2.8\text{V} < V_{CC} \leq 5.5\text{V}$ )     |                                                             | 1.42 | 1.75 | 2.15                   | A                |
|                          | Current clamp limit ( $2.25\text{V} \leq V_{CC} \leq 2.8\text{V}$ ) |                                                             | 0.65 |      | 1.85                   | A                |
| <b>THERMAL SHUT DOWN</b> |                                                                     |                                                             |      |      |                        |                  |
| $T_{SD+}$                | $T_{SD}$ turn on temperature                                        |                                                             | 154  | 168  | 181                    | $^\circ\text{C}$ |
| $T_{SD-}$                | $T_{SD}$ turn off temperature                                       |                                                             | 135  | 150  | 166                    | $^\circ\text{C}$ |
| $T_{SD-}$                | $T_{SD}$ hysteresis                                                 |                                                             | 13   | 17   | $^\circ\text{C}$       |                  |

## 5.10 Electrical Characteristics—5V Supply

$V_{CC1} = V_{CC2} = 5V \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER           |                                    | TEST CONDITIONS                                                          | MIN                            | TYP                  | MAX                  | UNIT        |
|---------------------|------------------------------------|--------------------------------------------------------------------------|--------------------------------|----------------------|----------------------|-------------|
| $V_{OH}$            | High-level output voltage          | $I_{OH} = -4mA$                                                          | $V_{CCO} - 0.4$ <sup>(1)</sup> | 4.8                  |                      | V           |
| $V_{OL}$            | Low-level output voltage           | $I_{OL} = 4mA$                                                           |                                | 0.2                  | 0.4                  | V           |
| $V_{IT+(IN)}$       | Rising input switching threshold   |                                                                          |                                | $0.6 \times V_{CCI}$ | $0.7 \times V_{CCI}$ | V           |
| $V_{IT-(IN)}$       | Falling input switching threshold  |                                                                          | $0.3 \times V_{CCI}$           | $0.4 \times V_{CCI}$ |                      | V           |
| $V_{I(HYS)}$        | Input threshold voltage hysteresis |                                                                          | $0.1 \times V_{CCI}$           | $0.2 \times V_{CCI}$ |                      | V           |
| $I_{IH}$            | High-level input current           | $V_{IH} = V_{CCI}$ <sup>(1)</sup> at INx                                 |                                |                      | 10                   | $\mu A$     |
| $I_{IL}$            | Low-level input current            | $V_{IL} = 0V$ at INx                                                     | -10                            |                      |                      | $\mu A$     |
| CMTI <sup>(3)</sup> | Common mode transient immunity     | $V_I = V_{CCI}$ or 0V, $V_{CM} = 1200V$                                  | 100                            | 150                  |                      | kV/ $\mu s$ |
| $C_I$               | Input Capacitance <sup>(2)</sup>   | $V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 1MHz$ , $V_{CC} = 5V$ |                                | 2                    |                      | pF          |

- (1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$   
(2) Measured from input pin to same side ground.  
(3) CMTI is measured only on digital isolator independent of transformer driver

## 5.11 Supply Current Characteristics—5V Supply

$V_{CC1} = V_{CC2} = 5V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC1}$ , (over recommended operating conditions unless otherwise noted)

| PARAMETER                                                             | TEST CONDITIONS                                                            |                            | SUPPLY CURRENT                                                      | MIN | TYP              | MAX  | UNIT |     |    |    |
|-----------------------------------------------------------------------|----------------------------------------------------------------------------|----------------------------|---------------------------------------------------------------------|-----|------------------|------|------|-----|----|----|
| ISO7741TA-Q1                                                          |                                                                            |                            |                                                                     |     |                  |      |      |     |    |    |
| Supply current - DC signal                                            | $V_I = V_{CCI}$ (ISO7741T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7741FT)        |                            | I <sub>CC1</sub>                                                    |     | 3                | 4.2  | mA   |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 2.4              | 3.7  |      |     |    |    |
|                                                                       | $V_I = 0V_I$ (ISO7741T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7741FT)      |                            | I <sub>CC1</sub>                                                    |     | 6.3              | 7.8  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 3.6              | 5.1  |      |     |    |    |
| Supply current - AC signal                                            | All channels switching with square wave clock input; C <sub>L</sub> = 15pF | 1Mbps                      | I <sub>CC1</sub>                                                    |     | 4.7              | 6.1  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 3.2              | 4.6  |      |     |    |    |
|                                                                       |                                                                            | 10Mbps                     | I <sub>CC1</sub>                                                    |     | 5.4              | 6.8  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 4.8              | 6.5  |      |     |    |    |
|                                                                       |                                                                            | 100Mbps                    | I <sub>CC1</sub>                                                    |     | 11.5             | 13.7 |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 20               | 23.5 |      |     |    |    |
|                                                                       |                                                                            | ISO7741TB-Q1               |                                                                     |     |                  |      |      |     |    |    |
|                                                                       |                                                                            | Supply current - DC signal | $V_I = V_{CCI}$ (ISO7741T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7741FT) |     | I <sub>CC1</sub> |      |      | 3.6 | 5  | mA |
| I <sub>CC2</sub>                                                      |                                                                            |                            |                                                                     |     | 2.4              | 3.7  |      |     |    |    |
| $V_I = 0V_I$ (ISO7741T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7741FT) |                                                                            |                            | I <sub>CC1</sub>                                                    |     | 6.9              | 8.6  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 3.6              | 5.1  |      |     |    |    |
| Supply current - AC signal                                            | All channels switching with square wave clock input; C <sub>L</sub> = 15pF | 1Mbps                      | I <sub>CC1</sub>                                                    |     | 5.3              | 6.9  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 3.2              | 4.6  |      |     |    |    |
|                                                                       |                                                                            | 10Mbps                     | I <sub>CC1</sub>                                                    |     | 5.9              | 7.7  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 4.8              | 6.5  |      |     |    |    |
|                                                                       |                                                                            | 100Mbps                    | I <sub>CC1</sub>                                                    |     | 12.1             | 14.6 |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 20               | 23.5 |      |     |    |    |
|                                                                       |                                                                            | ISO7742TA-Q1               |                                                                     |     |                  |      |      |     |    |    |
|                                                                       |                                                                            | Supply current - DC signal | $V_I = V_{CCI}$ (ISO7742T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7742FT) |     | I <sub>CC1</sub> |      | 3.3  | 4.8 | mA |    |
| I <sub>CC2</sub>                                                      |                                                                            |                            |                                                                     |     | 2.4              | 3.5  |      |     |    |    |
| $V_I = 0V_I$ (ISO7742T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7742FT) |                                                                            |                            | I <sub>CC1</sub>                                                    |     | 5.6              | 7.3  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 4.7              | 6    |      |     |    |    |
| Supply current - AC signal                                            | All channels switching with square wave clock input; C <sub>L</sub> = 15pF | 1Mbps                      | I <sub>CC1</sub>                                                    |     | 4.6              | 6.2  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 3.6              | 4.9  |      |     |    |    |
|                                                                       |                                                                            | 10Mbps                     | I <sub>CC1</sub>                                                    |     | 5.7              | 7.4  |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 4.7              | 6.1  |      |     |    |    |
|                                                                       |                                                                            | 100Mbps                    | I <sub>CC1</sub>                                                    |     | 16.6             | 19.6 |      |     |    |    |
|                                                                       |                                                                            |                            | I <sub>CC2</sub>                                                    |     | 15.7             | 18.4 |      |     |    |    |

$V_{CC1} = V_{CC2} = 5V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC1}$ , (over recommended operating conditions unless otherwise noted)

| PARAMETER                  | TEST CONDITIONS                                                       | SUPPLY CURRENT | MIN       | TYP  | MAX  | UNIT |
|----------------------------|-----------------------------------------------------------------------|----------------|-----------|------|------|------|
| <b>ISO7742TB-Q1</b>        |                                                                       |                |           |      |      |      |
| Supply current - DC signal | $V_I = V_{CCI}$ (ISO7742T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7742FT)   | $I_{CC1}$      |           | 3.9  | 5.6  | mA   |
|                            |                                                                       | $I_{CC2}$      |           | 2.4  | 3.5  |      |
|                            | $V_I = 0V_I$ (ISO7742T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7742FT) | $I_{CC1}$      |           | 6.2  | 8.2  |      |
|                            |                                                                       | $I_{CC2}$      |           | 4.7  | 6    |      |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps          | $I_{CC1}$ | 5.2  | 7    |      |
|                            |                                                                       |                | $I_{CC2}$ | 3.6  | 4.9  |      |
|                            |                                                                       | 10Mbps         | $I_{CC1}$ | 6.2  | 8.3  |      |
|                            |                                                                       |                | $I_{CC2}$ | 4.7  | 6.1  |      |
|                            |                                                                       | 100Mbps        | $I_{CC1}$ | 17.3 | 20.5 |      |
|                            |                                                                       |                | $I_{CC2}$ | 15.7 | 18.4 |      |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$

## 5.12 Electrical Characteristics—3.3V Supply

$V_{CC1} = V_{CC2} = 3.3V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC1}$ , (over recommended operating conditions unless otherwise noted)

| PARAMETER           | TEST CONDITIONS                                                           | MIN                            | TYP                  | MAX                                 | UNIT        |
|---------------------|---------------------------------------------------------------------------|--------------------------------|----------------------|-------------------------------------|-------------|
| $V_{OH}$            | High-level output voltage<br>$I_{OH} = -2mA$                              | $V_{CCO} - 0.3$ <sup>(1)</sup> | 3.2                  |                                     | V           |
| $V_{OL}$            | Low-level output voltage<br>$I_{OL} = 2mA$                                |                                | 0.1                  | 0.3                                 | V           |
| $V_{IT+(IN)}$       | Rising input switching threshold                                          |                                | $0.6 \times V_{CCI}$ | $0.7 \times V_{CCI}$ <sup>(1)</sup> | V           |
| $V_{IT-(IN)}$       | Falling input switching threshold                                         | $0.3 \times V_{CCI}$           | $0.4 \times V_{CCI}$ |                                     | V           |
| $V_{I(HYS)}$        | Input threshold voltage hysteresis                                        | $0.1 \times V_{CCI}$           | $0.2 \times V_{CCI}$ |                                     | V           |
| $I_{IH}$            | High-level input current<br>$V_{IH} = V_{CCI}$ <sup>(1)</sup> at INx      |                                |                      | 10                                  | $\mu A$     |
| $I_{IL}$            | Low-level input current<br>$V_{IL} = 0V$ at INx                           | -10                            |                      |                                     | $\mu A$     |
| CMTI <sup>(2)</sup> | Common mode transient immunity<br>$V_I = V_{CCI}$ or 0V, $V_{CM} = 1200V$ | 100                            | 150                  |                                     | kV/ $\mu s$ |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$

(2) CMTI is measured only on digital isolator independent of transformer driver

### 5.13 Supply Current Characteristics—3.3V Supply

$V_{CC1} = V_{CC2} = 3.3V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC1}$ , (over recommended operating conditions unless otherwise noted)

| PARAMETER                  | TEST CONDITIONS                                                       |         | SUPPLY CURRENT | MIN | TYP  | MAX  | UNIT |
|----------------------------|-----------------------------------------------------------------------|---------|----------------|-----|------|------|------|
| ISO7741TA-Q1               |                                                                       |         |                |     |      |      |      |
| Supply current - DC signal | $V_I = V_{CCI}$ (ISO7741T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7741FT)   |         | $I_{CC1}$      |     | 2.8  | 3.9  | mA   |
|                            |                                                                       |         | $I_{CC2}$      |     | 2.3  | 3.7  |      |
|                            | $V_I = 0V_I$ (ISO7741T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7741FT) |         | $I_{CC1}$      |     | 6.1  | 7.5  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 3.6  | 5.1  |      |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps   | $I_{CC1}$      |     | 4.5  | 5.7  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 3.1  | 4.5  |      |
|                            |                                                                       | 10Mbps  | $I_{CC1}$      |     | 4.9  | 6.3  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 4.2  | 5.9  |      |
|                            |                                                                       | 100Mbps | $I_{CC1}$      |     | 9.2  | 11.1 |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 15.1 | 18.2 |      |
| ISO7741TB-Q1               |                                                                       |         |                |     |      |      |      |
| Supply current - DC signal | $V_I = V_{CCI}$ (ISO7741T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7741FT)   |         | $I_{CC1}$      |     | 3.1  | 4.4  | mA   |
|                            |                                                                       |         | $I_{CC2}$      |     | 2.3  | 3.7  |      |
|                            | $V_I = 0V_I$ (ISO7741T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7741FT) |         | $I_{CC1}$      |     | 6.5  | 8    |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 3.6  | 5.1  |      |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps   | $I_{CC1}$      |     | 4.9  | 6.3  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 3.1  | 4.5  |      |
|                            |                                                                       | 10Mbps  | $I_{CC1}$      |     | 5.3  | 6.9  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 4.2  | 5.9  |      |
|                            |                                                                       | 100Mbps | $I_{CC1}$      |     | 9.6  | 11.7 |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 15.1 | 18.2 |      |
| ISO7742TA-Q1               |                                                                       |         |                |     |      |      |      |
| Supply current - DC signal | $V_I = V_{CCI}$ (ISO7742T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7742FT)   |         | $I_{CC1}$      |     | 3.2  | 4.5  | mA   |
|                            |                                                                       |         | $I_{CC2}$      |     | 2.4  | 3.4  |      |
|                            | $V_I = 0V_I$ (ISO7742T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7742FT) |         | $I_{CC1}$      |     | 5.4  | 7    |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 4.6  | 6    |      |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps   | $I_{CC1}$      |     | 4.4  | 5.9  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 3.6  | 4.8  |      |
|                            |                                                                       | 10Mbps  | $I_{CC1}$      |     | 5.1  | 6.7  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 4.3  | 5.6  |      |
|                            |                                                                       | 100Mbps | $I_{CC1}$      |     | 12.8 | 15.6 |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 12   | 14.4 |      |

$V_{CC1} = V_{CC2} = 3.3V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC1}$ , (over recommended operating conditions unless otherwise noted)

| PARAMETER                  | TEST CONDITIONS                                                       |         | SUPPLY CURRENT | MIN | TYP  | MAX  | UNIT |
|----------------------------|-----------------------------------------------------------------------|---------|----------------|-----|------|------|------|
| ISO7742TB-Q1               |                                                                       |         |                |     |      |      |      |
| Supply current - DC signal | $V_I = V_{CCI}$ (ISO7742T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7742FT)   |         | $I_{CC1}$      |     | 3.5  | 5    | mA   |
|                            |                                                                       |         | $I_{CC2}$      |     | 2.4  | 3.4  |      |
|                            | $V_I = 0V_I$ (ISO7742T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7742FT) |         | $I_{CC1}$      |     | 5.8  | 7.6  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 4.6  | 6    |      |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps   | $I_{CC1}$      |     | 4.7  | 6.4  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 3.6  | 4.8  |      |
|                            |                                                                       | 10Mbps  | $I_{CC1}$      |     | 5.5  | 7.3  |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 4.3  | 5.6  |      |
|                            |                                                                       | 100Mbps | $I_{CC1}$      |     | 13.2 | 16   |      |
|                            |                                                                       |         | $I_{CC2}$      |     | 12   | 14.4 |      |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$

## 5.14 Electrical Characteristics—2.5V Supply

$V_{CC1} = V_{CC2} = 2.5V \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER           | TEST CONDITIONS                    |                                            | MIN                            | TYP                  | MAX                  | UNIT        |
|---------------------|------------------------------------|--------------------------------------------|--------------------------------|----------------------|----------------------|-------------|
| $V_{OH}$            | High-level output voltage          | $I_{OH} = -1mA$                            | $V_{CCO} - 0.2$ <sup>(1)</sup> | 2.45                 |                      | V           |
| $V_{OL}$            | Low-level output voltage           | $I_{OL} = 1mA$                             |                                | 0.05                 | 0.2                  | V           |
| $V_{IT+(IN)}$       | Rising input switching threshold   |                                            |                                | $0.6 \times V_{CCI}$ | $0.7 \times V_{CCI}$ | V           |
| $V_{IT-(IN)}$       | Falling input switching threshold  |                                            | $0.3 \times V_{CCI}$           | $0.4 \times V_{CCI}$ |                      | V           |
| $V_{I(HYS)}$        | Input threshold voltage hysteresis |                                            | $0.1 \times V_{CCI}$           | $0.2 \times V_{CCI}$ |                      | V           |
| $I_{IH}$            | High-level input current           | $V_{IH} = V_{CCI}$ <sup>(1)</sup> at INx   |                                |                      | 10                   | $\mu A$     |
| $I_{IL}$            | Low-level input current            | $V_{IL} = 0V$ at INx                       | -10                            |                      |                      | $\mu A$     |
| CMTI <sup>(2)</sup> | Common mode transient immunity     | $V_I = V_{CCI}$ or $0V$ , $V_{CM} = 1200V$ | 100                            | 150                  |                      | kV/ $\mu s$ |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$

(2) CMTI is measured only on digital isolator independent of transformer driver

## 5.15 Supply Current Characteristics—2.5V Supply

$V_{CC1} = V_{CC2} = 2.5V \pm 10\%$ ,  $R_L = 50 \Omega$  to  $V_{CC1}$ , (over recommended operating conditions unless otherwise noted)

| PARAMETER                                                             | TEST CONDITIONS                                                       |                            | SUPPLY CURRENT                                                      | MIN | TYP       | MAX  | UNIT |     |     |    |
|-----------------------------------------------------------------------|-----------------------------------------------------------------------|----------------------------|---------------------------------------------------------------------|-----|-----------|------|------|-----|-----|----|
| ISO7741TA-Q1                                                          |                                                                       |                            |                                                                     |     |           |      |      |     |     |    |
| Supply current - DC signal                                            | $V_I = V_{CCI}$ (ISO7741T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7741FT)   |                            | $I_{CC1}$                                                           |     | 2.7       | 3.7  | mA   |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 2.3       | 3.7  |      |     |     |    |
|                                                                       | $V_I = 0V_I$ (ISO7741T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7741FT) |                            | $I_{CC1}$                                                           |     | 6         | 7.3  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 3.6       | 5.1  |      |     |     |    |
| Supply current - AC signal                                            | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps                      | $I_{CC1}$                                                           |     | 4.4       | 5.6  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 3         | 4.5  |      |     |     |    |
|                                                                       |                                                                       | 10Mbps                     | $I_{CC1}$                                                           |     | 4.7       | 6.1  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 3.9       | 5.5  |      |     |     |    |
|                                                                       |                                                                       | 100Mbps                    | $I_{CC1}$                                                           |     | 8         | 9.7  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 12.1      | 14.7 |      |     |     |    |
|                                                                       |                                                                       | ISO7741TB-Q1               |                                                                     |     |           |      |      |     |     |    |
|                                                                       |                                                                       | Supply current - DC signal | $V_I = V_{CCI}$ (ISO7741T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7741FT) |     | $I_{CC1}$ |      |      | 3   | 4.2 | mA |
| $I_{CC2}$                                                             |                                                                       |                            |                                                                     |     | 2.3       | 3.7  |      |     |     |    |
| $V_I = 0V_I$ (ISO7741T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7741FT) |                                                                       |                            | $I_{CC1}$                                                           |     | 6.3       | 7.8  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 3.6       | 5.1  |      |     |     |    |
| Supply current - AC signal                                            | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps                      | $I_{CC1}$                                                           |     | 4.7       | 6    |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 3         | 4.5  |      |     |     |    |
|                                                                       |                                                                       | 10Mbps                     | $I_{CC1}$                                                           |     | 5         | 6.5  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 3.9       | 5.5  |      |     |     |    |
|                                                                       |                                                                       | 100Mbps                    | $I_{CC1}$                                                           |     | 8.3       | 10.1 |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 12.1      | 14.7 |      |     |     |    |
|                                                                       |                                                                       | ISO7742TA-Q1               |                                                                     |     |           |      |      |     |     |    |
|                                                                       |                                                                       | Supply current - DC signal | $V_I = V_{CCI}$ (ISO7742T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7742FT) |     | $I_{CC1}$ |      | 3.1  | 4.3 | mA  |    |
| $I_{CC2}$                                                             |                                                                       |                            |                                                                     |     | 2.3       | 3.4  |      |     |     |    |
| $V_I = 0V_I$ (ISO7742T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7742FT) |                                                                       |                            | $I_{CC1}$                                                           |     | 5.3       | 6.9  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 4.6       | 5.9  |      |     |     |    |
| Supply current - AC signal                                            | All channels switching with square wave clock input; $C_L = 15pF$     | 1Mbps                      | $I_{CC1}$                                                           |     | 4.3       | 5.7  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 3.5       | 4.7  |      |     |     |    |
|                                                                       |                                                                       | 10Mbps                     | $I_{CC1}$                                                           |     | 4.8       | 6.4  |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 4.1       | 5.4  |      |     |     |    |
|                                                                       |                                                                       | 100Mbps                    | $I_{CC1}$                                                           |     | 10.6      | 13   |      |     |     |    |
|                                                                       |                                                                       |                            | $I_{CC2}$                                                           |     | 9.9       | 12   |      |     |     |    |

$V_{CC1} = V_{CC2} = 2.5V \pm 10\%$ ,  $R_L = 50 \Omega$  to  $V_{CC1}$ , (over recommended operating conditions unless otherwise noted)

| PARAMETER                  | TEST CONDITIONS                                                     | SUPPLY CURRENT | MIN       | TYP  | MAX  | UNIT |
|----------------------------|---------------------------------------------------------------------|----------------|-----------|------|------|------|
| <b>ISO7742TB-Q1</b>        |                                                                     |                |           |      |      |      |
| Supply current - DC signal | $V_I = V_{CCI}$ (ISO7742T) <sup>(1)</sup><br>$V_I = 0V$ (ISO7742FT) | $I_{CC1}$      |           | 3.4  | 4.8  | mA   |
|                            |                                                                     | $I_{CC2}$      |           | 2.3  | 3.4  |      |
|                            | $V_I = 0V$ (ISO7742T) <sup>(1)</sup><br>$V_I = V_{CCI}$ (ISO7742FT) | $I_{CC1}$      |           | 5.6  | 7.3  |      |
|                            |                                                                     | $I_{CC2}$      |           | 4.6  | 5.9  |      |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15pF$   | 1Mbps          | $I_{CC1}$ | 4.5  | 6.1  |      |
|                            |                                                                     |                | $I_{CC2}$ | 3.5  | 4.7  |      |
|                            |                                                                     | 10Mbps         | $I_{CC1}$ | 5.1  | 6.8  |      |
|                            |                                                                     |                | $I_{CC2}$ | 4.1  | 5.4  |      |
|                            |                                                                     | 100Mbps        | $I_{CC1}$ | 10.9 | 13.4 |      |
|                            |                                                                     |                | $I_{CC2}$ | 9.9  | 12   |      |

(1)  $V_{CCI}$  = Input-side  $V_{CC}$

## 5.16 Switching Characteristics—5V Supply

$V_{CC1} = V_{CC2} = 5V \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER                           |                                                                            | TEST CONDITIONS                                                                                                           | MIN | TYP  | MAX | UNIT |
|-------------------------------------|----------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay time                                                     |                                                                                                                           | 6   | 10.7 | 17  | ns   |
| PWD                                 | Pulse width distortion <sup>(1)</sup>  t <sub>PHL</sub> – t <sub>PLH</sub> |                                                                                                                           | 0   | 6.2  | ns  |      |
| t <sub>sk(o)</sub>                  | Channel-to-channel output skew time <sup>(2)</sup>                         | Same-direction channels                                                                                                   |     |      | 4   | ns   |
| t <sub>sk(pp)</sub>                 | Part-to-part skew time <sup>(3)</sup>                                      |                                                                                                                           |     |      | 4.4 | ns   |
| t <sub>r</sub>                      | Output signal rise time                                                    |                                                                                                                           |     | 2.4  | 3.9 | ns   |
| t <sub>f</sub>                      | Output signal fall time                                                    |                                                                                                                           |     | 2.4  | 3.9 | ns   |
| t <sub>DO</sub>                     | Default output delay time from input power loss                            | Measured from the time V <sub>CC</sub> goes below 1.7V                                                                    |     | 0.1  | 0.3 | μs   |
| t <sub>ie</sub>                     | Time interval error                                                        | 2 <sup>16</sup> – 1 PRBS data at 100Mbps                                                                                  |     | 0.8  |     | ns   |
| t <sub>BBM</sub>                    | Break-before-make time (ISO774xTA-Q1)                                      | Measured as voltage with R <sub>L</sub> = 50Ω to V <sub>CC</sub>                                                          |     | 115  |     | ns   |
| t <sub>BBM</sub>                    | Break-before-make time (ISO774xTB-Q1)                                      | Measured as voltage with R <sub>L</sub> = 50Ω to V <sub>CC</sub>                                                          |     | 90   |     | ns   |
| t <sub>SS</sub>                     | Soft-start time (ISO774xTA-Q1)                                             | 10% to 90% transition time on V <sub>OUT</sub><br>With transformer C <sub>LOAD</sub> = 40μF<br>R <sub>L</sub> = 5Ω        | 1   | 2.2  | 8   | ms   |
| t <sub>SS</sub>                     | Soft-start time (ISO774xTB-Q1)                                             | 10% to 90% transition time on V <sub>OUT</sub><br>With transformer C <sub>LOAD</sub> = 40μF<br>R <sub>L</sub> = 5Ω        | 1   | 4.25 | 8   | ms   |
| t <sub>SSdelay</sub>                | Soft-start time delay                                                      | From power up to 90% transition time on V <sub>OUT</sub> With transformer C <sub>LOAD</sub> = 40μF<br>R <sub>L</sub> = 5Ω | 3.5 | 8.5  | 18  | ms   |

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.17 Switching Characteristics—3.3V Supply

$V_{CC1} = V_{CC2} = 3.3V \pm 10\%$  (over recommended operating conditions unless otherwise noted)

| PARAMETER          |                                                             | TEST CONDITIONS                                                                                            | MIN | TYP  | MAX  | UNIT    |
|--------------------|-------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----|------|------|---------|
| $t_{PLH}, t_{PHL}$ | Propagation delay time                                      |                                                                                                            | 6   | 12   | 18.5 | ns      |
| PWD                | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |                                                                                                            |     | 0.1  | 6.2  | ns      |
| $t_{sk(o)}$        | Channel-to-channel output skew time <sup>(2)</sup>          | Same-direction channels                                                                                    |     |      | 4.4  | ns      |
| $t_{sk(pp)}$       | Part-to-part skew time <sup>(3)</sup>                       |                                                                                                            |     |      | 5    | ns      |
| $t_r$              | Output signal rise time                                     |                                                                                                            |     | 1.3  | 3    | ns      |
| $t_f$              | Output signal fall time                                     |                                                                                                            |     | 1.3  | 3    | ns      |
| $t_{DO}$           | Default output delay time from input power loss             | Measured from the time $V_{CC}$ goes below 1.7V                                                            |     | 0.1  | 0.3  | $\mu s$ |
| $t_{ie}$           | Time interval error                                         | $2^{16} - 1$ PRBS data at 100Mbps                                                                          |     | 0.9  |      | ns      |
| $t_{BBM}$          | Break-before-make time (ISO774xTA-Q1)                       | Measured as voltage with $R_L = 50\Omega$ to $V_{CC}$                                                      |     | 115  |      | ns      |
| $t_{BBM}$          | Break-before-make time (ISO774xTB-Q1)                       | Measured as voltage with $R_L = 50\Omega$ to $V_{CC}$                                                      |     | 90   |      | ns      |
| $t_{SS}$           | Soft-start time (ISO774xTA-Q1)                              | 10% to 90% transition time on $V_{OUT}$<br>With transformer $C_{LOAD} = 40\mu F$<br>$R_L = 5\Omega$        | 1   | 2.2  | 8    | ms      |
| $t_{SS}$           | Soft-start time (ISO774xTB-Q1)                              | 10% to 90% transition time on $V_{OUT}$<br>With transformer $C_{LOAD} = 40\mu F$<br>$R_L = 5\Omega$        | 1   | 4.25 | 8    | ms      |
| $t_{SSdelay}$      | Soft-start time delay                                       | From power up to 90% transition time on $V_{OUT}$ With transformer $C_{LOAD} = 40\mu F$<br>$R_L = 5\Omega$ | 3.5 | 8.5  | 18   | ms      |

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.18 Switching Characteristics—2.5V Supply

$V_{CC1} = V_{CC2} = 2.5V \pm 10\%$  (over recommended operating conditions unless otherwise noted)

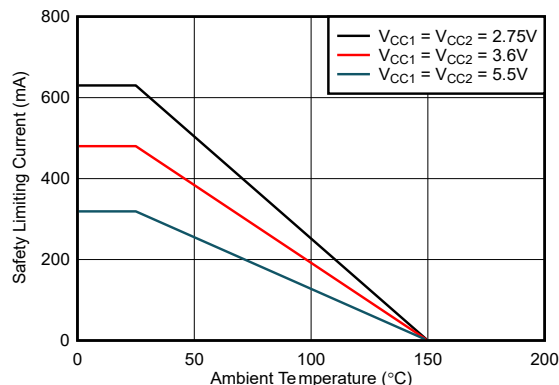
| PARAMETER          |                                                             | TEST CONDITIONS                                                                                            | MIN | TYP  | MAX | UNIT    |
|--------------------|-------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----|------|-----|---------|
| $t_{PLH}, t_{PHL}$ | Propagation delay time                                      |                                                                                                            | 7.5 | 13   | 21  | ns      |
| PWD                | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $ |                                                                                                            |     | 0.2  | 6.2 | ns      |
| $t_{sk(o)}$        | Channel-to-channel output skew time <sup>(2)</sup>          | Same-direction channels                                                                                    |     |      | 4.4 | ns      |
| $t_{sk(pp)}$       | Part-to-part skew time <sup>(3)</sup>                       |                                                                                                            |     |      | 5.3 | ns      |
| $t_r$              | Output signal rise time                                     |                                                                                                            |     | 1    | 3.5 | ns      |
| $t_f$              | Output signal fall time                                     |                                                                                                            |     | 1    | 3.5 | ns      |
| $t_{DO}$           | Default output delay time from input power loss             | Measured from the time $V_{CC}$ goes below 1.7V                                                            |     | 0.1  | 0.3 | $\mu s$ |
| $t_{ie}$           | Time interval error                                         | $2^{16} - 1$ PRBS data at 100Mbps                                                                          |     | 0.7  |     | ns      |
| $t_{BBM}$          | Break-before-make time (ISO774xTA-Q1)                       | Measured as voltage with $R_L = 50\Omega$ to $V_{CC}$                                                      |     | 115  |     | ns      |
| $t_{BBM}$          | Break-before-make time (ISO774xTB-Q1)                       | Measured as voltage with $R_L = 50\Omega$ to $V_{CC}$                                                      |     | 90   |     | ns      |
| $t_{SS}$           | Soft-start time (ISO774xTA-Q1)                              | 10% to 90% transition time on $V_{OUT}$<br>With transformer $C_{LOAD} = 40\mu F$<br>$R_L = 5\Omega$        | 1   | 2.2  | 8   | ms      |
| $t_{SS}$           | Soft-start time (ISO774xTB-Q1)                              | 10% to 90% transition time on $V_{OUT}$<br>With transformer $C_{LOAD} = 40\mu F$<br>$R_L = 5\Omega$        | 1   | 4.25 | 8   | ms      |
| $t_{SSdelay}$      | Soft-start time delay                                       | From power up to 90% transition time on $V_{OUT}$ With transformer $C_{LOAD} = 40\mu F$<br>$R_L = 5\Omega$ | 3.5 | 8.5  | 18  | ms      |

(1) Also known as pulse skew.

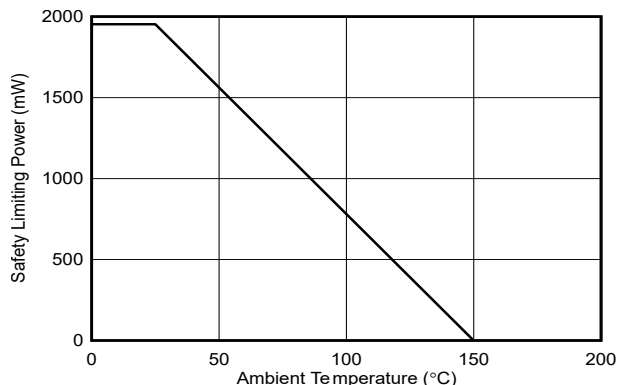
(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.19 Insulation Characteristics Curves

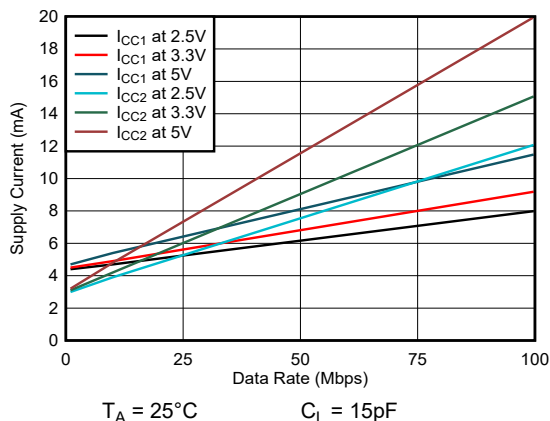


**Figure 5-1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package**

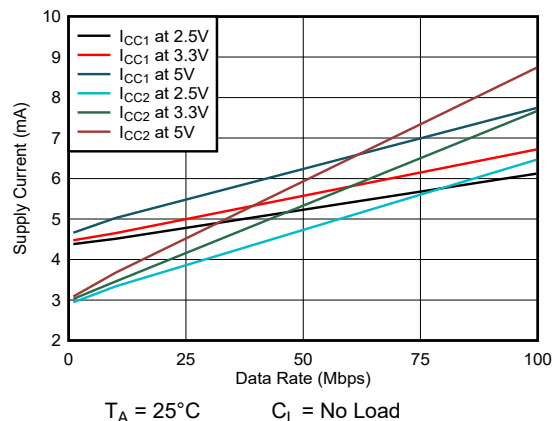


**Figure 5-2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package**

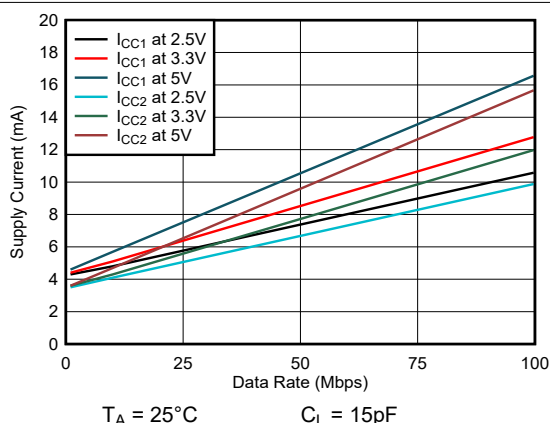
## 5.20 Typical Characteristics



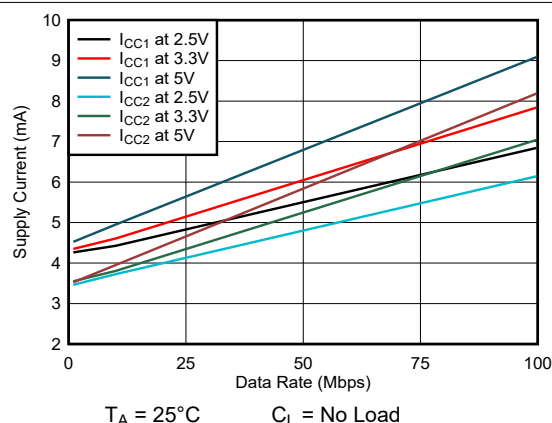
**Figure 5-3. ISO7741Tx-Q1 Supply Current vs. Data Rate (With 15pF Load)**



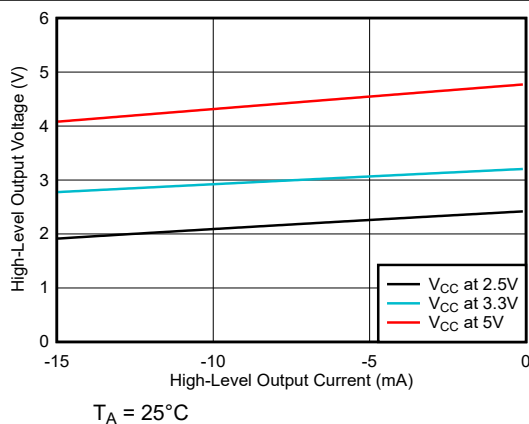
**Figure 5-4. ISO7741Tx-Q1 Supply Current vs. Data Rate (With No Load)**



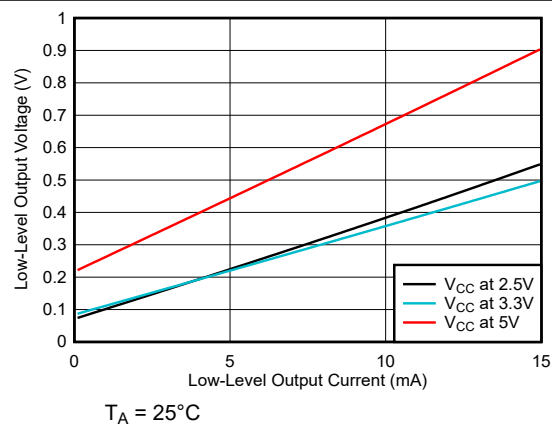
**Figure 5-5. ISO7742Tx-Q1 Supply Current vs. Data Rate (With 15pF Load)**



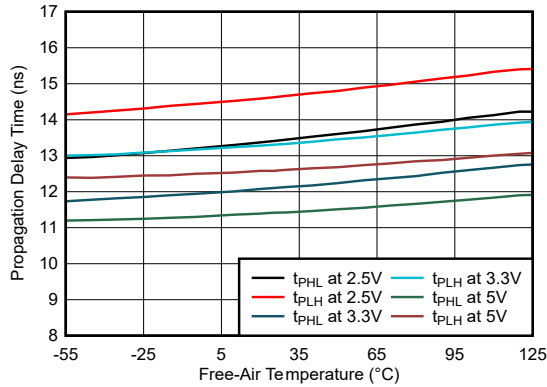
**Figure 5-6. ISO7742Tx-Q1 Supply Current vs. Data Rate (With No Load)**



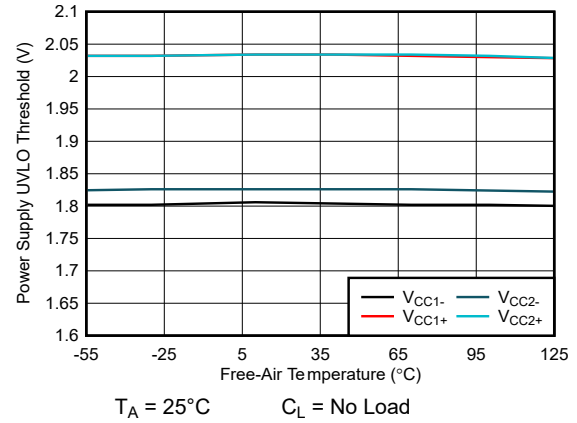
**Figure 5-7. High-Level Output Voltage vs. High-level Output Current**



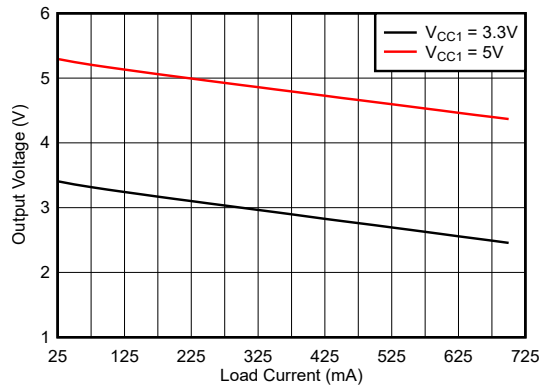
**Figure 5-8. Low-Level Output Voltage vs. Low-level Output Current**



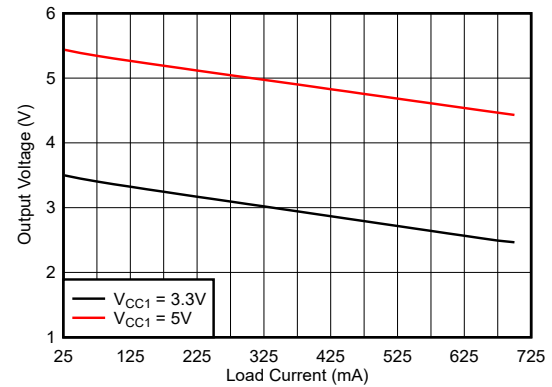
**Figure 5-9. Propagation Delay Time vs. Free-Air Temperature**



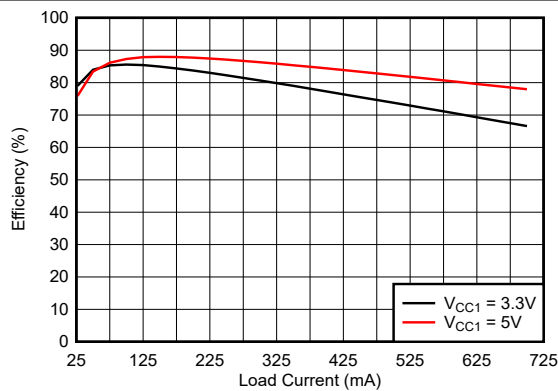
**Figure 5-10. Power Supply Undervoltage Threshold vs. Free-Air Temperature**



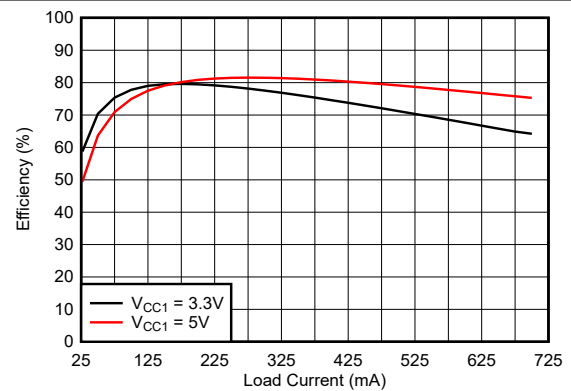
ISO774xTA-Q1 + Würth 750315240  
**Figure 5-11. ISO774xTA-Q1 Output Voltage vs. Load Current**



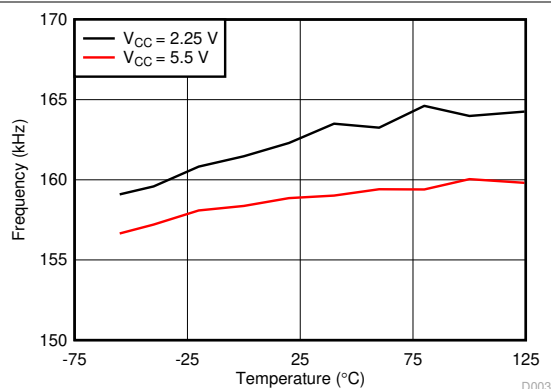
ISO774xTB-Q1 + Würth 750315371  
**Figure 5-12. ISO774xTB-Q1 Output Voltage vs. Load Current**



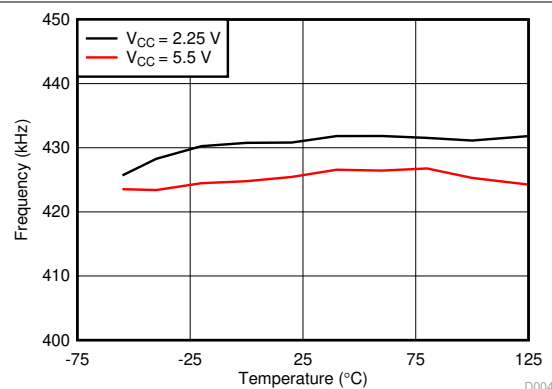
ISO774xTA-Q1 + Würth 750315240  
**Figure 5-13. ISO774xTA-Q1 Efficiency vs. Load Current**



ISO774xTB-Q1 + Würth 750315371  
**Figure 5-14. ISO774xTB-Q1 Efficiency vs. Load Current**

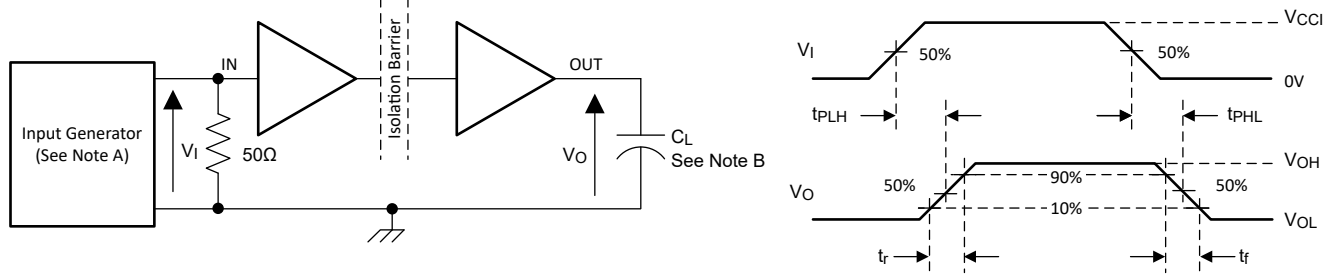


**Figure 5-15. ISO774xTA-Q1 Frequency vs. Free-Air Temperature**



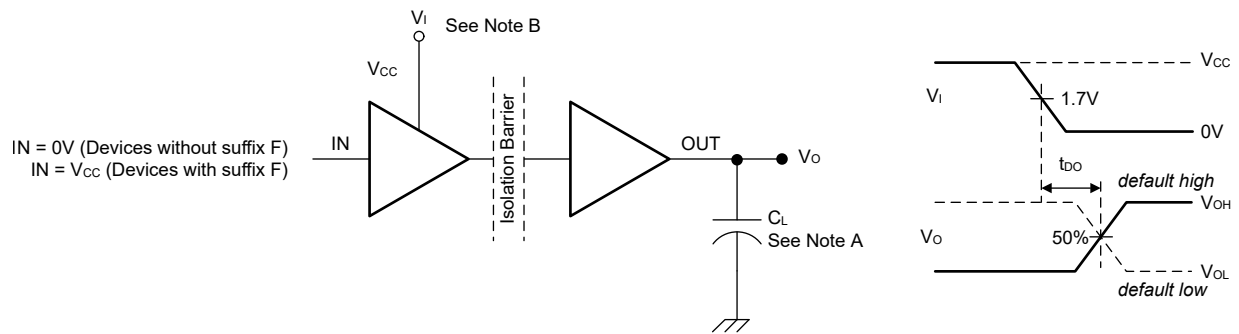
**Figure 5-16. ISO774xTB-Q1 Frequency vs. Free-Air Temperature**

## 6 Parameter Measurement Information



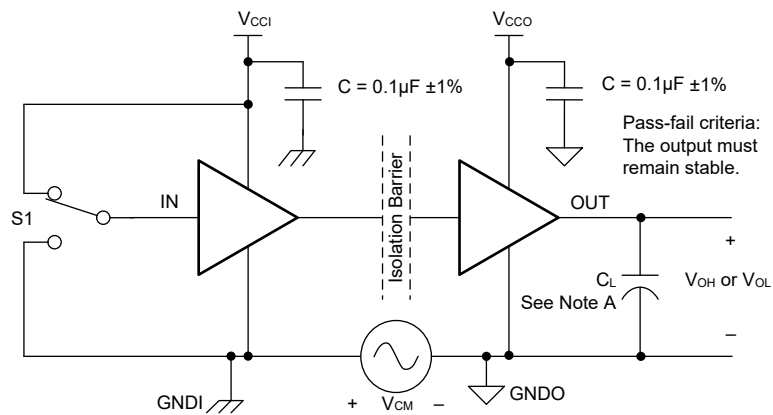
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50kHz, 50% duty cycle,  $t_r \leq$  3ns,  $t_f \leq$  3ns,  $Z_0 = 50\Omega$ . At the input, 50 $\Omega$  resistor is required to terminate Input Generator signal. The 50 $\Omega$  resistor is not needed in actual application.
- B.  $C_L = 15$ pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$ pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .
- B. Power Supply Ramp Rate = 10mV/ns

**Figure 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$ pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 6-3. Common-Mode Transient Immunity Test Circuit**

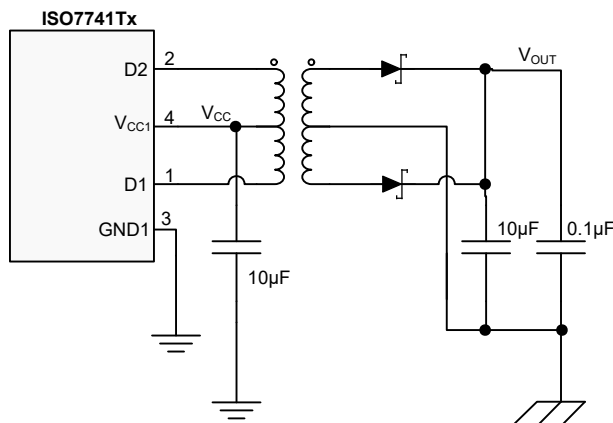


Figure 6-4. Measurement Circuit for Unregulated Output (TP1)

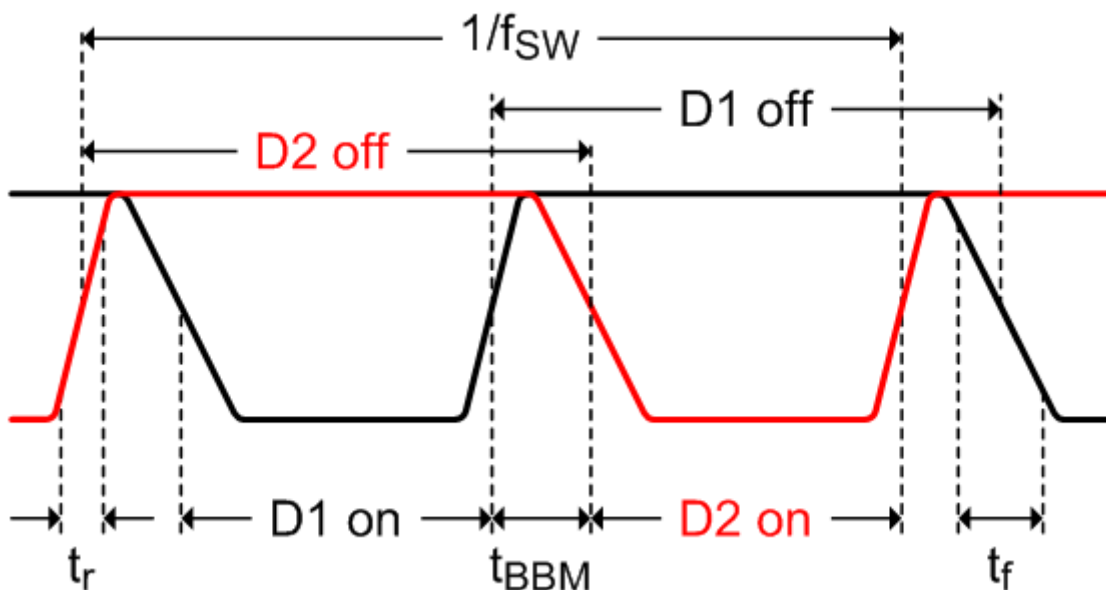


Figure 6-5. Timing Diagram

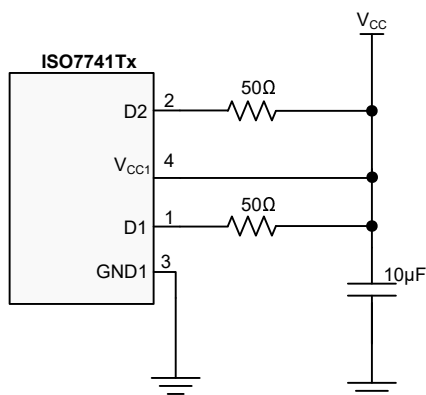
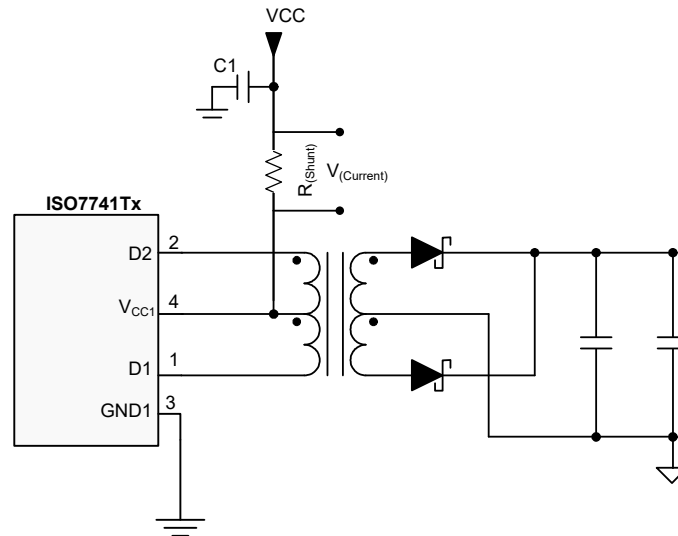


Figure 6-6. Test Circuit for FSW, V(slew), tBBM



**Figure 6-7. I(slew) Test Setup**

## 7 Detailed Description

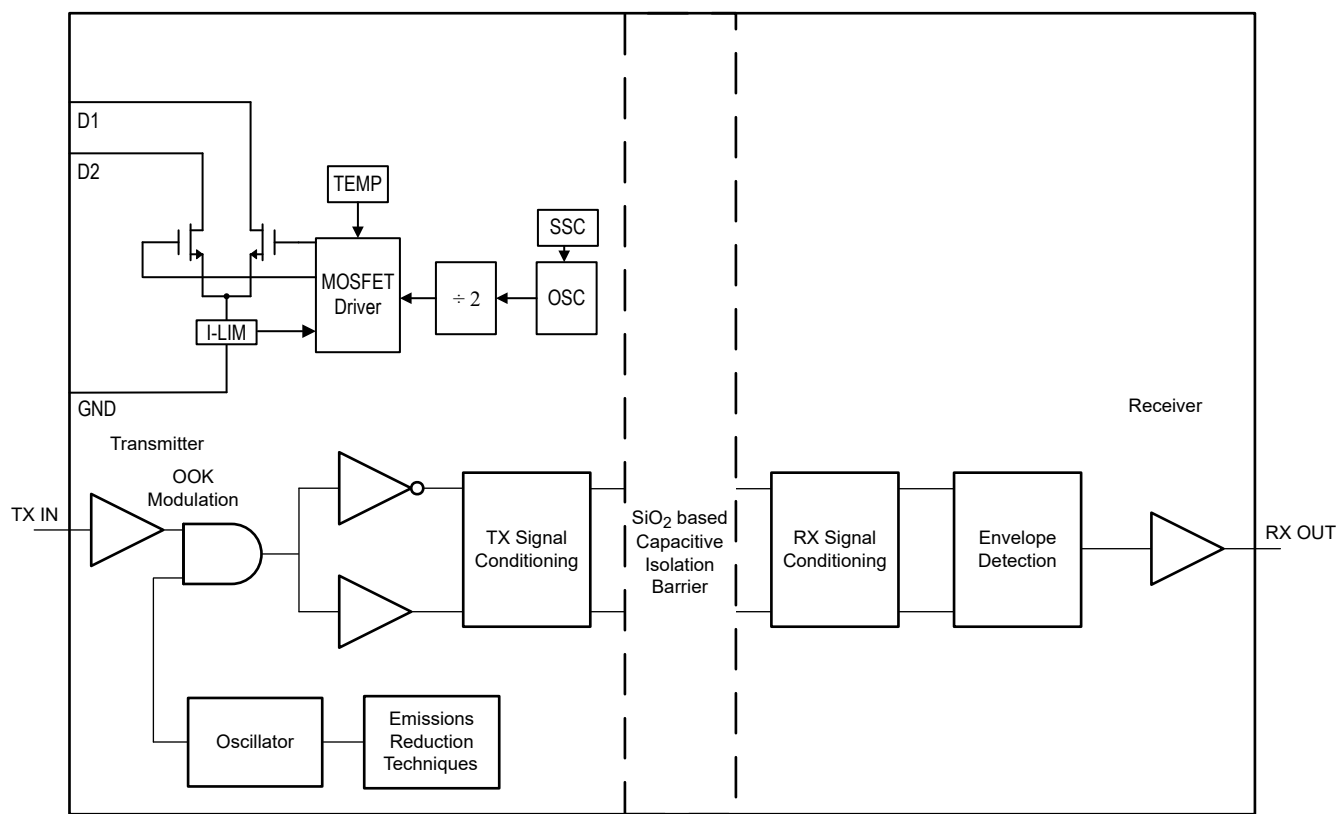
### 7.1 Overview

The ISO774xT devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO774xT also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching.

The transformer driver in ISO774xT is designed for cost competitive designs/applications, small form-factor, isolated DC/DC converters utilizing the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off. The output frequency of the oscillator is divided down by two. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. Before either one of the gates can assume logic high, the BBM logic provides a short time period during which both signals are low and both transistors are high-impedance. This short period, is required to avoid shorting out both ends of the primary. The resulting output signals, present the gate-drive signals for the output transistors.

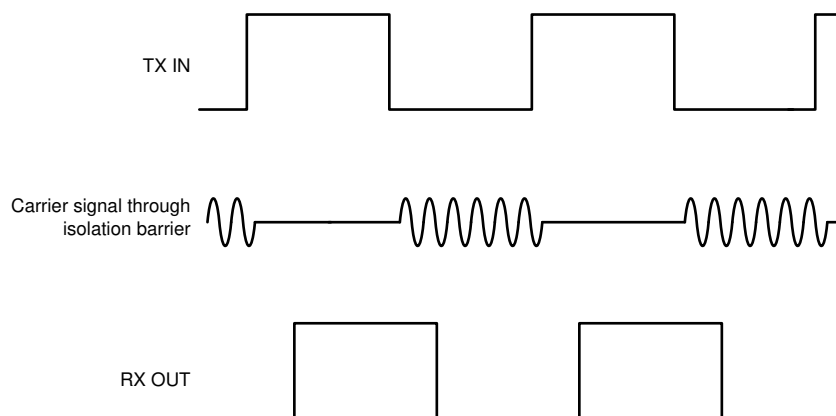
The conceptual block diagram of a digital capacitive isolator with integrated transformer driver, [Figure 7-1](#) and [Figure 7-2](#), shows a functional block diagram of a typical channel and transformer driver.

## 7.2 Functional Block Diagram



**Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

Figure 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.



**Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme**

## 7.3 Feature Description

**Table 7-1. Device Features**

| PART NUMBER | CHANNEL DIRECTION    | TYPICAL SWITCHING FREQUENCY | MAXIMUM DATA RATE | DEFAULT OUTPUT | PACKAGE | RATED ISOLATION                            |
|-------------|----------------------|-----------------------------|-------------------|----------------|---------|--------------------------------------------|
| ISO7741TA   | 3 Forward, 1 Reverse | 160kHz                      | 100Mbps           | High           | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |
| ISO7741FTA  |                      | 160kHz                      | 100Mbps           | Low            | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |
| ISO7741TB   |                      | 424kHz                      | 100Mbps           | High           | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |
| ISO7741FTB  |                      | 424kHz                      | 100Mbps           | Low            | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |
| ISO7742TA   | 2 Forward, 2 Reverse | 160kHz                      | 100Mbps           | High           | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |
| ISO7742FTA  |                      | 160kHz                      | 100Mbps           | Low            | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |
| ISO7742TB   |                      | 424kHz                      | 100Mbps           | High           | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |
| ISO7742FTB  |                      | 424kHz                      | 100Mbps           | Low            | DW-16   | 5000V <sub>RMS</sub> / 7071V <sub>PK</sub> |

See [Section 5.7](#) for detailed isolation ratings.

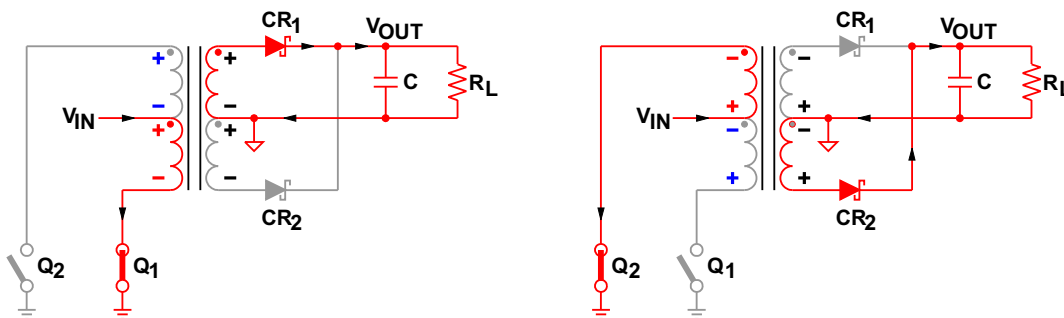
### 7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO774xT devices incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

### 7.3.2 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary (see [Figure 7-3](#)).



**Figure 7-3. Switching Cycles of a Push-Pull Converter**

When Q<sub>1</sub> conducts, V<sub>IN</sub> drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the V<sub>IN</sub> potential at the center-tap.

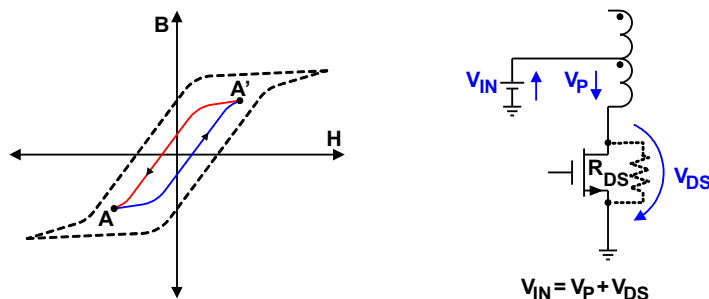
At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap to maintain the previously established current flow through  $Q_2$ , which now has turned high-impedance. The two voltage sources, each of which equaling  $V_{IN}$ , appear in series and cause a voltage potential at the open end of the primary of  $2 \times V_{IN}$  with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode  $CR_1$ . The secondary current starting from the upper secondary end flows through  $CR_1$ , charges capacitor  $C$ , and returns through the load impedance  $R_L$  back to the center-tap.

When  $Q_2$  conducts,  $Q_1$  goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a  $2 \times V_{IN}$  potential against ground. In this case  $CR_2$  is forward biased while  $CR_1$  is reverse biased and current flows from the lower secondary end through  $CR_2$ , charging the capacitor and returning through the load to the center-tap.

### 7.3.3 Core Magnetization

Figure 7-4 shows the ideal magnetizing curve for a push-pull converter with  $B$  as the magnetic flux density and  $H$  as the magnetic field strength. When  $Q_1$  conducts the magnetic flux is pushed from  $A$  to  $A'$ , and when  $Q_2$  conducts the flux is pulled back from  $A'$  to  $A$ . The difference in flux and thus in flux density is proportional to the product of the primary voltage,  $V_P$ , and the time,  $t_{ON}$ , the voltage is applied to the primary:  $B \cong V_P \times t_{ON}$ .



**Figure 7-4. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of  $R_{DS(on)}$**

This volt-seconds (V-t) product is important as the product determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

## 7.4 Device Functional Modes

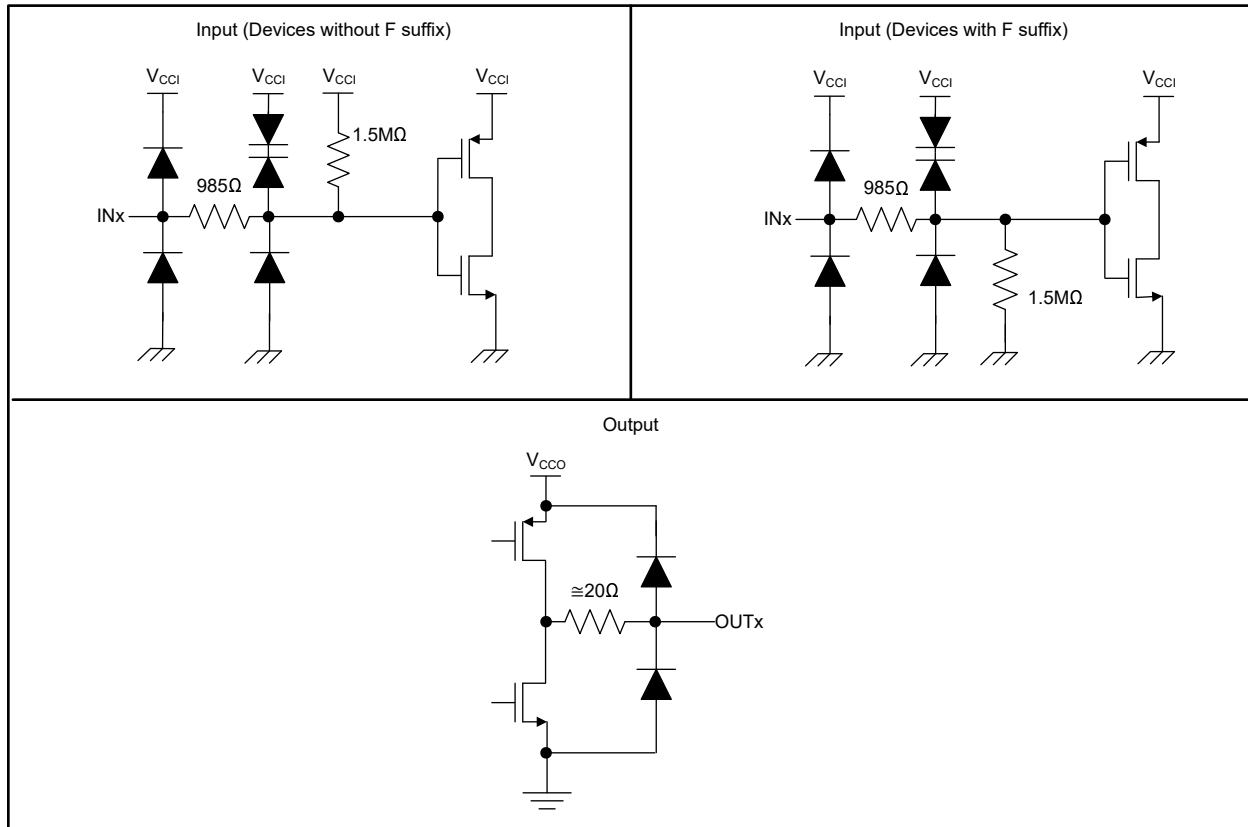
Table 7-2 lists the functional modes for the ISO774xT devices.

**Table 7-2. Function Table**

| $V_{CCI}$ 1 | $V_{CCO}$ | INPUT (INx)3 | OUTPUT (OUTx) | COMMENTS                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------|-----------|--------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PU          | PU        | H            | H             | Normal Operation:<br>A channel output assumes the logic state of the input.                                                                                                                                                                                                                                                                                                                                                     |
|             |           | L            | L             |                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|             |           | Open         | Default       | Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default is <i>High</i> for ISO774xTx and <i>Low</i> for ISO774xFTx.                                                                                                                                                                                                                                                           |
| PD          | PU        | X            | Default       | Default mode: When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is <i>High</i> for ISO774xTx and <i>Low</i> for ISO774xFTx.<br>When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.<br>When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |
| X           | PD        | X            | Undetermined  | When $V_{CCO}$ is unpowered, a channel output is undetermined 2.<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.                                                                                                                                                                                                                                             |

1.  $V_{CC1}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ ; PU = Powered up ( $V_{CC} \geq 2.25V$ ); PD = Powered down ( $V_{CC} \leq 1.7V$ ); X = Irrelevant; H = High level; L = Low level; Z = High Impedance
2. The outputs are in undetermined state when  $1.7V < V_{CC1}$ ,  $V_{CCO} < 2.25V$ .
3. A strongly driven input signal can weakly power the floating  $V_{CC}$  through an internal protection diode and cause undetermined output.

#### 7.4.1 Device I/O Schematics



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**Figure 7-5. Device I/O Schematics**

#### 7.4.2 Start-Up Mode

When the supply voltage at  $V_{CC1}$  ramps up to 2.25V, the internal oscillator starts operating. The output stage begins switching but the amplitude of the drain signals at D1 and D2 has not reached the full maximum yet.

ISO774xT-Q1 devices support soft-start feature. Upon power up, the gate drive of the output power-MOSFET is gradually increased over a period of time from 0V to  $V_{CC1}$ . Soft-start prevents high inrush current from  $V_{CC1}$  while charging large secondary side decoupling capacitors, and also prevents overshoot in secondary voltage during power-up.

#### 7.4.3 Operating Mode

When the device supply has reached the nominal value  $\pm 10\%$  the oscillator is fully operating. However variations over supply voltage and operating temperature can vary the switching frequencies at D1 and D2.

#### 7.4.4 Spread Spectrum Clocking

Radiated emissions is an important concern in high current switching power supplies. ISO774xT-Q1 transformer driver addresses this by modulating the internal clock in such a way that the emitting energy is spread over multiple frequency bins. This Spread Spectrum clocking feature greatly improves the emissions performance of

the entire power supply block and hence relieves the system designer from one major concern in isolated power supply design.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The device is a high-performance, quad-channel digital isolator with integrated high efficiency transformer driver. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to integrated transformer driver, with external transformer, the isolated supply can be generated to power the isolated side of the device and peripherals on isolated side, thus saving board space without compromising on efficiency. The voltage range is from 2.25V to 5.5V for both supplies,  $V_{CC1}$  and  $V_{CC2}$ . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is,  $\mu C$  or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

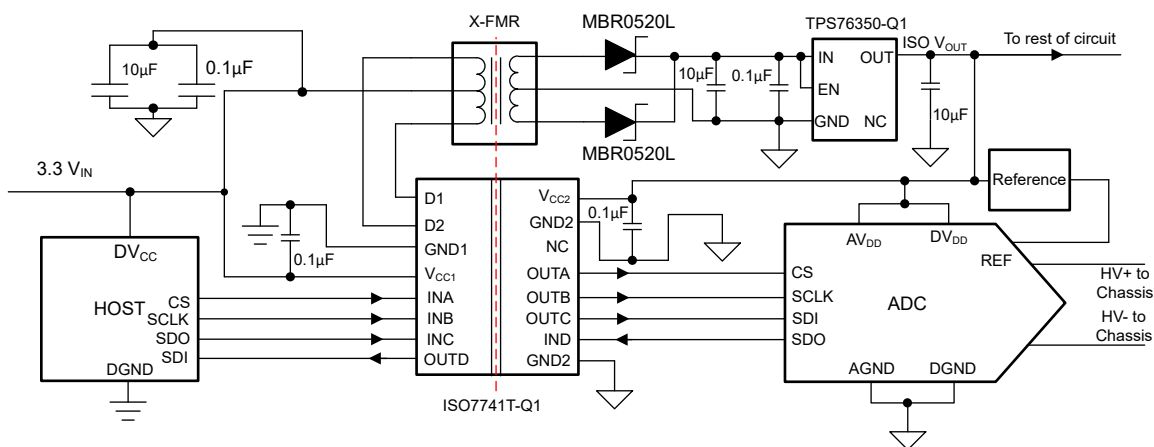
The device is designed for applications that have limited board space and desire more integration. The device is also designed for very high voltage applications with power transformer supporting high voltage isolation.

### 8.2 Typical Application

The following application circuit is shown for a 3.3V input supply commonly taken from the local, regulated microcontroller supply for SPI isolation. For 5V input voltages requiring different turn ratios refer to the transformer manufacturers and the web sites listed in [Transformer Manufacturers](#)

**Table 8-1. Transformer Manufacturers**

| MANUFACTURER                 | MORE INFORMATION                                                            |
|------------------------------|-----------------------------------------------------------------------------|
| Coilcraft Inc.               | <a href="http://www.coilcraft.com">http://www.coilcraft.com</a>             |
| Halo-Electronics Inc.        | <a href="http://www.haloelectronics.com">http://www.haloelectronics.com</a> |
| Murata Power Solutions       | <a href="http://www.murata-ps.com">http://www.murata-ps.com</a>             |
| Würth Electronics Midcom Inc | <a href="http://www.midcom-inc.com">http://www.midcom-inc.com</a>           |



**Figure 8-1. Isolated Power and SPI for ADC Sensing Application With ISO774xT-Q1**

### 8.2.1 Design Requirements

To design with these devices, use the parameters listed in [Design Parameters](#).

**Table 8-2. Design Parameters**

| PARAMETER                                       | VALUE                                 |
|-------------------------------------------------|---------------------------------------|
| Supply voltage, $V_{CC1}$                       | 2.25V to 5.5V                         |
| Decoupling capacitor between $V_{CC1}$ and GND1 | 0.1 $\mu$ F + 1 $\mu$ F to 10 $\mu$ F |
| Decoupling capacitor from $V_{CC2}$ and GND2    | 0.1 $\mu$ F + 1 $\mu$ F to 10 $\mu$ F |

### 8.2.2 Detailed Design Procedure

The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Contrary to popular belief, the output voltage of the unregulated converter output drops significantly over a wide range in load current. The characteristic curve in [Figure 8-2](#) and [Figure 8-3](#) for example, shows that the difference between  $V_{OUT}$  at minimum load and  $V_{OUT}$  at maximum load exceeds a transceiver supply range. Therefore, to provide a stable, load independent supply while maintaining maximum possible efficiency the implementation of a low dropout regulator (LDO) is strongly advised.

#### 8.2.2.1 Drive Capability

The transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 2.25V to 5.5V. While converter designs with higher output voltages are possible, care must be taken that higher turns ratios do not lead to primary currents that exceed the specified current limits of the device.

#### 8.2.2.2 LDO Selection

The minimum requirements for a suitable low dropout regulator are:

- The current drive capability must slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore, for a load current of 550mA, choose a 600mA to 700mA LDO. While regulators with higher drive capabilities are acceptable, these regulators also typically possess higher dropout voltages that reduce the overall converter efficiency.
- The internal dropout voltage,  $V_{DO}$ , at the specified load current must be as low as possible to maintain efficiency. For a low-cost 700mA LDO, a  $V_{DO}$  of 600mV at 700mA is common. Be aware; however, that this lower value is typically specified at room temperature and can increase by a factor of 2 over temperature, which in turn raises the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

$$V_{I-min} = V_{DO-max} + V_{O-max} \quad (1)$$

To determine  $V_I$  for worst-case condition, the user must take the maximum values for  $V_{DO}$  and  $V_O$  specified in the LDO data sheet for rated output current (that is, 600mA) and add these values together. The user must also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than  $V_{I-min}$ . If the output voltage is not, the LDO loses line-regulation and any variations at the input passes straight through to the output. Hence, below  $V_{I-min}$  the output voltage follows the input and the regulator behaves like a simple conductor.

- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across  $R_{DS-on}$  negligible and allowing the entire converter input voltage to drop across the primary. At this point, the secondary reaches the maximum voltage of

$$V_{S-max} = V_{IN-max} \times n \quad (2)$$

with  $V_{IN-max}$  as the maximum converter input voltage and  $n$  as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than  $V_{S-max}$ . [Table 8-3](#) lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters.

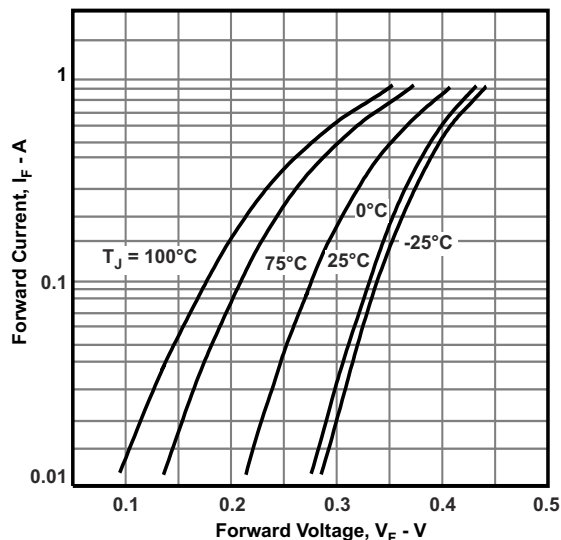
**Table 8-3. Required Maximum LDO Input Voltages for Various Push-Pull Configurations**

| PUSH-PULL CONVERTER         |                  |               |                 | LDO             |
|-----------------------------|------------------|---------------|-----------------|-----------------|
| CONFIGURATION               | $V_{IN-max}$ [V] | TURNS-RATIO   | $V_{S-max}$ [V] | $V_{I-max}$ [V] |
| $3.3V_{IN}$ to $3.3V_{OUT}$ | 3.6              | $1.5 \pm 3\%$ | 5.6             | 6 to 10         |
| $3.3V_{IN}$ to $5V_{OUT}$   | 3.6              | $2.2 \pm 3\%$ | 8.2             | 10              |
| $5V_{IN}$ to $5V_{OUT}$     | 5.5              | $1.5 \pm 3\%$ | 8.5             | 10              |

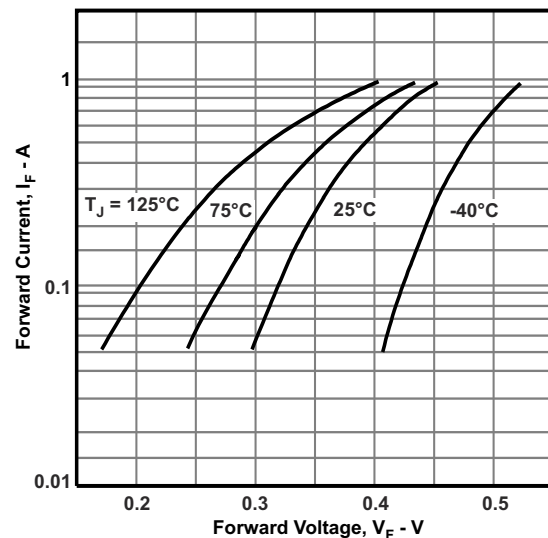
### 8.2.2.3 Diode Selection

A rectifier diode must always possess low-forward voltage to provide as much voltage to the converter output as possible. When used in high-frequency switching applications, such as the ISO774xTx-Q1 however, the diode must also possess a short recovery time. Schottky diodes meet both requirements and are therefore strongly recommended in push-pull converter designs. A good choice for low-volt applications and ambient temperatures of up to 85°C is the low-cost Schottky rectifier MBR0520L with a typical forward voltage of 275mV at 100mA forward current. For higher output voltages such as  $\pm 10V$  and above use the MBR0530 which provides a higher DC blocking voltage of 30V.

Lab measurements have shown that at temperatures higher than 100°C the leakage currents of the above Schottky diodes increase significantly. These conditions can cause thermal runaway leading to the collapse of the rectifier output voltage. Therefore, for ambient temperatures higher than 85°C use low-leakage Schottky diodes, such as RB168MM-40.



**Figure 8-2. Diode Forward Characteristics for MBR0520L**



**Figure 8-3. Diode Forward Characteristics for MBR0530**

### 8.2.2.4 Capacitor Selection

As with all high speed CMOS ICs, the device requires a bypass capacitor in the range of 10nF to 100nF.

The input bulk capacitor at the center-tap of the primary supports large currents into the primary during the fast switching transients. For minimum ripple make this capacitor 1 $\mu$ F to 10 $\mu$ F. In a 2-layer PCB design with a dedicated ground plane, place this capacitor close to the primary center-tap to minimize trace inductance. In a 4-layer board design with low-inductance reference planes for ground and  $V_{CC}$ , the capacitor can be placed at the supply entrance of the board. To provide low-inductance paths use two vias in parallel for each connection to a reference plane or to the primary center-tap.

The bulk capacitor at the rectifier output smooths the output voltage. Make this capacitor 1 $\mu$ F to 10 $\mu$ F.

The small capacitor at the regulator input is not necessarily required. However, good analog design practice suggests, using a small value of 47nF to 100nF improves the transient response and noise rejection of the regulator.

The LDO output capacitor buffers the regulated output for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7μF to 10μF satisfies these requirements.

### 8.2.2.5 Transformer Selection

#### 8.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation, the V-t product must be greater than the maximum V-t product applied by the device. The maximum voltage delivered by the device is the nominal converter input plus 10%. The maximum time this voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the minimum V-t product for the transformer is determined through:

$$V_{t_{min}} \geq V_{IN-max} \times \frac{T_{max}}{2} = \frac{V_{IN-max}}{2 \times f_{min}} \quad (3)$$

Taking an example of  $f_{min}$  as 138kHz for ISO774xTA-Q1 and 363kHz for ISO774xTB-Q1 with a 5V supply, the following equations yield the minimum V-t products of:

$$V_{t_{min}} \geq \frac{5.5V}{2 \times 138kHz} = 20V\mu s \text{ for ISO774xTA-Q1 applications, and}$$

$$V_{t_{min}} \geq \frac{5.5V}{2 \times 363kHz} = 7.6V\mu s \text{ for ISO774xTB-Q1 applications}$$

Common V-t values for low-power center-tapped transformers range from 22Vμs to 150Vμs with typical footprints of 10mm x 12mm. However, transformers specifically designed for PCMCIA applications provide as little as 11Vμs and come with a significantly reduced footprint of 6mm x 6mm only.

While Vt-wise all of these transformers can be driven by the device, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

#### 8.2.2.5.2 Turns Ratio Estimate

Assuming that the rectifier diodes and linear regulator are selected and that the transformer selected must have a V-t product of at least 11Vμs. However, before searching the manufacturer web sites for a suitable transformer, the user still needs to know the minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer typical efficiency of 97% into account:

$$V_{P-min} = V_{IN-min} - V_{DS-max} \quad (4)$$

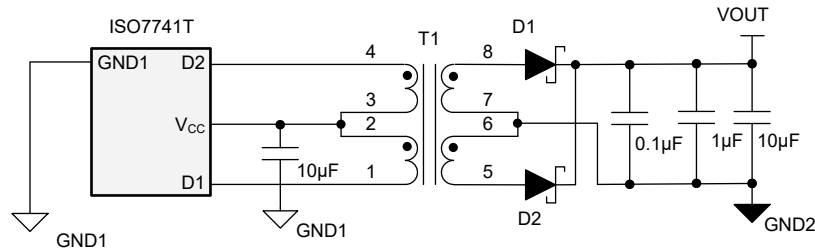
$V_{S-min}$  must be large enough to allow for a maximum voltage drop,  $V_{F-max}$ , across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the [LDO Selection](#) section, this minimum input voltage is known and by adding  $V_{F-max}$  gives the minimum secondary voltage with:

$$V_{S-min} = V_{F-max} + V_{DO-max} + V_{O-max} \quad (5)$$

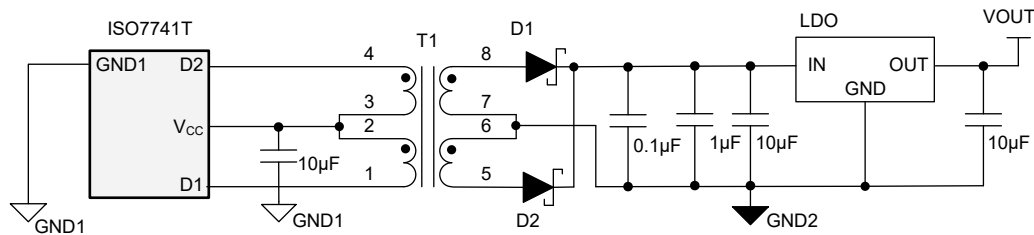


### 8.2.2.5.3 Recommended Transformers

Depending on the application, use the minimum configuration in [Figure 8-5](#) or standard configuration in [Figure 8-6](#).



**Figure 8-5. Unregulated Output for Low-Current Loads With Wide Supply Range**



**Figure 8-6. Regulated Output for Stable Supplies and High Current Loads**

The Würth Electronics Midcom isolation transformers in [Table 8-4](#) are optimized designs for the device, providing high efficiency and small form factor at low-cost.

The 1:1.1 and 1:1.7 turns-ratios are designed for logic applications with wide supply rails and low load currents. These applications operate without LDO, thus achieving further cost-reduction.

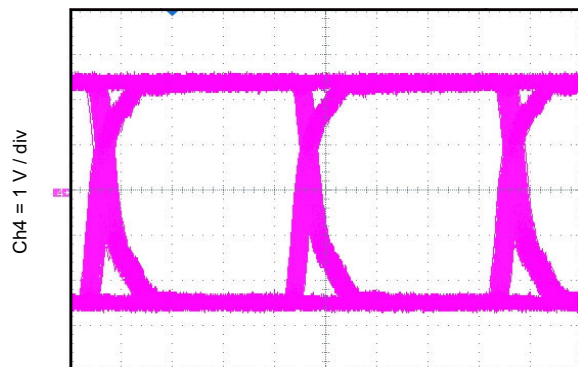
**Table 8-4. Recommended Isolation Transformers Optimized for the Device**

| Turns Ratio | V × T (Vμs) | Isolation (V <sub>RMS</sub> ) | Dimensions (mm)                  | Application                                                      | LDO <sup>(1)</sup>             | Order No.      | Manufacturer               |
|-------------|-------------|-------------------------------|----------------------------------|------------------------------------------------------------------|--------------------------------|----------------|----------------------------|
| 1:1.1 ±2%   | 7           | 2500                          | 6.73 x 10.05 x 4.19              | 3.3V → 3.3V, 100mA, ISO774xTB-Q1                                 | No                             | 760390011      | Würth Electronics / Midcom |
| 1:1.1 ±2%   | 11          |                               |                                  | 5V → 5V, 100mA, ISO774xTB-Q1                                     |                                | 760390012      |                            |
| 1:1.7 ±2%   |             |                               |                                  | 3.3V → 5V, 100mA, ISO774xTB-Q1                                   |                                | 760390013      |                            |
| 1:1.3 ±2%   |             |                               |                                  | 3.3V → 3.3V, 100mA, ISO774xTB-Q1                                 | Yes                            | 760390014      |                            |
| 1:1.3 ±2%   |             |                               |                                  | 5V → 5V, 100mA, ISO774xTB-Q1                                     |                                | 760390014      |                            |
| 1:2.1 ±2%   |             |                               |                                  | 3.3V → 5V, 100mA, ISO774xTB-Q1                                   |                                | 760390015      |                            |
| 1.23:1 ±2%  |             |                               | 5V → 3.3V, 100mA, ISO774xTB-Q1   | 750313710                                                        |                                |                |                            |
| 1:1.7 ±2%   | 8.9         |                               | 8.3 x 12.6 x 4.1                 | 3.3V → 3.3V, 1A, ISO774xTB-Q1                                    | No                             | 750316028      |                            |
| 1:2.1 ±2%   |             |                               |                                  | 3.3V → 5V, 1A, ISO774xTB-Q1                                      |                                | 750316029      |                            |
| 1.3:1 ±2%   | 10.8        |                               |                                  | 5V → 3.3V, 1A, ISO774xTB-Q1                                      |                                | 750316030      |                            |
| 1:1.1 ±2%   | 8.6         |                               |                                  | 3.3V → 3.3V, 1A, ISO774xTB-Q1                                    | No                             | 750315371      |                            |
|             |             |                               |                                  | 5V → 5V, 1A, ISO774xTB-Q1                                        |                                | 750315371      |                            |
| 1:1.1 ±2%   | 11          | 9.14 x 12.7 x 7.37            |                                  | 3.3V → 3.3V, 100mA, ISO774xTB-Q1                                 |                                | No             | 750313734                  |
| 1:1.1 ±2%   |             |                               | 5V → 5V, 100mA, ISO774xTB-Q1     | 750313734                                                        |                                |                |                            |
| 1:1.7 ±2%   |             |                               | 3.3V → 5V, 100mA, ISO774xTB-Q1   | 750313769                                                        |                                |                |                            |
| 1:1.3 ±2%   |             |                               | 3.3V → 3.3V, 100mA, ISO774xTB-Q1 | Yes                                                              | 750313638                      |                |                            |
| 1:2.1 ±2%   |             |                               | 5V → 5V, 100mA, ISO774xTB-Q1     |                                                                  | 750313626                      |                |                            |
| 1.3:1 ±2%   |             |                               | 5V → 3.3V, 100mA, ISO774xTB-Q1   | No                                                               | 750313638                      |                |                            |
| 1:1.75 ±2%  | 41          | 12.32 x 15.41 x 11.05         | 3.3V → 3.3V, 1A, ISO774xTA-Q1    | Yes                                                              | 750316031                      |                |                            |
| 1:2 ±2%     |             |                               | 3.3V → 5V, 1A, ISO774xTA-Q1      | No                                                               | 750316032                      |                |                            |
| 1.3:1 ±2%   | 42          |                               | 5.0V → 3.3V, 1A, ISO774xTA-Q1    |                                                                  | 750316033                      |                |                            |
| 1:1.1 ±2%   | 23          | 12.32 x 15.41 x 11.89         | 3.3V → 3.3V, 1A, ISO774xTA-Q1    |                                                                  | No                             | 750315240      |                            |
|             |             |                               | 5V → 5V, 1A, ISO774xTA-Q1        |                                                                  |                                | 750315240      |                            |
| 1:3.5 ±2%   | 9           | 9.14 x 12.95 x 7.62           | 5V → 17.5V, 100mA,ISO774xTB-Q1   | No                                                               | 750342879                      |                |                            |
| 1:3.9 ±2%   |             | 9.17 x 12.7 x 7.62            | 5V → 19.5V, 100mA,ISO774xTB-Q1   |                                                                  | 750343725                      |                |                            |
| 1:3.75 ±2%  | 9.5         | 8.3 x 12.6 x 4.1              | 5V → 18.75V, 100mA,ISO774xTB-Q1  |                                                                  | 78931812518                    |                |                            |
| 1:4.75 ±2%  |             |                               | 5V → 23.75V, 100mA,ISO774xTB-Q1  |                                                                  | 78931812523                    |                |                            |
| 1:2.5 ±2%   |             |                               | 5V → 12.5V, 200mA,ISO774xTB-Q1   |                                                                  | 78931812512                    |                |                            |
| 1:3.13 ±2%  |             |                               | 5V → 15.65V, 200mA,ISO774xTB-Q1  |                                                                  | 78931812515                    |                |                            |
| 1:3.5 ±2%   | 16          | 6000                          | 9.14 x 12.7 x 7.62               |                                                                  | 5V → 17.5V, 100mA,ISO774xTB-Q1 | 750320340      |                            |
| 1:1.3 ±3%   | 11          | 5000                          | 10.4 x 12.2 x 6.1                | 3.3V → 3.3V, 300mA, ISO774xTB-Q1<br>5V → 5V, 300mA, ISO774xTB-Q1 | No                             | HCT-SM-1.3-8-2 | Bourns                     |
| 1:1.5 ±3%   | 34.4        | 2500                          | 10 x 12.07 x 5.97                | 3.3V → 3.3V, 1A, ISO774xTB-Q1<br>5V → 5V, 1A, ISO774xTA/B-Q1     | Yes                            | DA2303-AL      | Coilcraft                  |
| 1:2.2 ±3%   | 21.5        | 2500                          | 10 x 12.07 x 5.97                | 3.3V → 5V, 1A, ISO774xTA/B-Q1                                    |                                | DA2304-AL      |                            |

(1) For configurations with LDO, a higher voltage than the required output voltage is generated, to allow for LDO drop-out. Figures show the voltage and efficiency at the LDO input.

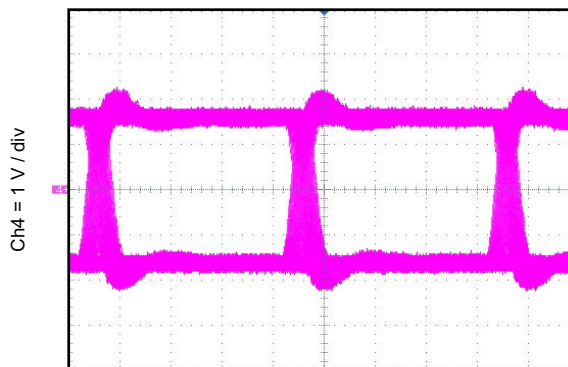
### 8.2.3 Application Curve

The following typical eye diagrams of the device indicates low jitter and wide open eye at the maximum data rate of 100Mbps.



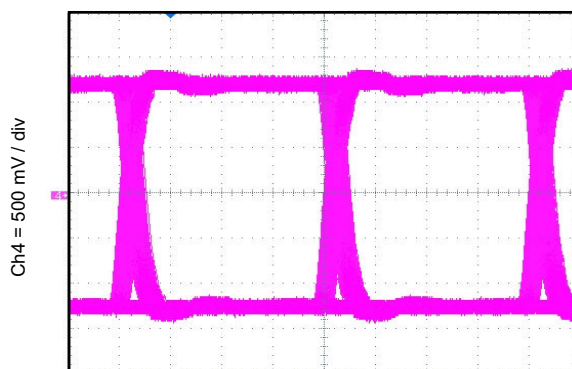
Time = 2.5 ns / div

**Figure 8-7. Eye Diagram at 100Mbps PRBS  $2^{16} - 1$ , 5V and 25°C**



Time = 2.5 ns / div

**Figure 8-8. Eye Diagram at 100Mbps PRBS  $2^{16} - 1$ , 3.3V and 25°C**



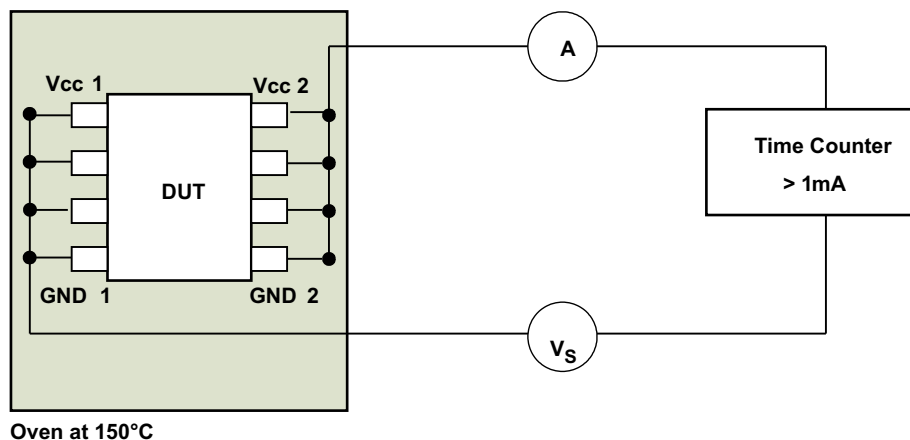
Time = 2.5 ns / div

**Figure 8-9. Eye Diagram at 100Mbps PRBS  $2^{16} - 1$ , 2.5V and 25°C**

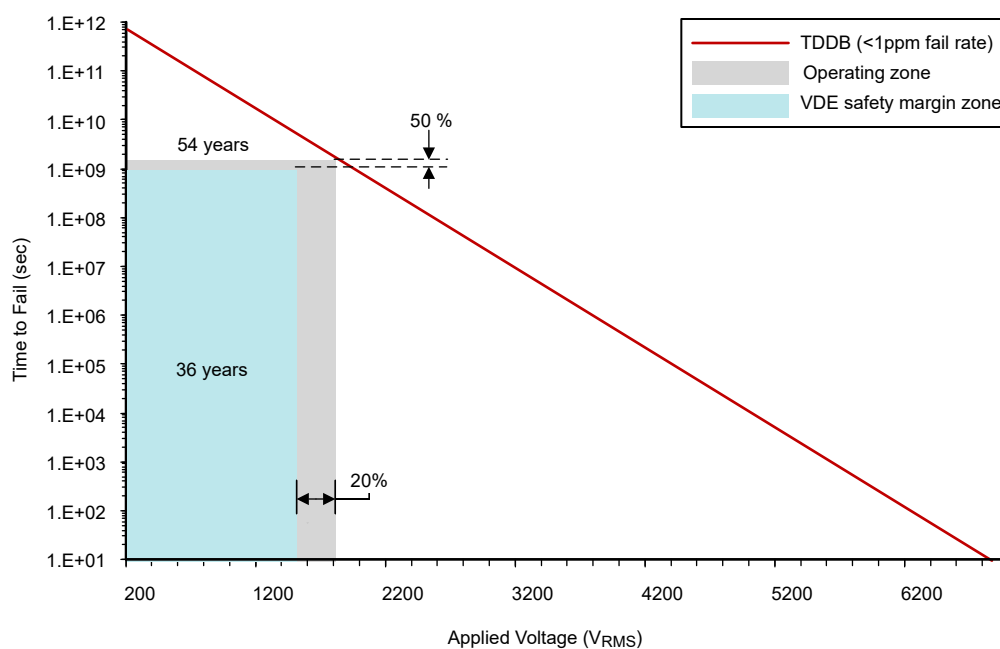
#### 8.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 8-10](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

[Figure 8-11](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 1500V<sub>RMS</sub> with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, and more can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to 1500V<sub>RMS</sub>. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.



**Figure 8-10. Test Setup for Insulation Lifetime Measurement**

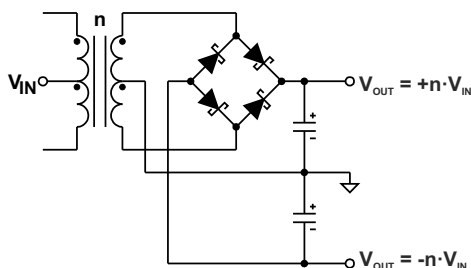


**Figure 8-11. Insulation Lifetime Projection Data**

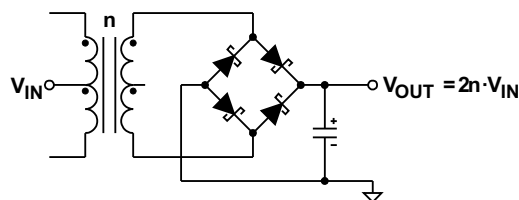
## 8.2.4 System Examples

### 8.2.4.1 Higher Output Voltage Designs

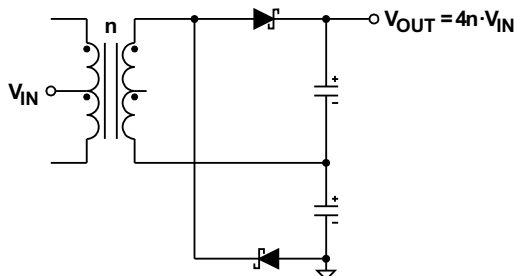
The device can drive push-pull converters that provide high output voltages of up to 30V, or bipolar outputs of up to  $\pm 15V$ . Using commercially available center-tapped transformers, with relatively low turns ratios of 0.8 to 5, requires different rectifier topologies to achieve high output voltages. Figure 8-12 to Figure 8-14 show some of these topologies together with the respective open-circuit output voltages.



**Figure 8-12. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs**



**Figure 8-13. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Doubling**



**Figure 8-14. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling  $V_{IN}$**

## 8.3 Power Supply Recommendations

The device is designed to operate in an input voltage supply range of 2.5V to 5V nominal. This input supply must be regulated within  $\pm 10\%$ . To help provide reliable operation at data rates and supply voltages, a  $0.1\mu F$  bypass capacitor is recommended at the input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors must be placed as close to the supply pins as possible. A  $10\mu F$  capacitor must be connected close to the transformer center-tap pin for reliable power transfer. The isolated power is generated for the secondary-side with help of a transformer driver as shown in the [application diagram](#).

## 8.4 Layout

### 8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 8-15). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately  $100pF/inch^2$ .
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

- A low-ESR ceramic bypass-capacitor must be connected between the  $V_{CC}$  and GND pins for both the supply. The recommended capacitor value can range from  $0.1\mu\text{F}$  to  $10\mu\text{F}$ . The capacitor must have a voltage rating of 10V minimum and a X5R or X7R dielectric. The optimum placement of decap is closest to the  $V_{CC}$  and GND pins.
- The connections between the device D1 and D2 pins and the transformer primary endings, and the connection of the device  $V_{CC1}$  pin and the transformer center-tap must be as close as possible for minimum trace inductance. And  $10\mu\text{F}$  capacitor must be connected close to the transformer center-tap pin. Length matching of D1 and D2 traces provide the best performance in efficiency and EMI.
- The rectifier diodes must be Schottky diodes with low forward voltage in the 10mA to 100mA current range to maximize efficiency.

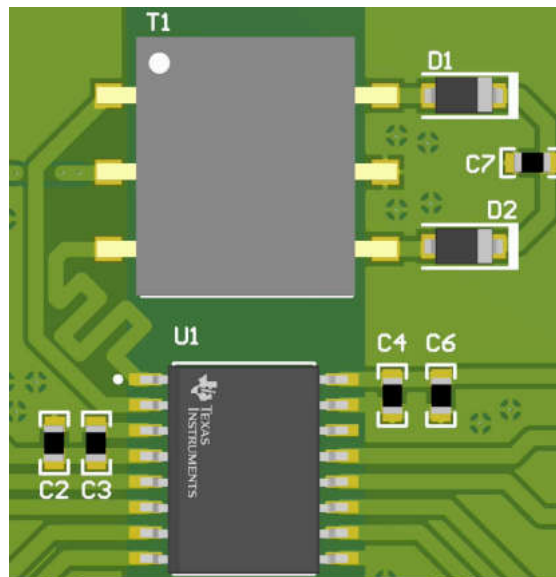
If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

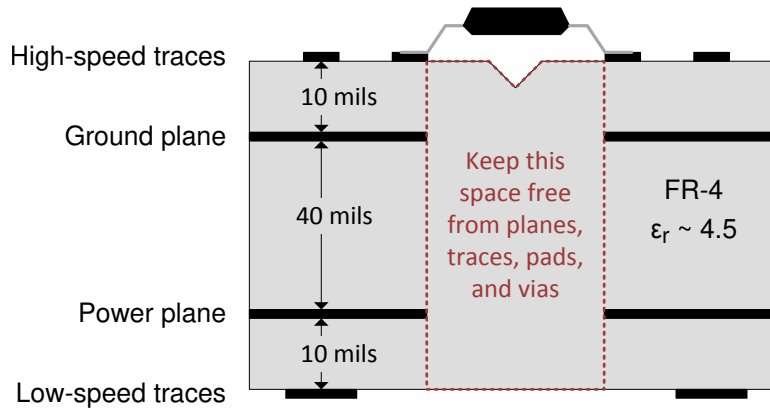
#### 8.4.1.1 PCB Material

For digital circuit boards operating below 150Mbps, (or rise and fall times higher than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to the lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

#### 8.4.2 Layout Example



**Figure 8-15. Example Layout**



**Figure 8-16. Example PCB Stackup**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#), application note
- Texas Instruments, [Isolation Glossary](#), application note
- Texas Instruments, [How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems](#), application note

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

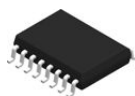
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision A (July 2024) to Revision B (January 2025)</b>                                                                    | <b>Page</b>        |
|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the documents.....                                     | <a href="#">1</a>  |
| • Added new spins ISO7742Tx-Q1.....                                                                                                        | <a href="#">1</a>  |
| • Moved the HBM and CDM values from the <i>Features</i> section to the <i>ESD Ratings</i> table.....                                       | <a href="#">6</a>  |
| • Changed CMTI TYP value from 75kV/μs to 100 kV/μs in all Electrical Characteristics tables.....                                           | <a href="#">12</a> |
| • Added new Device ISO7742Tx.....                                                                                                          | <a href="#">13</a> |
| • Changed the t <sub>DO</sub> TYP value from 6μs to 0.1μs and the MAX value from 9μs to 0.3μs in all Switching Characteristics tables..... | <a href="#">18</a> |

| <b>Changes from Revision * (April 2024) to Revision A (July 2024)</b>                                  | <b>Page</b>        |
|--------------------------------------------------------------------------------------------------------|--------------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the documents..... | <a href="#">1</a>  |
| • Changed minimum CMTI from 40 to 85 in all Electrical Characteristics tables.....                     | <a href="#">12</a> |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

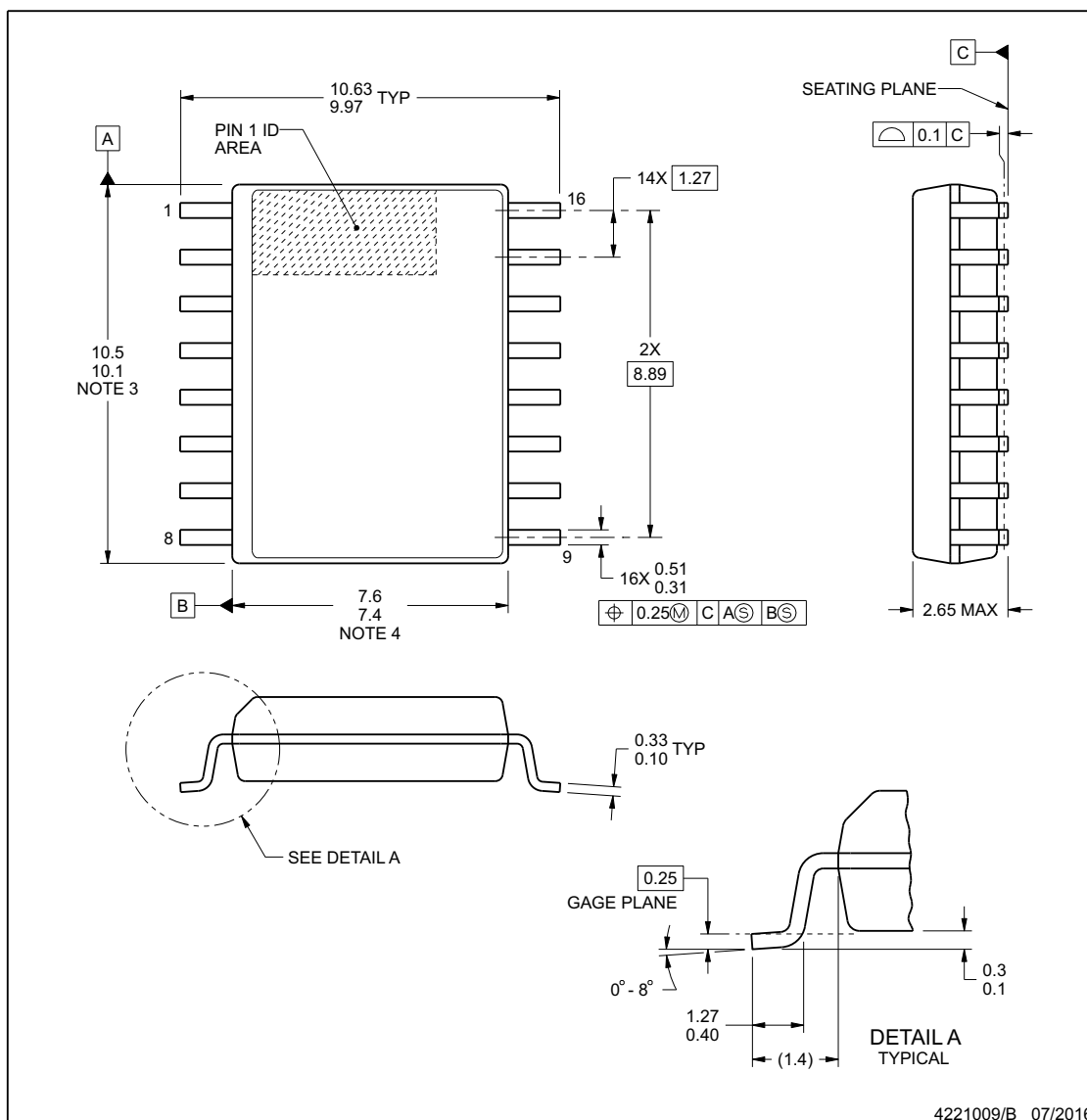


## PACKAGE OUTLINE

**DW0016B**

**SOIC - 2.65 mm max height**

SOIC



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

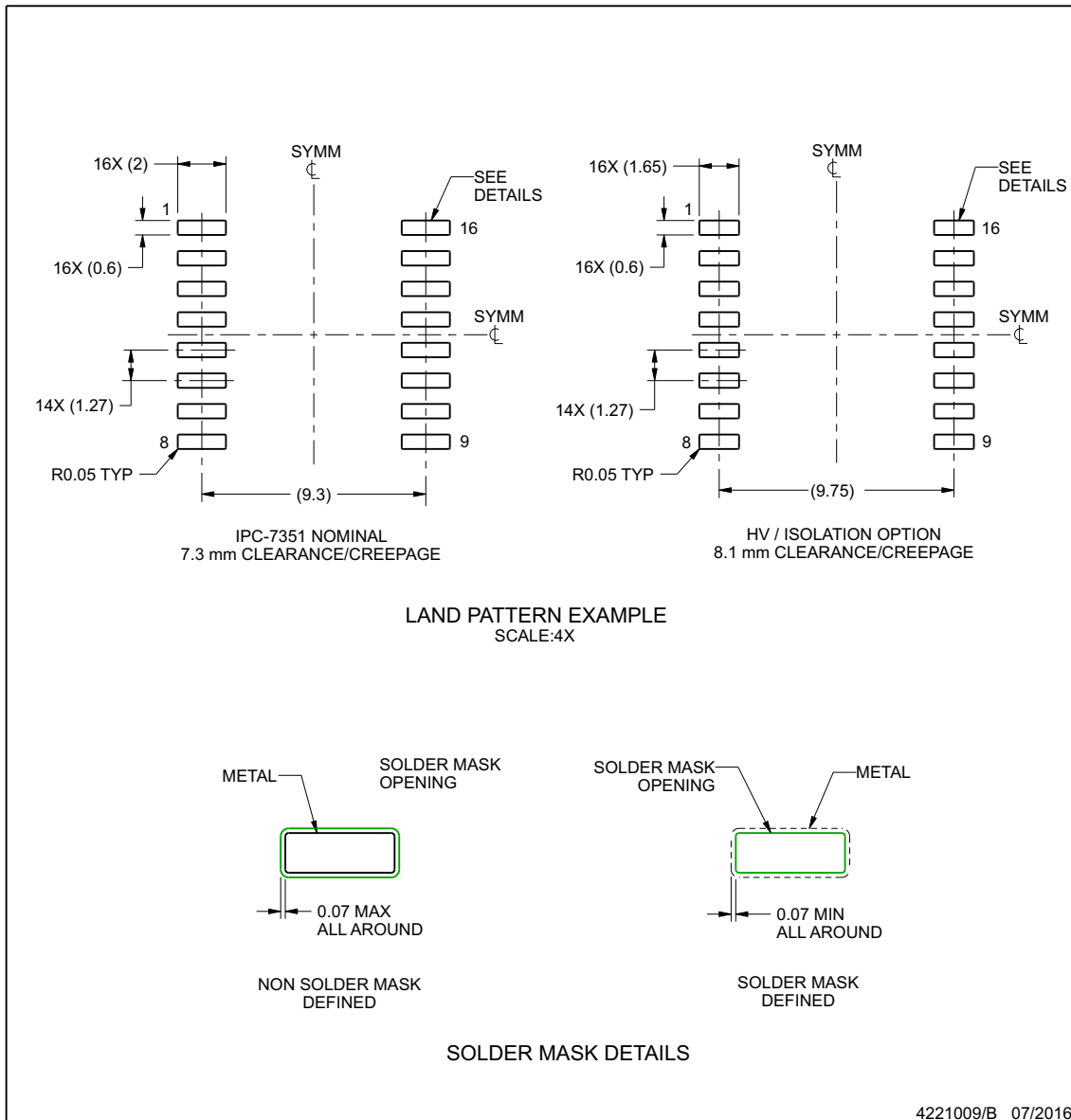
www.ti.com

## EXAMPLE BOARD LAYOUT

**DW0016B**

**SOIC - 2.65 mm max height**

SOIC



NOTES: (continued)

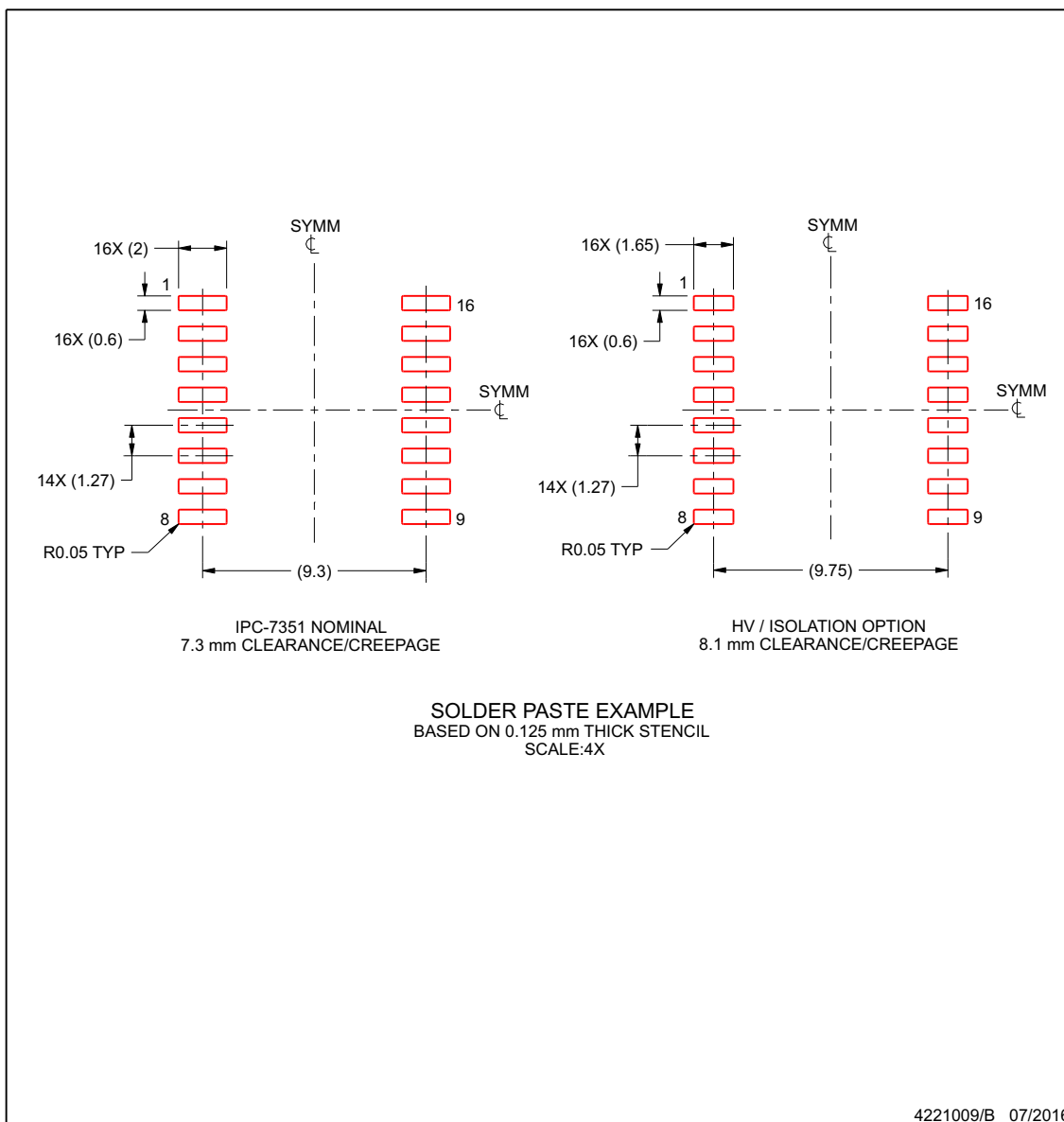
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DW0016B**

**SOIC - 2.65 mm max height**

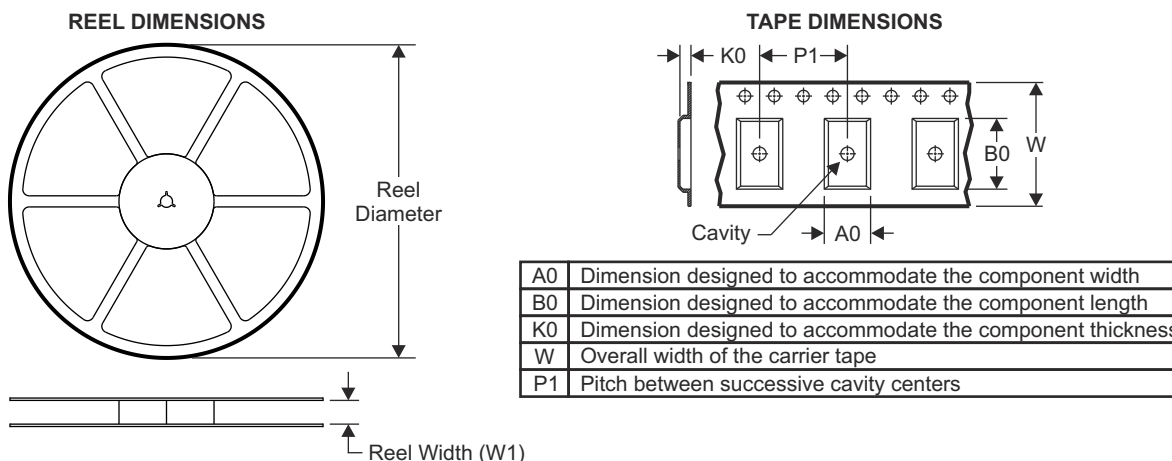
SOIC



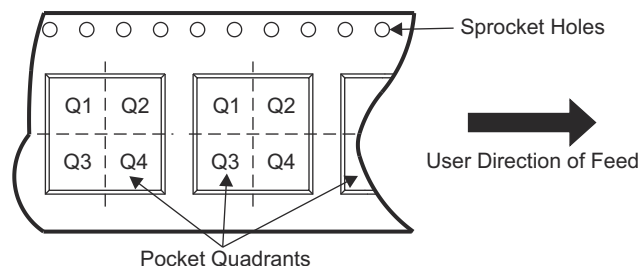
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 11.1 Tape and Reel Information

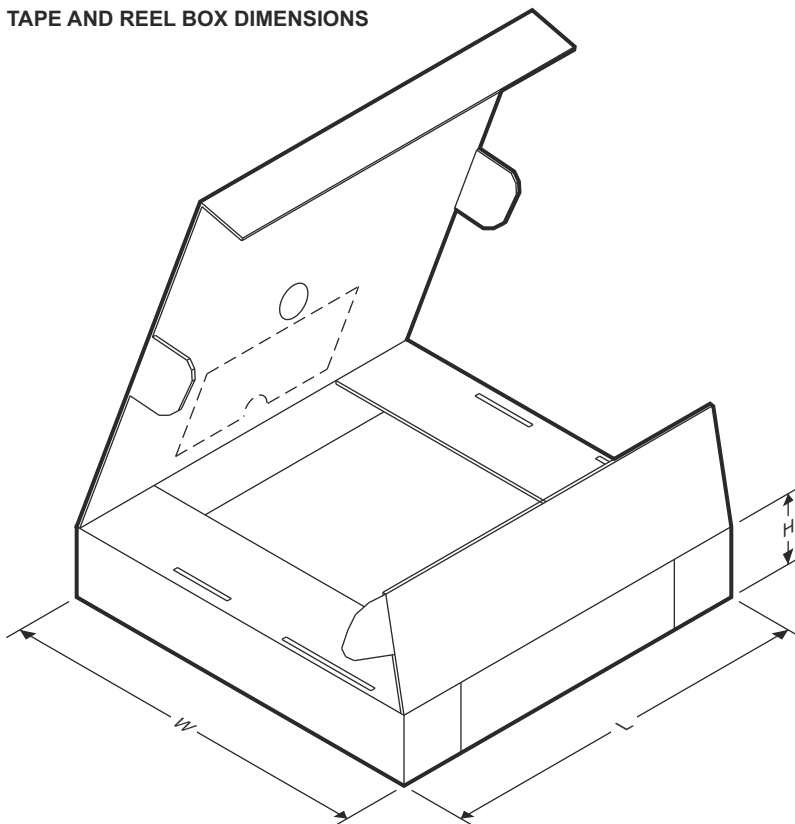


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device          | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO7741FTADWRQ1 | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |
| ISO7741FTBDWRQ1 | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |
| ISO7741TADWRQ1  | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |
| ISO7742TBDWRQ1  | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |
| ISO7742FTADWRQ1 | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |
| ISO7742FTBDWRQ1 | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |
| ISO7742TADWRQ1  | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |
| ISO7742TBDWRQ1  | SOIC         | DW              | 16   |     | 330                | 16.4               | 10.75   | 10.7    | 2.7     | 12      | 16     | Q1            |

TAPE AND REEL BOX DIMENSIONS



| Device          | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| ISO7741FTADWRQ1 | SOIC         | DW              | 16   |     | 367         | 367        | 45          |
| ISO7741FTBDWRQ1 | SOIC         | DW              | 16   |     | 367         | 367        | 45          |
| ISO7741TADWRQ1  | SOIC         | DW              | 16   |     | 367         | 367        | 45          |
| ISO7741TBDWRQ1  | SOIC         | DW              | 16   |     | 367         | 367        | 45          |
| ISO7742FTADWRQ1 | SOIC         | DW              | 16   |     | 367         | 367        | 45          |
| ISO7742FTBDWRQ1 | SOIC         | DW              | 16   |     | 367         | 367        | 45          |
| ISO7742TADWRQ1  | SOIC         | DW              | 16   |     | 367         | 367        | 45          |
| ISO7742TBDWRQ1  | SOIC         | DW              | 16   |     | 367         | 367        | 45          |

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">ISO7741FTADWRQ1</a> | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741FTA          |
| ISO7741FTADWRQ1.A               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741FTA          |
| <a href="#">ISO7741FTBDWRQ1</a> | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741FTB          |
| ISO7741FTBDWRQ1.A               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741FTB          |
| <a href="#">ISO7741TADWRQ1</a>  | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741TA           |
| ISO7741TADWRQ1.A                | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741TA           |
| <a href="#">ISO7741TBDWRQ1</a>  | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741TB           |
| ISO7741TBDWRQ1.A                | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7741TB           |
| <a href="#">ISO7742FTADWRQ1</a> | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742FTA          |
| ISO7742FTADWRQ1.A               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742FTA          |
| <a href="#">ISO7742FTBDWRQ1</a> | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742FTB          |
| ISO7742FTBDWRQ1.A               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742FTB          |
| <a href="#">ISO7742TADWRQ1</a>  | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742TA           |
| ISO7742TADWRQ1.A                | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742TA           |
| <a href="#">ISO7742TBDWRQ1</a>  | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742TB           |
| ISO7742TBDWRQ1.A                | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | ISO7742TB           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

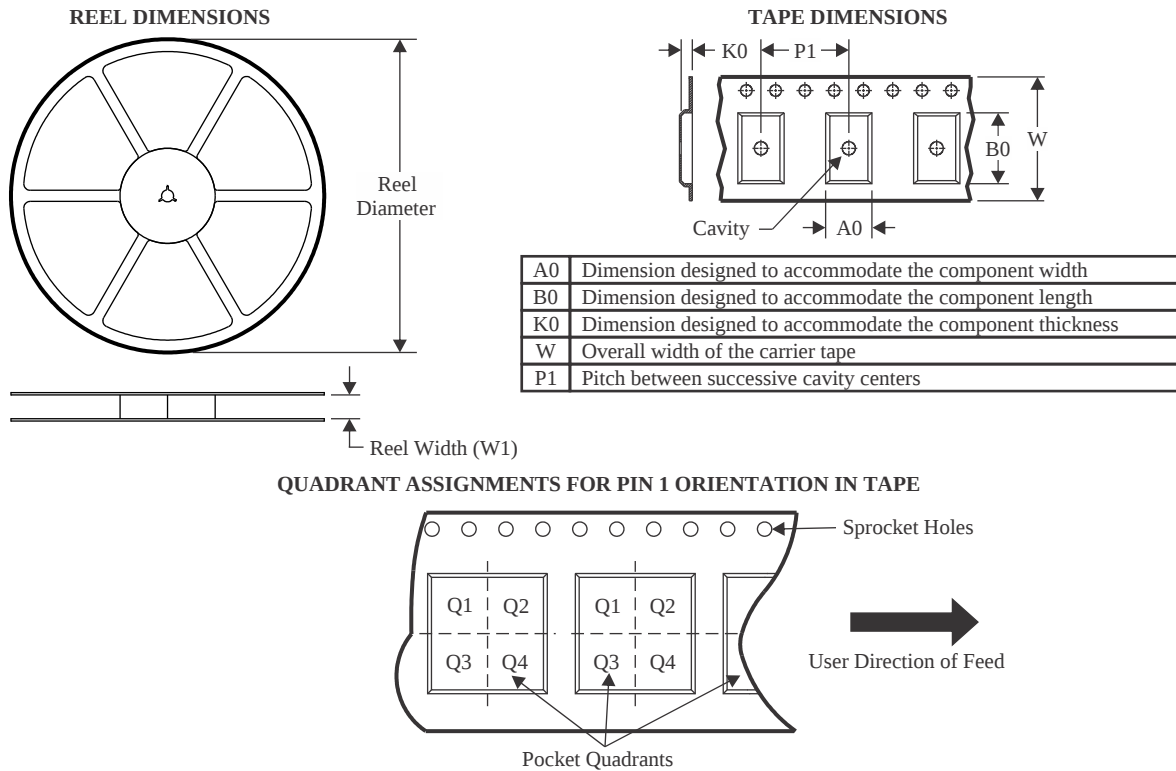
**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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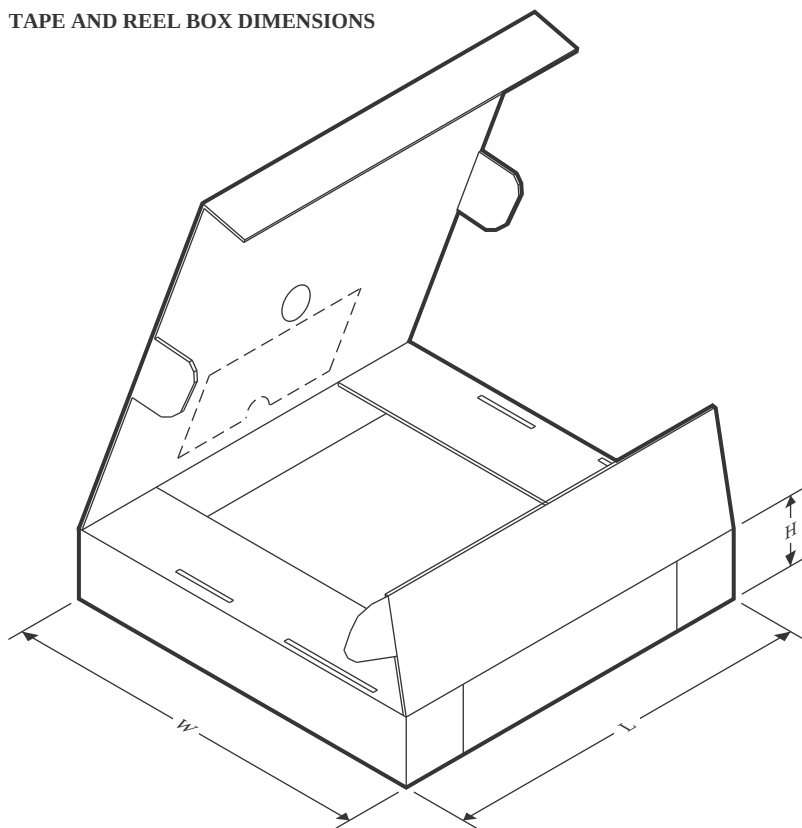
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO7741FTBWRQ1  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7741TADWRQ1  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7741TBDWRQ1  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7742FTADWRQ1 | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7742FTBWRQ1  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7742TADWRQ1  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| ISO7742TBDWRQ1  | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO7741FTBWRQ1  | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| ISO7741TADWRQ1  | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| ISO7741TBDWRQ1  | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| ISO7742FTADWRQ1 | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| ISO7742FTBWRQ1  | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| ISO7742TADWRQ1  | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| ISO7742TBDWRQ1  | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

## GENERIC PACKAGE VIEW

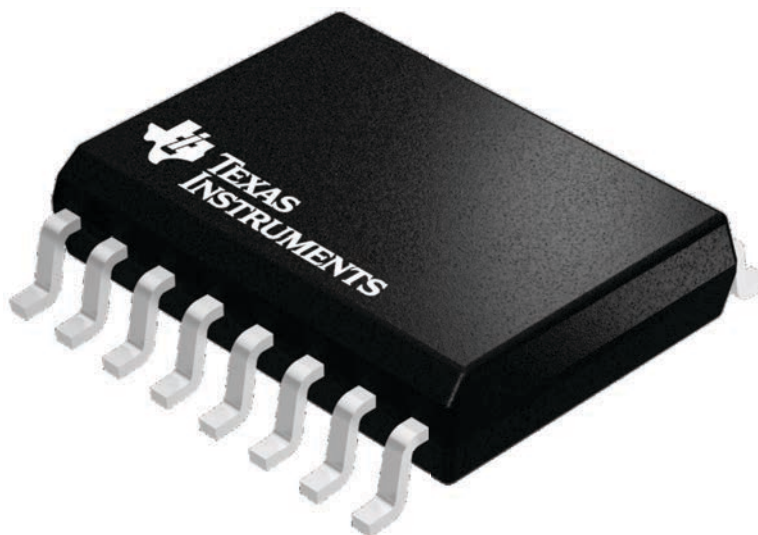
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

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