

Mobile Pixel Link (MPL) Display Interface Serializer and Deserializer

Check for Samples: [LM2502](#)

FEATURES

- >300 Mbps Dual Link Raw Throughput
- MPL Physical Layer (MPL-0)
- Pin Selectable Master / Slave Mode
- Frequency Reference Transport
- Complete LVCMOS / MPL Translation
- Interface Modes:
 - 16-bit CPU, i80 or m68 Style
 - RGB565 with Glue Logic
- –30°C to 85°C Operating Range
- Link Power Down Mode Reduces $I_{DDZ} < 10 \mu A$
- Dual Display Support (CS1* & CS2*)
- Via-less MPL Interconnect Feature
- 3.0V Supply Voltage (V_{DD} and V_{DDA})
- Interfaces to 1.7V to 3.3V Logic (V_{DDIO})

SYSTEM BENEFITS

- Small Interface
- Low Power
- Low EMI
- Frequency Reference Transport
- Intrinsic Level Translation

DESCRIPTION

The LM2502 device is a dual link display interface SERDES that adapts existing CPU / video busses to a low power current-mode serial MPL link. The chipset may also be used for a RGB565 application with glue logic. The interconnect is reduced from 22 signals to only 3 active signals with the LM2502 chipset easing flex interconnect design, size and cost.

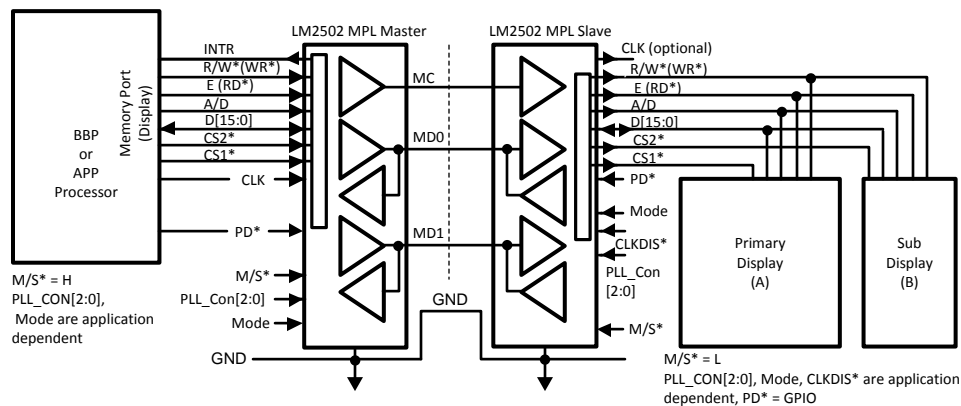
The Master Serializer (SER) resides beside an application processor or baseband processor and translates a parallel bus from LVCMOS levels to serial MPL levels for transmission over a flex cable and PCB traces to the Slave Deserializer (DES) located near the display module.

Dual display support is provided for a primary and sub display through the use of two ChipSelect signals. A Mode pin selects either a i80 or m68 style interface.

The Power_Down (PD*) input controls the power state of the MPL interface. When PD* is asserted, the MD1/0 and MC signals are powered down to save current.

The LM2502 implements the physical layer of the MPL Standard (MPL-0). The LM2502 is offered in NOPB (Lead-free) NFBGA and WQFN packages.

Typical Application Diagram



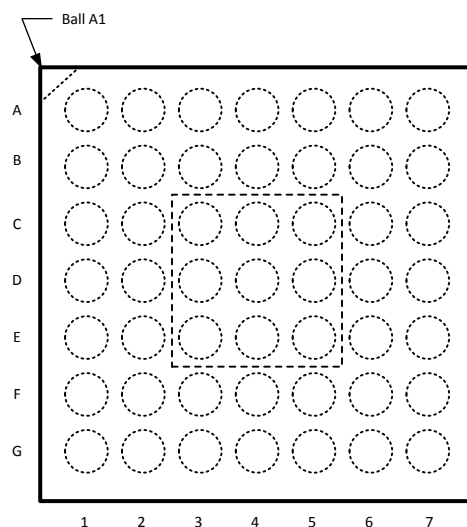
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2013, Texas Instruments Incorporated

NFBGA Connection Diagram



TOP VIEW
(not to scale)

Table 1. Ball Assignment⁽¹⁾

| Ball # | Master | Slave | | Ball # | Master | Slave |
|--------|-------------------|-------------------|--|--------------------|---------------------|---------------------|
| A1 | D0 | D0 | | D5 | NC | NC |
| A2 | D1 | D1 | | D6 | V _{SScore} | V _{SScore} |
| A3 | D2 | D2 | | D7 | V _{DDcore} | V _{DDcore} |
| A4 | V _{DDA} | V _{DDA} | | E1 | D8 | D8 |
| A5 | INTR | CLKDIS* | | E2 | D9 | D9 |
| A6 | MD1 | MD0 | | E3 | NC | NC |
| A7 | MC | MC | | E4 | NC | NC |
| B1 | D3 | D3 | | E5 | NC | NC |
| B2 | D4 | D4 | | E6 | CS1* | CS1* |
| B3 | D5 | D5 | | E7 | PLLCON2 | PLLCON2 |
| B4 | V _{SSA} | V _{SSA} | | F1 | D10 | D10 |
| B5 | M/S* | M/S* | | F2 | D11 | D11 |
| B6 | Mode | Mode | | F3 | D12 | D12 |
| B7 | MD0 | MD1 | | F4 | V _{SSIO} | V _{SSIO} |
| C1 | D6 | D6 | | F5 | MF0 | MF0 |
| C2 | D7 | D7 | | F6 | PLLCON1 | PLLCON1 |
| C3 | NC | NC | | F7 | PD* | PD* |
| C4 | NC | NC | | G1 | D13 | D13 |
| C5 | NC | NC | | G2 | D14 | D14 |
| C6 | CS2* | CS2* | | G3 | D15 | D15 |
| C7 | MF1 | MF1 | | G4 | V _{DDIO} | V _{DDIO} |
| D1 | V _{DDIO} | V _{DDIO} | | G5 | A/D | A/D |
| D2 | V _{SSIO} | V _{SSIO} | | G6 | PLLCON0 | PLLCON0 |
| D3 | NC | NC | | G7 | CLK | CLK |
| D4 | NC | NC | | NC = Not Connected | | |

(1) Note: Three pins are different between Master and Slave configurations - see also [Figure 17](#)

WQFN Connection Diagram

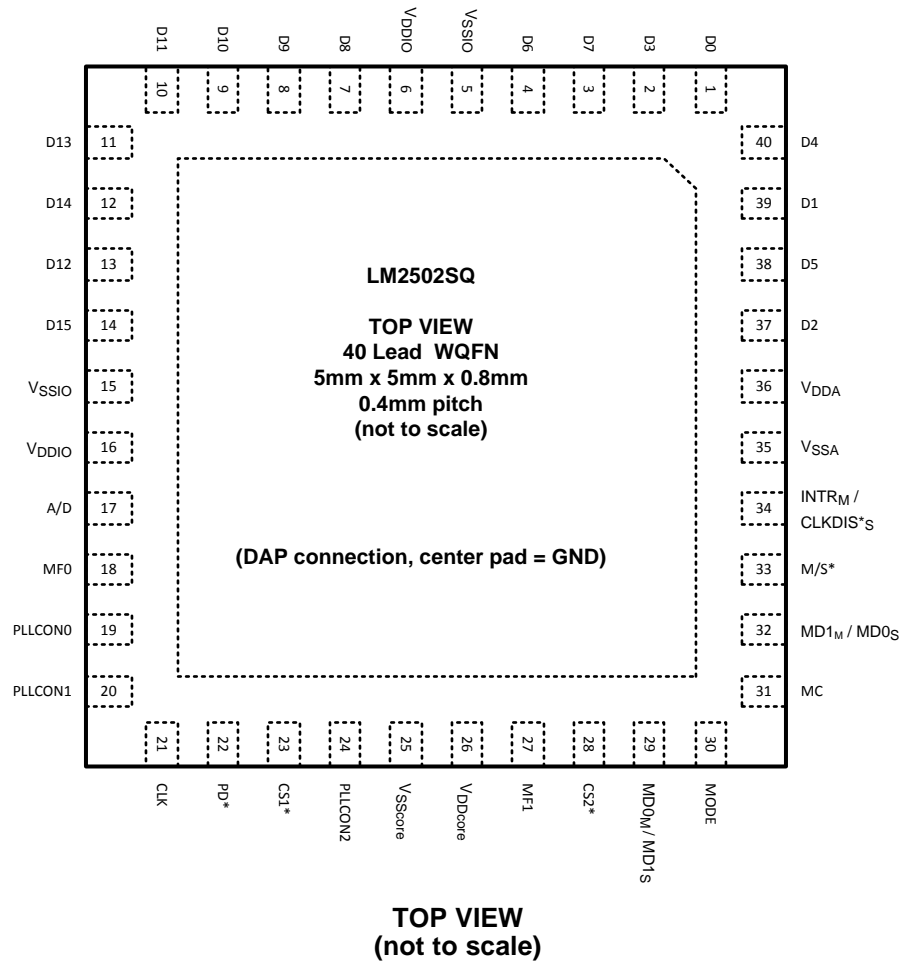


Table 2. Pad Assignment⁽¹⁾

| Pin # | Master | Slave | | Ball # | Master | Slave |
|-------|-------------------|-------------------|--|--------|-------------------------|----------------------------|
| 1 | D0 | D0 | | 21 | CLK | CLK |
| 2 | D3 | D3 | | 22 | PD* | PD* |
| 3 | D7 | D7 | | 23 | CS1* | CS1* |
| 4 | D6 | D6 | | 24 | PLLCON2 | PLLCON2 |
| 5 | V _{SSIO} | V _{SSIO} | | 25 | V _{SScore} | V _{SScore} |
| 6 | V _{DDIO} | V _{DDIO} | | 26 | V _{DDcore} | V _{DDcore} |
| 7 | D8 | D8 | | 27 | MF1 | MF1 |
| 8 | D9 | D9 | | 28 | CS2* | CS2* |
| 9 | D10 | D10 | | 29 | MD0_M | MD1_S |
| 10 | D11 | D11 | | 30 | MODE | MODE |
| 11 | D13 | D13 | | 31 | MC | MC |
| 12 | D14 | D14 | | 32 | MD1_M | MD0_S |
| 13 | D12 | D12 | | 33 | M/S* | M/S* |
| 14 | D15 | D15 | | 34 | INTR_M | CLKDIS*_S |
| 15 | V _{SSIO} | V _{SSIO} | | 35 | V _{SSA} | V _{SSA} |
| 16 | V _{DDIO} | V _{DDIO} | | 36 | V _{DDA} | V _{DDA} |
| 17 | A/D | A/D | | 37 | D2 | D2 |
| 18 | MF0 | MF0 | | 38 | D5 | D5 |
| 19 | PLLCON0 | PLLCON0 | | 39 | D1 | D1 |
| 20 | PLLCON1 | PLLCON1 | | 40 | D4 | D4 |
| DAP | GND | GND | | DAP | GND | GND |

(1) Note: Three pins are different between Master and Slave configurations.

Pin Descriptions

| Pin Name | No. of Pins | I/O, Type ⁽¹⁾ | Description | |
|---------------------------------|-------------|--------------------------|---|---|
| | | | Master (SER) | Slave (DES) |
| MPL SERIAL BUS PINS | | | | |
| MD[1:0] | 2 | IO, MPL | MPL Data Line Driver/Receiver | MPL Data Receiver/Line Driver |
| MC | 1 | IO, MPL | MPL Clock Line Driver | MPL Clock Receiver |
| V _{SSA} | | Ground | MPL Ground - see Power/Ground Pins | MPL Ground - see Power/Ground Pins |
| CONFIGURATION/PARALLEL BUS PINS | | | | |
| M/S* | 1 | I, LVCMOS | Master/Slave* Input, M/S* = H for Master | Master/Slave* Input M/S* = L for Slave |
| PD* | 1 | I, LVCMOS | Power_Down* Input, H = Active L = Power Down Mode | Power_Down* Input, H = Active L = Power Down Mode |
| MF0 (E or RD*) | 1 | IO, LVCMOS | Multi-function Input Zero (0): If MODE = L (m68 mode), E input pin, data is latched on E High-to-Low transition or E may be static High and Data is latched on CS* Low-to-High edge If MODE = H (i80 mode), Read Enable input pin, active low. Read data is driven when both RD* and CS* are Low. | Multi-function Output Zero (0): If MODE = L (m68 mode), E output pin, static High. If MODE = H (i80 mode), Read Enable output pin, active Low. |
| MF1 (R/W* or WR*) | 1 | IO, LVCMOS | Multi-function Input One (1): If Mode = L (m68 mode), Read/Write* pin, Read High, Write* Low If Mode = H (i80 mode), Write* enable input pin, active Low. Write data is latched on the Low-to-High transition of either WR* or CS* (which ever occurs first). | Multi-function Output One (1): If Mode = L (m68 mode) Read/Write* pin, Read High, Write* Low If Mode = H (i80 mode) Write* enable output pin, active Low. |

(1) Note: I = Input, O = Output, IO = Input/Output, V_{DDIO} ≤ V_{DD} (V_{DDA} = V_{DDcore}). Do not float input pins.

Pin Descriptions (continued)

| Pin Name | No. of Pins | I/O, Type ⁽¹⁾ | Description | |
|--------------------------|-------------|--------------------------|---|---|
| | | | Master (SER) | Slave (DES) |
| CS1* | 1 | IO, LVCMOS | ChipSelect1* – Input H = Ignored L = Active | ChipSelect1* – Output H = Ignored L = Active |
| CS2* | 1 | IO, LVCMOS | ChipSelect2* – Input H = Ignored L = Active | ChipSelect2* – Output H = Ignored L = Active |
| A/D (RS or A0) | 1 | IO, LVCMOS | Address/Data – Input H = Data L = Address (Command) | Address/Data – Output H = Data L = Address (Command) |
| D[15:0] | 16 | IO, LVCMOS | Data Bus – Inputs/Outputs | Data Bus – Outputs/Inputs |
| INTR or CLKDIS* | 1 | O or I, LVCMOS | INTR is asserted when the read data is ready and de-asserted upon a second CPU Read cycle. | Clock Disable - CLKDIS*: H = CLK output ON L = CLK output LOW, allows for the Slave clock output to be held static if not used. |
| CLK | 1 | IO, LVCMOS | Clock Input | Clock Output (Frequency Reference) – no phase relationship to data – frequency reference only. |
| Mode | 1 | I, LVCMOS | Mode Input Pin H = i80 Mode, L = m68 Mode | Mode Input Pin H = i80 Mode, L = m68 Mode |
| PLL_CON [2:0] | 3 | I, LVCMOS | PLL Configuration Input Pins – see Table 12 | Clock Divisor Configuration Input Pins – see Table 12 |
| POWER/GROUND PINS | | | | |
| V _{DDA} | 1 | Power | Power Supply Pin for the MPL Interface. 2.9V to 3.3V | |
| V _{SSA} | 1 | Ground | Ground Pin for the MPL Interface, a low impedance ground path is required between the Master and the Slave device - see Applications Information section. | |
| V _{DDcore} | 1 | Power | Power Supply Pin for the digital core. 2.9V to 3.3V | |
| V _{SScore} | 1 | Ground | Ground Pin for the digital core. | |
| V _{DDIO} | 2 | Power | Power Supply Pin for the parallel interface. 1.7V to 3.3V | |
| V _{SSIO} | 2 | Ground | Ground Pin for the parallel interface. | |
| | 9 | NC | Not Connected (C3-5, D3-5, E3-5). NFBGA Package only. | |
| | 1 | Ground | DAP = Ground. WQFN Package only. | |

Table 3. Master Pinout - NFBGA Package

| MST | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|-----|-------------------|-------------------|-----|-------------------|------|---------------------|---------------------|
| A | D0 | D1 | D2 | V _{DDA} | INTR | MD1 | MC |
| B | D3 | D4 | D5 | V _{SSA} | M/S* | Mode | MD0 |
| C | D6 | D7 | NC | NC | NC | CS2* | MF1 |
| D | V _{DDIO} | V _{SSIO} | NC | NC | NC | V _{SScore} | V _{DDcore} |
| E | D8 | D9 | NC | NC | NC | CS1* | PLLCON2 |
| F | D10 | D11 | D12 | V _{SSIO} | MF0 | PLLCON1 | PD* |
| G | D13 | D14 | D15 | V _{DDIO} | A/D | PLLCON0 | CLK |

Table 4. Slave Pinout - NFBGA Package

| SLV | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|-----|-------------------|-------------------|----|------------------|---------|---------------------|---------------------|
| A | D0 | D1 | D2 | V _{DDA} | CLKDIS* | MD0 | MC |
| B | D3 | D4 | D5 | V _{SSA} | M/S* | Mode | MD1 |
| C | D6 | D7 | NC | NC | NC | CS2* | MF1 |
| D | V _{DDIO} | V _{SSIO} | NC | NC | NC | V _{SScore} | V _{DDcore} |
| E | D8 | D9 | NC | NC | NC | CS1* | PLLCON2 |

Table 4. Slave Pinout - NFBGA Package (continued)

| SLV | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|-----|-----|-----|-----|-------------------|-----|---------|-----|
| F | D10 | D11 | D12 | V _{SSIO} | MF0 | PLLCON1 | PD* |
| G | D13 | D14 | D15 | V _{DDIO} | A/D | PLLCON0 | CLK |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

| | | |
|---|---------------------------------|--------------------------------------|
| Supply Voltage (V _{DDA}) | | –0.3V to +4.0 V |
| Supply Voltage (V _{DD}) | | –0.3V to +4.0 V |
| Supply Voltage (V _{DDIO}) | | –0.3V to +4.0 V |
| LVCMOS Input/Output Voltage | | –0.3V to (V _{DDIO} + 0.3) V |
| MPL Input/Output Voltage | | –0.3V to (V _{DDA} + 0.3) V |
| Junction Temperature | | +150 °C |
| Storage Temperature | | –65°C to +150 °C |
| Lead Temperature Soldering, 40 Seconds | | +260 °C |
| ESD Ratings: | HBM, 1.5 kΩ, 100pF | ≥±2 kV |
| | EIAJ, 0Ω, 200 pF | ≥±200 V |
| Maximum Package Power Dissipation Capacity at 25°C | NFBGA Package ⁽³⁾ | 2.5 W |
| | Derate NFBGA Package above 25°C | 25 mW/°C |
| | Theta JA | 45 °C/W |
| | WQFN Package ⁽³⁾ | 1.39 W |
| | Derate WQFN Package above 25°C | 11 mW/°C |
| | Theta JA | 90 °C/W |

- (1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) NFBGA assumes 4 layer PCB, WQFN assumes 2 layer PCB for thermal calculations.

RECOMMENDED OPERATING CONDITIONS

| | | Min | Typ | Max | Units |
|---------------------|---|-----|-----|-----|-------|
| Supply Voltage | V _{DDA} to V _{SSA} and V _{DDcore} to V _{SScore} | 2.9 | 3.0 | 3.3 | V |
| | V _{DDIO} to V _{SSIO} | 1.7 | | 3.3 | V |
| Clock Frequency | | 3.0 | | 26 | MHz |
| Ambient Temperature | | –30 | 25 | 85 | °C |

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified. ^{(1) (2)}

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---------------------------------|--|--|---|-----------------------|--------------------|------------------------|-------|
| MPL | | | | | | | |
| I _{OLL} | Logic Low Current (5X I _B) | | | 3.67 I _B | 5.0 I _B | 6.33 I _B | μA |
| I _{OMS} | Mid Scale Current | | | | 3.0 I _B | | μA |
| I _{OLH} | Logic High Current (1X I _B) | | | 0.7 I _B | 1.0 I _B | 1.3 I _B | μA |
| I _B | Current Bias | | | | 150 | | μA |
| I _{OFF} | MPL Leakage Current | PD* = L (PowerDown mode) | | -2 | 0 | +2 | μA |
| LVCMOS (1.7V to 3.3V Operation) | | | | | | | |
| V _{IH} | Input Voltage High Level | V _{DDIO} = 2.0V to 3.3V | | 0.7 V _{DDIO} | | V _{DDIO} +0.3 | V |
| | | V _{DDIO} = 1.7V to <2.0V | | 0.8 V _{DDIO} | | | |
| V _{IL} | Input Voltage Low Level | V _{DDIO} = 2.0V to 3.3V | | -0.3 | | 0.3 V _{DDIO} | V |
| | | V _{DDIO} = 1.7V to <2.0V | | -0.3 | | 0.2 V _{DDIO} | V |
| V _{HY} | Input Hysteresis | V _{DDIO} = 3.0V | | | 500 | | mV |
| | | V _{DDIO} = 1.8V | | | 300 | | mV |
| I _{IN} | Input Current (includes I _{OZ}) | LVCMOS IO Signals | | -2 | 0 | +2 | μA |
| I _{IH} | Input Current High Level | LVCMOS Input Only Signals (i.e. Mode) | | -1 | 0 | +1 | μA |
| I _{IL} | Input Current Low Level | | | -1 | 0 | +1 | μA |
| V _{OH} | Output Voltage High Level | I _{OH} = -2 mA | V _{DDIO} = 3.3V | 0.8 V _{DDIO} | 2.8 | | V |
| | | | V _{DDIO} = 1.7V | | 1.6 | | |
| V _{OL} | Output Voltage Low Level | I _{OL} = 2 mA | V _{DDIO} = 3.3V | | 0.08 | 0.2 V _{DDIO} | V |
| | | | V _{DDIO} = 1.7V | | 0.12 | | |
| I _{OS} | Output Short-Circuit Current | V _{OUT} = 0V, V _{DDIO} = 1.7 V | | | -5 | | mA |
| | | V _{OUT} = 0V, V _{DDIO} = 3.3 V | | | -30 | | mA |
| SUPPLY CURRENT | | | | | | | |
| I _{DD} | Total Supply Current—Enabled Conditions: MC = 76.8 MHz, MD = 1010-0101 pattern (worse case toggle, rail-to-rail levels), CLK = 19.2 MHz (4X) ⁽³⁾ | Master | V _{DDIO} | | 15 | 220 | μA |
| | | | V _{DD} = V _{DDA} | | 14 | 25 | mA |
| | | Slave, C _L = 10 pF | V _{DDIO} | | 1.5 | 9.0 | mA |
| | | | V _{DD} = V _{DDA} | | 9.0 | 13.0 | mA |
| | Total Supply Current—Enabled Conditions: MC = 20 MHz, MD = 1010-0101 pattern (worse case toggle, rail-to-rail levels), CLK = 5 MHz (4X) | Master | V _{DDIO} = 1.8V | | 10 | | μA |
| | | | V _{DD} = V _{DDA} = 3V | | 5 | | mA |
| | | Slave, C _L = 10 pF | V _{DDIO} = 1.8V | | 1 | | mA |
| | | | V _{DD} = V _{DDA} = 3V | | 4 | | mA |
| I _{DDZ} | Supply Current—Disabled | Power_Down Mode, PD* = 0V | | | 1 | 10 | μA |

(1) Typical values are given for $V_{DDIO} = 1.8V$ and $V_{DD} = V_{DDA} = 3.0V$ and $T_A = 25^\circ C$.

(2) Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

(3) Typical supply condition is $V_{DDIO} = 1.8V$ and $V_{DD} = V_{DDA} = 3.0V$, Maximum supply condition is $V_{DDIO} = V_{DD} = V_{DDA} = 3.3V$ for the I_{DD} parameter.

SWITCHING CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|--|--|--------------------------|-----|------|-----|------------|
| PARALLEL BUS TIMING | | | | | | | |
| t _{SET} | Set Up Time, Data to Edge | Inputs | | 5 | | | ns |
| t _{HOLD} | Hold Time, Edge to Data | | | 5 | | | ns |
| t _{RISE} | Rise Time | See Figure 2, Outputs, C _L = 10 pF Edge sensitive outputs tested only: m68 mode: CS1*, CS2* and CLKout i80 mode: RD*, WR*, and CLKout | V _{DDIO} = 1.7V | 2 | 7 | 14 | ns |
| t _{FALL} | Fall Time | | V _{DDIO} = 3.3V | 1 | 2 | 10 | ns |
| | | | V _{DDIO} = 1.7V | 2 | 6 | 14 | ns |
| | | | V _{DDIO} = 3.3V | 1 | 2 | 10 | ns |
| CLK _{DC} | Output Clock Duty Cycle | CLKDIS* = H, Slave (DES) | | | 50 | | % |
| Parallel Bus Timing - See Figure 13 Figure 14 Figure 15 Figure 16 and Table 7, Table 8, Table 9, and Table 10 | | | | | | | |
| SERIAL BUS TIMING | | | | | | | |
| t _{DVBC} | Data Valid before Clock | Master-to-Slave ⁽²⁾ | | 2.0 | | | ns |
| t _{DVAC} | Data Valid after Clock | | | 0.5 | | | ns |
| POWER UP TIMING ⁽²⁾ | | | | | | | |
| t ₀ | Master PLL Lock Counter | | See Figure 6 | | 4096 | | CLK cycles |
| t ₁ | MC Pulse Width Low (Master) | | | | 11 | | CLK cycles |
| t ₂ | MC Pulse Width HIGH (Master) | | | | 11 | | CLK cycles |
| t ₃ | MC Pulse Width Low (Master) | | | | 11 | | CLK cycles |
| t ₄ | CLK-Out Delay (Slave) | | | | 7 | | MC cycles |
| t ₅ | Power Up Total delay (t ₀ + t ₁ + t ₂ + t ₃ + t ₄) | | | | 4133 | | CLK cycles |
| MPL POWER OFF TIMING | | | | | | | |
| t _{PAZ} | Disable Time to Power Down | See Figure 7, This parameter is functionally tested by the I _{DDZ} parameter. ⁽³⁾ | | | | 50 | ms |

(1) Typical values are given for $V_{DDIO} = 1.8V$ and $V_{DD} = V_{DDA} = 3.0V$ and $T_A = 25^\circ C$.

(2) This parameter is specified by design based on simulation or bench characterization.

(3) This parameter is specified by a ATE tester delay, actual turn off time is faster.

RECOMMENDED INPUT TIMING REQUIREMENTS

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------------|--|-----------------------------|------|-----|-----|-------|
| MASTER REFERENCE CLOCK (CLK) | | | | | | |
| f_{CLK} | Clock Frequency | See Table 12 ⁽²⁾ | 3 | | 26 | MHz |
| t_{CP} | Clock Period | | 38.5 | | 333 | ns |
| CLK_{DC} | Clock Duty Cycle | | 40 | 50 | 60 | % |
| t_T | Clock Transition Times (Rise or Fall, 20%–80%) | | 1 | | 14 | ns |

(1) Typical values are given for $V_{DDIO} = 1.8V$ and $V_{DD} = V_{DDA} = 3.0V$ and $T_A = 25^\circ C$.

(2) This parameter is specified by design based on simulation or bench characterization.

TIMING DIAGRAMS

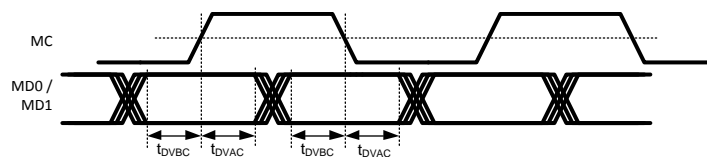


Figure 1. Serial Data Valid—Master to Slave

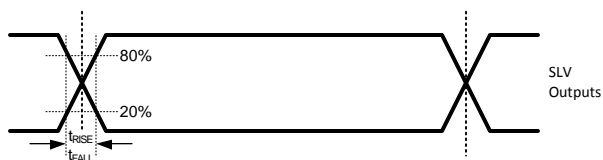


Figure 2. Slave Output Rise and Fall Time

FUNCTIONAL DESCRIPTION

BUS OVERVIEW

The LM2502 is a dual link Transceiver configurable part that supports a 16-bit CPU (m68 or i80) style interface. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver. A maximum raw throughput of 307 Mbps (raw) is possible with this chipset. When the protocol overhead is taken into account, a maximum data throughput of 245 Mbps is possible. The MPL interface is designed for use with common 50Ω to 100Ω lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 20cm.

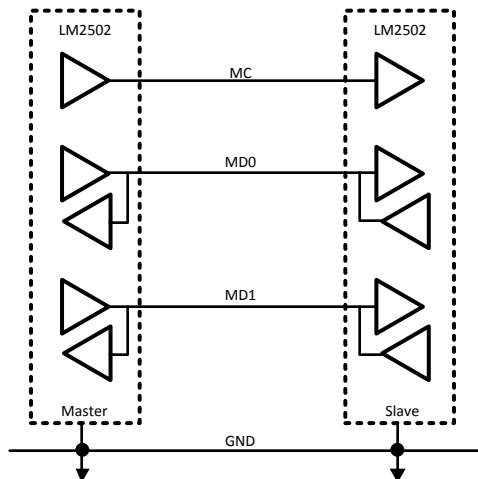


Figure 3. MPL Point-to-Point Bus

SERIAL BUS TIMING

Data valid is relative to both edges for a WRITE as shown in Figure 4. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500ps.

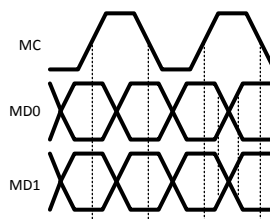


Figure 4. Dual Link Timing (WRITE)

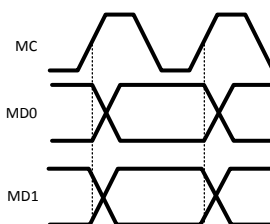


Figure 5. Dual Link Timing (READ)

Data is strobed out on the rising edge by the Slave for a READ as shown in [Figure 5](#). The Master monitors for the start bit transition (Low to High) and selects the best strobe to sample the incoming data on. This is done to account for the round trip delay of the interconnect and application data rate.

SERIAL BUS PHASES

There are four bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. The MPL bus phases are shown in [Table 5](#).

Table 5. Link Phases⁽¹⁾

| Name | | MC State | MDn State | Phase Description | Pre-Phase | Post-Phase |
|--------------|----------------|----------|-----------|---|-------------|------------|
| OFF (O) | | 0 | 0 | Link is Off | A, I or LU | LU |
| IDLE (I) | | A | L | Data is Static (Low) | A or LU | A or O |
| Active (A) | Data Out WRITE | A | X | Data Out (Write) — includes command, Data Out Phases | LU, A, or I | A, I, or O |
| | Data In READ | A | X | Data In (Read) — includes command, TA', Data In, and TA" phases | LU, A, or I | A, I, or O |
| LINK-UP (LU) | Master | H | - | Master initiated Link-Up | O | A, I, or O |

(1) Notes on MC/MD Line State:

0 = no current (off)

L = Logic Low—The higher level of current on the MC and MD lines

H = Logic High—The lower level of current on the MC and MD lines

X = Low or High

A = Active Clock

SERIAL BUS START UP TIMING

In the Serial Bus OFF phase, Master transmitters for MD0, MD1 and MC are turned off such that zero current flows over the MPL lines. In addition, both the Master and the Slave are internally held in a low power state. When the PD* input pins are de-asserted (driven High) the Master enables its PLL and waits for enough time to pass for its PLL to lock. After the Master's PLL is locked ($t_0 = 4,096$ CLK Cycles), the Master will perform an MPL start up sequence. The Slave will also power up and await the start up sequence from the Master.

The MPL start up sequence gives the Slave an opportunity to optimize the current sources in its transceiver to maximize noise margins. The Master begins the sequence by driving the MC line logically Low for 11 CLK cycles (t_1). During this part of the sequence the Slave's transceiver samples the MC current flow and adjusts itself to interpret that amount of current as a logical Low. Next the Master drives the MC line logically HIGH for 11 CLK cycles (t_2). On the Low-to-High transition of the MC – point B – the Slave latches the current source configuration. This optimized configuration is held as long as the MPL remains up. Next, the Master drives both the MC and the MD lines to a logical Low for another 11 CLK cycles (t_3), after which it begins to toggle the MC line at a rate determined by its PLL Configuration pins. The Master will continue to toggle the MC line as long as its PD* pin remains de-asserted (High). At this point the MPL bus may remain in IDLE phase, enter the ACTIVE phase or return to the OFF phase. Active data will occur at the Slave output latency delays (Master + line + Slave) after the data is applied to the Master input. Possible start points are shown by the "C" arrow in [Figure 6](#).

After seven subsequent MC cycles the Slave will start toggling its CLK pin at a rate configured by its CLK Divisor pins.

In the [Figure 6](#) example, an IDLE bus phase is shown until point C, after which the bus is active and the High start bit on MD initiates the transfer of information.

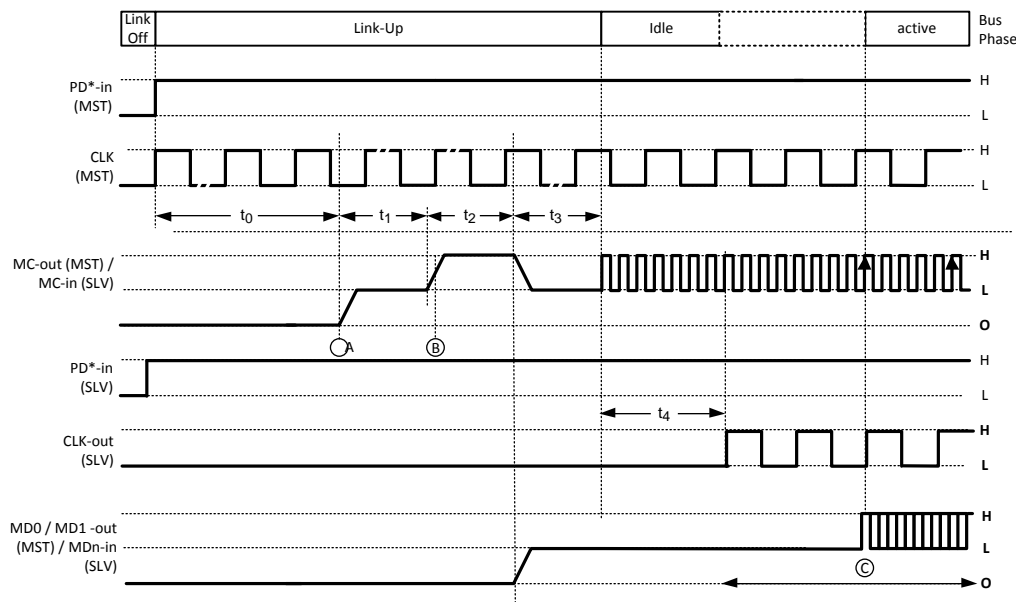


Figure 6. MPL Power Up Timing

OFF PHASE

In the OFF phase, both Master and Slave MPL transmitters are turned off with zero current flowing on the MC and MD lines. Figure 7 shows the transition of the MPL bus into the OFF phase. If an MPL line is driven to a logical Low (high current) when the OFF phase is entered it may temporarily pass through as a logical High (low current) before reaching the zero line current state.

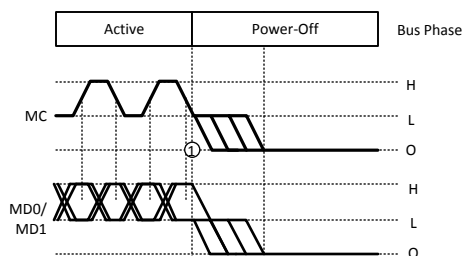


Figure 7. MPL Power Down Timing

The link may be powered down by asserting both the Master's and Slaves's PD* input pins (Low). This causes the devices to immediately put the link to the OFF Phase and internally enter a low power state. To avoid loss of data the Master's PD* input should only be asserted after the MPL bus has been in the IDLE state for at least 20 MC clock cycles. This gives the Slave enough time to complete any write operations received from the MPL bus.

CPU INTERFACE COMPATIBILITY

The CPU Interface mode provides compatibility between a CPU Interface and a small form factor (SFF) Display or other fixed I/O port application. Two options are allowed:

Table 6. Modes

| Mode | Description |
|------|---|
| 0 | m68 Interface (E, R/W*), 16-bit support |
| 1 | i80 Interface (WR*, RD*), 16-bit support |

It is not required that both the Master and the Slave to be configured in the same mode. For example the Master may be configured as an 80xx (i80) interface while the Slave is configured for an 68xx (m68) interface.

Control information is carried over both MD lines. MD0 carries the D0–7 data bits while MD1 the D8–15 data bits. See [Figure 8](#).

WRITE TRANSACTION

The WRITE transaction consists of two MC edges of control information followed by 8 MC edges of write data. Since WRITE transactions transfer information on both edges of MC it takes 5 MC cycles to complete a write transaction. The MD0 line carries the Start bit (High), the A/D (Address/Data) bit and then the data payload of 8 bits (D0–7). The MD1 line carries the R/W* bit (Read/Write*), the CS1/2 bit and then the data payload of 8 bits (D8–15). The data payload is sent least significant bit (LSB) first. The CS1/2 bit denotes which Chipset pin was active. CS1/2 = HIGH designates that CS1* is active (Low). CS1/2 = LOW designates that CS2* is active (Low). CS1* and CS2* LOW is not allowed.

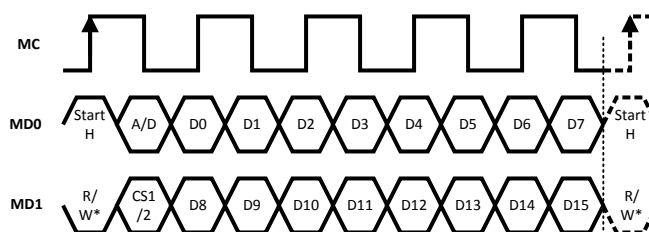


Figure 8. Dual MD Link WRITE Transaction

READ TRANSACTION

The READ transaction is variable in length. It consists of four sections.

In the first section the Master sends a READ_Command to the slave. This command is sent in a single MC cycle (2 edges) and uses a similar format to the 1st cycle of the WRITE transaction. The MD0 line carries the Start bit (High) and the A/D (Address/Data) bit. The MD1 line carries the R/W* bit (High for reads) and the CS1/2 bit.

In the second section (TA') the MD lines are turned around, such that the Master becomes the receiver and Slave becomes the transmitter. The Slave must drive the MD lines low by the 14th clock edge. It may then idle the line at the Logic Low state or drive the line High to indicate that read data transmission is starting. This ensures that the MD lines are a stable LOW state and that the Low-to-High transition of the "Start" bit is seen by the Master.

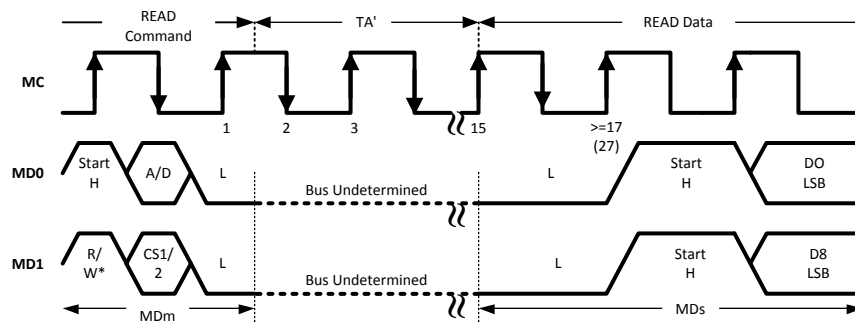


Figure 9. READ_Command and TA'

The third section consists of the transfer of the read data from the Slave to the Master. Note that the READ_Data operates on single-edge strobing (Rising Edge ONLY). Therefore the back channel data signaling rate is $\frac{1}{2}$ of the forward channel (Master-to-Slave direction). When the Slave is ready to transmit data back to the Master it drives the MD lines High to indicate start of read data, followed by 8 MC cycles of the actual read data payload. As in the WRITE command MD0 carries D0–7 and MD1 carries D8–5. The Master monitors for the start bit transition (Low to High) and selects the best strobe to sample the incoming data on. This is done to account for the round trip delay of the interconnect and application data rate.

The Master detects the location of the START bit on MD0 and selects the best strobe for data capture. Skew between the data lines is constrained tighter in the Master-to-Slave direction (Write) than in the Read direction due to the data rate difference. The Master uses its internal clock (multiple phases) to latch the data.

The fourth and final section (TA'') occurs after the read data has been transferred from the Slave to the Master. In the fourth section the MD lines are again turned around, such that the Master becomes the transmitter and the Slave becomes the receiver. The Slave drives the MD lines Low for 1 bit width and then turns off. The MD lines are off momentarily to avoid driver contention. The Master then drives the MD line Low for 1 bit time and then idles the bus until the next transaction is sent.

During a READ transaction (Double Read access on the Master), other MPL transactions are not allowed until the current READ dual cycle is completed.

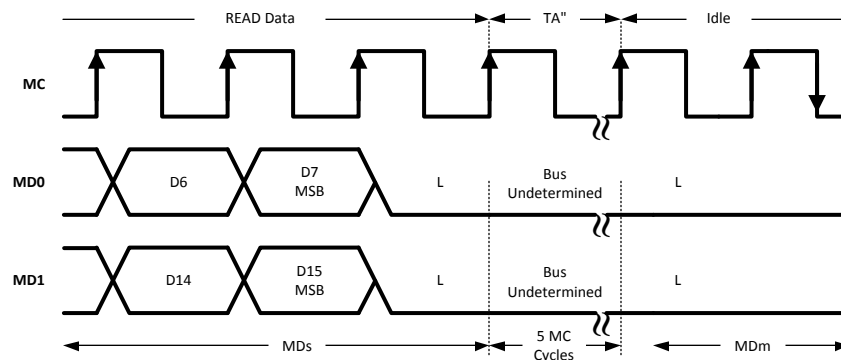


Figure 10. READ_Data and TA''

To account for the latency through the MPL link, a dual READ operation is required by the host. The first read returns invalid data (all Low). Once data has returned to the Master LM2502, the INTR signal is asserted to inform the host to initiate a second read operation. When the Master LM2502 sees the Read signal/CS* combination, it will de-assert the INTR signal and Valid data is presented.

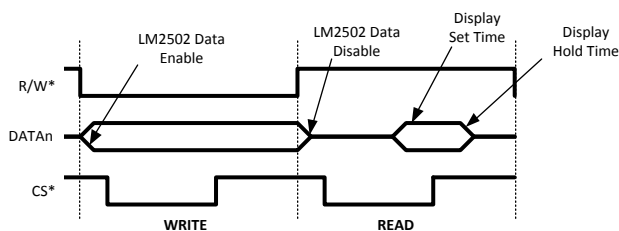


Figure 11. Slave WRITE and Slave READ m68 mode Operation

Figure 11 illustrates a m68 mode WRITE followed by a READ operation (Slave output to Display). At the end of the WRITE operation the SLAVE outputs are turned off. The SLAVE latches in the READ data on the rising edge of the CS* signal as shown. The Display should disable its outputs prior to the next operation to avoid any bus contention.

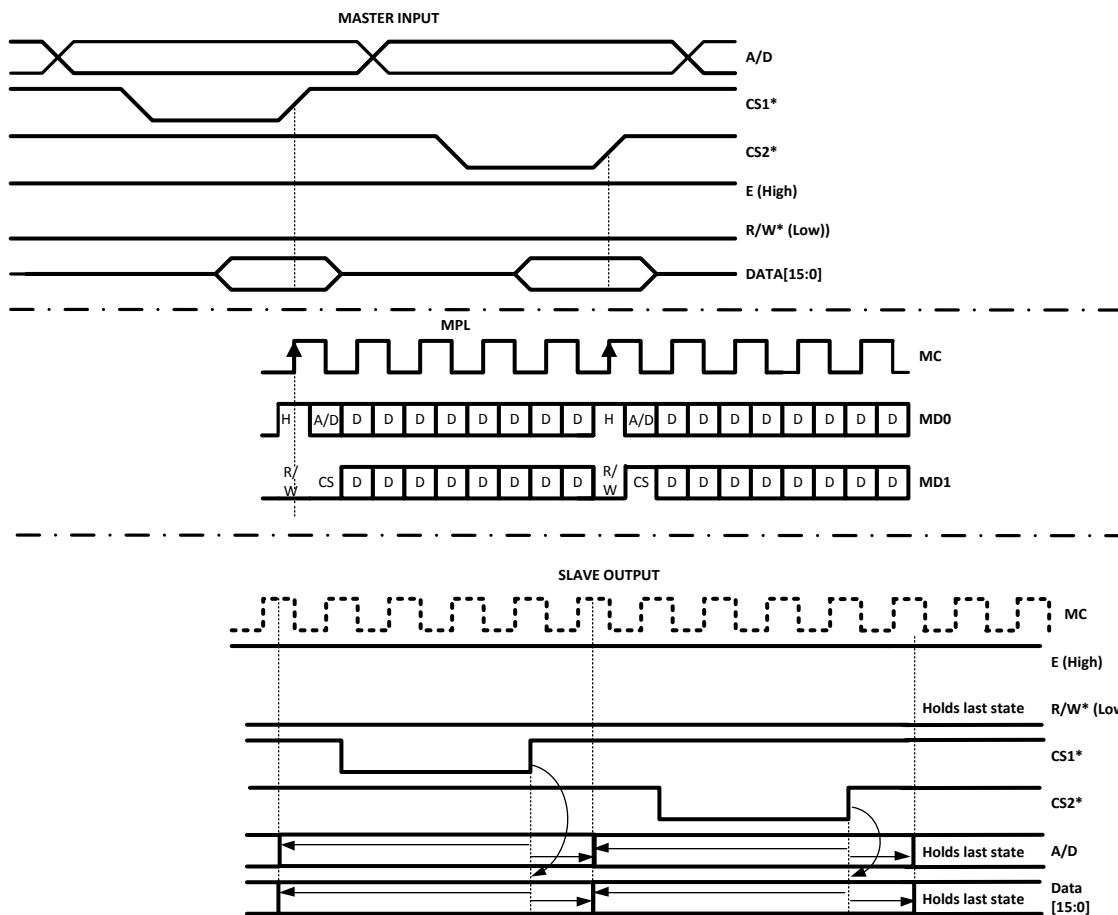
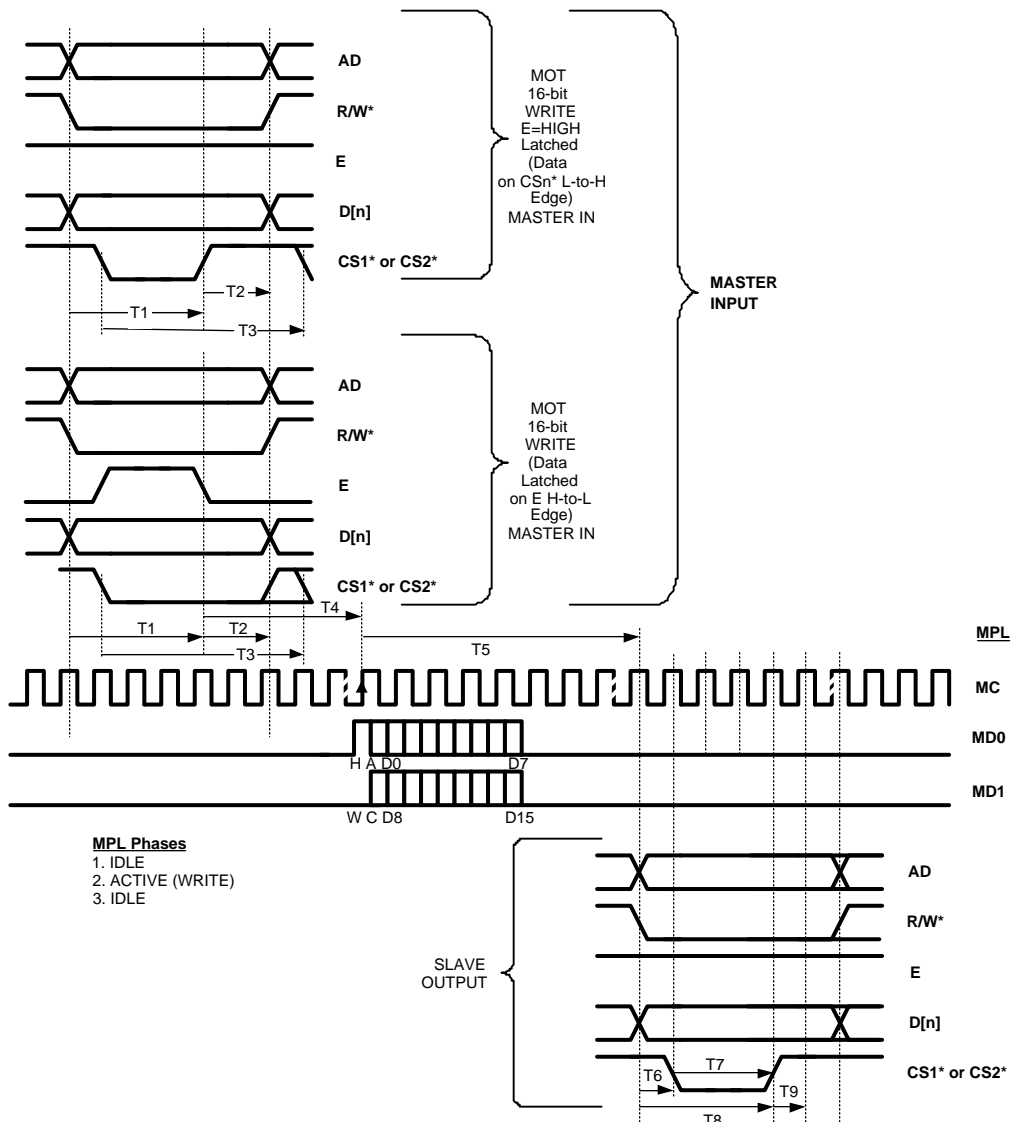


Figure 12. Back-to-Back WRITE Operations—m68 Mode

Figure 12 illustrates a m68 mode WRITE operation to the main display (CS1*) followed by a WRITE operation to the sub display (CS2*). This example shows the maximum operation rate with no idle time between the serial transactions.

CPU MODE—WRITE—m68**Figure 13. WRITE—MOT 6800 μ P Interface****Table 7. WRITE—MOT 6800 μ P Interface Parameters**

| No. | | Parameter | Min | Typ | Max | Units |
|-----|----------|---|-----|-----|-----|-----------|
| T1 | MasterIN | Data Setup Time before ChipSelect* Low-High (or E High-Low) | 5 | | | ns |
| T2 | MasterIN | Data Hold after ChipSelect* Low-High (or E High-Low) | 5 | | | ns |
| T3 | MasterIN | ChipSelect* Recovery Time, ⁽¹⁾ | 6 | | | MC Cycles |
| T4 | Master | Master Latency | | 5 | | MC Cycles |
| T5 | Slave | Slave Latency | | 9 | | MC Cycles |
| T6 | SlaveOUT | Data Valid before ChipSelect* High-Low | | 1 | | MC Cycles |
| T7 | SlaveOUT | ChipSelect* Low Pulse Width | | 3 | | MC Cycles |
| T8 | SlaveOUT | Data Valid before ChipSelect* Low-High | | 4 | | MC Cycles |

(1) This parameter is specified by design based on simulation or bench characterization.

Table 7. WRITE—MOT 6800 μ P Interface Parameters (continued)

| No. | | Parameter | Min | Typ | Max | Units |
|-----|----------|---------------------------------------|-----|-----|-----|-----------|
| T9 | SlaveOUT | Data Valid after ChipSelect* Low-High | | 1 | | MC Cycles |

CPU MODE—READ—m68

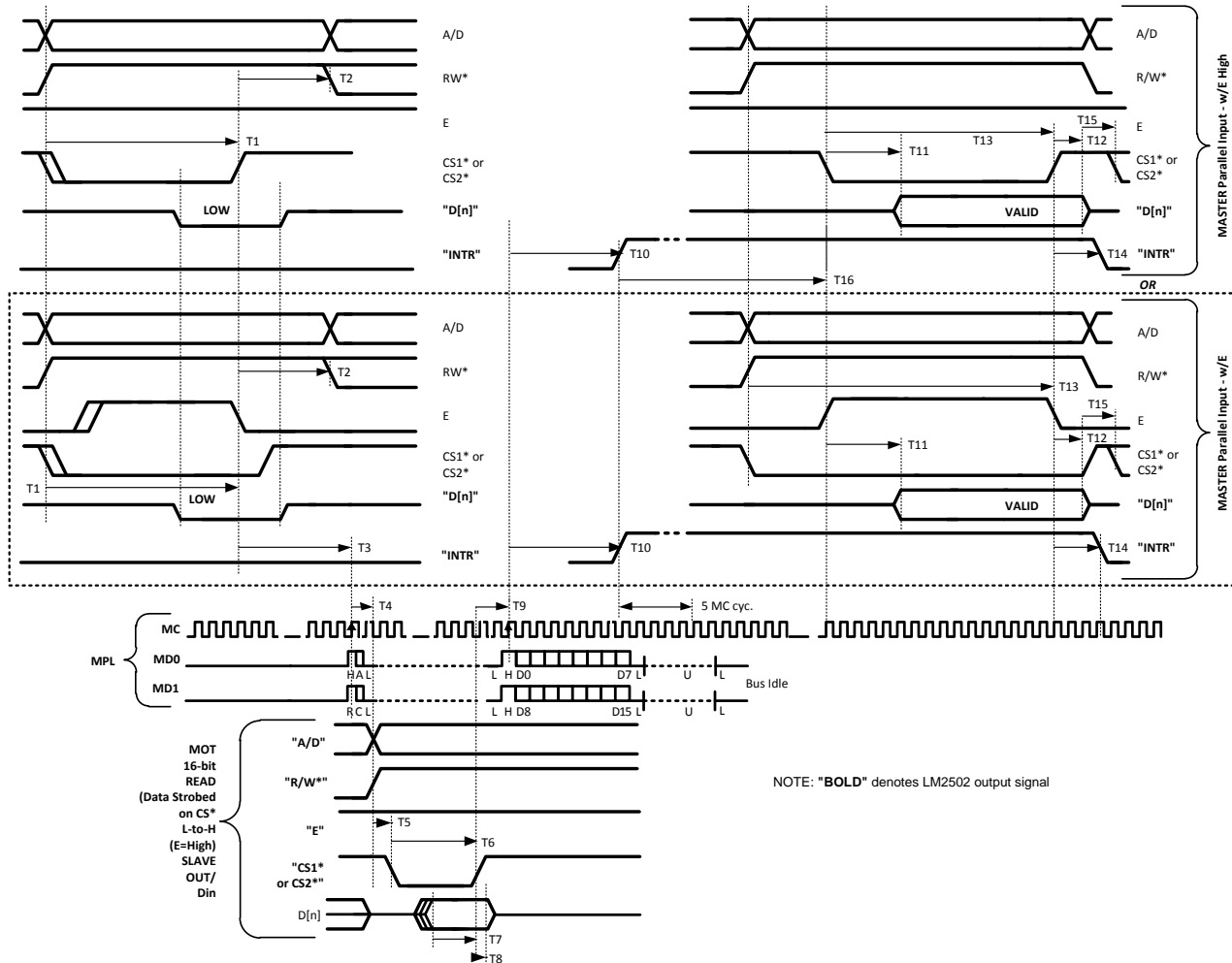


Figure 14. READ—6800 μ P Interface

Table 8. READ—6800 μ P Interface Parameters

| No. | | Parameter | Min | Typ | Max | Units |
|-----|----------|--|-----|-----|-----|-----------|
| T1 | MasterIN | Set Up Time (A/D, R/W*) and Data On Time | 20 | | | ns |
| T2 | MasterIN | Hold Time (A/D, R/W*) and Data Off Time | | 15 | | ns |
| T3 | Master | Master Latency | | 5 | | MC Cycles |
| T4 | Slave | Slave Latency | | 6 | | MC Cycles |
| T5 | Slave | ChipSelect* Delay | | 1 | | MC Cycles |
| T6 | Slave | ChipSelect Low Pulse Width | | 6 | | MC Cycles |
| T7 | Slave | Data Set Up Time | 5 | | | ns |
| T8 | Slave | Data Hold Time | 15 | | | ns |
| T9 | Slave | Slave Read Latency | | 4 | | MC Cycles |
| T10 | Master | MST Read Latency and INTR Delay | | 12 | | MC Cycles |

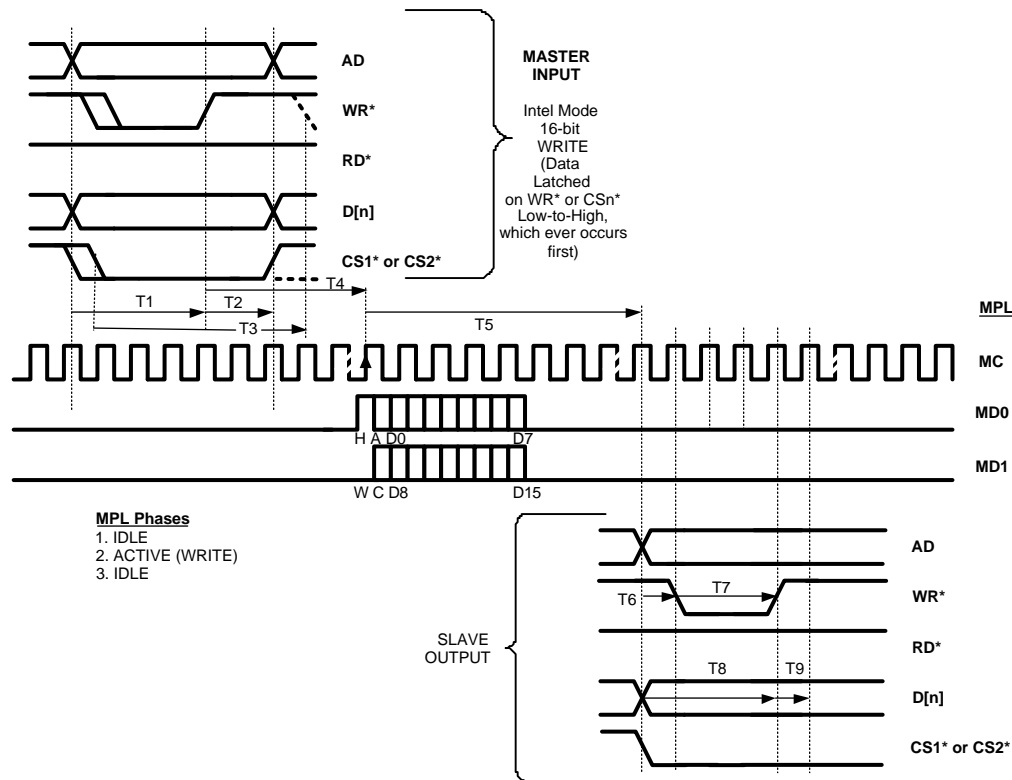
Table 8. READ—6800 μ P Interface Parameters (continued)

| No. | | Parameter | Min | Typ | Max | Units |
|-----|-----------|-------------------------------|-----|------|-----|-----------|
| T11 | Master | Data Delay | | 18.6 | | ns |
| T12 | MasterOUT | Data Valid after Strobe | | 15 | | ns |
| T13 | MasterOUT | CS* or E active pulse width | 20 | | | ns |
| T14 | MasterOUT | INTR De-assert | | 5 | | MC Cycles |
| T15 | MasterOUT | Recovery Time | | 5 | | ns |
| T16 | MasterOUT | INTR Response, ⁽¹⁾ | 0 | | | MC Cycles |

(1) This parameter is specified by design based on simulation or bench characterization.

For the MOT CPU 68xx mode, the Master accepts data on the CS* Low-to-High transition or the E High-to-Low transition, whichever come first. The Slave output only uses the CS* pin for data strobe/latch, as the E signal is held constantly High.

CPU MODE—WRITE—i80

**Figure 15. WRITE—80xx μ P Interface****Table 9. WRITE—80xx μ P Interface Parameters**

| No. | | Parameter | Min | Typ | Max | Units |
|-----|----------|--------------------------------------|-----|-----|-----|-----------|
| T1 | MasterIN | Data Setup before Write* High | 5 | | | ns |
| T2 | MasterIN | Data Hold after Write* High | 5 | | | ns |
| T3 | MasterIN | Write* Recovery Time, ⁽¹⁾ | 6 | | | MC Cycles |
| T4 | Master | Master Latency | | 5 | | MC Cycles |
| T5 | Slave | Slave Latency | | 9 | | MC Cycles |
| T6 | SlaveOUT | Data Valid before Write* High-to-Low | | 1 | | MC Cycles |

(1) This parameter is specified by design based on simulation or bench characterization.

Table 9. WRITE—80xx μ P Interface Parameters (continued)

| No. | | Parameter | Min | Typ | Max | Units |
|-----|----------|--------------------------------------|-----|-----|-----|-----------|
| T7 | SlaveOUT | WR* Pulse Width Low | | 3 | | MC Cycles |
| T8 | SlaveOUT | Data Valid before Write* Low-to-High | | 4 | | MC Cycles |
| T9 | SlaveOUT | Data Valid after Write* Low-to-High | | 1 | | MC Cycles |

CPU MODE—READ—i80

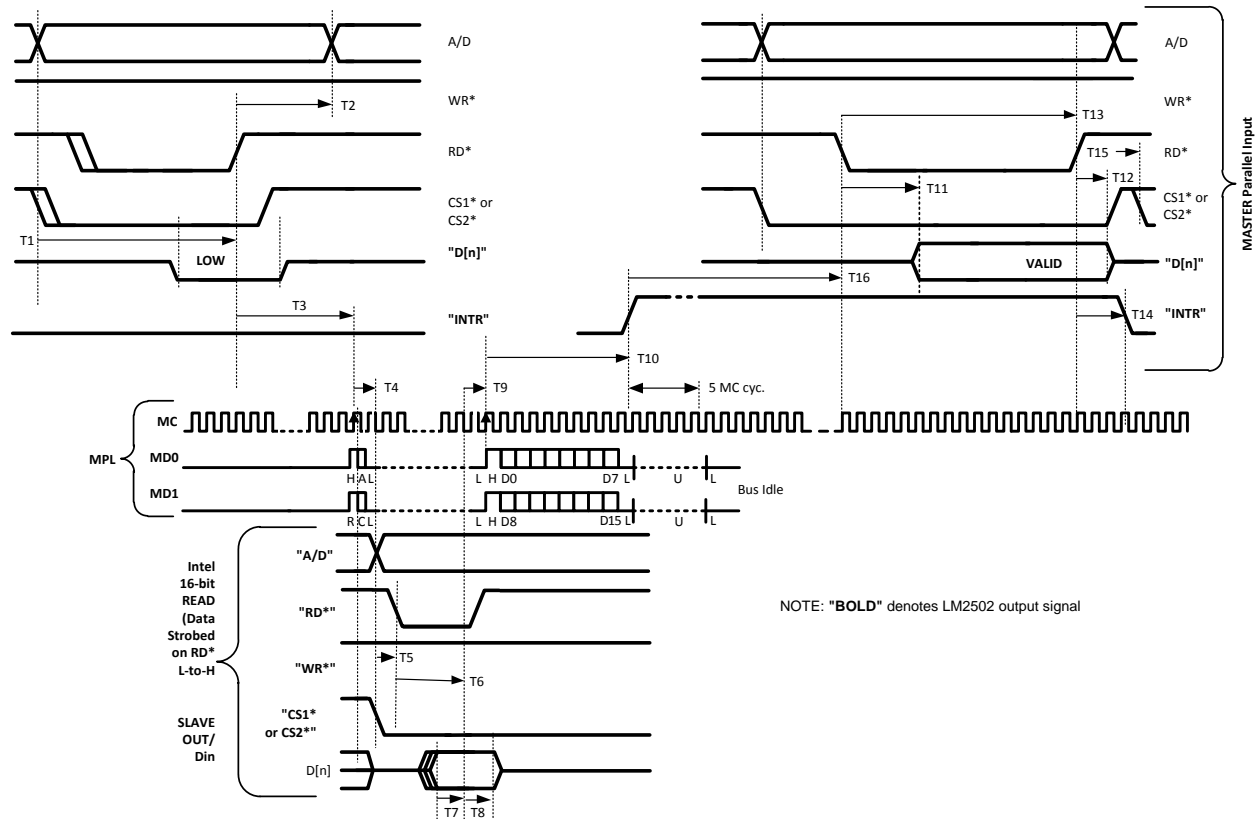


Figure 16. READ—INTEL μ P Interface

Table 10. READ—Intel μ P Interface Parameters

| No. | | Parameter | Min | Typ | Max | Units |
|-----|-----------|---|-----|------|-----|-----------|
| T1 | MasterIN | Set Up Time (A/D, RD*) and Data On Time | 20 | | | ns |
| T2 | MasterIN | Hold Time (A/D, RD*) and Data Off Time | | 15 | | ns |
| T3 | Master | Master Latency | | 5 | | MC Cycles |
| T4 | Slave | Slave Latency | | 6 | | MC Cycles |
| T5 | Slave | Read* Delay | | 1 | | MC Cycles |
| T6 | Slave | Read Low Pulse Width | | 6 | | MC Cycles |
| T7 | Slave | Data Set Up Time | 5 | | | ns |
| T8 | Slave | Data Hold Time | 15 | | | ns |
| T9 | Slave | Slave Read Latency | | 4 | | MC Cycles |
| T10 | Master | MST Read Latency and INTR Delay | | 12 | | MC Cycles |
| T11 | Master | Data Delay | | 18.6 | | ns |
| T12 | MasterOUT | Data Valid after Strobe | | 15 | | ns |
| T13 | MasterOUT | RD* active pulse width | 20 | | | ns |

Table 10. READ—Intel μ P Interface Parameters (continued)

| No. | | Parameter | Min | Typ | Max | Units |
|-----|-----------|-------------------------------|-----|-----|-----|-----------|
| T14 | MasterOUT | INTR De-assert | | 5 | | MC Cycles |
| T15 | MasterOUT | Recovery Time | | 5 | | ns |
| T16 | MasterOUT | INTR Response, ⁽¹⁾ | 0 | | | MC Cycles |

(1) This parameter is specified by design based on simulation or bench characterization.

LM2502 FEATURES AND OPERATION

POWER SUPPLIES

The V_{DDcore} and V_{DDA} (MPL and PLL) must be connected to the same potential between 2.9V and 3.3V. V_{DDIO} powers the logic interface and may be powered between 1.7 and 3.3V to be compatible with a wide range of host and target devices. V_{DDIO} should not be powered up without V_{DDcore}/V_{DDA} applied as V_{DDcore} biases the IO ring. During power up, all rails should power up at the same time, or V_{DDcore}/V_{DDA} should lead.

POWER DOWN/OFF

The Master and the Slave provide a PD* pin to save power when the link is not needed. A Low on this pin will power down the entire device and turn off the line current to MD0, MD1, and MC.

During power up, the PD* inputs should be held LOW and released once power is stable and within specification. The Slave PD* may be released first or at the same time as the Master's PD* pin. CLK (Master) should be applied prior to releasing PD*. If the Powerdown state is not required, the PD* pins maybe connected to V_{DDIO} , however V_{DDIO} should power up smooth through the logic threshold region.

In Powerdown (PD* = GND) the following outputs are driven to:

Master:

INTR = L

Slave depends on mode configuration - see [Table 11](#).

Table 11. SLV Output in Powerdown

| Pin | SLV i80 | SLV m68 |
|---------|------------|------------|
| AD | H | H |
| Data[n] | L | L |
| CLK | L | L |
| CS1* | H | H |
| CS2* | L | H |
| MF0 | H | H |
| MF1 | H | H |

BYPASS RECOMMENDATIONS

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 μ F capacitors. A 2.2 to 4.7 μ F Tantalum capacitor is recommended near the Master (SER) V_{DDA} pin for PLL bypass. Connect bypass capacitors with wide traces and use dual or larger via to reduce resistance and inductance of the feeds. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

UN-USED/OPEN PINS

Unused inputs must be tied to the proper input level—do not float them. Unused outputs should be left open to minimize power dissipation.

PHASE-LOCKED LOOP

When the LM2502 is configured as a Master, a PLL is enabled to generate the serial link clock. The Phase-locked loop system generates the serial data clock at several multiples of the input clock. The PLL operates with an input clock between 3 and 26 MHz. See [Table 12](#) below, Multiplier/Divisor times CLK rate must also be less than 76.8 MHz. The 76.8 MHz limitation is based on the semiconductor process used on this implementation—it is not an MPL limitation.

Line rate should also be selected such that it is faster than the input load rate when bursting data across the link. Otherwise 8/10 X Line rate must be greater than the input load rate to the Master. At the maximum raw data rate of 307 Mbps, the maximum information rate is 245 Mbps. Thus the parallel load rate at the Master input must not exceed 15.4 Mega Transfers per second sustained (of 16 data bits). The Master can accommodate up to four words at a higher rate due to internal FIFOs.

Configuration pins (PLL_CON[2:0], and M/S*) are used to determine the mode of which the part is operating in. In the Slave configuration the PLL block is disabled. The Slave PLL_CON pins are required to set up the proper divisor for the CLK pin. Slave PLL_CON[2:0] pins do not need to be set the same as the Master, this allows for clock multiplication / division to be supported for the output clock reference signal.

RESET

On both the Master and the Slave, the PD* pin resets the logic. The PD* pins should be held low until the power supply has ramped up and is stable and within specifications. The Slave PD* pin should be driven High first or at the same time as the Master. This will ensure that the Slave sees the start up sequence from the Master.

MASTER/SLAVE SELECTION

The M/S* pin is used to configure the device as either a Master or Slave device. When the M/S* pin is a Logic High, the Master configuration is selected. The Driver block is enabled for the MC line, and the MD lines. When the M/S* pin is a Logic Low, the Slave configuration is selected. The Receiver block is enabled for the MC line, and the MD lines.

Table 12. PLL_CON Settings

| PLLCON2 | PLLCON1 | PLLCON0 | Multiplier (Master) MC out | Divisor (Slave) CLKout | Minimum CLK Input | Maximum CLK Input (MC ≤ 76.8 MHz) |
|---------|---------|---------|----------------------------------|------------------------------|----------------------|---|
| 0 | 0 | 0 | CLK X 2 | MC / 2 | 13 MHz | 26 MHz |
| 0 | 0 | 1 | CLK X 4 | MC / 4 | 6 MHz | 19.2 MHz |
| 0 | 1 | 0 | CLK X 6 | MC / 6 | 3 MHz | 12.8 MHz |
| 0 | 1 | 1 | CLK X 7 | MC / 7 | 3 MHz | 10.97 MHz |
| 1 | 0 | 0 | CLK X 8 | MC / 8 | 3 MHz | 9.60 MHz |
| 1 | 0 | 1 | CLK X 9 | MC / 9 | 3 MHz | 8.53 MHz |
| 1 | 1 | 0 | CLK X 10 | MC / 10 | 3 MHz | 7.68 MHz |
| 1 | 1 | 1 | | | | (Reserved) |

APPLICATION INFORMATION

SYSTEM CONSIDERATIONS

When employing the MPL SERDES chipset in place of a parallel bus, a few system considerations must be taken into account. Before sending commands (ie initialization commands) to the display, the SERDES must be ready to transmit data across the link. The MPL link must be powered up, and the PLL must be locked. Also a review of the Slave output timing should be completed to insure that the timing parameters provided by the Slave output meet the requirements of the LCD driver input. Specifically, pulse width on CSn*, RD* / WR*, data valid time, and bus cycle rate should be reviewed and checked for inter-operability. Additional details are provided next:

The MPL link should be started up as follows: The chipset should be powered up first, V_{DDIO} should not be powered up first, it may be at the same time as V_{DD}/V_{DDA} or lag. During power up, the PD* inputs should be held LOW and released once power is stable and within specification. The Slave PD* may be released first or at the same time as the Master. CLK should be applied prior to releasing PD*.

Before data can be sent across the MPL serial link, the link must be ready for transmission. The CLK needs to be applied to the device, and the PLL locked. This is controlled by a keep-off counter set for 4096 cycles. After the PLL has lock and the counter expired, an additional 40 clock cycles are required for the calibration of the MPL link. After this, data may now be written to the device.

It takes 5MC Cycles to send a 16-bit CPU Write including the serial overhead. The MC cycle time is calculated based on the PLL_CON[2:0] setting and also the input clock frequency. For example, a 19.2MHz input CLK and a 4X PLLCON setting yields a MC frequency of 76.8MHz. Thus it takes 65.1ns to send the word in serial form. To allow some idle time between transmissions (this will force a bit sync per word if the gap is long enough in between), the load rate on the Master input should not be faster than 6MC cycles, or every 78ns in our example to support a data pipe line. This is sometimes referred to as the bus cycle time (time between commands).

The Slave output times is also a function of MC cycles. Note that in i80 mode, the width of the WR* pulse (in m68 mode the width of the CS*) pulse low is **three MC cycles** regardless of the pulse width applied to the Master input. System designers need to check compatibility with the display driver to ensure this pulse width meets its requirement. If it is too fast, select a lower PLLCON setting or apply a slower input clock.

The CLK input must be free running and not gapped. If the clock is stopped a RESET (PD* = Low) cycle should be done and the link brought up again.

MPL SWAP FEATURE

The LM2502 provides a swap function of MPL MD lines depending upon the state of the M/S* pin. This facilitates a straight through MPL interface design eliminating the needs for via and crossovers as shown on [Figure 17](#). See also [Connection Diagram](#) and [Table 1](#).

Note that three pins are defined differently on the MASTER and the SLAVE configured device. Schematic Capture device diagrams should take this into account for proper connection. The following pin descriptions apply for the three pins given in Ball Number : Master (Slave) function

NFBGA Package

- A5 : INTR (CLKDIS*)
- A6 : MD1 (MD0)
- B7 : MD0 (MD1)

WQFN Package

- 34 : INTR (CLKDIS*)
- 32 : MD1 (MD0)
- 29 : MD0 (MD1)

FLEX CIRCUIT RECOMMENDATIONS

The three MPL lines should generally run together to minimize any trace length differences (skew). For impedance control and also noise isolation (crosstalk), guard ground traces are recommended in between the signals. Commonly a Ground-Signal-Ground (GSGSGSG) layout is used. Locate fast edge rate and large swing signals further away to also minimize any coupling (unwanted crosstalk). In a stacked flex interconnect, crosstalk also needs to be taken into account in the above and below layers (vertical direction). To minimize any coupling locate MPL traces next to a ground layer. Power rails also tend to generate less noise than LVCMOS so they are also good candidates for use as isolation and separation.

The interconnect from the Master to the Slave typically acts like a transmission line. Thus impedance control and ground returns are an important part of system design. Impedance should be in the 50 to 100 Ohm nominal range for the LM2502. Testing has been done with cables ranging from 40 to 110 Ohms without error (BER Testing). To obtain the impedance, adjacent grounds are typically required (1 layer flex), or a ground shield / layer. Total interconnect length is intended to be in the 20cm range, however 30cm is possible at lower data rates. Skew should be less than 500ps to maximize timing margins.

GROUNDING

While the LM2502 employs three separate types of ground pins, these are intended to be connected together to a common ground plane. The separate ground pins help to isolate switching currents from different sections of the integrated circuit (IC). Also required is a nearby signal return (ground) for the MPL signals. These should be provided next to the MPL signals, as that will create the smallest current loop area. The grounds are also useful for noise isolation and impedance control.

PCB RECOMMENDATIONS

General guidelines for the PCB design:

- Floor plan, locate MPL Master near the connector to limit chance of cross talk to high speed serial signals.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines as guards to minimize any noise coupling (specifies distance).
- Avoid parallel runs with fast edge, large LVCMOS swings.
- Also use a GSGSG pinout in connectors (Board to Board or ZIF).
- Slave device - follow similar guidelines.
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.

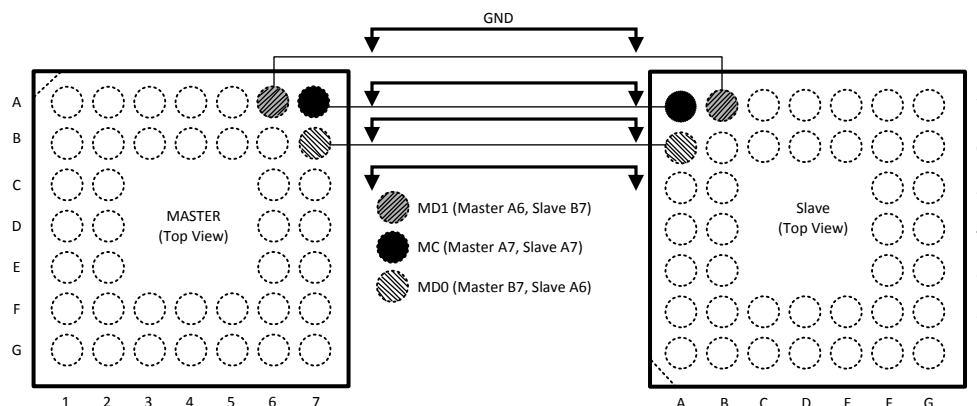


Figure 17. MPL Interface Layout - NFBGA Example

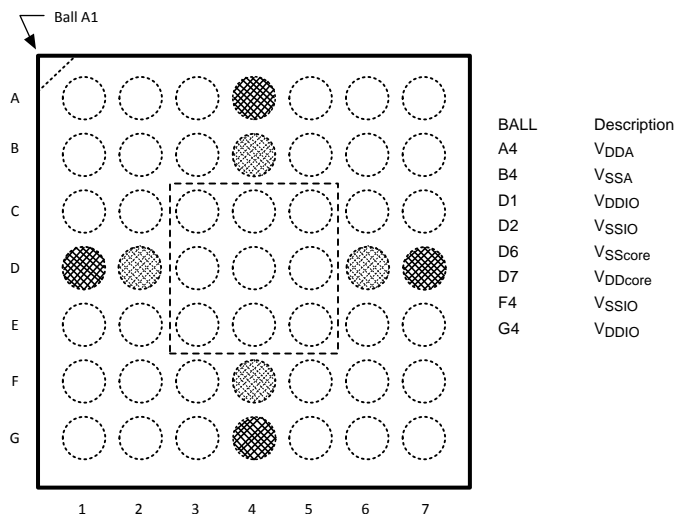


Figure 18. LM2502 NFBGA Package PWR (V_{DD}) and GND (V_{SS}) Balls

DISPLAY APPLICATION

The LM2502 chipset is intended for Interface between a host (processor) and a Display. It supports a 16 or 8-bit CPU style interface and can be configured for i80 or m68 modes.

The Master side connection is shown in [Figure 19](#). Input Clock frequency and the selection of the PLL_CON setting are determined by system parameters. These include the required display bandwidth, the Master load rate and the Display Driver input timing requirements. See the [System Considerations](#) section for more details.

The Display side parallel bus may be connected to one or two displays. Each display has its own chipselect signal. If only one display is required, the unused CS signal should be tied HIGH (V_{DDIO}) on the Master, and the unused output left open on the Slave. The Slave provides an optional clock output. If this is desired the CLKDIS* pin needs to be also tied HIGH. A different PLL_CON setting can be used to alter the frequency if desired. As the Divisor setting in the Slave is not used for data recovery. For the dual display application, the multidrop bus should be laid out to minimize any resulting stub lengths on the Data, A/D, and control signals.

If required, the Slave output clock can be enabled to provide a output frequency reference. The frequency can be adjusted by setting different PLL_CON (divisor) settings (on the Slave). This can then be used as a frequency reference signal to the display module or other subsystem (ie camera module). If the CLK output is not needed, tie the Slave CLKDIS* pin Low to disable it. The Clock is available when ever the MPL link is enabled.

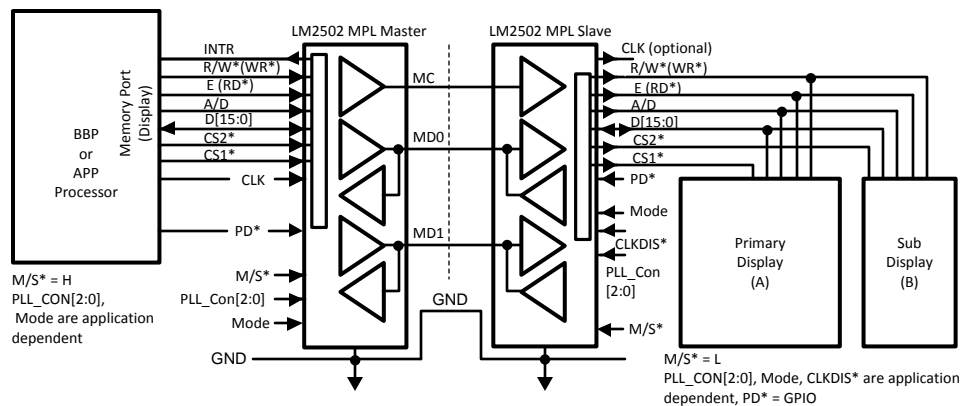


Figure 19. Display Interface Application

RGB565 APPLICATION

The LM2502 chipset may also be configured for a RGB565 application. This is also known as a "buffer-less" or "dumb" display application. In this configuration 16 color bits (R[4:0], G[5:0], B[4:0]), Pixel Clock (PCLK) and two control bits (VS and HS) are supported. An external inverter is also required.

To configure for the RGB565 mode, the i80 mode must be selected. The Pixel clock should be connected to both the CLK input and the WR* pins on the Master. The PLL_CON pins should be configured for a 6X mode, as it takes 5 MC cycles to transfer the RGB data, and the 6X setting will provide a 50% output PCLK from the Slave device. The 50% duty cycle PCLK is created by the WR* signal which pulses low for 3 MC cycles and is high for 2 MC cycles and an idle MC cycle. See [Figure 20](#) for details. Support is provided for PCLKs in the 3 to 12.8 MHz range. PLLCON setting of X8 is also possible, however, the Slave output PCLK (WR*) will have some duty cycle distortion (37.5%) and the CLK range is further restricted.

Slower PCLK rates maybe supported if a higher frequency multiple of the PCLK is available. For example, if a 2MHz PCLK is required, then a 6MHz CLK (freq locked, not phase) may be applied to the MST CLK input and the 2MHz PCLK to the MST WR* signal input. The PLLCON setting should be selected as 2X (PLLCON[2:0] = 000'b). Once again 5 MC cycles are required to transfer the pixel data, and the WR* (PCLK) will be 50% duty cycle. The applied CLK and PLLCON should be selected such that is creates a 6X multiple on MC to ensure a 50% duty cycle.

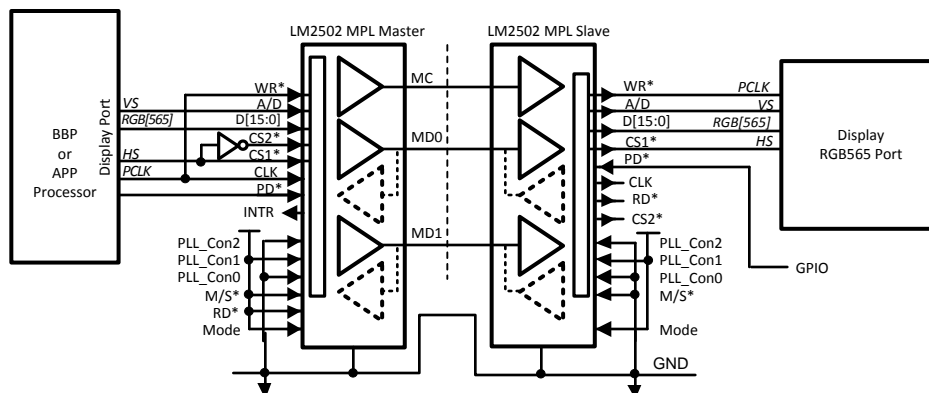


Figure 20. RGB565 Application

QVGA Example - For a QVGA display (320 by 240), with 16 bits of color depth and 60 frames per second, a net bandwidth requirement is 73.728 Mbps. Maximum transfer rate for the LM2502 chipset is 245 Mbps (307 Mbps raw - includes overhead), thus there is adequate bandwidth for this application and even larger resolution displays.

Figure 21 shows the typical timing of the RGB application. The 6X PLL setting (PLLCON[2:0] = 010'b) is selected. The PCLK is applied to both the WR* and CLK inputs on the Master. The rising edge on the WR* (PCLK) signal samples the data by the Master for serialization. The CLK input can be the PCLK (if timing requirements are met) or a synchronous clock to the PCLK signal. The HS connects to the CS1* signal and the HS* (inverted HS) is connected to the CS2*. With this configuration there will always be a valid CS* LOW on the Master input. The RGB information is then serialized and passed to the Slave via the MPL bus. It takes 5 MC cycles to complete the transfer and with the 6X PLL setting, there will be two idle bits on the MD (1 MC cycle) before the next transfer. Recovery of the RGB interface (RGB565, HS, VS and PCLK) is provided at the Slave output. The PCLK is slightly shifted later in time (1 MC cycle) but adequate timing margin (increased set, shorted hold) is still provided.

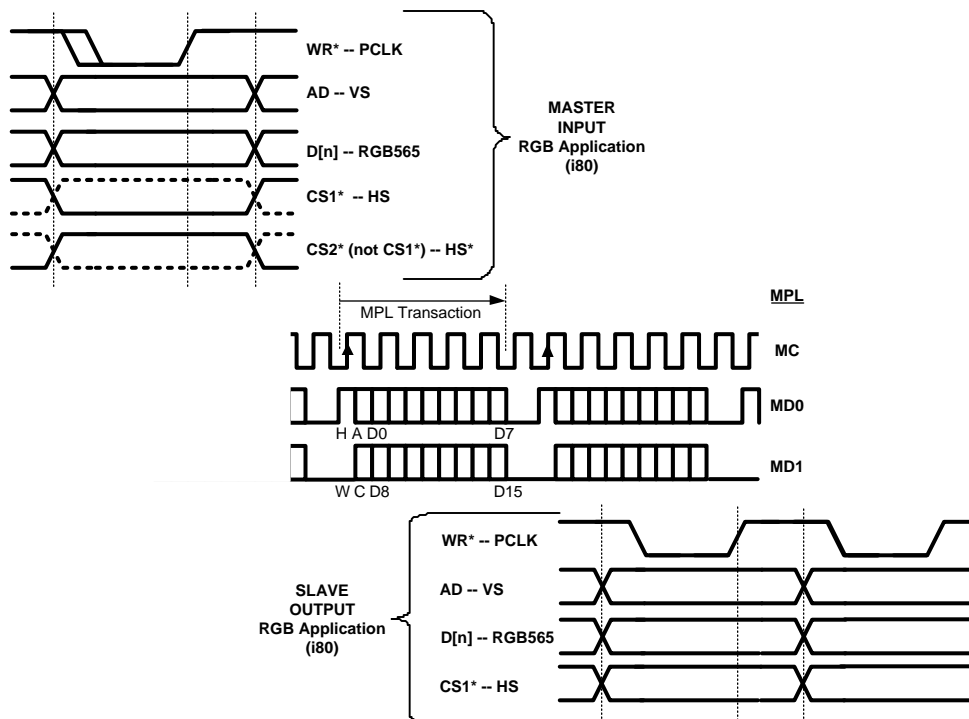


Figure 21. RGB565 Application Timing

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LM2502SQ/NOPB | Active | Production | WQFN (RSB) 40 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -30 to 85 | L2502SQ |
| LM2502SQ/NOPB.A | Active | Production | WQFN (RSB) 40 | 1000 SMALL T&R | Yes | SN | Level-3-260C-168 HR | -30 to 85 | L2502SQ |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

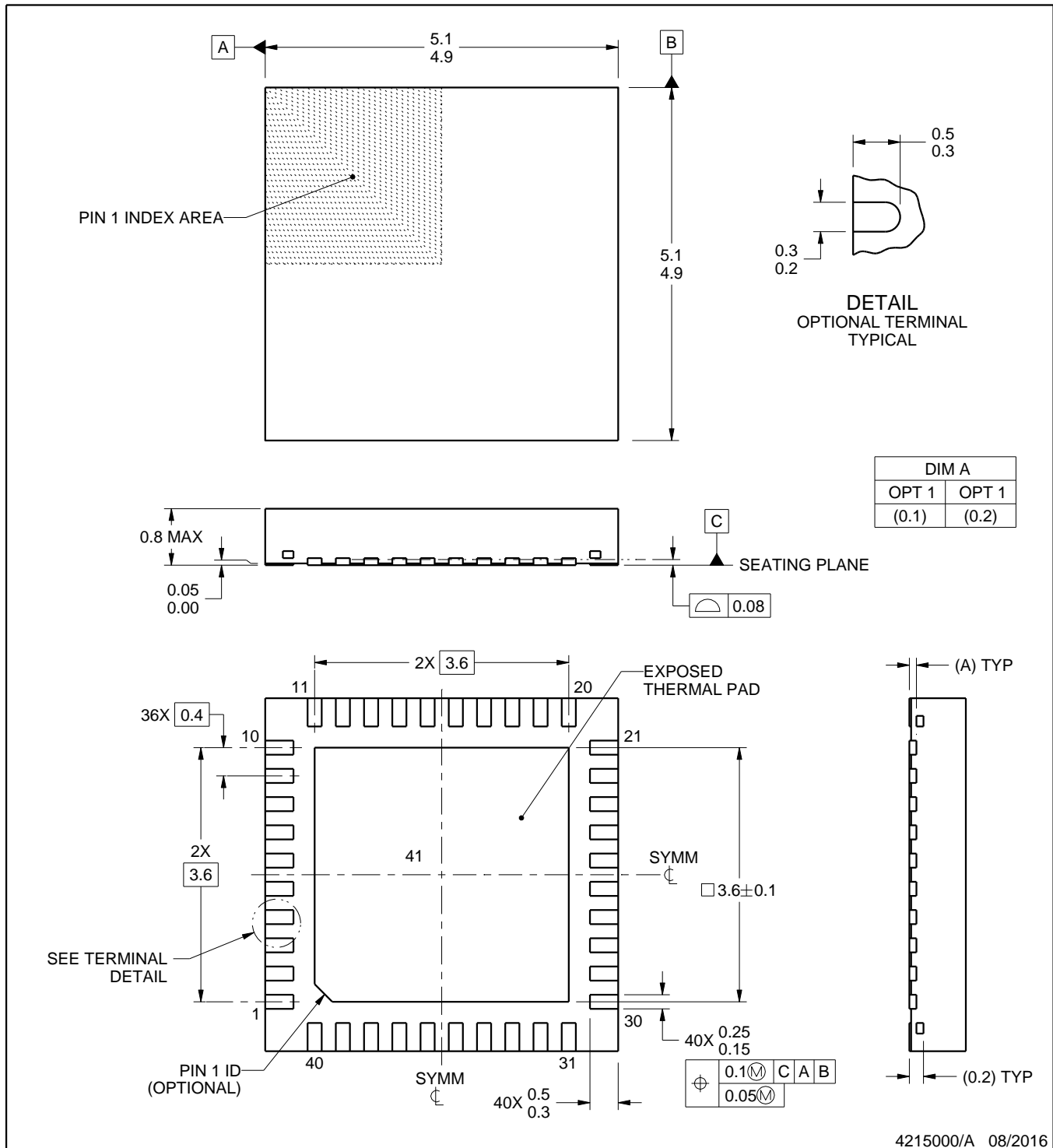
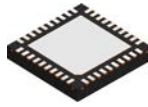
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM2502SQ/NOPB | WQFN | RSB | 40 | 1000 | 177.8 | 12.4 | 5.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM2502SQ/NOPB | WQFN | RSB | 40 | 1000 | 208.0 | 191.0 | 35.0 |



NOTES:

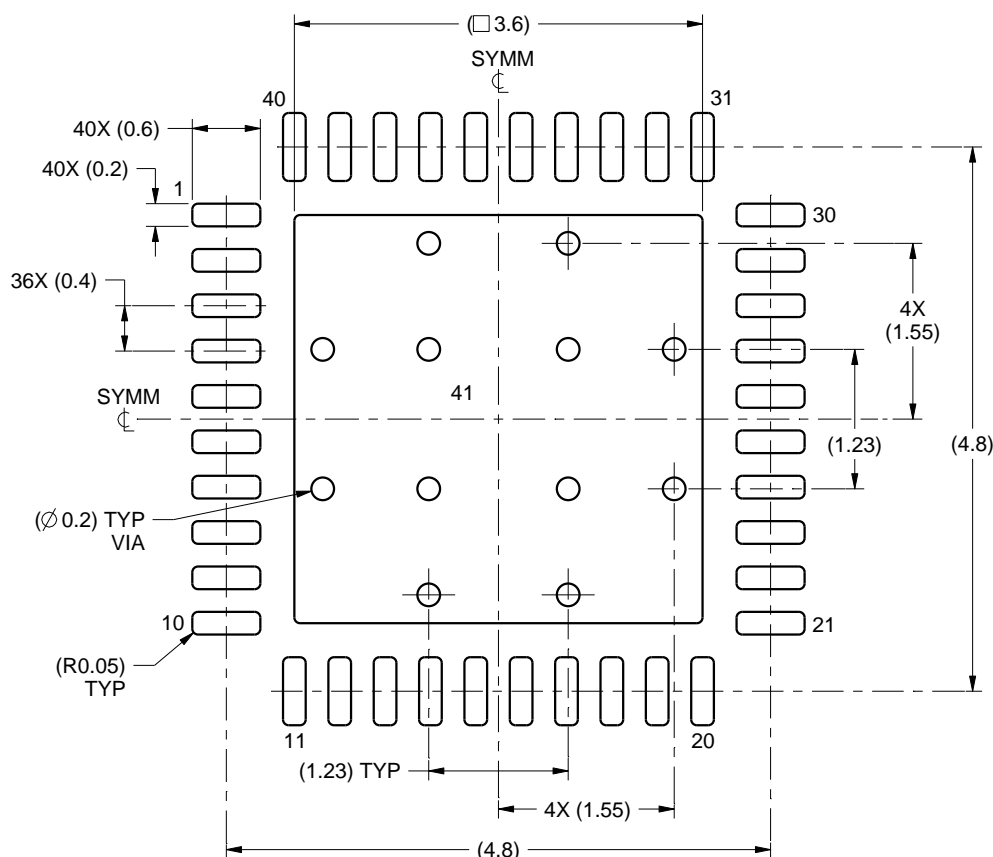
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

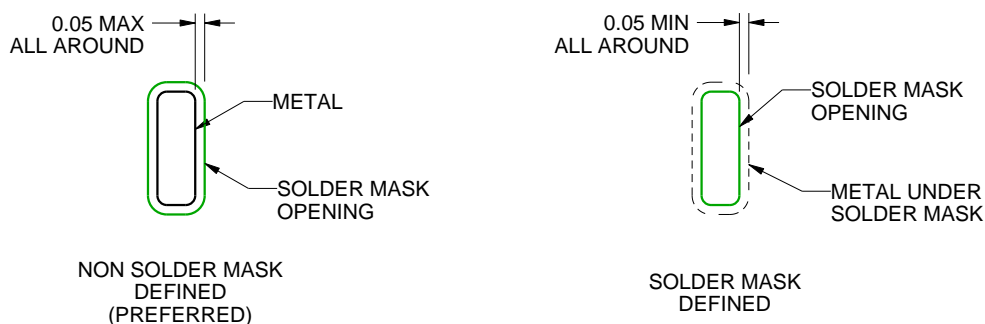
RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4215000/A 08/2016

NOTES: (continued)

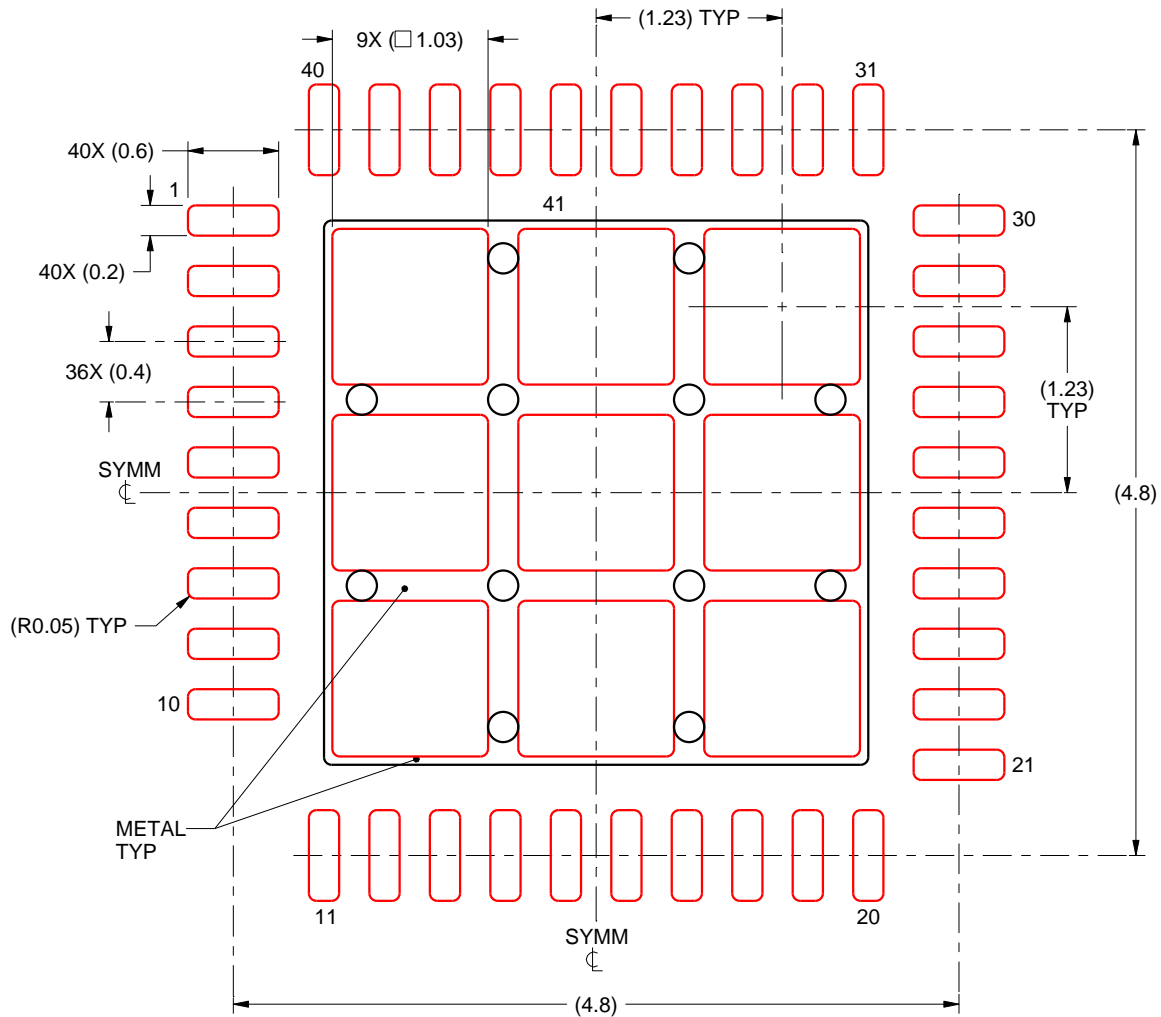
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/A 08/2016

NOTES: (continued)

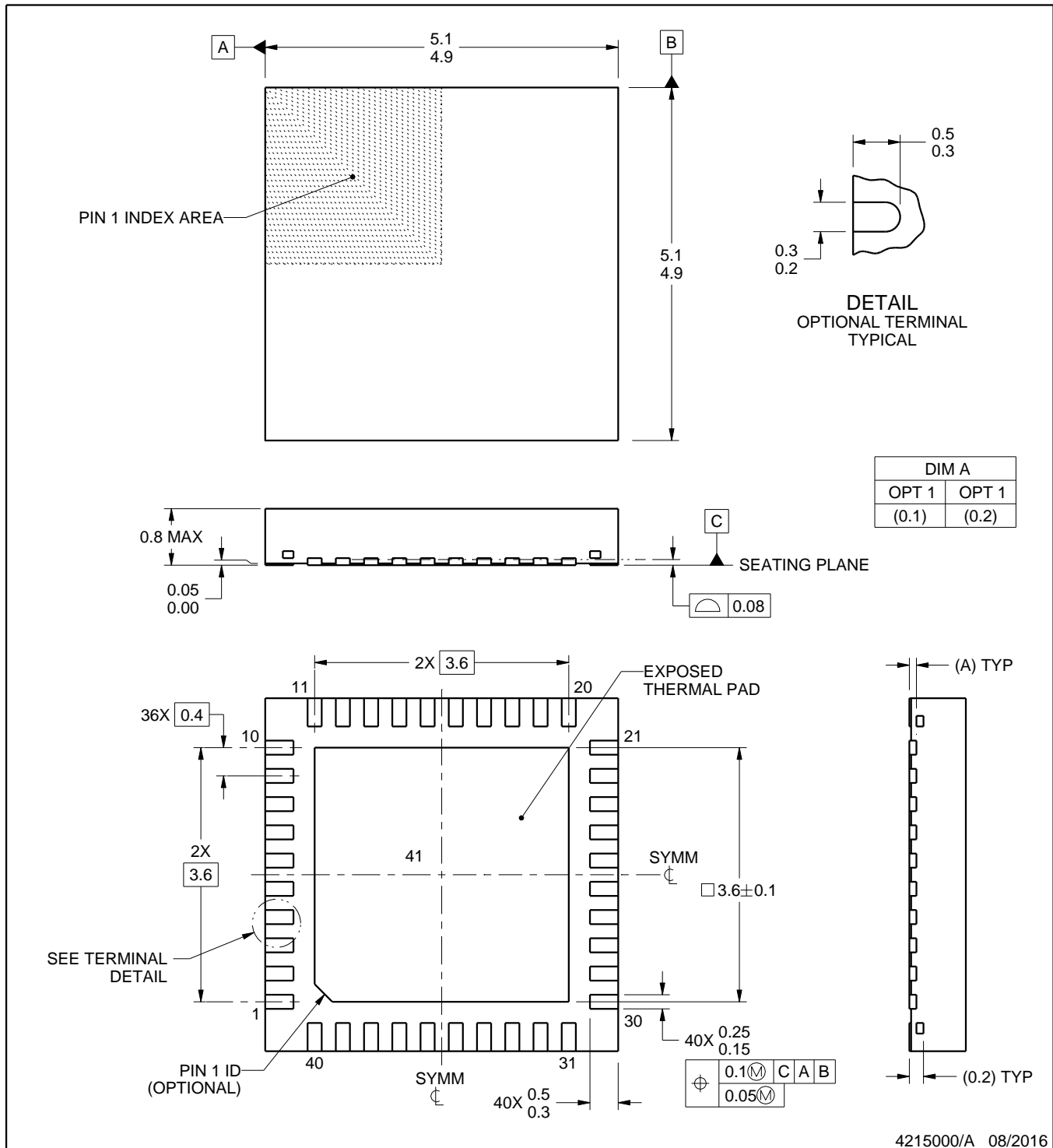
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RSB0040A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

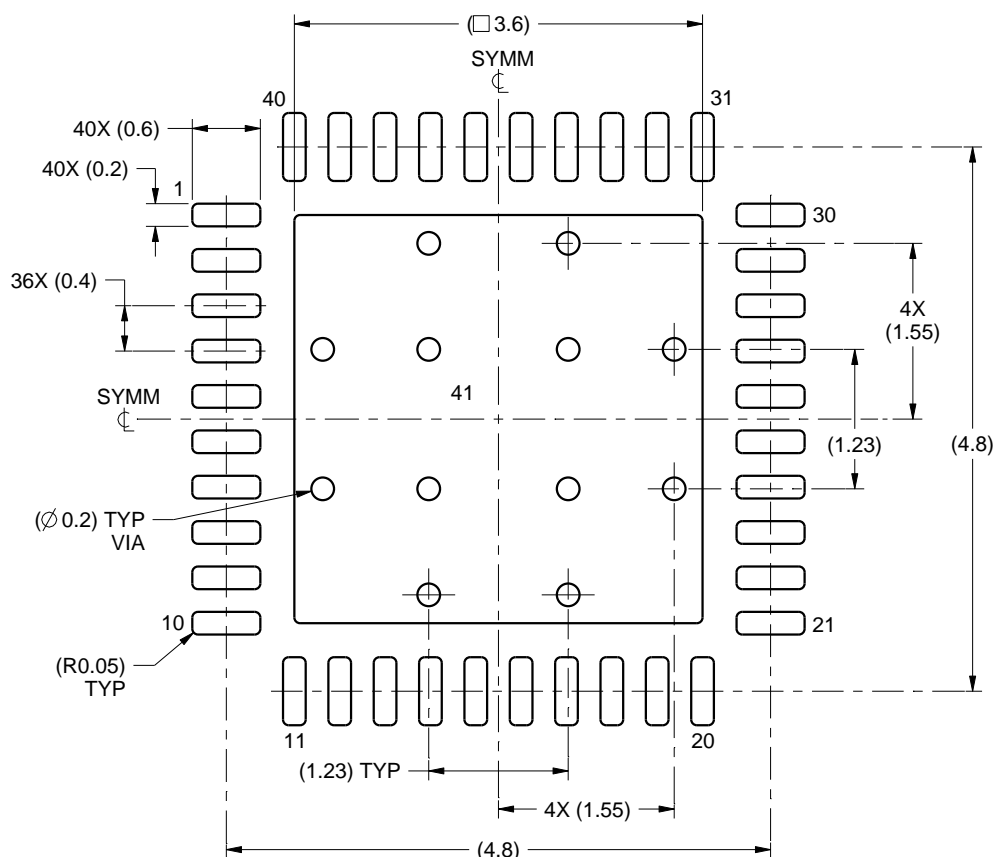
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

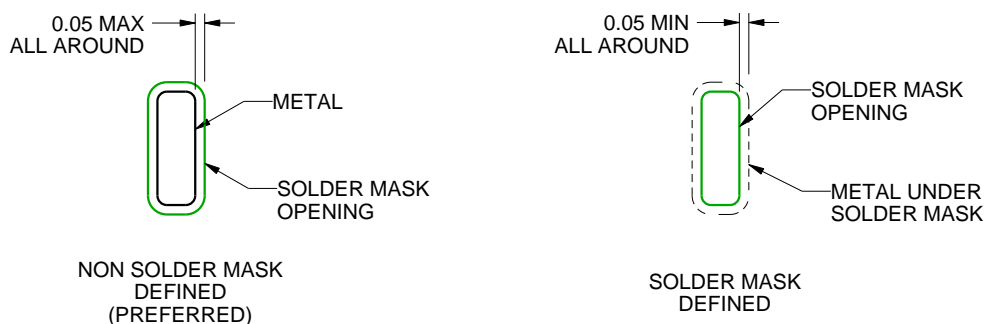
RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4215000/A 08/2016

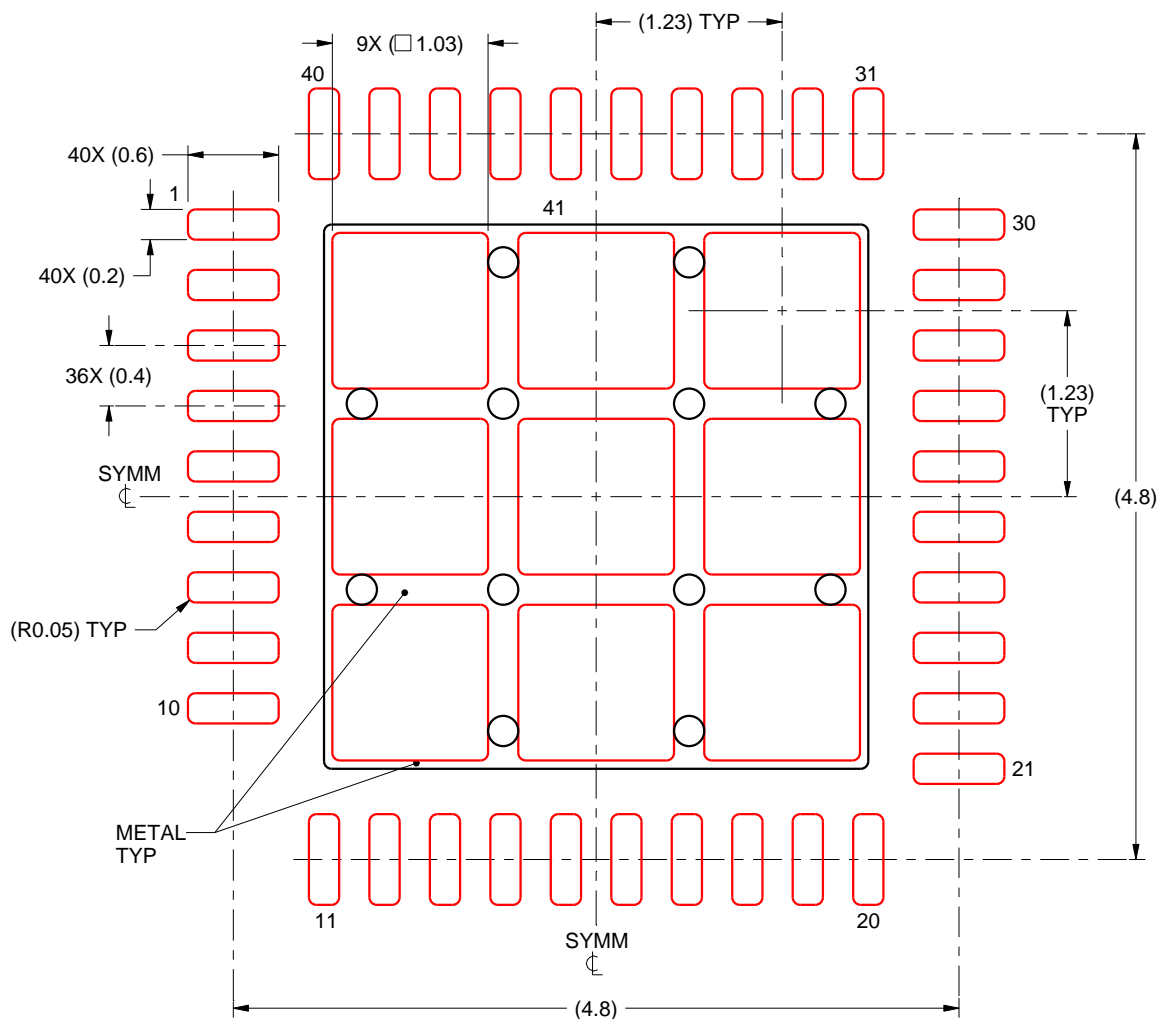
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RSB0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
73.7% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4215000/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025