LM3269 Seamless-Transition Buck-Boost Converter for 3G and 4G RF Power Amplifiers

1 Features

- Operates From a Single Li-Ion Cell: 2.7 V to 5.5 V
- Adjustable Output Voltage: 0.6 V to 4.2 V
- Automatic PFM or PWM Mode Change
- 750-mA Maximum Load Capability for $V_{BATT} \geq 3$ V, $V_{OUT} = 3.8$ V
- 2.4-MHz (typical) Switching Frequency
- Seamless Buck-Boost Mode Transition
- Fast Output Voltage Transition: 1.4 V to 3 V in 10 µs
- High-Efficiency: 95% typical at $V_{BATT} = 3.7$ V, $V_{OUT} = 3.3$ V, at 300 mA
- Input Overcurrent Limit
- Internal Compensation

2 Applications

- Power Supply for 3G/4G Power Amplifiers
- Cellular Phones
- Portable Hard Disk Drives
- PDAs

3 Description

The LM3269 is buck-boost DC-DC converter designed to generate output voltages above or below a given input voltage and is particularly suitable for portable applications powered by a single-cell Li-ion battery.

The LM3269 operates at a 2.4-MHz typical switching frequency in full synchronous operation and provides seamless transitions between buck and boost operating regimes. The LM3269 operates in energy-saving Pulse Frequency Modulation (PFM) mode for increased efficiencies and current savings during low-power RF transmission modes.

The power converter topology needs only one inductor and two capacitors. A unique internal power switch topology enables high overall efficiency.

The LM3269 is internally compensated for buck and boost modes of operation, thus providing an optimal transient response.

When considering using the LM3269 in a system design, please review the layout instruactions at the end of this document.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3269	DSBGA (12)	2.529 mm x 2.022 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

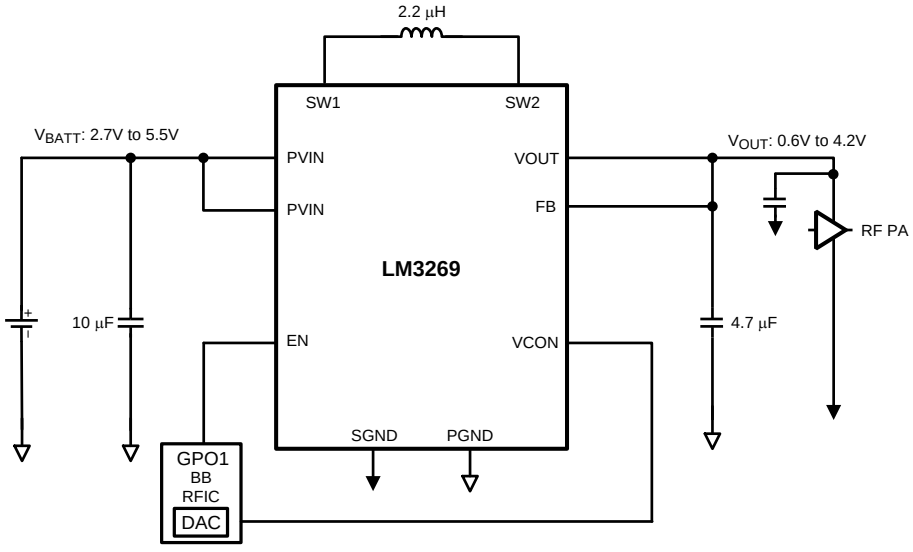


Table of Contents

4 Revision History

Changes from Revision C (May 2013) to Revision D — **Page**

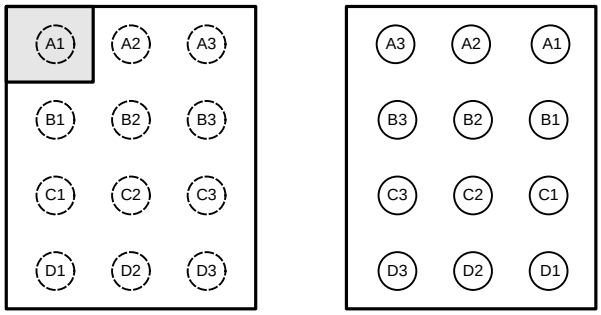
- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* , *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted *Recommended Capacitance Specifications* table as info contained in other tables ... 12

Changes from Revision B (August 2012) to Revision C — **Page**

- Changed product brief to full data sheet ... 1

5 Pin Configuration and Functions

YZR Package
12-Pin DSBGA
Top View



Top View Bottom View

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
A1	NC	—	Non Connection. Leave this pin floating; **do not** connect to PVIN or PGND.
A2	NC	—	Non Connection. Leave this pin floating, **do not** connect to PVIN or PGND.
A3	PVIN	P/I	Power MOSFET input and power current input pin. Optional low-pass filtering may help buck and buck-boost modes for radiated EMI and noise reduction.
B1	VCON	A/I	Voltage Control analog input. VCON controls the output voltage in PWM and PFM modes.
B2	EN	D/I	Enable pin. Pulling this pin higher than 1.2 V enables part to function.
B3	PVIN	P/I	Power MOSFET input and power current input pin. Optional low-pass filtering may help buck and buck-boost modes for radiated EMI and noise reduction.
C1	FB	A	Feedback input to inverting input of error amplifier. Connect output voltage directly to this node at load point.
C2	SGND	G	Signal Ground for analog circuits and control circuitry.
C3	SW1	P/O	Switch pin for Internal Power Switches. Connect inductor between SW1 and SW2.
D1	VOUT	O	Regulated output voltage of the LM3269. Connect this to a 4.7-µF ceramic output filter capacitor to GND.
D2	SW2	P/O	Switch pin for Internal Power Switches. Connect inductor between SW1 and SW2.
D3	PGND	G	Power Ground for Power MOSFETs and gate drive circuitry.

(1) A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
PVIN, VOUT to GND	−0.2	6	V
EN, VCON to SGND, PGND	−0.2	P_{VIN} + 0.2 V or 6 V(3)	V
FB to PGND	−0.2	V_{OUT} + 0.2 V or 6 V(3)	V
SW1, SW2	−0.2	P_{VIN} + 0.2 V or 6 V(3)	V
Continuous power dissipation(4)	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Whichever is smaller.
(4) Internal thermal circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typical) and disengages at T_J = 125°C (typical).

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	NOM	MAX	UNIT
Input voltage	2.7		5.5	V
Output voltage	0.6		4.2	V
Recommended load current	0		750	mA
Junction temperature (T_J)	−30		125	°C
Ambient temperature (T_A)(3)	−30		85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3269 YZR (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	85	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

6.5 Electrical Characteristics

Unless otherwise specified, typical (TYP) limits are for $T_A = T_J = 25°C$, and minimum (MIN) and maximum (MAX) limits apply over the full operating ambient temperature range ($-30°C \le T_J = T_A \le +85°C$). Unless otherwise noted, specifications apply to the *Figure 16* with: $P_{VIN} = EN = 3.6V$.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB,\ min}$	Min FB voltage	VCON = 0.2 V	0.53	0.60	0.67	V
$V_{FB,\ max}$	Max FB voltage	VCON = 1.4 V	4.13	4.2	4.27	
I_{Q_PWM}	Quiescent current	No switching(3)		0.9	1.2	mA
I_{SHDN}	Shutdown supply current	EN = 0 V, VCON = 0 V, SW1 = SW2 = V_{OUT} = 0 V		0.02	5	µA
I_{LIM_L}	Input current limit (large)	Open loop(4) VCON = 1.2 V	1500	1700	1900	mA
I_{LIM_S}	Input current limit (small)	Open loop(4) VCON = 0.2 V	750	850		
Gain	Internal gain(5)	0.2 V ≤ VCON ≤ 1.4 V		3		V/V
I_{EN}	EN pin pulldown current			5	10	µA
I_{VCON}	VCON pin leakage current		–1		1	
V_{IH}	Logic high input threshold for EN		1.2			V
V_{IL}	Logic low input threshold for EN				0.6	
$I_{OUT\_LEAKAGE}$	Leakage into VOUT pin of buck-boost	EN = 0 V, $V_{OUT} \le 4.2$ V, $P_{VIN} \le 5.5$ V			5	µA

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.
(3) I_Q specified here is when the part is not switching.
(4) The parameters in the electrical characteristics table are tested under open loop conditions at $P_{VIN} = 3.6$ V.
(5) To calculate V_{OUT}, use the following equation: $V_{OUT} = VCON \times 3$.

6.6 System Characteristics

The following spec table entries are specified by design and verification provided the component values in the typical application circuit are used (L = 2.2 µH, DCR = 110 mΩ, MIPSZ2520D2R2/FDK; C_{IN} = 10 µF, 6.3 V, C1608X5R0J106K/TDK (0603); C_{OUT} = 4.7 µF, 6.3 V, C1608X5R0J475M/TDK (0603). *These parameters are not verified by production testing.* Typical (TYP) limits are for $T_A = T_J = 25°C$; minimum (MIN) and maximum (MAX) limits apply over the full operating ambient temperature range ($-30°C \le T_J = T_A \le 85°C$) and over the $V_{BATT} = P_{VIN} = 2.7$ V to 5.5 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OUT_MAX}	Max output current	$V_{BATT} \ge 3$ V, V_{OUT} = 3.8 V	750			mA
V_{CON_LIN}	VCON linearity	0.2 V ≤ VCON ≤ 1.4 V	–2.5%		2.5%	
V_{O_RIPPLE}	Ripple voltage	$V_{BATT} \ge 3.2$ V, 0.6 V ≤ $V_{OUT} \le 4.2$ V, 0 mA ≤ $I_{OUT} \le 430$ mA, $T_A = 25°C$		15	50	mV
	PFM ripple	V_{OUT} = 0.6 V, I_{OUT} = 5 mA		45		
	Ripple voltage in mode transition	V_{BATT} = 3 V to 5 V, $T_R = T_F$ = 30 µs, 3.3 V ≤ $V_{OUT} \le 4.2$ V			50	
ΔV_{OUT}	Line regulation	V_{BATT} = 2.7 V to 4.7 V, V_{OUT} = 3.8 V, I_{OUT} = 500 mA			10	mV
	Load regulation	I_{OUT} = 0 mA to 500 mA, V_{BATT} = 2.7 V to 4.7 V			20	
V_{OUT_TR}	VOUT rise time	V_{BATT} = 3.2 V to 4.7 V, V_{OUT} = 1.4 V to 3 V, 0.1 µs < $Tr_{\_VCON}$ < 1 µs, R_{LOAD} = 11.4 Ω		10		µs

System Characteristics (continued)

The following spec table entries are specified by design and verification provided the component values in the typical application circuit are used (L = 2.2 µH, DCR = 110 mΩ, MIPSZ2520D2R2/FDK; C_{IN} = 10 µF, 6.3 V, C1608X5R0J106K/TDK (0603); C_{OUT} = 4.7 µF, 6.3 V, C1608X5R0J475M/TDK (0603). *These parameters are not verified by production testing.* Typical (TYP) limits are for $T_A = T_J$ = 25°C; minimum (MIN) and maximum (MAX) limits apply over the full operating ambient temperature range (−30°C ≤ $T_J = T_A$ ≤ 85°C) and over the $V_{BATT} = P_{VIN}$ = 2.7 V to 5.5 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
η	Efficiency	V_{BATT} = 3.7 V, V_{OUT} = 0.6 V, I_{OUT} = 10 mA −30°C ≤ $T_J = T_A$ ≤ 85°C		61%		
		V_{BATT} = 3.7 V, V_{OUT} = 1 V I_{OUT} = 20 mA −30°C ≤ $T_J = T_A$ ≤ 85°C		78%		
		V_{BATT} = 3.7 V, V_{OUT} = 1.4 V I_{OUT} = 50 mA −30°C ≤ $T_J = T_A$ ≤ 85°C		85%		
		V_{BATT} = 3.7 V, V_{OUT} = 2.7 V I_{OUT} = 200 mA −30°C ≤ $T_J = T_A$ ≤ 85°C		95%		
		V_{BATT} = 3.7 V, V_{OUT} = 3.3 V, I_{OUT} = 480 mA −30°C ≤ $T_J = T_A$ ≤ 85°C		94%		
		V_{BATT} = 3 V, V_{OUT} = 3.6 V, I_{OUT} = 200 mA −30°C ≤ $T_J = T_A$ ≤ 85°C		95%		

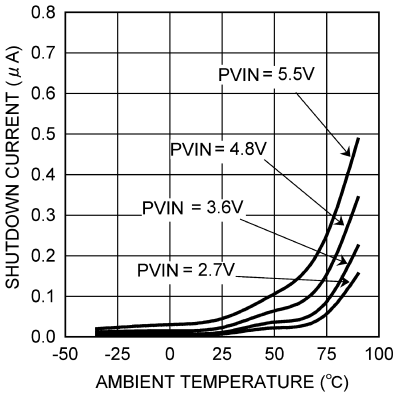
6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON}	Turnon time (time for output to reach 0V→90% × 3.5 V)	EN = L to H, V_{BATT} = 3.7 V, V_{OUT} = 3.5 V, I_{OUT} = 0 mA −30°C ≤ $T_J = T_A$ ≤ 85°C		35	50	µs
F_{OSC_PFM}	PFM operating frequency	V_{BATT} = 3.7 V, V_{OUT} = 0.6 V, I_{OUT} = 13 mA		63		kHz
F_{OSC_PWM}	Internal oscillator frequency	PWM	2.1	2.4	2.7	MHz
D_{MAX}	Maximum duty cycle	Boost			50%	
		Buck			100%	
V_{OUT_TR}	VCON change to 90%	V_{BATT} = 3.2 V to 4.7 V, V_{OUT} = 1.4 V to 3 V, 0.1 µs < $Tr_{\_VCON}$ < 1 µs R_{LOAD} = 11.4 Ω		10		µs

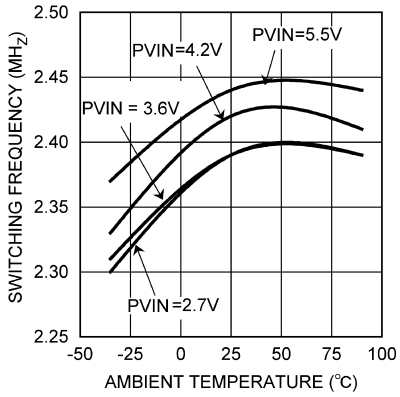
6.8 Typical Characteristics

(P_{VIN} = EN = 3.6 V and T_A = 25°C, unless otherwise noted)



VCON = V_{OUT} = SW1 = SW2 = EN = 0 V

Figure 1. Shutdown Current vs. Temperature



V_{OUT} = 3.5 V I_{OUT} = 300 mA

Figure 2. Switching Frequency vs. Temperature

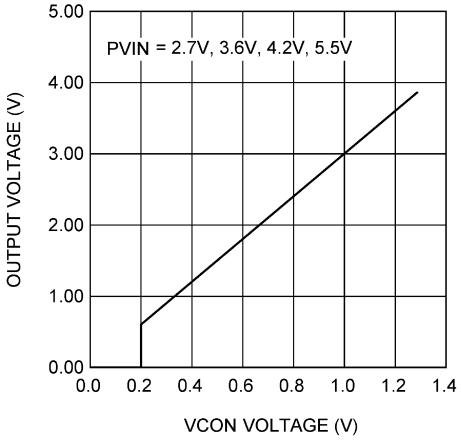
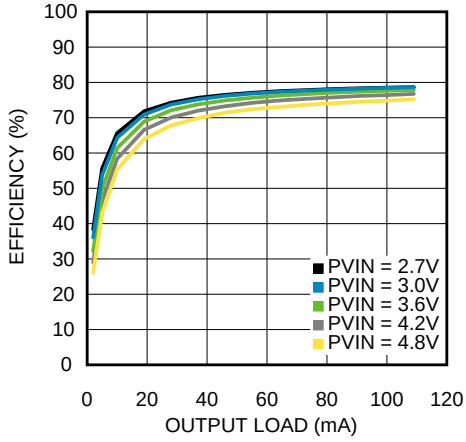
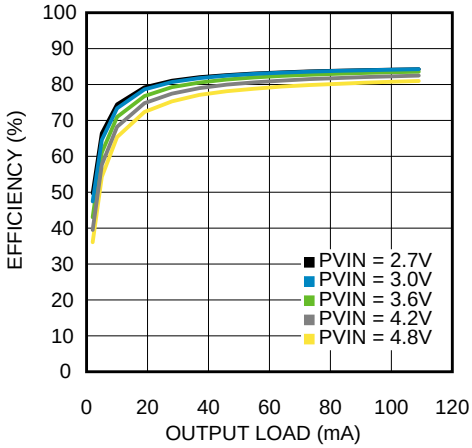


Figure 3. VCON Voltage vs. Output Voltage (No Load)



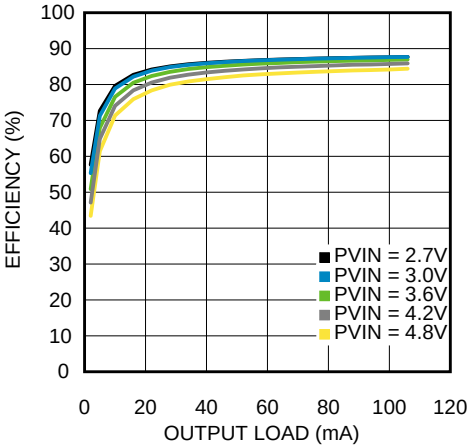
V_{OUT} = 0.6 V

Figure 4. PFM Efficiency



V_{OUT} = 1 V

Figure 5. PFM Efficiency



V_{OUT} = 1.4 V

Figure 6. PFM Efficiency

Typical Characteristics (continued)

(P_{VIN} = EN = 3.6 V and T_A = 25°C, unless otherwise noted)

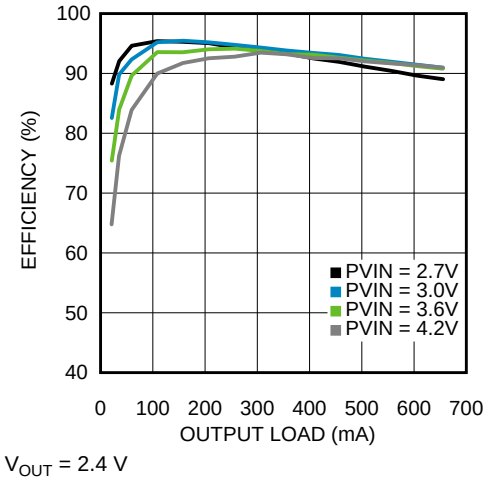


Figure 7. PWM Efficiency

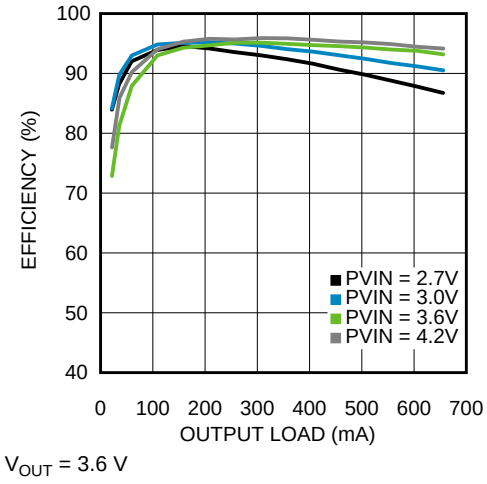


Figure 8. PWM Efficiency

7 Detailed Description

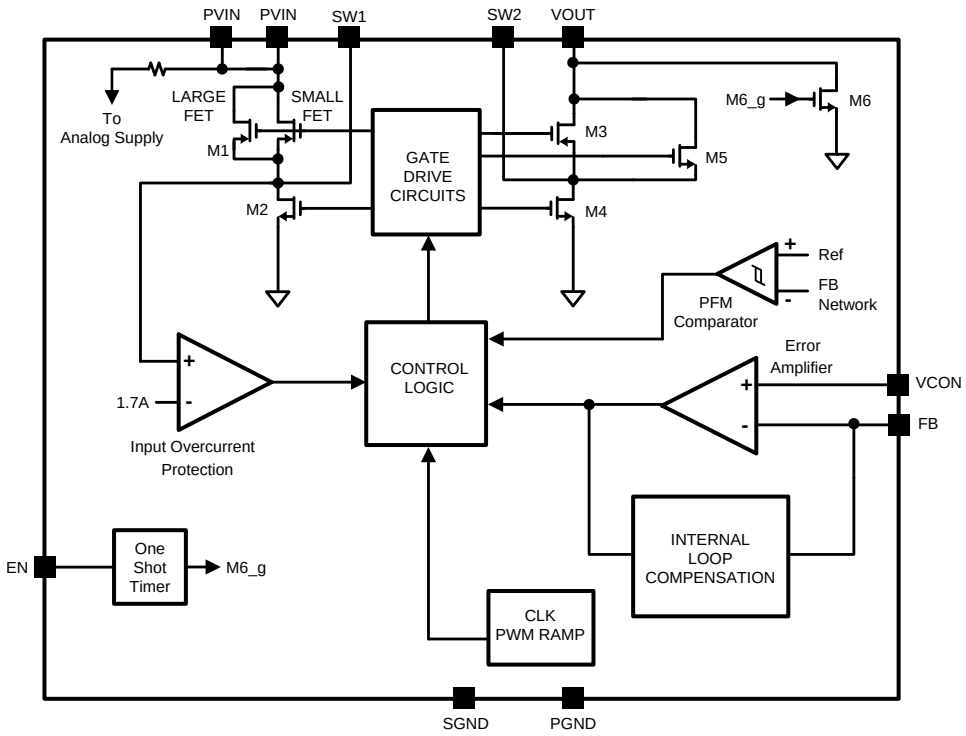
7.1 Overview

The LM3269 buck-boost converter provides high-efficiency, low-noise power for RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery-powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency for a wide range of power levels from a single Li-Ion battery cell. The capability of the LM3269 to provide an output voltage lower than, as well as higher than, the input battery voltage enables the PA to operate with high linearity for a wide range of battery voltages, thereby extending the usable voltage range of the battery. The converter feedback loop is internally compensated for both buck and boost operation, and the architecture is such that it provides seamless transition between buck and boost modes of operation. The LM3269 operates in energy saving Pulse Frequency Modulation (PFM) mode for increased efficiencies and current savings during low-power RF transmission modes. The output voltage is dynamically programmable from 0.6 V to 4.2 V by adjusting the voltage on the control pin VCON without the need for external feedback resistors. The fast output voltage transient response of the LM3269 makes it suitable for adaptively adjusting the PA supply voltage depending on its transmitting power, which prolongs battery life.

Additional features include current overload protection, output overvoltage clamp, and thermal overload shutdown.

The LM3269 is constructed using a chip-scale 12-bump DSBGA package that offers the smallest possible size for space-critical applications such as cell phones, where board area is an important design consideration. Use of high switching frequency (2.4 MHz, typical) reduces the size of external components. As shown in the Typical Application Circuit, only three external power components are required for circuit operation. Use of DSBGA package requires special design considerations for implementation. (See *DSBGA Package Assembly And Use*) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications where its edges are not subjected to high-intensity ambient red or infrared light. In addition, the system controller should set EN low during power-up and other low supply voltage conditions. (See *Enable And Shutdown Mode*.)

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Dynamically Adjustable Output Voltage

The LM3269 features a dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.6 V to 4.2 V by changing the voltage on the analog VCON pin. This feature is useful in cell phone RF PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced; therefore the supply voltage to the PA can be reduced, promoting longer battery life. In order to adaptively adjust the supply voltage to the PA in real time in a cell-phone application, the output voltage transition should be fast enough to meet the RF transmit signal specifications. The LM3269 offers ultra-fast output voltage transition without drawing very large currents from the battery supply. For a current limit of 1700 mA (typical), the output voltage can transition from 1.4 V to 3 V in 10 µs with a load resistance of 11.4 Ω.

7.3.2 Seamless Buck Transition

The LM3269 features a unique internal power switch topology that improves converter efficiency, especially compared to typical non-inverting buck-boost converters. The LM3269 operates either as buck converter or a boost converter, depending upon the input and output voltage conditions. This creates a boundary between the buck and boost mode of operation. When the input battery voltage is close to the set output voltage, the converter automatically switches seamlessly such that the output voltage does not see any perturbations at the mode boundary. The excellent mode transition capability of the LM3269 enables low noise output with highest efficiency. Internal feedback loop compensation ensures stable operation in buck, boost and buck-boost mode transition operation.

7.3.3 Thermal Overload Protection

The LM3269 has a thermal overload protection function that operates to protect itself from short-term misuse and over-load conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. All power MOSFET switches are turned off in PWM mode. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

7.4 Device Functional Modes

7.4.1 Enable And Shutdown Mode

Setting the EN digital pin low (< 0.6 V) places the LM3269 in shutdown mode (0.01 µA typical). During shutdown, the output of the LM3269 is tri-stated, maintaining charge storage on the output capacitor. Setting EN high (> 1.2 V) enables normal operation. EN should be set low to turn off the LM3269 during power up and undervoltage conditions when the power supply (PVIN) is less than the 2.7-V minimum operating voltage.

7.4.2 $V_{CON,ON}$

The output is disabled when VCON is below 125 mV (typical). It is enabled when VCON is above 150 mV (typical). The threshold has approximately 25 mV (typical) of hysteresis.

7.4.3 Pulse Frequency Modulation (PFM) Mode

The LM3269 enters PFM mode and operates with reduced switching frequency and supply current to maintain very high efficiencies when the output voltage is less than 1.5 V. In PFM mode, the LM3269 will support up to 120 mA max. In PFM, if the output voltage exceeds 1.5 V, the device will automatically transition into a forced PWM mode of operation.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Setting The Output Voltage

The LM3269 features a pin-controlled variable output voltage which eliminates the need for external feedback resistors. It can be programmed for an output voltage from 0.6 V to 4.2 V by setting the voltage on the VCON pin, as in Equation 1.

$$V_{OUT} = 3 \times VCON \quad (1)$$

When VCON is between 0.2 V and 1.4 V, the output voltage will follow the formula in Equation 1.

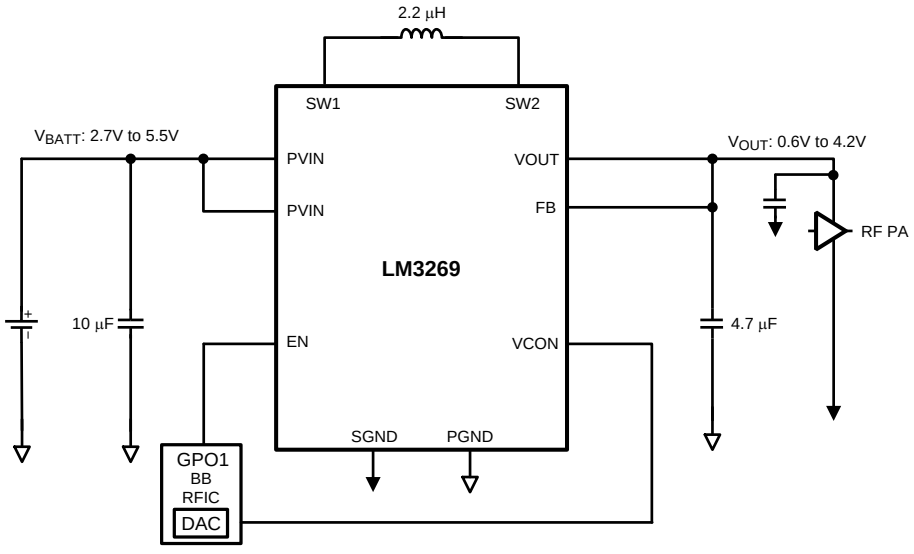
8.1.2 Output Current Capacity

The LM3269 load capability is as shown in Table 1.

Table 1. Output Voltage vs. Maximum Output Current Derating

V_{OUT}	V_{BATT}	MAXIMUM I_{OUT} CAPABILITY
4.2 V	> 3 V	650 mA
	2.7 V to 3 V	500 mA
3.8 V	> 3 V	750 mA
	2.7 V to 3 V	600 mA
< 1.5 V	2.7 V to 5.5 V	120 mA (in PFM mode)

8.2 Typical Application



Typical Application (continued)

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7 V
Minimum output voltage	0.6 V
Output current	0 to 750 mA
Switching frequency	2.4 MHz (typical)

8.2.2 Detailed Design Procedure

8.2.2.1 Recommended External Components

8.2.2.1.1 Inductor Selection

A 2.2-µH inductor with a saturation current rating over 1500 mA and low inductance drop at the full DC bias condition is recommended for almost all applications. An inductor with a smaller DC resistance, such as 110 mΩ (depending on case size of resistor), should be used for good efficiency.

Table 2. Suggested 2.2-µH Inductors

VENDOR	MODEL	DIMENSIONS (mm)	I_{SAT} (30% drop)	I_{RATING} (Δ40°)	DCR
FDK	MIPSZ2520D2R2	2.5 x 2.0 x 1.0	1.5 A	1.1 A	110 mΩ
Murata	LQH2HPN1R0NG0	2.5 x 2.0 x 1.2	2 A	1.2 A	112 mΩ
Samsung	CIG22H2R2MNE	2.5 x 2.0 x 1.2	1.9 A	1.6 A	116 mΩ
TDK	TFM201610A2R2M	2.0 x 1.6 x 1.0	1.7 A	1.3 A	180 mΩ
TOKO	DFE201612C2R2N	2.0 x 1.6 x 1.2	2.1 A	1.3 A	155 mΩ

8.2.2.1.2 Input Capacitor Selection

A ceramic input capacitor of 10 µF, 6.3 V, 0603 (1608) is recommended for use in most applications. Place the input capacitor as close as possible to the PVIN pin and PGND pin of the device. A larger value of higher voltage rating may be used to improve input filtering. Use X7R, X5R, or B types; do not use Y5V or F. DC board characteristics of ceramic capacitors must be considered when selecting case sizes like 0402 (1005). The input filter capacitor supplies current to the PFET (high-side) switch in first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low equivalent series resistance (ESR) provides the best noise filtering of the input voltage spikes due to this rapidly changing current.

8.2.2.1.3 Output Capacitor Selection

Use a 4.7 µF capacitor for the output capacitor. Use of capacitor types such as X5R, X7R are recommended for the filter. These provide an optimal balance between small size, cost, reliability, and performance for cell phones and similar applications. Table 3 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller case sizes for the output capacitor mitigate piezo-electric vibrations of the capacitor when the output voltage is stepped up and down at fast rates. However, they have a bigger percentage drop in value with DC bias. A 0603 (1608) case size capacitor is recommended for output. For RF Power Amplifier applications, split the output capacitor between DC-DC converter and RF Power Amplifier(s). (4.7 µF (0402 (1005)) + PA input cap (0402(1005)/0201(0603)) is recommended.) The optimum capacitance split is application dependent. Place all the output capacitors very close to their respective device.

NOTE

If using a 4.7 µF, 0402 (1005) as the output capacitor, the total recommended actual capacitance on V_{OUT} bus should be at least 7 µF (4.7 µF + PA decoupling caps) to take into account the 0402 (1005) DC bias degradation and other tolerances.

Table 3. Suggested Capacitors

MODEL	VENDOR
10 µF for C_{IN}	
C1608X5R0J106K (0603)	TDK
CL05A106MQ5NUN (0402)	Samsung
4.7 µF for C_{OUT}	
C1608X5R0J475M (0603)	TDK
CL05A475MQ5NRN (0402)	Samsung
C1005X5RR0J475M (0402)	TDK

8.2.3 Application Curves

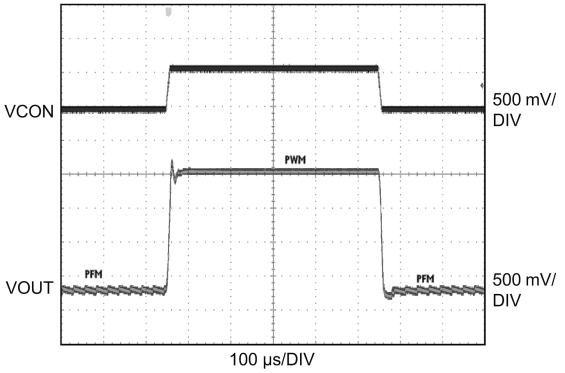


Figure 9. V_{OUT} Transient Response (PFM ↔ PWM)

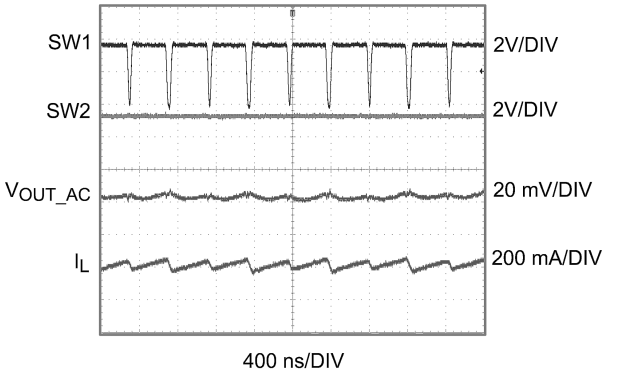


Figure 10. Buck Mode Operation

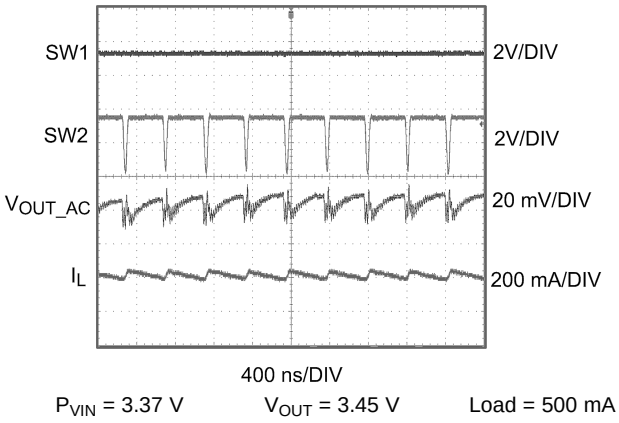


Figure 11. Boost Mode Operation

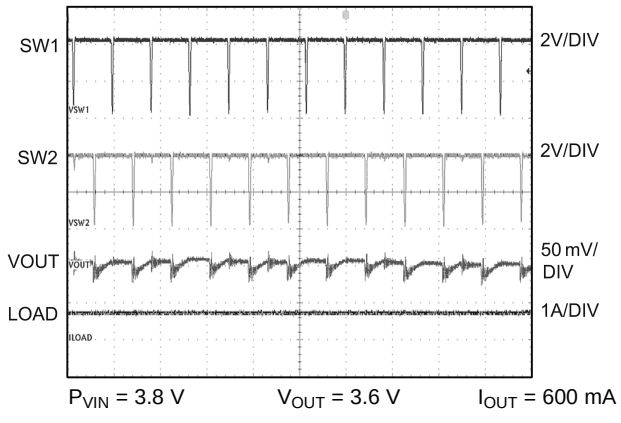


Figure 12. Buck-Boost Operation

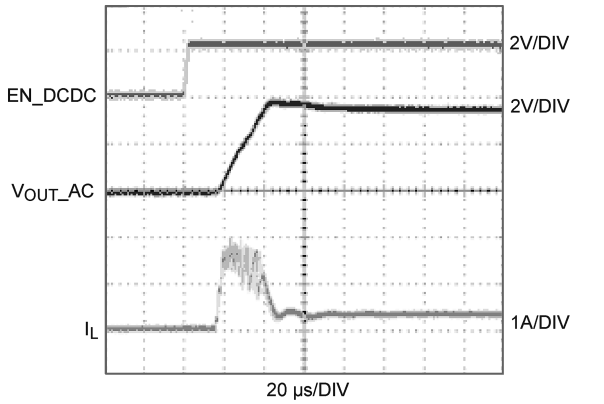


Figure 13. Start-Up

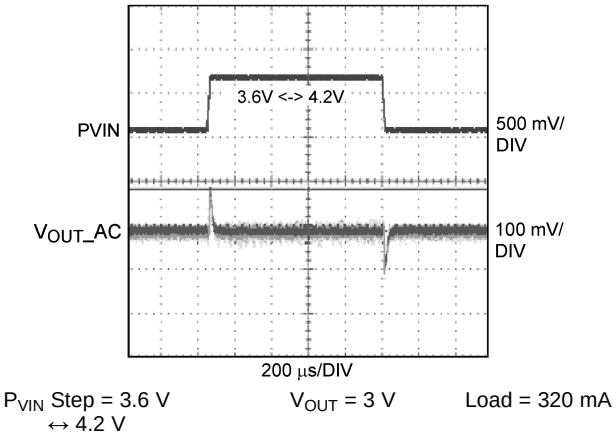


Figure 14. Line Transient For DC-DC

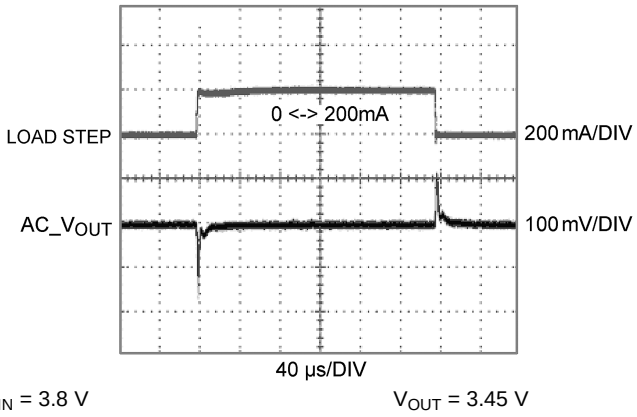


Figure 15. Load Transient DC-DC

9 Power Supply Recommendations

The LM3269 device is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply should be well regulated. If the input supply is located more than a few inches from the LM3269 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

10.1.1 Overview

PC board layout is critical to successfully designing a DC-DC converter into a product. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impact on board quality and final product yield.

10.1.1.1 PCB

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

10.1.1.1.1 Energy Efficiency

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

10.1.1.1.2 EMI

By its very nature, any switching converter generates electrical noise. The circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3269, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To help minimize radiated noise:

- Place the LM3269 switcher, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle (buck mode), current flows from the input filter capacitor, through the internal PFET of the LM3269 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle (buck mode), current is pulled up from ground, through the internal synchronous NFET of the LM3269 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible.

To help minimize conducted noise in the ground-plane:

- Reduce the amount of switching current that circulates through the ground plane: Connect the ground bumps of the LM3269 and its input/output filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) by multiple vias. These multiple vias help to minimize ground bounce at the LM3269 by giving it a low-impedance ground connection.

To help minimize coupling to the DC-DC converter's own voltage feedback trace:

- Route noise sensitive traces, such as the voltage feedback path (FB), as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components. If possible, connect FB bump directly to VOUT bump.

To decouple common power supply lines, series impedances may be used to strategically isolate circuits:

- Take advantage of the inherent inductance of circuit traces to reduce coupling among function blocks, by way of the power supply traces.
- Use star connection for separately routing VBATT to PVIN and VBATT_PA (VCC1).
- Inserting a single ferrite bead in-line with a power supply trace may offer a favorable tradeoff in terms of board area, by allowing the use of fewer bypass capacitors.

Layout Guidelines (continued)

10.1.1.2 Manufacturing Considerations

The LM3269 package employs a 12-bump (4 x 3) array of 300 micron solder balls, with a 0.5 mm pad pitch. A few simple design rules will go a long way toward ensuring a good layout.

- Pad size should be 0.265 ± 0.02 mm. Solder mask opening should be 0.375 ± 0.02 mm.
- As a thermal relief, connect to each pad with 9.5 mil wide, 5 mil long traces and incrementally increase each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly. Refer to TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

10.1.1.3 LM3269 RF Evaluation Board

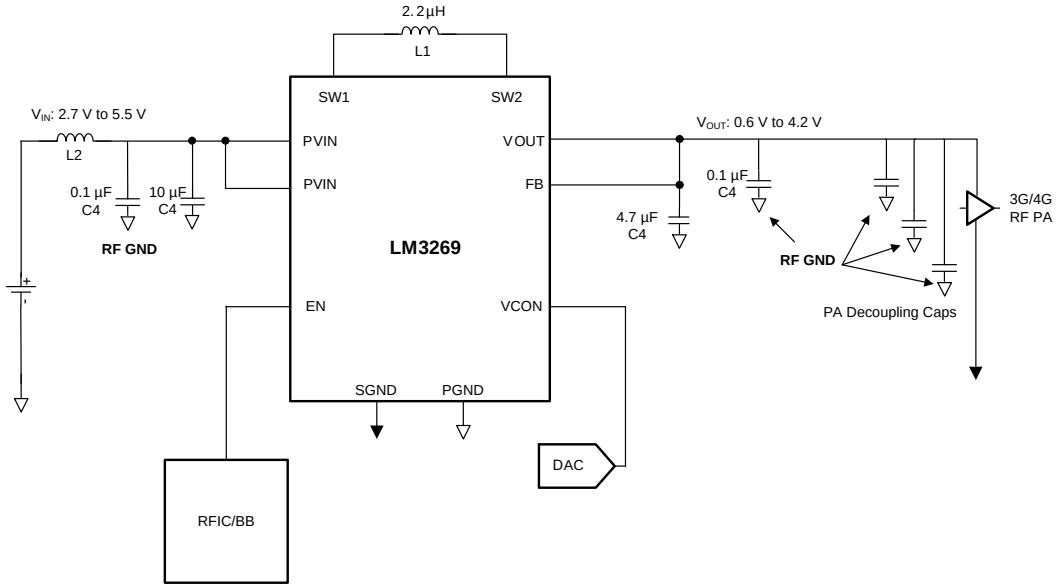


Figure 16. Simplified LM3269 RF Evaluation Board Schematic

1. Input Capacitor C2 should be placed closer to LM3269 than C1.
2. It is optional to add 100 nF (C1) on input of LM3269 for high frequency filtering.
3. Bulk Output Capacitor C3 should be placed closer to LM3269 than C4.
4. It is optional to add 100 nF (C4) on output of LM3269 for high frequency filtering.
5. Connect both GND terminals of C1 and C4 directly to System RF GND layer of phone board.
6. Connect bumps SGND (C2) directly to System GND.
7. TI has seen improvement in high frequency filtering for small bypass capacitors (C1 and C4) when they are connected to System GND instead of same ground as PGND. These capacitors should be 0201 (0603 metric) case size for minimum footprint and best high frequency characteristics.
8. A ferrite bead (L2) may help to improve high frequency noise.

Table 4. Recommended Components

DESIGNATOR	PART NUMBER	VALUE	CASE SIZE	VENDOR
C1*	GMR033R60J104KE19D	0.1 µF	0201 (0603 metric)	Murata
C2	C1608X5R0J106	10 µF	0603 (1608 metric)	TDK
C3	C1608X5RR0J475M	4.7 µF	0603 (1608 metric)	TDK
C4*	GRM033R60J104KE19D	0.1 µF	0201 (0603 metric)	Murata
L1	MIPSZ2520D2R2	2.2 µH	1008 (2520 metric)	FDK
L2*	BLM15AX100SN1	10 Ω	0402 (1005 metric)	Murata
*Optional high frequency caps and high-frequency ferrit bead.				

10.1.1.4 Component Placement

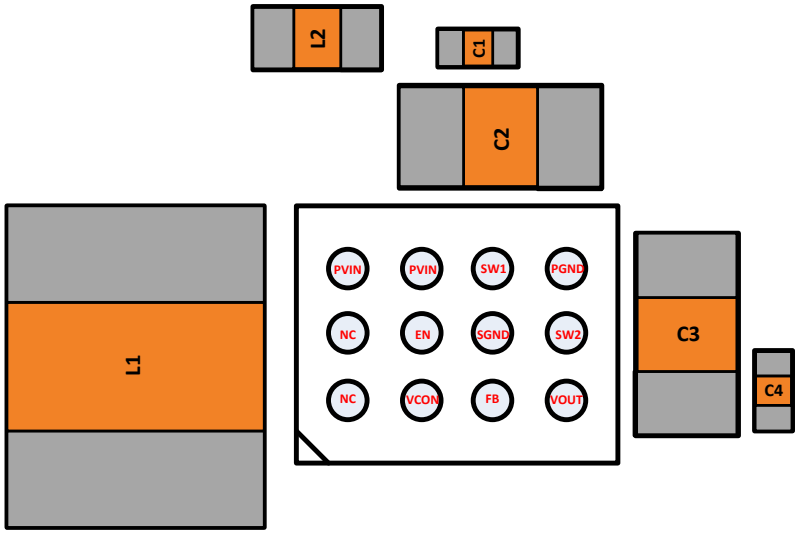


Figure 17. LM3269 Recommended Parts Placement (Top View)

10.1.1.5 PCB Considerations By Layer

10.1.1.5.1 VBATT

Use a star connection from VBATT to LM3269 and VBATT to PA VBATT (VCC1) connection. Do not daisy-chain VBATT connection to LM3269 circuit and then to PA device VBATT connection.

Top Layer (Numbers correspond to those in the *Layout Examples* section.)

1. Create a PGND island as shown. PGND pads of C2 (CIN) and C3 (COUT) must be isolated from each other. This PGND island will connect to the dedicated system ground with many vias.
2. Each SW (C3) and (D2) bump will have a via in pad and an additional via next to it, to drop down the SW trace to layer
3. SGND bump (C2) will have a via in pad, and directly connecting it to the system ground.
4. FB (C1) should connect directly to the VOUT bump (D1).
5. Have PVIN vias next to optional ferrite bead.
6. Leave NC bumps (A1 and A2) floating; Do not connect to VBATT or GND

Layer 2

7. VCON and Digital logic signals may be routed on this layer.
8. VOUT (VCC2 of PA) can be routed on this layer.
9. PVIN for the LM3269 can be routed on this layer.

Layer 3

10. Each SW trace is routed on this layer. The width of each trace should be 15 mils (0.381 mm) for current capabilities. Have two vias bring each SW trace up to the inductor pads.

Layer 4

11. Connect the PGND, SGND, and high Frequency vias from the top layer on this layer.

10.2 Layout Examples

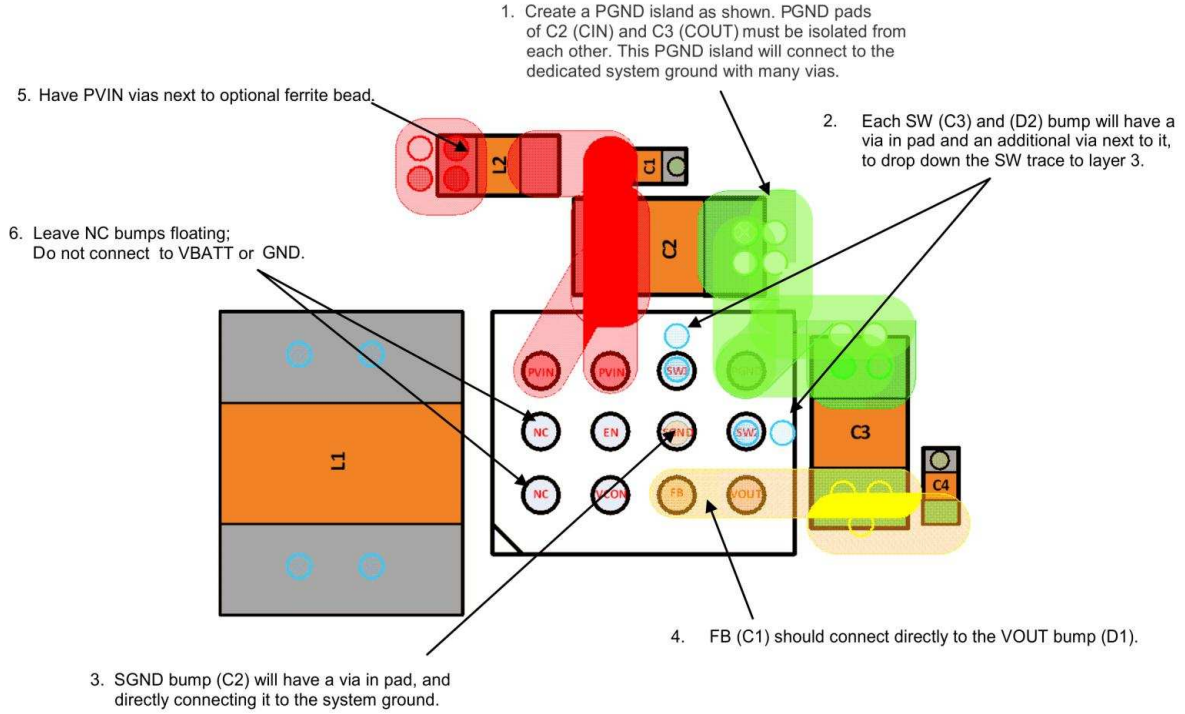


Figure 18. Top Layer

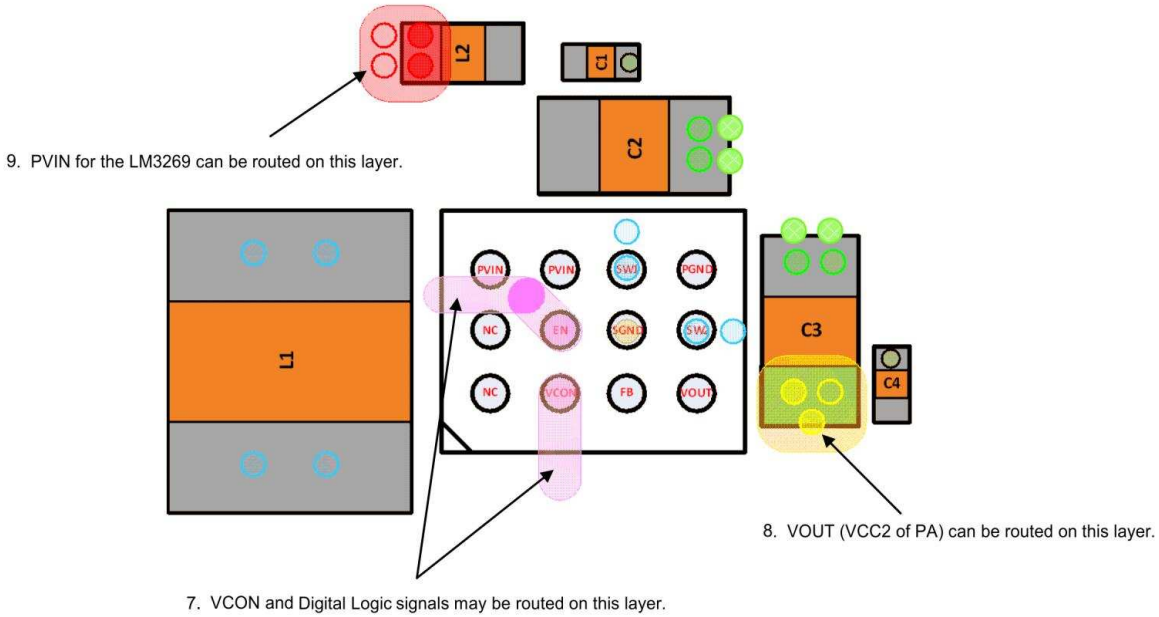


Figure 19. Board Layer 2 - Logic and PVIN Routing

Layout Examples (continued)

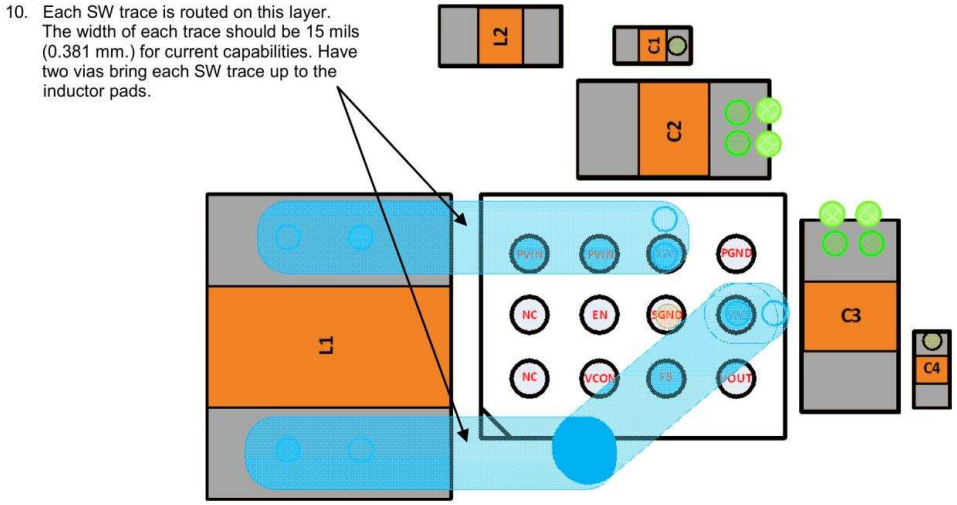


Figure 20. Board Layer 3 - SW Routing

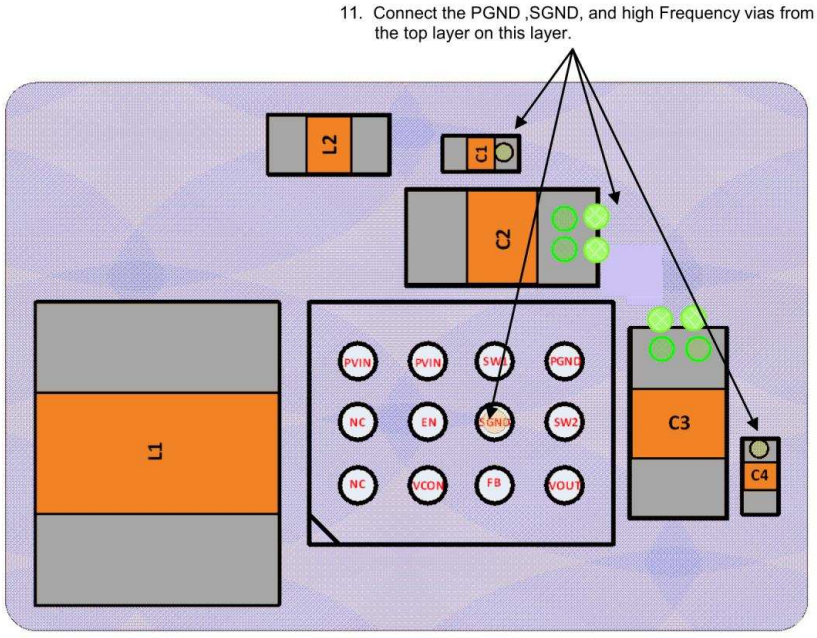


Figure 21. Board Layer 4 - System

10.3 DSBGA Package Assembly And Use

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap from holding the device off the surface of the board and interfering with mounting. See Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009) for specific instructions how to do this.

The 12-bump package used for the LM3269 has 300 micron solder balls. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 9.5 mil wide, for a section approximately 5 mil long, as a thermal relief. Then each trance should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3269 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A3, B3, and D3. Because PVIN and PGND are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light (in the red and infrared range) shining on the package's exposed die edges.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3269TLE/NOPB	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3269
LM3269TLE/NOPB.A	Active	Production	DSBGA (YZR) | 12	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3269
LM3269TLX/NOPB	Active	Production	DSBGA (YZR) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3269
LM3269TLX/NOPB.A	Active	Production	DSBGA (YZR) | 12	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-30 to 85	3269

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

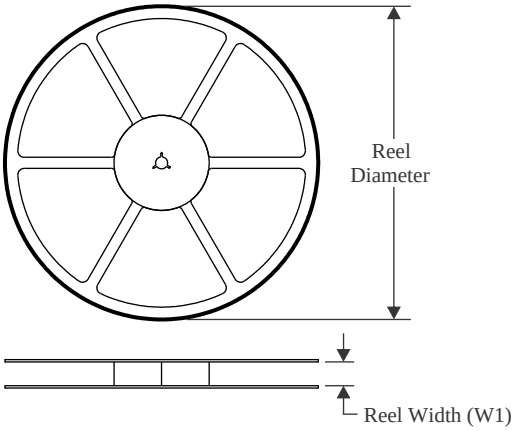
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

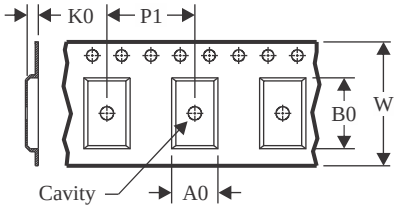
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

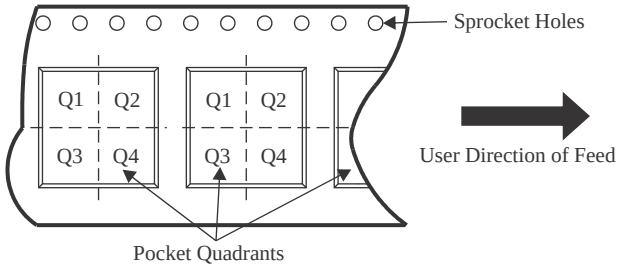


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

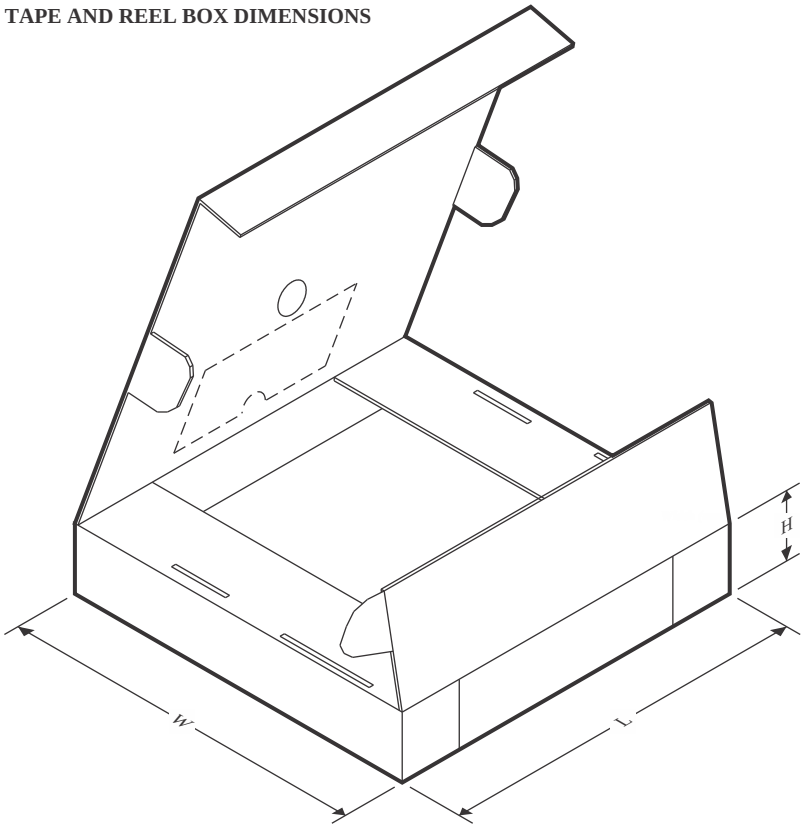
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3269TLE/NOPB	DSBGA	YZR	12	250	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1
LM3269TLX/NOPB	DSBGA	YZR	12	3000	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1

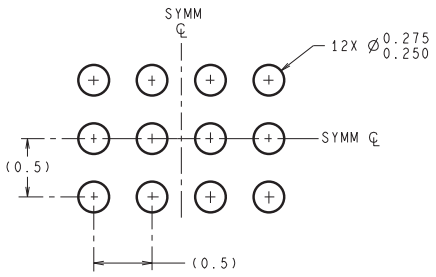
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

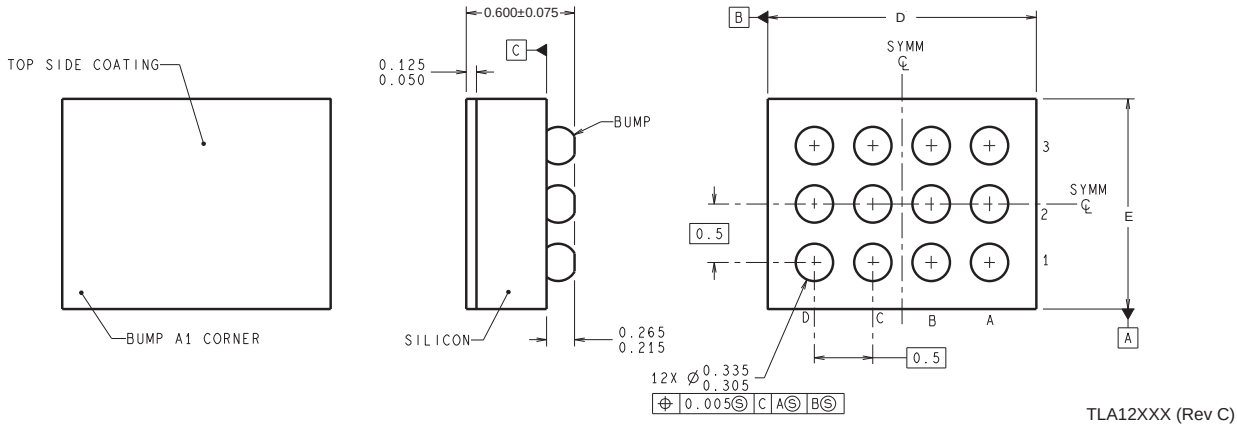
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3269TLE/NOPB	DSBGA	YZR	12	250	208.0	191.0	35.0
LM3269TLX/NOPB	DSBGA	YZR	12	3000	208.0	191.0	35.0

YZR0012



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TLA12XXX (Rev C)

D: Max = 2.529 mm, Min =2.469 mm

E: Max = 2.022 mm, Min =1.961 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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