LM3302 Quad Differential Comparator

1 Features

- Single supply or dual supplies
- Wide range of supply voltage . . . 2V to 28V
- Low supply-current drain independent of supply voltage . . . 0.8mA typical
- Low input bias current . . . 25nA typical
- Low input offset current . . . 3nA typical
- Low input offset voltage . . . 3mV typical
- Common-mode input voltage range includes ground
- Differential input voltage range equal to maximum-rated supply voltage: ±28V
- Low output saturation voltage
- Output compatible with TTL, MOS, and CMOS
- For wider temperature range, see the LM2901
- For single version, see the TL331
- For dual version, see the LM393 or LM2903

2 Applications

- Vacuum robot
- Single phase UPS
- Server PSU
- Cordless power tool
- Wireless infrastructure
- Applicances
- Building automation
- Factory automation & control
- Motor drives
- Infotainment & cluster

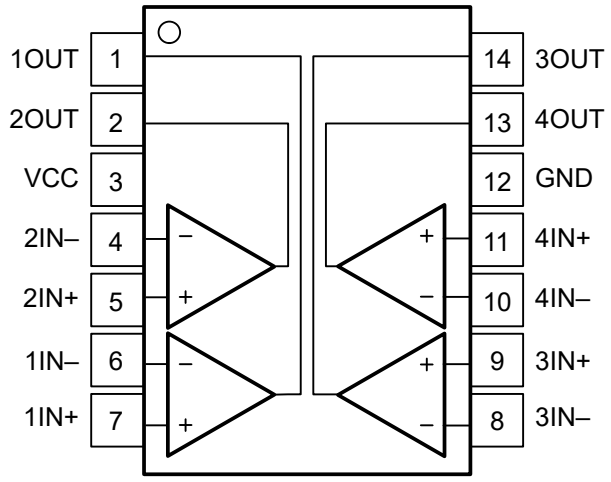
3 Description

This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is 2V to 28V and VCC is a least 1.5V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
LM3302	SOIC (14)	8.70mm × 3.90mm
	PDIP (14)	19.30mm × 6.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



LM3302 Pinout

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4 Pin Configuration and Functions

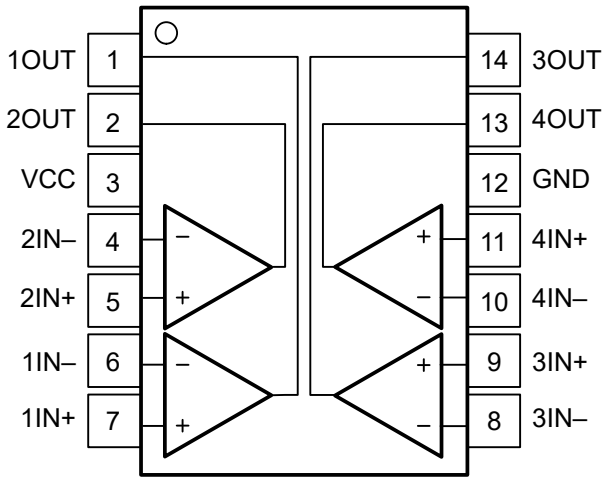


Figure 4-1. D, N Packages
14-Pin SOIC, PDIP
Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME[1]	D, N		
OUT1 [1]	1	Output	Output pin of the comparator 2
OUT2 [1]	2	Output	Output pin of the comparator 1
V_{CC}	3	—	Positive supply
IN2– [1]	4	Input	Negative input pin of the comparator 1
IN2+ [1]	5	Input	Positive input pin of the comparator 1
IN1– [1]	6	Input	Negative input pin of the comparator 2
IN1+ [1]	7	Input	Positive input pin of the comparator 2
IN3–	8	Input	Negative input pin of the comparator 3
IN3+	9	Input	Positive input pin of the comparator 3
IN4–	10	Input	Negative input pin of the comparator 4
IN4+	11	Input	Positive input pin of the comparator 4
GND	12	—	Negative supply
OUT4	13	Output	Output pin of the comparator 4
OUT3	14	Output	Output pin of the comparator 3

(1) Some manufacturers transpose the names of channels 1 & 2. Electrically the pinouts are identical, just a difference in the channel naming convention.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		28	V
Differential input voltage : V_{ID} (2)		±28	V
Input pins (IN+, IN–)	-0.3	28	V
Current into input pins (IN+, IN–)		-20	mA
Output pin (OUT)	-0.3	28	V
Output sink current		20	mA
Output short-circuit duration(3)		Unlimited	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Differential voltages are at IN+ with respect to IN-
(3) Short circuits from outputs to V+ can cause excessive heating and eventual destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Human-body model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	2	28	V
Ambient temperature, T_A	–40	85	°C
Input Voltage Range, V_{IVR}	V-	(V+) – 2.0	V
Output Voltage	V-	28	V

5.4 Thermal Information

THERMAL METRIC(1)		LM3302		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.9	111.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	66.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.7	67.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	60.4	28.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.7	67.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semicondctor and IC Package Thermal Metrics report, SPRA953.

5.5 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		T_A	LM3302			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, V_O = 1.4V, V_{CC} = 5V to 28V		25°C		3	20	mV
				-40°C to +85°C			40	
I_{IO}	Input offset current	V_O = 1.4V		25°C		3	100	nA
				-40°C to +85°C			300	
I_{IB}	Input bias current			25°C		–25	–500	nA
				-40°C to +85°C			–1000	
V_{ICR}	Common-mode input-voltage range			25°C	0 to V_{CC} – 1.5			V
				-40°C to +85°C	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15V, V_O = 1.4V to 11.4V, R_L ≥ 15kΩ to V_{CC}		25°C	2	30		V/mV
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V	25°C		0.1		nA
				-40°C to +85°C			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1V	I_{OL} = 4mA	25°C		150	500	mV
				-40°C to +85°C			700	
I_{OL}	Low-level output current	V_{ID} = –1V,	V_{OL} = 1.5V	25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5V, No load	V_{CC} = 5V	25°C		0.8		mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		LM3302	UNIT
			TYP	
Response time	R_L connected to 5V through 5.1kΩ, C_L = 15pF[1] [2]	100mV input step with 5mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

5.7 Typical Characteristics

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

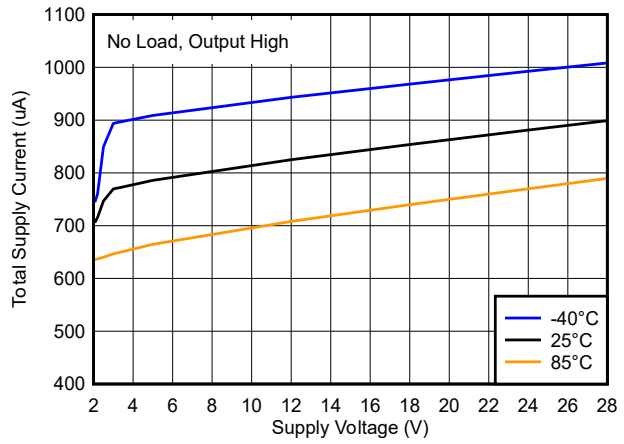


Figure 5-1. Total Supply Current vs. Supply Voltage

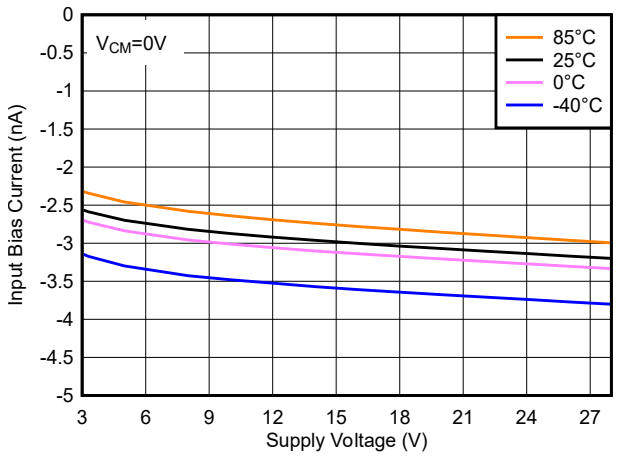


Figure 5-2. Input Bias Current vs. Supply Voltage

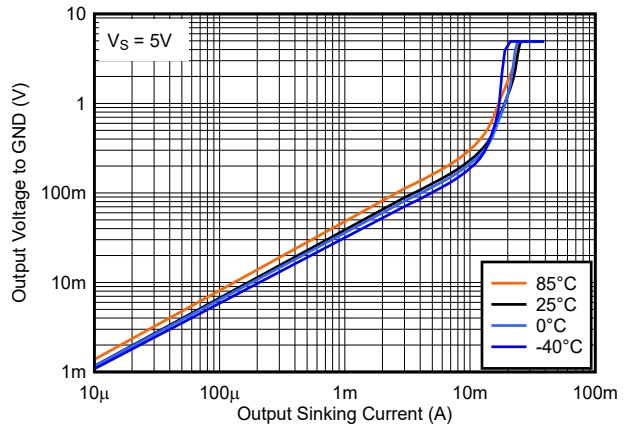


Figure 5-3. Output Low Voltage vs. Output Sinking Current at 5V

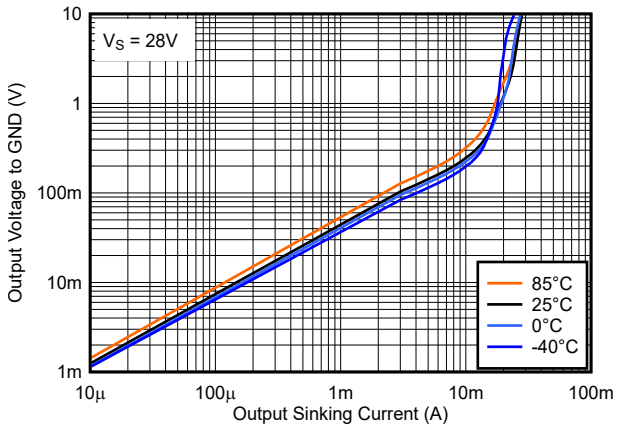


Figure 5-4. Output Low Voltage vs. Output Sinking Current at 28V

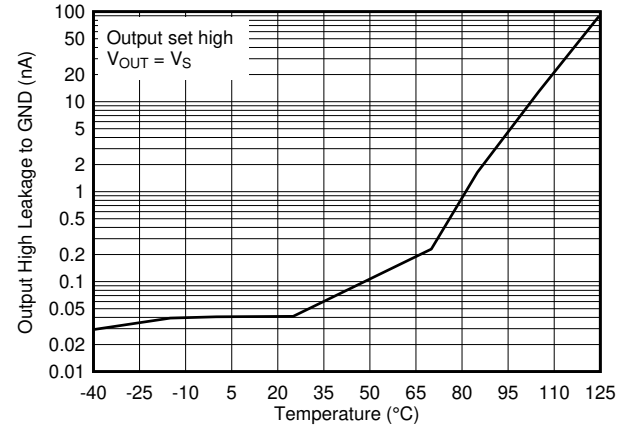


Figure 5-5. Output High Leakage Current vs. Temperature at 5V

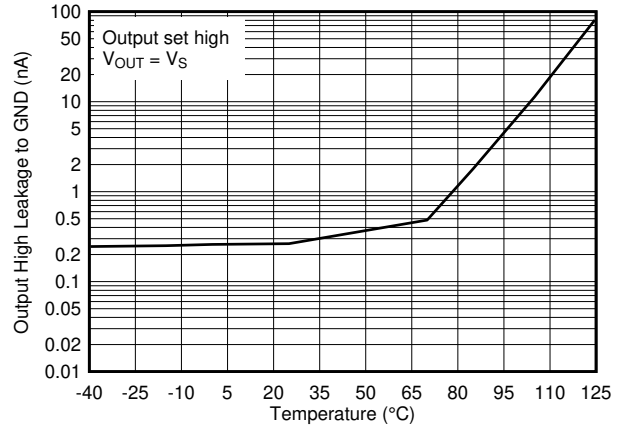


Figure 5-6. Output High Leakage Current vs. Temperature at 28V

5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

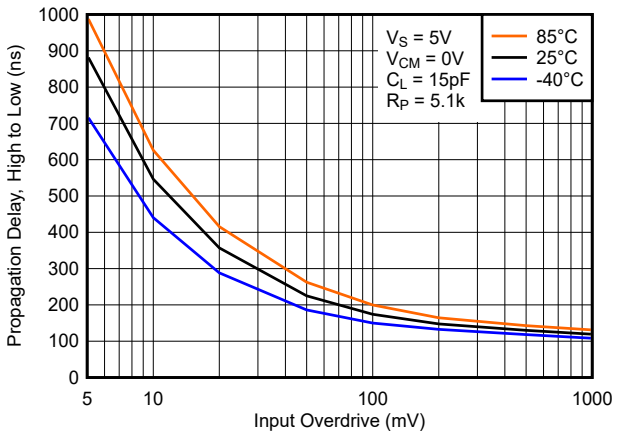


Figure 5-7. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

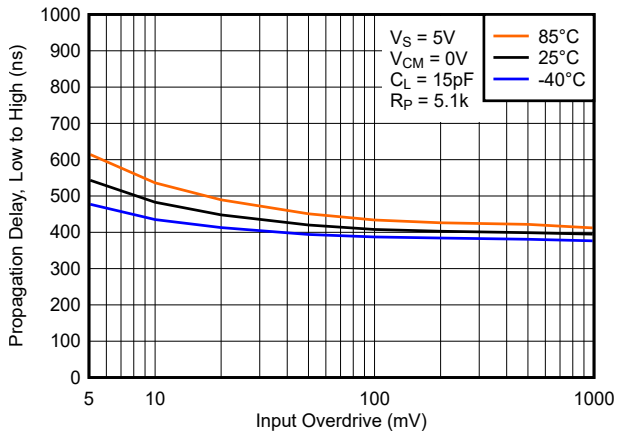


Figure 5-8. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

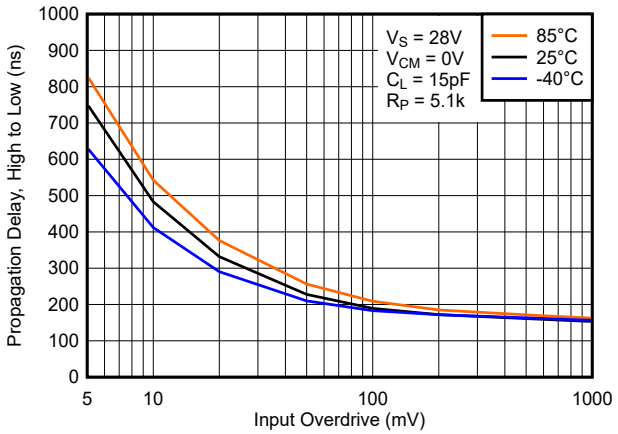


Figure 5-9. High to Low Propagation Delay vs. Input Overdrive Voltage, 28V

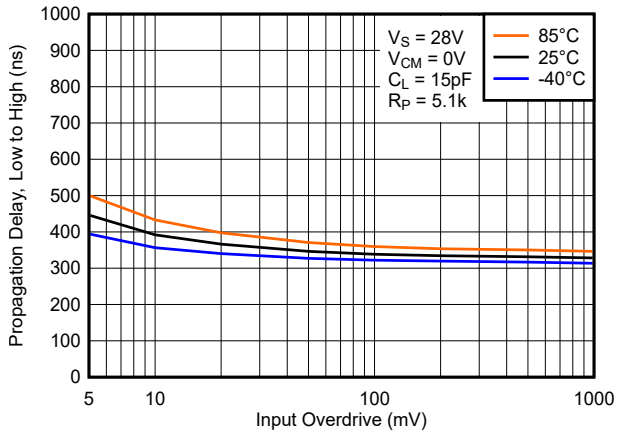


Figure 5-10. Low to High Propagation Delay vs. Input Overdrive Voltage, 28V

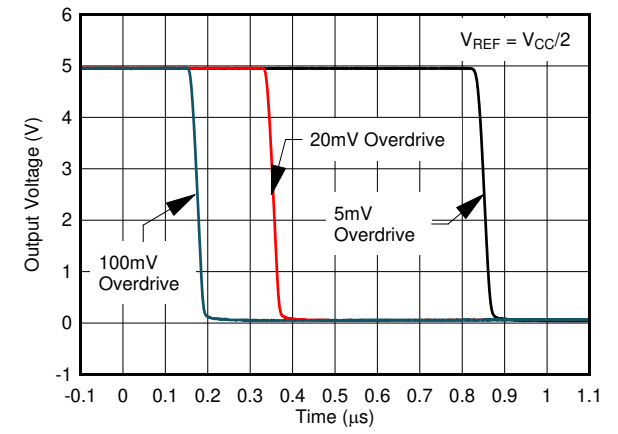


Figure 5-11. Response Time for Various Overdrives, High-to-Low Transition

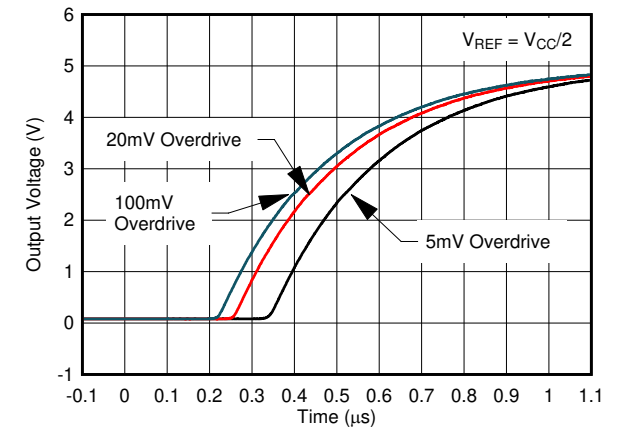


Figure 5-12. Response Time for Various Overdrives, Low-to-High Transition

6 Detailed Description

6.1 Overview

These quad comparators have the ability to operate up to absolute maximum of 28V on the supply pin. This device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range, low Iq and fast response of the devices.

The open-collector outputs allow the user to level shift to the desired logic level independent of VCC, while also enabling AND functionality when multiple outputs are connected together.

6.2 Functional Block Diagram

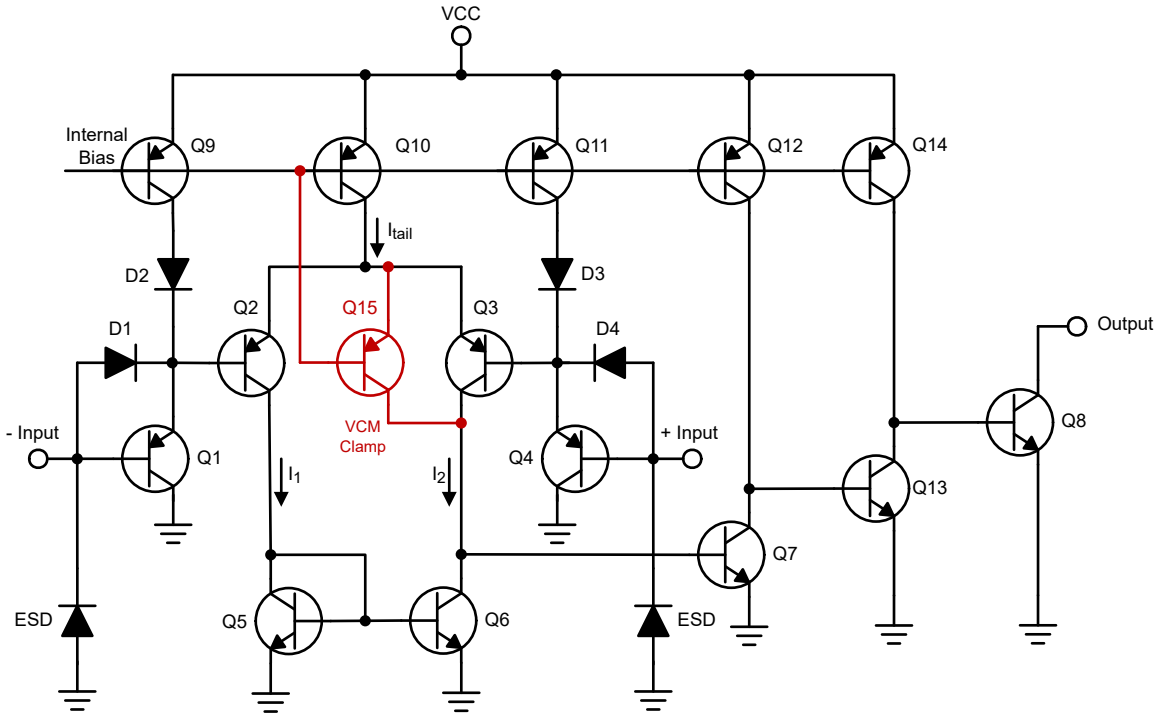


Figure 6-1. Schematic (Each Comparator)

6.3 Feature Description

The comparator consists of a PNP Darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing the comparator to accurately function from ground to V_{CC}– 2V over temperature. A clamp was added around Q3 to mimic the both inputs above input voltage range behavior of the original classic silicon.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. Please see the "Output Low Voltage vs. Output Sinking Current" graphs for V_{OL} values with respect to the output current.

6.4 Device Functional Modes

6.4.1 Voltage Comparison

The comparator operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Typically, a comparator compares either a single signal to a reference, or to two differnt signals. Many users take advantage of the open-drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM3302 an excellent choice for level shifting to a higher or lower voltage.

7.2 Typical Application

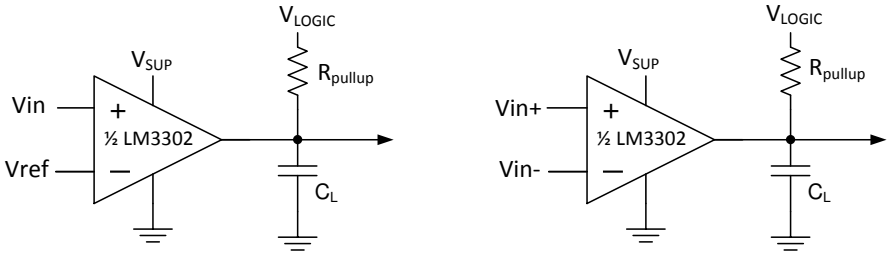


Figure 7-1. Single-ended and Differential Comparator Configurations

7.2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to Vsup-2V
Supply Voltage	4.5V to V_{CC} maximum
Logic Supply Voltage	0V to V_{CC} maximum
Output Current (R_{PULLUP})	1µA to 4mA
Input Overdrive Voltage	100mV
Reference Voltage	2.5V
Load Capacitance (C_L)	15pF

7.2.2 Detailed Design Procedure

When using the LMx39 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

7.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is below 25°C the V_{ICR} can range from 0V to V_{CC}– 2.0V. This limits the input voltage range to as high as V_{CC}– 2.0V and as low as 0V. Operation outside of this range can yield incorrect comparisons.

The following is a list of input voltage situation and the outcomes:

1. When both IN- and IN+ are both within the common-mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common-mode, see Section 2 of Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions.

7.2.2.2 Minimum Overdrive Voltage

Overdrive voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison, the overdrive voltage (V_{OD}) must be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 7-2 and Figure 7-3 show positive and negative response times with respect to overdrive voltage.

7.2.2.3 Output and Drive Current

Output current is determined by the load and pullup resistance and logic and pullup voltage. The output current produces a low-level output voltage (V_{OL}) from the comparator, where V_{OL} is proportional to the output current.

The output current can also effect the transient response.

7.2.2.4 Response Time

Response time is a function of input over-drive. See the Typical Characteristics graphs for typical response times. The rise and fall times can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R = R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F = R_{CE} \times C_L$
  – R_{CE} can be determined by taking the slope of Figure 5-11 in the linear region at the desired temperature, or by dividing the V_{OL} by I_{OUT}

7.2.3 Application Curves

Figure 7-2 and Figure 7-3 were generated with scope probe parasitic capacitance of 50pF.

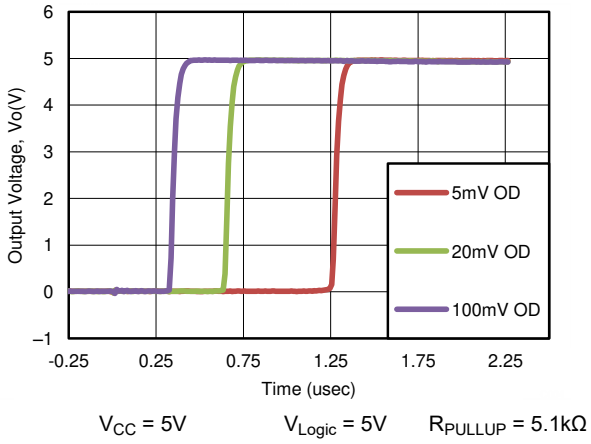


Figure 7-2. Response Time vs Output Voltage (Positive Transition)

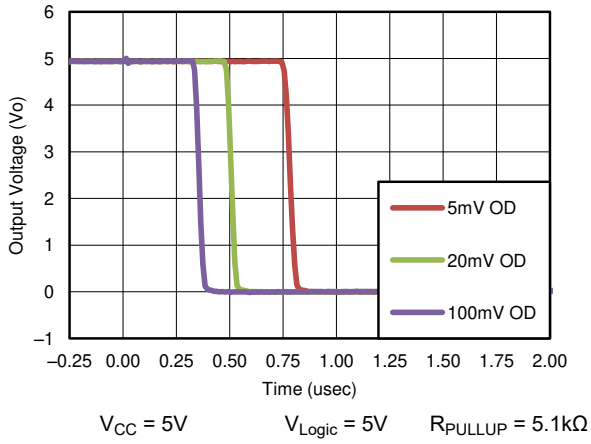


Figure 7-3. Response Time vs Output Voltage (Negative Transition)

7.3 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can affect the common-mode range of the comparator input and create an inaccurate comparison.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications without hysteresis maintaining a stable power supply with minimized noise and glitches is critical. Best practice is to add a bypass capacitor between the supply voltage and ground. This can be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the GND pin and system ground.

Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V_{CC} or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.

7.4.2 Layout Example

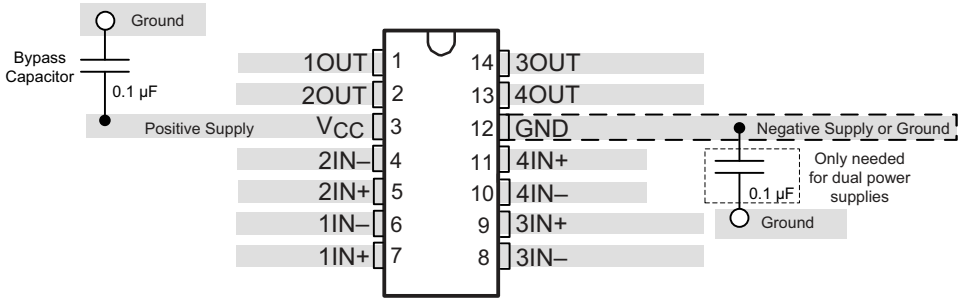


Figure 7-4. LM3302 Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2003) to Revision B (April 2025)	Page
• Updated to current TI data sheet format. No changes to Electrical Table specs	1
• Updated ESD table for new packages	4
• Updated Thermal Information table for new packages	4
• Added Typical Graphs	6
• Updated Functional Block Diagram	8

Changes from Revision * (October 1977) to Revision A (August 2003)	Page
• Removed Ceramic 'J' package. Added SOIC ordering options	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3302D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	LM3302
LM3302DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LM3202, LM3302)
LM3302DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LM3202, LM3302)
LM3302DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
LM3302N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LM3302N
LM3302N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	LM3302N

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

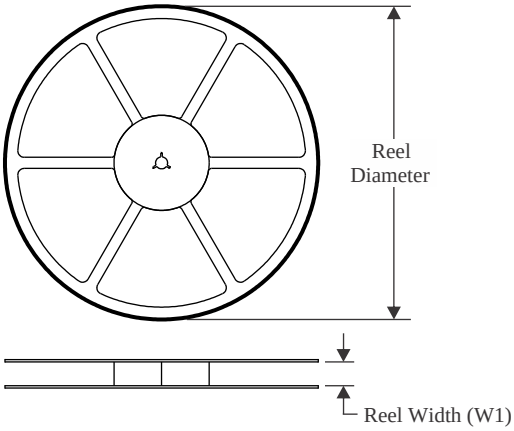
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

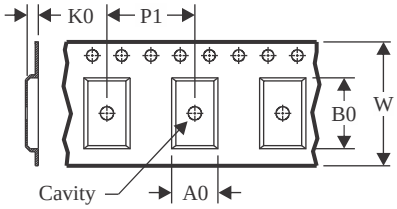
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

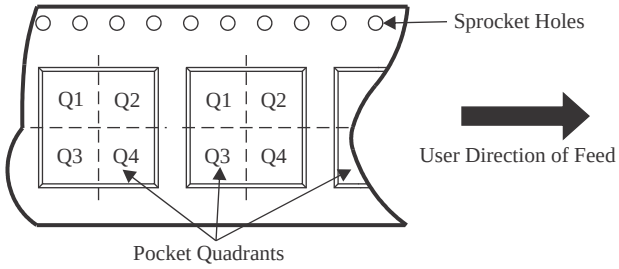


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

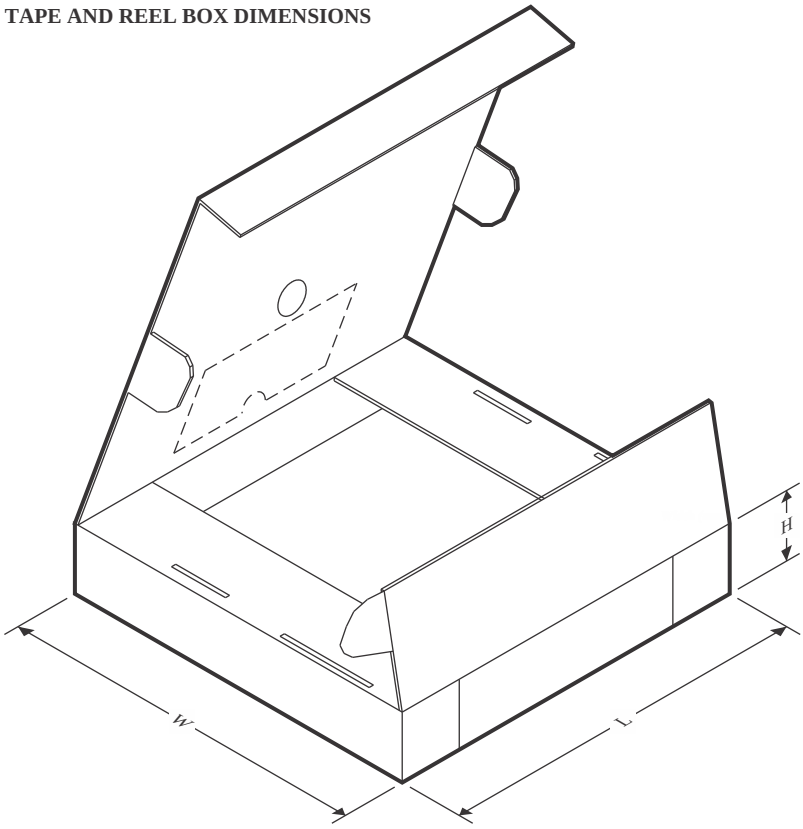
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3302DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM3302DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

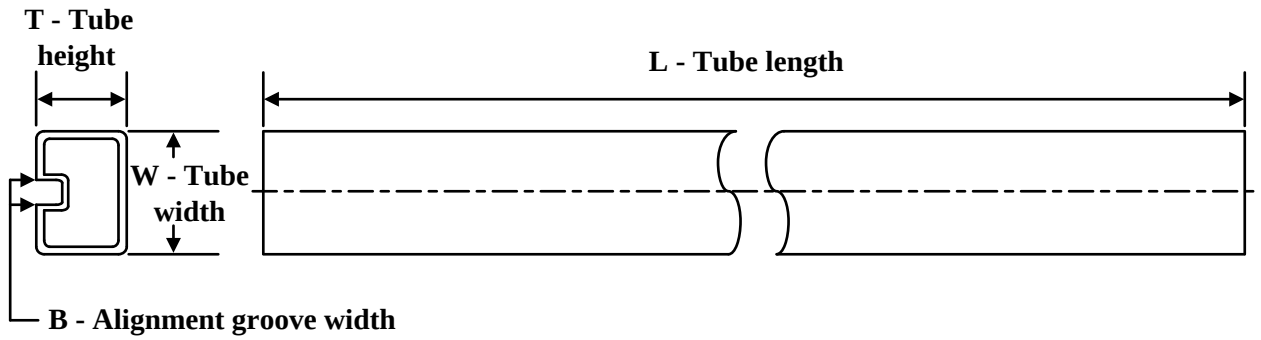
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

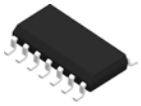
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3302DR	SOIC	D	14	2500	353.0	353.0	32.0
LM3302DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM3302N	N	PDIP	14	25	506	13.97	11230	4.32
LM3302N	N	PDIP	14	25	506	13.97	11230	4.32
LM3302N.A	N	PDIP	14	25	506	13.97	11230	4.32
LM3302N.A	N	PDIP	14	25	506	13.97	11230	4.32

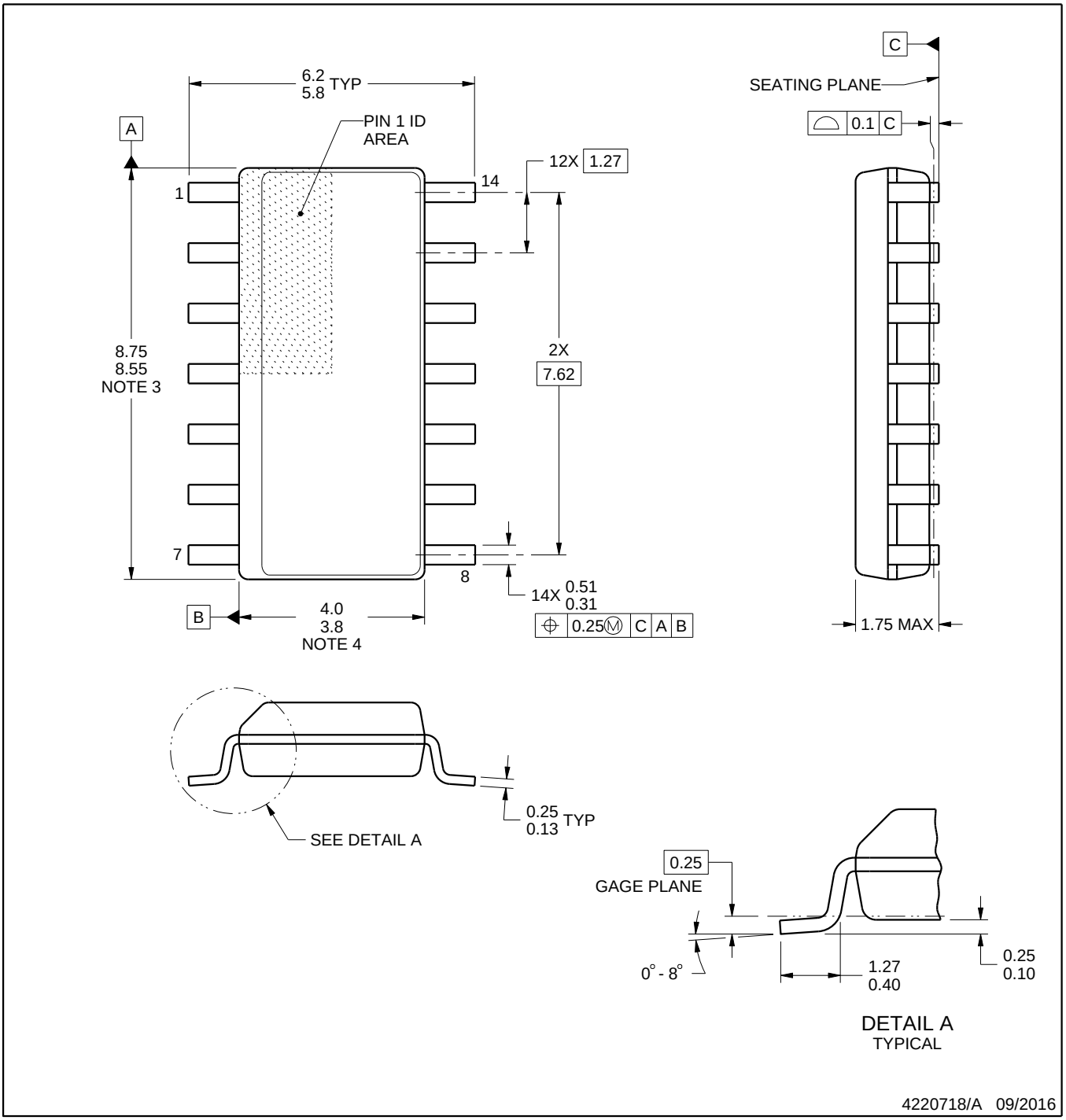


PACKAGE OUTLINE

D0014A

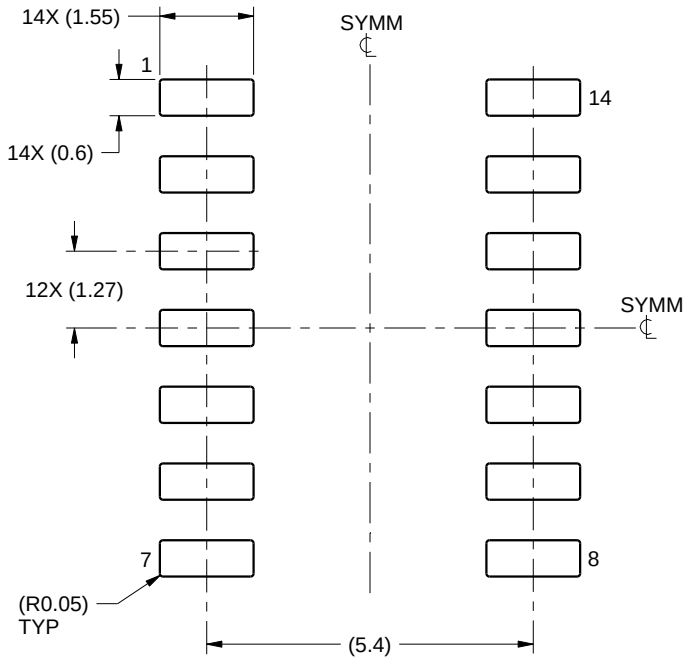
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

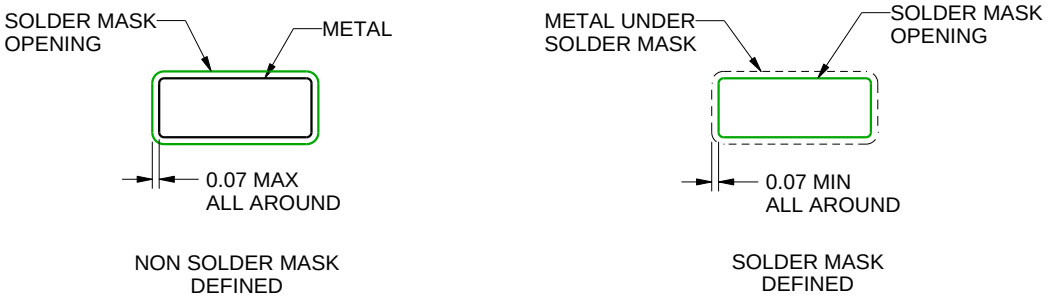


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

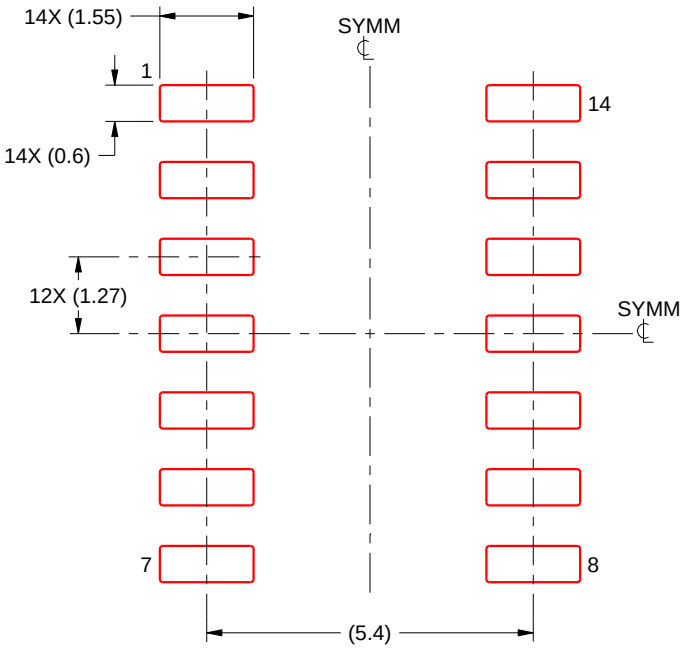
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

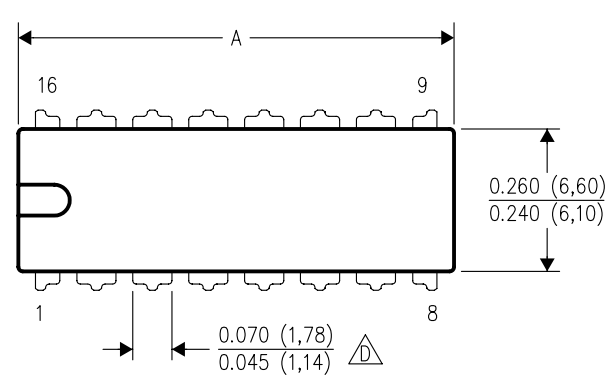
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

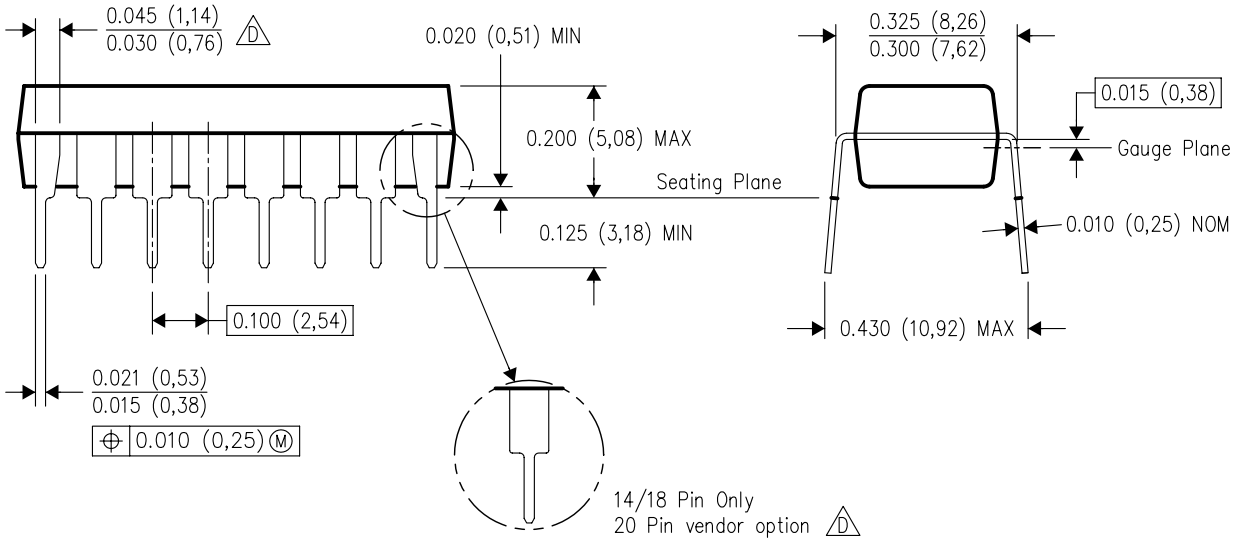
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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