LM72630-Q1 70V, 3A, Automotive, High-Efficiency CC-CV Buck Converter With I²C

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Synchronous CC-CV buck converter with I²C
  - Wide input voltage range: 4.5V to 70V
    - Meets LV148 / ISO21780 requirements
  - Programmable V_{OUT} from 1V to 24V in 10mV steps or from 3.3V to 24V in 20mV steps
  - Programmable $I_{LIM(avg)}$ from 0.5A to 4.5A
  - Adjustable cable drop compensation (CDC)
  - Analog current monitoring pin (IMON)
- Compatible with TPS2674X-Q1 USB Type-C® power delivery (PD) controllers
- Designed for low EMI requirements
  - Facilitates CISPR 25 Class 5 compliance
  - ±5% dual-random spread spectrum with programmable modulation frequency
  - Programmable f_{SW}: 200kHz to 2.2MHz
- Programmable protection features
  - UV/OV (PG) warning: ±5% or ±10%
  - OVP warning, fault: 105% to 136% in 1% steps
  - HICCUP-mode OCP, TSD
- 6mm × 6mm thermally optimized, RoHS compliant, VQFN-29 package with Pb-free plating
- Create a custom design using the LM72630-Q1 with the WEBENCH® Power Designer

2 Applications

- Automotive electronic systems
- Infotainment and cluster
- Automotive USB charging

3 Description

The LM72630-Q1 is a 70V, synchronous buck converter with constant-current constant-voltage (CC-CV) regulation and I²C interface. The device is compatible with USB Type-C PD controllers including the TPS2674X-Q1 family.

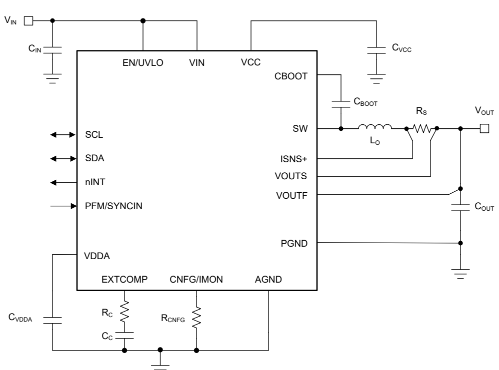
The converter uses a peak current-mode control architecture for easy loop compensation, fast transient response, and excellent load and line regulation. The highly accurate CC-CV operation enables seamless transition between constant-current and constant-voltage modes. The I²C interface allows programming of output voltage in 10mV or 20mV steps, average output current limit in 50mA steps, as well as output voltage slew rate, switching frequency, soft-start slew rate, mode of operation, current loop compensation, output active discharge strength, and cable drop compensation gain.

The LM72630-Q1 also contains an array of safety features including undervoltage and overvoltage protection with programmable thresholds, overcurrent protection with programmable hiccup mode, and thermal shutdown.

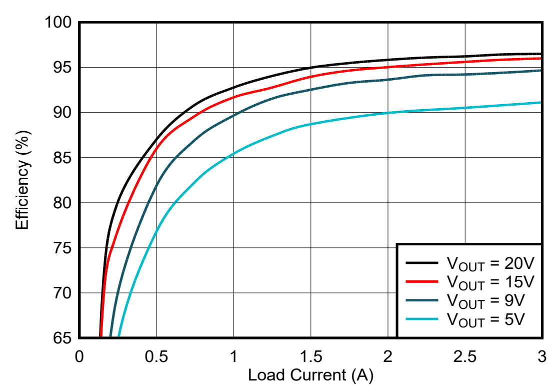
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LM72630-Q1	RRX (VQFN, 29)	6mm × 6mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit



Typical Efficiency, V_{IN} = 48V, f_{SW} = 400kHz

Additional features of the LM72630-Q1 include programmable diode emulation for lower current consumption at light-load conditions, open-drain nINT flag for fault reporting and output monitoring, precision enable input, monotonic start-up into prebiased load, integrated dual input (VIN and VOUTF) VCC supply regulator, and oversized VDDA regulator for powering external loads, such as companion USB PD controllers.

The LM72630-Q1 converter comes in a 6mm × 6mm thermally-optimized, 29-pin VQFN package. The three die-attach pads (VIN, SW, and PGND) improve thermal performance and board level reliability (BLR).

The LM72630-Q1 converter belongs to a family of synchronous buck converters with constant-current constant-voltage (CC-CV) regulation and I^{2}C interface listed in *Related Products*.

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4 Related Products

DEVICE OPTION	V_{IN} (Max)	V_{OUT} (Max)	I_{OUT} (Max)	$I_{LIM(avg)}$ (Max)
LM72630-Q1	70V	24V	3A (R_S = 8mΩ)	4.5A
LM72650-Q1	70V	24V	5A (R_S = 8mΩ)	7.5A
LM72680-Q1	70V	48V	5A (R_S = 8mΩ)	7.5A
			8A (R_S = 5mΩ)	12A
LM72880-Q1	80V	48V	5A (R_S = 8mΩ)	7.5A
			8A (R_S = 5mΩ)	12A

5 Pin Configuration and Functions

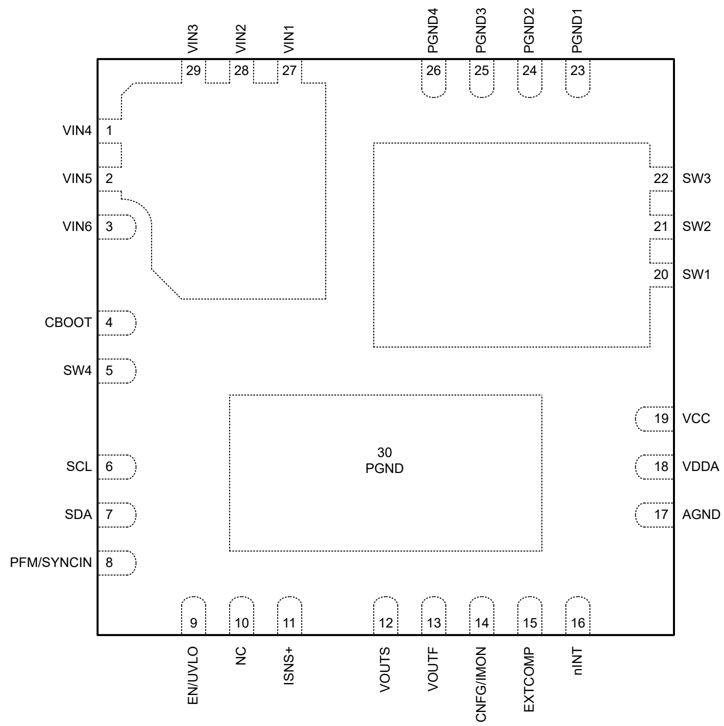


Figure 5-1. RRX 29-Pin VQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VIN4	P	Converter input pins to the drain of the high-side power MOSFET and the VCC regulator (VIN6). Connect to the input supply and the input filter capacitors. The path from the VIN pin to the input capacitors must be as short as possible.
2	VIN5	P	
3	VIN6	P	
4	CBOOT	P	High-side driver supply for the bootstrap gate drive. Connect a 47nF bootstrap capacitor between the CBOOT and SW4 pins.
5	SW4	P	Switch pin. Connect a 47nF bootstrap capacitor between the CBOOT and SW4 pins. This pin is internally connected to the switch pins SW1, SW2, and SW3. There is no need to route this pin to the other switch pins on a PCB.
6	SCL	I	I^2C clock pin.
7	SDA	I/O	I^2C data pin.
8	PFM / SYNCIN	I	PFM / FPWM mode selection and synchronization input pin. Connect the PFM / SYNCIN pin to VDDA to enable diode emulation mode. Connect the PFM / SYNCIN pin to AGND to operate in forced PWM (FPWM) mode with continuous conduction at light loads. The PFM / SYNCIN pin can also be used as a synchronization input to synchronize the internal oscillator to an external clock.
9	EN / UVLO	I	Enable / undervoltage lockout pin. Drive this pin high / low to enable / disable the device. If the enable function is not needed, tie this pin to VIN. Connect an external resistor divider network to set UVLO threshold.
10	NC	N/A	No connect pin. Leave floating or tie to GND.
11	ISNS+	A	Current sense amplifier input. Connect the ISNS+ pin to the inductor side of the external current sense resistor using a low-current Kelvin connection.
12	VOUTS	A	Output voltage sense and the current sense amplifier input. Connect the VOUTS pin to the output side of the respective current sense resistor using a low-current Kelvin connection.
13	VOUTF	P	Output voltage discharge pin and the VCC bias regulator input. Connect the VOUTF pin to the output side of the respective output capacitor.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
14	CNFG/ IMON	A	Configuration and output current monitoring pin. Connect a resistor to ground to set the I^2C address and enable or disable the IMON feature. Limit total capacitance on the pin to <200pF.
15	EXTCOMP	A	External compensation pin. This pin is the output of the transconductance amplifier. Connect a compensation network from the EXTCOMP pin to AGND.
16	nINT	O	Interrupt pin. This pin is an open-drain output that toggles low in case of a status register change.
17	AGND	G	Analog ground pin. Ground return for the internal voltage reference and analog circuits.
18	VDDA	P	Internal analog bias regulator output pin. Connect a 22µF ceramic decoupling capacitor from VDDA to AGND as close as possible to the pins.
19	VCC	P	VCC bias supply pin. Connect a 4.7µF ceramic capacitor between VCC and PGND as close as possible to the pins.
20	SW1	P	Switch pins. These pins form a switching node that is internally connected to the source terminal of the buck switch (high-side MOSFET) and the drain terminal of the synchronous rectifier (low-side MOSFET). Connect to the buck inductor.
21	SW2	P	
22	SW3	P	
23	PGND1	G	Power ground pins. These pins form a power ground node for the low-side MOSFET. Connect to the system ground on a PCB. Path to CIN must be as short as possible.
24	PGND2	G	
25	PGND3	G	
26	PGND4	G	
27	VIN1	P	Converter input pins to the drain of the high-side power MOSFET. Connect to the input supply and the input filter capacitors. The path from the VIN pin to the input capacitors must be as short as possible.
28	VIN2	P	
29	VIN3	P	
30	PGND	G	Controller power ground pin. Connect to the system ground using multiple vias.

(1) P = Power, G = Ground, I = Input, O = Output, A = Analog.

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN to PGND	–0.3	75	V
Pin voltage	SW to PGND	–0.3	75	V
Pin voltage	SW to PGND transient < 20ns	–5	80	V
Pin voltage	CBOOT to SW	–0.3	10	V
Pin voltage	CBOOT to SW, transient < 20ns	–2		V
Pin voltage	EN/UVLO to PGND	–0.3	75	V
Pin voltage	VDDA, SDA, SCL, nINT, CNFG, PFM/SYNCIN, EXTCOMP to AGND	–0.3	6.5	V
Pin voltage	VCC to AGND	–0.3	10	V
Pin voltage	VOUTF, VOUTS, ISNS+ to PGND	–0.3	30	V
Pin voltage	VOUTS to ISNS+	–0.3	0.3	V
Pin voltage	PGND to AGND	–0.3	0.3	V
T_{stg}	Storage temperature	–55	150	°C
T_J	Operating junction temperature	–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, 16, 17, 22, 23 and 29)	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		4.5		70	V
V_{OUT}	Output voltage range (10mV step), FPWM mode		1		24	V
V_{OUT}	Output voltage range (10mV step), PFM mode		1		22.5	V
V_{OUT}	Output voltage range (20mV step), FPWM mode		3.3		24	V
V_{OUT}	Output voltage range (20mV step), PFM mode		3.3		24	V
	Pin voltage	VIN, EN/UVLO, SW to PGND	0		70	V
	Pin voltage	SDA, SCL, PFM/SYNCIN, nINT to AGND	0		5.25	V
	Pin voltage	VOUTF, VOUTS, ISNS+ to PGND	0		24	V
	PGND to AGND		0		0.3	V
I_{OUT}	Output current range, LM72630-Q1		0		3	A
R_S	Sense resistor		7.92	8	8.08	mΩ
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM726x0-Q1 JESD 51-7 RRX (VQFN) 29 PINS	LM726x0-Q1 EVM RRX (VQFN) 29 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.5 (2)	18.6 (3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.6	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.7	–	°C/W
Ψ_{JT}	Junction-to-top characterization parameter ($T_{case-center}$)	11.5	7.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter ($T_{case-max}$)	–	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.6	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. These values do not represent the performance obtained in an actual application.
(3) Refer to the EVM User's Guide for board layout and additional information.

6.5 Electrical Characteristics

T_J = –40°C to +150°C. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VIN)						
I_{Q-SD}	V_{IN} shutdown current	Non-switching, V_{EN} = 0V, V_{FB} = V_{REF} + 50mV, V_{IN} = 48V, T_J = 25°C		4.7	6	µA
		Non-switching, V_{EN} = 0V, V_{FB} = V_{REF} + 50mV, V_{IN} = 48V, T_J = 125°C		8	10	µA
I_{Q-SBY}	V_{IN} standby current (1)	Non-switching, 0.5V ≤ V_{EN} ≤ 1V		310		µA
$I_{Q-READY}$	V_{IN} ready current (1)	Non-switching, V_{EN} ≥ 1V		1		mA
$I_{Q-SLEEP2-48V}$	V_{IN} sleep current, 5V output, no load	V_{EN} = 5V, V_{IN} = 48V, V_{OUTF} = V_{VOUTS} = 5V, no-load, non-switching, $V_{PFM/SYNCIN}$ = 5V		43	100	µA
ENABLE (EN / UVLO)						
V_{SBY-TH}	Shutdown-to-standby threshold voltage	$V_{EN/UVLO}$ rising		0.55		V
V_{EN-TH}	Enable voltage rising threshold	$V_{EN/UVLO}$ rising	0.95	1.0	1.05	V
V_{EN-HYS}	Enable voltage hysteresis			0.1		V
INTERNAL LDO (VCC)						
V_{VCC2}	VCC regulation voltage	I_{VCC} = 50mA	7.5	8	8.5	V
$V_{VCC(DO1)}$	VIN to VCC dropout voltage	V_{IN} = 5V, I_{VCC} = 50mA		130		mV
$V_{VCC(DO2)}$	BIAS to VCC dropout voltage	V_{VOUTF} = 5V, I_{VCC} = 50mA		110		mV
$I_{VCC(LIM)}$	VCC current limit	V_{CC} = 4V	80	220	367	mA
INTERNAL LDO (VDDA)						
V_{VDDA}	VDDA regulation voltage	I_{VDD} = 5mA	4.75	5	5.25	V
$V_{VDDA(DO)}$	VCC to VDDA dropout voltage	V_{IN} = 5V, I_{VDD} = 30mA		125		mV
$I_{VDDA-CL}$	VDDA current limit	V_{DDA} = 4.5V	36	50	67	mA
EXTERNAL BIAS (VOUTF)						
$V_{BIAS-TH}$	V_{IN} to V_{VOUTF} switchover rising threshold		4.85	4.92	4.98	V
$V_{BIAS-HYS}$	V_{IN} to V_{VOUTF} switchover hysteresis			140		mV
ACTIVE DISCHARGE (VOUTF)						
$I_{DISCHARGE}$	Output discharge current	0xD2[2:1] = 01b		24		mA
		0xD2[2:1] = 10b		48		mA
		0xD2[2:1] = 11b		72		mA
OUTPUT VOLTAGE (VOUTS)						
$V_{OUT(MIN)}$	Minimum output voltage setpoint - 10mV step	0xD1[7] = 0b, 0x21 = 0x64h, T_J = –40°C to +85°C	0.96	1	1.04	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT(MIN)}$	Minimum output voltage setpoint - 20mV step	0xD1[7] = 1b, 0x21 = 0xA5h, T_J = –40°C to +85°C	3.24	3.3	3.36	V
$V_{OUT(DEFAULT)}$	Default output voltage setpoint	0xD1[7] = 1b, 0x21 = 0xFAh, T_J = –40°C to +85°C	4.95	5.0	5.05	V
$V_{OUT(MAX)}$	Maximum output voltage setpoint	0xD1[7] = 1b, 0x21 = 0x4B0h, T_J = –40°C to +85°C	23.76	24	24.24	V
V_{OUT_STEP}	Output voltage step size - 10mV	0xD1[7] = 0b		10		mV
	Output voltage step size - 20mV	0xD1[7] = 1b		20		mV
ERROR AMPLIFIER (EXTCOMP)						
$g_{m\text{-}EXTERNAL}$	EA transconductance external compensation			1000		µS
PULSE FREQUENCY MODULATION (PFM/SYNCIN)						
$V_{IL\text{-}SYNCIN}$	PFM/SYNCIN input threshold low		0.8			V
$V_{IH(SYNCIN)}$	PFM/SYNCIN input threshold high				1.17	V
Δf_{SYNC}	Synchronization frequency range		–20		20	%
$t_{SYNC\text{-}TON\text{-}MIN}$	Minimum positive pulse width of external synchronization signal				25	ns
$t_{SYNC\text{-}TOFF\text{-}MIN}$	Minimum negative pulse width of external synchronization signal				250	ns
SWITCHING FREQUENCY (SW)						
f_{SW1}	Switching frequency 1	0xD1[4:3] = 00b	180	200	225	kHz
f_{SW2}	Switching frequency 2	0xD1[4:3] = 01b	360	400	440	kHz
f_{SW3}	Switching frequency 3	0xD1[4:3] = 10b	540	600	660	kHz
f_{SW4}	Switching frequency 4	0xD1[4:3] = 11b	1.98	2.2	2.42	MHz
$t_{ON\text{-}MIN}$	Minimum on-time[(1)]			25		ns
$t_{OFF\text{-}MIN}$	Minimum off-time			70	125	ns
DUAL RANDOM SPREAD SPECTRUM (DRSS)						
Δf_{SS}	Modulation range			10		%
f_m	Modulation frequency	0xD1[5] = 0b		10		kHz
POWER GOOD						
$V_{PG\text{-}UV}$	Power-Good UV trip level	Falling with respect to the set V_{OUT} (5V), 0xD9[3] = 0b, T_J = –40°C to +85°C	92.5	95	97	%
		Falling with respect to the set V_{OUT} (20V), 0xD9[3] = 1b	88	90	92	%
$V_{PG\text{-}OV}$	Power-Good OV trip level	Rising with respect to the set V_{OUT} (5V), 0xD9[3] = 0b, T_J = –40°C to +85°C	102.5	105	107	%
		Rising with respect to the set V_{OUT} (20V), 0xD9[3] = 1b	108	110	112	%
$V_{PG\text{-}UV\text{-}HYST}$	Power-Good UV hysteresis	Falling with respect to the regulated output		1.1		%
$V_{PG\text{-}OV\text{-}HYST}$	Power-Good OV hysteresis	Rising with respect to the regulated output		1.1		%
$t_{PG\text{-}DEGLITCH}$	Power-Good deglitch filter time	V_{OUT} falling or rising		30		µs
OVERVOLTAGE PROTECTION (nINT)						
V_{OV2}	Overvoltage protection	Rising with respect to the set V_{OUT}, 0xD5 = 60h		105		%
V_{OV2}	Overvoltage protection	Rising with respect to the set V_{OUT}, 0xD5 = 7Fh		136		%
V_{OV2_HYST}	Overvoltage protection hysteresis	Rising with respect to the set V_{OUT}		2		%
V_{OL_nINT}	nINT voltage low	Open collector, I_{nFAULT} = 2mA			0.4	V
STARTUP (SOFT START)						
SR_{SS}	Internal soft-start slew rate	0xD2[0] = 0b, SEL_FB_DIV20 = 1b		5		V/ms
		0xD2[0] = 1b, SEL_FB_DIV20 = 1b		2.5		V/ms
POWER SWITCHES						

6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, V_{IN} = 48V, $V_{BOOT-SW}$ = 8V, I_{SW}= 500mA		22		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, V_{VCC} = 8V, I_{SW}= 500mA		18		mΩ
INTERNAL HICCUP MODE						
$t_{HIC-DLY}$	HICCUP mode activation delay	V_{ISNS+} − V_{VOUT} > 60mV		512		CYCLES
$t_{HIC-DURATION}$	HICCUP mode fault duration	V_{ISNS+} − V_{VOUT} > 60mV		16384		CYCLES
OVERCURRENT PROTECTION (OCP)						
V_{CS-TH}	CS voltage threshold	Measured from ISNS+ to VOUTS	34	40	46	mV
$t_{DELAY-CS}$	CS delay to output			85		ns
A_{CS}	CS amplifier gain (1)			10		V/V
$I_{BIAS-CS}$	CS amplifier input bias current (1)			0.3		µA
$V_{CS-TH-NEG}$	CS negative voltage threshold	Measured from VOUTS to ISNS+		20		mV
AVERAGE OUTPUT CURRENT LIMIT						
$I_{LIM(MIN)}$	Minimum average current limit setpoint	R_{SENSE} = 8mΩ, 0xD0 = 0Ah, T_J = –40°C to +85°C	380	500	620	mA
$I_{LIM(TYP)}$	Typical average current limit setpoint	R_{SENSE} = 8mΩ, 0xD0 = 3Ch, T_J = –40°C to +85°C	2.88	3	3.12	A
$I_{LIM(MAX)}$	Maximum average current limit setpoint	R_{SENSE} = 8mΩ, 0xD0 = 5Ah		4.5		A
I_{LIM_STEP}	Average current limit step size	R_{SENSE} = 8mΩ		50		mA
OUTPUT CURRENT MONITOR (IMON)						
A_{IMON}	I_{OUT} monitor amplifier gain from V_{CS} to V_{OUT}	V_{CS} = 40mV, T_J = –40°C to +85°C	24.5	25	25.5	V/V
V_{OFFSET}	I_{OUT} monitor amplifier offset voltage	V_{CS} = 0mV, T_J = –40°C to +85°C	0.98	1	1.02	V
CABLE DROP COMPENSATION (CDC)						
A_{CDC}	Maximum cable drop compensation gain	0xD8[5:0] = 3Fh		62		V/V
A_{CDC_STEP}	Cable drop compensation gain step size			2		V/V
SERIAL CONTROL BUS (SCL, SDA)						
V_{IH}	Input high level		2			V
V_{IL}	Input low level				0.8	V
V_{HYST}	Input hysteresis			320		mV
V_{OL}	Output low level	I_{OL} = 3mA, standard-mode/fast-mode	0		0.4	V
V_{OL}	Output low level	I_{OL} = 20mA, fast-mode plus	0		0.4	V
I_{IH}	Input high current	Pin connected to V_{I2C}	-10		10	µA
I_{IL}	Input low current	Pin connected to GND	-10		10	µA
C_{IN}	Input capacitance			5		pF
THERMAL SHUTDOWN (TSD)						
T_{J-SD}	Thermal shutdown threshold (1)	Temperature rising		175		°C
T_{J-HYS}	Thermal shutdown hysteresis (1)			15		°C

(1) Specified by design. Not production tested.

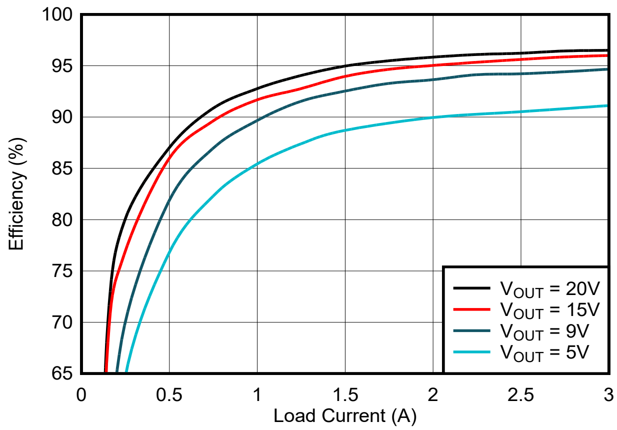
6.6 Timing Requirements for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard-mode	> 0		100	kHz
		Fast-mode	> 0		400	kHz
		Fast-mode Plus	> 0		1	MHz
t_{LOW}	SCL low period	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_{HIGH}	SCL high period	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard-mode	4.7			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard-mode	0			µs
		Fast-mode	0			µs
		Fast-mode Plus	0			µs
$t_{SU;DAT}$	Data setup time	Standard-mode	250			ns
		Fast-mode	100			ns
		Fast-mode Plus	50			ns
$t_{SU;STO}$	Setup time for STOP condition	Standard-mode	4.0			µs
		Fast-mode	0.6			µs
		Fast-mode Plus	0.26			µs
t_{BUF}	Bus free time between STOP and START	Standard-mode	4.7			µs
		Fast-mode	1.3			µs
		Fast-mode Plus	0.5			µs
t_r	SCL and SDA rise time	Standard-mode			1000	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
t_f	SCL and SDA fall time	Standard-mode			300	ns
		Fast-mode			300	ns
		Fast-mode Plus			120	ns
C_b	Capacitive load for each bus line	Standard-mode			400	pF
		Fast-mode			400	pF
		Fast-mode Plus			550	pF
$t_{VD:DAT}$	Data valid time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
$t_{VD;ACK}$	Data valid acknowledge time	Standard-mode			3.45	µs
		Fast-mode			0.9	µs
		Fast-mode Plus			0.45	µs
t_{SP}	Input filter	Fast-mode			50	ns
		Fast-mode Plus			50	ns

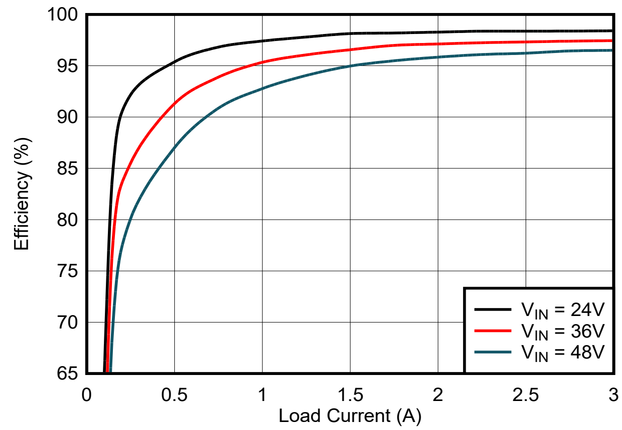
6.7 Typical Characteristics

T_J = 25°C, unless otherwise stated.



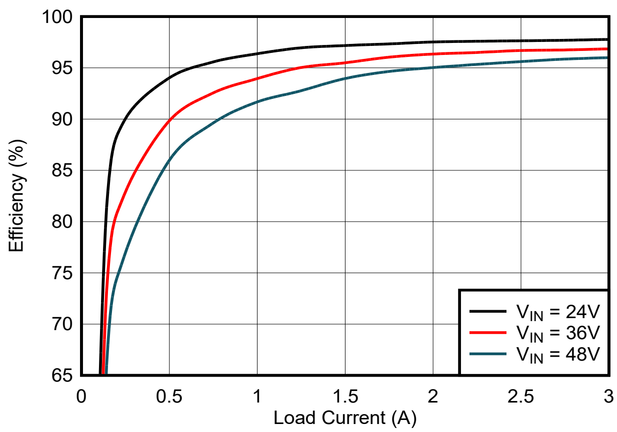
V_{IN} = 48V FPWM mode
f_{SW} = 400kHz L_O = 22μH XGL1010

Figure 6-1. Efficiency, V_{IN} = 48V



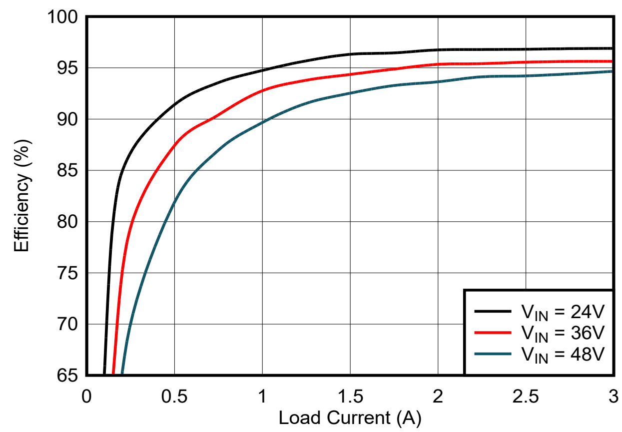
V_{OUT} = 20V FPWM mode
f_{SW} = 400kHz L_O = 22μH XGL1010

Figure 6-2. Efficiency, V_{OUT} = 20V



V_{OUT} = 15V FPWM mode
f_{SW} = 400kHz L_O = 22μH XGL1010

Figure 6-3. Efficiency, V_{OUT} = 15V



V_{OUT} = 9V FPWM mode
f_{SW} = 400kHz L_O = 22μH XGL1010

Figure 6-4. Efficiency, V_{OUT} = 9V

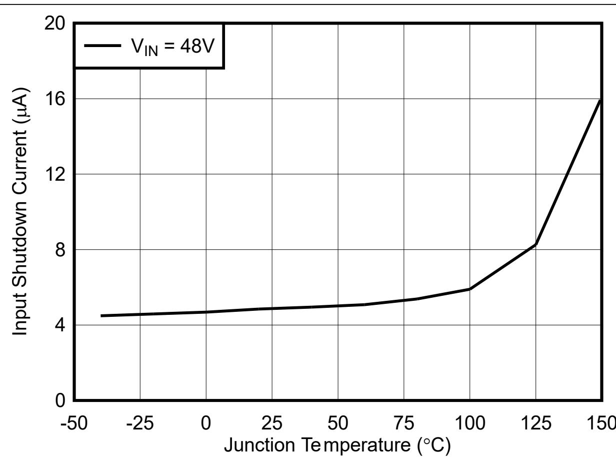


Figure 6-5. Input Shutdown Current vs Temperature

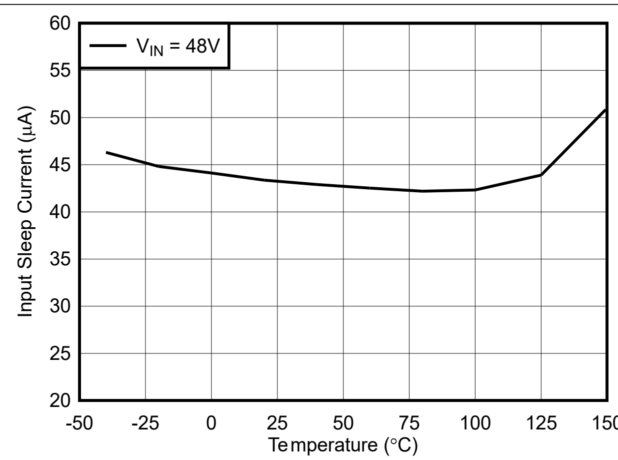


Figure 6-6. Input Sleep Current vs Temperature, V_{OUT} = 5V

6.7 Typical Characteristics (continued)

T_J = 25°C, unless otherwise stated.

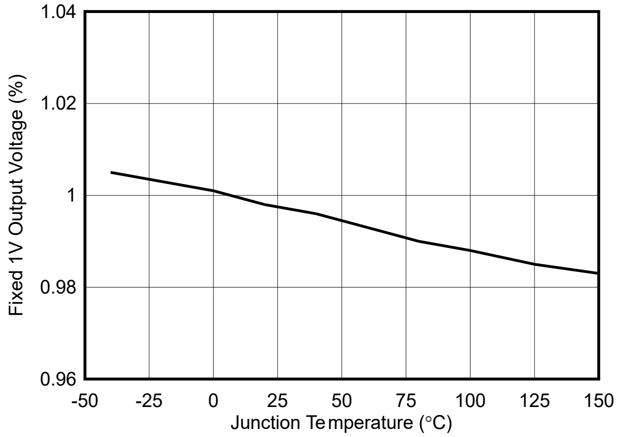


Figure 6-7. Fixed Output Voltage vs Temperature, V_{OUT} = 1V

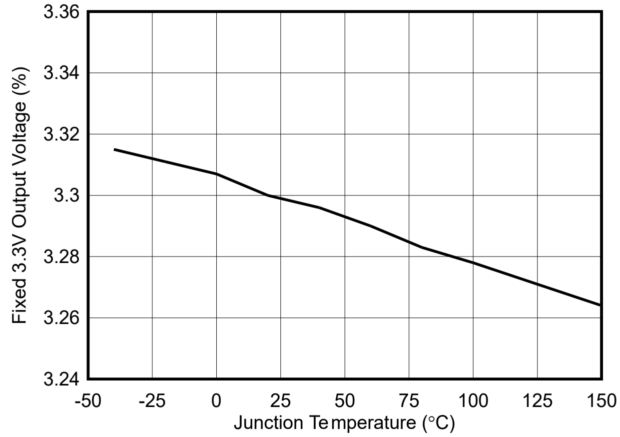


Figure 6-8. Fixed Output Voltage vs Temperature, V_{OUT} = 3.3V

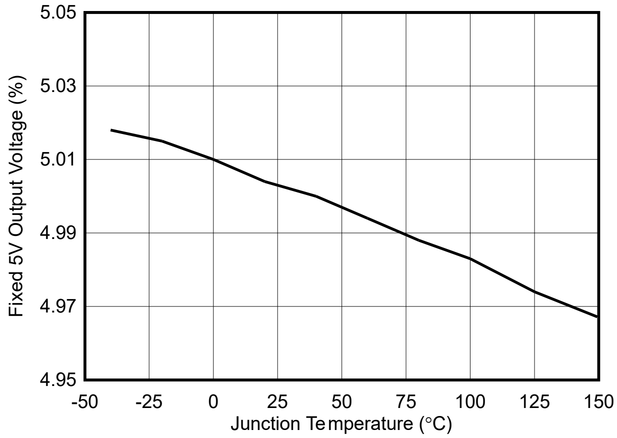


Figure 6-9. Fixed Output Voltage vs Temperature, V_{OUT} = 5V

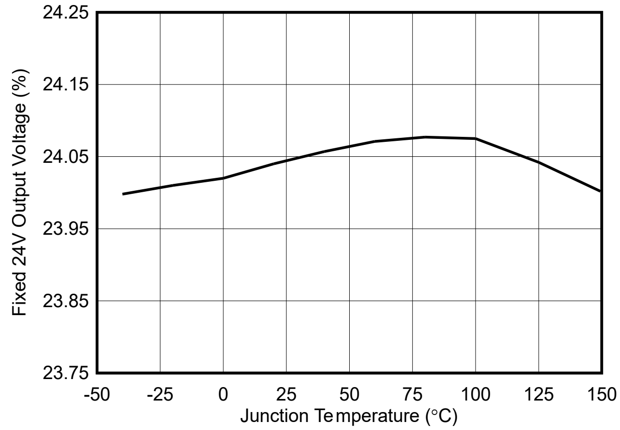


Figure 6-10. Fixed Output Voltage vs Temperature, V_{OUT} = 24V

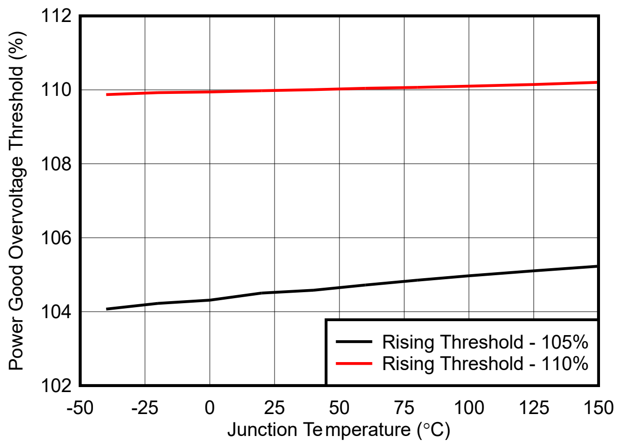


Figure 6-11. PG Overvoltage Threshold vs Temperature

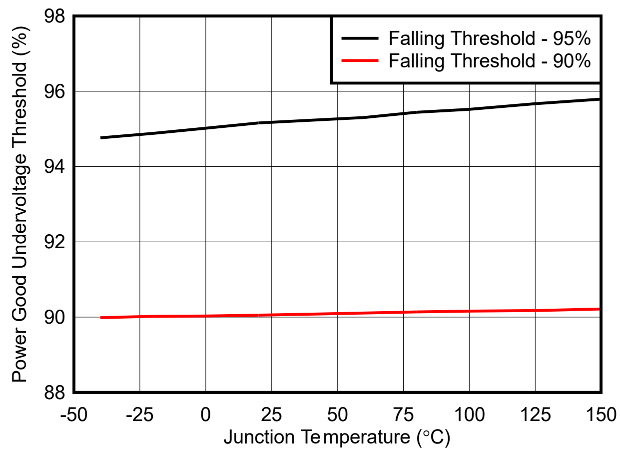


Figure 6-12. PG Undervoltage Threshold vs Temperature

6.7 Typical Characteristics (continued)

T_J = 25°C, unless otherwise stated.

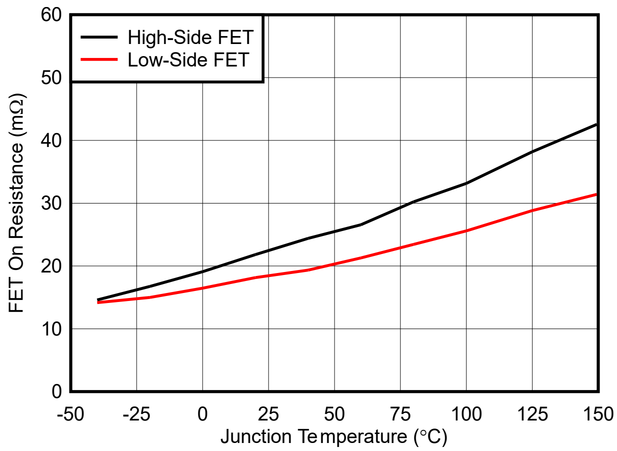


Figure 6-13. FET On Resistance vs Temperature

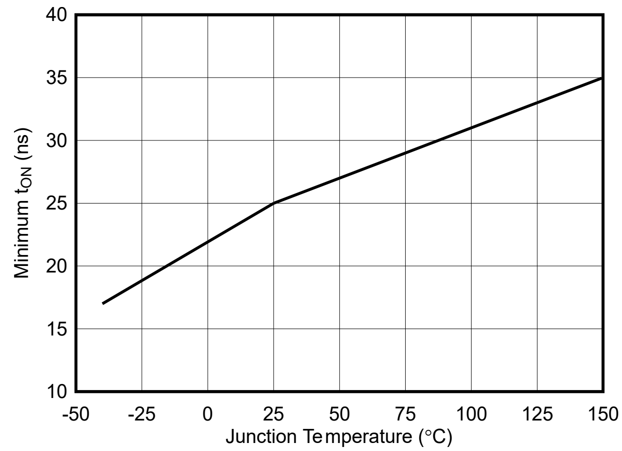


Figure 6-14. Minimum On-Time vs Temperature

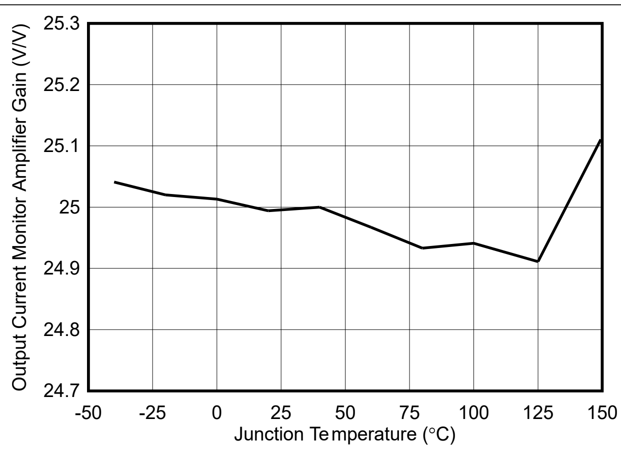


Figure 6-15. IMON Amplifier Gain vs Temperature

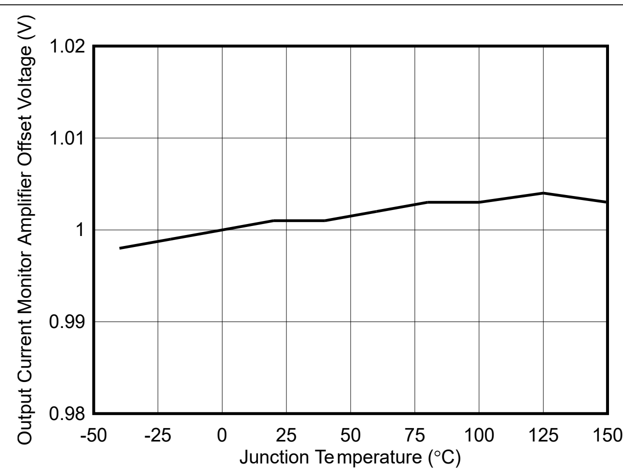


Figure 6-16. IMON Amplifier Voltage Offset vs Temperature

7 Detailed Description

7.1 Overview

The LM72630-Q1 is a 70V, ultra-low I_Q, synchronous buck converter with constant-current constant-voltage (CC-CV) regulation and I^2C interface. The device is designed to work with any micro-controller featuring compatible I^2C interface, including the TPS2674X-Q1 family of USB type-C PD controllers.

The converter uses a peak current-mode control architecture for easy loop compensation, fast transient response, and excellent load and line regulation. The highly accurate CC-CV operation enables seamless transition between constant-current and constant-voltage modes. The device features integrated dual input (VIN and VOUTF) VCC supply regulator, and oversized VDDA regulator for powering external loads such as companion USB PD controllers. The I^2C interface allows programming of output voltage in 10mV or 20mV steps, average output current limit in 50mA steps, as well as output voltage slew rate, switching frequency, soft-start slew rate, mode of operation, current loop compensation, output active discharge strength, and cable drop compensation gain.

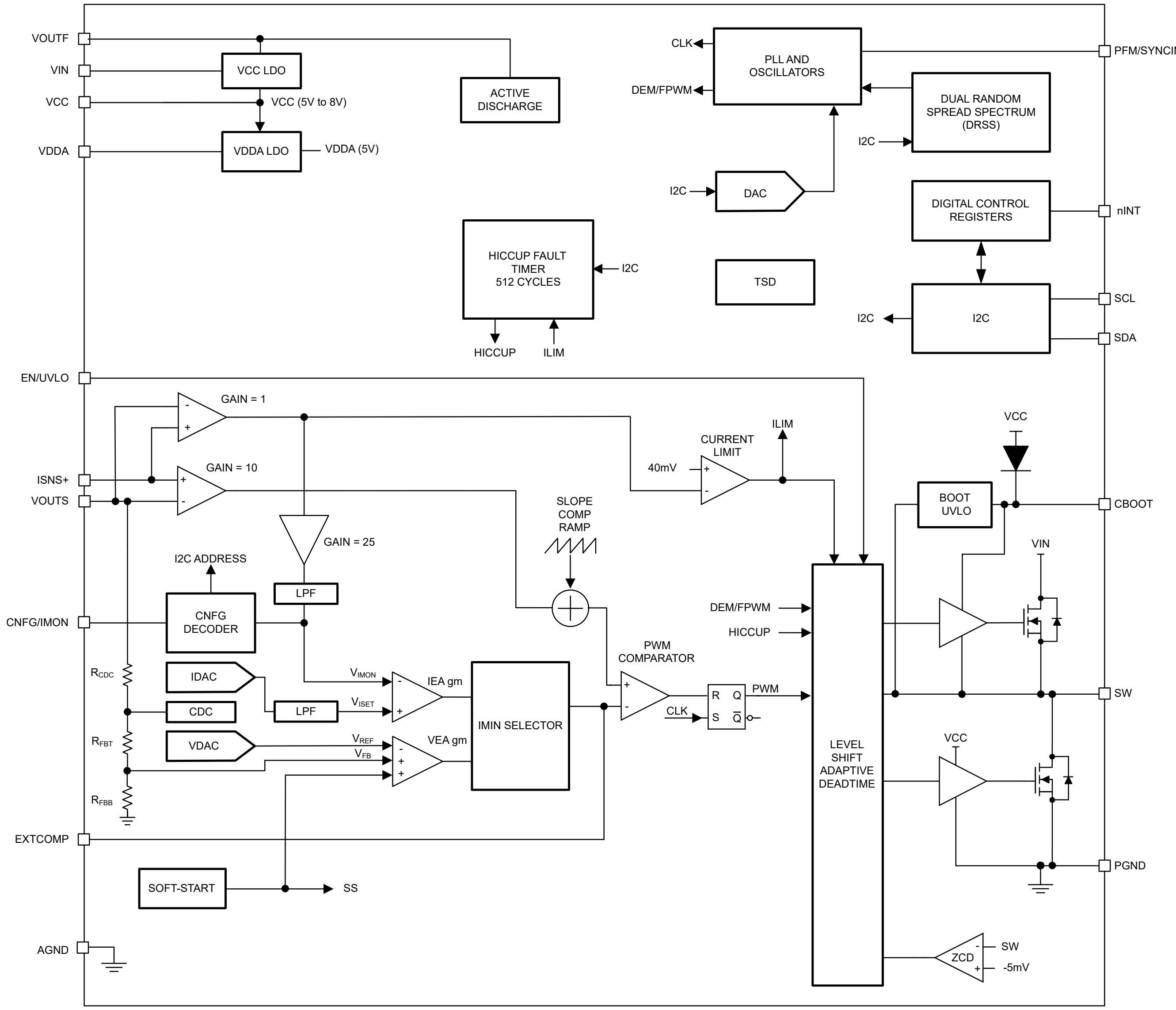
Connect the output to the VOUTF pin to maximize efficiency in high input voltage applications. A programmable diode emulation feature enables discontinuous conduction mode (DCM) operation to further improve efficiency and reduce power dissipation during light-load conditions.

The LM72630-Q1 also features an array of safety features including output undervoltage and overvoltage protection with programmable thresholds, overcurrent protection with programmable hiccup mode, thermal shutdown, precision enable, and open-drain nINT flag for fault and status reporting.

The LM72630-Q1 incorporates features to simplify the compliance with various EMI standards including CISPR 25 Class 5 that defines automotive EMI requirements. Dual Random Spread Spectrum (DRSS) technique reduces the peak harmonic EMI signature.

LM72630-Q1 is provided in a 29-pin VQFN package with the exposed VIN, SW, and PGND pads to maximize thermal dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range (V_{IN})

The LM72630-Q1 operational input voltage range is from 4.5V to 70V. The device is intended for step-down conversions from 12V, 24V and 48V automotive supply rails. The LM72630-Q1 uses internal LDOs to provide a 5V to 8V VCC bias rail and a 5V VDDA rail for the gate drive and control circuits.

In high input voltage applications, make sure that the VIN and SW pins do not exceed the absolute maximum voltage rating of 75V during line or load transient events. Voltage excursions that exceed the absolute maximum ratings of these pins can damage the IC. Follow PCB board layout recommendations and use high-quality input bypass capacitors to minimize voltage overshoot and ringing.

As V_{IN} approaches V_{OUT}, the LM72630-Q1 skips t_{OFF} cycles to allow the controller to extend the duty cycle up to approximately 99%. Refer to Figure 7-1.

Use Equation 1 to calculate when the LM72630-Q1 enters dropout mode.

$$V_{IN} = V_{OUT} \times \left(\frac{t_P}{t_P - t_{OFF}}\right) \quad (1)$$

- t_P = oscillator period
- t_{OFF} = minimum off time

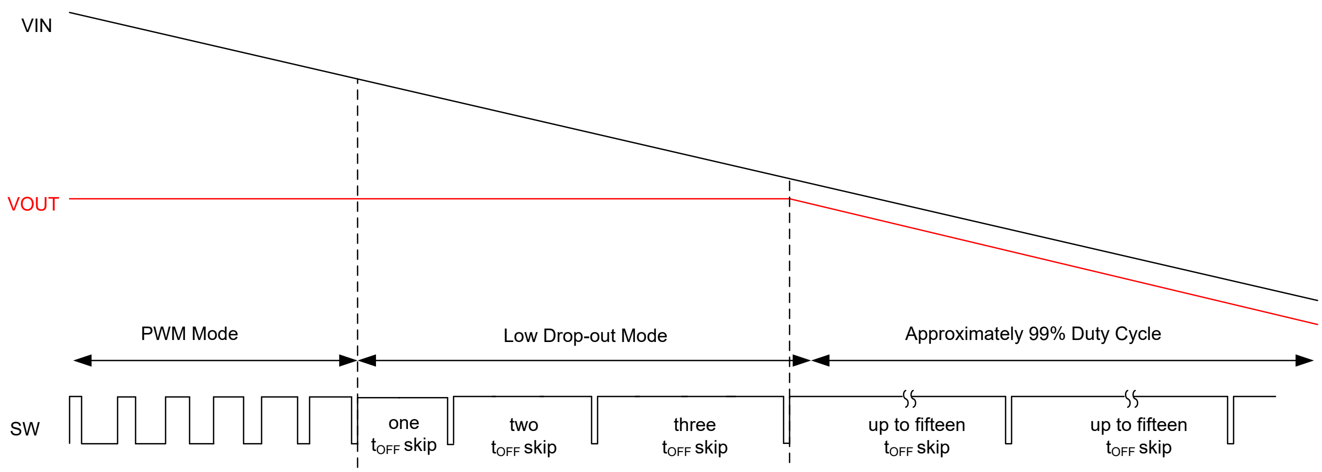


Figure 7-1. Dropout Mode Operation

7.3.2 High-Voltage Bias Supply Regulators (VCC, VDDA)

The LM72630-Q1 contains an internal high-voltage VCC bias regulator that provides the bias supply for the gate drivers for the power MOSFETs. The input voltage pin (VIN) can connect directly to an input voltage source up to 70V. However, when the input voltage is below the VCC setpoint level, the VCC voltage tracks VIN minus a small voltage drop.

When the output voltage is < 5V, the VCC bias regulator output voltage is 8V. When the output voltage is from 5V to 8V and the BIAS_EN bit is set, the VCC bias regulator output voltage tracks the output voltage. When the output voltage is ≥8V, the VCC bias regulator output is 8V. TI recommends connecting a 4.7µF capacitor from the VCC pin to PGND.

The LM72630-Q1 also contains a linear regulator, VDDA, that takes the VCC regulator output as an input and generates a 5V output. The VDDA powers internal control circuitry including the digital block. The VDDA has a 50mA (typical) current limit and can be used to power an external companion USB Type-C controller device such as the TPS2674X-Q1. Bypass VDDA with a 22µF ceramic capacitor to achieve a low-noise internal bias rail.

7.3.3 Enable (EN/UVLO)

Connect the enable pin to voltage as high as 70V. If the EN pin is pulled below 0.55V, the LM72630-Q1 is in shutdown mode with an I_Q of 4.7µA (typical) current draw from V_{IN}. When the enable voltage is between 0.55V < EN < 1V, the LM72630-Q1 is in standby mode. When in standby mode, the VCC regulator is enabled, default registers and trim bits loaded, the digital block is disabled, the device is not switching, and the I_Q current is 310µA (typical). When the enable voltage is above 1V, the LM72630-Q1 is in ready mode after the 100µs (typical) enable to ready delay. When in ready mode, the I^2C interface is available, the device is not switching, and the I_Q current is 1mA (typical). The LM72630-Q1 starts up and enters active mode, when the CONV_EN bit in the OPERATION register is set.

Users can also enable the LM72630-Q1 with standard CMOS logic drivers. A voltage greater than 2.0V enables the LM72630-Q1, and a voltage less than 0.4V disables the LM72630-Q1. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in Figure 7-2 to establish a precision UVLO threshold. TI recommends setting the input voltage turn-on threshold at 4.5V or higher when the rise time of the input supply to LM72630-Q1 is significantly slower than soft-start time. TI does not recommend leaving the EN pin floating.

Use Equation 2 to calculate the UVLO resistors given the required input turn-on voltage. The EN voltage hysteresis, $V_{EN\text{-}HYS}$, is 100mV or 10% of the EN voltage rising threshold, $V_{EN\text{-}TH}$, therefore the input turn-off voltage is 90% of the input turn-on voltage.

$$R_{UV1} = \left(\frac{V_{IN(on)}}{V_{EN-TH}} - 1\right) \times R_{UV2} \tag{2}$$

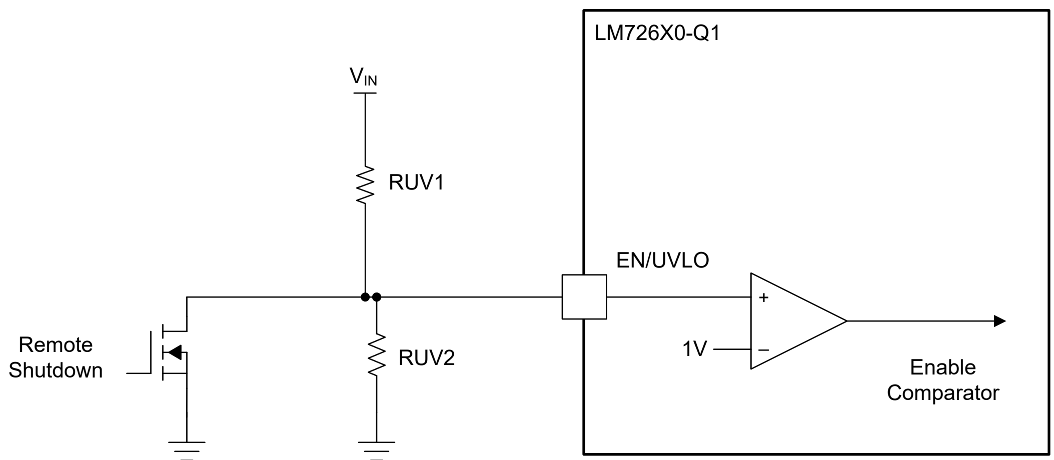


Figure 7-2. Programmable Input Voltage UVLO Turn-on and Turn-off

7.3.4 Switching Frequency

Program the LM72630-Q1 oscillator by setting the FREQ bits in the MFR_DEVICE_CFG_D1 device configuration register according to Table 7-1.

Table 7-1. Switching Frequency Selection

MFR_DEVICE_CFG_D1[4:3]	SWITCHING FREQUENCY SELECTION
0b00	200kHz
0b01	400kHz (default)
0b10	600kHz
0b11	2.2MHz

Note

As with any buck converter, the switching losses increase at higher switching frequency, especially at higher V_{IN}. Limit 2.2MHz operation to $V_{IN} \leq 36V$ and consider derating the maximum output current as detailed in Section 9.1.3 .

Under low V_{IN} conditions when the high-side MOSFETs on-time exceeds the programmed oscillator period, the LM72630-Q1 extends the switching period of that channel until the PWM latch is reset by the current sense ramp exceeding the controller compensation voltage. In such an event, the oscillators operate independently and asynchronously until the channel maintains output regulation at the programmed frequency.

The approximate input voltage level where this occurs is given by Equation 3, where t_{SW} is the switching period and $t_{OFF(min)}$ is the minimum off-time of 70ns.

$$V_{IN(min)} = V_{OUT} \times \left(\frac{t_{SW}}{t_{SW} - t_{OFF(min)}}\right) \quad (3)$$

7.3.5 Dual Random Spread Spectrum (DRSS)

The LM72630-Q1 provides a dual random spread spectrum (DRSS) function, which reduces the EMI of the power supply over a wide frequency range. The DRSS function combines a low-frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in the lower radio frequency bands, while the high frequency random modulation improves performance in the higher radio frequency bands.

Spread spectrum works by converting a narrowband signal into a wideband signal which spreads the energy over multiple frequencies. Industry standards require different spectrum analyzer resolution bandwidth (RBW) settings for different frequency bands. The RBW has an impact on the spread spectrum performance. For example, the CISPR-25 requires 9kHz RBW for the 150kHz to 30MHz frequency band. For frequencies greater than 30MHz, the required RBW is 120kHz. DRSS simultaneously improves the EMI performance in the high and low RBWs with the low-frequency triangular modulation and high-frequency cycle-by-cycle random modulation as shown in Figure 7-3. In the low-frequency band (150kHz – 30MHz), the DRSS function reduces the conducted emissions by as much as 15dBµV, and in the high-frequency band (30MHz – 108MHz) reduces the conducted emissions by as much as 5dBµV.

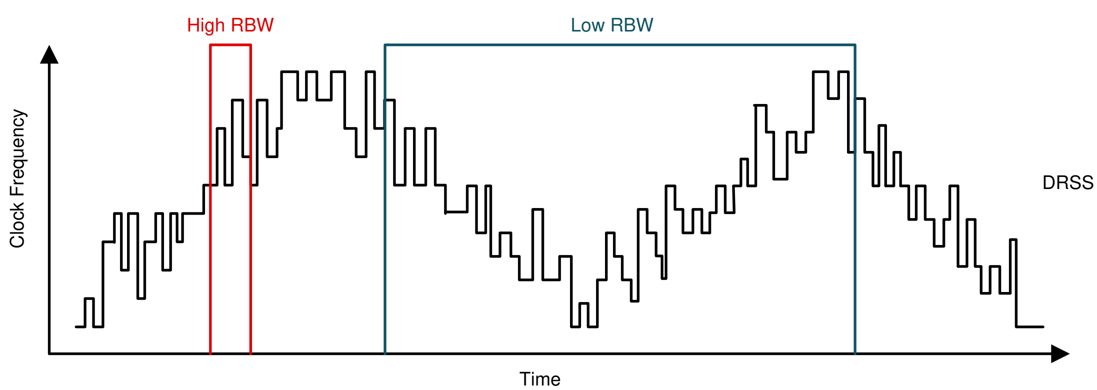


Figure 7-3. Dual Random Spread Spectrum Implementation

Enable the DRSS function by setting the DRSS_EN bit. Note that the external clock synchronization through the PFM/SYNCIN pin is not possible when the DRSS function is enabled.

The LM72630-Q1 also supports two modulation frequencies, select the frequencies according to Table 7-2.

Table 7-2. DRSS Modulation Frequency Selection

DRSS_FMOD	MODULATION FREQUENCY
0b0	10kHz
0b1	2.5kHz

7.3.6 Soft Start

The LM72630-Q1 has a programmable soft-start slew rate. The soft-start feature allows the regulator to gradually reach the steady-state operating point, thus reducing start-up stresses and surges.

Select the soft-start slew rate using the SOFT_START_TIME bit according to Table 7-3.

Table 7-3. Soft-Start Slew Rate Selection

SOFT_START_TIME	SOFT-START SLEW RATE	
	20mV VOUT STEP SIZE	10mV VOUT STEP SIZE
0b0	5V/ms	2.5V/ms
0b1	2.5V/ms	1.25V/ms

7.3.7 Output Voltage and Output Voltage Slew Rate

Program the LM72630-Q1 output voltage from 1V to 24V in 10mV steps or from 3.3V to 24V in 20mV steps by setting the VOUT_COMMAND register. Prior to programming the output voltage, select the output voltage step size and range according to Table 7-4.

Table 7-4. Output Voltage Step Size and Range Selection

SEL_FB_DIV20	OUTPUT VOLTAGE STEP SIZE	MODE OF OPERATION	OUTPUT VOLTAGE RANGE
0b0	10mV	PFM	1V – 22.5V
		FPWM	1V – 24V
0b1	20mV	PFM	3.3V – 24V
		FPWM	3.3V – 24V

Note

When in PFM mode, set the OUT_OF_AUDIO bit in MFR_DEVICE_CFG_D9 register to allow full output voltage range in PFM mode.

For controlled output voltage ramp up and ramp down times, adjust the output voltage slew rate by setting the VOUT_SLEW_RATE bits according to Table 7-5. Note that the effective output slew rate can be affected by the average, peak, and negative current limits when charging or discharging output capacitors. When in PFM mode, the output voltage slew rate is limited by the load current and the set active discharge current.

Table 7-5. Output Voltage Slew Rate Selection

VOUT_SLEW_RATE	VOUT SLEW RATE	
	(20mV VOUT STEP SIZE)	(10mV VOUT STEP SIZE)
0b00	40mV/µs	20mV/µs
0b01	20mV/µs	10mV/µs
0b10	1mV/µs	0.5mV/µs
0b11	0.5mV/µs	0.25mV/µs

7.3.8 Minimum Controllable On-Time

There are two limitations to the minimum output voltage adjustment range: the LM72630-Q1 voltage reference and the minimum controllable switch-node pulse width, $t_{ON(min)}$.

$t_{ON(min)}$ effectively limits the voltage step-down conversion ratio V_{OUT}/V_{IN} at a given switching frequency. For fixed-frequency PWM operation, the voltage conversion ratio must satisfy Equation 4.

$$\frac{V_{OUT}}{V_{IN}} > t_{ON(min)} \times F_{SW} \tag{4}$$

where

- $t_{ON(min)}$ is 25ns (typical).
- F_{SW} is the switching frequency.

If the desired voltage conversion ratio does not meet the above condition, the LM72630-Q1 transitions from a fixed switching frequency operation mode to a pulse-skipping mode to maintain output voltage regulation.

For wide V_{IN} applications and low output voltages, an alternative is to reduce the LM72630-Q1 switching frequency to meet the requirement of Equation 4.

7.3.9 Dual Loop Architecture

The LM72630-Q1 has two control loops, a voltage loop and a current loop, and an IMIN Selector block that compares output currents from the voltage loop error amplifier and the current loop error amplifier. The IMIN Selector block selects the lower current to take the control of the constant voltage (CV) or constant current (CC) regulation. The block enables seamless transition between CC and CV operation, and is shown in the following figure.

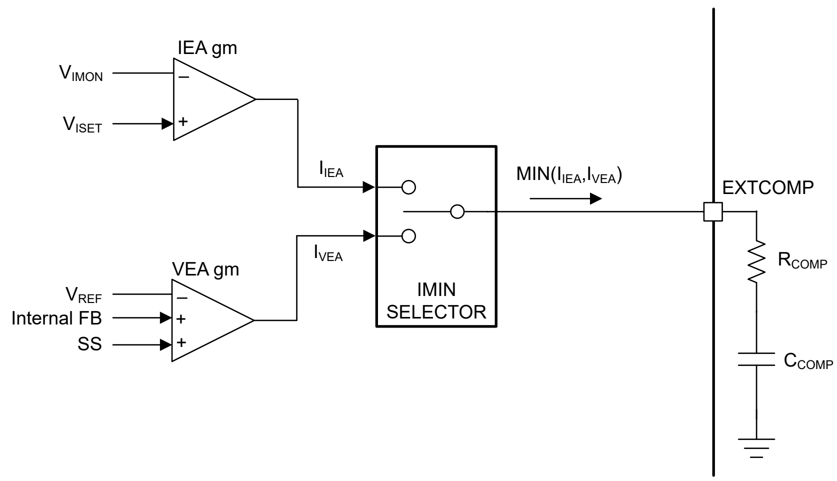


Figure 7-4. Dual Loop Architecture Block Diagram

7.3.9.1 Voltage Loop Error Amplifier

In the voltage control loop, the LM72630-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the internal feedback voltage and a programmable precision reference, V_{REF}. The transconductance of the amplifier is 1000µS. The voltage loop error amplifier takes the control when the internal minimum function block, IMIN SELECTOR, selects the current from the voltage loop error amplifier as shown in the following figure.

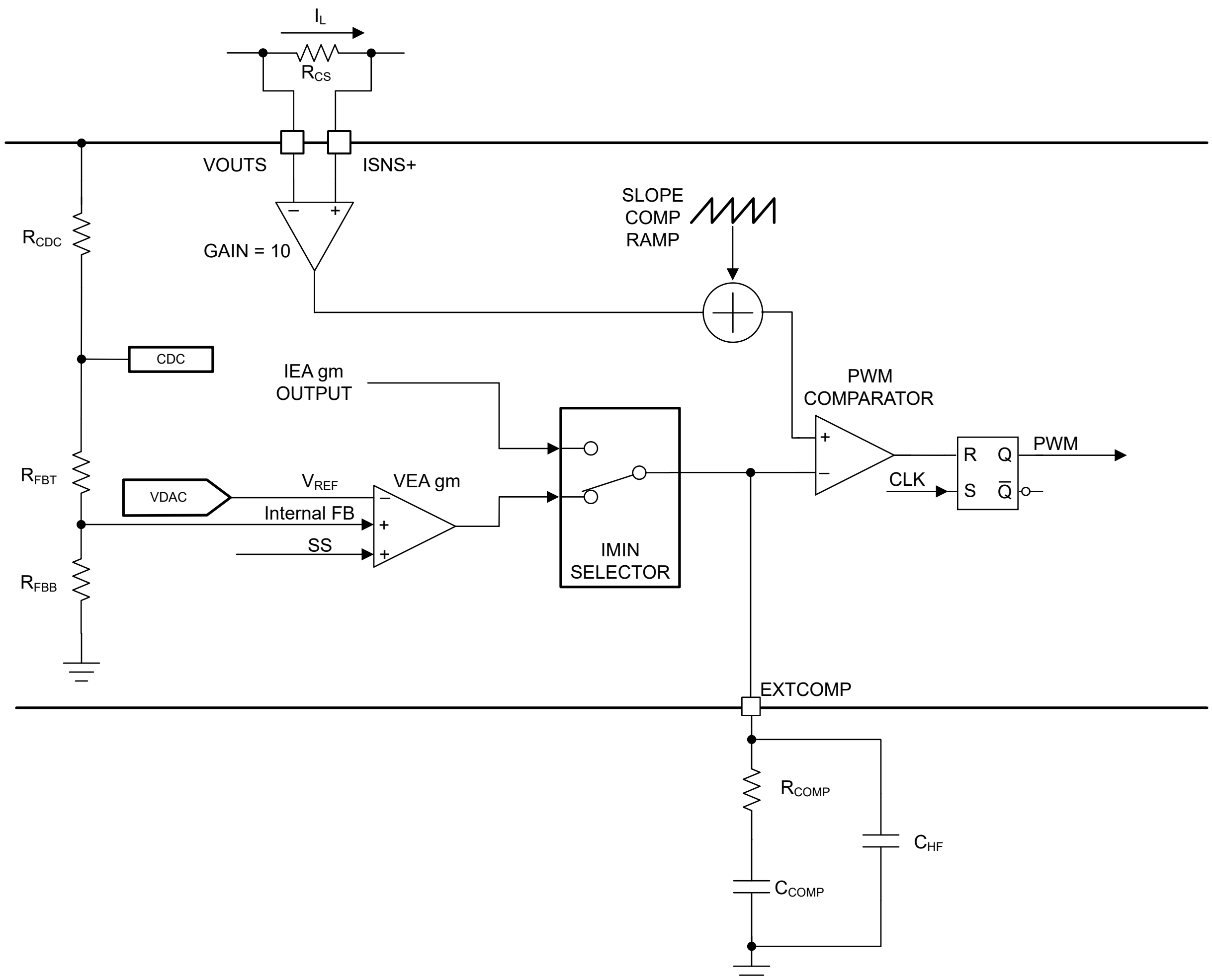


Figure 7-5. Voltage Loop Functional Block Diagram

The voltage control loop requires an external compensation network. TI generally recommends a type-II compensation network for peak current-mode control.

7.3.9.2 Current Loop Error Amplifier

In the current control loop, the LM72630-Q1 has a high-gain transconductance amplifier that generates an error current proportional to the difference between the IMON voltage, V_{IMON}, and the programmable ISET reference voltage, V_{ISET}. The transconductance of the amplifier is 1000µS. The current loop error amplifier takes the control when the internal minimum function block, IMIN SELECTOR, selects the current from the current loop error amplifier as shown in the following figure.

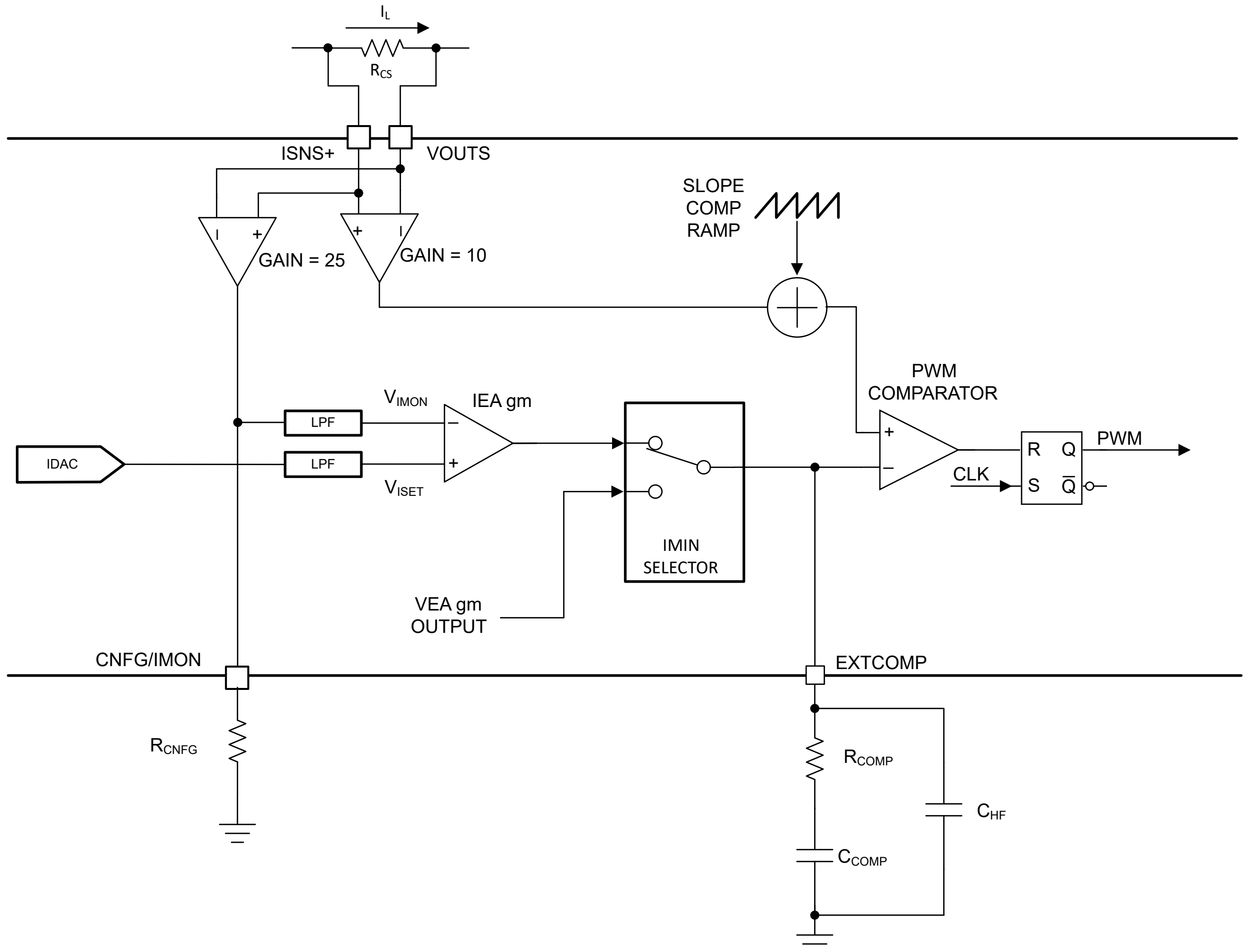


Figure 7-6. Current Loop Functional Block Diagram

The current control loop features a programmable compensation. Use CC_COMP bits in MFR_DEVICE_CFG_D1 register to set the compensation time constant. Select the compensation time constant value that is closest to the time constant value defined by the load (R_{OUT} and C_{OUT}).

7.3.10 Programmable OVP

The LM72630-Q1 has a programmable output overvoltage protection.

The output OVP is set by programming an internal 8-bit DAC. Use the OVP_THRESHOLD field described in Section 8.9 to set the OVP threshold between 105% and 136% in 1% steps.

By default, the LM72630-Q1 OVP detection is enabled and the OVP threshold set to 110% above the set output voltage. When the output voltage exceeds the OVP threshold, the device interrupts switching, discharges the VOUT node, and sets the VOUT_OV bits in STATUS_BYTE and STATUS_WORD registers.

7.3.11 Programmable ILIM

The LM72630-Q1 has a programmable average output current limit.

The average output current limit is set by programming an internal 8-bit DAC. Use the AVG_ILIM_THRESHOLD field described in Section 8.6 to set the average output current limit between 0.5A and 4.5A in 50mA steps with the recommended 8mΩ sense resistor.

The LM72630-Q1 also features an MFI function that, if enabled and the set current limit is 3A or less, increases the set current limit by a factor of 1.67x for the first 1ms of the constant current regulation. Use the MFI_EN bit in the register 0xD9 to enable the function.

7.3.12 IOUT Monitor

Use the IMON pin of LM72630-Q1 as the average inductor current or converter output current monitor when the converter is operating in the constant voltage control loop. Read the average inductor current from the voltage on the IMON pin using Equation 5.

$$I_{AVG} = \frac{V_{IMON} - V_{OFFSET}}{A_{IMON} \times R_S} \tag{5}$$

where

- V_{IMON} is the voltage on the IMON pin
- V_{OFFSET} is the output current monitor amplifier offset voltage of 1V (typical)
- A_{IMON} is the output current monitor amplifier gain of 25V/V (typical)
- R_S is the sense resistor of 8mΩ (typical)

7.3.13 Cable Drop Compensation

The LM72630-Q1 has a cable drop compensation (CDC) feature. The CDC feature increases the output voltage based on the output current and the programmable CDC gain to offset the voltage drop across a USB cable. The CDC gain is programmable from 0V/V to 62V/V in 2V/V steps. Set the CDC gain to a value closest to the ratio of the cable resistance and the sense resistor, R_S. For example, if the cable resistance is 150mΩ and the selected sense resistor is 8mΩ, the desired CDC gain is calculated as 150mΩ / 8mΩ = 18.75. The closest programmable CDC gain value is 18V/V.

Use the CDC_EN bit in the register 0xD8 to enable the cable drop compensation. Set the CDC gain using the CDC_GAIN field in the register 0xD8. For example, to set the CDC gain to 18V/V, set the CDC_GAIN field to 18V/V / 2V/V(LSB) = 9h.

7.3.14 Slope Compensation

The LM72630-Q1 provides internal slope compensation for stable operation with peak current-mode control and a duty cycle greater than 50%. Calculate the buck inductance to provide a slope compensation contribution equal to one times the inductor downslope using the following equation.

$$L_{O(sc)} = \frac{V_{OUT}[V] \times R_S[m\Omega]}{24 \times F_{SW}[MHz]} \tag{6}$$

- A lower inductance value increases the peak-to-peak inductor current, which typically minimizes size and cost, and improves transient response at the cost of reduced light-load efficiency due to higher cores losses and peak currents.
- A higher inductance value decreases the peak-to-peak inductor current, which typically increases the full-load efficiency by reducing switch peak and RMS currents at the cost of requiring larger output capacitors to meet load-transient specifications.

7.3.15 Shunt Current Sensing

Figure 7-7 shows inductor current sensing using a shunt resistor. This configuration continuously monitors the inductor current to provide accurate overcurrent protection across the operating temperature range. For excellent current sense accuracy and overcurrent protection, use a low inductance ±1% tolerance shunt resistor between the inductor and the output, with a Kelvin connection to the LM72630-Q1 current sense amplifier.

If the peak differential current signal sensed from ISNS+ to VOUTS exceeds the current limit threshold of 40mV, the current limit comparator immediately terminates the high-side gate driver output for cycle-by-cycle current limiting. Use the following equation to calculate the shunt resistance.

$$R_S = \frac{V_{CS(TH)}}{I_{OUT(CL)} + \frac{\Delta I_L}{2}} \tag{7}$$

where

- $V_{CS(TH)}$ is current sense threshold of 40mV.
- $I_{OUT(CL)}$ is the overcurrent setpoint that is set higher than the maximum load current to avoid tripping the overcurrent comparator during load transients.
- ΔI_L is the peak-to-peak inductor ripple current.

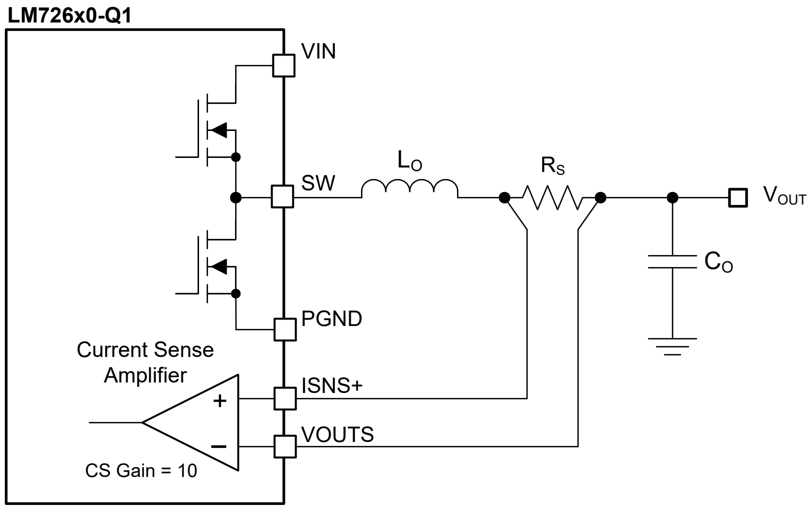


Figure 7-7. Shunt Current Sensing Implementation

The typical current sense delay ($t_{DELAY(CS)}$) is 85ns. Use the following equation to calculate the resultant inductor current overshoot above the overcurrent threshold.

$$I_{L(overshoot)} = \frac{(V_{IN} - V_{OUT}) \times t_{DELAY(CS)}}{L_O} \quad (8)$$

The respective SS voltage is clamped 75mV above FB during an overcurrent condition. The SS clamp only enables after the occurrence of 8 overcurrent events. This requirement makes sure that SS can be pulled low during brief overcurrent events, preventing output voltage overshoot during recovery.

7.3.16 Hiccup Mode Current Limiting

The LM72630-Q1 includes an internal hiccup mode protection function. When an overload condition occurs, a 512-cycle counter starts counting consecutive cycle-by-cycle current limit incidents after the internal soft-start sequence is completed. The 512-cycle counter is reset if four consecutive switching cycles occur without exceeding the current limit threshold. If after 512-cycle counts are completed, the internal soft start is pulled low and the internal high-side and low-side drivers are disabled. Then, a 16384 counter is enabled. After the counter reaches 16384, the internal soft start is enabled, and the output restarts. Note the hiccup mode current limit is not enabled during soft start and until the output voltage exceeds 50% of the set voltage.

Enable or disable the hiccup mode using HICCUP_EN bit.

7.3.17 Device Configuration (CNFG)

The LM72630-Q1 I2C address is configured and IMON function enabled as detailed in Table 7-6.

After VDDA is above 3.8V (typical), the CNFG/IMON pin is sampled and latched. The configuration is not easily changed. The LM72630-Q1 input voltage must be recycled and VCC must drop below 3.65V before the device can be reconfigured. Figure 7-8 shows the configuration timing diagram.

Table 7-6. Device Configuration

R_{CONFIG}	I2C ADDRESS	IMON
3.01kΩ	0x6A	Disabled
9.53kΩ	0x6B	Disabled
19.1kΩ	0x6C	Disabled
29.4kΩ	0x6D	Disabled
41.2kΩ	0x6A	Enabled
54.9kΩ	0x6B	Enabled
71.5kΩ	0x6C	Enabled
90.9kΩ	0x6D	Enabled

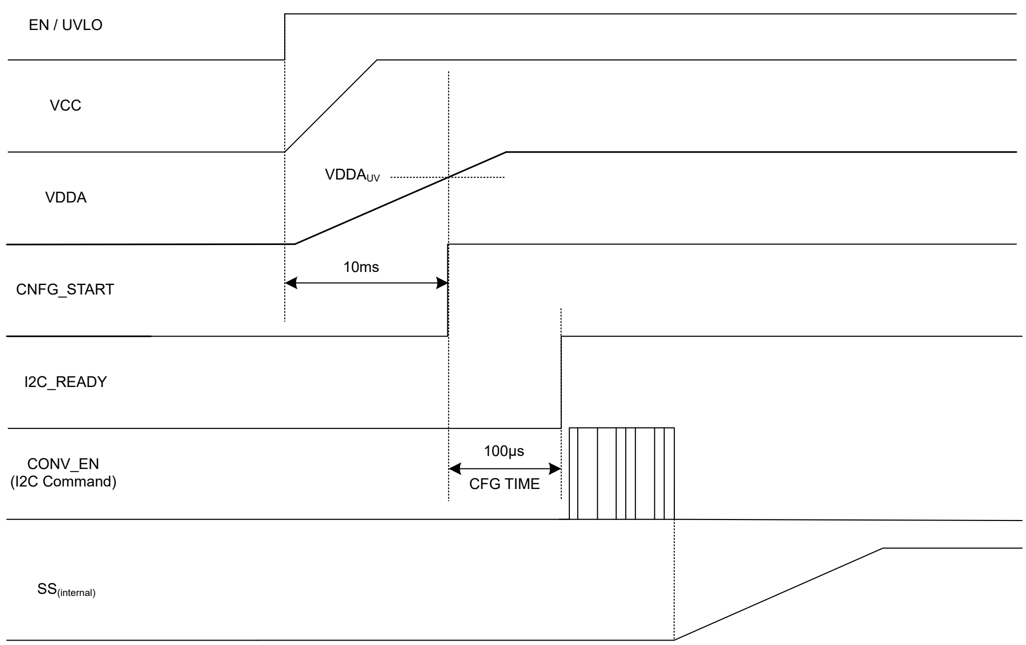


Figure 7-8. Configuration Timing

7.3.18 Pulse Frequency Modulation (PFM) / Synchronization

The LM72630-Q1 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation (DEM), the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss during light load operation. Note configuring the device for DEM has an effect of slower response to load transients during light load operation.

The diode emulation feature is configured with the PFM / SYNCIN pin or OVERRIDE_PFM and MODE bits. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect PFM / SYNCIN to VDDA or set OVERRIDE_PFM and MODE bits. If forced pulse-width modulation (FPWM) or continuous conduction mode (CCM) operation is desired, tie PFM / SYNCIN to AGND or set OVERRIDE_PFM bit and reset MODE bit. Note that diode emulation is automatically engaged to prevent reverse current flow during a prebias start-up in PFM. During start-up, when the output voltage approaches the regulation set point a gradual change from DCM to CCM occurs, preventing the output voltage overshoot. Changing the mode of operation dynamically is possible, however, the rate of change must be < 10Hz. The time to transition from PFM to FPWM operation is dependent on the output load current. In a typical application, the transition from PFM to FPWM operation occurs in less than 1ms if the output current is greater than 100mA. Similarly, for the output currents of around 1mA, the transition generally occurs in tens of milliseconds. Enable the output active discharge feature during the transition between PFM and FPWM to reduce the transition time. Select 24mA, 48mA, or 72mA active discharge strength using ACTIVE_DISCHARGE_STRENGTH bits.

If forced pulse-width modulation (FPWM) or continuous conduction mode (CCM) operation is desired, tie PFM / SYNCIN to AGND. Note that the LM72630-Q1 transitions from PFM to FPWM mode whenever LM72630-Q1 is reset. The time to transition to FPWM operation is dependent on the output load current. In a typical application, the transition from PFM to FPWM operation occurs in less than 1ms if the output current is greater than 100mA. Similarly, for the output currents of around 1mA, the transition generally occurs in tens of milliseconds.

To synchronize the LM72630-Q1 to an external source, apply a logic-level clock (greater than 2V) to the PFM / SYNCIN pin. The LM72630-Q1 can be synchronized to ±20% of the programmed frequency up to a maximum of 2.2MHz. Never synchronize the device to an external clock with frequency of < 100kHz. Under low V_{IN} conditions when the minimum off-time is reached, the synchronization signal is ignored, allowing the switching frequency to be reduced to maintain output voltage regulation.

When in FPWM mode, the time for the LM72630-Q1 to be synchronized to an external clock frequency is approximately 100µs. If an external clock is applied after start-up while operating in PFM mode, the time to synchronize the switching frequency is dependent on the output load current. In a typical application, switch synchronization and FPWM operation occurs in less than 1ms if the output current exceeds 100mA. Similarly, for the output currents of 1mA or more synchronization generally occurs in tens of milliseconds. Enable the output active discharge feature during the transition between PFM and FPWM to reduce the synchronization time.

7.3.19 Out-of-Audio™ Operation

When operating in PFM mode under light load conditions, the effective switching frequency can be in the audible frequency range (< 20kHz). For applications requiring switching frequency to be outside of the audible range (> 20kHz), the LM72630-Q1 provides an Out-of-Audio operation feature that can limit the switching frequency to 20kHz with minimal load.

Enable the Out-of-Audio operation while in PFM mode by setting the OUT_OF_AUDIO bit to high (0xD9[2] = 1b). With the Out-of-Audio operation enabled, the minimum inductor peak current criteria for PFM switching is disabled allowing much less energy to be delivered to the output each cycle. This dramatically reduces the minimum output current required to switch continuously at the nominal switching frequency. Additionally, the maximum number of skipped off times while in dropout is reduced from 16x to 8x when the switching frequency is set to 200kHz.

7.3.20 Thermal Shutdown (TSD)

The LM72630-Q1 includes an internal junction temperature monitor of the controller die. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

1. Turns off the high-side and low-side MOSFETs
2. Turns off the VCC regulator
3. Sets the TEMPERATURE bit in the STATUS_BYTE and STATUS_WORD registers
4. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 15°C (typical).

This protection is a non-latching protection, therefore, the device cycles into and out of thermal shutdown if the fault persists. If VCC or VDDA fall below the respective UVLO thresholds while in thermal shutdown, the LM72630-Q1 clears the STATUS_BYTE and STATUS_WORD registers upon exiting thermal shutdown.

Note that depending on the operating conditions, the high-side FET or low-side FET die can be at higher temperature than the controller die. Careful thermal design is necessary to ensure junction temperature of the FETs stays within rated limits. See also Section 9.1.3.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN / UVLO pin provides ON and OFF control for the LM72630-Q1. When V_{EN} is below 0.55V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 4.7µA (typical). The LM72630-Q1 also includes undervoltage (UV) protection of the internal bias LDO. If the internal bias supply voltage is below the UV threshold level, the switching regulator remains off.

7.4.2 Standby Mode

The internal bias LDO has a lower enable threshold than the switching regulator. When V_{EN} is above 0.55V and below the precision enable threshold (1V typical), the internal VCC and VDDA LDOs are enabled and regulating, the default register values and trim bits are loaded, the digital block is disabled, the device is not switching, and the I_Q current is 310µA (typical).

7.4.3 Ready Mode

When the enable voltage is above 1V and after the 100µs (typical) enable to ready delay, the LM72630-Q1 is in ready mode. When in ready mode, the I^2C interface is available, the device is not switching, and the I_Q current is 1mA (typical).

7.4.4 Active Mode

The LM72630-Q1 is in active mode when V_{EN} is above the precision enable threshold, the internal bias rail is above the UV threshold level, and when the CONV_EN bit in the OPERATION register is set. In active mode, the device operates in one of two modes depending on the load current, input voltage, output voltage, and PFM / SYNCIN pin configuration:

1. Forced pulse width modulation (FPWM) mode. This mode of operation is configured by tying the PFM / SYNCIN pin to GND or driving with an external clock source. The device operates in continuous conduction mode (CCM) with fixed switching frequency regardless of the load current.
2. Pulse frequency modulation (PFM) mode. This mode of operation is configured by tying the PFM / SYNCIN pin to VDDA. The device operates in discontinuous conduction mode (DCM) if the load current is less than half of the peak-to-peak inductor current, otherwise the device operates in continuous conduction mode (CCM). The transition between CCM and DCM is automatic.

7.4.5 Sleep Mode

The LM72630-Q1 operates with peak current-mode control such that the compensation voltage is proportional to the peak inductor current. During no-load or light-load conditions, the output capacitor discharges very slowly. As a result, the compensation voltage goes low and the switching is stopped. When the LM72630-Q1 controller detects 16 missed switching cycles, the LM72630-Q1 enters sleep mode and switches to a low $I_{Q\text{-}SLEEP}$ state to reduce the current drawn from the input. For the LM72630-Q1 to go into sleep mode, the device must be programmed for PFM mode.

7.5 Programming

7.5.1 I2C Bus Operation

The I 2 C bus is a communications link between a controller and a series of target devices. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the target terminals. Each device has an open-drain output to transmit data on the serial data line (SDA). Place an external pullup resistor on the serial data line to pull the drain output high during data transmission. The device hosts a target I 2 C that supports standard-mode, fast-mode and fast-mode plus operation with data rates up to 100kbit/s, 400kbit/s and 1000kbit/s respectively and auto-increment addressing compatible to I 2 C standard 3.0.

The 7-bit target address of this device is set by CNFG pin according to Table 7-6.

Data transmission is initiated with a start bit from the controller as shown in the figure below. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device receives serial data on the SDA input and checks for a valid address and control information. If the target address bits are set for the device, then the device issues an acknowledge pulse and prepares to receive the register address and data. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line targeted to occur during the low portion of the SCL signal for valid communication. An acknowledge is issued after the reception of valid address, sub-address, and data words. The I2C interfaces auto-sequence through register addresses, to send multiple data words for a given I2C transmission.

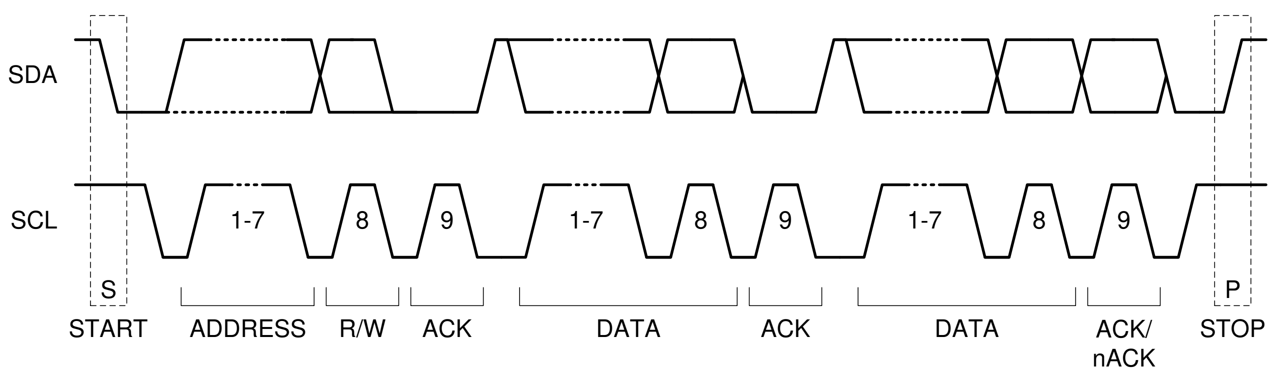


Figure 7-9. I 2 C START / STOP / ACKNOWLEDGE Protocol

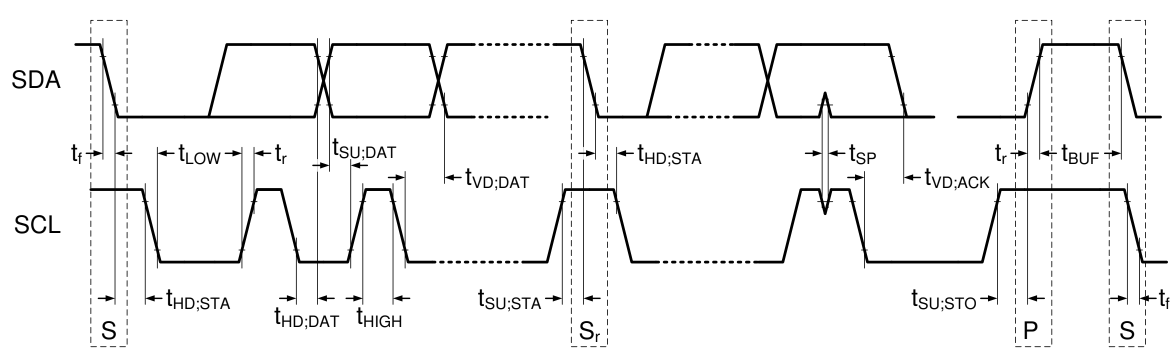


Figure 7-10. I 2 C Data Transmission Timing

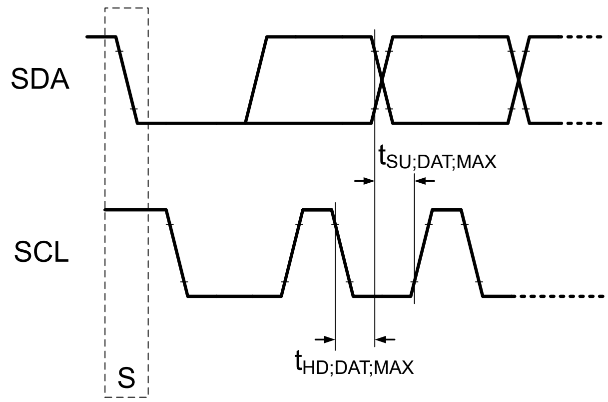


Figure 7-11. I 2 C Data Transmission Timing for Maximum Rise and Fall Times

7.5.2 Clock Stretching

Clock stretching is not supported. If the device is addressed while busy and not able to process the received data, the transaction is not acknowledged. TI recommends using this device in I2C systems with an I2C timeout feature.

7.5.3 Data Transfer Formats

The device supports four different read/write operations:

- Single read from a defined register address
- Single write to a defined register address
- Sequential read starting from a defined register address
- Sequential write starting from a defined register address

7.5.4 Single READ from a Defined Register Address

Figure 7-12 shows the format of a single read from a defined register address. First, the controller issues a start condition followed by a seven-bit I^{2}C address. Next, the controller writes a zero to signify that the controller is conducting a write operation. Upon receiving an acknowledge from the target the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the internal I^{2}C register number to the defined value. Then the controller issues a repeat start condition and the seven-bit I^{2}C address followed by a one to signify that the controller is conducting a read operation. Upon receiving a third acknowledge, the controller releases the bus to the device. The device then returns the eight-bit data value from the register on the bus. The controller does not acknowledge (nACK) and issues a stop condition. This action concludes the register read.

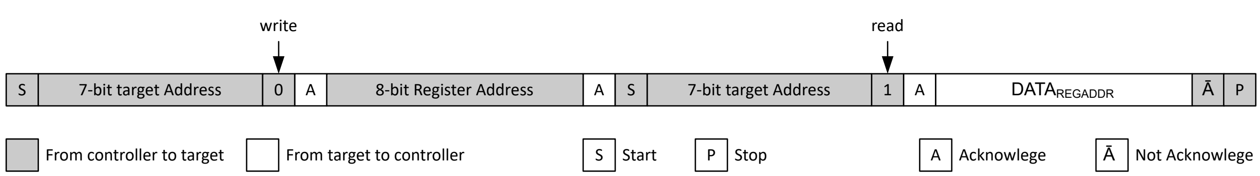


Figure 7-12. Single READ From a Defined Register Address

7.5.5 Sequential READ Starting from a Defined Register Address

A sequential read operation is an extension of the single read protocol and shown in Figure 7-13. The controller acknowledges the reception of a data byte, and the device auto increments the register address and returns the data from the next register. The data transfer is stopped by the controller not acknowledging the last data byte and sending a stop condition.

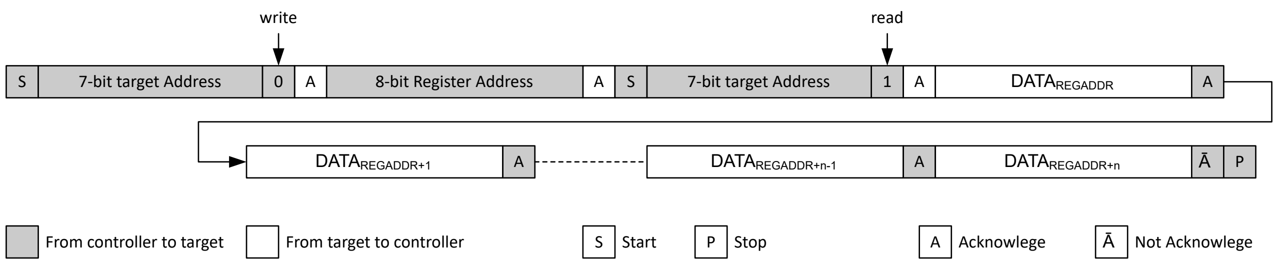


Figure 7-13. Sequential READ Starting from a Defined Register Address

7.5.6 Single WRITE to a Defined Register Address

Figure 7-14 shows the format of a single write to a defined register address. First, the controller issues a start condition followed by a seven-bit I^2C address. Next, the controller writes a zero to signify that the controller is trying to conduct a write operation. Upon receiving an acknowledge from the target, the controller sends the eight-bit register address across the bus. Following a second acknowledge the device sets the I^2C register address to the defined value and the controller writes the eight-bit data value. Upon receiving a third acknowledge the device auto increments the I^2C register address by one and the controller issues a stop condition. This action concludes the register write.

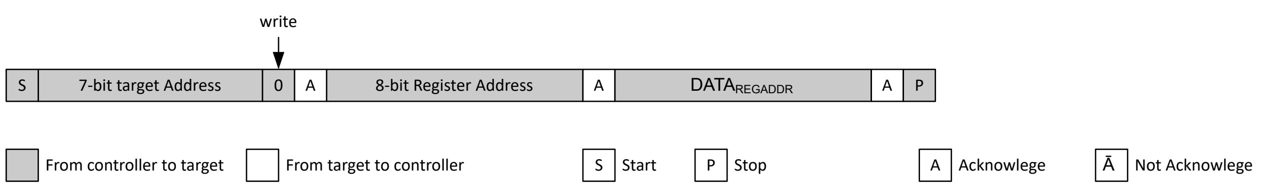


Figure 7-14. Single WRITE to Defined Register Address

7.5.7 Sequential WRITE Starting at a Defined Register Address

A sequential write operation is an extension of the single write protocol and shown in Figure 7-15. If the controller does not send a stop condition after the device has issued an ACK, the device auto increments the register address by one and the controller is able to write to the next register.

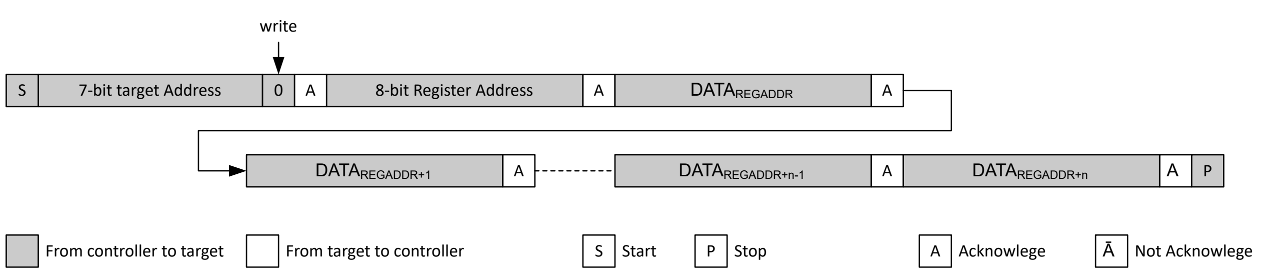


Figure 7-15. Sequential WRITE Starting at a Defined Register Address

8 LM72630-Q1 Registers

Table 8-1 lists the memory-mapped registers for the LM72630-Q1 registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. LM72630-Q1 Registers

Address	Acronym	Register Name	Section
1h	OPERATION	Operation register	Section 8.1
3h	CLEAR_FAULTS	Clear faults register	Section 8.2
21h	VOUT_COMMAND	Set output voltage register	Section 8.3
78h	STATUS_BYTE	Device status register	Section 8.4
79h	STATUS_WORD	Device status word	Section 8.5
D0h	MFR_DEVICE_CFG_D0	Set average output current limit register	Section 8.6
D1h	MFR_DEVICE_CFG_D1	Device configuration register 1	Section 8.7
D2h	MFR_DEVICE_CFG_D2	Device configuration register 2	Section 8.8
D5h	MFR_DEVICE_CFG_D5	Device configuration register 3	Section 8.9
D8h	MFR_DEVICE_CFG_D8	Device configuration register 4	Section 8.10
D9h	MFR_DEVICE_CFG_D9	Device configuration register 5	Section 8.11

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. LM72630-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1 OPERATION Register (Address = 1h) [Reset = 00h]

OPERATION is shown in Table 8-3.

Return to the Summary Table.

Operation register is used to enable or disable the device.

Table 8-3. OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONV_EN	R/W	0h	Converter enable bit. 0h = Disabled 1h = Enabled
6-0	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.

8.2 CLEAR_FAULTS Register (Address = 3h) [Reset = 00h]

CLEAR_FAULTS is shown in Table 8-4.

Return to the Summary Table.

Clear faults register is used to clear the fault bits in the status register 0x78h.

Table 8-4. CLEAR_FAULTS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLEAR_FAULTS	R	0h	Clear faults bit. A READ operation clears STATUS_BYTE and STATUS_WORD registers. Note, each individual STATUS_BYTE or STATUS_WORD bit can also be cleared by setting it to a 1 with a WRITE operation. Recycling power or toggling EN pin clears STATUS_BYTE and STATUS_WORD registers as well.

8.3 VOUT_COMMAND Register (Address = 21h) [Reset = 00FAh]

VOUT_COMMAND is shown in Table 8-5.

Return to the Summary Table.

Set output voltage register is used to set the target output voltage.

Table 8-5. VOUT_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
11-8	VOUT_MSB	R/W	0h	Output voltage setting upper byte. Lower limit: 3.3V (1V) Upper limit: 24V Step size: 20mV (10mV) SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0000h = 3.3V (1V) 0064h = 3.3V (1V) 00A5h = 3.3V (1.65V) 00FAh = 5V (2.5V) 01C2h = 9V (4.5V) 02EEh = 15V (7.5V) 03E8h = 20V (10V) 04B0h = 24V (12V) 0960h = 24V (24V) FFFFh = 24V (24V)
7-0	VOUT_LSB	R/W	FAh	Output voltage setting lower byte. Lower limit: 3.3V (1V) Upper limit: 24V Step size: 20mV (10mV) SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0000h = 3.3V (1V) 0064h = 3.3V (1V) 00A5h = 3.3V (1.65V) 00FAh = 5V (2.5V) 01C2h = 9V (4.5V) 02EEh = 15V (7.5V) 03E8h = 20V (10V) 04B0h = 24V (12V) 0960h = 24V (24V) FFFFh = 24V (24V)

8.4 STATUS_BYTE Register (Address = 78h) [Reset = 00h]

STATUS_BYTE is shown in Table 8-6.

Return to the Summary Table.

Device status register.

Table 8-6. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R/W	0h	Device busy status bit. If set, the device is busy and unable to respond. 0h = No fault 1h = Fault
6	OFF	R/W	0h	Device on/off status bit. If set, the device is disabled / off. 0h = No fault 1h = Fault
5	VOUT_OV	R/W	0h	Device output overvoltage status bit. If set, the voltage on the device output has exceeded the set OVP threshold. 0h = No fault 1h = Fault
4	IOUT_OC	R/W	0h	Device output overcurrent status bit. If set, the cycle-by-cycle current limit has been triggered. 0h = No fault 1h = Fault
3	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
2	TEMPERATURE	R/W	0h	Device overtemperature status bit. If set, the device temperature has triggered the thermal shut down (TSD) threshold. 0h = No fault 1h = Fault
1	CML	R/W	0h	Device communication, memory, or logic fault status bit. If triggered, the device communication, memory, or logic error has occurred. 0h = No fault 1h = Fault
0	NONE_OF_THE_ABOVE	R/W	0h	Device other fault or warning status bit. If set, a fault or warning not listed in the status byte has occurred. 0h = No fault 1h = Fault

8.5 STATUS_WORD Register (Address = 79h) [Reset = 0000h]

STATUS_WORD is shown in Table 8-7.

Return to the Summary Table.

Device status word.

Table 8-7. STATUS_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VOUT	R/W	0h	Device output voltage status bit. If set, the voltage on the device output has exceeded the set OVP threshold or PG OV threshold. 0h = No fault 1h = Fault
14	IOUT_POUT	R/W	0h	Output current or output power warning. 0h = No fault 1h = Fault
13	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
12	CC_STATUS	R/W	0h	Constant current (CC) status bit. If set, the device operates in CC regulation mode. Otherwise, the device operates in constant voltage (CV) regulation mode. 0h = CV regulation 1h = CC regulation
11	nPG_STATUS	R	0h	Power not good status bit. If set, the voltage on the output of the device has triggered either PG UV or PG OV threshold. 0h = No fault 1h = Fault
10	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
9	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
8	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
7	BUSY	R/W	0h	Device busy status bit. If set, the device is busy and unable to respond. 0h = No fault 1h = Fault
6	OFF	R/W	0h	Device on/off status bit. If set, the device is disabled / off. 0h = No fault 1h = Fault
5	VOUT_OV	R/W	0h	Device output overvoltage status bit. If set, the voltage on the device output has exceeded the set OVP threshold. 0h = No fault 1h = Fault
4	IOUT_OC	R/W	0h	Device output overcurrent status bit. If set, the cycle-by-cycle current limit has been triggered. 0h = No fault 1h = Fault
3	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
2	TEMPERATURE	R/W	0h	Device overtemperature status bit. If set, the device temperature has triggered the thermal shut down (TSD) threshold. 0h = No fault 1h = Fault

Table 8-7. STATUS_WORD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CML	R/W	0h	Device communication, memory, or logic fault status bit. If triggered, the device communication, memory, or logic error has occurred. 0h = No fault 1h = Fault
0	NONE_OF_THE_ABOVE	R/W	0h	Device other fault or warning status bit. If set, a fault or warning not listed in the status byte has occurred. 0h = No fault 1h = Fault

8.6 MFR_DEVICE_CFG_D0 Register (Address = D0h) [Reset = 0Ah]

MFR_DEVICE_CFG_D0 is shown in Table 8-8.

Return to the Summary Table.

Set average output current limit register.

Table 8-8. MFR_DEVICE_CFG_D0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AVG_ILIM_THRESHOLD	R/W	Ah	Set average output current limit threshold. Assumes 8mΩ sense resistor is selected. Lower limit: 0.5A Upper limit: 4.5A Step size: 50mA 0h = 0.5A Ah = 0.5A 3Ch = 3A 5Ah = 4.5A FFh = 4.5A

8.7 MFR_DEVICE_CFG_D1 Register (Address = D1h) [Reset = 8Ah]

MFR_DEVICE_CFG_D1 is shown in Table 8-9.

Return to the Summary Table.

Device configuration register 1 is used to select FB divider, configure DRSS function, set the switching frequency, and select compensation for the constant current loop.

Table 8-9. MFR_DEVICE_CFG_D1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SEL_FB_DIV20	R/W	1h	Select FB divider. The selection determines the output voltage range and step size. 0h = DIV10 (10mV step size, 1V-24V range) 1h = DIV20 (20mV step size, 3.3V-24V range)
6	DRSS_EN	R/W	0h	Enable DRSS function. 0h = DRSS disabled 1h = DRSS enabled
5	DRSS_FMOD	R/W	0h	Select DRSS triangular modulation frequency. 0h = 10kHz 1h = 2.5kHz
4-3	FREQ	R/W	1h	Select switching frequency. 0h = 200kHz 1h = 400kHz 2h = 600kHz 3h = 2.2MHz
2-1	CC_COMP	R/W	1h	Select CC compensation time constant. 0h = 0.1ms 1h = 0.2ms 2h = 0.3ms 3h = 0.4ms
0	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.

8.8 MFR_DEVICE_CFG_D2 Register (Address = D2h) [Reset = C9h]

MFR_DEVICE_CFG_D2 is shown in Table 8-10.

Return to the Summary Table.

Device configuration register 2 is used to configure output active discharge, output voltage slew rate, and select soft-start time.

Table 8-10. MFR_DEVICE_CFG_D2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ACTIVE_DISCHARGE_CFG1	R/W	1h	Enable active discharge during VOUT high to low transition. 0h = Disabled 1h = Enabled
6	ACTIVE_DISCHARGE_CFG2	R/W	1h	Enable active discharge during PFM to FPWM transition. 0h = Disabled 1h = Enabled
5	ACTIVE_DISCHARGE_CFG3	R/W	0h	Enable continuous active discharge. 0h = Disabled 1h = Enabled
4-3	VOUT_SLEW_RATE	R/W	1h	Select output voltage slew rate. SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0h = 40mV/us (20mV/us) 1h = 20mV/us (10mV/us) 2h = 1mV/us (0.5mV/us) 3h = 0.5mV/us (0.25mV/us)
2-1	ACTIVE_DISCHARGE_STRENGTH	R/W	0h	Select active discharge strength. 0h = Disabled 1h = 24mA 2h = 48mA 3h = 72mA
0	SOFT_START_TIME	R/W	1h	Select soft-start ramp time. SEL_FB_DIV20 =1 (SEL_FB_DIV20 =0) 0h = 5V/ms (2.5V/ms) 1h = 2.5V/ms (1.25V/ms)

8.9 MFR_DEVICE_CFG_D5 Register (Address = D5h) [Reset = 65h]

MFR_DEVICE_CFG_D5 is shown in Table 8-11.

Return to the Summary Table.

Device configuration register 3 is used to enable and configure overvoltage protection (OVP) function and set OVP thresholds.

Table 8-11. MFR_DEVICE_CFG_D5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved. This bit is not implemented in hardware. During write operations data for this bit is ignored. During read operations the value of 0 is returned.
6	OVP_EN	R/W	1h	Enable OVP detection. 0h = Disabled 1h = Enabled
5	OVP_CFG	R/W	1h	Configure OVP detection. 0h = OVP detection only results in the Status register update 1h = OVP detection interrupts switching, discharges VOUT, sets the VOUT_OV bit in the Status register
4-0	OVP_THRESHOLD	R/W	5h	Select OVP rising threshold. Lower limit: 105% Upper limit: 136% Step size: 1% 0h = 105% 5h = 110% Ah = 115% 1Fh = 136%

8.10 MFR_DEVICE_CFG_D8 Register (Address = D8h) [Reset = CAh]

MFR_DEVICE_CFG_D8 is shown in Table 8-12.

Return to the Summary Table.

Device configuration register 4 is used to set the NINT mask, enable a connection from the VCC regulator input to the VOUTF pin, enable and configure gain of the cable drop compensation function.

Table 8-12. MFR_DEVICE_CFG_D8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NINT_MASK	R/W	1h	Mask NINT for all STATUS register bits except the CC_STATUS bit. 0h = NINT for most STATUS BYTE/WORD faults. 1h = NINT for only CC_STATUS bit.
6	BIAS_EN	R/W	1h	Enable connection from the VCC regulator bias input to the VOUTF pin. 0h = Disabled 1h = Enabled
5	CDC_EN	R/W	0h	Enable cable drop compensation. 0h = Disabled 1h = Enabled
4-0	CDC_GAIN	R/W	Ah	Configure CDC gain. Lower limit: 0V/V Upper limit: 62V/V Step size: 2V/V 0h = 0V/V 1h = 2V/V Ah = 20V/V 1Fh = 62V/V

8.11 MFR_DEVICE_CFG_D9 Register (Address = D9h) [Reset = 00h]

MFR_DEVICE_CFG_D9 is shown in Table 8-13.

Return to the Summary Table.

Device configuration register 5 is used to enable MFI function, enable HICCUP mode, override mode selection of the PFM pin, select MODE, and power good (PG) detection window.

Table 8-13. MFR_DEVICE_CFG_D9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MFI_EN	R/W	0h	Enable MFI CC regulation (1.67xILIM for the 1ms of CC regulation). 0h = Disabled 1h = Enabled
6	HICCUP_EN	R/W	0h	Enable HICCUP operation. 0h = Disabled 1h = Enabled
5	OVERRIDE_PFM	R/W	0h	Override PFM pin setting. 0h = PFM pin sets the mode of operation 1h = MODE bit sets the mode of operation
4	MODE	R/W	0h	Select mode of operation. 0h = FPWM 1h = PFM
3	PG_10PCT	R/W	0h	Select PG window. 0h = 5% 1h = 10%
2	OUT_OF_AUDIO	R/W	0h	Enable out-of-audio mode of operation. 0h = Disabled 1h = Enabled
1	SPARE1	R/W	0h	Spare bit#1 0h = Disabled 1h = Enabled
0	SPARE0	R/W	0h	Spare bit#0 0h = Disabled 1h = Enabled

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Power Train Components

A comprehensive understanding of the buck regulator power train components is critical to successfully completing a synchronous buck regulator design. The following sections discuss the output inductor, input and output capacitors, EMI input filter, and compensation components.

9.1.1.1 Buck Inductor

For most applications, choose a buck inductance such that the inductor ripple current, ΔI_L, is between 30% to 50% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 9 based on a peak inductor current given by Equation 10.

$$L_O = \frac{V_{OUT}}{\Delta I_L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{9}$$

$$I_{L(PK)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{10}$$

Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This action results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally decreases as the core temperature increases. Accurate overcurrent protection is key to avoiding inductor saturation.

9.1.1.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, select an output capacitance that is larger than that given by the following equation.

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times F_{SW}\sqrt{\Delta V_{OUT}^2 + (R_{ESR} \times \Delta I_L)^2}} \tag{11}$$

Figure 9-1 conceptually shows the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

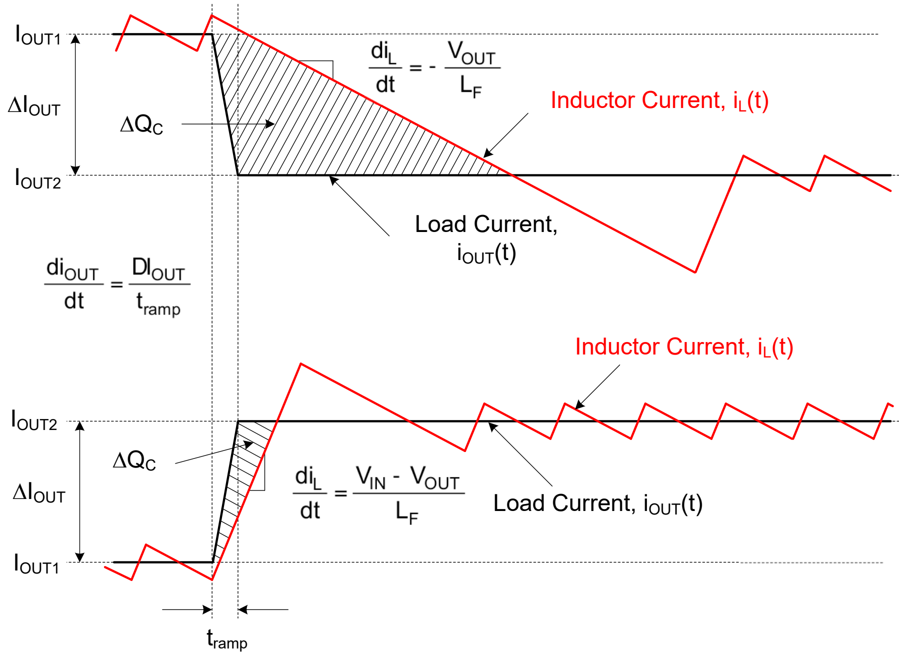


Figure 9-1. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 12V input to low output voltage (for example, 3.3V), the load-off transient represents the worst case in terms of output voltage transient deviation. In that conversion ratio application, the steady-state duty cycle is approximately 28% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $–V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below the nominal level following the load step. In this scenario, advantageously employ a large output capacitance to absorb the excess charge and minimize the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance must be larger than:

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} \tag{12}$$

The ESR of a capacitor is provided in the manufacturer data sheet either explicitly as a specification or implicitly in the impedance versus frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 5mΩ and above, and relatively large ESL, 5nH to 20nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, conversely, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

Ignoring the ESR term in Equation 11 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. Use Equation 12 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid and high-frequency decoupling characteristics with the low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with the large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

9.1.1.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X7S or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. Use the following equation to calculate the input capacitor RMS current for a single-channel buck regulator.

$$I_{CIN(rms)} = \sqrt{D \times \left(I_{OUT}^2 \times (1 - D) + \frac{\Delta I_L{}^2}{12}\right)} \tag{13}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the input capacitors must be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude ($I_{OUT} - I_{IN}$) during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together, with the ESR-related ripple component, calculate the peak-to-peak ripple voltage amplitude using the following equation.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \tag{14}$$

Calculate the input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN} using the following equation.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \tag{15}$$

Place low-ESR ceramic capacitors in parallel with higher valued bulk capacitance to provide peak input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. Select the input bulk capacitor based on the ripple current rating and operating temperature range.

9.1.1.4 EMI Filter

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^2}{P_{IN}} \right| \tag{16}$$

The EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter.
- Input filter inductor L_{IN} is usually selected between 1µH and 10µH, but can be lower to reduce losses in a high-current design.
- Calculate input filter capacitor C_F.

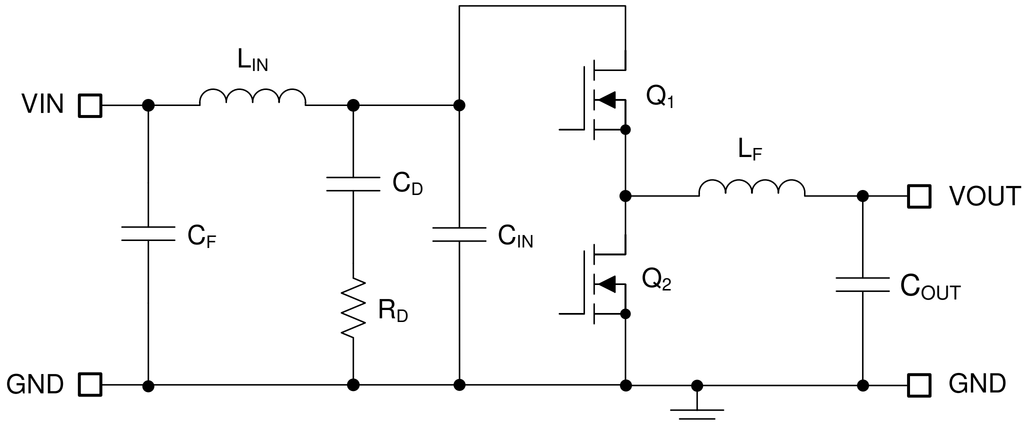


Figure 9-2. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 17.

$$\mathrm{Attn} = 20\log\left(\frac{I_{L(PEAK)}}{\pi^2 \times F_{SW} \times C_{IN}} \times \sin(\pi \times D_{MAX}) \times \frac{1}{1\mu V}\right) - V_{MAX} \tag{17}$$

where

- V_{MAX} is the allowed dBµV noise level for the applicable conducted EMI specification, for example CISPR 25 Class 5.
- C_{IN} is the existing input capacitance of the buck regulator.
- D_{MAX} is the maximum duty cycle.
- I_{PEAK} is the peak inductor current.

For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from Equation 18.

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|\mathrm{Attn}|}{40}}}{2\pi \times F_{SW}}\right)^2 \tag{18}$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. Calculate the resonant frequency of the filter using the following equation.

$$f_{res} = \frac{1}{2\pi \times \sqrt{L_{IN} \times C_F}} \tag{19}$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D must have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by Equation 20.

$$C_D \geq 4 \times C_{IN} \tag{20}$$

Select the damping resistor R_D using Equation 21.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{21}$$

9.1.2 Error Amplifier and Compensation

A Type-II compensator using a transconductance error amplifier (EA) is shown in Figure 9-3. The dominant pole of the EA open-loop gain is set by the EA output resistance, R_{OEA}, and effective bandwidth-limiting capacitance, C_{BW} as shown by Equation 22.

$$G_{EA(openloop)}(s) = -\frac{g_m \times R_{OEA}}{1 + s \times R_{OEA} \times C_{BW}} \tag{22}$$

The EA high-frequency pole is neglected in the above expression. The compensator transfer function from output voltage to COMP node, including the gain contribution from the (internal or external) feedback resistor network, is calculated in Equation 23.

$$G_c(s) = \frac{\hat{v}_c(s)}{\hat{v}_{out}(s)} = -\frac{V_{REF}}{V_{OUT}} \times \frac{g_m \times R_{OEA} \times \left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \times \left(1 + \frac{s}{\omega_{p2}}\right)} \tag{23}$$

where

- V_{REF} is the feedback voltage reference.
- g_m is the EA gain transconductance of 1mS.
- $R_{O\text{-}EA}$ is the error amplifier output impedance of 70MΩ.

$$\omega_{z1} = \frac{1}{R_{COMP} \times C_{COMP}} \tag{24}$$

$$\omega_{p1} = \frac{1}{R_{OEA} \times (C_{COMP} + C_{HF} + C_{BW})} \cong \frac{1}{R_{OEA} \times C_{COMP}} \tag{25}$$

$$\omega_{p2} = \frac{1}{R_{COMP} \times (C_{COMP} \,||\, (C_{HF} + C_{BW}))} \cong \frac{1}{R_{COMP} \times C_{HF}} \tag{26}$$

The EA compensation components create a pole close to the origin, a zero, and a high-frequency pole. Typically, R_{COMP} << $R_{O\text{-}EA}$ and C_{COMP} >> C_{BW} and C_{HF}, so the approximations are valid. Figure 9-3 circles the poles in red and the zero in blue.

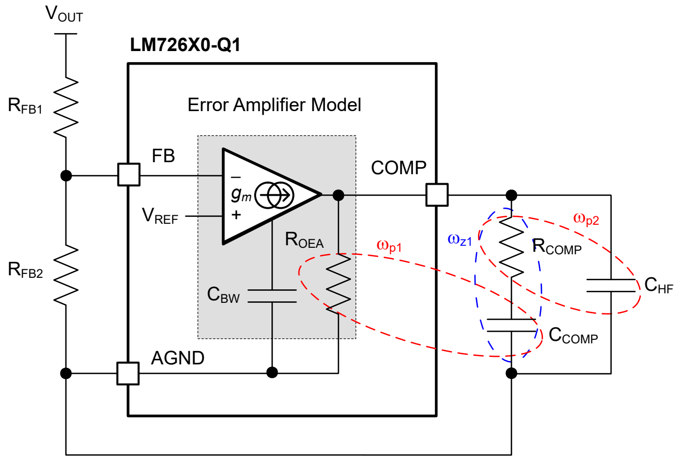


Figure 9-3. Error Amplifier and Compensation Network

9.1.3 Maximum Ambient Temperature

As with any power conversion device, the LM72630-Q1 dissipates internal power while operating. The effect of this power dissipation is the rise of the internal temperature of the converter above ambient temperature. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the device
- PCB layout

The maximum internal die temperature for the LM72630-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. Equation 27 shows the relationships between the important parameters. Larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the LM72630-Q1 quick-start design tool. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{(1-\eta)} \times \frac{1}{V_{OUT}} \tag{27}$$

where

- η = efficiency
- T_A = ambient temperature
- T_J = junction temperature
- $R_{\theta JA}$ = the effective thermal resistance of the IC junction to the air, mainly through the PCB

The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics* application note the JESD 51-7 value of $R_{\theta JA}$ given in *Thermal Information* is not valid for design purposes and must not be used to estimate the thermal performance of the device in a real application. The JESD 51-7 values reported in *Thermal Information* are measured under a specific set of conditions that are rarely obtained in an actual application.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors. The following are the most critical parameters:

- Power dissipation
- Air temperature
- Airflow
- PCB area
- Copper heat-sink area

- Number of thermal vias under or near the package
- Adjacent component placement

Typical curves of maximum output current versus ambient temperature are shown in *Derating Curves* for a good thermal layout.

Use *Thermal Design Resources* as a guide for thermal PCB design and estimating $R_{\theta JA}$ for a given application environment.

9.1.3.1 Derating Curves

The data in this section is taken on the LM72880QEVM evaluation board (BOM updated for LM72630-Q1) with a device and PCB combination giving an $R_{\theta JA}$ of approximately 19°C/W. The actual performance for a given application depends on the previously mentioned factors. Use the Thermal Design Resources as a guide for thermal design of the PCB and to estimate $R_{\theta JA}$ for a given application environment.

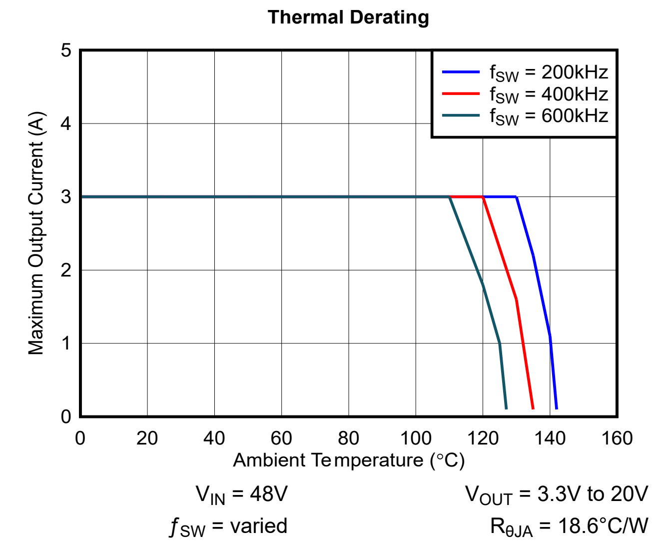


Figure 9-4. Maximum Output Current versus Ambient Temperature

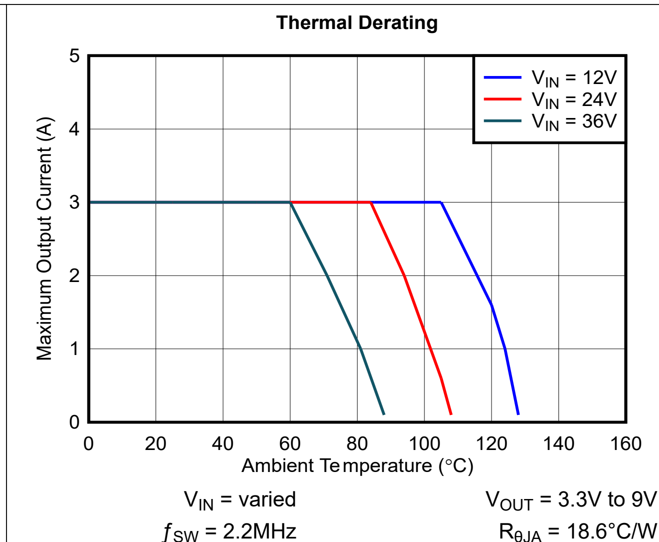


Figure 9-5. Maximum Output Current versus Ambient Temperature

9.2 Typical Application

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results, refer to *TI Designs* reference design library.

9.2.1 High Efficiency, Wide Input, 400kHz, Synchronous Buck Regulator

Figure 9-6 shows the schematic diagram of a single-output, synchronous, buck regulator with I2C interface, which provides maximum output voltages of 20V and a rated load current of 3A. In this example, the target full-load efficiencies at 24V and 48V inputs are 98.3% and 96.6%, respectively. The regulator is designed for 400kHz switching frequency.

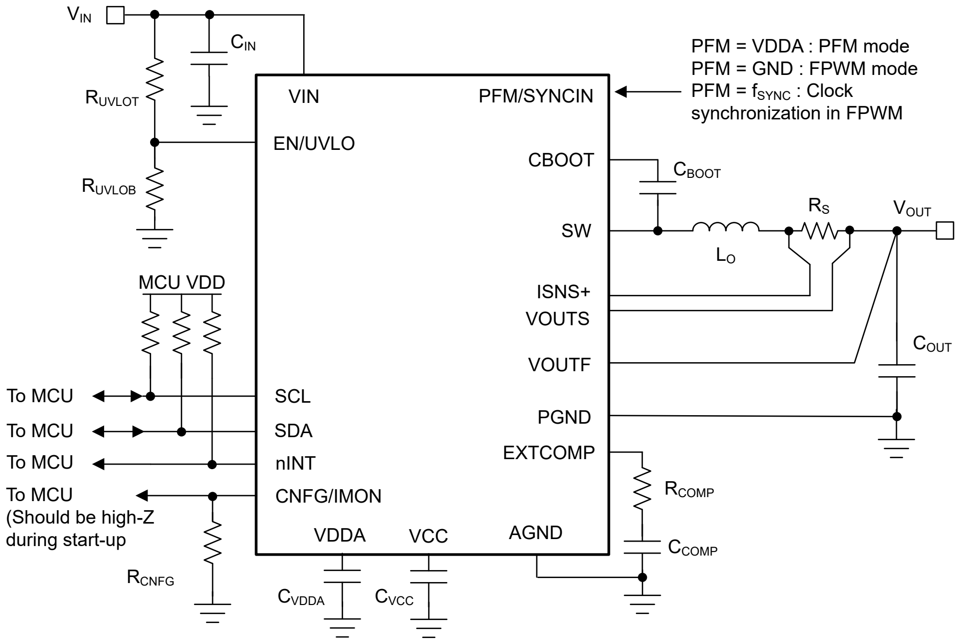


Figure 9-6. Application Circuit With I2C Interface

Note

This and subsequent design examples are provided herein to showcase the device in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor can be required at the input to make sure of stability, particularly at low input voltage and high output current operating conditions. See also Section 9.3.

9.2.1.1 Design Requirements

Table 9-1 shows the intended input, output, and performance parameters for this USB-C PD design example.

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	24V to 70V
Output voltage	Maximum 20V
Output current	Rated 3A
Switching frequency	Typical 400kHz

The switching frequency, the output regulation target in CV mode, and the output current limit in CC mode must be programmed by I2C before enabling the converter. In terms of control loop performance, the target loop crossover frequency is 30kHz with a phase margin greater than 50°.

The selected buck regulator powertrain components are cited in Table 9-2, and many of the components are available from multiple vendors. This design uses a low-DCR composite inductor.

Table 9-2. List of Materials for Application Circuit

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	4	4.7µF, 100V, X7S, 1210, ceramic	Murata	GCM32DC72A475KE02L
C_O	1	47µF, 25V, ±20%, SMD, aluminum - polymer	Chemi-Con	HHXC250ARA470MF61G
	2	10µF, 25V, X7R, 1210, ceramic	TDK	CGA6P1X7R1E106M250AC
L_O	1	22µH, 19.6mΩ, 13.2A, shielded	Coilcraft	XGL1010-223MED
R_S	1	Shunt, 8mΩ, 0508, 1W	Susumu	KRL2012M-R008
U_1	1	70V buck converter with I^2C interface	Texas Instruments	LM72630-Q1

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM72630-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.2.2 Buck Inductor

1. Use Equation 28 to calculate the required buck inductance based on a 40% inductor ripple current at nominal input voltages.

$$L_O = \frac{V_{OUT}}{\Delta I_{LO} \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) = \frac{20V}{1.2A \times 400kHz} \times \left(1 - \frac{20V}{48V}\right) = 24.3\mu H \tag{28}$$

2. Select a standard inductor value of 22µH. Use Equation 29 to calculate the peak inductor currents at maximum steady-state input voltage. Subharmonic oscillation occurs with a duty cycle greater than 50% for peak current-mode control. For design simplification, the device has an internal slope compensation ramp proportional to the switching frequency that is added to the current sense signal to damp any tendency toward subharmonic oscillation.

$$\begin{aligned} I_{LO(PK)} &= I_{OUT} + \frac{\Delta I_{LO}}{2} = I_{OUT} + \frac{V_{OUT}}{2 \times L_O \times F_{SW}} \times \left[1 - \frac{V_{OUT}}{V_{IN(max)}}\right] \\ &= 3A + \frac{20V}{2 \times 22\mu H \times 400kHz} \times \left[1 - \frac{20V}{70V}\right] \\ &= 3.812A \end{aligned} \tag{29}$$

3. Based on Equation 6, use Equation 30 to cross-check the inductance to set a slope compensation close to the ideal one times the inductor current downslope.

$$L_{O(sc)} = \frac{V_{OUT} \times R_S}{24 \times F_{SW}} = \frac{20V \times 8m\Omega}{24 \times 0.4MHz} = 16.6\mu H \tag{30}$$

9.2.1.2.3 Current-Sense Resistance

1. Calculate the current-sense resistance based on a maximum peak current capability of at least 20% – 25% higher than the peak inductor current at full load to provide sufficient margin during start-up and load-on transients. Calculate the current sense resistance using Equation 31.

$$R_S = \frac{V_{CS(TH)}}{1.2 \times I_{LO(PK)}} = \frac{40mV}{1.2 \times 3.812} = 8.7m\Omega \tag{31}$$

where

$V_{CS(TH)}$ is the 40mV current limit threshold.
2. Select a standard resistance value of 8mΩ for the shunt. A 0508 footprint component with wide aspect ratio termination design provides 1W power rating, low parasitic series inductance, and compact PCB layout. Carefully observe the *Layout Guidelines* to make sure that noise and DC errors do not corrupt the differential current-sense voltages measured at the ISNS+ and VOUTS pins.
3. Place the shunt resistor close to the inductor.
4. Use Kelvin-sense connections, and route the sense lines differentially from the shunt to the device.
5. The ISNS-to-output propagation delay (related to the current limit comparator, internal logic and power MOSFET gate drivers) causes the peak current to increase above the calculated current limit threshold. For a total propagation delay $t_{ISNS(delay)}$ of 85ns, use Equation 32 to calculate the worst-case peak inductor current with the output shorted.

$$I_{LOPK(SC)} = \frac{V_{CS(TH)}}{R_S} + \frac{V_{IN(max)} \times t_{ISNS(delay)}}{L_O} = \frac{40mV}{8m\Omega} + \frac{70V \times 85ns}{22\mu H} = 5.27A \tag{32}$$

6. Based on this result, select an inductor with saturation current greater than 8A across the full operating temperature range.

9.2.1.2.4 Output Capacitors

1. Use Equation 33 to estimate the output capacitance required to manage the output voltage overshoot during a load-off transient (from full load to no load), assuming a load transient deviation specification of 0.5% (100mV for a 20V output).

$$C_{OUT} \geq \frac{L_O \times \Delta I_{OUT}^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2} = \frac{22\mu H \times (3A)^2}{(20V + 100mV)^2 - 20V^2} = 49\mu F \tag{33}$$

2. Noting the voltage coefficient of ceramic capacitors where the effective capacitance decreases significantly with applied voltage, select two 10µF, 25V, X7R, 1210 ceramic output capacitors, and one 47µF, 25V, aluminum-polymer capacitor. Generally, when sufficient capacitance is used to satisfy the load-off transient response requirement, the voltage undershoot during a no-load to full-load transient is also satisfactory.
3. Use Equation 34 to estimate the peak-peak output voltage ripple at nominal input voltage.

$$\Delta V_{OUT} = \sqrt{\left(\frac{\Delta I_{LO}}{8 \times F_{SW} \times C_{OUT}}\right)^2 + (R_{ESR} \times \Delta I_{LO})^2} = \sqrt{\left(\frac{1.326A}{8 \times 400kHz \times 61\mu F}\right)^2 + (4m\Omega \times 1.326A)^2} = 8.6mV \tag{34}$$

where

- R_{ESR} is the effective equivalent series resistance (ESR) of the output capacitors.
- 61µF is the total effective (derated) output capacitance.

4. Use Equation 35 to calculate the output capacitor RMS ripple current using and verify that the ripple current is within the capacitor ripple current rating.

$$I_{CO(RMS)} = \frac{\Delta I_{LO}}{\sqrt{12}} = \frac{1.326A}{\sqrt{12}} = 0.383A \tag{35}$$

9.2.1.2.5 Input Capacitors

A power supply input typically has a relatively high source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the input ripple voltage.

1. Select the input capacitors with sufficient voltage and RMS ripple current ratings.
2. Use Equation 36 to calculate the input capacitor RMS ripple current assuming a worst-case duty-cycle operating point of 50%.

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{D \times (1-D)} = 3A \times \sqrt{0.5 \times (1-0.5)} = 1.5A \quad (36)$$

3. Use Equation 37 to find the required input capacitance.

$$C_{IN} \geq \frac{D \times (1-D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} = \frac{0.5 \times (1-0.5) \times 3A}{400kHz \times (480mV - 2m\Omega \times 3A)} = 3.9\mu F \quad (37)$$

   where

   - ΔV_{IN} is the input peak-to-peak ripple voltage specification.
   - R_{ESR} is the input capacitor ESR.
4. Recognizing the voltage coefficient of ceramic capacitors, select four 4.7µF, 100V, X7S, 1210 ceramic input capacitors. Place these capacitors adjacent to the VIN and PGND pins.
5. Use a 100nF, 100V, X7R, 0603 ceramic capacitor near the VIN and PGND pins to supply the high di/dt current during MOSFET switching transitions. Such capacitors offer high self-resonant frequency (SRF) and low effective impedance above 100MHz. The result is lower power loop parasitic inductance, thus minimizing switch-node voltage overshoot and ringing for lower conducted and radiated EMI signature. Refer to *Section 9.4.1* for more detail.

9.2.1.2.6 Compensation Components

Select compensation components for a stable control loop using the procedure outlined as follows.

1. Based on a specified loop gain crossover frequency, f_C, of 30kHz, use Equation 38 to calculate R_{COMP}, assuming an effective output capacitance of 61µF. Select a standard value for R_{COMP} of 18.2kΩ. V_{REF} is $V_{OUT}/10$ if V_{STEP} is 10mV. V_{REF} is $V_{OUT}/20$ if V_{STEP} is 20mV.

$$R_{COMP} = 2 \times \pi \times f_C \times \frac{V_{OUT}}{V_{REF}} \times \frac{R_S \times G_{CS}}{gm} \times C_{OUT} = 2 \times \pi \times 30kHz \times \frac{20V}{1V} \times \frac{8m\Omega \times 10}{1000\mu S} \times 61\mu F = 18.4k\Omega \quad (38)$$

2. To provide adequate phase boost at crossover while also allowing a fast settling time during a load or line transient, select C_{COMP} to place a zero at the higher of (1) one tenth of the crossover frequency, or (2) the load pole. Select a standard value for C_{COMP} of 2.7nF.

$$C_{COMP} = \frac{10}{2 \times \pi \times f_C \times R_{COMP}} = \frac{10}{2 \times \pi \times 30kHz \times 18.4k\Omega} = 2.9nF \quad (39)$$

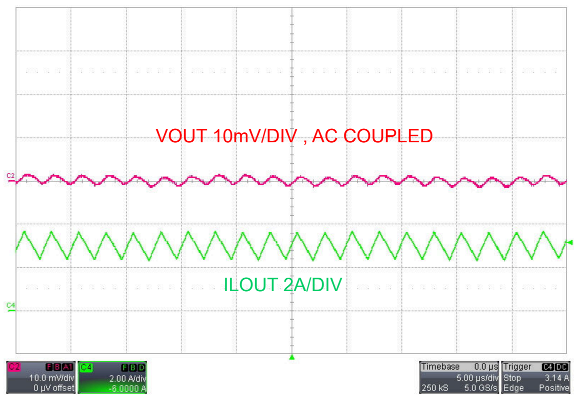
3. Calculate C_{HF} to create a pole at the ESR zero and to attenuate high-frequency noise on the COMP pin. C_{BW} is the bandwidth-limiting capacitance of the error amplifier. A negative C_{HF} can be ignored in this design. However, in noisy environments, especially at high V_{IN} and high load currents, additional capacitance can help filter out the noise.

$$C_{HF} = \frac{1}{2 \times \pi \times f_{ESR} \times R_{COMP}} - C_{BW} = \frac{1}{2 \times \pi \times 650kHz \times 18.4k\Omega} - 15pF = -2pF \quad (40)$$

Note

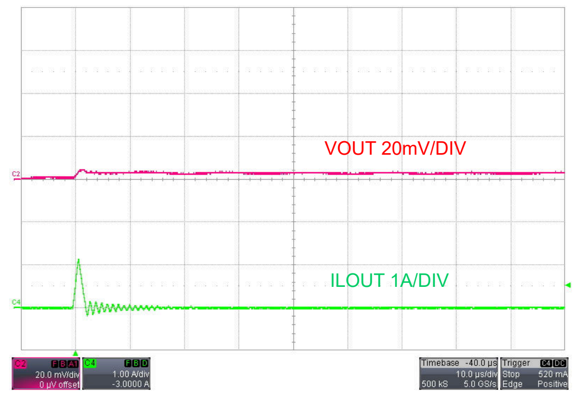
Set a fast loop with high R_{COMP} and low C_{COMP} values to improve the response when recovering from operation in dropout.

9.2.1.3 Application Curves



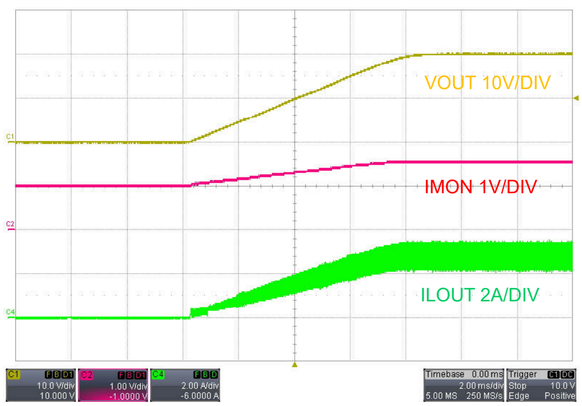
20V Output, 3A Load

Figure 9-7. V_{OUT} Ripple



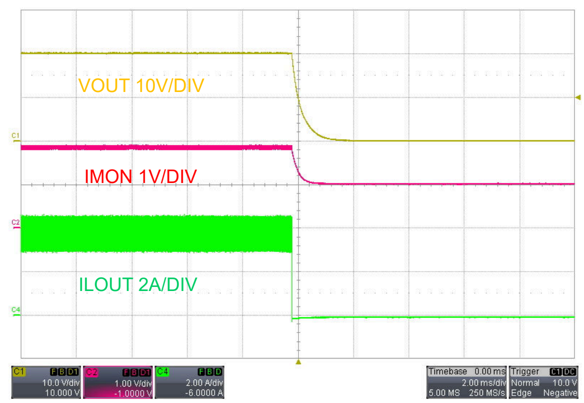
No load

Figure 9-8. PFM Switching



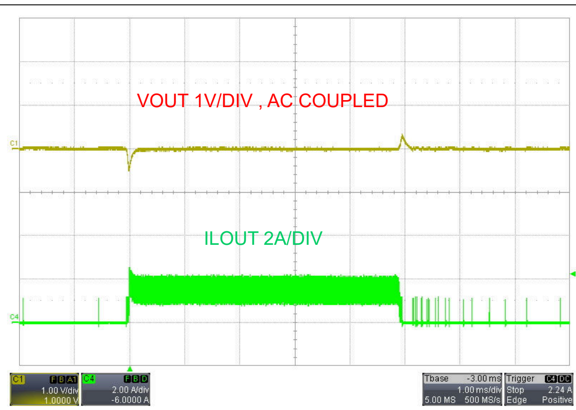
V_{IN} = 48V 3A Resistive Load

Figure 9-9. Start-Up



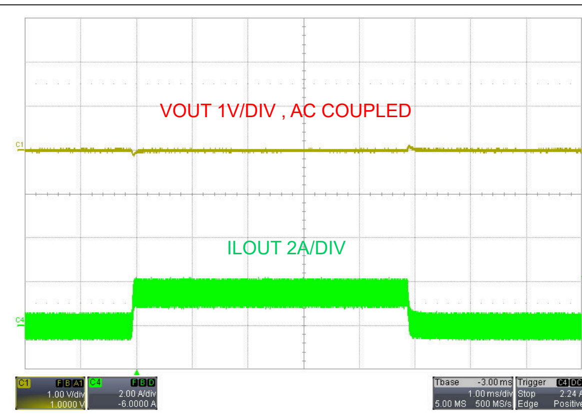
V_{IN} = 48V 3A Resistive Load

Figure 9-10. Shutdown



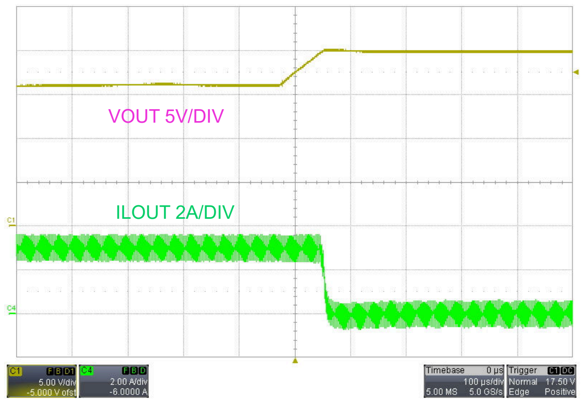
V_{IN} = 48V 0A to 1.5A

Figure 9-11. Load Transient (PFM)



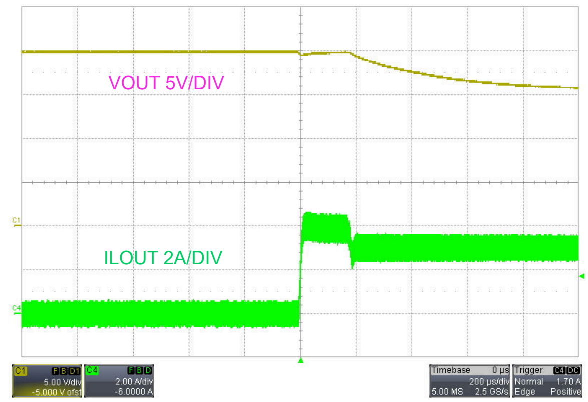
V_{IN} = 48V 0A to 1.5A

Figure 9-12. Load Transient (FPWM)



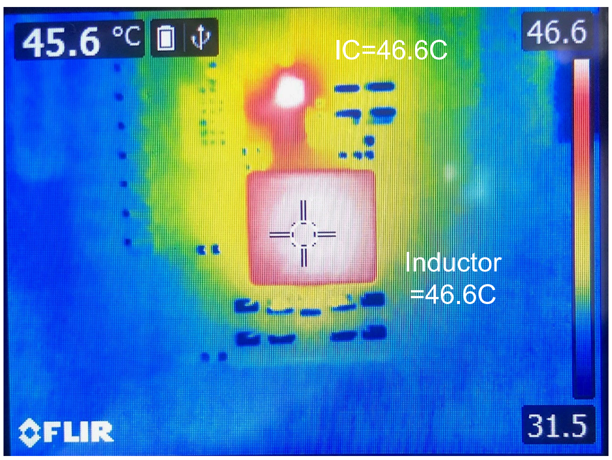
V_{IN} = 48V 5Ω load to no-load

Figure 9-13. CC Mode to CV Mode Transition



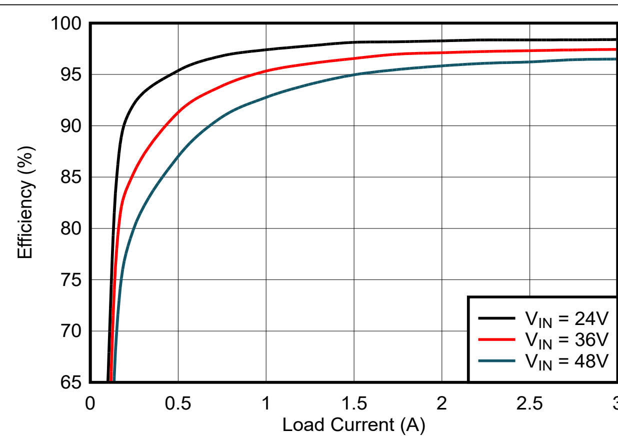
V_{IN} = 48V No-load to 5Ω load

Figure 9-14. CV Mode to CC Mode Transition



V_{IN} = 48V 3A Resistive Load

Figure 9-15. Temperature



V_{OUT} = 20V f_{SW} = 400kHz, FPWM

Figure 9-16. Efficiency vs I_{OUT}

9.3 Power Supply Recommendations

The device is designed to operate over a wide input voltage range. The input supply must be capable of delivering the required input current to the fully-loaded regulator over the input voltage range. Use the following equation to estimate the average input current.

$$I_{IN} = \frac{P_{OUT}}{V_{IN} \times \eta} \quad (41)$$

where

η is the efficiency.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10µF to 47µF is usually sufficient to provide parallel input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The *AN-2162 Simple Success With Conducted EMI From DCDC Converters* application note provides helpful suggestions when designing an input filter for any switching regulator.

9.4 Layout

9.4.1 Layout Guidelines

Proper PCB design and layout is important in high-current, fast-switching converter circuits (with high current and voltage slew rates) to achieve reliable device operation and design robustness. Furthermore, the EMI performance of the converter depends to a large extent on PCB layout.

The high-frequency power loop of a buck regulator power stage is denoted in red in Figure 9-17. The topological architecture of a buck regulator means that particularly high di/dt current flows in the components of the shaded loop, and reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory (Figure 9-17).

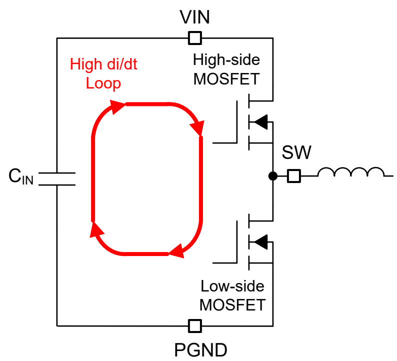


Figure 9-17. Input Current Loop

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC converter performance, including thermals and EMI signature. Figure 9-18 shows a recommended layout of the device with optimized placement and routing of the power-stage and small-signal components.

- *Place the ceramic input capacitors as close as possible to the input power pins*: The VIN and PGND pins are close together (with a gap in between to increase clearance), thus simplifying input capacitor placement.
  – Use low-ESR ceramic capacitors with X7R or X7S dielectric from VIN to PGND. Place an 0402 or 0603 capacitor close to VIN for high-frequency bypass as shown in Figure 9-18. Use additional 1206 or 1210 capacitors for bulk capacitance.
  – Ground return paths for both the input and output capacitors must consist of localized top-side planes that connect to the PGND pins.
- *Use a solid ground plane on the PCB layer beneath the top layer with the IC*: This plane acts as a noise shield and a heat dissipation path. Using the PCB layer directly below the IC minimizes the magnetic field associated with the currents in the switching loops, thus reducing parasitic inductance and switch voltage overshoot and ringing. Use numerous thermal vias near VIN and PGND for heatsinking to the inner copper planes.
- *Make the VIN, VOUT, and GND bus connections as wide as possible*: These paths must be wide and direct as possible to reduce any voltage drops on the input or output paths of the converter, thus maximizing efficiency.
- *Locate the buck inductor close to the SW1, SW2, and SW3 pins*: Use a short, wide connection trace from the converter SW pins to the inductor. At the same time, minimize the length (and area) of this high-dv/dt surface to help reduce capacitive coupling and radiated EMI. Connect the dotted terminal of the inductor to the SW pins.

- *Place the VCC and BOOT capacitors close to the respective pins*: The VCC and BOOT capacitors represent the supplies for the internal low-side and high-side MOSFET gate drivers, respectively, and thus carry high-frequency currents. Locate C_{VCC} close to the VCC pin and place a GND via at the return terminal to connect to the GND plane and thus back to IC GND at the exposed pad. Connect C_{BOOT} close to the CBOOT and SW4 pins.
- *Provide enough PCB area for proper heatsinking*: Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. Provide adequate heatsinking for the device to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad (GND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes. Make the top and bottom PCB layers preferably with two-ounce copper thickness (and no less than one ounce). Use Pb-free solder.

9.4.1.1 Thermal Design and Layout

For a DC/DC converter to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The device is available in a small 6mm × 6mm 29-pin VQFN integrated circuit package to cover a range of application requirements.

Numerous vias connected from the thermal pads to the internal and solder-side plane or planes are vital to help power dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this action provide a plane for the power stage currents to flow but this action also represents a thermally conductive path away from the heat generating devices.

9.4.2 Layout Example

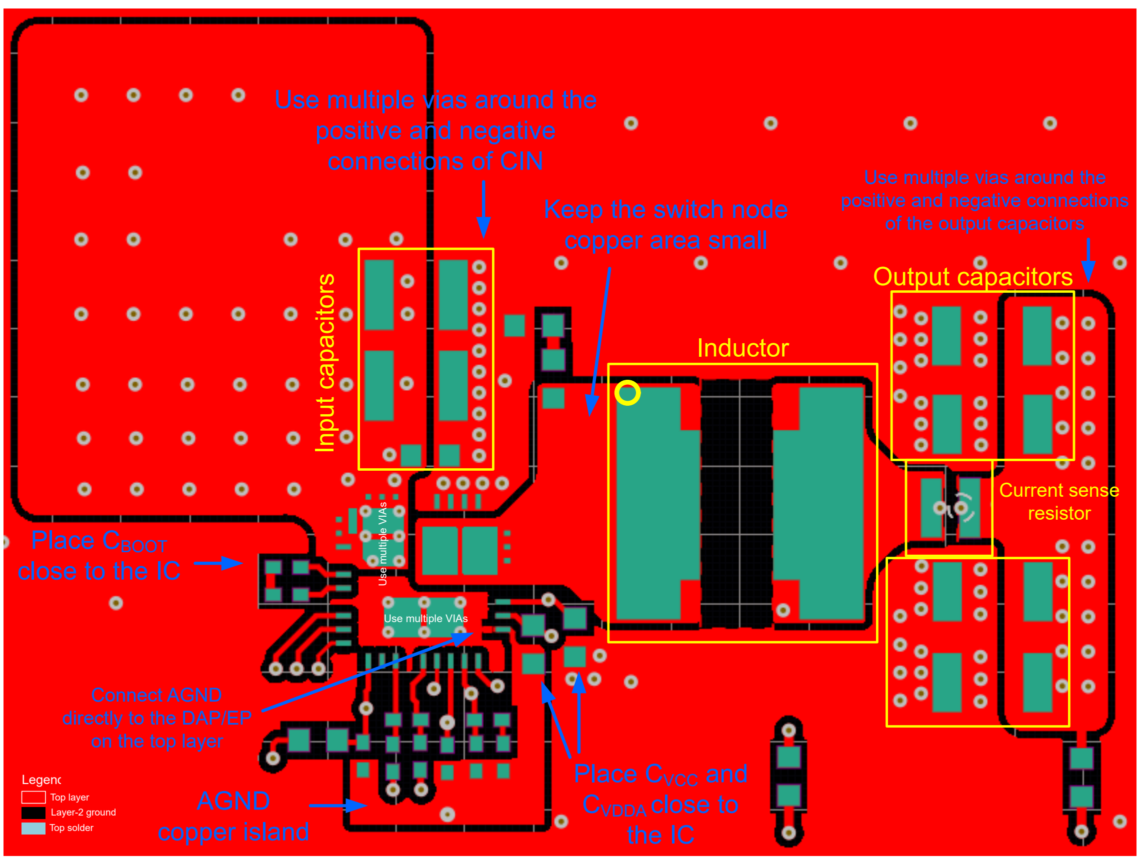


Figure 9-18. PCB Top Layer

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

For development support, see the following:

- LM72XX0-Q1 Quickstart Calculator
- For TI's reference design library, visit TI Designs
- For TI's WEBENCH Design Environment, visit the WEBENCH® Design Center
- TI designs:
  – *Automotive EMI and Thermally Optimized Synchronous Buck Converter Reference Design*
  – *Automotive High Current, Wide V_{IN} Synchronous Buck Controller Reference Design Featuring LM5141-Q1*
  – *25W Automotive Start-Stop Reference Design Operating at 2.2 MHz*
  – *Synchronous Buck Converter for Automotive Cluster Reference Design*
  – *137W Holdup Converter for Storage Server Reference Design*
  – *Automotive Synchronous Buck With 3.3V @ 12.0A Reference Design*
  – *Automotive Synchronous Buck Reference Design*
  – *Wide Input Synchronous Buck Converter Reference Design With Frequency Spread Spectrum*
  – *Automotive Wide V_{IN} Front-end Reference Design for Digital Cockpit Processing Units*
- Technical articles:
  – *High-Density PCB Layout of DC/DC Converters*
  – *Synchronous Buck Controller Solutions Support Wide V_{IN} Performance and Flexibility*
  – *How to Use Slew Rate for EMI Control*

10.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM72630-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- Application notes:
  – Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout Application Report*
  – Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*
  – Texas Instruments, *Maintaining Output Voltage Regulation During Automotive Cold-Crank with LM5140-Q1 Dual Synchronous Buck Controller*
- Analog design journal:
  – Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics*

- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

10.2.1.1 PCB Layout Resources

- Application notes:
  - Texas Instruments, *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout*
  - Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies*
  - Texas Instruments, *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines*
  - Texas Instruments, *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*
- Seminars:
  - Texas Instruments, *Constructing Your Power Supply – Layout Considerations*

10.2.1.2 Thermal Design Resources

- Application notes:
  - Texas Instruments, *AN-2020 Thermal Design by Insight, Not Hindsight*
  - *AN-1520A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - Texas Instruments, *Semiconductor and IC Package Thermal Metrics*
  - Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602*
  - Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
  - Texas Instruments, *PowerPAD Made Easy*
  - Texas Instruments, *Using New Thermal Metrics*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

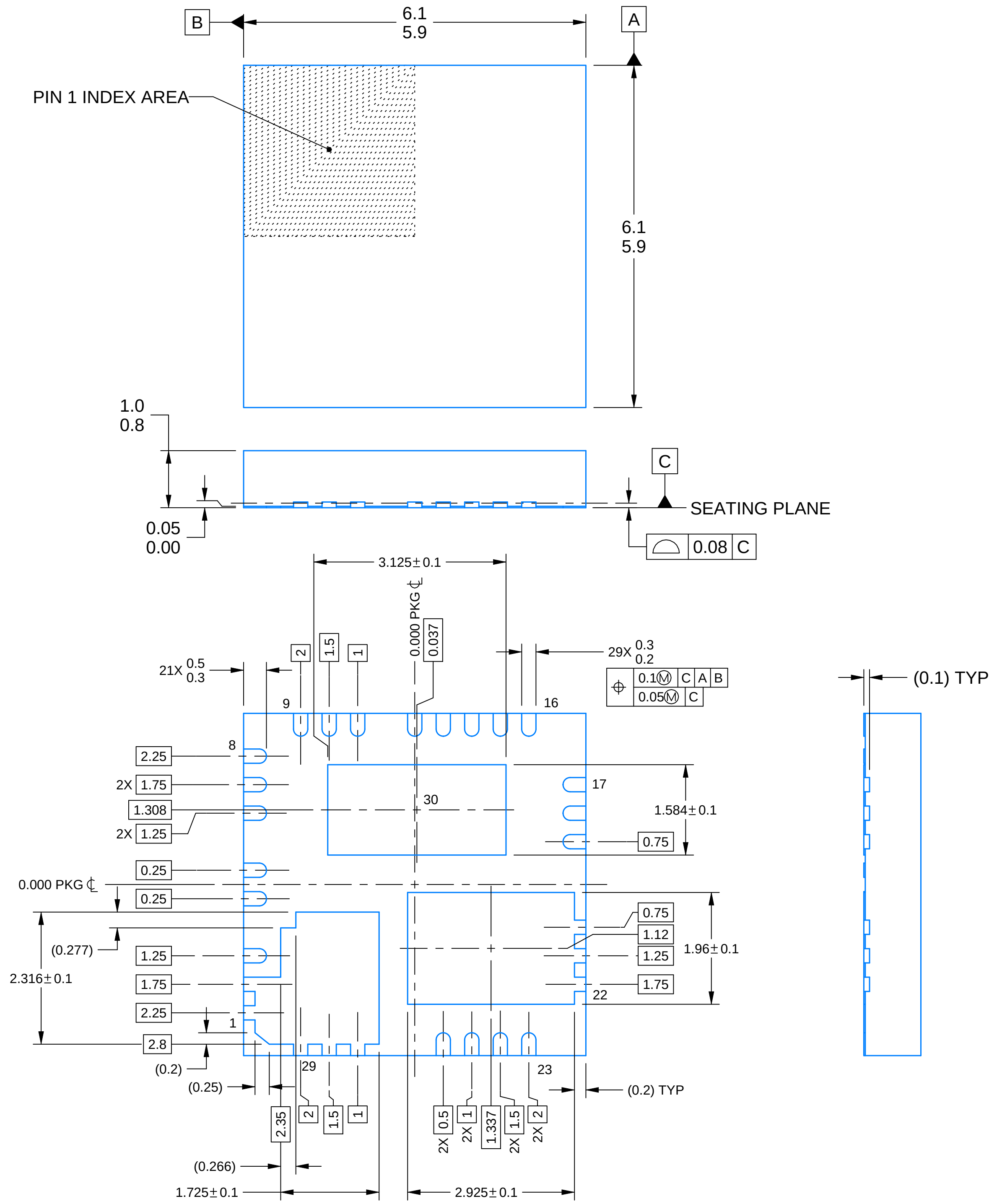
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

DATE	REVISION	NOTES
July 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

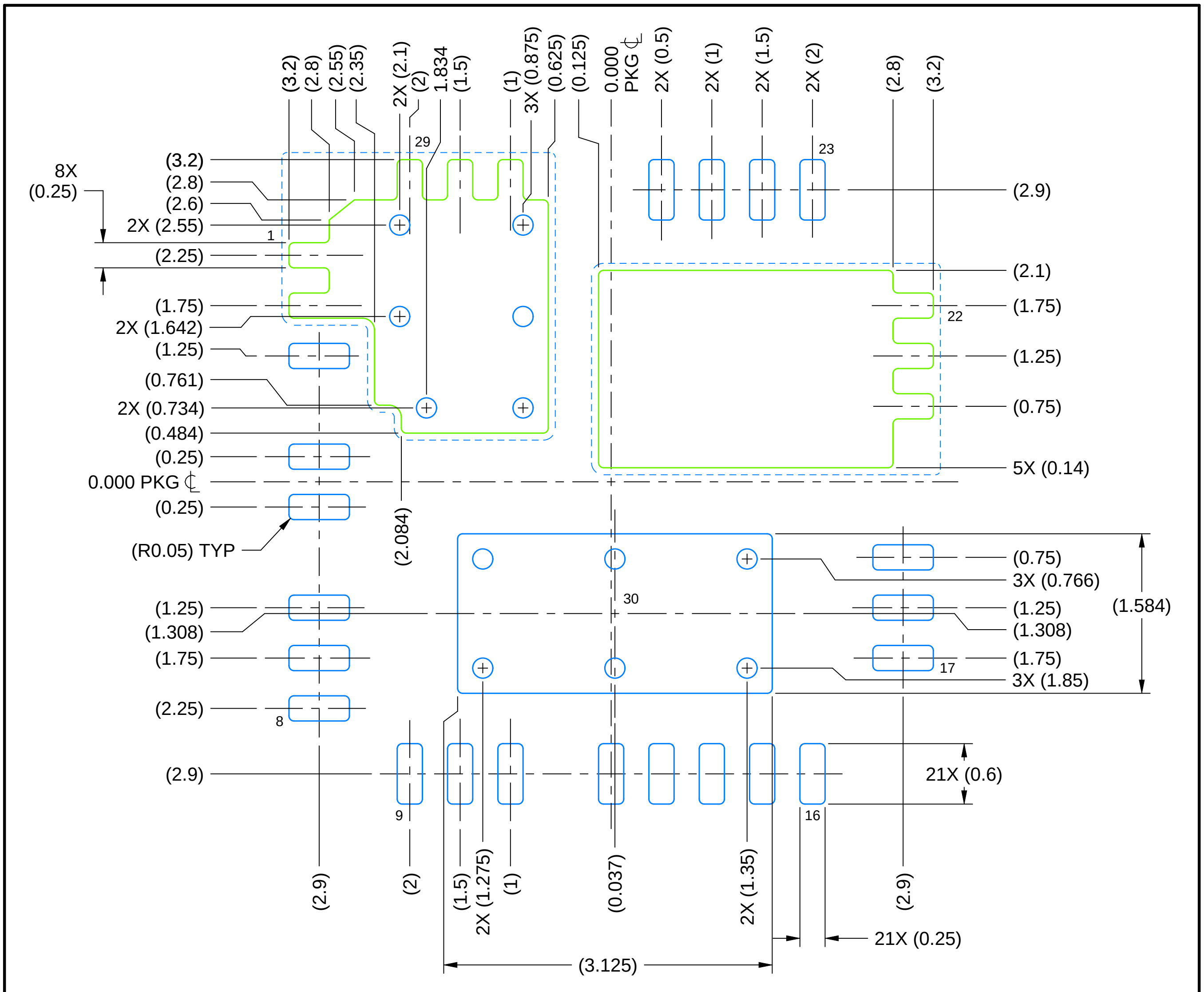
The following pages show mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



4228757/D 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON SOLDER MASK DEFINED (PREFERRED)

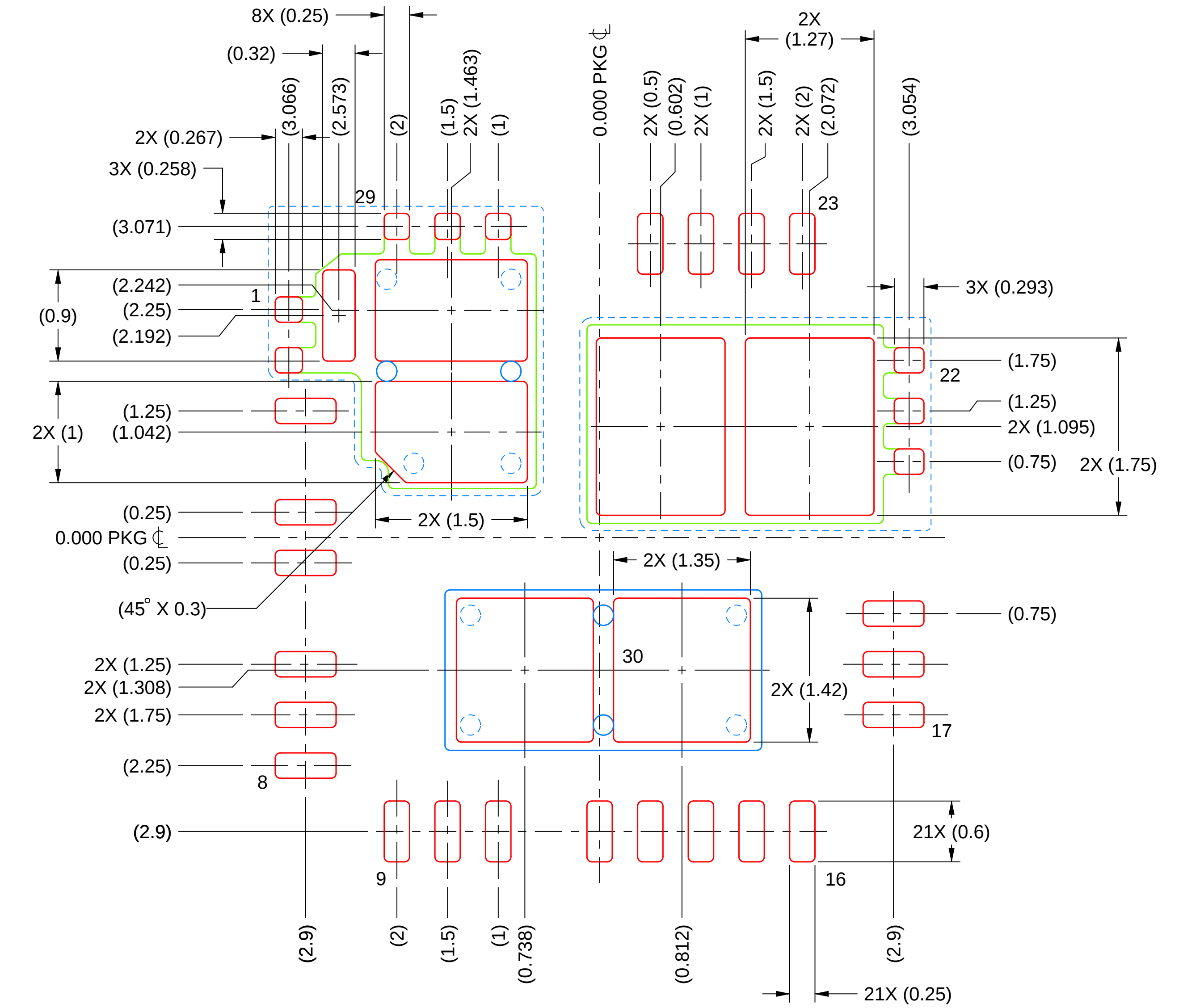
SOLDER MASK DETAILS

SOLDER MASK DEFINED

4228757/D 04/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

4228757/D 04/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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