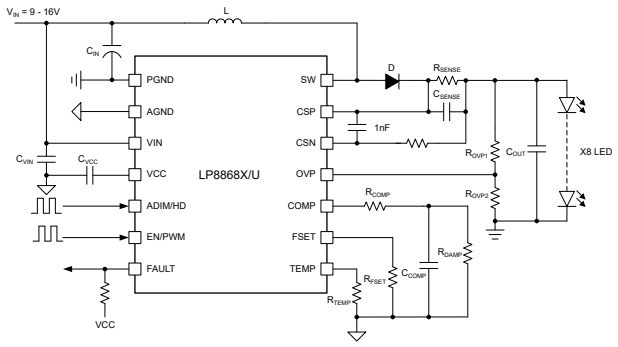
LP8868-Q1 Automotive Multi-Topology LED Driver with Inductive Fast Dimming

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Integrated MOSFET for buck, buck-boost and boost topology
  - Wide input voltage: 4.5V to 65V
  - Integrated 5.2A and 150mΩ MOSFET
  - Switching frequency 100kHz to 2.2MHz
  - Spread spectrum for lower EMI
- High precision power FET dimming
  - Up to 4A output current in buck topology
  - Analog dimming (dimming ratio 256 :1)
  - Fast PWM dimming (150ns pulse width)
  - Hybrid and flexible dimming
- Full protection features:
  - Fault output
  - LED open and short protection
  - Cycle-by-cycle current limit
  - Switching FET failure protection
  - Thermal shutdown
  - Configurable thermal foldback curve

2 Applications

- Automotive infotainment
- Automotive instrument clusters
- Heads-up displays(HUD)
- Automotive lighting



Typical Boost LED Driver Application Schematic

3 Description

The LP8868-Q1 family is a non-synchronous multi-topology solution with 4.5V to 65V wide input range. By integrating the low-side NMOS switch, the device is capable of driving LEDs with high power density and high efficiency. The family also supports common cathode connection and single layer PCB design. The switching frequency is configurable from 100kHz to 2.2MHz with an optional spread spectrum feature for better EMI performance.

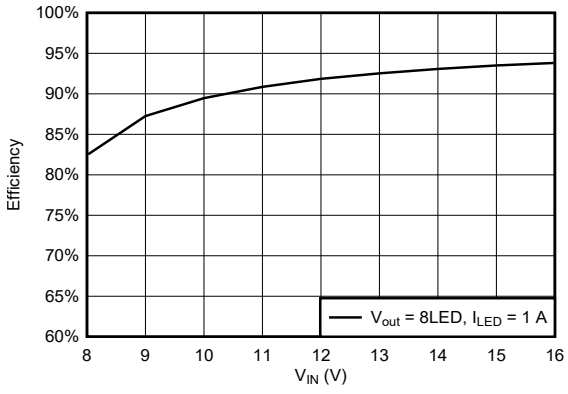
The LP8868-Q1 family supports four dimming options, including analog, PWM, hybrid and flexible dimming. Each dimming method can be configured through the PWM and ADIM input pins by means of simple high and low signals. The family adopts an adaptive off-time current mode control along with smart and accurate sampling to enable inductive fast dimming (IFD) and achieve high dimming accuracy.

The LP8868-Q1 family also provides multiple systematic protections, including LED open and short, sense resistor open and short, configurable thermal foldback and thermal shutdown. Fault output will send out acknowledge signals as soon as any fault condition is detected.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LP8868-Q1	VSON (14)	4.5mm x 3mm
	HVSSOP (12)	4mm x 4.9mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency VS Input Voltage

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4 Comparison Table

Part Number	Topology	MOSFET Current Limit (Typical)	Spread Spectrum	Package
LP8868XQDMTRQ1	Boost	6A	Enabled	VSON
LP8868YQDMTRQ1	Buck-boost	6A	Enabled	VSON
LP8868ZQDMTRQ1	Buck	6A	Enabled	VSON
LP8868UQDMTRQ1	Boost	6A	Disabled	VSON
LP8868VQDMTRQ1	Buck-boost	6A	Disabled	VSON
LP8868WQDMTRQ1	Buck	6A	Disabled	VSON
LP8868XQDGNRQ1	Boost	6A	Enabled	HVSSOP
LP8868YQDGNRQ1	Buck-boost	6A	Enabled	HVSSOP
LP8868ZQDGNRQ1	Buck	6A	Enabled	HVSSOP

5 Pin Configuration and Functions

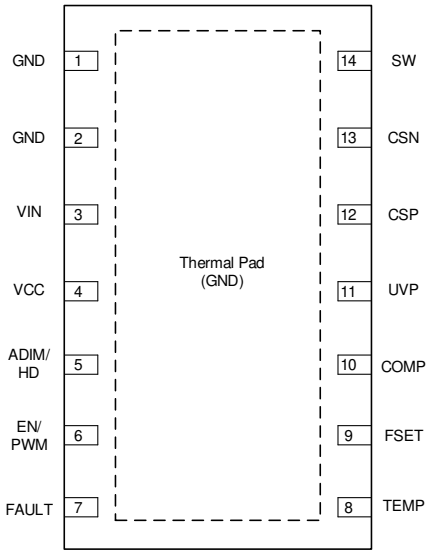


Figure 5-1. 14-Pin Buck VSON (Top View)

Table 5-1. VSON Pin Functions for buck topology

PIN		TYPE[1]	DESCRIPTION
No.	NAME		
1	PGND	G	Power ground pin.
2	AGND	G	Analog ground pin.
3	VIN	P	Input power pin.
4	VCC	P	Internal LDO output pin. Connect with a 10V, 1µF capacitor to GND.
5	ADIM/HD	I	Analog dimming or hybrid dimming pin. Pull high for PWM dimming only, pull low for hybrid dimming, input PWM signal for analog dimming.
6	PWM/EN	I	PWM dimming or EN pin. Pull high for always on, pull low for disabling the device, input PWM signal for PWM dimming.
7	FAULT	O	Open drain output. Pull low when fault is detected.
8	TEMP	I/O	Thermal foldback pin. Put different resistor values to GND to set different thermal foldback behavior curves.
9	FSET	I/O	Switching frequency set pin, with range from 100kHz to 2.2MHz. Put different resistor values to GND for different switching frequencies.
10	COMP	I/O	Error-amplifier output. Connect capacitors to GND. Different capacitor values determine different soft start times and bandwidths.
11	UVP	I	Undervoltage detection pin. Put different resistor dividers to set the LED open detection thresholds.
12	CSP	I	LED current sense positive pin.
13	CSN	I	LED current sense negative pin.
14	SW	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the Schottky diode.
Pad	Thermal Pad	G	Power ground pin.

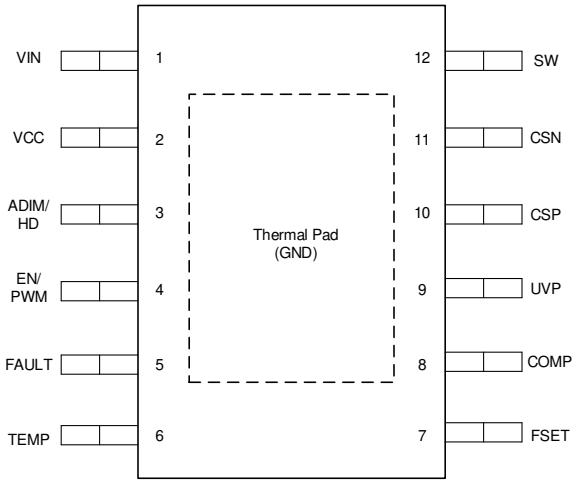


Figure 5-2. 12-Pin Buck HVSSOP (Top View)

Table 5-2. HVSSOP Pin Functions for buck topology

PIN		TYPE(1)	DESCRIPTION
No.	NAME		
1	VIN	P	Input power pin.
2	VCC	P	Internal LDO output pin. Connect with a 10V, 1µF capacitor to GND.
3	ADIM/HD	I	Analog dimming or hybrid dimming pin. Pull high for PWM dimming only, pull low for hybrid dimming, input PWM signal for analog dimming.
4	PWM/EN	I	PWM dimming or EN pin. Pull high for always on, pull low for disabling the device, input PWM signal for PWM dimming.
5	FAULT	O	Open drain output. Pull low when fault is detected.
6	TEMP	I/O	Thermal foldback pin. Put different resistor values to GND to set different thermal foldback behavior curves.
7	FSET	I/O	Switching frequency set pin, with range from 100kHz to 2.2MHz. Put different resistor values to GND for different switching frequencies.
8	COMP	I/O	Error-amplifier output. Connect capacitors to GND. Different capacitor values determine different soft start times and bandwidths.
9	UVP	I	Undervoltage detection pin. Put different resistor dividers to set the LED open detection thresholds.
10	CSP	I	LED current sense positive pin.
11	CSN	I	LED current sense negative pin.
12	SW	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the schottky diode.
Pad	Thermal Pad	G	Power ground pin and analog ground pin

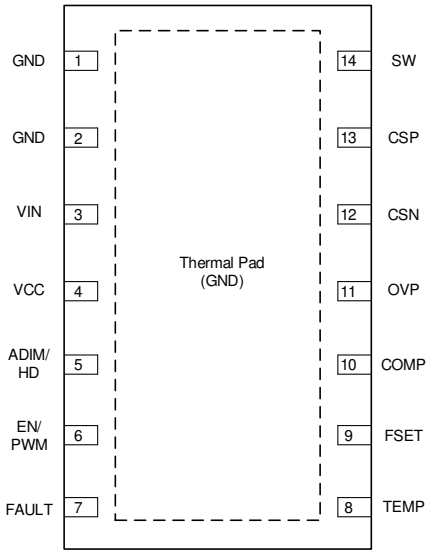


Figure 5-3. 14-Pin Boost/Buck-Boost VSON Top View

Table 5-3. VSON Pin Functions for boost/buck-boost topology

PIN		TYPE(1)	DESCRIPTION
No.	NAME		
1	PGND	G	Power ground pin.
2	AGND	G	Analog ground pin.
3	VIN	P	Input power pin.
4	VCC	P	Internal LDO output pin. Connect with a 10V, 1µF capacitor to GND.
5	ADIM/HD	I	Analog dimming or hybrid dimming pin. Pull high for PWM dimming only, pull low for hybrid dimming, input PWM signal for analog dimming.
6	PWM/EN	I	PWM dimming or EN pin. Pull high for always on, pull low for disabling the device, input PWM signal for PWM dimming.
7	FAULT	O	Open drain output. Pull low when fault is detected.
8	TEMP	I/O	Thermal foldback pin. Put different resistor values to GND to set different thermal foldback behavior curves.
9	FSET	I/O	Switching frequency set pin, with range from 100kHz to 2.2MHz. Put different resistor values to GND for different switching frequencies.
10	COMP	I/O	Error-amplifier output. Connect capacitors to GND. Different capacitor values determine different soft start times and bandwidths.
11	OVP	I	Overvoltage detection pin. Put different resistor dividers to set the LED open detection thresholds.
12	CSN	I	LED current sense negative pin.
13	CSP	I	LED current sense positive pin.
14	SW	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the Schottky diode.
Pad	Thermal Pad	G	Power ground pin.

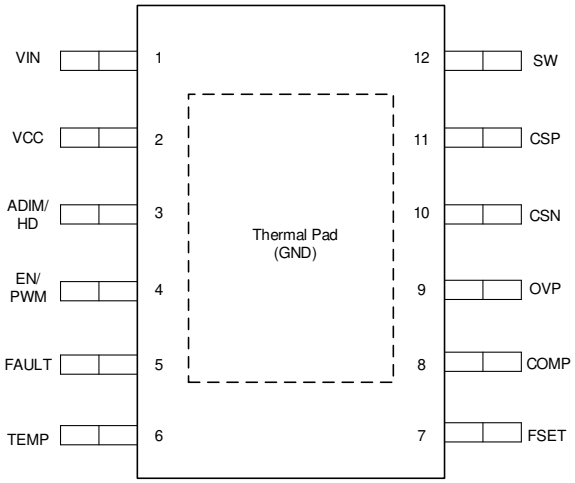


Figure 5-4. 12-Pin Boost/Buck-Boost HVSSOP Top View

Table 5-4. VSON Pin Functions for boost/buck-boost topology

PIN		TYPE(1)	DESCRIPTION
VSON Package	NAME		
1	VIN	P	Input power pin.
2	VCC	P	Internal LDO output pin. Connect with a 10V, 1µF capacitor to GND.
3	ADIM/HD	I	Analog dimming or hybrid dimming pin. Pull high for PWM dimming only, pull low for hybrid dimming, input PWM signal for analog dimming.
4	PWM/EN	I	PWM dimming or EN pin. Pull high for always on, pull low for disabling the device, input PWM signal for PWM dimming.
5	FAULT	O	Open drain output. Pull low when fault is detected.
6	TEMP	I/O	Thermal foldback pin. Put different resistor values to GND to set different thermal foldback behavior curves.
7	FSET	I/O	Switching frequency set pin, with range from 100kHz to 2.2MHz. Put different resistor values to GND for different switching frequencies.
8	COMP	I/O	Error-amplifier output. Connect capacitors to GND. Different capacitor values determine different soft start times and bandwidths.
9	OVP	I	Overvoltage detection pin. Put different resistor dividers to set the LED open detection thresholds.
10	CSN	I	LED current sense negative pin.
11	CSP	I	LED current sense positive pin.
12	SW	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the Schottky diode.
Pad	Thermal Pad	G	Power ground pin and analog ground pin

(1) I = Input, O = Output, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	VIN, UVP, OVP, CSP, CSN, SW,	–0.3	65	V
Voltage on pins	VCC, ADIM/HD, EN/PWM, FAULT, TEMP, FSET, COMP	–0.3	5.5	V
Operation junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN	4.5	63	V
Input voltage range	UVP, OVP, CSP, CSN	0	63	V
Input voltage range	VCC, ADIM/HD, EN/PWM, TEMP, FSET	0	5	V
Output voltage range	SW	0	63	V
	FAULT, COMP	0	5	V
Operating junction temperature, T_J		–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		Device		UNIT
		HVSSOP	SON	
		12 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.3	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.2	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.9	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.9	14.7	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_A = –40°C to +125°C, V_{IN} = 4.5 V to 60 V, (unlessotherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN_UVLO}	V_{IN} undervoltage lockout	Rising V_{IN}	3.0	3.2	3.4	V
		Falling V_{IN}	2.8	3.0	3.2	V
	Hysteresis			0.2		V
I_{SD}	Shut down current from V_{IN}	V_{IN} = 12 V, $V_{EN/PWM}$ = 0 V		0.8	2.3	µA
I_{OFF}	PWM off current from V_{IN}	V_{IN} = 12 V, $V_{EN/PWM}$ = 0 V		2.5		mA
I_{OP}	Normal operating current	400-kHz switching frequency		4.6		mA
I_{OP}	Normal operating current	2.2-MHz switching frequency		10.0		mA
V_{VCC}	Internal LDO output voltage	I_{VCC} = 10mA	5.0	5.15	5.3	V
I_{VCC_LIM}	Internal LDO output current limit		38	47	56	mA
DIMMING						
V_{PWM_L}	Low-level input voltage				0.4	V
V_{PWM_H}	High-level input voltage		1.2			V
V_{ADIM_L}	Low-level input voltage				0.4	V
V_{ADIM_H}	High-level input voltage		1.2			V
$t_{PWM\_OUT\_ON}$	PWM output minimum on time				150	ns
$t_{PWM\_IN\_ON}$	PWM input minimum on time				150	ns
$t_{PWM\_IN\_OFF}$	PWM input minimum off time to disable device		57		77	ms
f_{ADIM}	Analog Dimming input frequency	6-bit ADIM resolution	0.1		156	kHz
f_{ADIM}	Analog Dimming input frequency	8-bit ADIM resolution	0.1		39	kHz
FAULT						
V_{OL}	Output level low	I = 3mA			0.1	V
$I_{LEAKAGE}$	Output leakage current	V = 5 V			1	µA
FEEDBACK AND ERROR AMPLIFIER						
$g_{M(ea)}$	Transconductance gain	ADIM 100% duty cycle, $V_{CSP-CSN}$ = 200mV, V_{COMP} = 1.5V	205	265	325	µA/V
I_{COMP}	Source/sink current	ADIM 100% duty cycle, $V_{CSP-CSN}$ = 200mV ± 200mV, V_{COMP} = 1.5V	±24	±40	±56	µA
$V_{CSP-CSN}$	Current sense threshold	ADIM 100% duty cycle	194	200	206	mV
$V_{CSP-CSN}$	Current sense threshold	ADIM 12.5% duty cycle, compared with 100% duty cycle	11.875	12.5	13.125	%
$V_{CSP-CSN}$	Current sense threshold	ADIM 1.17% duty cycle, compared with 100% duty cycle	0.82	1.17	1.52	%
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current	V_{IN} = 60 V, $V_{EN/PWM}$ = 5 V	22		31	µA
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current	V_{IN} = 60 V, $V_{EN/PWM}$ = 0 V	10		15	µA
POWER STAGE						
R_{DSON}	Switching FET on resistance	V_{IN} ≥ 5 V		150		mΩ
t_{min_ON}	Switching FET minimum on time			100		ns
t_{min_OFF}	Switching FET minimum off time			100		ns
f_{SW}	Switching FET frequency		0.1		2.2	MHz
CURRENT LIMIT						
I_{LIM}	Switching FET cycle-by-cycle current limit (LP8868X/LP8868Y/LP8868U/LP8868V)		5.8	6.5	7.6	A
I_{LIM}	Switching FET cycle-by-cycle current limit (LP8868Z/LP8868W)		5.2	6	7	A
I_{LIM}	Switching FET cycle-by-cycle current limit (LP8868X/LP8868Y/LP8868U/LP8868V) HVSSOP package		5.8	7	7.8	A

6.5 Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_A = –40°C to +125°C, V_{IN} = 4.5 V to 60 V, (unlessotherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIM}	Switching FET cycle-by-cycle current limit (LP8868Z/LP8868W) HVSSOP package		5.2	6.5	7.2	A
THERMAL PROTECTION						
T_{th}	Thermal foldback starting temperature threshold	R_{TEMP} = 20 kΩ		130		°C
T_{TSD}	Thermal shutdown temperature			165		°C
	Hysteresis			15		°C

6.6 Typical Characteristics

V_{IN} = 12V, L = 22 µH, F_{SW} = 400kHz, unless otherwise specified

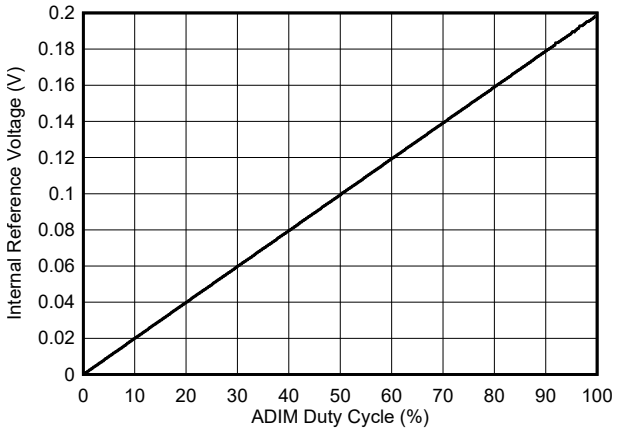


Figure 6-1. ADIM Duty Cycle vs Reference Voltage in Analog Dimming

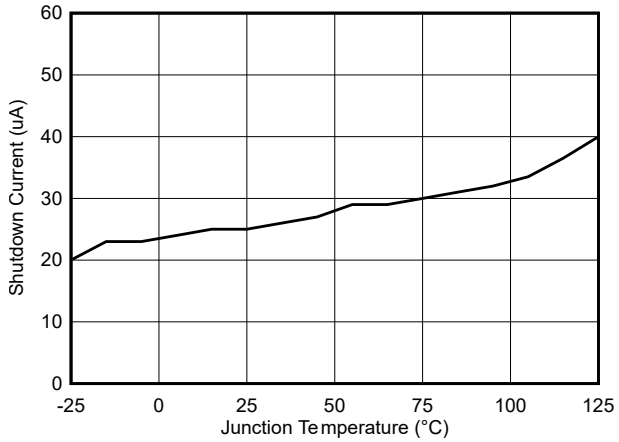


Figure 6-2. Shutdown Current vs Junction Temperature

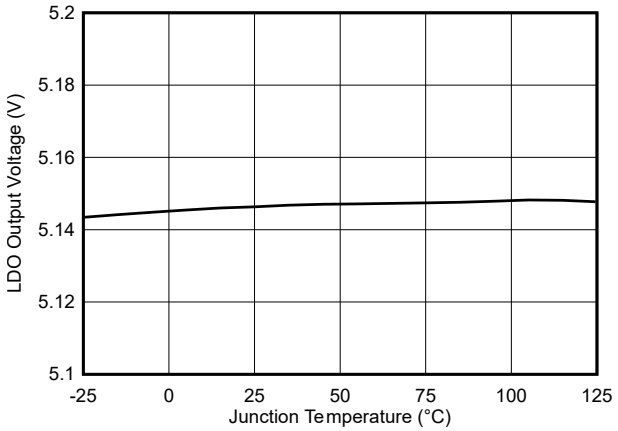


Figure 6-3. Internal LDO Output vs Junction Temperature

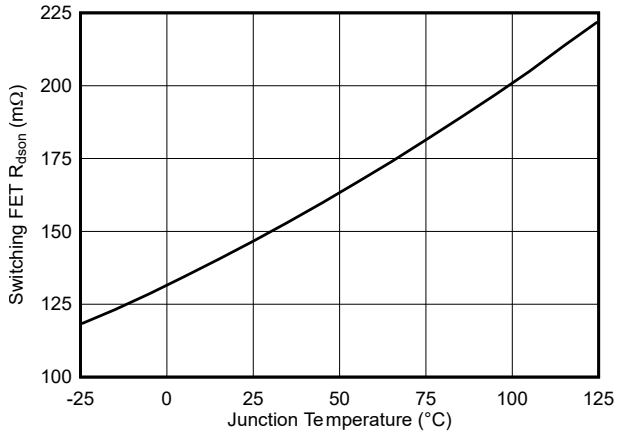


Figure 6-4. Switching FET Rdson vs Junction Temperature

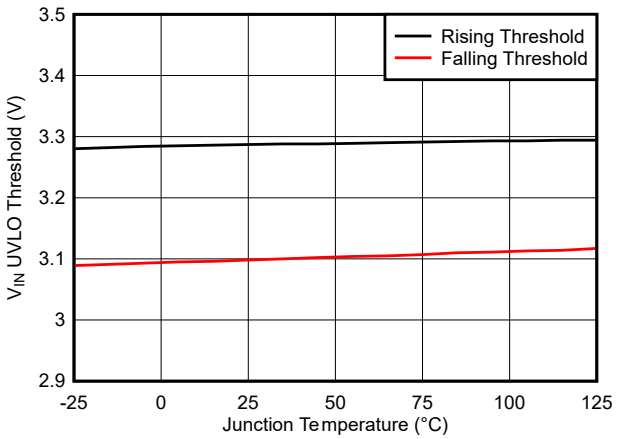


Figure 6-5. VIN UVLO Threshold vs Junction Temperature

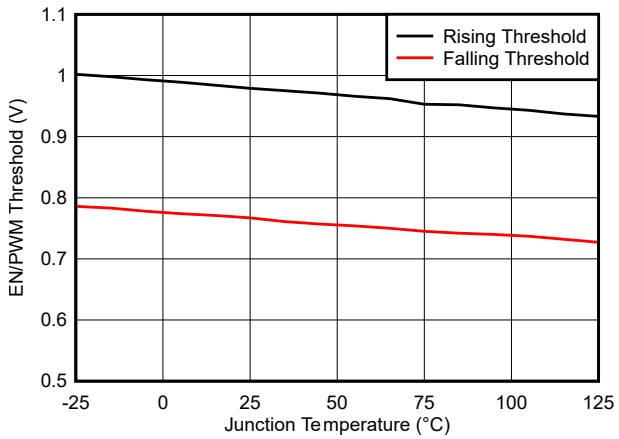


Figure 6-6. EN/PWM Threshold vs Junction Temperature

6.6 Typical Characteristics (continued)

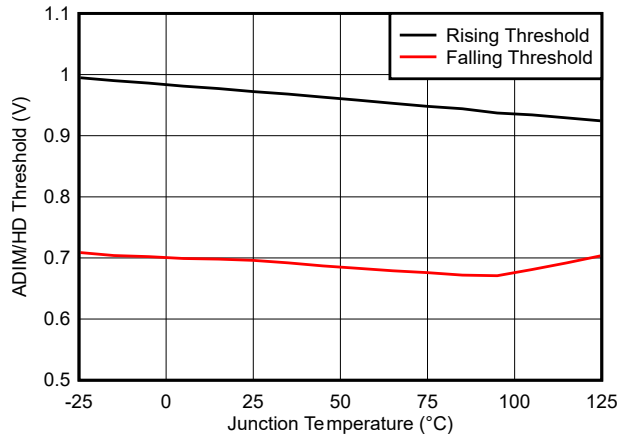


Figure 6-7. ADIM/HD Threshold vs Junction Temperature

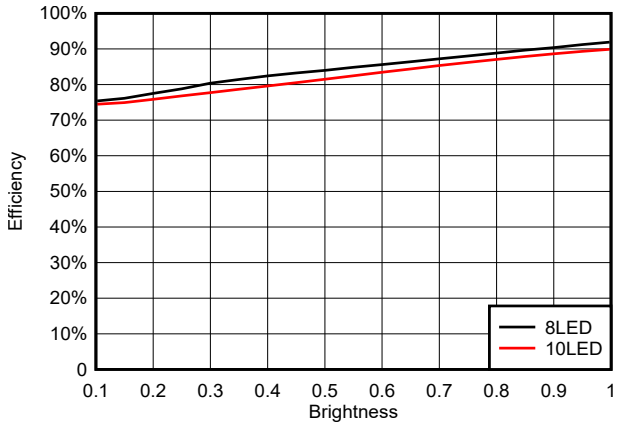


Figure 6-8. Efficiency at 1A Max Output Current with PWM Dimming, 22uH Inductor, Boost Topology

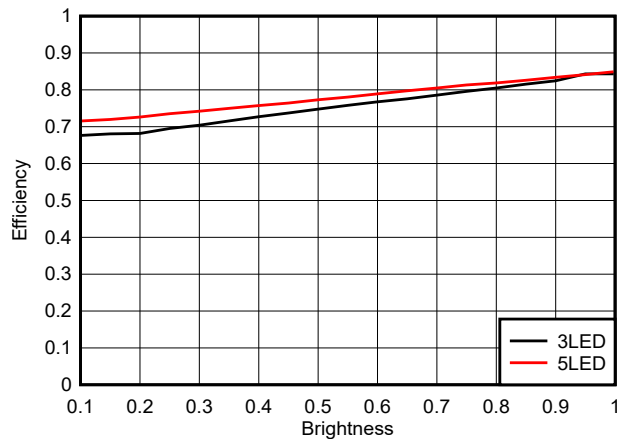


Figure 6-9. Efficiency at 1A Max Output Current with PWM Dimming, 22uH Inductor, Buck-Boost Topology

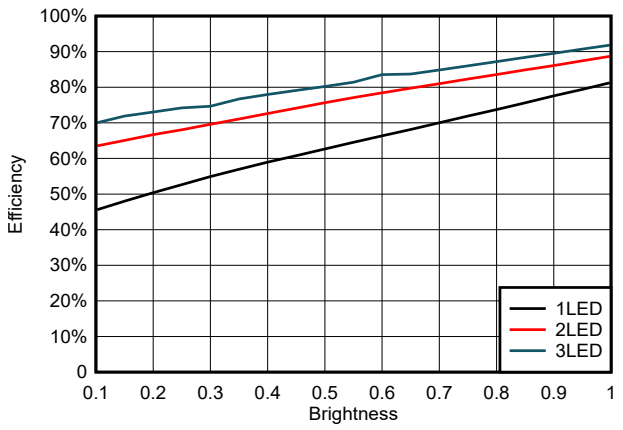


Figure 6-10. Efficiency at 3A Max Output Current with PWM Dimming, 22uH Inductor, Buck Topology

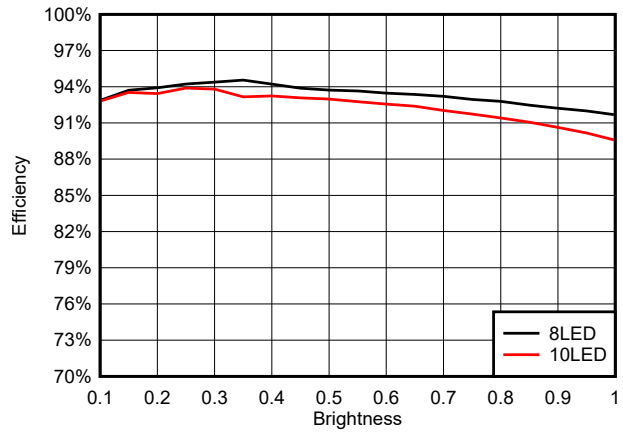


Figure 6-11. Efficiency at 1A Max Output Current with Analogy Dimming, 22uH Inductor, Boost Topology

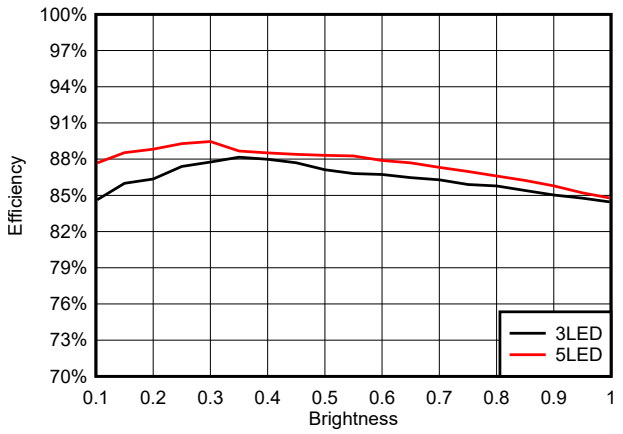


Figure 6-12. Efficiency at 1A Max Output Current with Analogy Dimming, 22uH Inductor, Buck-Boost Topology

6.6 Typical Characteristics (continued)

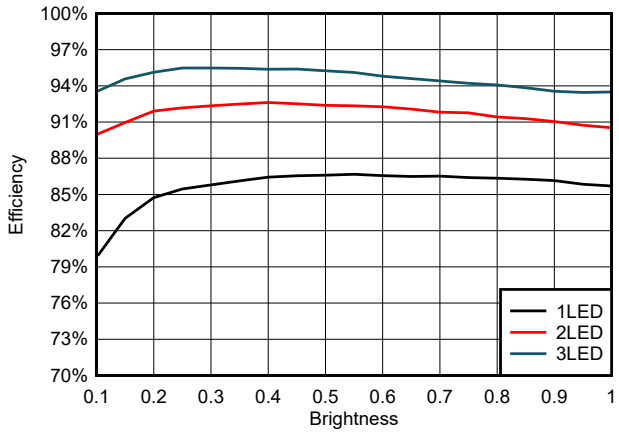


Figure 6-13. Efficiency at 3A Max Output Current with Analogy Dimming, 22uH Inductor, Buck Topology

7 Detailed Description

7.1 Overview

The LP8868-Q1 family is a 4A non-synchronous buck/boost/buck-boost LED drivers with 4.5V to 65V wide input range. By integrating the low-side NMOS switch with constant current and constant voltage controls, the device is capable of driving LEDs and charging batteries with high power density and high efficiency.

The switching frequency is configurable through the FSET pin, ranging from 100kHz to 2.2MHz, with optional spread spectrum feature to decrease the EMC emission and reduce the input filter size. The device supports four dimming options:

- Analog dimming
- PWM dimming
- Hybrid dimming
- Flexible dimming

Each dimming method is configurable through the PWM and ADIM input pins through simple high or low sequencing signals at start-up.

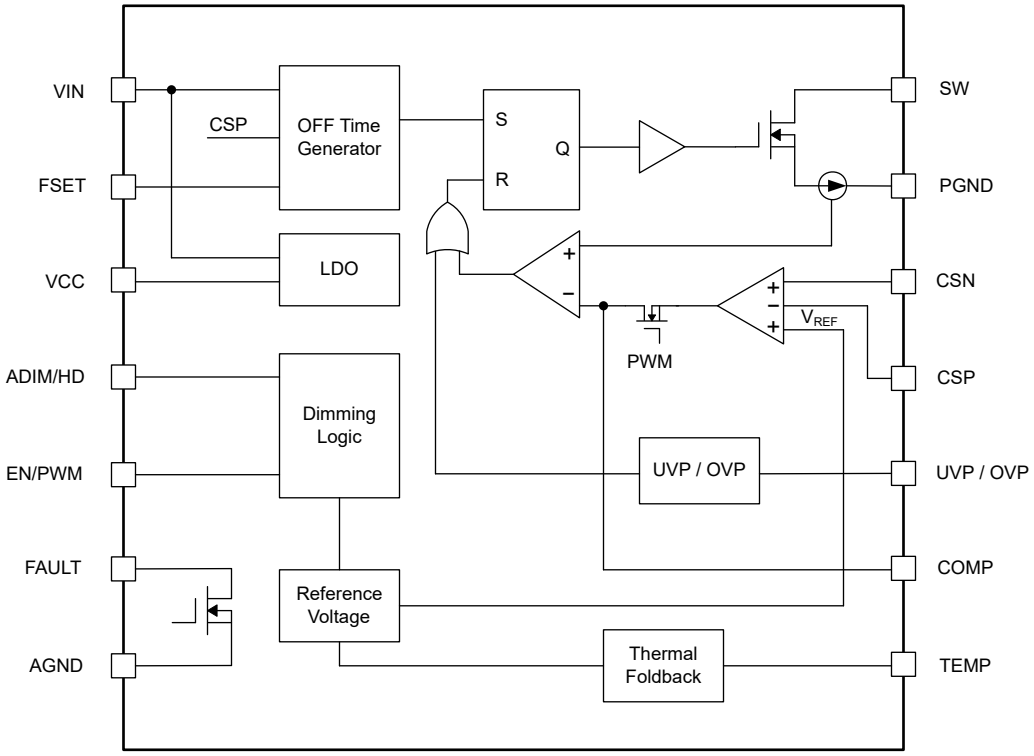
The device adopts an adaptive off-time current-mode control along with smart and accurate sampling to enable inductive fast dimming (IFD) and achieve high dimming ratio. The compensation bandwidth can be adjusted through an external capacitor on COMP pin based on system requirement.

The LP8868-Q1 family has extensive fault detection features:

- LED open and short detection
- Sense resistor open and short detection
- Configurable thermal foldback and thermal shutdown protection

The fault condition is indicated through the FAULT output pin.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive Off-Time Current Mode Control

The LP8868-Q1 family adopts an adaptive off-time current-mode control to support fast transient response over a wide range of operation. The switching frequency is configurable through the FSET pin, ranging from 100kHz to 2.2MHz.

For average output current regulation, the sensed voltage across the sensing resistor between the CSP and CSN pins compares with the internal voltage reference, V_{REF}, through the error amplifier. The output of the error amplifier, V_{COMP}, passes through an external compensation network and compares with the peak current feedback at the PWM comparator

During each switching cycle, when the internal N-MOSFET is turned on, the peak current is sensed through the internal FET. When the sensed value of peak current reaches VCOMP at the input of PWM comparator, the N-MOSFET is turned off and the adaptive off-time counter starts counting. Once the adaptive off-time counter stops counting, the counter remains reset until when the N-MOSFET turns off. The counting off time is determined by the external resistor connected to the FSET pin and the input/output feed forward. Thus, the device maintains a nearly constant switching frequency at steady state and regulate the output average current at a desired value.

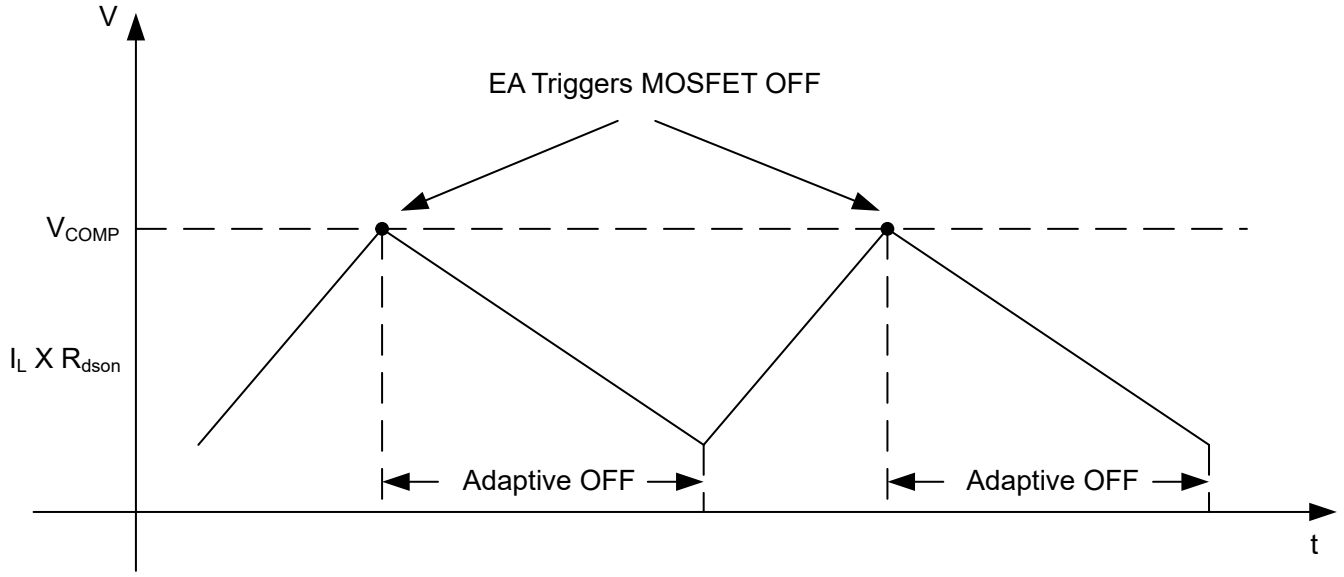


Figure 7-1. Adaptive Off-time Current Mode Control Method

7.3.1.1 Switching Frequency Settings

The switching frequency of LP8868 family is adjustable from 100kHz to 2.2MHz through changing R_{FSET} connected between FSET pin and AGND. The default switching frequency is 100kHz when the FSET pin is connected to nothing.

The resistor value and the corresponding switching frequency are listed in Table 7-1.

Table 7-1. Switching Frequency versus R_{FSET} Resistor Value

Switching Frequency	Resistor Value (kΩ)
100kHz	232
200kHz	138
300kHz	83
400kHz	59
600kHz	38
800kHz	28

Table 7-1. Switching Frequency versus R_{FSET} Resistor Value (continued)

Switching Frequency	Resistor Value (kΩ)
1MHz	23
1.2MHz	18
1.5MHz	13
1.8MHz	11
2.2MHz	9

For example, if R_{FSET} is set to 59kΩ, the corresponding switching frequency is 400kHz.

In most cases, lower switching frequency has a higher system efficiency and better thermal performance.

7.3.1.2 Spread Spectrum

The LP8868X/Y/Z-Q1 enables the spread spectrum feature (±7% from central frequency, 2kHz modulation frequency) which reduces EMI noise at the switching frequency and its harmonic frequencies.

Also, the LP8868U/V/W-Q1 disables the spread spectrum feature toward better brightness performance in low brightness scenario.

7.3.2 Setting LED Current

The output current of the LED is controlled with external resistor R_{sense} between CSP and CSN pins. Calculate the R_{sense} value for the target current using equation Equation 1. To realize the IFD function and improve the accuracy of the output current in low duty cycle, the capacitor in parallel with sense resistor is required for boost and buck-boost topology. The capacitor in parallel with sense resistor is optional for buck topology. To avoid noise injection and increase robustness, a 100Ω resistor is recommended in the CSN pin.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \quad (1)$$

where

- V_{REF} = 200mV
- R_{SENSE} is current setting resistor (mΩ)
- I_{LED} is output current (mA)

For example, if R_{sense} is set to 100mΩ, I_{LED} is calculated as 2A.

7.3.3 Internal Soft Start

The LP8868-Q1 family implements the internal soft-start function. Once V_{IN} rises above V_{VIN_MIN}, the internal LDO starts to charge V_{CC} capacitor. If a 1µF capacitor is connected to the V_{CC} pin, it takes approximately 800µs for V_{CC} to rise above the V_{VIN_UVLO}. If EN/PWM pin is pulled high before V_{CC} rises above V_{VIN_UVLO}, the POR enables directly after V_{CC} is above V_{VIN_UVLO} and waits for 100µs to start dimming mode. EN/PWM pin remains high for more than 5µs after V_{CC} rises above V_{VIN_UVLO}. If using 1µF V_{CC} capacitor, the recommendation is to wait for 1ms prior to starting dimming mode after V_{IN} rises above V_{VIN_MIN}.

If EN/PWM pin has the first PWM pulse appearing after V_{CC} rises above V_{VIN_UVLO}, the device waits for 200µs to enable POR and another 100µs to begin dimming mode. Hence, without triggering V_{IN} UVLO, the device can be re-enabled after disabled and wait for 300µs to start dimming mode. The initial enable PWM pulse lasting more than 5µs is required at EN/PWM input pin to enable the device. After dimming mode is started, the device enters four different dimming modes based on the configuration of ADIM/HD pin and EN/PWM pin.

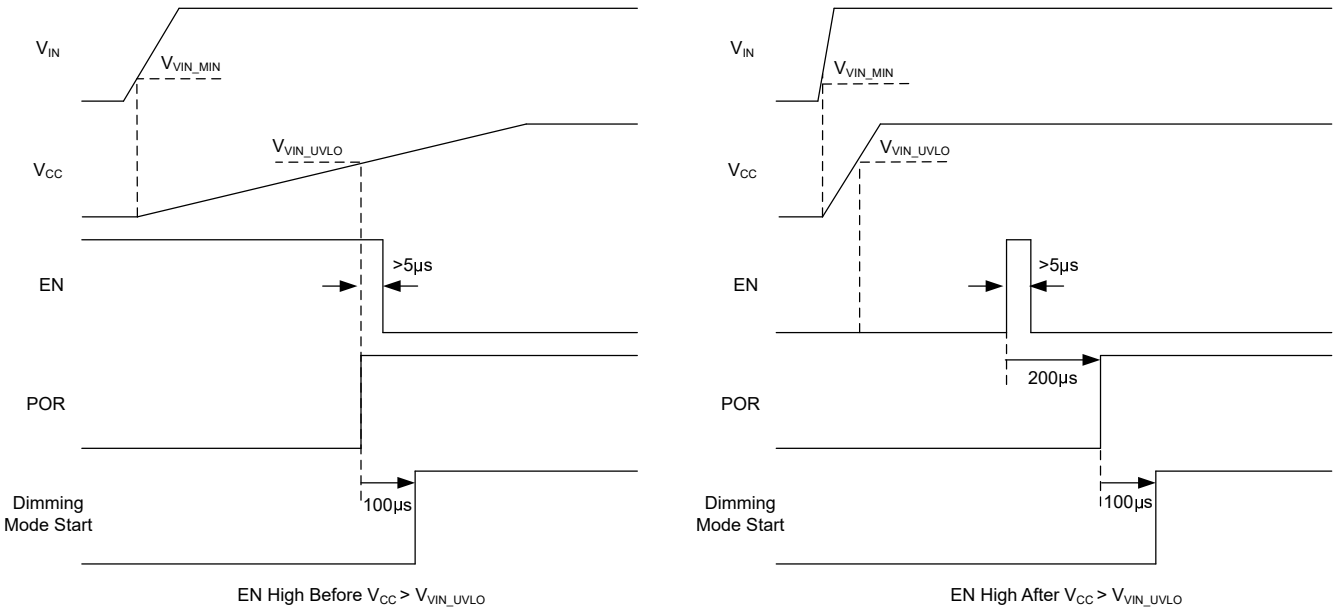


Figure 7-2. Start-up Sequence

7.3.4 Dimming Mode

The LP8868 family has 4 optional dimming modes determined by the waveform in PWM and ADIM pins. The dimming mode is started either 1ms after VIN exits UVLO or 300µs after renable by EN/PWM pin. The configuration to one of the four dimming modes are shown in the table below.

Table 7-2. Dimming Mode Configuration

Dimming Mode	EN/PWM Pin	ADIM/HD Pin
PWM dimming	PWM signal	High
Analog dimming	High	PWM signal
Hybrid dimming	PWM signal	Low
Flexible dimming	PWM signal	PWM signal

7.3.4.1 PWM Dimming

The PWM dimming mode is enabled when the ADIM/HD input pin is always high and the PWM/EN input pin is configured by a PWM input signal. Device supports PWM input signals with ultra-narrow pulse width down to 200ns in PWM dimming mode. The input duty cycle can be changed in the opposite direction only when duty cycle changes by more than 0.38% in hybrid dimming.

In PWM dimming mode, when the PWM input signal at the PWM pin turns from low to high, the internal NMOS FET starts switching and the inductor current rises to the determined value. The LED current is then regulated at the determined value, as long as the PWM input signal remains high. When the PWM input signal turns from high to low, the internal FET is turned off, causing the inductor current to fall to zero. The internal FET remains off and the LED current remains at zero if the PWM input signal stays low.

7.3.4.2 Analog Dimming

The LP8868 family supports analog dimming which regulates the LED current through the ADIM/HD pin. The analog dimming mode is enabled when the PWM/EN pin is always high and the ADIM/HD pin is configured by a PWM input signal. The internal digital circuits respond to the duty cycle change of the PWM input signal within a delay that lasts tens of micro-seconds.

The internal voltage reference, V_{REF}, changes in proportion to the duty cycle of the PWM input signal at the ADIM/HD pin. For example, V_{REF} is 200mV when the PWM input signal at the ADIM/HD pin has a 100% duty cycle. For example, V_{REF} is 20mV when the PWM input signal has a 10% duty cycle.

7.3.4.3 Hybrid Dimming

The LP8868 family supports a unique hybrid dimming function to maximize the dimming performance, especially when both high dimming frequency and high dimming ratio are needed. The hybrid dimming mode is enabled when the ADIM/HD pin is always low and the PWM/EN pin is configured by a PWM input signal.

When the hybrid dimming is enabled, the LED current is regulated by the analog dimming at high brightness level (from 12.5% to 100%) and by the PWM dimming at low brightness level (form 0% to 12.5%). At a high brightness level, the internal voltage reference, V_{REF}, changes in proportion to the duty cycle of the PWM input signal at the PWM/EN pin. At a low brightness level, V_{REF} remains unchanged and an internal PWM generator is enabled. Thus, the LED is turned on and off corresponding to the on and off of the internal PWM signal of which the frequency and the duty cycle are configured by the PWM input signal at the PWM/EN pin. The detailed hybrid dimming behavior is illustrated in the below figure.

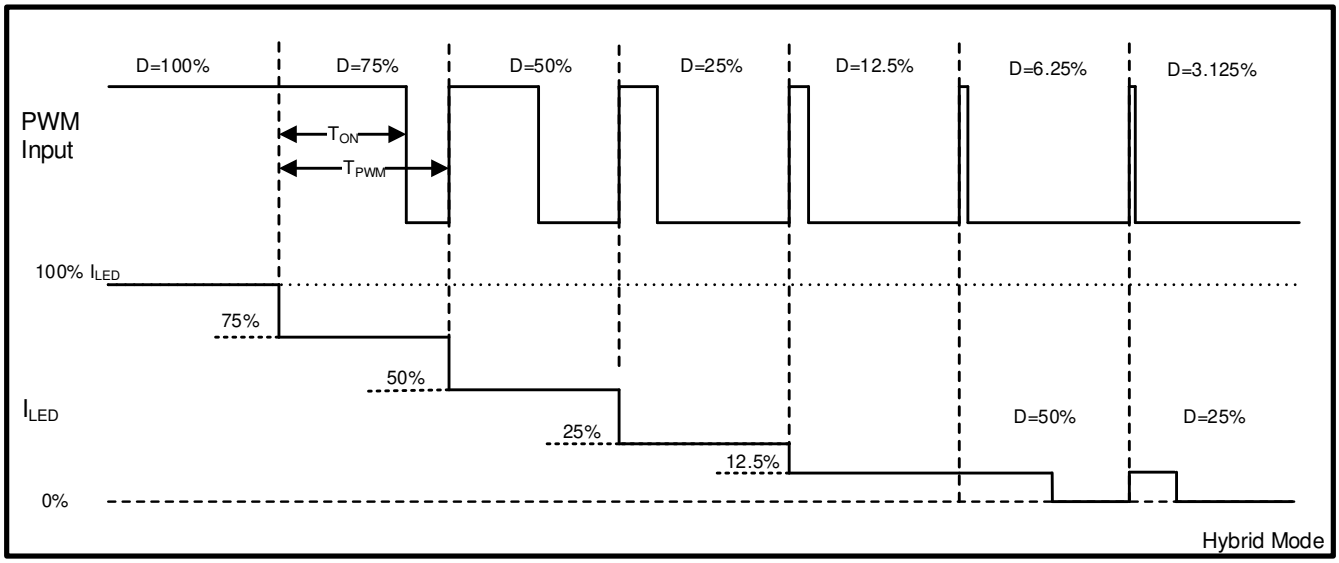


Figure 7-3. Hybrid Dimming

7.3.4.4 Flexible Dimming

The LP8868 family also supports flexible dimming to maximize the flexibility of dimming control, in which the LED current value and the on/off behavior are independently controllable. The flexible dimming mode is enabled when both the ADIM/HD pin and the PWM/EN pin are configured by PWM input signals at the same time. Therefore, in flexible dimming mode, the LED is turned on and off corresponding to the on and off of the PWM input signal at the PWM/EN pin while the reference voltage changes in proportion to the duty cycle of the PWM input signal at the ADIM/HD pin.

7.3.5 Undervoltage Lockout

The LP8868 family implements an internal undervoltage-lockout (UVLO) circuitry connecting to the VCC pin. The UVLO is triggered and then device is disabled when the VCC pin voltage falls below the internal UVLO threshold voltage, V_{VCC_UVLO} typically 3.0V, with a typical 0.2V hysteresis. The VCC pin is the output of an internal regulator of which the input is supplied by the VIN pin. Therefore, if VIN pin voltage falls close to above the V_{VCC_UVLO} (around 500mV above), the UVLO is triggered.

7.3.6 Fault Protection

The LP8868 family provides fault protections and send fault report signals in many fault conditions, including:

- LED open
- LED short to GND
- Sense resistor open and short
- Internal switching FET fault

- Thermal shutdown

The fault criterion for different topology is listed below.

Table 7-3. Protections in Buck Topology

TYPE	CRITERION	BEHAVIOR
LED open load	V_{UVP} < 1.2V for 100us	Fault pin pulls low. The device stops switching when V_{UVP} < 1.2V.
LED+ and LED- short circuit	V_{IN} - V_{CSP} < 300mV for 30ms	Fault pin pulls low. The device keeps normal behavior.
LED- short to GND	V_{UVP} < 1.2V for 100us	Fault pin pulls low. The device stops switching and recovers when fault is removed.
Sense-resistor open load	V_{CSP} - V_{CSN} > 300mV for 20us	Fault pin pulls low. The device stops switching and recovers when fault is removed.
Sense-resistor short circuit	Error amplifier output high for 100us	Fault pin pulls low. The device keeps switching under the cycle-by-cycle current limit.
Switching FET open	Error amplifier output high for 100us	Fault pin pulls low. The device keeps maximum duty cycle turn-on switching.
Switching FET short	V_{CSP} - V_{CSN} > 300mV for 20us	Fault pin pulls low. The device stops switching and recovers when fault is removed.
Thermal shutdown	T_J > T_{TSD} for 100us	Fault pin pulls low. The device stops switching when T_J>T_{TSD}, and is re-activated when T_J falls below the hysteresis level.
VIN UVLO	VCC < 3V	Fault pin pulls low. The device stops switching and recovers when fault is removed.

Table 7-4. Protections in Boost / Buck-Boost topology

TYPE	CRITERION	BEHAVIOR
LED open load	V_{OVP} > 1.2V for 100us	Fault pin pulls low. The device stops switching when V_{OVP} > 1.2V.
LED+ and LED- short circuit (Buck-Boost)	V_{CSP} - V_{IN} < 300mV for 30ms	Fault pin pulls low. The device keeps normal behavior.
LED+ short to GND	$_{CSP}$ - V_{CSN} > 300mV for 20us	Fault pin pulls low. The device stops switching and recovers when fault is removed.
Sense-resistor open load	V_{CSP} - V_{CSN} > 300mV for 20us	Fault pin pulls low. The device stops switching and recovers when fault is removed.
Sense-resistor short circuit	Error amplifier output high for 100us	Fault pin pulls low. The device keeps switching under the cycle-by-cycle current limit.
Switching FET open	Error amplifier output high for 100us	Fault pin pulls low. The device keeps maximum duty cycle turn-on switching.
Switching FET short	Error amplifier output high for 100us	Fault pin pulls low. The device tries to keep switching.
Thermal shutdown	T_J > T_{TSD} for 100us	Fault pin pulls low. The device stops switching when T_J > T_{TSD}, and is re-activated when T_J falls below the hysteresis level.
VIN UVLO	VCC < 3V	Fault pin pulls low. The device stops switching and recovers when fault is removed.

7.3.7 Thermal Foldback

The LP8868 family integrates thermal shutdown protection to prevent the device from overheating. To provide design margin of system thermal performance, the device enables a programmable thermal foldback function which automatically reduces the full-scale output current, I_{FS}, at high junction temperature. When the device, along with the LEDs, are mounted on the same thermal substrate, the thermal performance is effectively improved due to the reduction of dissipation need for both and LED.

As the junction temperature rises above the thermal foldback threshold temperature, T_{th}, the full-scale current starts to reduce following the current-temperature curve shown in the below figure. The current starts to reduce from the 100% level, typically at a rate of 2% of I_{FS} per °C until the current drops to 50% of the full scale. Once the junction temperature rises 25°C above the T_{th}, the current continues to decrease at a lower rate until the temperature reaches above the overtemperature shutdown threshold temperature, T_{TSD}.

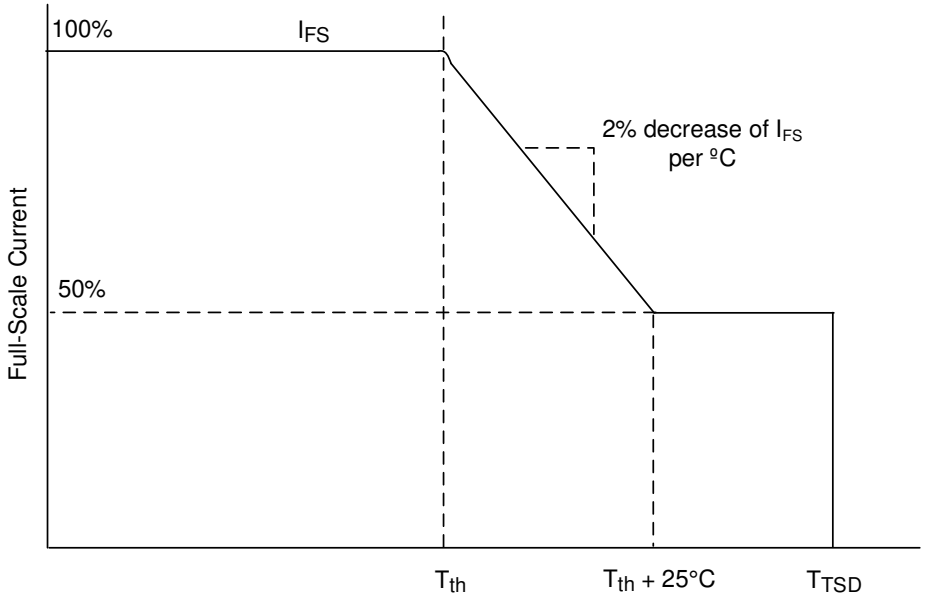


Figure 7-4. Thermal Foldback

The T_{th} can be adjusted by changing the resistor R_{TEMP} which connects between the TEMP and GND pin. The T_{th} and the corresponding R_{TEMP} value are listed in below table.

Table 7-5. T_{th} versus R_{TEMP} Resistor Value

T_{th} (°C)	Resistor Value (kΩ)
80	200
90	100
100	60
110	40
120	28
130	20
140	15
150	10

8 Application and Implementation

8.1 Application Information

LP8868 family can support buck, boost, and buck-boost topology with different part numbers.

The LP8868X is typically used as a boost converter, the LP8868Y is typically used as a buck-boost converter and the LP8868Z is typically used as a buck converter.

8.2 Typical Application

8.2.1 LP8868XQDMTRQ1 12V Input, 1A Output, 8-piece LED With Boost Topology

Figure 8-1 shows a typical application for the LP8868X in a boost topology. The switching current limit is 5.8 A and limits the output current.

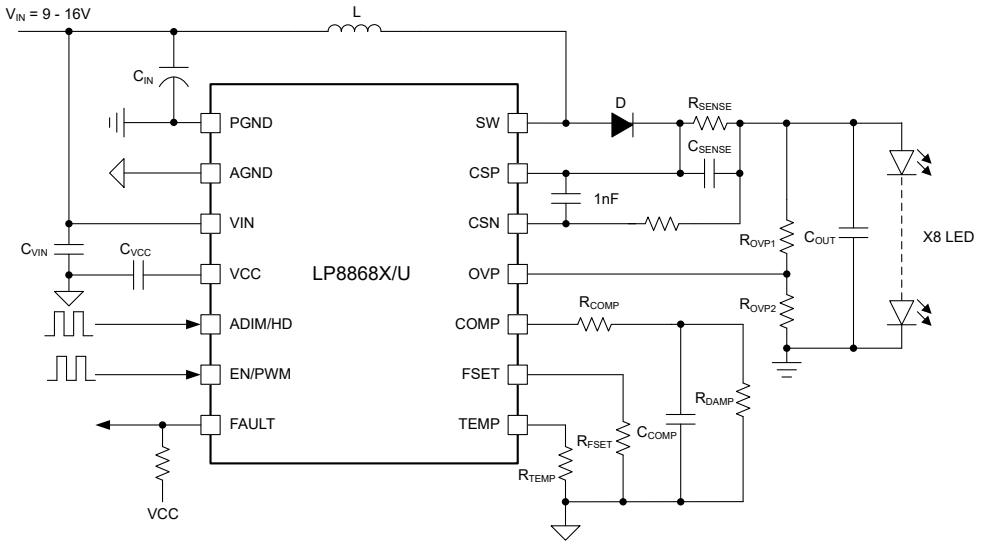


Figure 8-1. Typical Application for Boost Topology with LP8868X

8.2.1.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	9V − 16V
LED string	8 LED
Output voltage	24V
Switching frequency	400kHz
Maximum LED current	1A
Inductor current ripple	40% of maximum inductor current
Dimming type	PWM dimming and ADIM dimming

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

For this design, the input voltage is 9V to 16V. The output is 8 white LEDs in series and the inductor current ripple by requirement is less than 40% of maximum LED current. To choose a proper peak-to-peak inductor current ripple, do not violate the low-side FET current limit when the converter works in no-load condition. Avoiding violation requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to confirm reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once the peak-to-peak inductor current ripple is chosen, use Equation 2 to calculate the recommended value of the inductor L.

$$L = \frac{V_{IN(min)} \times \left(V_{OUT} - V_{IN[min]}\right)}{V_{OUT} \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (2)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current
- $I_{L(max)}$ is the maximum average inductor current
- f_{SW} is the switching frequency
- $V_{IN(min)}$ is the minimum input voltage
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor

With the chosen inductor value, calculate the actual inductor current ripple using Equation 3.

$$I_{L(ripple)} = \frac{V_{IN(min)} \times \left(V_{OUT} - V_{IN[min]}\right)}{V_{OUT} \times L \times f_{SW}} \quad (3)$$

Verify that the design ratings of inductor RMS current and saturation current are greater than the ratings in the system requirement. Perform this verification to establish that there is no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed the normal operating current and reach the current limit. Therefore, the preference is to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 4 and Equation 5.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (4)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^{2} + \frac{I_{L(ripple)}^{2}}{2}} \quad (5)$$

In this design, $V_{IN(min)}$ = 9V, V_{OUT} = 24V, I_{LED} = 1A, considering the efficiency as 0.9, $I_{L(max)}$ = 2.96A, f_{SW} = 400kHz, choose K_{IND} = 0.4, the calculated inductance is 11.9µH. A 10µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 1.41A, 3.67A, 2.96A, respectively.

8.2.1.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. For most applications, the recommendation is to place a 10µF ceramic capacitor along with a 0.1µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. Verify that the input capacitor voltage rating is greater than the maximum input voltage. Use Equation 6 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = \frac{I_{L(ripple)}}{8 \times K_{DR} \times C_{IN} \times f_{SW}} \quad (6)$$

In this design, a 33µF, 100V electrolytic capacitor, 10µF, 100V X7R ceramic capacitor and 0.1µF, 100V X7R ceramic capacitor are chosen, yielding approximately 88mV input ripple voltage.

8.2.1.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer data sheet.
2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.
3. Calculate the minimum effective output capacitance required.
4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See Equation 7, Equation 8, and Equation 9.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ \text{of LEDs} \tag{7}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \tag{8}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{9}$$

Once the output capacitor is chosen, use Equation 10 to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(ripple)}}{Z_{COUT} + R_{LED}} \tag{10}$$

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. In this design, a 10µF, 50V X7R ceramic capacitor is chosen.

8.2.1.2.4 Sense Resistor Selection

The maximum LED current is 1A at 100% PWM duty and the corresponding V_{REF} is 200mV. Use Equation 11 to calculate the sense resistance as 200mΩ. Note that the power consumption of the sense resistor is 200mW, requiring enough margin of the resistor's power rating in selection.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \tag{11}$$

In boost topology, C_{SENSE} is required to achieve the IFD control. Using Equation 12, a 10µF, 50V X7R ceramic capacitor is chosen for C_{SENSE} to suppress the ac magnitude of sense feedback less than 200mV. A 100Ω resistor is recommended at CSN pin to avoid noise injection and increase robustness.

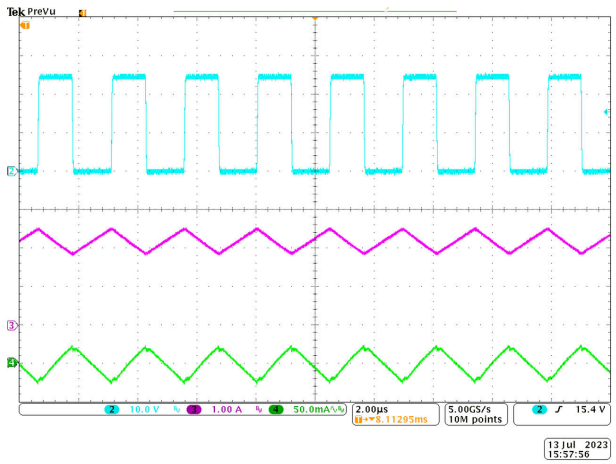
$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \tag{12}$$

8.2.1.2.5 Other External Components Selection

In this design, a 0.1µF, 50V X7R ceramic capacitor is chosen for high-frequency filtering of sense feedback.

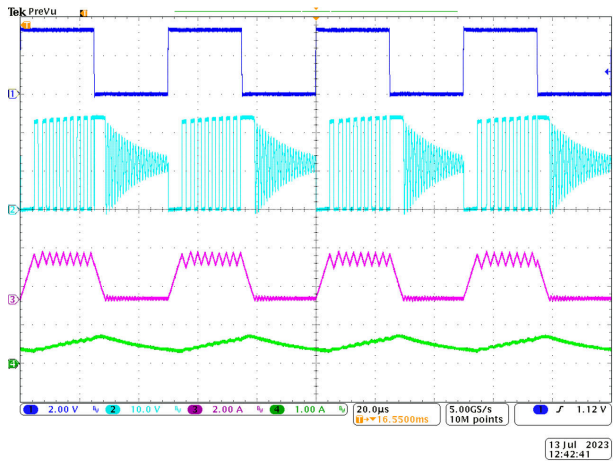
For loop stability, the recommendation is to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and a 1kΩ resistor for R_{COMP}. A 1MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.

8.2.1.3 Application Curves



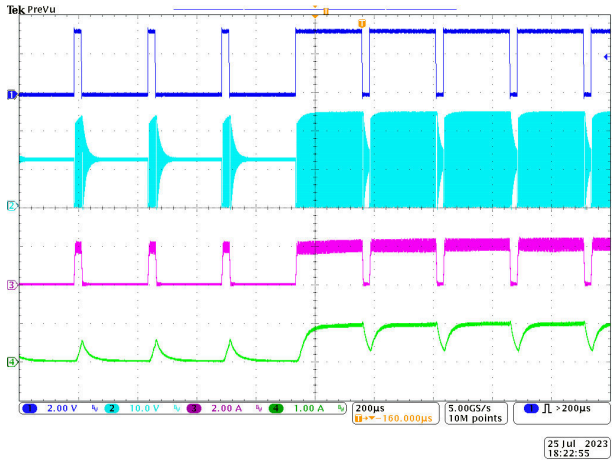
Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current Ripple (AC)

Figure 8-2. LED Current Ripple at ADIM = 100%, 1kHz and F_{SW} = 400kHz



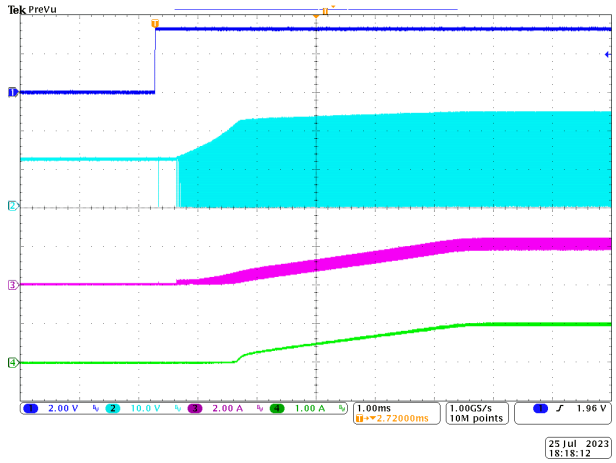
Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-3. LED Current Ripple at PWM = 50%, 20kHz and F_{SW} = 400kHz



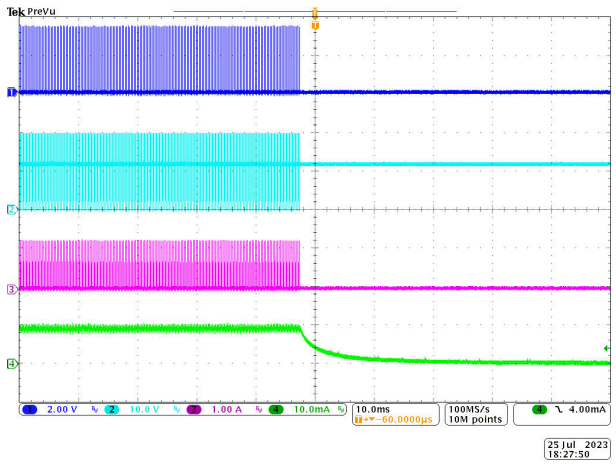
Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-4. LED Current Transient for a PWM Transition from 10% to 99%, 4kHz



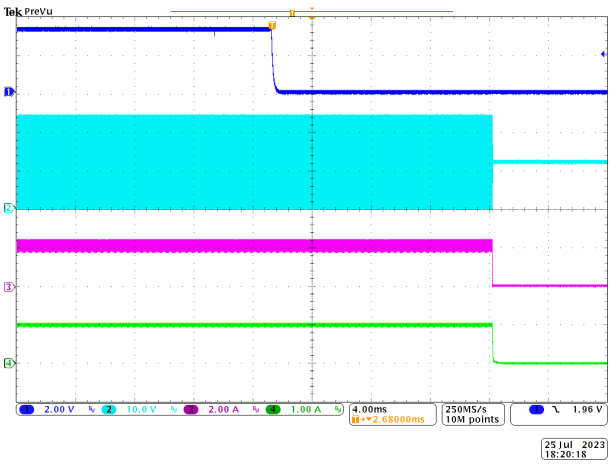
Ch 1: ADIM, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-5. Startup at ADIM = 100%, 500Hz



Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-6. Shutdown at PWM = 1%, 4kHz



Ch 1: ADIM, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-7. Shutdown at ADIM = 100%, 500Hz

8.2.2 LP8868YQDMTRQ1 12V Input, 1-A Output, 5-piece LED With Buck-Boost Topology

Figure 8-8 shows a typical application for the LP8868Y in a buck-boost topology. The switching current limit is 5.8 A and the switching current limit restricts the output current.

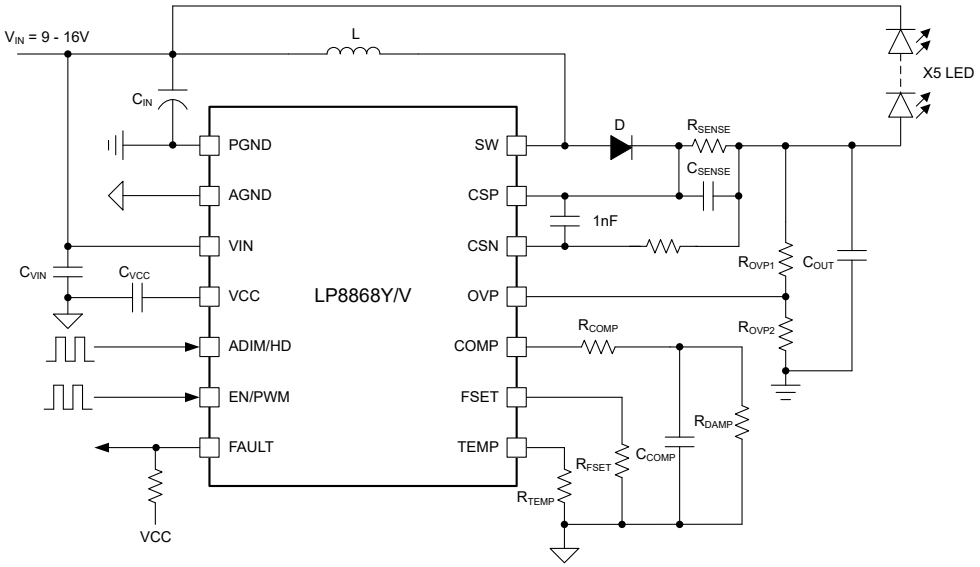


Figure 8-8. Typical Application for Buck-Boost Topology with LP8868Y

8.2.2.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-2. Design Parameters

PARAMETER	VALUE
Input voltage range	9V – 16V
LED string	5 LED
Output voltage	15V
Switching frequency	400kHz
Maximum LED current	1A

Table 8-2. Design Parameters (continued)

PARAMETER	VALUE
Inductor current ripple	40% of maximum inductor current
Dimming type	PWM dimming/ADIM dimming

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Inductor Selection

For this design, the input voltage is 9V to 16V. The output is 8 white LEDs in series and the inductor current ripple by requirement is less than 40% of maximum LED current. To choose a proper peak-to-peak inductor current ripple, do not violate the low-side FET current limit when the converter works in no-load condition. Avoiding violation requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to establish that reasonable inductor core loss and copper loss is caused by the peak-to-peak current ripple. After choosing the peak-to-peak inductor current ripple, use Equation 13 to calculate the recommended value of the inductor L.

$$L = \frac{V_{IN(min)} \times V_{OUT}}{\left(V_{OUT} + V_{IN[min]}\right) \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (13)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current
- $I_{L(max)}$ is the maximum average inductor current
- f_{SW} is the switching frequency
- $V_{IN(min)}$ is the minimum input voltage
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor

With the chosen inductor value, calculate the actual inductor current ripple using Equation 14.

$$I_{L(ripple)} = \frac{V_{IN(min)} \times V_{OUT}}{\left(V_{OUT} + V_{IN[min]}\right) \times L \times f_{SW}} \quad (14)$$

Verify that the design ratings of inductor RMS current and saturation current are greater than the design ratings in the system requirement to confirm that there is no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 15 and Equation 16.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (15)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^2 + \frac{I_{L(ripple)}^2}{2}} \quad (16)$$

In this design, $V_{IN(min)}$ = 9V, V_{OUT} = 15V, I_{LED} = 1A, considering the efficiency as 0.8, $I_{L(max)}$ = 2.083A, f_{SW} = 400kHz, choose K_{IND} = 0.4, the calculated inductance is 16.87µH. A 22µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.64A, 2.40A, 2.08A, respectively.

8.2.2.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. For most applications, the recommendation is to place a 10µF capacitor and a 0.1µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. Check that the input capacitor voltage rating is greater than the

maximum input voltage. Use Equation 17 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = I_{L(max)} \times \left(\frac{V_{OUT}}{K_{DR} \times C_{IN} \times f_{SW} \times V_{IN(max)}} + ESR_{CIN} \right) \quad (17)$$

In this design, a 33µF, 100V electrolytic capacitor, a 10µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding around 40 mV input ripple voltage.

8.2.2.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer data sheet.
2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$, $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.
3. Calculate the minimum effective output capacitance required.
4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage. See Equation 18, Equation 19, and Equation 20.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ \text{of LEDs} \quad (18)$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \quad (19)$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \quad (20)$$

Once the output capacitor is chosen, use Equation 21 to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(ripple)}}{Z_{COUT} + R_{LED}} \quad (21)$$

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. In this design, a 10µF, 50V X7R ceramic capacitor is chosen.

8.2.2.2.4 Sense Resistor Selection

The maximum LED current is 1A at 100% PWM duty and the corresponding V_{REF} is 200mV. By using Equation 22, the sense resistance is 200mΩ. Note that the power consumption of the sense resistor is 200mW, requiring enough margin of the resistor power rating in selection.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \quad (22)$$

In buck-boost topology, C_{SENSE} is required to achieve the IFD control. Using Equation 23, a 10µF, 50V X7R ceramic capacitor is chosen for C_{SENSE} to suppress the ac magnitude of sense feedback less than 200mV. A 100Ω resistor is recommended at CSN pin to avoid noise injection and increase robustness.

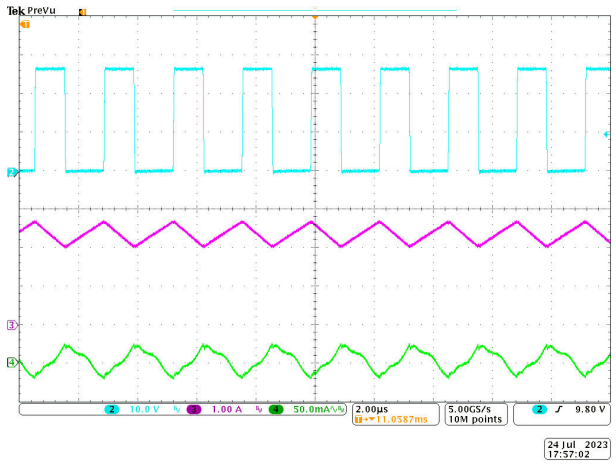
$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \quad (23)$$

8.2.2.2.5 Other External Components Selection

In this design, a 0.1µF, 50V X7R ceramic capacitor is chosen for high-frequency filtering of sense feedback.

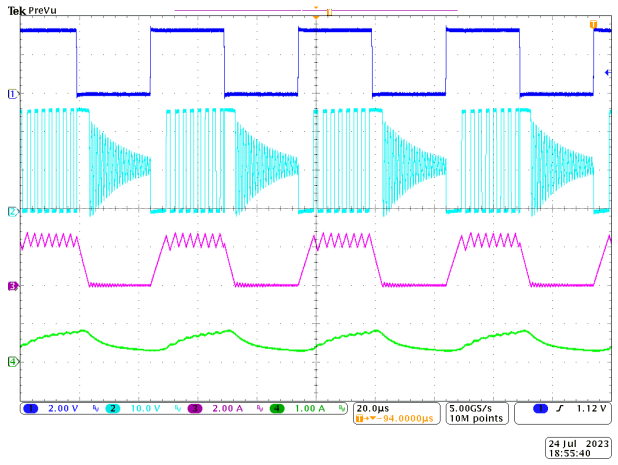
For loop stability, the recommendation is to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and a 1kΩ resistor for R_{COMP}. A 1MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.

8.2.2.3 Application Curves



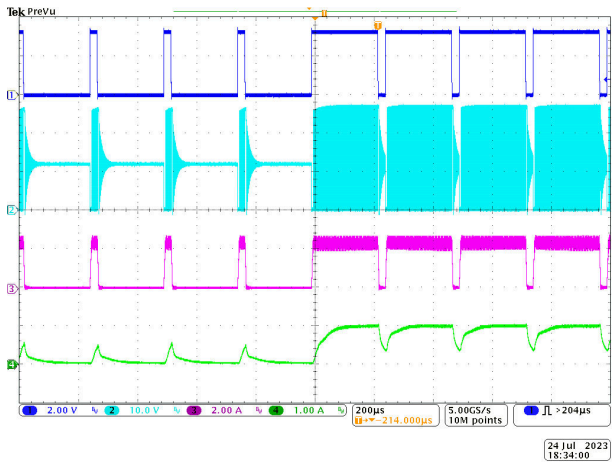
Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current Ripple (AC)

Figure 8-9. LED Current Ripple at ADIM = 100%, 1kHz and F_{SW} = 400kHz



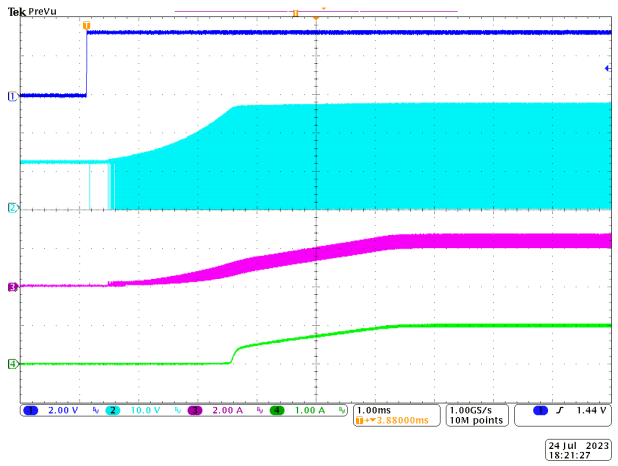
Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-10. LED Current Ripple at PWM = 50%, 20kHz and F_{SW} = 400kHz



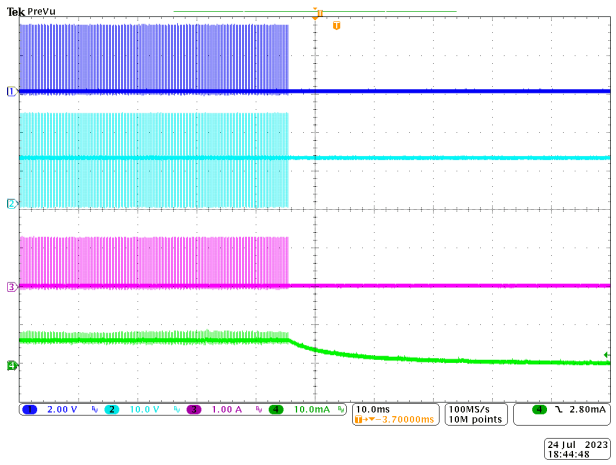
Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-11. LED Current Transient for a PWM Transition from 10% to 99%, 4kHz



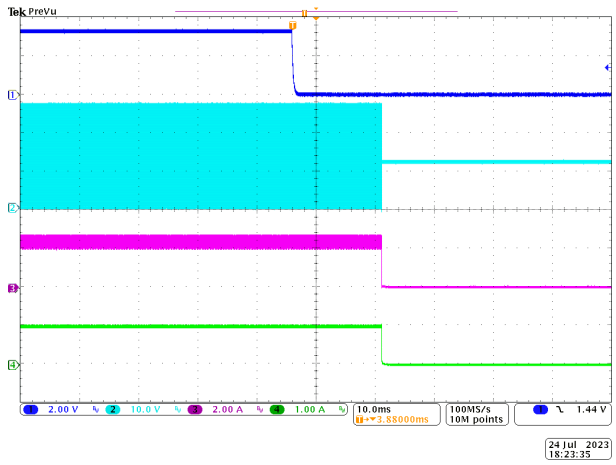
Ch 1: ADIM, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-12. Startup at ADIM = 100%, 500Hz



Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-13. Shutdown at PWM = 1%, 4kHz



Ch 1: ADIM, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-14. Shutdown at ADIM = 100%, 500Hz

8.2.3 LP8868ZQDMTRQ1 12V Input, 2A Output, 1-piece LED With Buck Topology

Figure 8-15 shows a typical application for the LP8868Z in a buck topology. The switching current limit is 5.2 A and the output current limit is equal to the limit of switching current limit.

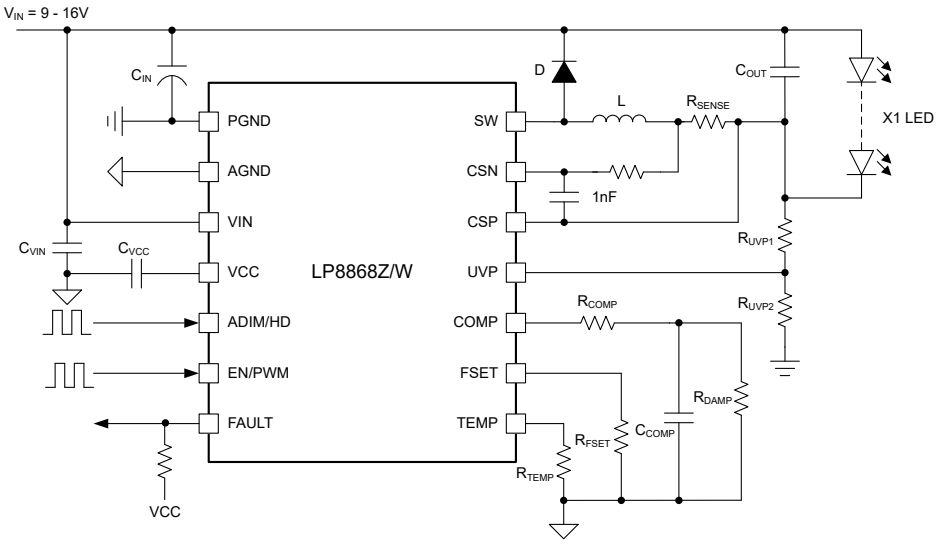


Figure 8-15. Typical Application for Buck Topology with LP8868Z

8.2.3.1 Design Requirements

For this design example, use the parameters in the following table.

Table 8-3. Design Parameters

PARAMETER	VALUE
Input voltage range	9V – 16V
LED string	1 LED
Output voltage	3V
Switching frequency	400kHz
Maximum LED current	2A

Table 8-3. Design Parameters (continued)

PARAMETER	VALUE
Inductor current ripple	40% of maximum inductor current
Dimming type	PWM dimming/ADIM dimming

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Inductor Selection

For this design, the input voltage is 9V to 16V. The output is single white LED and the inductor current ripple by requirement is less than 40% of maximum LED current. When choosing a proper peak-to-peak inductor current ripple, do not violate the low-side FET current limit when the converter works in no-load condition. To avoid violation, establish that half of the peak-to-peak inductor current ripple is lower than that limit. Another consideration is to verify the reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once the peak-to-peak inductor current ripple is chosen, use Equation 24 to calculate the recommended value of the inductor L.

$$L = \frac{V_{OUT} \times \left(V_{IN[max]} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (24)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current
- $I_{L(max)}$ is the maximum average LED current
- f_{SW} is the switching frequency
- $V_{IN(max)}$ is the maximum input voltage
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor

With the chosen inductor value, calculate the actual inductor current ripple using Equation 25.

$$I_{L(ripple)} = \frac{V_{OUT} \times \left(V_{IN[max]} - V_{OUT}\right)}{V_{IN(max)} \times L \times f_{SW}} \quad (25)$$

Establish that the design ratings of inductor RMS current and saturation current are greater than the design ratings in the system requirement to ensure that inductor overheat or saturation does not occur. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, the preference is to select a saturation current rating that is equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in Equation 26and Equation 27.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (26)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^{2} + \frac{I_{L(ripple)}^{2}}{2}} \quad (27)$$

In this design, $V_{IN(max)}$ = 16V, V_{OUT} = 3V, I_{LED} = 2A, choose K_{IND} = 0.4, the calculated inductance is 7.6µH. A 10-µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.61A, 2.30A, 2A, respectively.

8.2.3.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. For most applications, the recommendation is to place a 10µF capacitor along with a 0.1µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. Verify that the input capacitor voltage rating is greater than the maximum input voltage. Use Equation 28 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = I_{L(max)} \times \left(\frac{V_{OUT}}{K_{DR} \times C_{IN} \times f_{SW} \times V_{IN(max)}} + ESR_{CIN} \right) \quad (28)$$

In this design, a 33µF, 100V electrolytic capacitor, two 22µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding approximately 113mV input ripple voltage.

8.2.3.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer data sheet.
2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.
3. Calculate the minimum effective output capacitance required.
4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage. See Equation 29, Equation 30, and Equation 31.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \text{ \# of LEDs} \quad (29)$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \quad (30)$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \quad (31)$$

Once the output capacitor is chosen, use Equation 32 to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(ripple)}}{Z_{COUT} + R_{LED}} \quad (32)$$

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of the low ESR and small temperature coefficients. In this design, a 10µF, 35V X7R ceramic capacitor is chosen.

8.2.3.2.4 Sense Resistor Selection

The maximum LED current is 2A at 100% PWM duty and the corresponding V_{REF} is 200mV. Use Equation 33 to calculate the sense resistance as 100mΩ. Note that the power consumption of the sense resistor is 400mW, requiring enough margin of the resistor power rating in selection. A 100Ω resistor is recommended at CSN pin to avoid noise injection and increase robustness.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \quad (33)$$

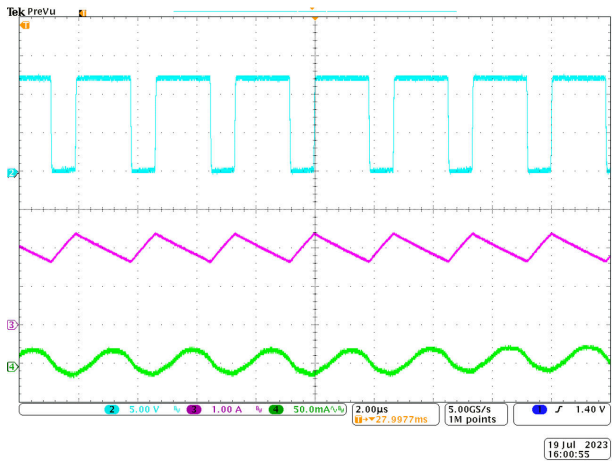
In buck topology, C_{sense} is optional to use.

8.2.3.2.5 Other External Components Selection

In this design, a 0.1µF, 50V X7R ceramic capacitor is chosen for high-frequency filtering of sense feedback.

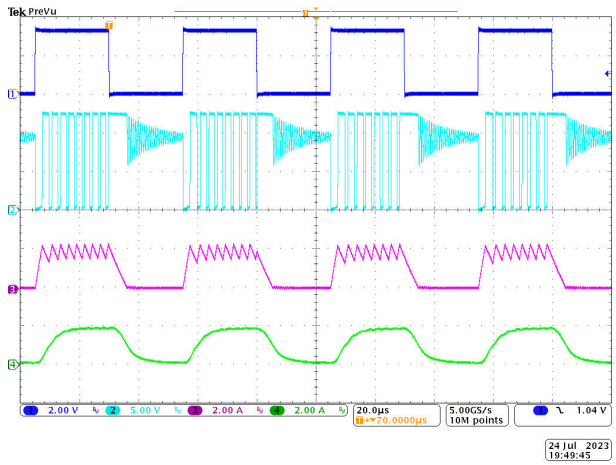
For loop stability, the recommendation is to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and a 1kΩ resistor for R_{COMP}. A 1MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.

8.2.3.3 Application Curves



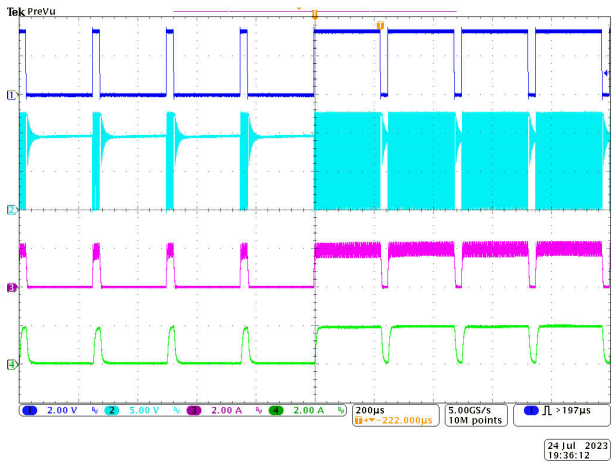
Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current Ripple (AC)

Figure 8-16. LED Current Ripple at ADIM = 100%, 1kHz and F_{SW} = 400kHz



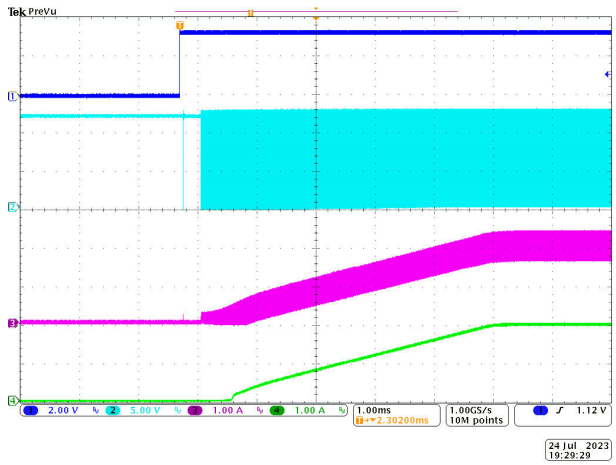
Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-17. LED Current Ripple at PWM = 50%, 20kHz and F_{SW} = 400kHz



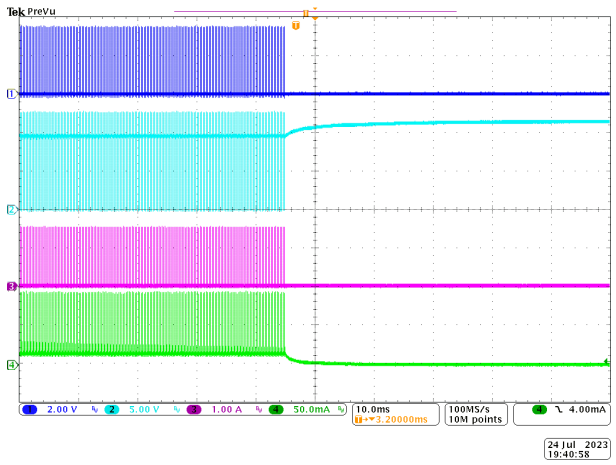
Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-18. LED Current Transient for a PWM Transition from 10% to 99%, 4kHz



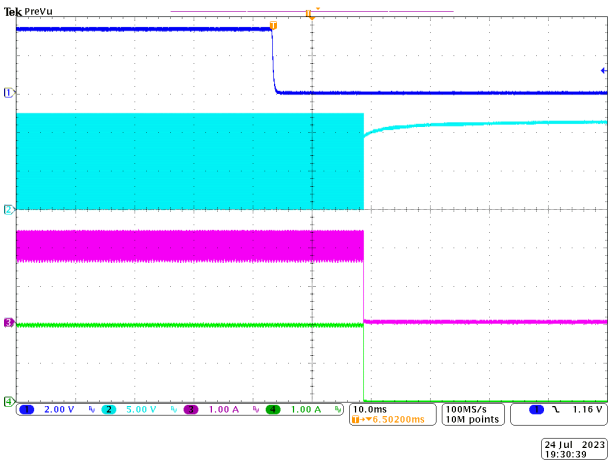
Ch 1: ADIM, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-19. Startup at ADIM = 100%, 500Hz



Ch 1: PWM/EN, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-20. Shutdown at PWM = 1%, 4kHz



Ch 1: ADIM, Ch 2: SW, Ch 3: Inductor Current, Ch 4: LED Current

Figure 8-21. Shutdown at ADIM = 100%, 500Hz

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging between 4.5V and 65V. Verify that the input supply is well regulated. The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because the dielectrics have low ESR and small temperature coefficients. For most applications, a 10µF capacitor is enough.

8.4 Layout

The LP8868-Q1 family requires a proper layout for peak performance. The following section provides guidelines to establish a proper layout.

8.4.1 Layout Guidelines

Examples of a proper layout for boost, buck-boost, and buck, topology of the LP8868 family are shown below.

- Creating a large GND plane for good electrical and thermal performance is important.
- Confirm that the IN and GND traces are as wide as possible to reduce trace impedance. Wide traces have the additional advantage of providing excellent heat dissipation.
- Use thermal vias to connect the top-side GND plane to additional printed-circuit board (PCB) layers for heat dissipation and grounding.
- Locate the input capacitors as close as possible to the IN pin and the GND pin.
- Place the VCC capacitor as close as possible to VCC pin to provide stable LDO output voltage.
- Verify that the SW trace remains as short as possible to reduce parasitic inductance and thereby reduce transient voltage spikes. Short SW trace also reduces radiated noise and EMI.
- Do not allow switching current to flow under the device.
- The routing of CSN and CSP traces are recommended to be in parallel and kept as short as possible and placed away from the high-voltage switching trace and the ground shield.
- Place the compensation capacitor as close as possible to COMP pin to prevent oscillation and system instability.

8.4.2 Layout Example

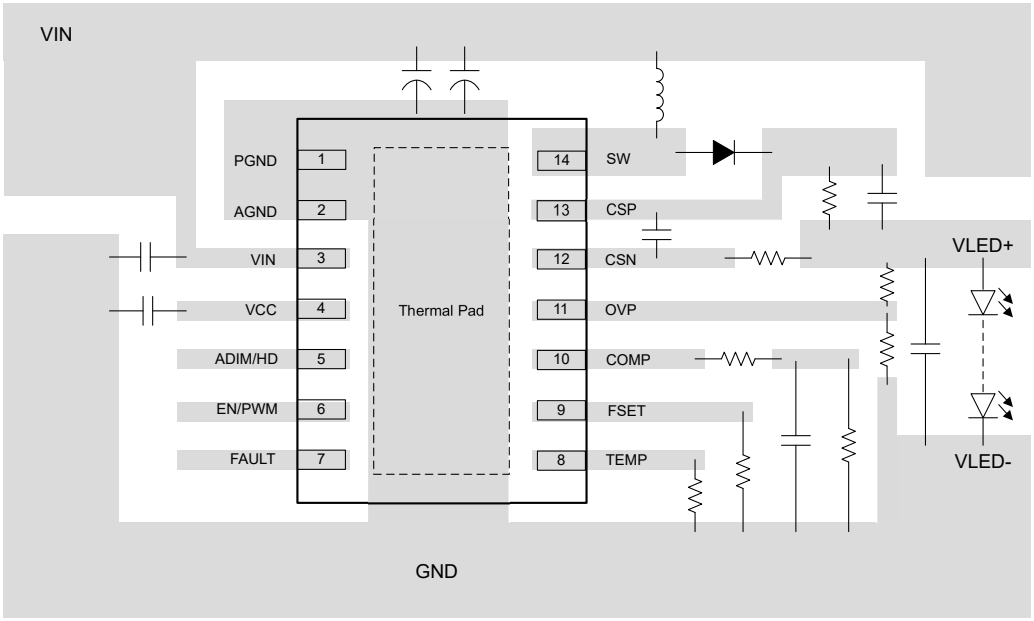


Figure 8-22. Boost Topology Top View Layout Example

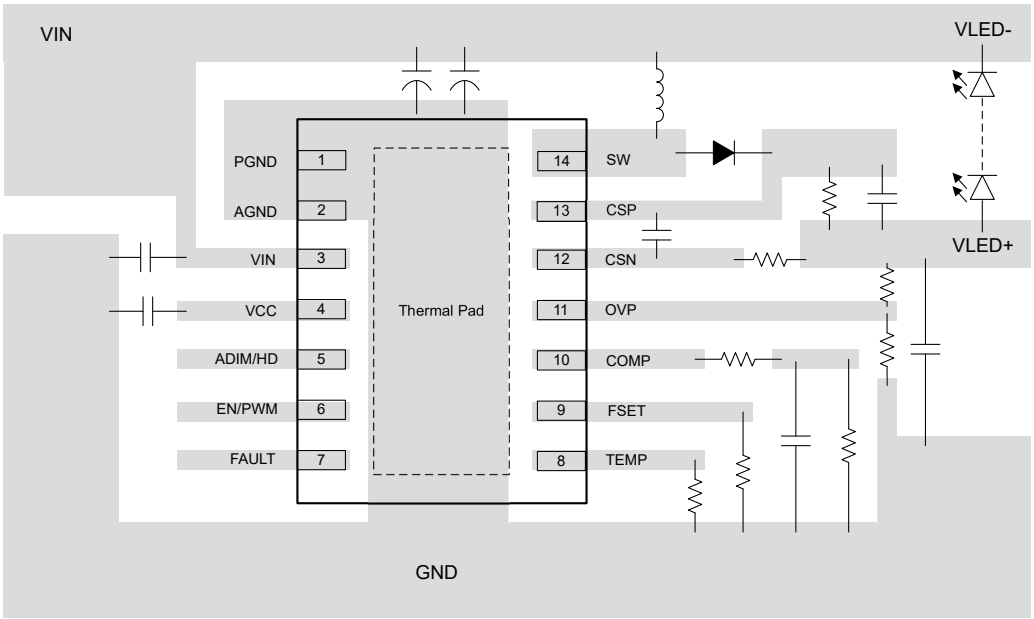


Figure 8-23. Buck-Boost Topology Top View Layout Example

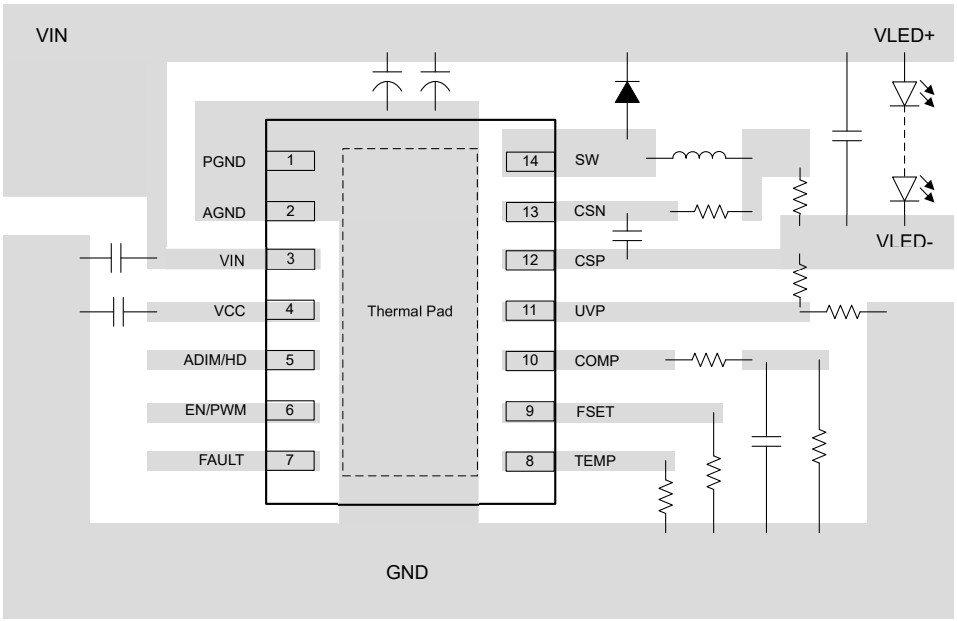


Figure 8-24. Buck Topology Top View Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision A (November 2023) to Revision B (Aug 2025)	Page
• Deleted the Product preview note from the HVSSOP package	1
• Updated Typical Boost LED Driver Application Schematic	1
• Updated the *Comparison Table*	3
• Updated the *Pin Configuration and Functions* for the HVSOP package	4
• Changed the Operation temp MAX value from 125 to 150 in Absolute Maximum Rating	8
• Add the HVSSOP values to the Thermal Information	8
• Updated the HVSSOP Current Limit section of the Electrical Characteristics	9
• Added text to the *Setting LED Current* section: "To avoid noise injection …"	16
• Changed Figure 8-1	21
• Changed Equation 2 and Equation 3	22
• Changed Equation 6	22
• Changed Figure 8-8	25
• Changed Equation 13 and Equation 14	26
• Changed Figure 8-15	29
• Updated values in the last paragraph in the *Inductor Selection*	30
• Updated the Layout Example	33

Changes from Revision * (July 2023) to Revision A (November 2023)	Page
• Added LP8868U-Q1, LP8868V-Q1, LP8868W-Q1 to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated s. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP8868UQDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868U
LP8868UQDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868U
LP8868VQDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868V
LP8868VQDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868V
LP8868WQDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868W
LP8868WQDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868W
LP8868XQDGNRQ1	Active	Production	HVSSOP (DGN) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L68X
LP8868XQDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868X
LP8868XQDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868X
LP8868YQDGNRQ1	Active	Production	HVSSOP (DGN) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L68Y
LP8868YQDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868Y
LP8868YQDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868Y
LP8868ZQDGNRQ1	Active	Production	HVSSOP (DGN) | 12	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L68Z
LP8868ZQDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868Z
LP8868ZQDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L868Z

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

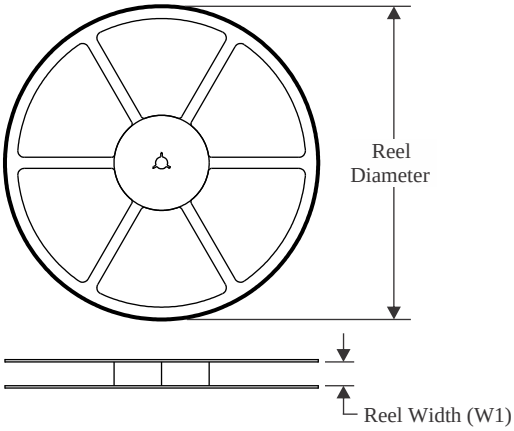
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

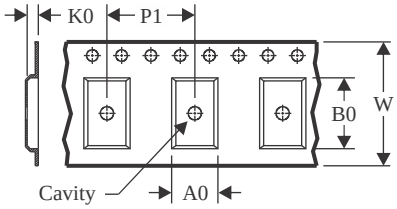
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

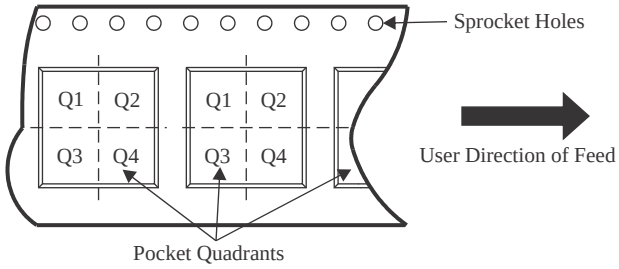


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

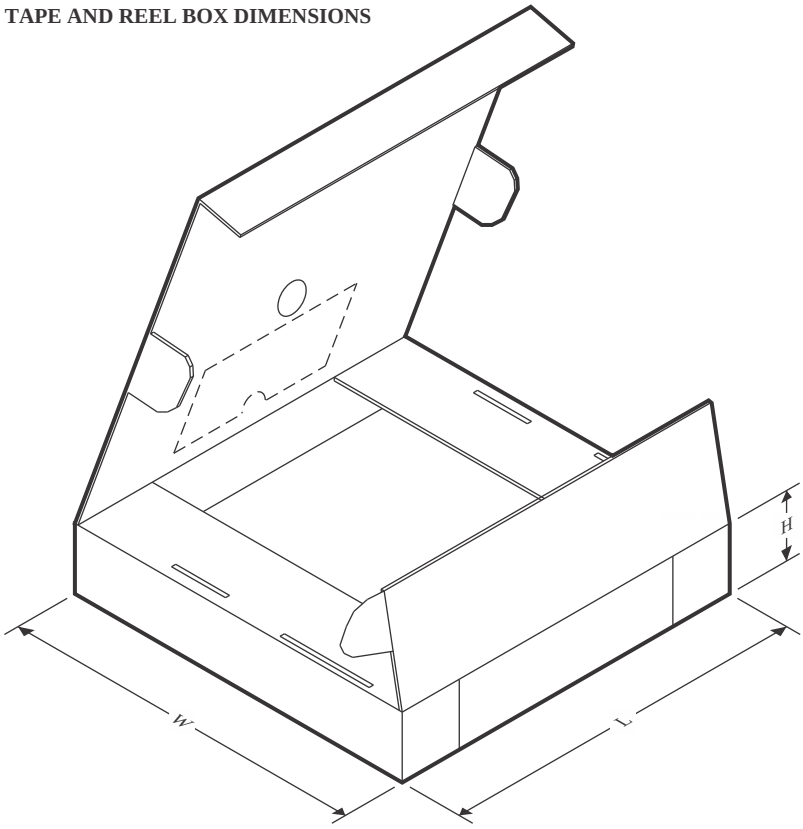
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8868UQDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
LP8868VQDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
LP8868WQDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
LP8868XQDGNRQ1	HVSSOP	DGN	12	5000	330.0	12.4	5.2	4.3	1.45	8.0	12.0	Q1
LP8868XQDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
LP8868YQDGNRQ1	HVSSOP	DGN	12	5000	330.0	12.4	5.2	4.3	1.45	8.0	12.0	Q1
LP8868YQDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
LP8868ZQDGNRQ1	HVSSOP	DGN	12	5000	330.0	12.4	5.2	4.3	1.45	8.0	12.0	Q1
LP8868ZQDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8868UQDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
LP8868VQDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
LP8868WQDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
LP8868XQDGNRQ1	HVSSOP	DGN	12	5000	353.0	353.0	32.0
LP8868XQDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
LP8868YQDGNRQ1	HVSSOP	DGN	12	5000	353.0	353.0	32.0
LP8868YQDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
LP8868ZQDGNRQ1	HVSSOP	DGN	12	5000	353.0	353.0	32.0
LP8868ZQDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

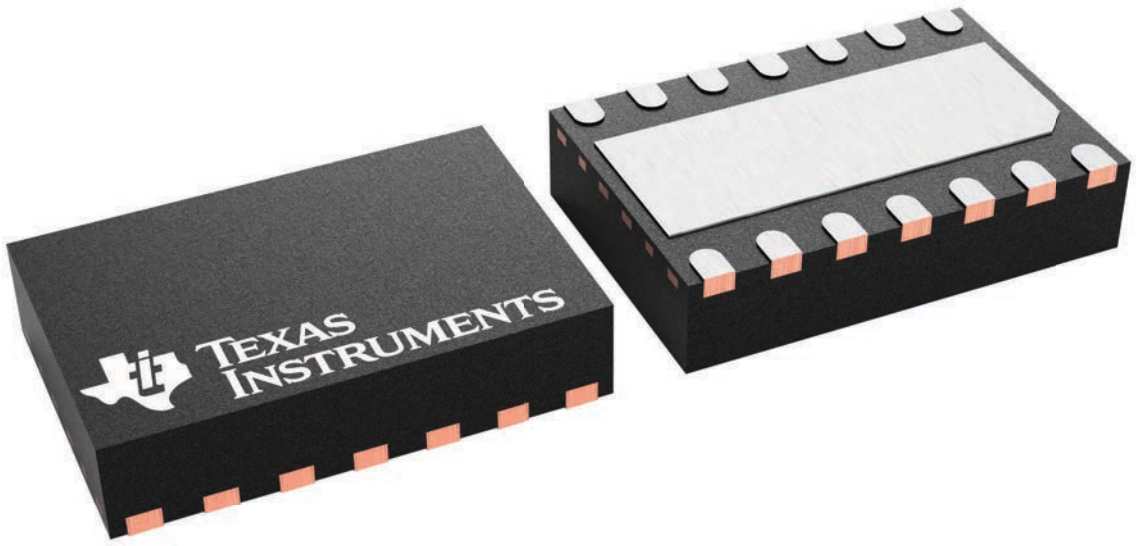
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



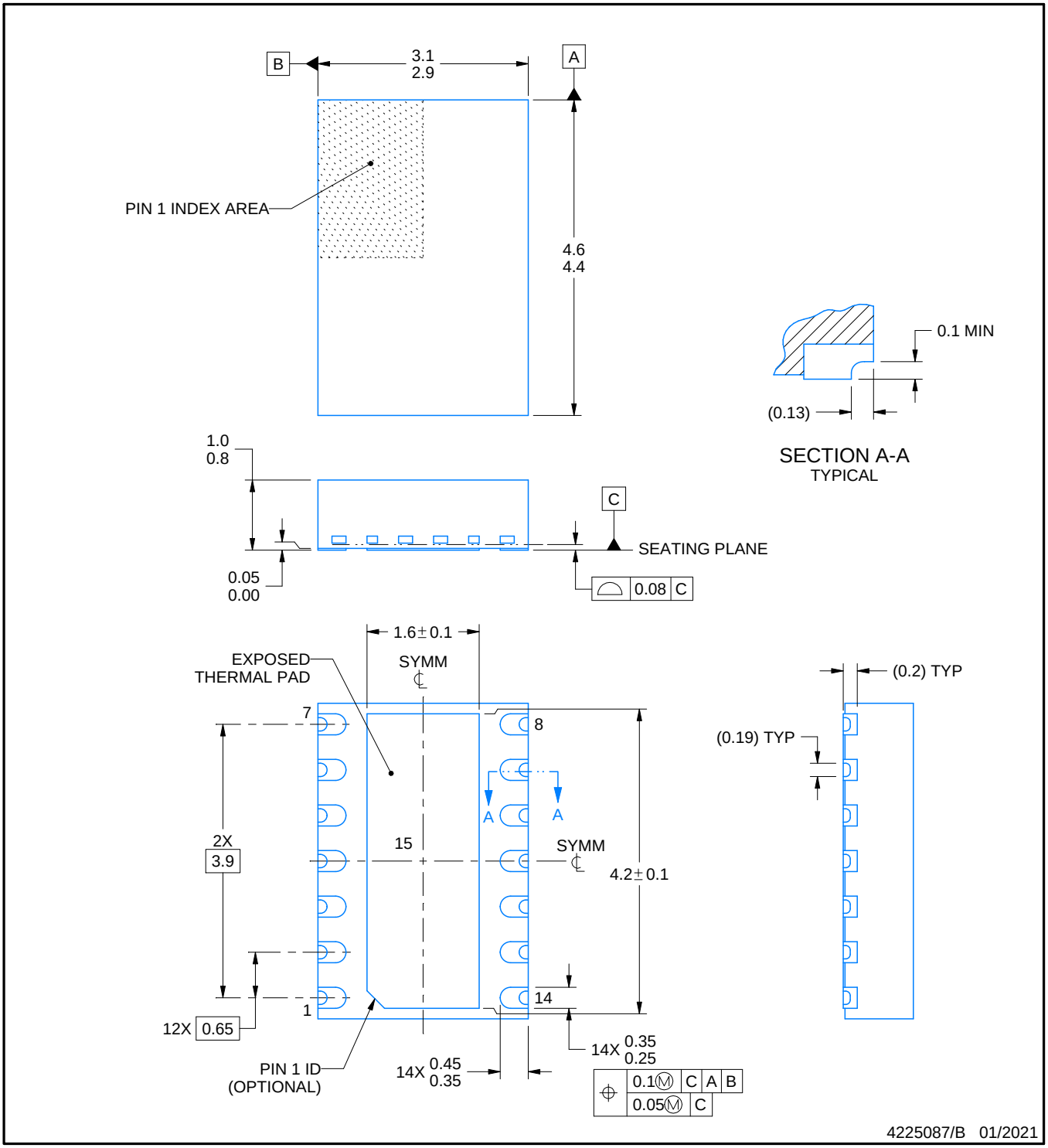
4225088/A

DMT0014B

PACKAGE OUTLINE

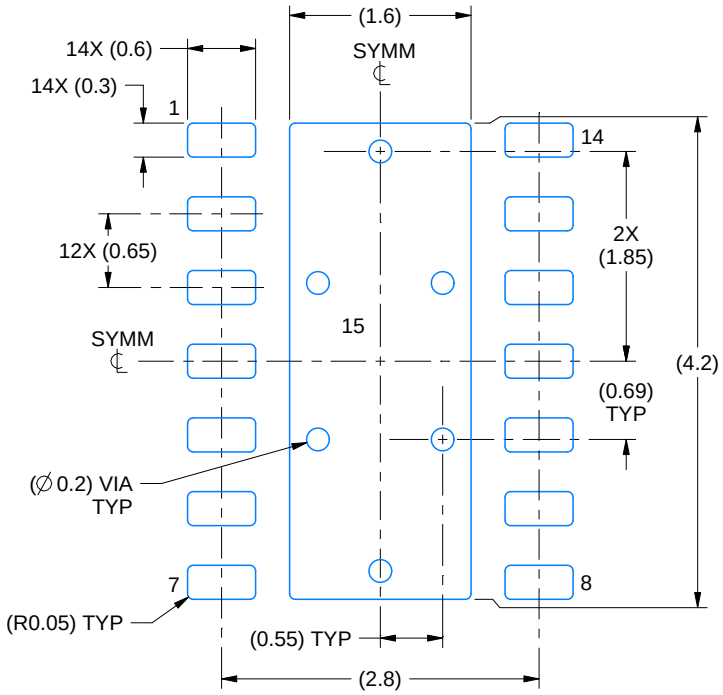
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

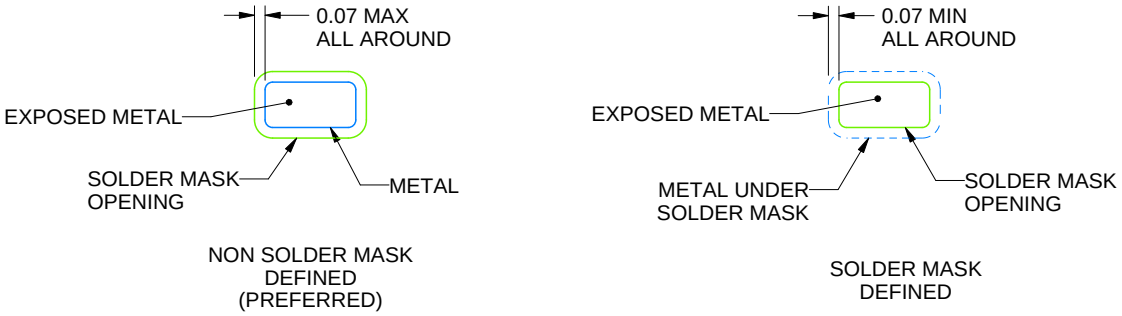


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

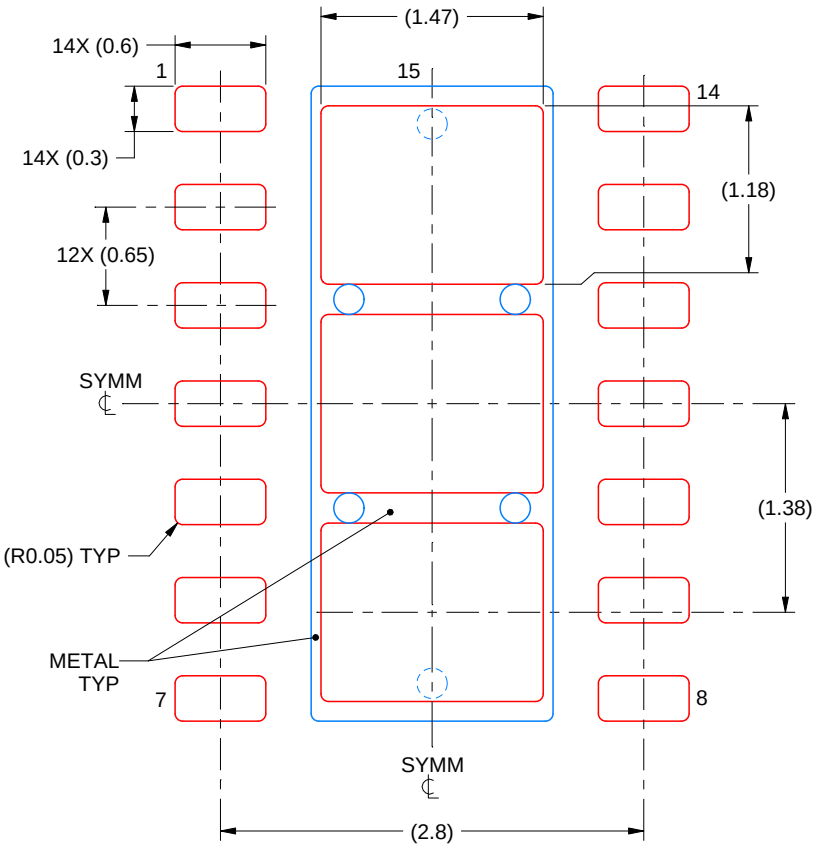


SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

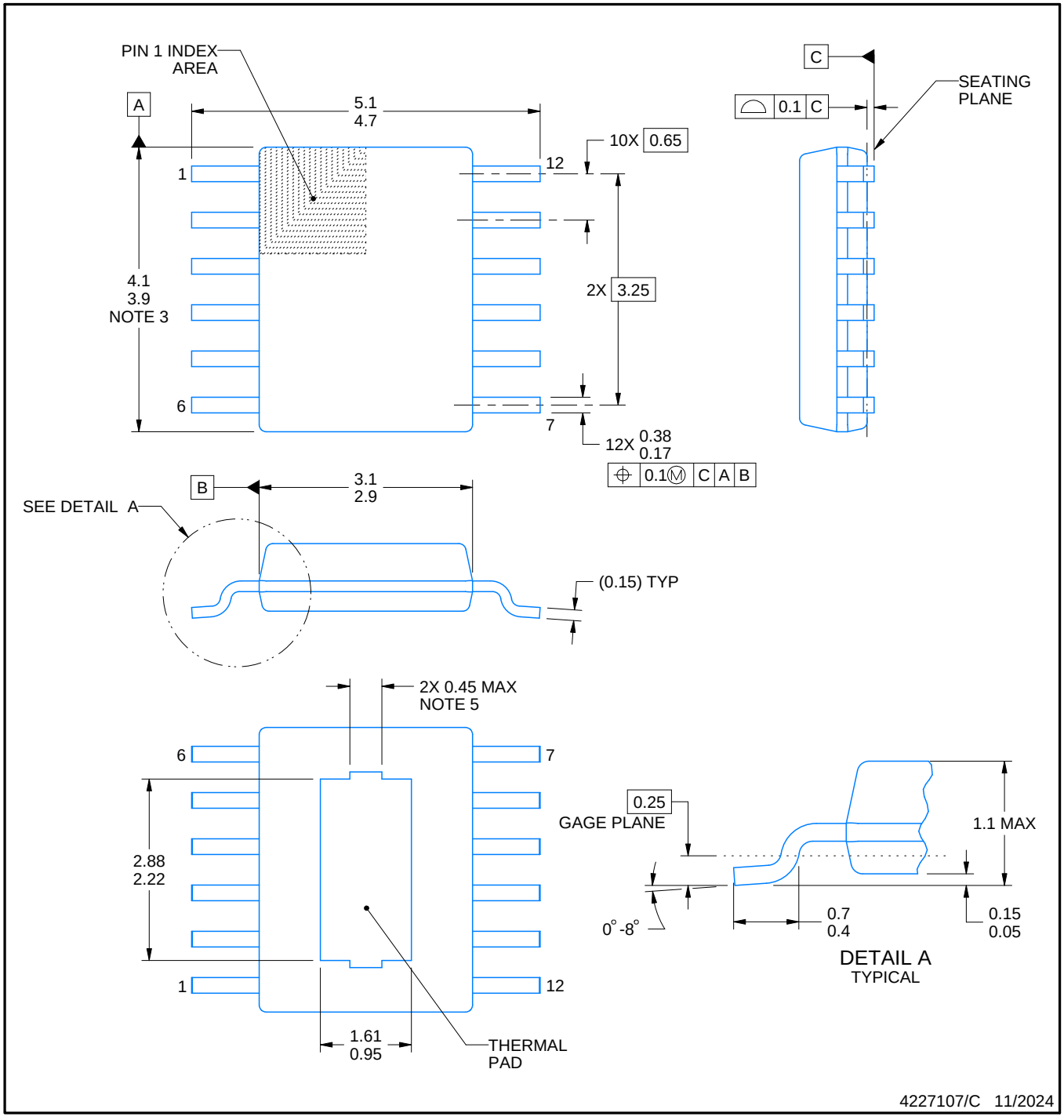
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGN0012A

PowerPAD™ HVSSOP - 1.1 mm max height

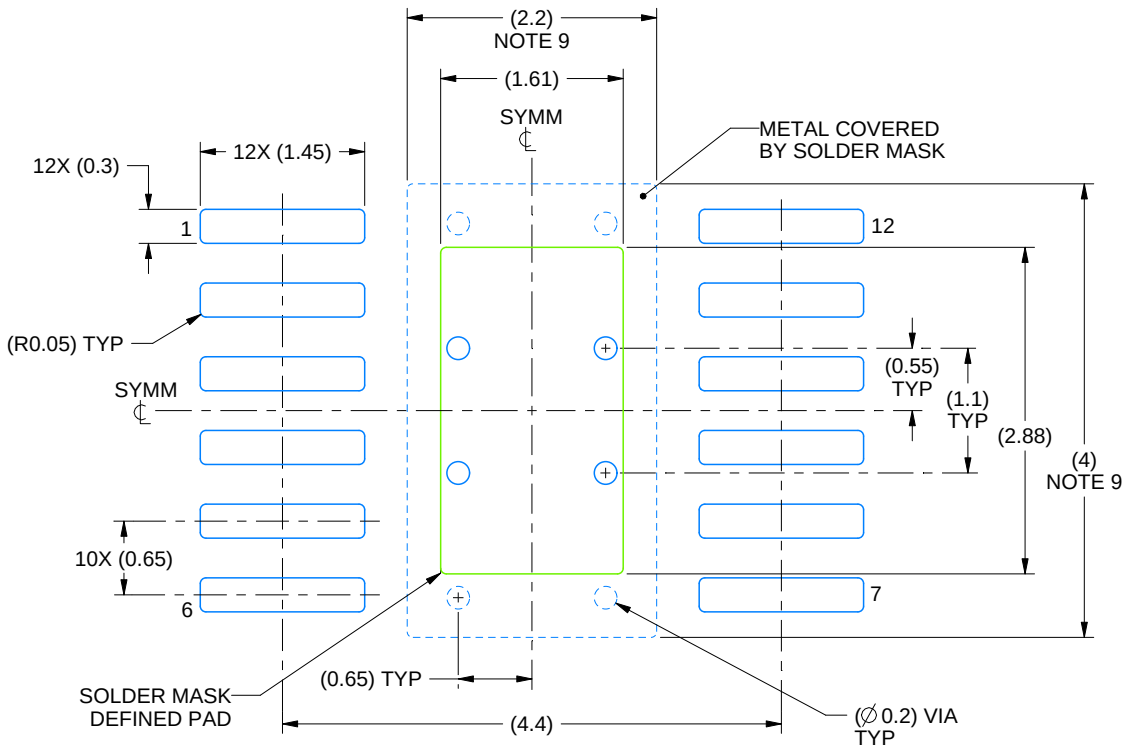
SMALL OUTLINE PACKAGE



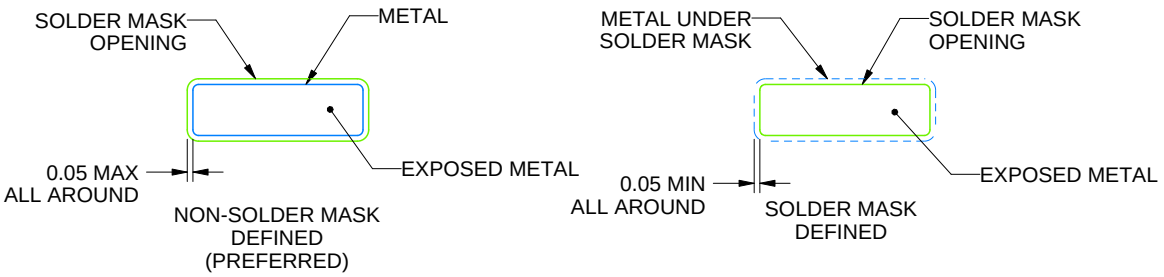
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

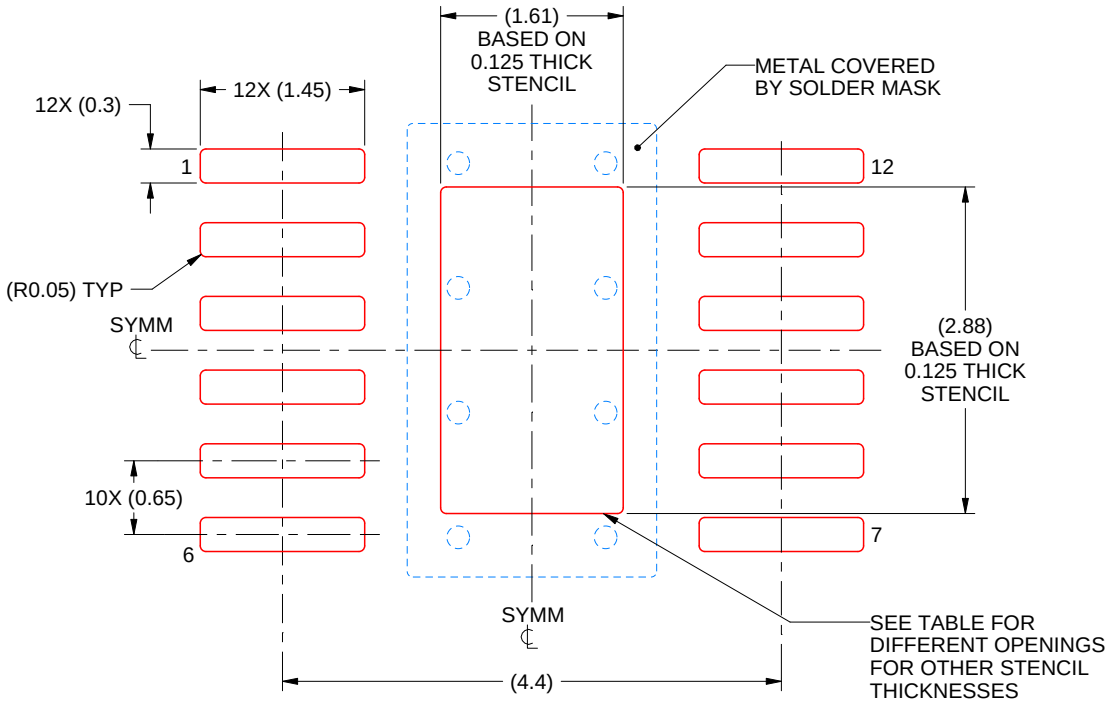


SOLDER MASK DETAILS

4227107/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.80 X 3.22
0.125	1.61 X 2.88 (SHOWN)
0.15	1.47 X 2.63
0.175	1.36 X 2.43

4227107/C 11/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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