MCT8329A High Speed Sensorless Trapezoidal Control Three-phase BLDC Gate Driver

1 Features

- Three-phase BLDC gate driver with integrated sensorless motor control algorithm
  - Code-free high speed Trapezoidal Control
  - Supports up to 3 kHz (electrical frequency)
  - Very fast startup time (<50 ms)
  - Fast Deceleration (<150 ms)
  - Supports 120° or 150° modulation to improve acoustic performance
  - Forward and reverse windmilling support
  - Analog, PWM, freq. or I^2C based control input
  - Configurable motor startup and stop options
  - Optional closed loop speed or power control, open loop voltage control
  - 5-point configurable reference profile support
  - Anti-voltage surge prevents overvoltage
  - Variable monitoring through DACOUT
- 65-V Three phase half-bridge gate driver
  - Drives 3 high-side and 3 low-side N-Channel MOSFETs, 4.5 to 60-V operating voltage
  - Supports 100% PWM duty cycle
  - Bootstrap based gate driver architecture
  - 1-A/2-A Maximum peak source/sink current
- Integrated current sense amplifier
  - Adjustable gain (5, 10, 20, 40 V/V)
- Low power sleep mode
  - 5-µA (maximum) at V_{PVDD} = 24-V, T_A = 25°C
- Speed loop accuracy: < 3% with internal clock
- Supports up to 100-kHz PWM frequency
- Accurate LDO (AVDD) 3.3-V ±3%, 50-mA support with AVDD connected to VREG
- Independent driver shutdown path (DRVOFF)
- Spread spectrum for EMI mitigation
- Suite of Integrated protection features
  - Supply undervoltage lockout (UVLO)
  - Motor lock detection (3 different types)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
  - Fault condition indication pin (nFAULT)
  - Optional fault diagnostics over I^2C interface

2 Applications

- Brushless-DC (BLDC) Motor Modules
- Cordless Vacuum Cleaners
- HVAC Blowers and Ventilators
- Appliance Fans and Pumps
- Cordless Garden and Power Tools, Lawnmowers

3 Description

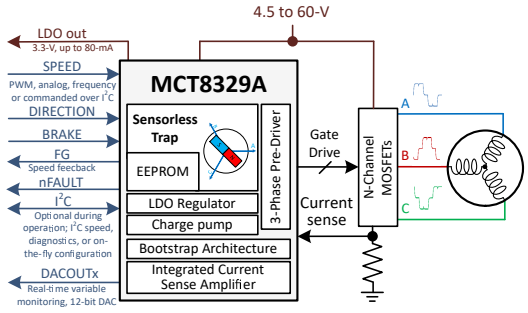
The MCT8329A provides a single-chip, code-free sensorless trapezoidal solution for applications requiring high speed operation or very fast startup time for three phase brushless-DC motors. The device provide three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The device generates correct gate drive voltages using an internal charge pump and enhances the high-side MOSFETs using a bootstrap circuit. A trickle charge pump is included to support 100% duty cycle. The gate drive architecture supports peak gate drive currents up to 1-A source and 2-A sink. The MCT8329A can operate from a single power supply and supports a wide input supply range of 4.5 to 60 V.

Sensorless trapezoidal control is highly configurable through register settings in a non-volatile EEPROM (MCT8329A1I) ranging from motor start-up behavior to closed loop operation, which allows the device to operate stand-alone once it has been configured. Motor current is sensed using an integrated current sensing amplifier supporting single external shunt resistor. The device receives a speed command through a PWM input or analog voltage or variable frequency square wave or I^2C command. There are a large number of protection features integrated into the MCT8329A, intended to protect the device, motor, and system against fault events.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCT8329A1IREER	VQFN (36)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2023	*	Initial Release

5 Pin Configuration and Functions

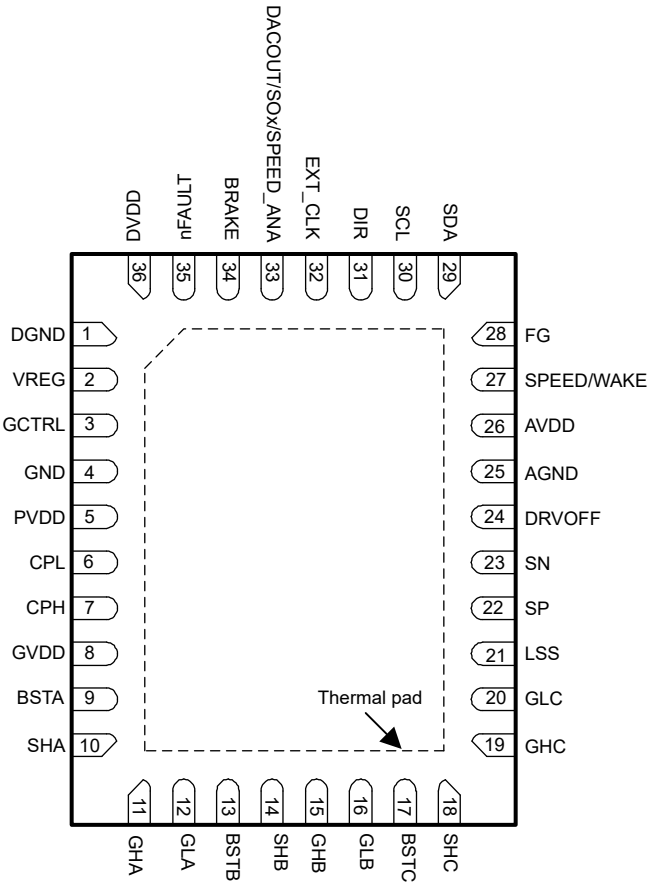


Figure 5-1. MCT8329A1I 36-Pin VQFN With Exposed Thermal Pad Top View

Table 5-1. Pin Functions

PIN	36-pin Package	TYPE[1]	DESCRIPTION
NAME	MCT8329A1I		
AGND	25	GND	Device analog ground
AVDD	26	PWR	3.3-V regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 50 mA external (if AVDD shorted to VREG) . TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
BRAKE	34	I	High → brake the motor Low → normal operation Connect to GND via 10-kΩ resistor, if not used
BSTA	9	O	Bootstrap output pin. Connect a X5R or X7R, 1-µF, 25-V ceramic capacitor between BSTA and SHA.
BSTB	13	O	Bootstrap output pin. Connect a X5R or X7R, 1-µF, 25-V ceramic capacitor between BSTB and SHB.
BSTC	17	O	Bootstrap output pin. Connect a X5R or X7R, 1-µF, 25-V ceramic capacitor between BSTC and SHC.
CPH	7	PWR	Charge pump switching node. Connect a X5R or X7R, PVDD-rated ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
CPL	6	PWR	
DACOUT/SOx/SPEED_ANA	33	I/O	Multipurpose pin. Configurable as DAC output, current sense amplifier output or analog reference (speed or power or voltage) input.

Table 5-1. Pin Functions (continued)

PIN	36-pin Package	TYPE[1]	DESCRIPTION
NAME	MCT8329A1I		
DGND	1	GND	Device digital ground
DIR	31	I	Direction of motor spinning; When low, phase driving sequence is OUT A → OUT B → OUT C When high, phase driving sequence is OUT A → OUT C → OUT B Connect to GND via 10-kΩ resistor, if not used
DRVOFF	24	I	Independent driver shutdown path. Pulling DRVOFF high turns off all external MOSFETs by putting the gate drivers into the pull-down state. This signal bypasses and overrides the digital and control core.
DVDD	36	PWR	1.5-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and DGND pins.
EXT_CLK	32	I	External clock reference input in external clock reference mode.
FG	28	O	Motor speed indicator output. Open-drain output requires an external pull-up resistor to 1.8 to 5-V. External pull up resistor needs to be connected even if the pin functionality is not used.
GCTRL	3	O	Gate control for external MOSFET used as regulator to supply current to digital subsystem through VREG pin. This functionality helps to reduce power dissipation inside the device.
GHA	11	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GHB	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GHC	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GLA	12	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GLB	16	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GLC	20	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GND	4	GND	Device power ground
GVDD	8	PWR	Gate driver power supply output. Connect a X5R or X7R, 30-V rated ceramic ≥ 10-uF local capacitance between the GVDD and GND pins. TI recommends a capacitor value of >10x C_{BSTx} and voltage rating at least twice the normal operating voltage of the pin.
LSS	21	PWR	Low side source pin, connect all sources of the external low-side MOSFETs here. This pin is the sink path for the low-side gate driver, and serves as an input to monitor the low-side MOSFET VDS voltage and VSEN_OCP voltage.
nFAULT	35	O	Fault indicator. This pin is pulled logic-low with fault condition. Open-drain output requires an external pull-up resistor to 1.8V to 5 V. External pull up resistor needs to be connected even if the pin functionality is not used.
PVDD	5	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1- µF, >2x PVDD-rated ceramic and >10-uF local capacitance between the PVDD and GND pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
SCL	30	I	I^2C clock input
SDA	29	I/O	I^2C data line
SHA	10	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHB	14	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHC	18	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SN	23	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.
SP	22	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPEED/ WAKE	27	I	Multifunction input. Device sleep/wake input. Device speed input; supports analog, PWM or frequency based reference (speed or power or voltage) input.

Table 5-1. Pin Functions (continued)

PIN	36-pin Package	TYPE(1)	DESCRIPTION
NAME	MCT8329A1I		
VREG	2	PWR	Voltage regulator input supply for internal DVDD LDO. Connect to AVDD or external 3-5.5 V. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the VREG and DGND pins.
Thermal pad	-	PWR	Must be connected to ground

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	-0.3	65	V
Bootstrap pin voltage	BSTx	-0.3	80	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	20	V
Bootstrap pin voltage	BSTx with respect to GHx	-0.3	20	V
Charge pump pin voltage	CPL, CPH	-0.3	V_{GVDD}	V
Voltage difference between ground pins	GND, DGND, AGND	-0.3	0.3	V
Voltage regulator pin voltage (VREG)	VREG	-0.3	6	V
Gate control pin voltage (GCTRL)	GCTRL	-0.3	7	V
Gate driver regulator pin voltage	GVDD	-0.3	20	V
Digital regulator pin voltage	DVDD	-0.3	1.7	V
Analog regulator pin voltage	AVDD	-0.3	4	V
Logic pin voltage	BRAKE, DRVOFF, DIR, EXT_CLK, SCL, SDA, SPEED/WAKE, DACOUT/SOx/SPEED_ANA	-0.3	6	V
Open drain pin output voltage	nFAULT, FG	-0.3	6	V
High-side gate drive pin voltage	GHx	-8	80	V
Transient 500-ns high-side gate drive pin voltage	GHx	-10	80	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	20	V
High-side source pin voltage	SHx	-8	70	V
Transient 500-ns high-side source pin voltage	SHx	-10	72	V
Low-side gate drive pin voltage	GLx with respect to LSS	-0.3	20	V
Transient 500-ns low-side gate drive pin voltage(2)	GLx with respect to LSS	-1	20	V
Low-side gate drive pin voltage	GLx with respect to GVDD		0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx with respect to GVDD		1	V
Low-side source sense pin voltage	LSS	-1	1	V
Transient 500-ns low-side source sense pin voltage	LSS	-10	8	V
Gate drive current	GHx, GLx	Internally Limited	Internally Limited	A
Shunt amplifier input pin voltage	SN, SP	-1	1	V
Transient 500-ns shunt amplifier input pin voltage	SN, SP	-10	8	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) Supports upto 5A for 500 nS when GLx-LSS is negative

6.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Power supply voltage	PVDD	4.5		60	V
V_{PVDD_RAMP}	Power supply voltage ramp rate at power up	PVDD			30	V/us
V_{BST}	Bootstrap pin voltage with respect to SHx	SPEED/WAKE = High, Outputs are switching	4		20	V
I_{AVDD} (1)	Regulator external load current (AVDD connected to VREG)	AVDD			50	mA
$I_{TRICKLE}$	Trickle charge pump external load current	BSTx			2	µA
V_{VREG}	VREG pin voltage	VREG	2.2		5.5	V
V_{IN}	Logic input voltage	BRAKE, DRVOFF, DIR, EXT_CLK, SPEED/WAKE, SDA, SCL	0		5.5	V
f_{PWM}	PWM frequency		0		100	kHz
V_{OD}	Open drain pullup voltage	FG, nFAULT			5.5	V
I_{OD}	Open drain output current	nFAULT			-10	mA
I_{GS} (1)	Total average gate-drive current (Low Side and High Side Combined)	I_{GHx}, I_{GLx}			30	mA
V_{SHSL}	Slew Rate on SHx pins				4	V/ns
C_{BOOT}	Capacitor between BSTx and SHx				4.7(2)	µF
C_{GVDD}	Capacitor between GVDD and GND				130	µF
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed
(2) Current flowing through boot diode (DBOOT) needs to be limited for C_{BSTx} > 4.7µF.

6.4 Thermal Information 1pkg

THERMAL METRIC(1)		MCT8329A REE (VQFN) 36	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (PVDD, GVDD, AVDD, DVDD, VREG, GCTRL)						
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} = 24V, $V_{SPEED/WAKE}$ = 0, T_A = 25 °C, AVDD connected to VREG		3	5	µA
		$V_{SPEED/WAKE}$ = 0, T_A = 125 °C, AVDD connected to VREG		3.5	6	µA
I_{PVDDS}	PVDD standby mode current	V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ < V_{EN_SB}, DRVOFF = LOW, T_A = 25 °C, AVDD connected to VREG		25	28	mA
		$V_{SPEED/WAKE}$ < V_{EN_SB} , DRVOFF = LOW, AVDD connected to VREG		25	28	mA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), T_J = 25 °C, No FETs and motor connected, AVDD connected to VREG		28	30	mA
		V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), No FETs and motor connected, AVDD connected to VREG		28	30	mA
		V_{PVDD} = 8 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), T_J = 25 °C, No FETs and motor connected, AVDD not connected to VREG, VREG = 3.3V external		8.5	14.1	mA
		V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), No FETs and motor connected, AVDD not connected to VREG, VREG = 3.3V external		8.5	11.1	mA
I_{VREG}	VREG pin active mode current	$V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 10000b (25 kHz), VREG connected to AVDD			25	mA
IL_{BSx}	Bootstrap pin leakage current	V_{BSTx} = V_{SHx} = 60V, V_{GVDD} = 0V, $V_{SPEED/WAKE}$ = LOW	5	10	16	µA
IL_{BS_TRAN}	Bootstrap pin active mode transient leakage current	GLx = GHx = Switching at 20kHz, No FETs connected	60	115	300	µA
V_{GVDD_RT}	GVDD Gate driver regulator voltage (Room Temperature)	V_{PVDD} ≥ 40 V, I_{GS} = 10 mA, T_J= 25°C	11.8	13	15	V
		22 V ≤V_{PVDD} ≤ 40 V, I_{GS} = 30 mA, T_J= 25°C	11.8	13	15	V
		8 V ≤V_{PVDD} ≤ 22 V, I_{GS} = 30 mA, T_J= 25°C	11.8	13	15	V
		6.75 V ≤V_{PVDD} ≤ 8 V, I_{GS} = 10 mA, T_J= 25°C	11.8	13	14.5	V
		4.5 V ≤V_{PVDD} ≤ 6.75 V, I_{GS} = 10 mA, T_J= 25°C	2*V_{PVDD} - 1		13.5	V
V_{GVDD}	GVDD Gate driver regulator voltage	V_{PVDD} ≥ 40 V, I_{GS} = 10 mA	11.5		15.5	V
		22 V ≤V_{PVDD} ≤ 40 V, I_{GS} = 30 mA	11.5		15.5	V
		8 V ≤V_{PVDD} ≤ 22 V; I_{GS} = 30 mA	11.5		15.5	V
		6.75 V ≤V_{PVDD} ≤ 8 V, I_{GS} = 10 mA	11.5		14.5	V
		4.5 V ≤V_{PVDD} ≤ 6.75 V, I_{GS} = 10 mA	2*V_{PVDD} - 1.4		13.5	V

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD_RT}	AVDD Analog regulator voltage (Room Temperature)	V_{PVDD} ≥ 6 V, 0 mA ≤ I_{AVDD} ≤ 30 mA, T_J= 25°C	3.26	3.3	3.33	V
		V_{PVDD} ≥ 6 V, 30 mA ≤ I_{AVDD} ≤ 80 mA, T_J= 25°C	3.2	3.3	3.4	V
		V_{PVDD} ≤ 6 V, 0 mA ≤ I_{AVDD} ≤ 50 mA, T_J= 25°C	3.13	3.3	3.46	V
V_{DVDD}	Digital regulator voltage	VREG = 3.3V	1.4	1.55	1.65	V
V_{AVDD}	AVDD Analog regulator voltage	V_{PVDD} ≥ 6 V, 0 mA ≤ I_{AVDD} ≤ 80 mA	3.2	3.3	3.4	V
		V_{PVDD} ≤ 6 V, 0 mA ≤ I_{AVDD} ≤ 50 mA	3.125	3.3	3.5	V
V_{GCTRL}	Gate control volatge	V_{PVDD} > 4.5 V	4.9	5.7	6.5	V
GATE DRIVERS (GHx, GLx, SHx, SLx)						
V_{GSHx_LO}	High-side gate drive low level voltage	I_{GHx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0.05	0.11	0.24	V
V_{GSHx_HI}	High-side gate drive high level voltage (V_{BSTx} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.28	0.44	0.82	V
V_{GSLx_LO}	Low-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0.05	0.11	0.27	V
V_{GSLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GLx})	I_{GLx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.28	0.44	0.82	V
$R_{DS(ON)\_PU\_HS}$	High-side pullup switch resistance	I_{GHx} = 100 mA; V_{GVDD}= 12V	2.7	4.5	8.4	Ω
$R_{DS(ON)\_PD\_HS}$	High-side pulldown switch resistance	I_{GHx} = 100 mA; V_{GVDD} = 12V	0.5	1.1	2.4	Ω
$R_{DS(ON)\_PU\_LS}$	Low-side pullup switch resistance	I_{GLx} = 100 mA; V_{GVDD} = 12V	2.7	4.5	8.3	Ω
$R_{DS(ON)\_PD\_LS}$	Low-side pulldown switch resistance	I_{GLx} = 100 mA; V_{GVDD} = 12V	0.5	1.1	2.8	Ω
I_{DRIVEP_HS}	High-side peak source gate current	V_{GSHx} = 12V	550	1000	1575	mA
I_{DRIVEN_HS}	High-side peak sink gate current	V_{GSHx} = 0V	1150	2000	2675	mA
I_{DRIVEP_LS}	Low-side peak source gate current	V_{GSLx} = 12V	550	1000	1575	mA
I_{DRIVEN_LS}	Low-side peak sink gate current	V_{GSLx} = 0V	1150	2000	2675	mA
R_{PD_LS}	Low-side passive pull down	GLx to LSS	80	100	120	kΩ
R_{PDSA_HS}	High-side semiactive pull down	GHx to SHx, V_{GSHx} = 2V	8	10	12.5	kΩ
BOOTSTRAP DIODES						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA			0.8	V
		I_{BOOT} = 100 mA			1.6	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 50 mA	4.5	5.5	9	Ω
LOGIC-LEVEL INPUTS (BRAKE, DIR, EXT_CLK, SCL, SDA, SPEED/WAKE)						
V_{IL}	Input logic low voltage	AVDD = 3 to 3.6 V			0.25*AVDD	V
V_{IH}	Input logic high voltage	AVDD = 3 to 3.6 V	0.65*AVDD			V
V_{HYS}	Input hysteresis		50	500	800	mV
I_{IL}	Input logic low current	AVDD = 3 to 3.6 V	-0.15		0.15	µA
I_{IH}	Input logic high current	AVDD = 3 to 3.6 V	-0.3		0.1	µA
R_{PD_SPEED}	Input pulldown resistance	SPEED/WAKE pin To GND	0.6	1	1.4	MΩ
LOGIC-LEVEL INPUTS (DRVOFF)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2.2			V

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Input hysteresis		200	400	650	mV
I_{IL}	Input logic low current	Pin Voltage = 0 V;	-1	0	1	µA
I_{IH}	Input logic high current	Pin Voltage = 5 V;	7	20	35	µA
R_{PD_DRVOFF}	Input pulldown resistance	DRVOFF To GND	100	200	300	kΩ
OPEN-DRAIN OUTPUTS (nFAULT, FG)						
V_{OL}	Output logic low voltage	I_{OD} =-5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = 3.3 V	0		0.5	µA
SPEED INPUT - ANALOG MODE						
V_{ANA_FS}	Analog full-speed voltage		2.95	3	3.05	V
V_{ANA_RES}	Analog voltage resolution			732		µV

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPEED INPUT - PWM MODE						
f_{PWM}	PWM input frequency		0.01		95	kHz
Res_{PWM}	PWM input resolution	f_{PWM} = 0.01 to 0.35 kHz	11	12	13	bits
		f_{PWM} = 0.35 to 2 kHz	12	13	14	bits
		f_{PWM} = 2 to 3.5 kHz	11	11.5	12	bits
		f_{PWM} = 3.5 to 7 kHz	13	13.5	14	bits
		f_{PWM} = 7 to 14 kHz	12	12.5	13	bits
		f_{PWM} = 14 to 29.2 kHz	11	11.5	12	bits
		f_{PWM} = 29.3 to 60 kHz	10	10.5	11	bits
		f_{PWM} = 60 to 95 kHz	8	9	10	bits
SPEED INPUT - FREQUENCY MODE						
f_{PWM_FREQ}	PWM input frequency range	Duty cycle = 50%	3		32767	Hz
SLEEP MODE						
V_{EN_SL}	Analog voltage to enter sleep mode	SPD_CTRL_MODE = 00b (analog mode)			40	mV
V_{EX_SL}	Analog voltage to exit sleep mode		2.6			V
t_{DET_ANA}	Time needed to detect wake up signal on SPEED/WAKE pin	SPD_CTRL_MODE = 00b (analog mode), $V_{SPEED/WAKE}$ > V_{EX_SL}	0.5	1	1.5	µs
t_{WAKE}	Wakeup time from sleep mode	$V_{SPEED/WAKE}$ > V_{EX_SL} to DVDD voltage available, SPD_CTRL_MODE = 00b (analog mode)		3	5	ms
$t_{EX\_SL\_DR\_ANA}$	Time taken to drive motor after exiting from sleep mode	SPD_CTRL_MODE = 00b (analog mode) $V_{SPEED/WAKE}$ > V_{EX_SL}, ISD detection disabled			30	ms
t_{DET_PWM}	Time needed to detect wake up signal on SPEED pin	SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED/WAKE}$ > V_{IH}	0.5	1	1.5	µs
t_{WAKE_PWM}	Wakeup time from sleep mode	$V_{SPEED/WAKE}$ > V_{IH} to DVDD voltage available and release nFault, SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode)		3	5	ms
$t_{EX\_SL\_DR\_PWM}$	Time taken to drive motor after wakeup from sleep state	SPD_CTRL_MODE = 01b (PWM mode) $V_{SPEED/WAKE}$ > V_{IH}, ISD detection disabled			30	ms
$t_{DET\_SL\_ANA}$	Time needed to detect sleep command	SPD_CTRL_MODE = 00b (analog mode) $V_{SPEED/WAKE}$ < V_{EN_SL}, SLEEP_TIME = 00b or 01b	0.5	1	2	ms

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DET\_SL\_PWM}$	Time needed to detect sleep command	SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), SLEEP_TIME = 00b	0.035	0.05	0.065	ms
		SPD_CTRL_MODE = 01b (PWM mode), or 11b (Frequency mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), SLEEP_TIME = 01b	0.14	0.2	0.26	ms
		SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode) or 00b (analog mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), $V_{SPEED/WAKE}$ < V_{EN_SL} (analog mode), SLEEP_TIME = 10b	14	20	26	ms
		SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode) or 00b (analog mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), $V_{SPEED/WAKE}$ < V_{EN_SL} (analog mode), SLEEP_TIME = 11b	140	200	260	ms
t_{EN_SL}	Time needed to stop driving motor after detecting sleep command	$V_{SPEED/WAKE}$ < V_{EN_SL} (analog mode) or $V_{SPEED/WAKE}$ < V_{IL} (PWM and frequency mode)		1	2	ms

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STANDBY MODE						
$t_{EX\_SB\_DR\_ANA}$	Time taken to drive motor after exiting standby mode	SPD_CTRL_MODE = 00b (analog mode) V_{SPEED} > V_{EN_SB}, ISD detection disabled			6	ms
$t_{EX\_SB\_DR\_PWM}$	Time taken to drive motor after exiting standby mode	SPD_CTRL_MODE = 01b (PWM mode) V_{SPEED} > V_{IH}, ISD detection disabled			6	ms
$t_{DET\_SB\_ANA}$	Time needed to detect standby mode	SPD_CTRL_MODE = 00b (analog mode) V_{SPEED} < V_{EN_SB}	0.5	1	2	ms
$t_{EN\_SB\_PWM}$	Time needed to detect standby command	SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_TIME = 00b	0.035	0.05	0.065	ms
		SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_TIME = 01b	0.14	0.2	0.26	ms
		SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_TIME = 10b	14	20	26	ms
		SPD_CTRL_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_TIME = 11b	140	200	260	ms
$t_{EN\_SB\_DIG}$	Time needed to detect standby mode	SPD_CTRL_MODE = 10b (I2C mode), SPEED_CMD = 0		1	2	ms
t_{EN_SB}	Time needed to stop driving motor after detecting standby command	V_{SPEED} < V_{EN_SL} (analog mode) or V_{SPEED} < V_{IL} (PWM mode) or SPEED command = 0 (I2C mode)		1	2	ms
OSCILLATOR						
SL_{ACC}	Speed loop accuracy	T_J = -25 to 125 ºC .	-2.25		2.25	%
f_{OSCREF}	External clock reference	EXT_CLK_CONFIG = 000b		8		kHz
		EXT_CLK_CONFIG = 001b		16		kHz
		EXT_CLK_CONFIG = 010b		32		kHz
		EXT_CLK_CONFIG = 011b		64		kHz
		EXT_CLK_CONFIG = 100b		128		kHz
		EXT_CLK_CONFIG = 101b		256		kHz
		EXT_CLK_CONFIG = 110b		512		kHz
		EXT_CLK_CONFIG = 111b		1024		kHz
PROTECTION CIRCUITS						
V_{VREG_UVLO}	Regulator input undervoltage lockout (VREG-UVLO)	Supply rising	1.8	1.9	2	V
		Supply falling	1.7	1.8	1.9	V
$V_{VREG\_UVLO\_HYS}$	Regulator UVLO hysteresis	Rising to falling threshold	30	100	160	mV
$t_{VREG\_UVLO\_DEG}$	Regulator UVLO deglitch time			5		µs
V_{DVDD_UVLO}	Digital regulator undervoltage lockout (DVDD-UVLO)	Supply rising	1.2	1.25	1.32	V
V_{DVDD_UVLO}	Digital regulator undervoltage lockout (DVDD-UVLO)	Supply falling	1.25	1.35	1.45	V
V_{PVDD_UV}	PVDD undervoltage lockout threshold	V_{PVDD} rising	4.3	4.4	4.5	V
		V_{PVDD} falling	4	4.1	4.25	
$V_{PVDD\_UV\_HYS}$	PVDD undervoltagelockout hysteresis	Rising to falling threshold	225	265	325	mV
$t_{PVDD\_UV\_DG}$	PVDD undervoltage deglitch time		10	20	30	µs

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD_POR}	AVDD supply POR threshold	AVDD rising	2.7	2.85	3.0	V
		AVDD falling	2.5	2.65	2.8	
$V_{AVDD\_POR\_HYS}$	AVDD POR hysteresis	Rising to falling threshold	170	200	250	mV
$t_{AVDD\_POR\_DG}$	AVDD POR deglitch time		7	12	22	µs
V_{GVDD_UV}	GVDD undervoltage threshold	V_{GVDD} rising	7.3	7.5	7.8	V
		V_{GVDD} falling	6.4	6.7	6.9	V
$V_{GVDD\_UV\_HYS}$	GVDD undervoltage hysteresis	Rising to falling threshold	800	900	1000	mV
$t_{GVDD\_UV\_DG}$	GVDD undervoltage deglitch time		5	10	15	µs
V_{BST_UV}	Bootstrap undervoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} rising	3.9	4.45	5	V
		V_{BSTx}- V_{SHx}; V_{BSTx} falling	3.7	4.2	4.8	V
$V_{BST\_UV\_HYS}$	Bootstrap undervoltage hysteresis	Rising to falling threshold	150	220	285	mV
$t_{BST\_UV\_DG}$	Bootstrap undervoltage deglitch time		2	4	6	µs
V_{DS_LVL}	V_{DS} overcurrent protection threshold Reference	SEL_VDS_LVL = 0000	0.04	0.06	0.08	V
		SEL_VDS_LVL = 0001	0.09	0.12	0.15	V
		SEL_VDS_LVL = 0010	0.14	0.18	0.23	V
		SEL_VDS_LVL = 0011	0.19	0.24	0.29	V
		SEL_VDS_LVL = 0100	0.23	0.3	0.37	V
		SEL_VDS_LVL = 0101	0.3	0.36	0.43	V
		SEL_VDS_LVL = 0110	0.35	0.42	0.5	V
		SEL_VDS_LVL = 0111	0.4	0.48	0.56	V
		SEL_VDS_LVL = 1000	0.5	0.6	0.7	V
		SEL_VDS_LVL = 1001	0.65	0.8	0.9	V
		SEL_VDS_LVL = 1010	0.85	1	1.15	V
		SEL_VDS_LVL = 1011	1	1.2	1.34	V
		SEL_VDS_LVL = 1100	1.2	1.4	1.58	V
		SEL_VDS_LVL = 1101	1.4	1.6	1.78	V
		SEL_VDS_LVL = 1110	1.6	1.8	2	V
		SEL_VDS_LVL = 1111	1.7	2	2.2	V
V_{SENSE_LVL}	V_{SENSE} overcurrent protection threshold	LSS to GND pin = 0.5V	0.48	0.5	0.52	V
t_{DS_BLK}	V_{DS} overcurrent protection blanking time		0.5	1	2.7	µs
t_{DS_DG}	V_{DS} and V_{SENSE} overcurrent protection deglitch time		1.5	3	5	µs
$t_{SD\_SINK\_DIG}$	DRVOFF peak sink current duration		3	5	7	µs
t_{SD_DIG}	DRVOFF digital shutdown delay		0.5	1.5	2.2	µs
t_{SD}	DRVOFF analog shutdown delay		7	14	21	µs
T_{OTSD}	Thermal shutdown temperature	T_J rising;	160	170	187	°C
T_{HYS}	Thermal shutdown hysteresis		16	20	23	°C
I^2C Serial Interface						
V_{I2C_L}	LOW-level input voltage		-0.5		0.3*AVDD	V
V_{I2C_H}	HIGH-level input voltage		0.7*AVDD		5.5	V
V_{I2C_HYS}	Hysterisis		0.05*AVDD			V
V_{I2C_OL}	LOW-level output voltage	open-drain at 2mA sink current	0		0.4	V

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{I2C_OL}	LOW-level output current	V_{I2C_OL} = 0.6V			6	mA
I_{I2C_IL}	Input current on SDA and SCL		-10(1)		10(1)	µA
C_i	Capacitance for SDA and SCL				10	pF
t_{of}	Output fall time from V_{I2C_H}(min) to V_{I2C_L}(max)	Standard Mode			250(2)	ns
		Fast Mode			250(2)	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast Mode	0		50(3)	ns
EEPROM						
EE_{Prog}	Programing voltage		1.35	1.5	1.65	V
EE_{RET}	Retention	T_A = 25 ℃		100		Years
		T_J = -40 to 150 ℃	10			Years
EE_{END}	Endurance	T_J = -40 to 150 ℃	1000			Cycles
		T_J = -40 to 85 ℃	20000			Cycles

(1) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.
(2) The maximum tf for the SDA and SCL bus lines (300 ns) is longer than the specified maximum tof for the output stages (250 ns). This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
(3) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns

6.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Standard-mode						
f_{SCL}	SCL clock frequency		0		100	kHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock		4.7			µs
t_{HIGH}	HIGH period of the SCL clock		4			µs
t_{SU_STA}	Set-up time for a repeated START condition		4.7			µs
t_{HD_DAT}	Data hold time (1)	I2C bus devices	0 (2)		(3)	µs
t_{SU_DAT}	Data set-up time		250			ns
t_r	Rise time for both SDA and SCL signals				1000	ns
t_f	Fall time of both SDA and SCL signals (2) (5) (6) (7)				300	ns
t_{SU_STO}	Set-up time for STOP condition		4			µs
t_{BUF}	Bus free time between STOP and START condition		4.7			µs
C_b	Capacitive load for each bus line (8)				400	pF
t_{VD_DAT}	Data valid time (9)				3.45 (3)	µs
t_{VD_ACK}	Data valid acknowledge time (10)				3.45 (3)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V
Fast-mode						
f_{SCL}	SCL clock frequency		0		400	KHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6			µs

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD_DAT}	Data hold time (1)		0 (2)		(3)	µs
t_{SU_DAT}	Data set-up time		100 (4)			ns
t_r	Rise time for both SDA and SCL signals		20		300	ns
t_f	Fall time of both SDA and SCL signals (2) (5) (6) (7)		20 x (AVDD/ 5.5V)		300	ns
t_{SU_STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between STOP and START condition		1.3			µs
C_b	Capacitive load for each bus line (8)				400	pF
t_{VD_DAT}	Data valid time (9)				0.9 (3)	µs
t_{VD_ACK}	Data valid acknowledge time (10)				0.9 (3)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVD D			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVD D			V

(1) t_{HD_DAT} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(2) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(3) The maximum t_{HD_DAT} could be 3.45 µs and .9 µs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_DAT} or t_{VD_ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
(4) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + t_{SU_DAT} = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
(5) If mixed with HS-mode devices, faster fall times according to Table 10 are allowed.
(6) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(7) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
(8) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
(9) t_{VD_DAT} = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(10) t_{VD_ACK} = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, dependging on which one is worse).

6.7 Typical Characteristics

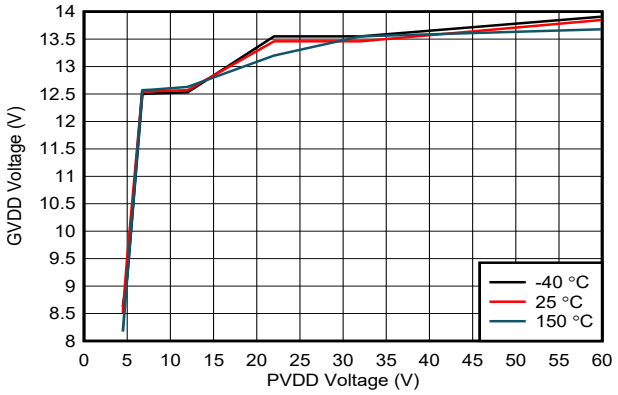


Figure 6-1. GVDD Voltage over PVDD Voltage

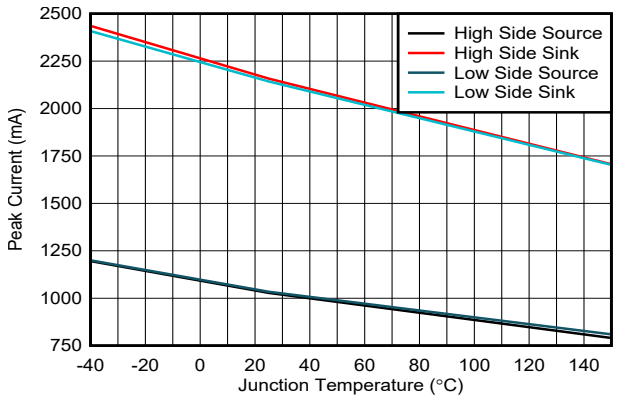


Figure 6-2. Driver Peak Current over Junction Temperature

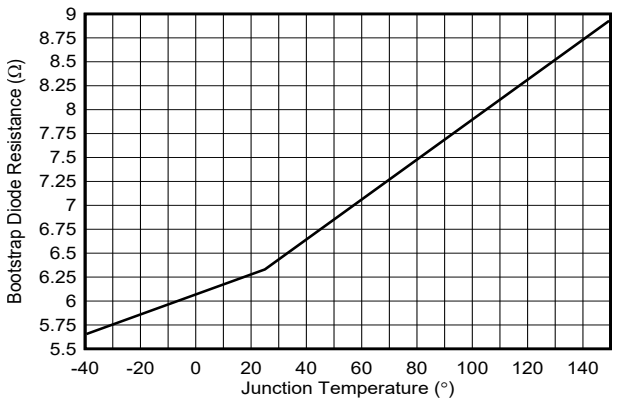


Figure 6-3. Bootstrap Diode Resistance over Junction Temperature

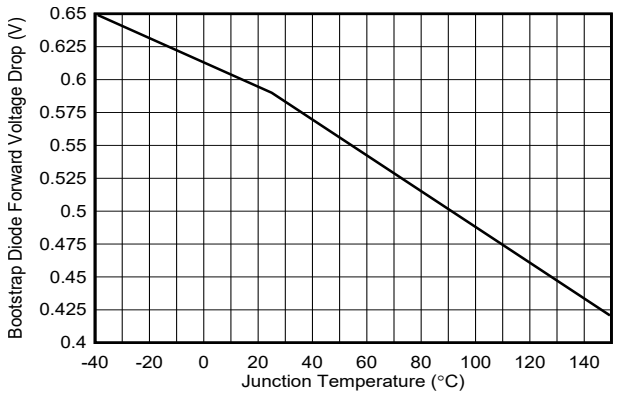


Figure 6-4. Bootstrap Diode Forward Voltage Drop over Junction Temperature

7 Detailed Description

7.1 Overview

The MCT8329A provides a code-free sensorless trapezoidal control solution with integrated three phase gate driver for applications requiring high speed operation (up to 3 kHz electrical speed) or very fast startup time (< 50ms) for brushless-DC motors.

The devices provide three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. Motor current is sensed using an integrated current sensing amplifier with the need of an external low side sense resistor. The device integrates an LDO that generate the necessary voltage rails for the device and can be used to power external circuits.

Sensorless trapezoidal control is highly configurable through register settings ranging from motor start-up behavior to closed loop operation. Register settings can be stored in non-volatile EEPROM (MCT8329A1I), which allows the device to operate stand-alone once it has been configured. MCT8329A1I allows for a high level of monitoring; any variable in the algorithm can be displayed and observed as an analog output through a 12-bit DAC. This feature provides an effective method to tune speed loops as well as motor acceleration. The device receives a speed command through a PWM input, analog voltage, frequency input or I^2C command.

In-built protection features include power-supply undervoltage lockout (PVDD_UVLO), regulator undervoltage lockout (GVDD_UV), bootstrap voltage undervoltage lockout (BST_UV), VDS overcurrent protection (OCP), Sense resistor overcurrent protection (SEN_OCP), motor lock detection and overtemperature shutdown (OTSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the status registers.

A standard I^2C provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller.

The MCT8329A device is available in a 0.4-mm pin pitch, VQFN surface-mount package. The VQFN package size is 5 mm × 4 mm.

7.2 Functional Block Diagram

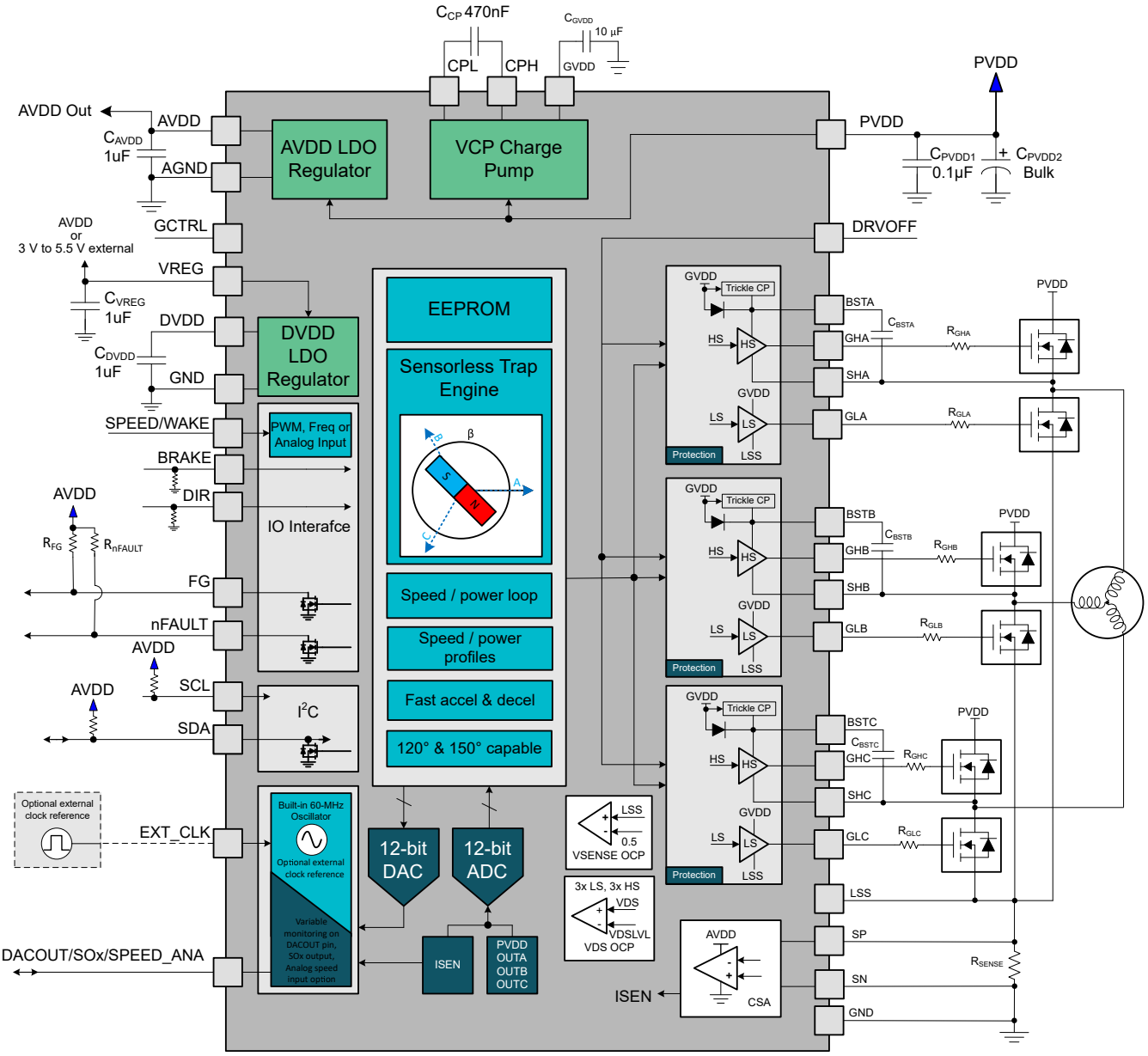


Figure 7-1. MCT8329A Functional Block Diagram

7.3 Feature Description

Table 7-1 lists the recommended values of the external components for the driver.

Table 7-1. MCT8329A External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{PVDD1}	PVDD	PGND	X5R or X7R, 0.1-µF, >2x PVDD-rated capacitor
C_{PVDD2}	PVDD	PGND	≥ 10 µF, >2x PVDD-rated bulk capacitor
C_{CP}	CPH	CPL	X5R or X7R, 470-nF, PVDD-rated capacitor
C_{AVDD}	AVDD	AGND	X5R or X7R, ≥1-µF, 6.3-V capacitor
C_{GVDD}	GVDD	GND	X5R or X7R, ≥10-uF, 30-V-rated capacitor
C_{DVDD}	DVDD	GND	X5R or X7R, 1-µF, ≥ 4-V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.6-µF to 1.3-µF at 1.5-V across operating temperature.
C_{VREG}	VREG	GND	X5R or X7R, ≥1-µF, 10-V capacitor
C_{BSTx}	BSTx	SHx	X5R or X7R, 1-µF (typical), 25-V-rated capacitor
R_{nFAULT}	1.8 to 5 V Supply	nFAULT	5.1-kΩ, Pullup resistor
R_{FG}	1.8 to 5 V Supply	FG	5.1-kΩ, Pullup resistor
R_{SDA}	1.8 to 5 V Supply	SDA	5.1-kΩ, Pullup resistor
R_{SCL}	1.8 to 5 V Supply	SCL	5.1-kΩ, Pullup resistor
R_{BRAKE}	BRAKE	GND	Optional <100-kΩ resistor for better noise immunity, if BRAKE pin is used
R_{DIR}	DIR	GND	Optional <100-kΩ resistor for better noise immunity, if DIR pin is used

Note

For FG and nFAULT pins, the external pull up resistors needs to be connected even if the pin functionality is not used. The FG and nFAULT pins needs to be pulled high prior to device entering active state if external supply is used for pull up.

7.3.1 Three Phase BLDC Gate Drivers

The MCT8329A device integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A charge pump is used to generate the GVDD to supply the correct gate bias voltage across a wide operating voltage range. The low side gate outputs are driven directly from GVDD, while the high side gate outputs are driven using a bootstrap circuit with an integrated diode, and an internal trickle charge pump provides support for 100% duty cycle operation.

7.3.2 Gate Drive Architecture

The gate driver device use a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate drivers are supplied directly from the GVDD regulator supply. For the high-side gate drivers a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used on the BSTx pin. To support 100% duty cycle control, a trickle charge pump is integrated into the device. The trickle charge pump is connected to the BSTx node to prevent voltage drop due to the leakage currents of the driver and external MOSFET.

The high-side gate driver has semi-active pull down and low side gate has passive pull down to help prevent the external MOSFET from turning ON during sleep state or when power supply is disconnected.

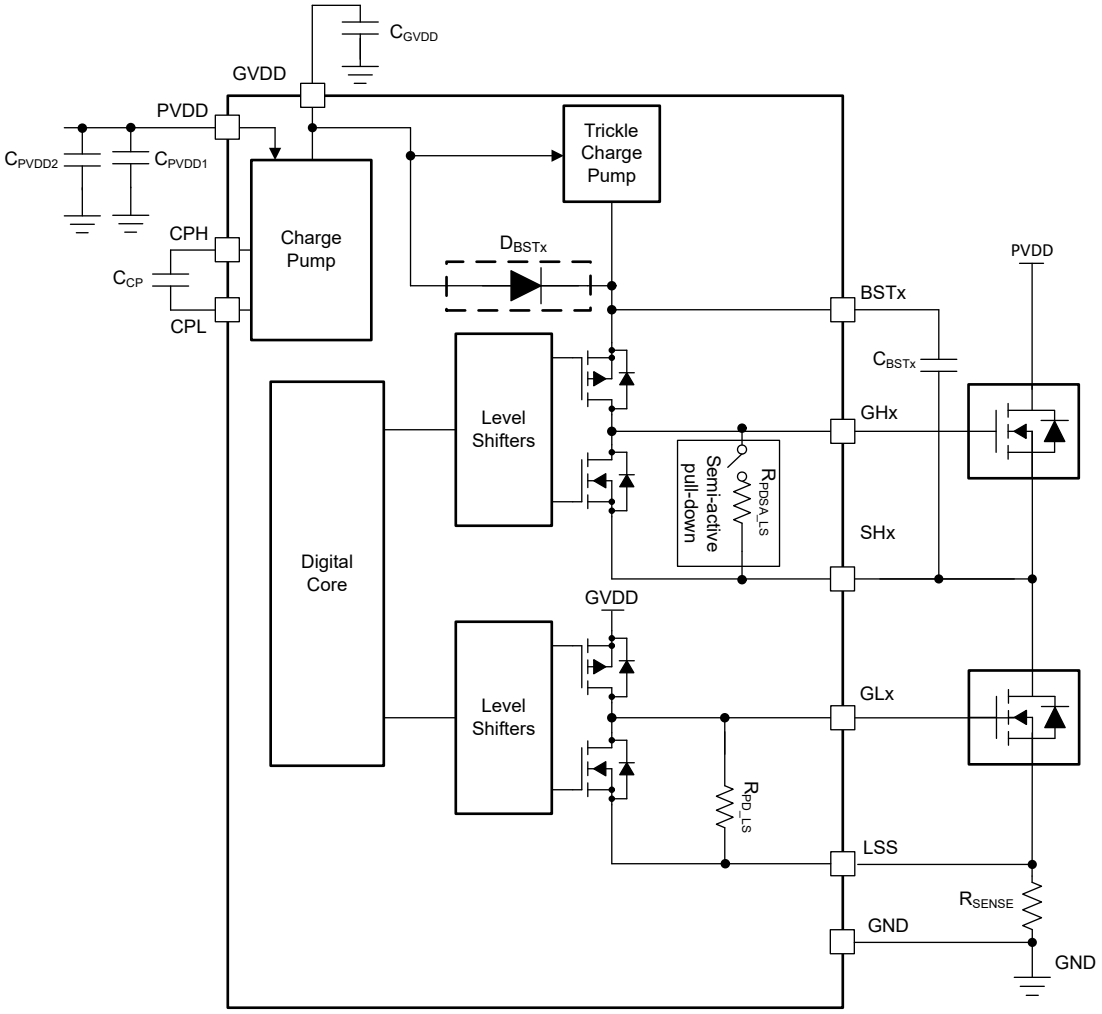


Figure 7-2. Gate Driver Block Diagram

7.3.2.1 Dead time and Cross Conduction Prevention

The MCT8329A provide digital dead time insertion between the high side and low side PWM signals, to prevent both external MOSFETs of each half-bridge from switching on at the same time. Digital dead time can be adjusted between 50 ns and 1000 ns by configuring EEPROM register DIG_DEAD_TIME.

7.3.3 AVDD Linear Voltage Regulator

A 3.3-V, 80-mA linear regulator is integrated into the MCT8329A and is available for use by external circuitry. If VREG is connected to AVDD, then only 50 mA is available for use by external circuitry. The output of the LDO is fixed to 3.3-V. This regulator can provide the supply voltage for a low-power MCU or other circuitry with low supply current needs. The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed back to the AGND pin.

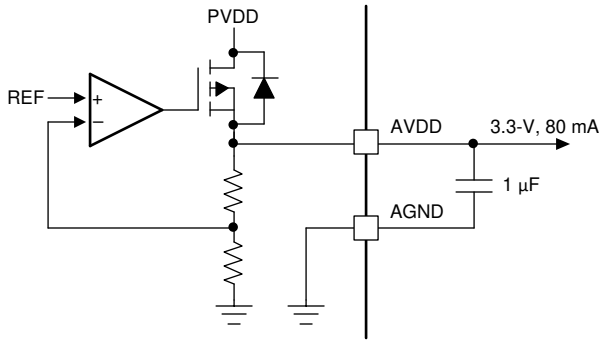


Figure 7-3. AVDD Linear Regulator Block Diagram

The power dissipated in the device by the AVDD linear regulator can be calculated as Equation 1:

$$P = (V_{PVDD} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{PVDD} of 24-V, drawing 20-mA out of AVDD results in a power dissipation as shown in Equation 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (2)$$

7.3.4 DVDD Voltage Regulator

VREG pin is used as the supply input for the integrated DVDD voltage regulator. There are several options available for providing supply voltage to VREG pin, either an external 3 V to 5.5V supply (30mA source) can be used or AVDD can be connected to VREG or an external MOSFET controlled by GCTRL pin can be used.

7.3.4.1 AVDD Powered VREG

When neither external MOSFET regulator nor external supply is used, connect AVDD to VREG pin (see Figure 7-4). In this mode digital circuitry which are connected to DVDD will be powered using AVDD. In this mode capability AVDD of supporting external load will be reduced to 50 mA.

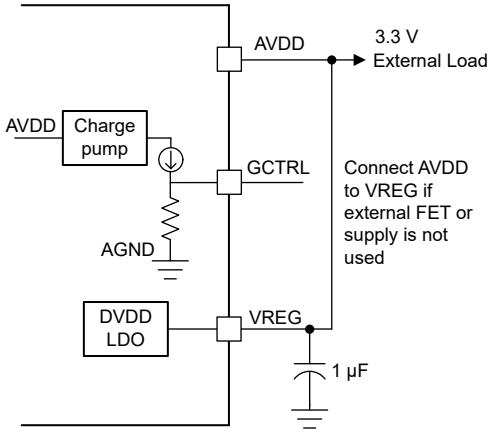


Figure 7-4. AVDD Powering VREG

7.3.4.2 External Supply for VREG

MCT8329A provides provision to connect the external supply voltage to VREG pin (see Figure 7-5). In this mode GCTRL pin should be left floating and external regulator is connected to VREG pin. When external MOSFET or external supply is used to power DVDD then maximum external load supported by AVDD is 80 mA

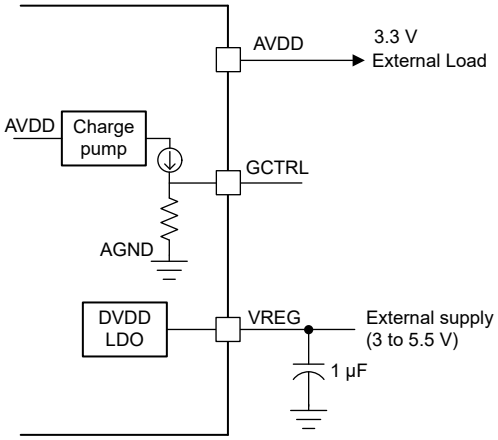


Figure 7-5. External Supply for VREG

7.3.4.3 External MOSFET for VREG Supply

MCT8329A provides option to drive external MOSFET which can act as regulator and can be used to power internal digital circuitry through VREG pin (see Section 7.3.4.3. In this case VREG must not be connected to AVDD or external 3.3V/5V power supply. This option of connecting external MOSFET can be used to reduce power dissipation in MCT8329A and transfer the power loss to the external MOSFET, for use cases that have thermal challenges.

The $V_{GS(th)}$ of external MOSFET has to be selected to ensure that the VREG voltage is between 2.2V to 5.5V across operating conditions. Refer Section 8.2.1for application example design calculations. The input capacitance of external MOSFET need to be less than 2nF to meet startup time $_{EX\_SL\_DR\_ANA}$(Analog input) or $t_{EX\_SL\_DR\_PWM}$ (PWM input).

Note

The GCTRL pin is a high impedance node (> 1MΩ) and this pin should not be loaded externally other than the external MOSFET gate and C_{GCTRL}. External loading on GCTRL pin (to GND) reduces the voltage at GCTRL pin and VREG pin.

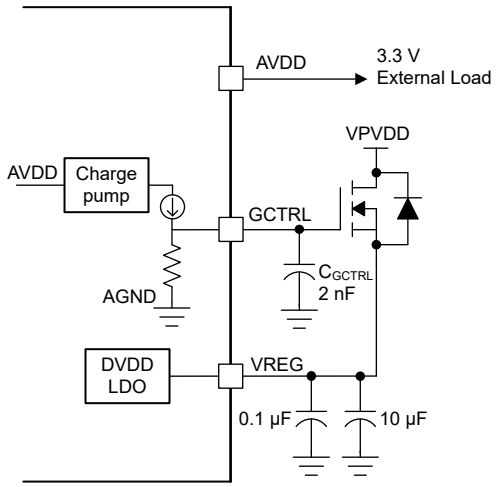


Figure 7-6. External MOSFET Voltage Regulator for VREG

7.3.5 Low-Side Current Sense Amplifier

MCT8329A integrates a high-performance low-side current sense amplifier for current measurements using low-side shunt resistor. Low-side current measurements are used for multiple control features and protections in MCT8329A. The current sense amplifiers features configurable gain (5 V/V, 10 V/V, 20 V/V, and 40 V/V) through

EEPROM setting. The current sene amplifier can support sensing bidirectional or unidirection current through the low-side shunt resistor by configuring the EEPROM bit VREF_SEL.

In bidirectional current sense mode MCT8329A internally generates common mode voltage of V_{REF}/2 to obtain maximum resolution for current measurement for both the direction of current. V_{REF} is an internally generated reference voltage having a typical value of 3 V.

Use Equation 3 to design the value of the shunt resistor (R_{SENSE}) connected between SP and SN, in bidirectional current sense mode, for the range of current (I) through the low side single shunt and the selected current sense amplifier gain configured by EEPROM bits CSA_GAIN.

$$R_{SENSE} = \frac{V_{SO} - \frac{V_{REF}}{2}}{CSA\_GAIN \times I} \quad (3)$$

In unidirectional current sense mode MCT8329A internally generates common mode voltage of V_{REF}/8 to obtain maximum resolution for current measurement for current direction from SP to SN.

Use Equation 4 to calculate the current through the shunt resistor (R_{SENSE}) connected between SP and SN, in unidirectional current sense mode.

$$R_{SENSE} = \frac{V_{SO} - \frac{V_{REF}}{8}}{CSA\_GAIN \times I} \quad (4)$$

Note

In unidirectional and bidirectional currrent sense mode, TI recommends to design the shunt resistor R_{SENSE}value to limit the current sense amplifier output voltage (V_{SO}) between 0.25 V and 3 V across the operating range of low side single shunt resistor current (I) at the selected gain of CSA_GAIN. Appropriately size the shunt resistor power rating based on the I^2R_{SENSE} losses with sufficient margin.

7.3.6 Device Interface Modes

The MCT8329A family of devices support I^2C interface to provide end application design suited for either flexibility or simplicity. Along with the I^2C interface the device support I/O pins like FG, nFAULT, DIR, BRAKE, SPEED/WAKE, DACOUT/SOx/SPEED_ANA, EXT_CLK, DRVOFF.

7.3.6.1 Interface - Control and Monitoring

Motor Control and I/O Signals

- **BRAKE**: When BRAKE pin is driven 'High', MCT8329A enters brake state. Low-side braking (see Low-Side Braking) is implemented during this brake state. MCT8329A decreases output speed to value defined by BRAKE_DUTY_THRESHOLD before entering brake state. As long as BRAKE is driven 'High', MCT8329A stays in brake state. Brake pin input can be overwritten by configuring BRAKE_INPUT over the I^2C interface.
- **DIR**: The DIR pin decides the direction of motor spin; when driven 'High', the sequence is OUTA → OUTC → OUTB, and when driven 'Low' the sequence is OUTA → OUTB → OUTC. DIR pin input can be overwritten by configuring DIR_INPUT over the I^2C interface.
- **DRVOFF**: When DRVOFF pin is driven 'High', MCT8329A turns off all external MOSFETs by putting the gate drivers into the pull-down state. When DRVOFF is driven 'Low', MCT8329A returns to normal state of operation, as if restarting the motor. DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active. Entry and exit from sleep or standby condition is controlled by SPEED/WAKE pin.
- **SPEED/WAKE**: The SPEED/WAKE pin is used to control motor speed (or power or voltage) and wake up MCT8329A from sleep mode. SPEED/WAKE pin can be configured to accept PWM, frequency or analog control input signals. The pin is used to enter and exit from sleep and standby mode (see Table 7-3).
- **DACOUT/SOx/SPEED_ANA**: The DACOUT/SOx/SPEED_ANA pin provides a multiplexed functionality and the pin can be configured as a DACOUT output pin or current sense amplifier output pin or as speed (or power or open loop voltage) control analog input pin. With the pin DACOUT/SOx/SPEED_ANA configured as DACOUT, the device allows monitoring of algorithm variables, speed etc (see Section 7.5.2) . With the pin DACOUT/SOx/SPEED_ANA configured as SOx, the device allows monitoring of integrated current sense

amplifier output (V_{SOx}). With the pin DACOUT/SOx/SPEED_ANA configured as SPEED_ANA enable the user to give analog control input for speed or power or voltage through the DACOUT/SOx/SPEED_ANA pin and in that case the SPEED/WAKE pin can be used as an independent speed or standby control input pin. The pin functionality can be configured through EEPROM register bit DAC_SOX_ANA_CONFIG.

- **EXT_CLK**: The EXT_CLK pin can be used to provide an external clock reference and in that case the internal clock gets calibrated using the external clock.
- **FG**: The FG pin provides pulses which are proportional to motor speed (see Section 7.3.19).
- **nFAULT**: The nFAULT pin provides fault status in device or motor operation.

7.3.6.2 I²C Interface

The MCT8329A supports an I²C serial communication interface that allows an external controller to send and receive data. This I²C interface lets the external controller configure the EEPROM and read detailed fault and motor state information. The I²C bus is a two-wire interface using the SCL and SDA pins which are described as follows:

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

7.3.7 Motor Control Input Options

The MCT8329A offers three ways of controlling the motor:

1. SPEED Control: In speed control mode, the speed of the motor is controlled using a closed loop PI control according to the input reference.
2. POWER Control: In power control mode, the DC input power of the inverter power stage is controlled using a closed loop PI control according to the input reference.
3. VOLTAGE Control: In voltage control mode, the voltage applied to the motor is controlled according to the input reference.

The MCT8329A offers four methods of directly controlling the reference input of the motor. The reference control method is configured by SPD_CTRL_MODE.

The reference (speed or power or voltage) input command can be controlled in one of the following four ways.

- PWM input on SPEED/WAKE pin by varying duty cycle of input signal
- Frequency input on SPEED/WAKE pin by varying frequency of input signal
- Analog input on SPEED/WAKE pin or DACOUT/SOx/SPEED_ANA pin by varying amplitude of input signal
- Over I^2C by configuring SPEED_CTRL

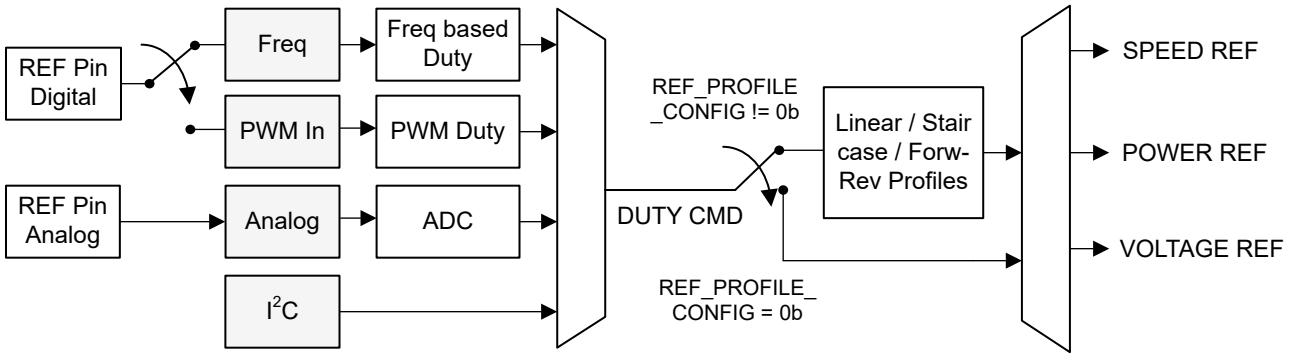


Figure 7-7. Multiplexing the Reference Input Command

The signal path from REF (SPEED/WAKE or DACOUT/SOx/SPEED_ANA) pin input (or I^2C based input) to output reference is shown in Figure 7-7. User has the option to use the REF pin full resolution values as DUTY CMD to derive the SPEED or POWER or VOLTAGE reference. User also has the option to insert different profiles (linear- or staircase- or Bi-Directoional-) before deriving the SPEED or POWER or VOLTAGE reference. The selection can be made by configuring REF_PROFILE_CONFIG.

7.3.7.1 Analog-Mode Motor Control

Analog input based motor control can be configured by setting SPD_CTRL_MODE to 00b. In this mode, the duty command (DUTY CMD) varies with the analog voltage input (V_{SPEED}) on the SPEED/WAKE pin or DACOUT/SOx/SPEED_ANA pin (configurable via DAC_SOX_ANA_CONFIG) V_{SPEED}. When $0 < V_{SPEED} < V_{EN\_SB}$, DUTY CMD is set to zero and the motor is stopped. When $V_{EN\_SB} < V_{SPEED} < V_{ANA\_FS}$, DUTY CMD varies linearly with V_{SPEED} as shown in Figure 7-8 . When $V_{SPEED} > V_{ANA\_FS}$, DUTY CMD is clamped to 100%.

With DACOUT/SOx/SPEED_ANA pin used as the analog control input, the SLEEP/WAKE pin can be independently used to control the sleep or standby entry and exit as described in Table 7-3

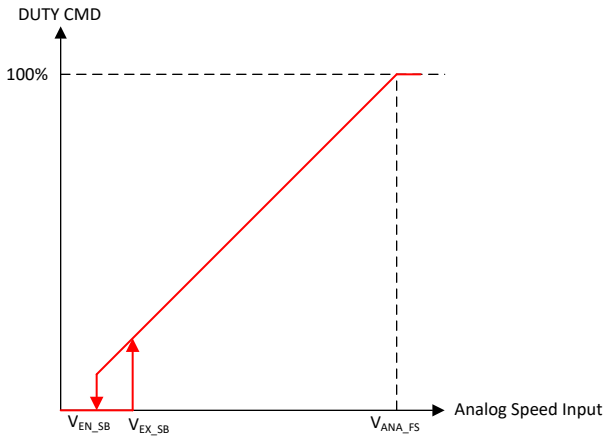


Figure 7-8. Analog-Mode Speed Control

7.3.7.2 PWM-Mode Motor Control

PWM based speed control can be configured by setting SPD_CTRL_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED/WAKE pin can be varied from 0 to 100% and duty command (DUTY CMD) varies linearly with the applied PWM duty cycle. DUTY CMD is set to zero and the motor is stopped when the PWM signal at SPEED pin stays < V_{IL} for longer than $t_{EN\_SB\_PWM}$. The frequency of the PWM input signal applied to the SPEED pin is defined as f_{PWM} and the range for this frequency can be configured through SPD_PWM_RANGE_SELECT.

Note

f_{PWM} is the frequency of the PWM signal the device can accept at SPEED/WAKE pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM_FREQ_OUT (see Section 7.3.14).

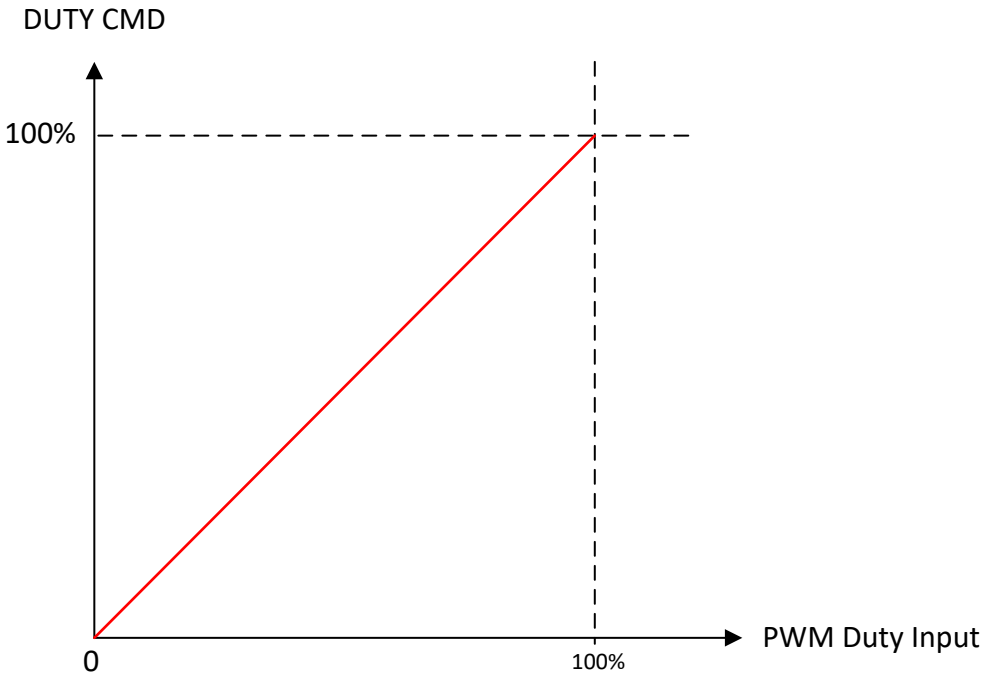


Figure 7-9. PWM-Mode Speed Control

7.3.7.3 Frequency-Mode Motor Control

Frequency based speed control is configured by setting SPD_CTRL_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at SPEED/WAKE pin as given in Equation 5. Input frequency greater than INPUT_MAX_FREQUENCY clamps the duty command to 100%. The duty command is set to zero and the motor is stopped when the frequency signal at SPEED pin stays < V_{IL} for longer than $t_{EN\_SB\_FREQ}$.

Duty command = Frequency at SPEED pin / INPUT_MAX_FREQUENCY * 100 (5)

7.3.7.4 I^2C based Motor Control

I^2C based serial interface can be used for speed control by setting SPD_CTRL_MODE to 10b. In this mode, the duty command can be written directly into SPEED_CTRL. The sleep entry and exit is controlled through SLEEP/WAKE as described in Table 7-3.

7.3.7.5 Input Control Signal Profiles

MCT8329A supports three different kinds of profiles (linear, step, forward-reverse) to input control reference signal to enable a variety of end-user applications. The input control reference signal can be motor speed, DC input power or motor voltage (motor PWM duty cycle) as configured by CLOSED_LOOP_MODE and CONST_POWER_MODE. The different profiles can be configured through REF_PROFILE_CONFIG. When REF_PROFILE_CONFIG is set to 00b, the profiler is not applied and the input reference is same as the duty command as explained in Section 7.3.7.6.

In speed control mode, the profiler output REF_X corresponds to percentage of Maximum Speed (configured by MAX_SPEED) as shown in Equation 6. In power control mode, the profiler output REF_X corresponds to percentage of Maximum Power (configured by MAX_POWER) as shown in Equation 7. In voltage control mode REF_X corresponds to the percentage of PWM duty cycle of applied voltage to the motor.

$$SPEED\ REF(Hz) = \frac{REF\_X}{255} \times Maximum\ Speed\ (Hz) \quad (6)$$

$$POWER\ REF(W) = \frac{REF\_X}{255} \times Maximum\ Power\ \left(W\right) \quad (7)$$

7.3.7.5.1 Linear Control Profiles

Note

For all types of control profiles, duty command = 0 stops the motor irrespective of the reference profile register settings.

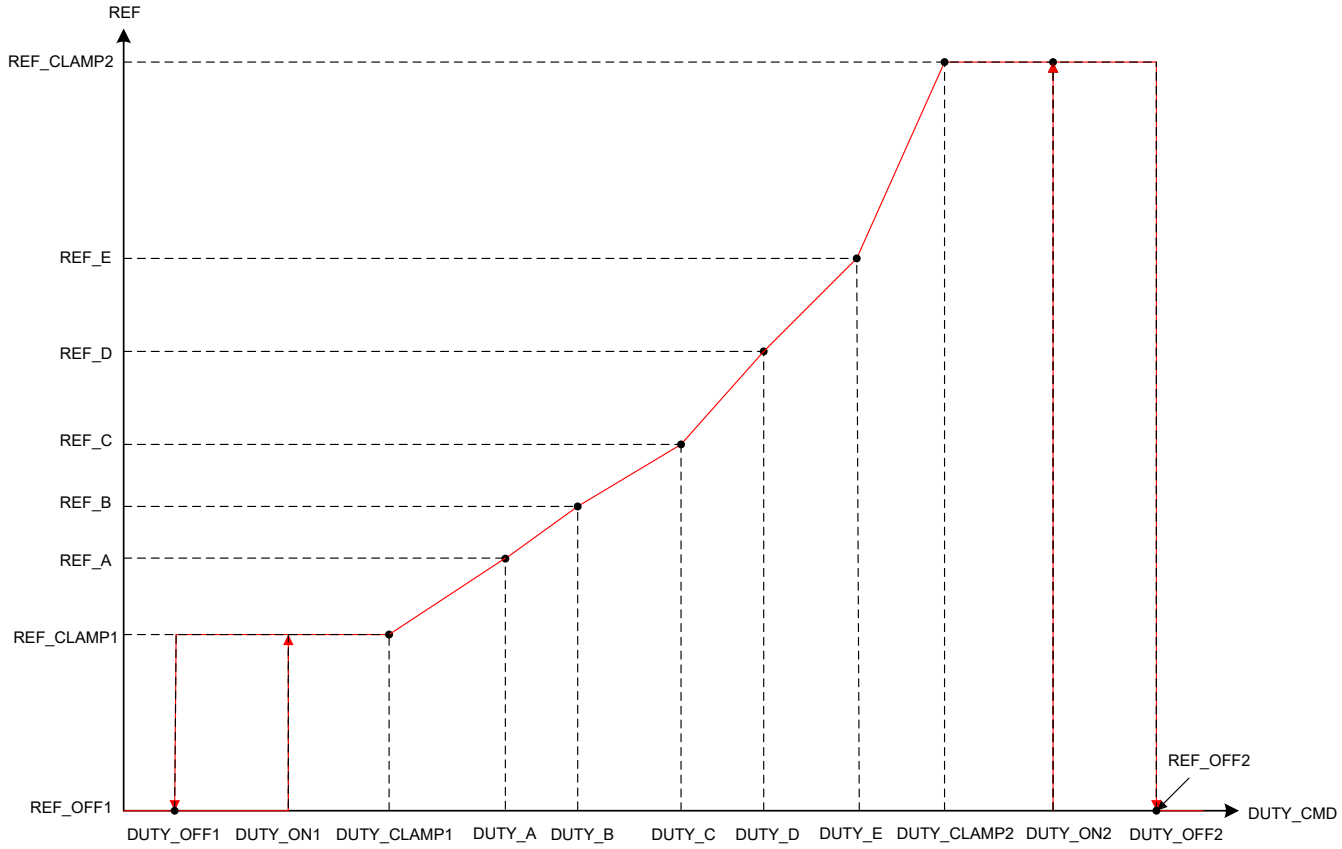


Figure 7-10. Linear Control Profiles

Linear control profiles can be configured by setting REF_PROFILE_CONFIG to 01b. Linear profiles feature input control references which change linearly between REF_CLAMP1 and REF_CLAMP2 with different slopes which can be set by configuring DUTY_x and REF_x combination.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 7-10.
- DUTY_CLAMP1 configures the duty command till which reference will be constant with a value REF_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. The reference changes from REF_CLAMP1 to REF_A linearly between DUTY_CLAMP1 and DUTY_A. DUTY_A to DUTY_E has to be in the same order as shown in Figure 7-10.
- DUTY_B configures the duty command for reference REF_B. The reference changes linearly between DUTY_A and DUTY_B.
- DUTY_C configures the duty command for reference REF_C. The reference changes linearly between DUTY_B and DUTY_C.
- DUTY_D configures the duty command for reference REF_D. The reference changes linearly between DUTY_C and DUTY_D.
- DUTY_E configures the duty command for reference REF_E. The reference changes linearly between DUTY_D and DUTY_E.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2 . The reference changes linearly between DUTY_E and DUTY_CLAMP2. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.
- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 7-10.

- DUTY_OFF2 configures the duty command above which the reference will change from REF_CLAMP2 to REF_OFF2.

7.3.7.5.2 Staircase Control Profiles

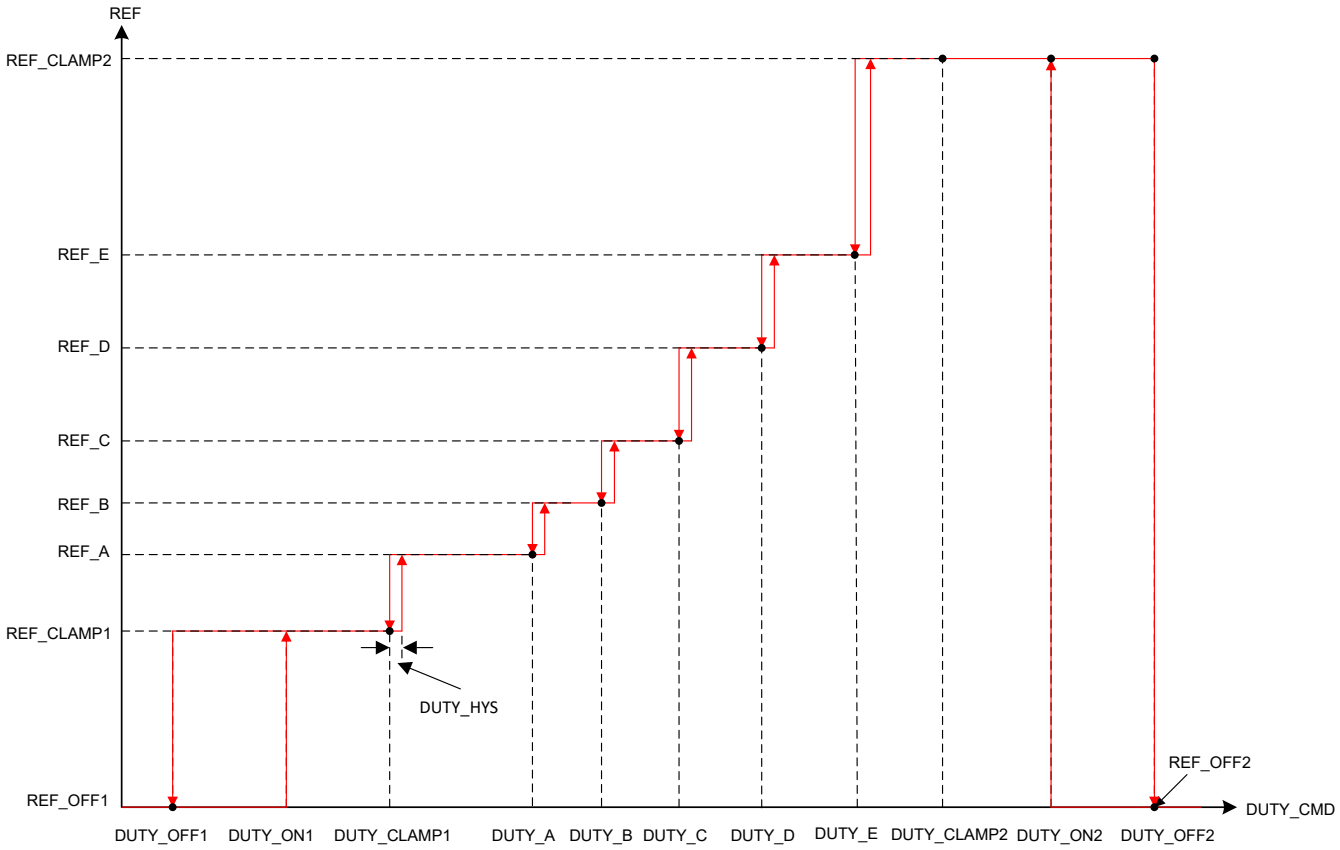


Figure 7-11. Staircase Control Profiles

Staircase control profiles can be configured by setting REF_PROFILE_CONFIG to 10b. Staircase profiles feature input control reference changes in steps between REF_CLAMP1 and REF_CLAMP2, by configuring DUTY_x and REF_x.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 7-11.
- DUTY_CLAMP1 configures the duty command till which reference will be constant. REF_CLAMP1 configures this constant reference between DUTY_OFF1 and DUTY_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. There is a step change in reference from REF_CLAMP1 to REF_A at DUTY_CLAMP1. DUTY_A to DUTY_E has to be in the same order as shown in Figure 7-11.
- DUTY_B configures the duty command for reference REF_B. There is a step change in reference from REF_A to REF_B at DUTY_A.
- DUTY_C configures the duty command for reference REF_C. There is a step change in reference from REF_B to REF_C at DUTY_B.
- DUTY_D configures the duty command for reference REF_D. There is a step change in reference from REF_C to REF_D at DUTY_C.
- DUTY_E configures the duty command for reference REF_E. There is a step change in reference from REF_D to REF_E at DUTY_D.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2. There is

a step change in reference from REF_E to REF_CLAMP2 at DUTY_E. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.

- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 7-11.
- DUTY_OFF2 configures the duty command above which the reference will change from REF_CLAMP2 to REF_OFF2.
- DUTY_HYS configures the hysteresis during every step change at DUTY_CLAMP1, DUTY_A to DUTY_E.

7.3.7.5.3 Forward-Reverse Profiles

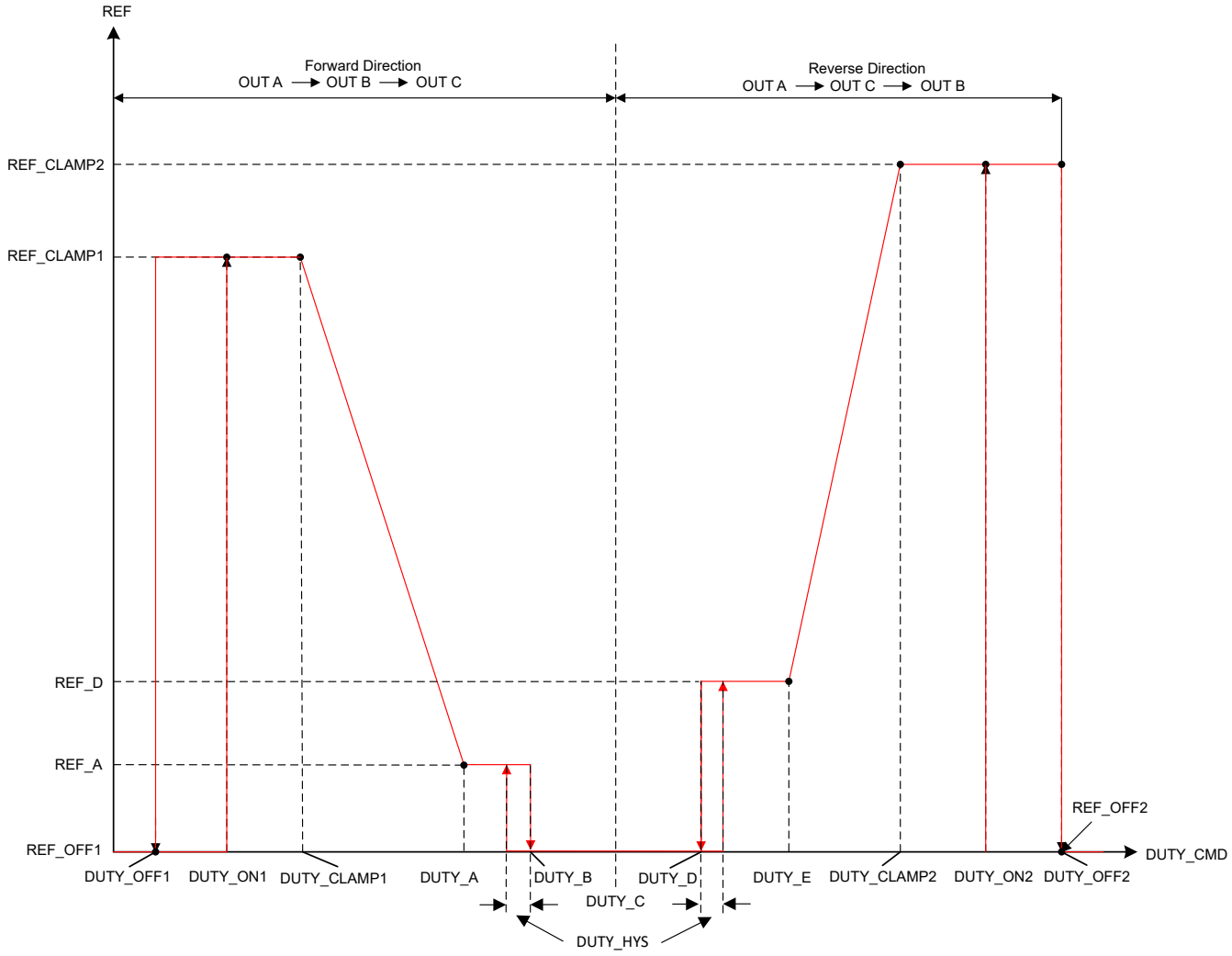


Figure 7-12. Forward Reverse Control Profiles

Forward-Reverse control profiles can be configured by setting REF_PROFILE_CONFIG to 11b. Forward-Reverse profiles feature direction change through adjusting the duty command. DUTY_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can be used to eliminate the separate signal used to control the motor direction.

Note

The direction change functionality through DIR pin and DIR_INPUT bits are disabled in forward reverse profile mode.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 7-12.

- DUTY_CLAMP1 configures the duty command till which reference will be constant. REF_CLAMP1 configures this constant reference between DUTY_OFF1 and DUTY_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. The reference changes linearly between DUTY_CLAMP1 and DUTY_A. DUTY_A to DUTY_E has to be in the same order as shown in Figure 7-12.
- DUTY_B configures the duty command above which MCT8329A will be in off state. The reference remains constant at REF_A between DUTY_A and DUTY_B.
- DUTY_C configures the duty command at which the direction is changed
- DUTY_D configures the duty command above which the MCT8329A will be in running state in the reverse direction. REF_D configures constant reference between DUTY_D and DUTY_E.
- DUTY_E configures the duty command above which reference changes linearly between DUTY_E and DUTY_CLAMP2.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.
- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 7-12.
- DUTY_OFF2 configures the duty command above which the reference changes in the reverse direction from REF_CLAMP2 to REF_OFF2.
- DUTY_HYS configures the hysteresis during step change at DUTY_B and DUTY_D.

7.3.7.6 Control Input Transfer Function without Profiler

The input control signal can be motor speed, DC input power or motor voltage (motor PWM duty cycle) as configured by CLOSED_LOOP_MODE and CONST_POWER_MODE bits.

Speed Input Transfer Function

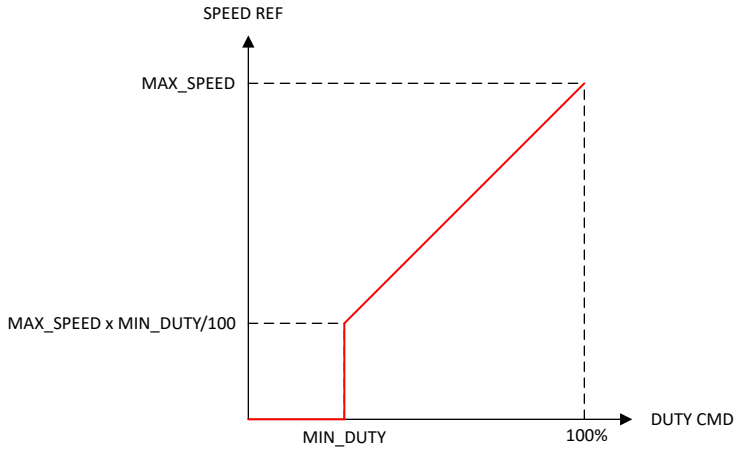


Figure 7-13. Speed Input Transfer Function

Figure 7-13 shows the relationship between DUTY CMD and SPEED REF. When speed loop is enabled, DUTY CMD sets the SPEED REF in Hz. MAX_SPEED sets the SPEED REF at DUTY CMD of 100%. MIN_DUTY sets the minimum SPEED REF (MIN_DUTY x MAX_SPEED). If MAX_SPEED is set to 0, SPEED REF is clamped to zero (irrespective of DUTY CMD) and motor is in stopped state.

Power Input Transfer Function

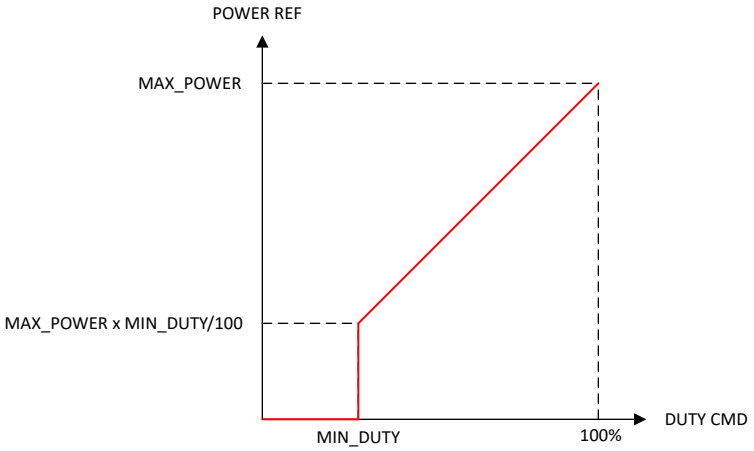


Figure 7-14. Power Input Transfer Function

Figure 7-14 shows the relationship between DUTY CMD and POWER REF. When power loop is enabled, DUTY CMD sets the POWER REF in Watt. MAX_POWER sets the POWER REF at DUTY CMD of 100%. MIN_DUTY sets the minimum POWER REF (MIN_DUTY x MAX_POWER). If MAX_POWER is set to 0, POWER REF is clamped to zero (irrespective of DUTY CMD) and motor is in stopped state.

Voltage Input Transfer Function

In voltage control mode, the phase voltage applied to motor is proportional to the DUTY CMD (from MIN_DUTY to 100% PWM duty applied to motor). For DUTY CMD less than MIN_DUTY, the applied voltage to motor is clamped to zero by making the duty cycle to zero.

7.3.8 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCT8329A begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCT8329A includes a number of features to allow for reliable motor start-up under all of these conditions. Figure 7-15 shows the motor start-up flow for each of the three initial motor states.

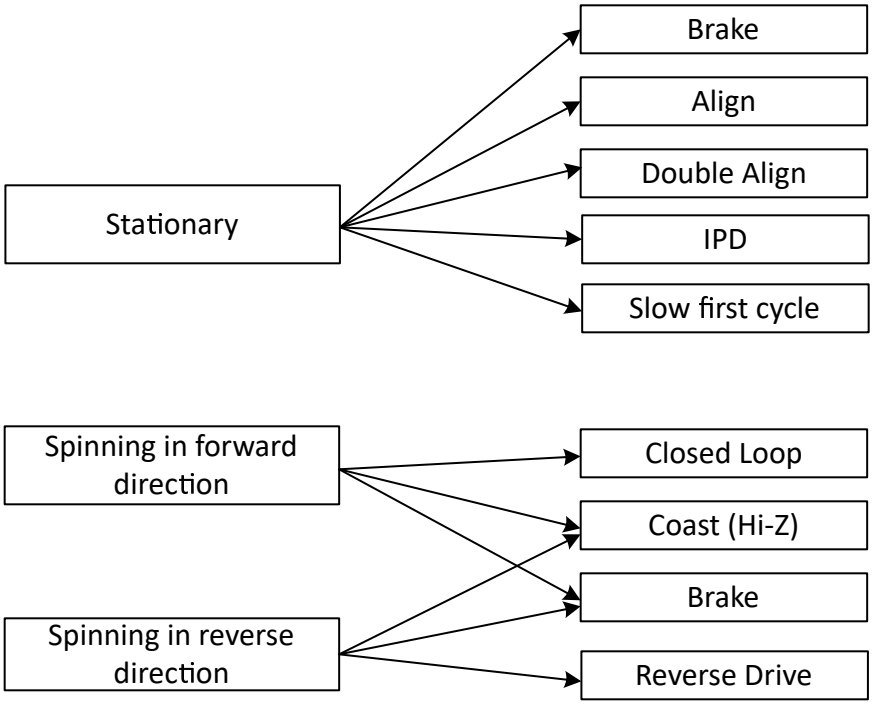


Figure 7-15. Starting the motor under different initial conditions

Note

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

7.3.8.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCT8329A provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCT8329A also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

7.3.8.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCT8329A resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC_EN. If resynchronization is disabled, the MCT8329A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

7.3.8.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCT8329A provides several methods to change the direction and drive the motor to the target speed reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed. The motor achieves the shortest possible spin-up time when spinning in the reverse direction.

If reverse drive is not enabled, then the MCT8329A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

Note

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

7.3.9 Motor Start Sequence (MSS)

Figure 7-16 shows the motor-start sequence implemented in the MCT8329A device.

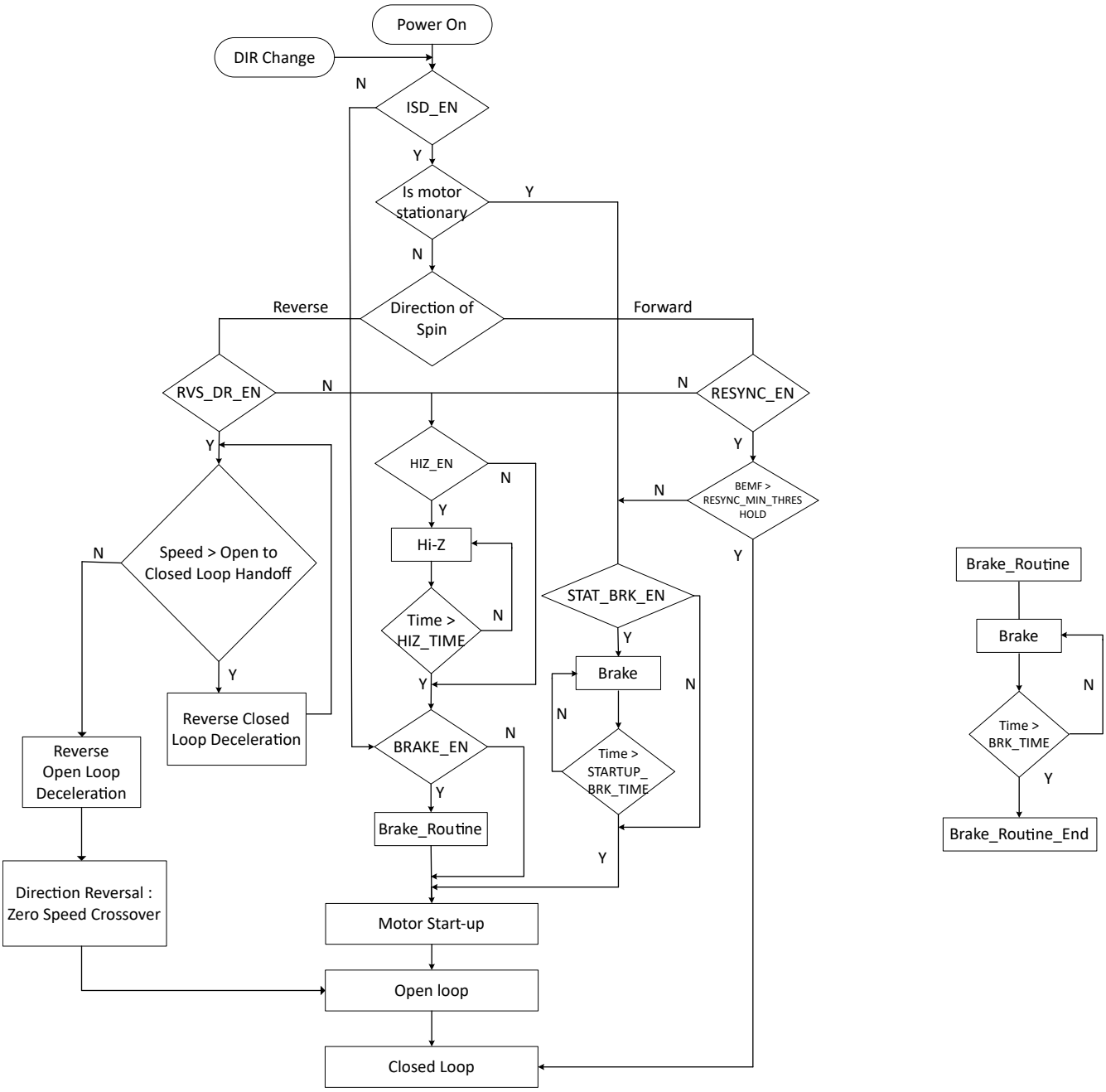


Figure 7-16. Motor Starting-Up Flow

Power-On State This is the initial state of the Motor Start Sequence (MSS). The MSS starts in this state on initial power-up or whenever the MCT8329A device comes out of standby or sleep mode.

DIR Change Judgement In MCT8329A, if direction change command is detected at start of MSS, the motor direction detected in ISD is assumed to be opposite to commanded direction and reverse drive is performed if RVS_DR_EN is set to 1b.

ISD_EN Judgement	After power-on, the MCT8329A MSS enters the ISD_EN judgement where it checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1b). If ISD is disabled, the MSS proceeds directly to the BRAKE_EN judgement. If ISD is enabled, MSS advances to the ISD (Is Motor Stationary) state.
ISD State	The MSS determines the initial condition (speed, direction of spin) of the motor (see Initial Speed Detect (ISD)). If motor is deemed to be stationary (motor BEMF < STAT_DETECT_THR), the MSS proceeds to STAT_BRK_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.
STAT_BRK_EN Judgement	The MSS checks if the stationary brake function is enabled (STAT_BRK_EN =1b). If the stationary brake function is enabled, the MSS advances to the stationary brake routine. If the stationary brake function is disabled, the MSS advances to motor start-up state (see Section 7.3.9.4).
Stationary Brake Routine	The stationary brake routine can be used to ensure the motor is completely stationary before attempting to start the motor. The stationary brake is applied by turning on all three low-side driver MOSFETs for a time configured by STARTUP_BRK_TIME.
Direction of Spin Judgement	The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCT8329A proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.
RESYNC_EN Judgement	If RESYNC_EN is set to 1b, MCT8329A proceeds to BEMF > RESYNC_MIN_THRESHOLD judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.
BEMF > RESYNC_MIN_THRESHOLD Judgement	If motor speed is such that BEMF > RESYNC_MIN_THRESHOLD, MCT8329A uses the speed and position information from the ISD state to transition to the closed loop state (see Motor Resynchronization) directly. If BEMF < RESYNC_MIN_THRESHOLD, MCT8329A proceeds to STAT_BRK_EN judgement.
RVS_DR_EN Judgement	The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled, the MSS advances to the HIZ_EN judgement.
Speed > Open to Closed Loop Handoff Judgement	The MSS checks to see if the reverse speed is high enough for MCT8329A to decelerate in closed loop. Till the speed (in reverse direction) is high enough, MSS stays in reverse closed loop deceleration. If speed is too low, then the MSS transitions to reverse open loop deceleration.
Reverse Closed Loop, Open Loop Deceleration and Zero Speed Crossover	The MCT8329A resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see *Reverse Drive*). When motor speed in reverse direction is too low, the MCT8329A switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high.
HIZ_EN Judgement	The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN =1). If the coast function is enabled, the MSS advances to the coast routine. If the coast function is disabled, the MSS advances to the BRAKE_EN judgement.
Coast (Hi-Z) Routine	The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.

BRAKE_EN Judgement	The MSS checks to determine whether the brake function is enabled (BRAKE_EN =1). If the brake function is enabled, the MSS advances to the brake routine. If the brake function is disabled, the MSS advances to the motor start-up state (see Section 7.3.9.4).
Brake Routine	Brake is applied either using high-side or low-side MOSFETs based on BRK_MODE configuration.
Closed Loop State	In this state, the MCT8329A drives the motor with trapezoidal control.

7.3.9.1 Initial Speed Detect (ISD)

The ISD function is used to identify the initial condition of the motor and is enabled by setting ISD_EN to 1b. The initial speed, position and direction is determined by sampling the phase voltage through the internal ADC. ISD can be disabled by setting ISD_EN to 0b. If the function is disabled (ISD_EN set to 0b), the MCT8329A does not perform the initial speed detect function and proceeds to check if the brake routine (BRAKE_EN) is enabled.

7.3.9.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCT8329A, which can transition directly into closed loop state without needing to stop the motor. In the MCT8329A, motor resynchronization can be enabled/disabled through RESYNC_EN bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

7.3.9.3 Reverse Drive

The MCT8329A uses the reverse drive function to change the direction of the motor rotation when ISD_EN and RVS_DR_EN are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see Figure 7-17). MCT8329A uses the same parameter values for open to closed loop handoff threshold (OPN_CL_HANDOFF_THR), open loop acceleration rates (OL_ACC_A1, OL_ACC_A2) and open loop current limit (OL_ILIMIT) in the reverse direction as in the forward direction..

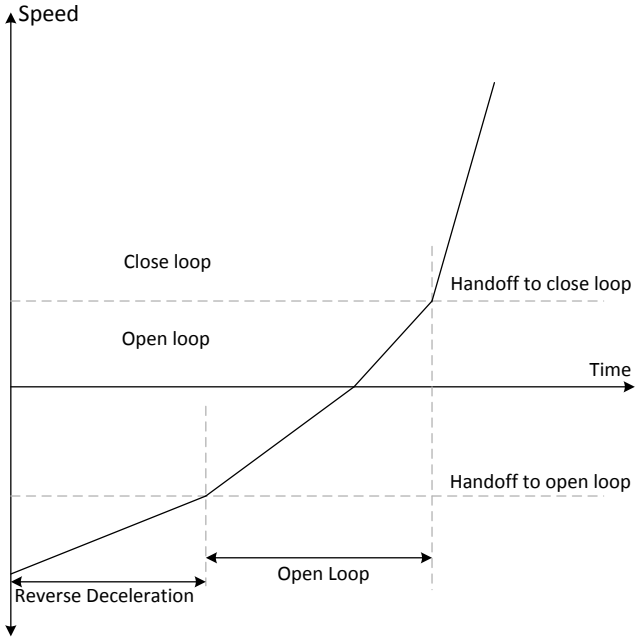


Figure 7-17. Reverse Drive Function

7.3.9.4 Motor Start-up

There are different options available for motor start-up from a stationary position and these options can be configured by MTR_STARTUP. In align and double align mode, the motor is aligned to a known position by injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

7.3.9.4.1 Align

Align is enabled by configuring MTR_STARTUP to 00b. The MCT8329A aligns the motor by injecting a DC current using a particular phase pattern (phase-C high-side FET and phase-B low-side FET are ON) - current flowing for a certain time configured by ALIGN_TIME.

The duty cycle during align is defined by ALIGN_DUTY. In MCT8329A, current limit during align is configured through ALIGN_CURR_THR and CBC_ILIMIT.

A fast change in the phase current during align may result in a sudden change in the driving torque and this could result in acoustic noise. To avoid this, the MCT8329A ramps up duty cycle from 0 to until it reaches ALIGN_DUTY at a configurable rate set by ALIGN_RAMP_RATE. At the end of align routine, the motor will be aligned at the known position.

7.3.9.4.2 Double Align

Double align is enabled by configuring MTR_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180^{o} out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliability of align based start-up, the MCT8329A provides the option of double align start-up. In double align start-up, MCT8329A uses a phase pattern for the second align that is 60^{o} out of phase with the first align phase pattern in the commanded direction. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

7.3.9.4.3 Initial Position Detection (IPD)

Initial Position Detection (IPD) can be enabled by configuring MTR_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

7.3.9.4.3.1 IPD Operation

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see Figure 7-18). When the current reaches the threshold configured by IPD_CURR_THR, the MCT8329A stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD_CURR_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

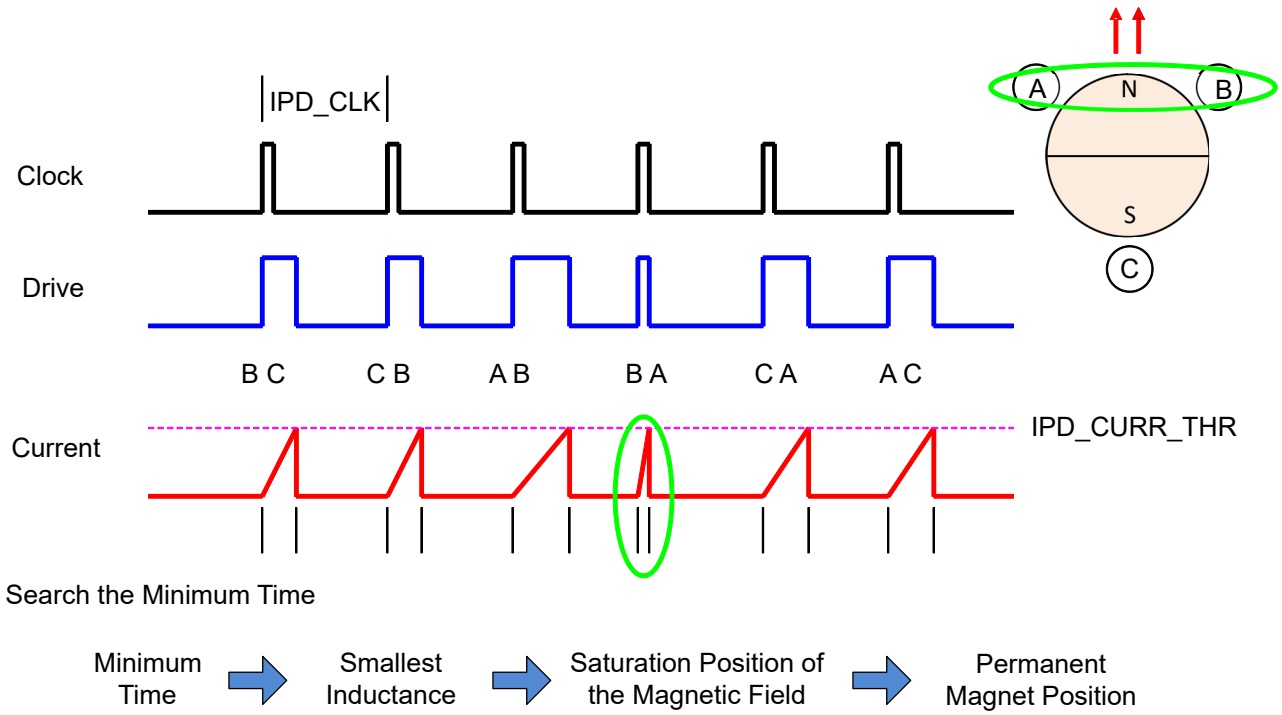


Figure 7-18. IPD Function

7.3.9.4.3.2 IPD Release

IPD release uses Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see Figure 7-19).

The Hi-Z mode during IPD release can result in a voltage increase on motor DC supply voltage VM (V_{PVDD}). The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between V_{PVDD} and GND to absorb the energy.

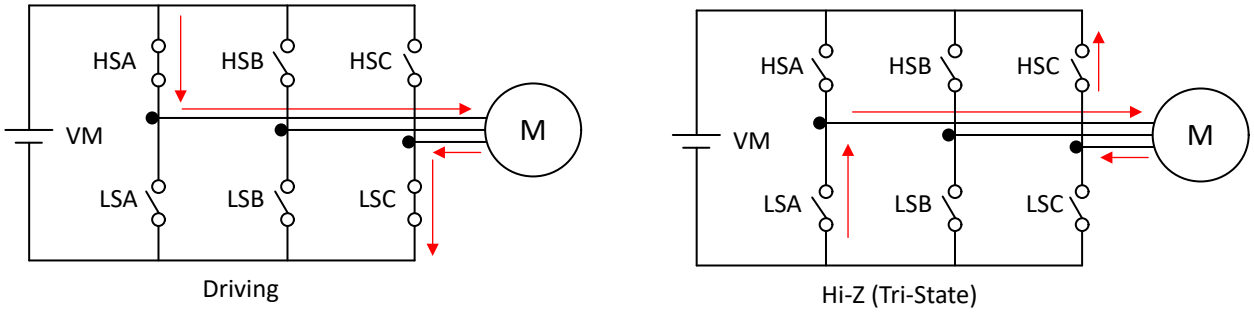


Figure 7-19. IPD Release Hi-Z mode

7.3.9.4.3.3 IPD Advance Angle

After the initial position is detected, the MCT8329A begins driving the motor in open loop at an angle specified by IPD_ADV_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD_ADV_ANGLE to allow for smooth acceleration in the application (see Figure 7-20).

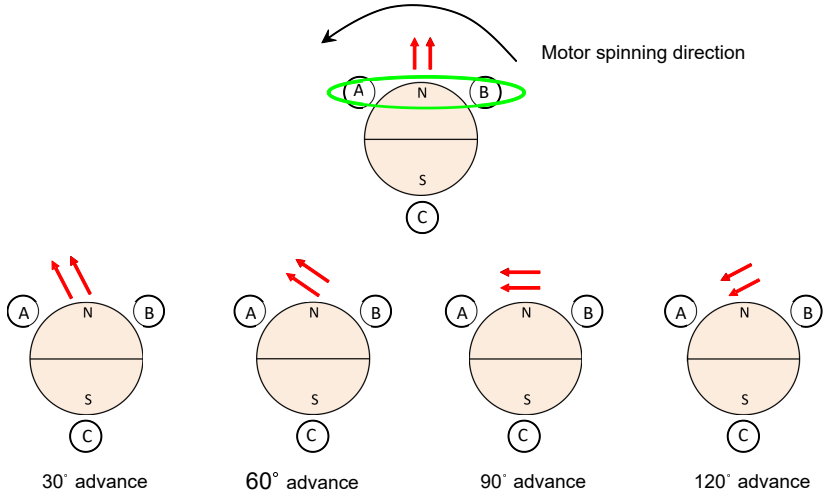


Figure 7-20. IPD Advance Angle

7.3.9.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR_STARTUP to 11b. In slow first cycle start-up, the MCT8329A starts motor commutation at a frequency defined by SLOW_FIRST_CYCLE_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

7.3.9.4.5 Open loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCT8329A begins to accelerate the motor in open loop. During open loop, fixed duty cycle is applied and the cycle by cycle current limit functionality is used to regulate the current.

In MCT8329A, open loop current limit threshold is selected through OL_ILIMIT_CONFIG and is set either by CBC_ILIMIT or OL_ILIMIT based on the configuration of OL_ILIMIT_CONFIG. Open loop duty cycle is configured through OL_DUTY. While the motor is in open loop, speed (and commutation instants) is determined by Equation 8. In MCT8329A, open loop acceleration coefficients, A1 and A2 are configured through OL_ACC_A1 and OL_ACC_A2 respectively. The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the BEMF zero-crossing based commutation control to accurately drive the motor.

$$\text{Speed}(t) = A1 * t + 0.5 * A2 * t^2 \quad (8)$$

7.3.9.4.6 Transition from Open to Closed Loop

MCT8329A has an internal mechanism to determine the motor speed for transition from open loop commutation to BEMF zero crossing based closed loop commutation. This feature of automatically deciding the open to closed handoff speed can be enabled by configuring AUTO_HANDOFF to 1b. If AUTO_HANDOFF is set to 0b, the open to closed loop handoff speed needs to be configured by OPN_CL_HANDOFF_THR. The closed loop in this section does not refer to closed speed loop - it refers to the commutation control changing from open loop (equation based) to closed loop (BEMF zero crossing based).

7.3.10 Closed Loop Operation

In closed loop operation (closed loop commutation control), the MCT8329A drives the motor using trapezoidal commutation. The commutation instant is determined by the BEMF zero crossing on the phase which is not driven (Hi-Z).

7.3.10.1 120º Commutation

In 120º commutation, each phase is driven for 120º and is Hi-Z for 60º within each half electrical cycle as shown in Figure 7-21. In 120º commutation there are six different commutation states. 120º commutation can be configured by setting COMM_CONTROL to 00b. MCT8329A supports different modulation modes with 120º commutation which can be configured through PWM_MODUL.

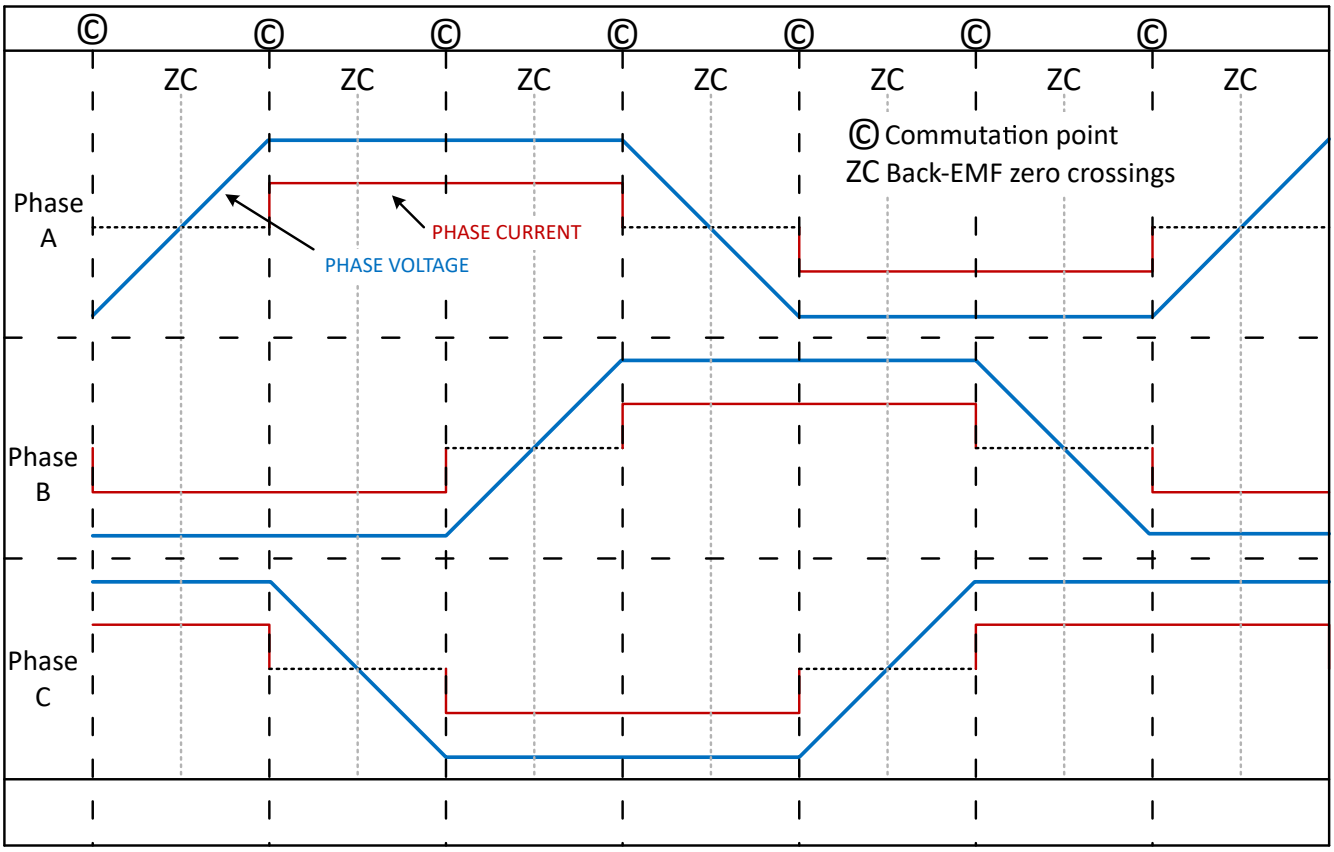


Figure 7-21. 120º commutation

7.3.10.1.1 High-Side Modulation

High-side modulation can be configured by setting PWM_MODUL to 00b. In high-side modulation, for a given commutation state, one of the high-side FETs is switching with the commanded duty cycle DUTY_OUT, while the low-side FET is ON with 100% duty cycle (see Figure 7-22).

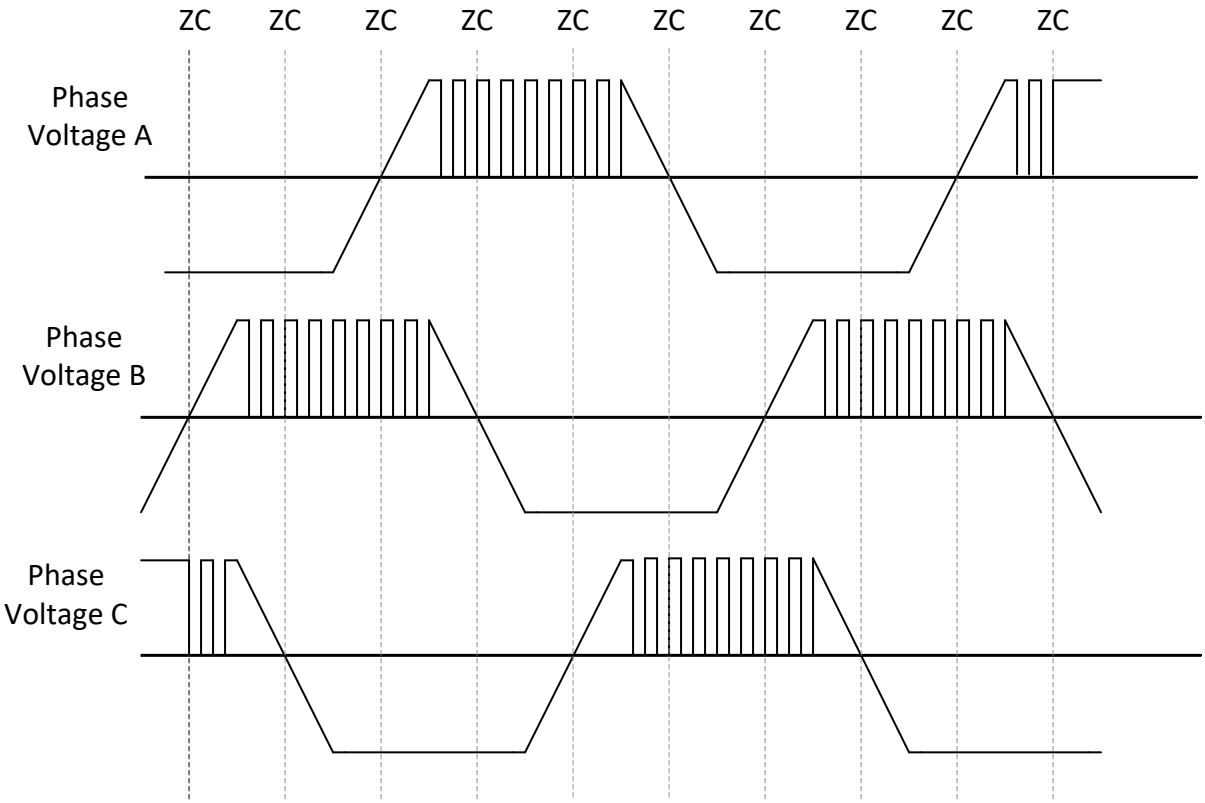


Figure 7-22. 120° commutation in High Side Modulation Mode

7.3.10.1.2 Low-Side Modulation

Low-side modulation can be configured by setting PWM_MODUL to 01b. In low-side modulation, for a given commutation state, one of the low-side FETs is switching with the commanded duty cycle DUTY_OUT, while the high-side FET is ON with 100% duty cycle (see Figure 7-23).

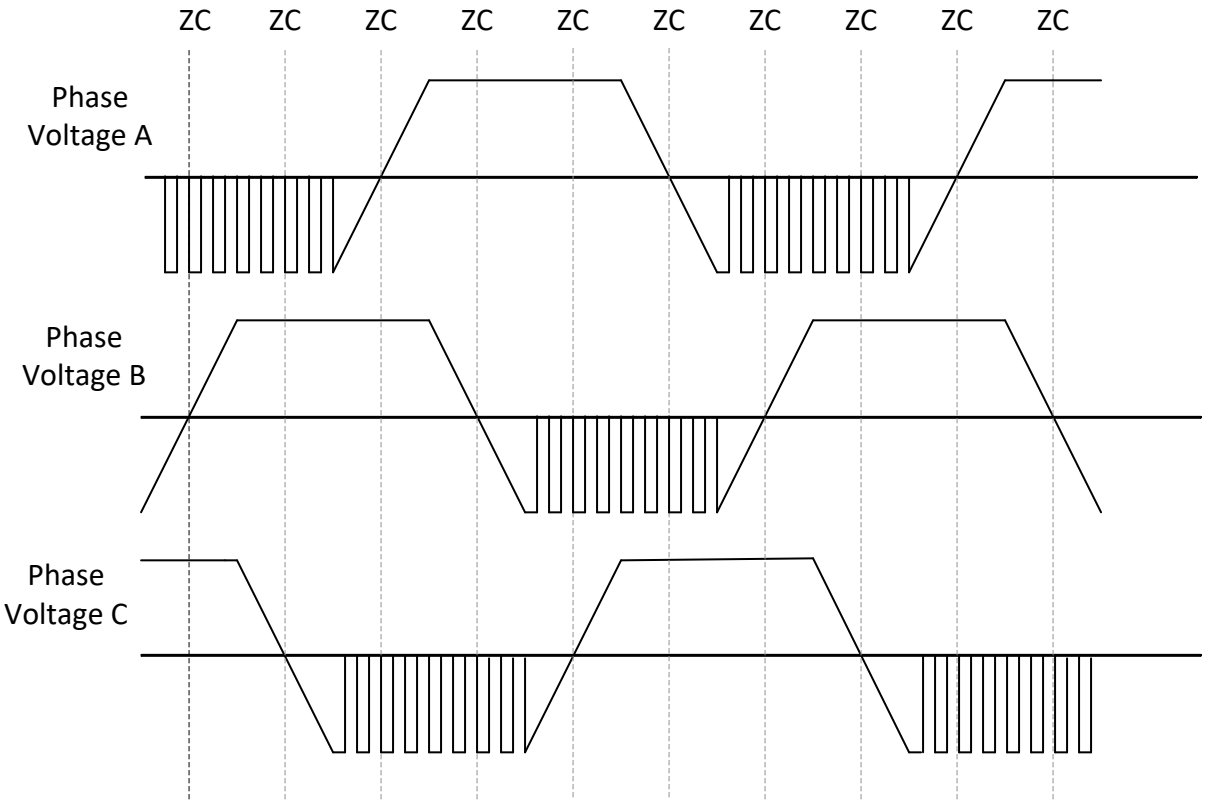


Figure 7-23. 120 º commutation in Low Side Modulation Mode

7.3.10.1.3 Mixed Modulation

Mixed modulation can be configured by setting PWM_MODUL to 10b. In mixed modulation, MCT8329A dynamically switches between high and low-side modulation (see Figure 7-24). The switching losses are distributed evenly amongst the high and low-side MOSFETs in mixed modulation mode.

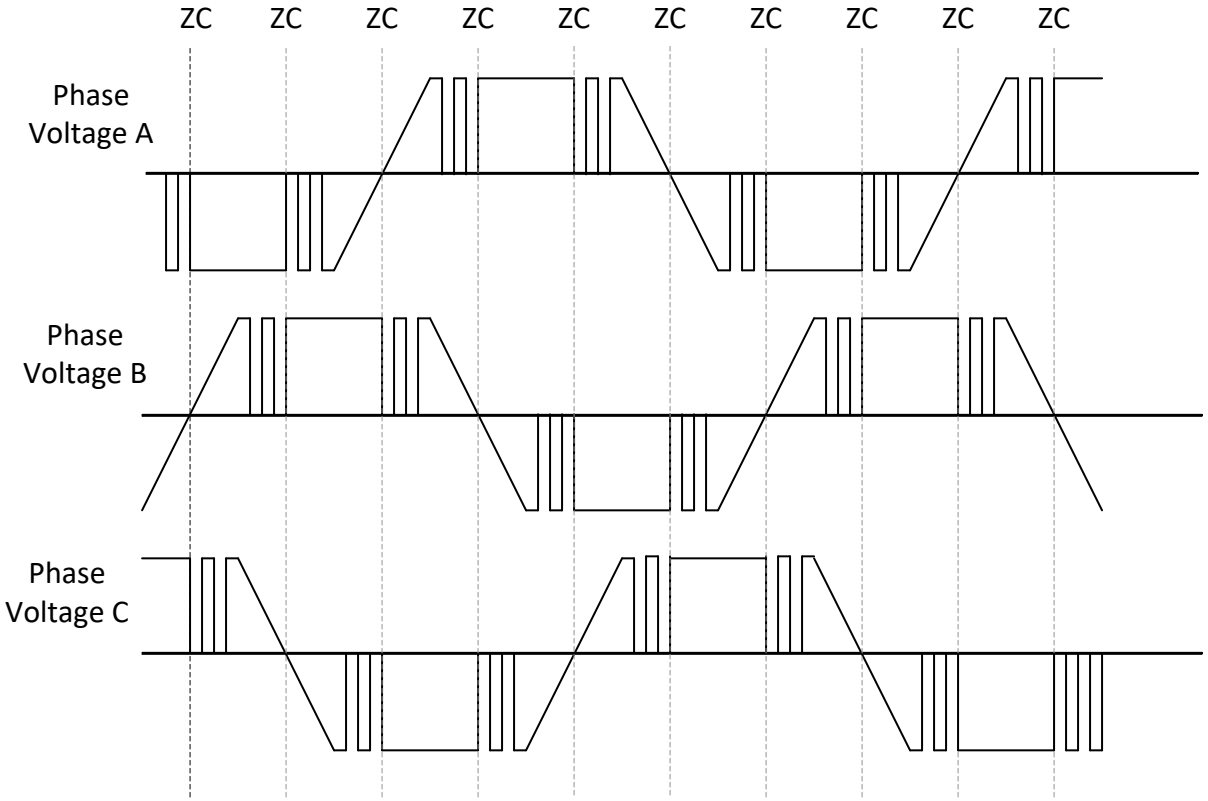


Figure 7-24. 120° commutation in Mixed Modulation Mode

7.3.10.2 Variable Commutation

Variable commutation can be configured by setting COMM_CONTROL to 01b. 120° commutation may result in acoustic noise due to the long Hi-Z period causing some torque ripple in the motor. In order to reduce this torque ripple and acoustic noise, the MCT8329A uses variable commutation to reduce the phase current ripple at commutation by extending 120° driving time and gradually decreasing duty cycle prior to entering Hi-Z state. In this mode, the phase is Hi-Z between 30° and 60° and this window size is dynamically adjusted based on speed. A smaller window size will typically give better acoustic performance. Figure 7-25 shows 150° commutation with 30° window size.

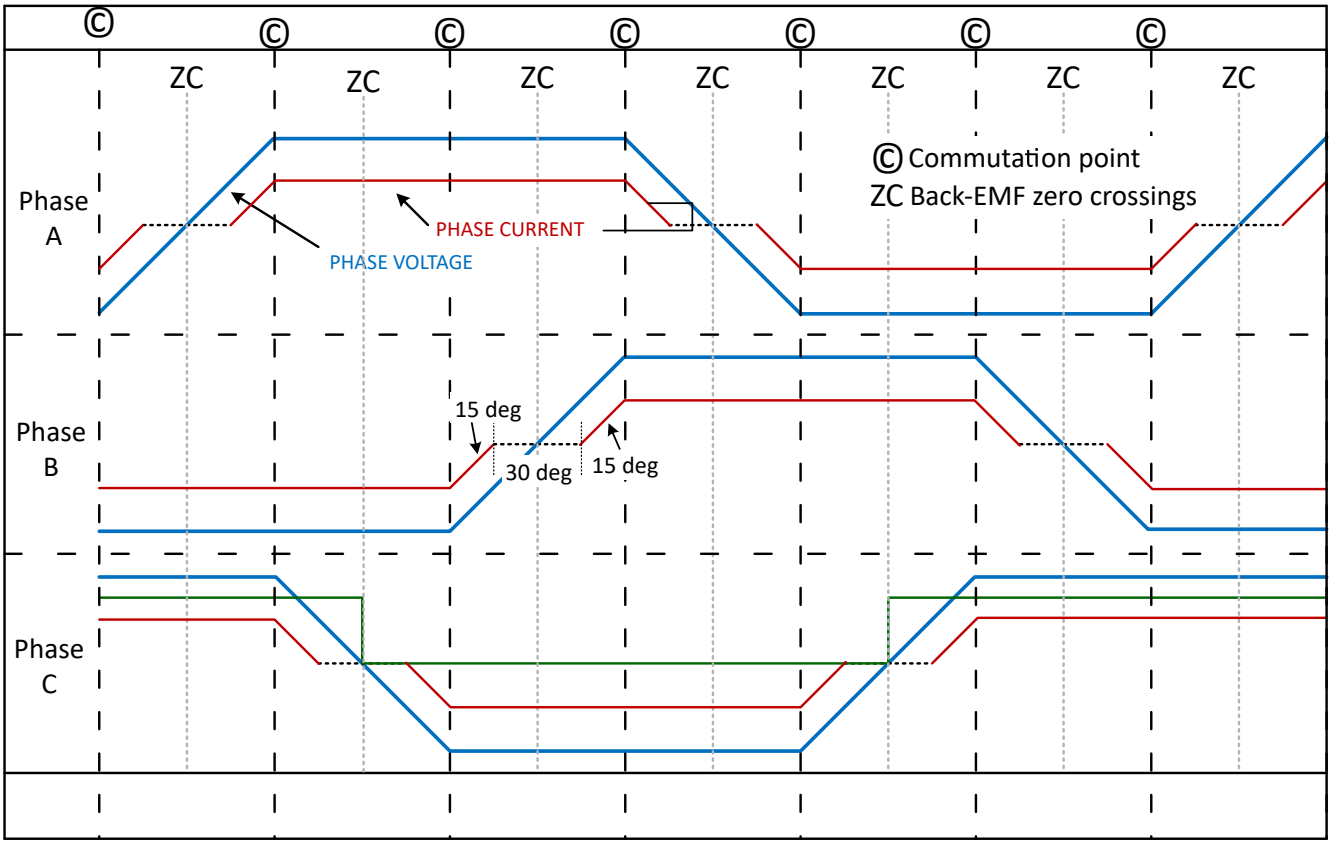


Figure 7-25. 150º commutation

Note

Different modulation modes are supported only with 120º commutation; variable commutation uses mixed modulation mode only.

7.3.10.3 Lead Angle Control

To achieve the best efficiency, it is often desirable to control the drive state of the motor so that the motor phase current is aligned with the motor BEMF voltage. MCT8329A provides the option to advance or delay the phase voltage from the commutation point by adjusting the lead angle. The lead angle can be adjusted to obtain optimal efficiency. This can be accomplished by operating the motor at constant speed and load conditions and adjusting the lead angle (LD_ANGLE) until the minimum current is achieved. The MCT8329A has the capability to apply both positive and negative lead angle (by configuring LD_ANGLE_POLARITY) as shown in Figure 7-26

Lead angle can be calculated by {LD_ANGLE x 0.12}º; for example, if the LD_ANGLE is 0x1E and LD_ANGLE_POLARITY is 1b, then a lead angle of +3.6º(advance) is applied. If LD_ANGLE_POLARITY is 0b, then a lead angle of -3.6º(delay) is applied.

Note

For 120º commutation, the negative lead angle is limited to -20º; any lead angle lower than that will be clamped to -20º.

For variable commutation, negative lead angle is not supported and positive lead angle is limited to +15º. Anything configured higher than +15º or lower than 0^0 will be clamped to 15º and 0º respectively.

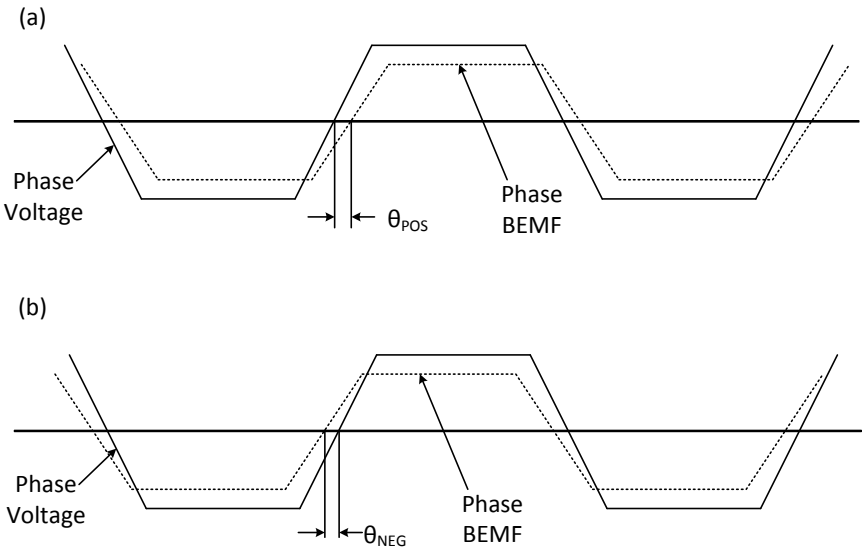


Figure 7-26. Positive and Negative Lead Angle Definition

7.3.10.4 Closed loop accelerate

To prevent sudden changes in the torque applied to the motor which could result in acoustic noise, the MCT8329A device provides the option of limiting the maximum rate at which the duty command input can change in voltage control mode. The closed loop acceleration rate parameter sets the maximum rate at which the duty command (Voltage control reference duty) changes (shown in Figure 7-27). In the MCT8329A , closed loop acceleration rate is configured through CL_ACC. In closed loop speed and closed loop power control modes, CL_ACC has no impact and the PI loop limit the rate of PWM duty change applied to the motor.

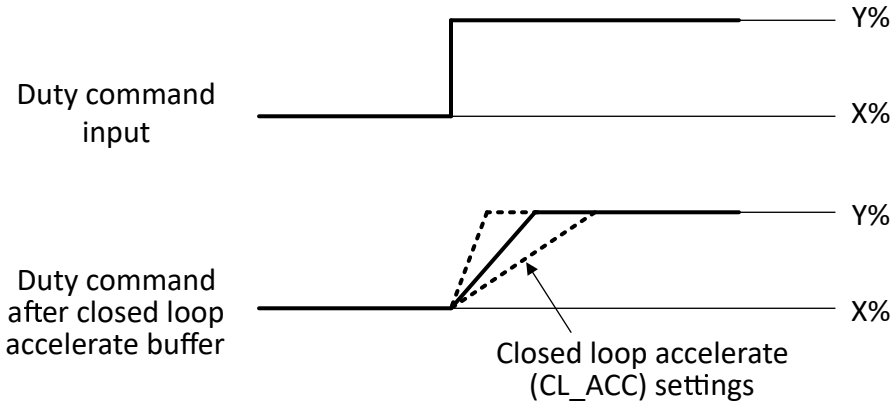


Figure 7-27. Closed loop accelerate

7.3.11 Speed Loop

MCT8329A has a speed loop option which can be used to maintain constant speed under varying operating conditions. Speed loop is enabled by setting CLOSED_LOOP_MODE to 01b. K_p and K_i coefficients are configured through SPD_POWER_KP and SPD_POWER_KI. The output of speed loop (SPEED_PI_OUT) is used to generate the DUTY OUT (duty cycle of the PWM voltage applied to the motor winding). The PI controller output upper (V_{MAX}) and lower bound (V_{MIN}) saturation limits are configured through SPD_POWER_V_MAX and SPD_POWER_V_MIN respectively. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up. The speed loop PI controller is as in Figure 7-28.

With REF_PROFILE_CONFIG = 0b, SPEED_REF is derived from duty command input (DUTY CMD) from maximum speed (configured by MAX_SPEED) as shown in Equation 9 or from the input profiler output (see Section 7.3.7.5.

$$SPEED\ REF(Hz) = DUTY\ CMD \times Maximum\ Speed\ (Hz) \quad (9)$$

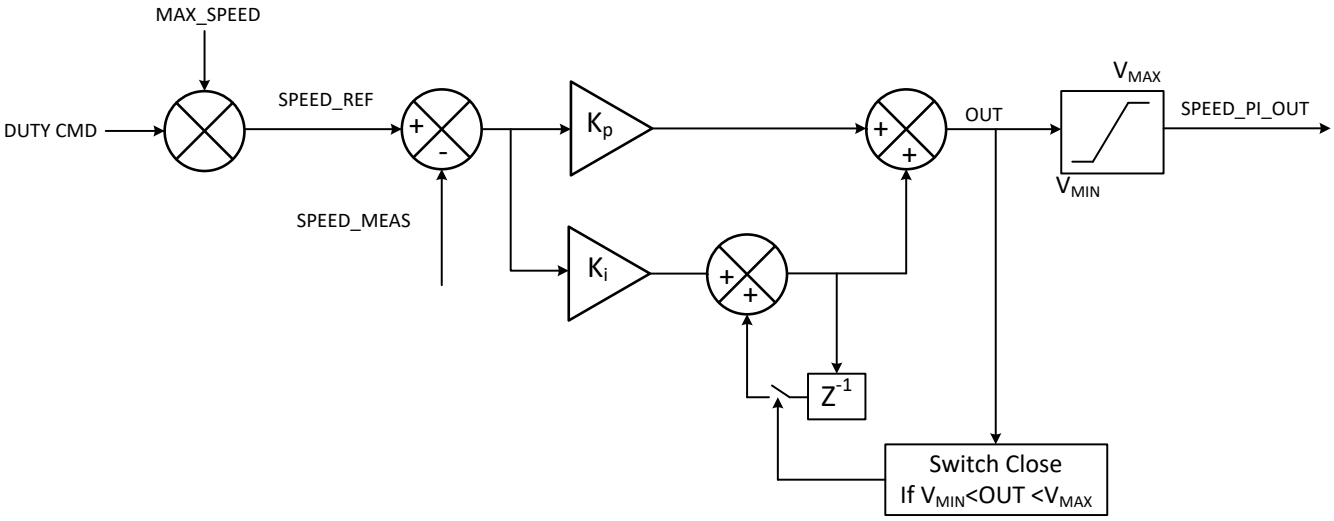


Figure 7-28. Speed Loop

7.3.12 Power Loop

MCT8329A provides an option of regulating the (input) power instead of motor speed - this input power regulation can be done in two modes, namely, closed loop power control and power limit control. Input power regulation (instead of motor speed) mode is selected by setting CLOSED_LOOP_MODE to 10b. This should be accompanied by setting CONST_POWER_MODE to 01b for closed loop power control or to 10b for power limit control. In either of the power regulation modes, the maximum power that MCT8329A can draw from the DC input supply is set by MAX_POWER - the power reference (POWER_REF in Figure 7-29).

With REF_PROFILE_CONFIG = 0b, POWER_REF is derived from duty command input (DUTY CMD) from maximum power (configured by MAX_POWER) as shown in Equation 10 or from the input profiler output (see Section 7.3.7.5. The hysteresis band for the power reference is set by CONST_POWER_LIMIT_HYST. In both the power regulation modes, the minimum power reference is set by MIN_DUTY x MAX_POWER.

$$POWER\ REF(W) = DUTY\ CMD \times Maximum\ Power\ (W) \quad (10)$$

In both the power regulation modes, MCT8329A uses the same PI controller parameters as in the speed loop mode. K_p and K_i coefficients are configured through SPD_POWER_KP and SPD_POWER_KI. The PI controller output upper (V_{MAX}) and lower bound (V_{MIN}) saturation limits are configured through SPD_POWER_V_MAX and SPD_POWER_V_MIN respectively. The key difference between closed loop power control and power limit control is in the when the PI controller decides the DUTY OUT (duty cycle of PWM) applied to FETs. In closed loop power control, DUTY OUT is always equal to POWER_PI_OUT from the PI controller output in Figure 7-29. However, in power limit control, the PI controller decides the DUTY OUT only if POWER_MEAS > POWER_REF + CONST_POWER_LIMIT_HYST. If POWER_MEAS < POWER_REF + CONST_POWER_LIMIT_HYST, the PI controller is not used and DUTY OUT is equal to DUTY CMD. Essentially, in closed loop power control, input power is always actively regulated to POWER_REF whereas, in power limit control, input power is only limited to POWER_REF and not actively regulated to POWER_REF. When output of the power PI loop saturates, the integrator is disabled to prevent integral wind-up.

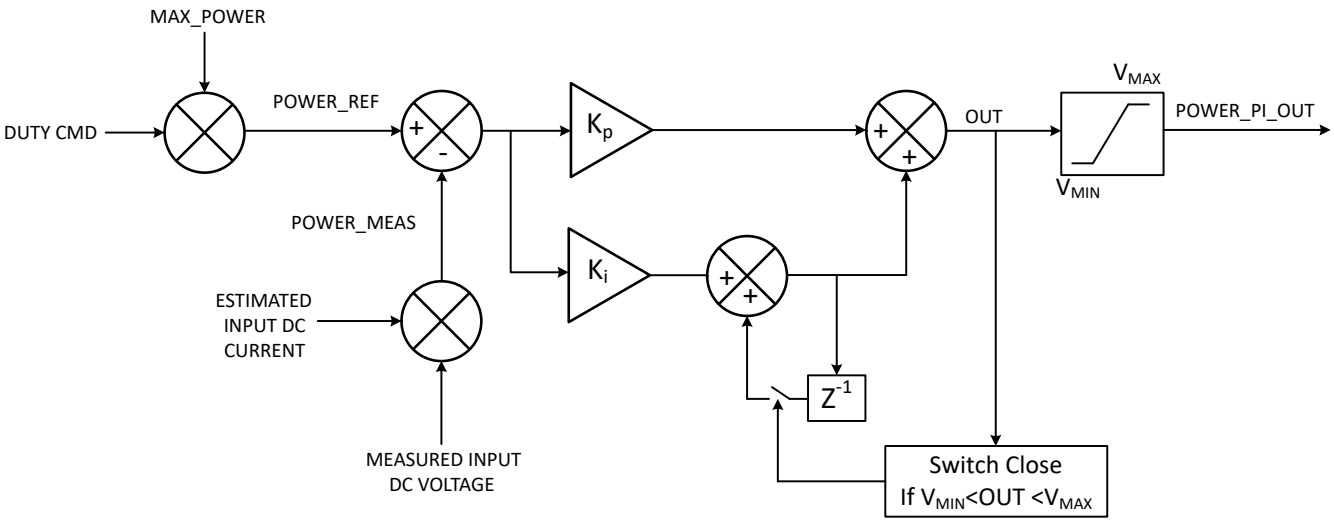


Figure 7-29. Power Regulation

7.3.13 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_{PVDD} voltage surges. The AVS feature works to prevent this voltage surge on V_{PVDD} and can be enabled by setting AVS_EN to 1b. AVS can be disabled by setting AVS_EN to 0b. When AVS is disabled, the deceleration rate is configured through CL_DEC_CONFIG.

7.3.14 Output PWM Switching Frequency

MCT8329A provides the option to configure the output PWM switching frequency of the MOSFETs through PWM_FREQ_OUT. PWM_FREQ_OUT has range of 5-100 kHz. In order to select optimal output PWM switching frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

7.3.15 Fast Start-up (< 50 ms)

The MCT8329A has the capability to accelerate a motor from 0 to 100% speed within 50ms. This will only work on low inertia motors which are capable of this level of acceleration. In order to achieve fast start-up, the commutation instant detection needs to be configured to hybrid mode by setting INTEG_ZC_METHOD to 1b. In the hybrid mode, the commutation instant is determined by using back-EMF integration at low-medium speeds and by using built-in comparators (BEMF zero crossing) at higher speeds. MCT8329A automatically transitions between back-EMF integration and comparator based commutation depending on the motor speed as shown in Figure 7-30. The duty cycles for commutation method transition at lower speeds are directly configured by INTEG_DUTY_THR_LOW and INTEG_DUTY_THR_HIGH and at higher speeds are indirectly configured by INTEG_CYC_THR_LOW and INTEG_CYC_THR_HIGH. These duty cycles should be configured to provide a sufficient hysteresis band to avoid repeated commutation method transitions near threshold duty cycles. The BEMF threshold values used to determine the commutation instant in the back-EMF integration method are configured by BEMF_THRESHOLD1 and BEMF_THRESHOLD2.

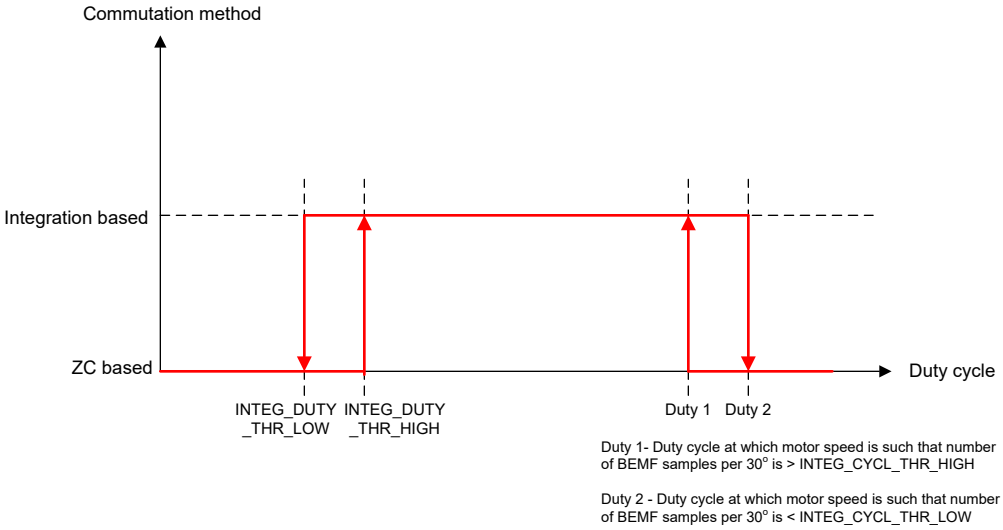


Figure 7-30. Commutation Method Transition

7.3.15.1 BEMF Threshold

Figure 7-31 shows the three-phase voltages during 120° trapezoidal operation. One of the phases is always floating within a 60° commutation interval and MCT8329A integrates this floating phase voltage (which denotes the motor back-EMF) in the back-EMF integration method to detect the next commutation instant. The floating phase voltage can either be increasing or decreasing and the algorithm starts the integration after the zero cross detection to eliminate integration errors due to variable degauss time. The floating phase voltage is periodically sampled (after zero cross) and added (discrete form of integration). BEMF threshold (BEMF_THRESHOLD1 and BEMF_THRESHOLD2) value is set such that the integral value of the floating phase voltage crosses the BEMF_THRESHOLD1 or BEMF_THRESHOLD2 value at (or very near) to the commutation instant. BEMF_THRESHOLD1 is the threshold for rising floating phase voltage and BEMF_THRESHOLD2 is the threshold for falling floating phase voltage. If BEMF_THRESHOLD2 is set to 0, then BEMF_THRESHOLD1 is used as the threshold for both rising and falling floating phase voltage.

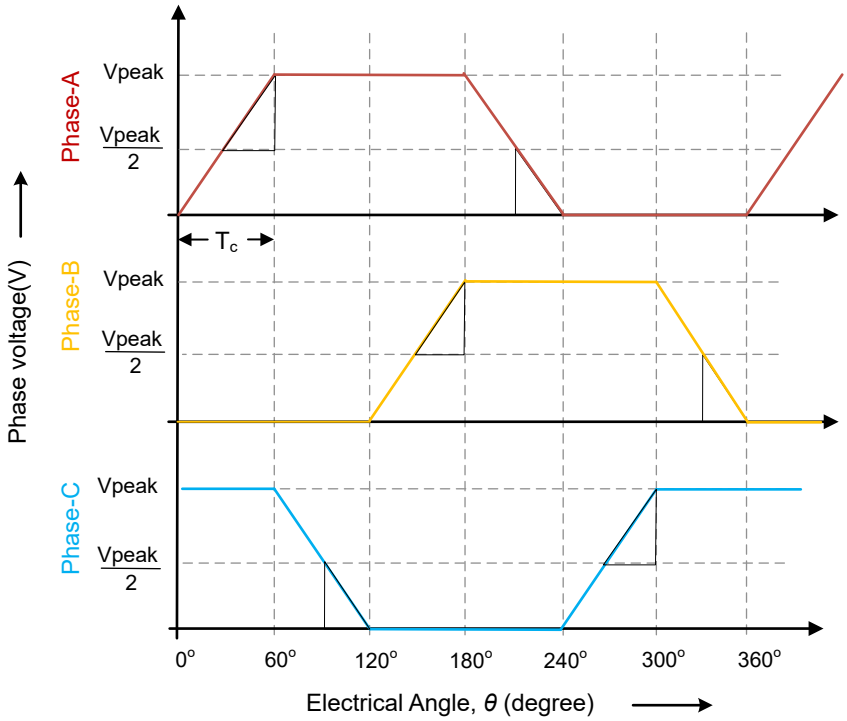


Figure 7-31. Back-EMF integration using floating phase voltage

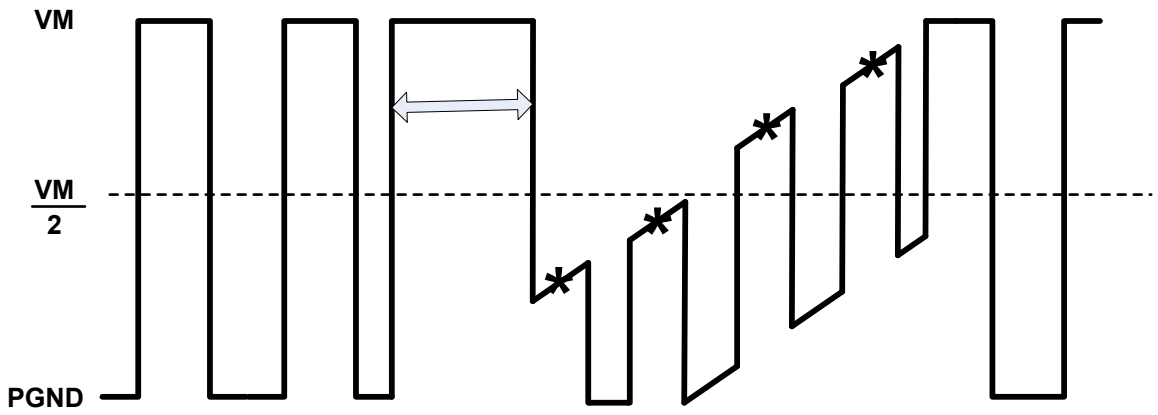
In Figure 7-31 , Vpeak is the peak-peak value of the back-EMF , Vpeak/2 denotes the zero cross of the back-EMF and Tc is the commutation interval or time period of the 60º window. The highlighted triangle in each 60º window is the integral value of back-EMF used by the algorithm to determine the commutation instant. This integral value, which can be approximated as the area of the highlighted triangle, is given by Equation 11.

$$(½)^* (Vpeak/2) * Tc/2 \quad (11)$$

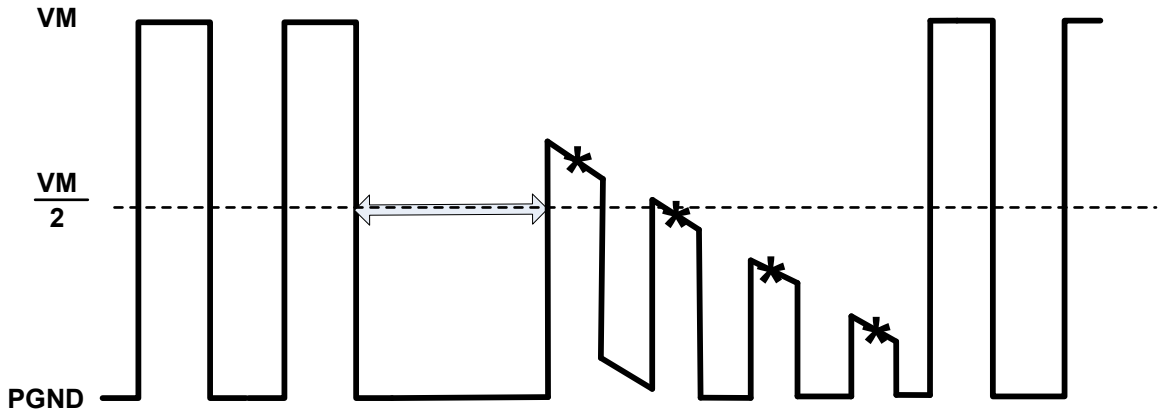
See Section 8.2.2.4for an example application on setting the BEMF threshold.

7.3.15.2 Dynamic Degauss

In MCT8329A, the degauss time (time for the outgoing phase current to decay to zero) can be dynamically computed after the commutation for a precise detection of the zero crossing instant. This is done by enabling the dynamic degauss feature (DYN_DEGAUSS_EN is set to 1b). This feature allows the motor control algorithm to capture the zero crossing instant after the outgoing (floating) phase voltage is completely settled; that is, when the outgoing phase current has decayed to zero and the outgoing (floating) phase voltage is not clamped (to either PVDD (VM) or PGND), represents the true back-EMF. This accurate measurement of zero cross instant allows fast acceleration of the motors (< 50 ms) using MCT8329A.



Degauss time(shown by double-sided arrow) after commutation during which the outgoing(floating) phase voltage is clamped to VM(by negative outgoing phase current) during increasing back-EMF; sampling of back-EMF(denoted by *) should start after degauss time is over for accurate zero cross instant detection



Degauss time(shown by double-sided arrow) after commutation during which the outgoing(floating) phase voltage is clamped to PGND(by positive outgoing phase current) during decreasing back-EMF; sampling of back-EMF(denoted by *) should start after degauss time is over for accurate zero cross instant detection

Figure 7-32. Degauss Time

7.3.16 Fast Deceleration

MCT8329A has the capability to decelerate a motor quickly (100% to 10% speed reduction within tens of ms) without pumping energy back into the input DC supply using the fast deceleration feature in conjunction with the AVS feature. The fast deceleration feature can be enabled by setting FAST_DECEL_EN to 1b; AVS_EN should be set to 1b to prevent energy pump-back into the input DC supply. This combination enables a linear braking effect resulting in a fast and smooth speed reduction without energy pump-back into the DC input supply. This feature combination can also be used during reverse drive (see Reverse Drive) or motor stop (see Active Spin-Down) to reduce the motor speed quickly without energy pump-back into the DC input supply.

Note

Fast deceleration feature is available only in bi-directional CSA mode. The feature is not available in uni-directional CSA mode.

The deceleration time can be controlled by appropriately configuring the current limit during deceleration, FAST_DECEL_CURR_LIM. A higher current limit results in a lower deceleration time and vice-versa. A higher than necessary current limit setting may result in motor stall faults, at low target speeds, due to excessive braking torque. This can also lead to higher losses in the external FETs, especially in repeated

acceleration-deceleration cycles. Therefore, the FAST_DECEL_CURR_LIM should be chosen appropriately, so as to decelerate within the required time without resulting in stall faults or overheating.

FAST_BRK_DELTA is used to configure the target speed hysteresis band to exit the fast deceleration mode and re-enter motoring mode when motor reaches the target speed. For example, if FAST_BRK_DELTA is set to 1%, the fast deceleration is deemed complete when motor speed reaches within 1% of target speed. Setting a higher value for FAST_BRK_DELTA may eliminate motor stall faults, especially when high FAST_DECEL_CURR_LIM values are used. Setting a higher value for FAST_BRK_DETLA will also result in higher speed error between target speed and motor speed at the end of deceleration mode - motor will eventually reach the target speed once motoring mode is resumed. FAST_DECEL_CURR_LIM and FAST_BRK_DELTA should be configured in tandem to optimize between lower deceleration time and reliable (no stall faults) deceleration profile.

FAST_DEC_DUTY_THR configures the speed below which fast deceleration will be implemented. For example, if FAST_DEC_DUTY_THR is set to 70%, any deceleration from speeds above 70% will not use fast deceleration until the speed goes below 70%. FAST_DEC_DUTY_WIN is used to set the minimum deceleration window (initial speed - target speed) below which fast deceleration will not be implemented. For example, if FAST_DEC_DUTY_WIN is set to 15% and 50%->40% deceleration command is received, fast deceleration is not used to reduce the speed from 50% to 40% since the deceleration window (10%) is smaller than FAST_DEC_DUTY_WIN.

MCT8329A provides a dynamic current limit option during fast deceleration to improve the stability of fast deceleration when braking to very low speeds; using this feature the current limit during fast deceleration can be reduced as the motor speed decreases. This feature can be enabled by setting DYNAMIC_BRK_CURR to 1b. The current limit at the start of fast deceleration (at FAST_DEC_DUTY_THR) is configured by FAST_DECEL_CURR_LIM and the current limit at zero speed is configured by DYN_BRK_CURR_LOW_LIM; the current limit during fast deceleration varies linearly with speed between these two operating points when dynamic current limit is enabled. If dynamic current limit is disabled, current limit during fast deceleration stays constant and is configured by FAST_DECEL_CURR_LIM.

7.3.17 Dynamic Voltage Scaling

The MCT8329A integrates dynamic voltage scaling to improve the resolution of phase voltage sensing. The motor phase voltage is sensed using an integrated voltage divider with voltage scaling of 10 V/V or 20 V/V, to limit the sense voltage to less than 3-V across operating voltage. Setting the bit DYN_VOLT_SCALING_EN = 0b disables dynamic voltage scaling and MCT8329A uses 20 V/V gain. Setting the bit DYN_VOLT_SCALING_EN = 1b enables dynamic voltage scaling and MCT8329A sense the DC bus voltage during motor idle state and select the appropriate voltage scaling of 10 V/V or 20 V/V.

Note

TI recommends to disable dynamic voltage scaling in case of DC bus voltage more than 24 V is expected.

7.3.18 Motor Stop Options

The MCT8329A provides different options for stopping the motor which can be configured by MTR_STOP.

7.3.18.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR_STOP to 000b. When motor stop command is received, the MCT8329A turns off all the external MOSFETs creating Hi-Z state at the phase motor terminals. When the MCT8329A transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example Figure 7-33).

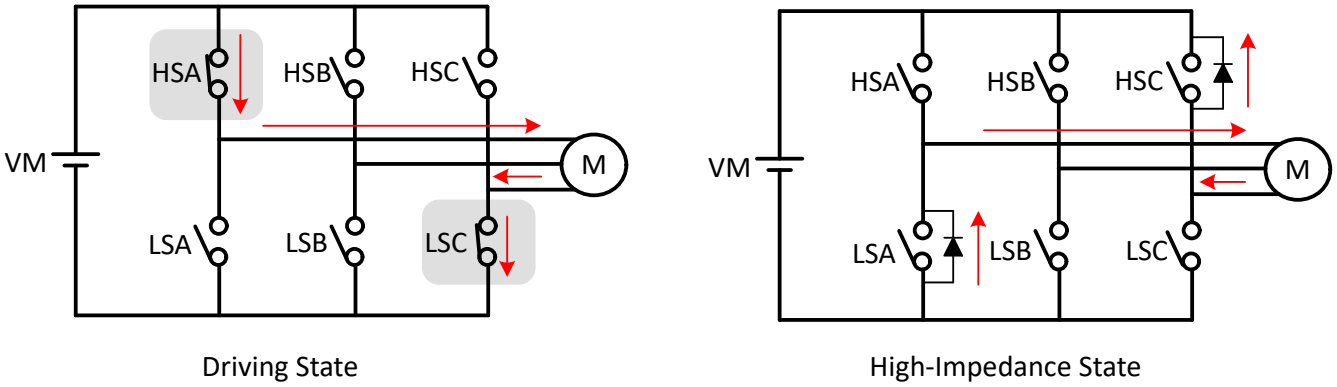


Figure 7-33. Coast (Hi-Z) Mode

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA and HSC.

7.3.18.2 Recirculation Mode

Recirculation mode is configured by setting MTR_STOP to 001b. In order to prevent the inductive energy from returning to DC input supply during motor stop, the MCT8329A allows current to circulate within the external MOSFETs by selectively turning OFF some of the active (ON) MOSFETs for a certain time (auto calculated recirculation time to allow the inductive current to decay to zero) before transitioning into Hi-Z by turning OFF the remaining MOSFETs.

If high-side modulation was active, prior to motor stop command, then the high-side MOSFET is turned OFF on receiving motor stop command and the current recirculation takes place through low-side MOSFET (see example Figure 7-34). Once the recirculation time lapses, the low-side MOSFET also turns OFF and all MOSFETs are in Hi-Z state.

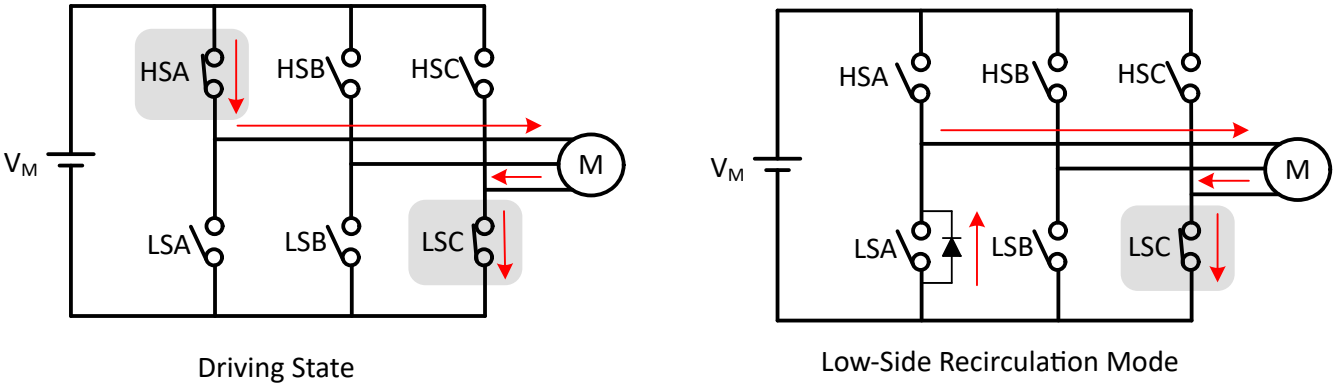


Figure 7-34. Low-Side Recirculation

If low-side modulation was active, prior to motor stop command, then the low-side MOSFET is turned OFF on receiving motor stop command and the current recirculation takes place through high-side MOSFET (see example Figure 7-35). Once the recirculation time lapses, the high-side MOSFET also turns OFF and all MOSFETs are in Hi-Z state

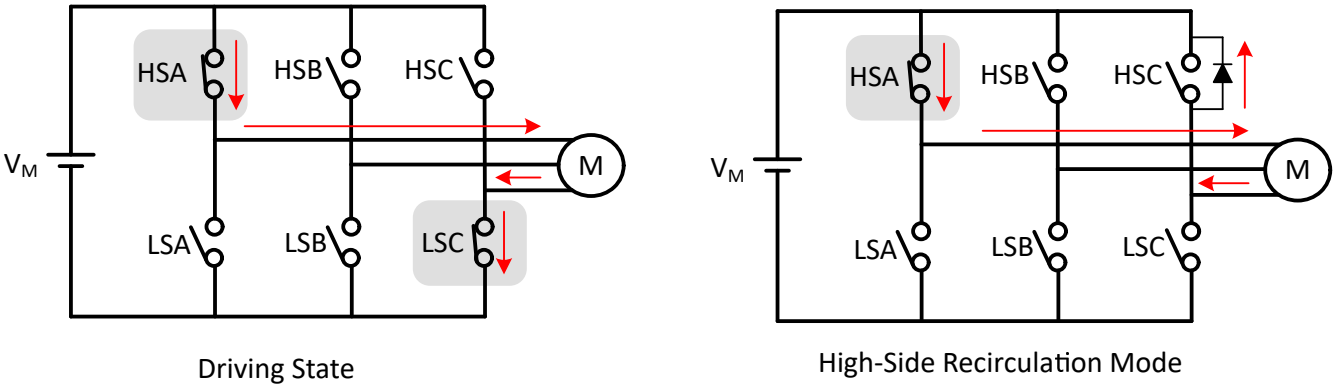


Figure 7-35. High-Side Recirculation

7.3.18.3 Low-Side Braking

Low-side braking mode is configured by setting MTR_STOP to 010b. When a motor stop command is received, the output speed is reduced to a value defined by ACT_SPIN_BRK_THR prior to turning all low-side MOSFETs ON (see example Figure 7-36) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below ACT_SPIN_BRK_THR prior to receiving stop command, then the MCT8329A transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCT8329A transitions into the Hi-Z state by turning OFF all MOSFETs.

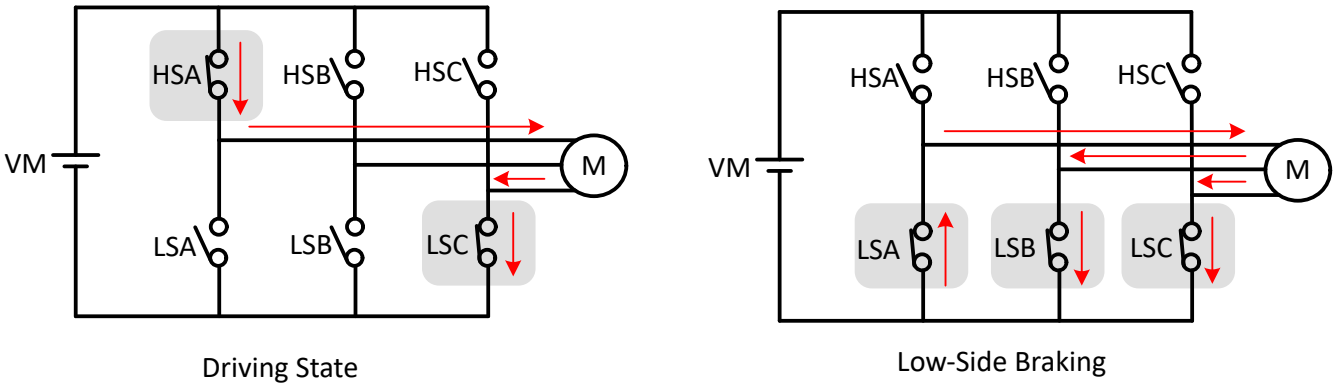


Figure 7-36. Low-Side Braking

The MCT8329A can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE_DUTY_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCT8329A stays in low-side brake state till BRAKE pin changes to LOW state.

7.3.18.4 High-Side Braking

High-side braking mode is configured by setting MTR_STOP to 011b. When a motor stop command is received, the output speed is reduced to a value defined by ACT_SPIN_BRK_THR prior to turning all high-side MOSFETs ON (see example Figure 7-37) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below ACT_SPIN_BRK_THR prior to receiving stop command, then the MCT8329A transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCT8329A transitions into Hi-Z state by turning OFF all MOSFETs.

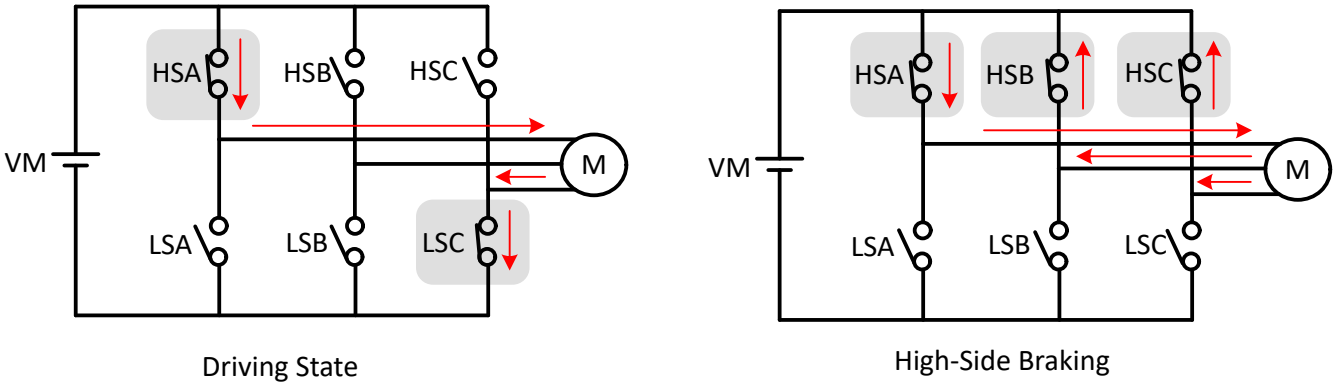


Figure 7-37. High-Side Braking

7.3.18.5 Active Spin-Down

Active spin down mode is configured by setting MTR_STOP to 100b. When motor stop command is received, MCT8329A reduces duty cycle to ACT_SPIN_BRK_THR and then transitions to Hi-Z state by turning all MOSFETs OFF. The advantage of this mode is that by reducing duty cycle, the motor is decelerated to a lower speed thereby reducing the phase currents before entering Hi-Z. Now, when motor transitions into Hi-Z state, the energy transfer to power supply is reduced. The threshold ACT_SPIN_BRK_THR needs to configured high enough for MCT8329A to not lose synchronization with the motor.

7.3.19 FG Configuration

The MCT8329A provides information about the motor speed through the Frequency Generate (FG) pin. In MCT8329A, the FG pin output is configured through FG_CONFIG. When FG_CONFIG is configured to 1b, the FG output is active as long as the MCT8329A is driving the motor. When FG_CONFIG is configured to 0b, the MCT8329A provides an FG output until the motor back-EMF falls below the threshold configured by FG_BEMF_THR.

7.3.19.1 FG Output Frequency

The FG output frequency can be configured by FG_DIV_FACTOR. In MCT8329A, FG toggles once every commutation cycle if FG_DIV_FACTOR is set to 0000b. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor. Different FG_DIV_FACTOR configurations can accomplish this for 2-pole up to 30-pole motors.

Figure 7-38 shows the FG output when MCT8329A has been configured to provide FG pulses once every commutation cycle (electrical cycle/3), once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.

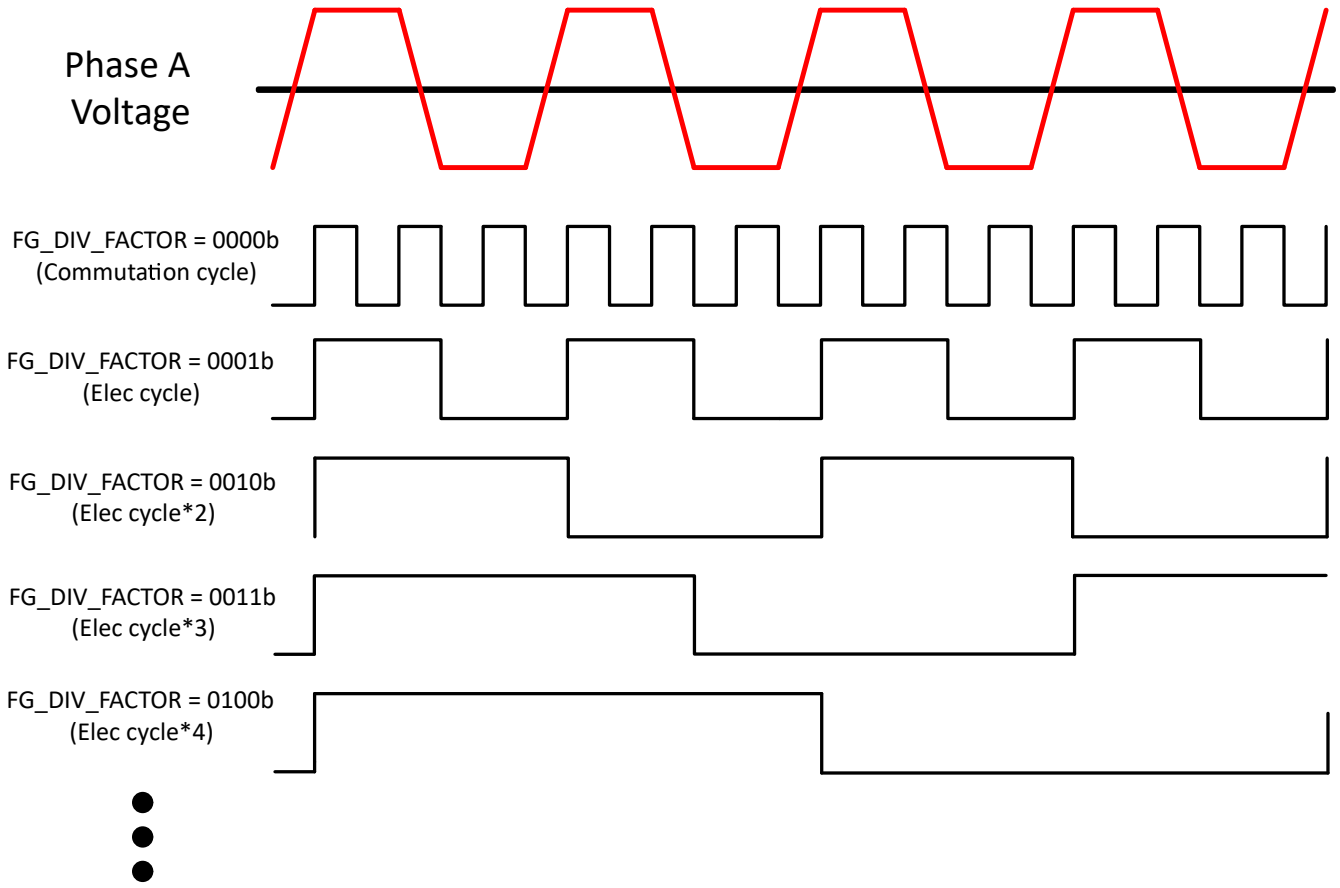


Figure 7-38. FG Frequency Divider

7.3.19.2 FG in Open-Loop

During closed loop (commutation) operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed. The open loop and closed loop here refers to the motor commutation method and not referred to closed loop speed or power control.

The MCT8329A provides three options for controlling the FG output during open loop, as shown in Figure 7-39. The selection of these options is configured through FG_SEL.

If FG_SEL is set to,

- 00b : Output FG in open loop and closed loop.
- 01b : Output FG in only closed loop. FG pin will be Hi-Z (high with external pull up) during open loop.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be Hi-Z (high with external pull up) during open loop operation in subsequent start-up cycles.

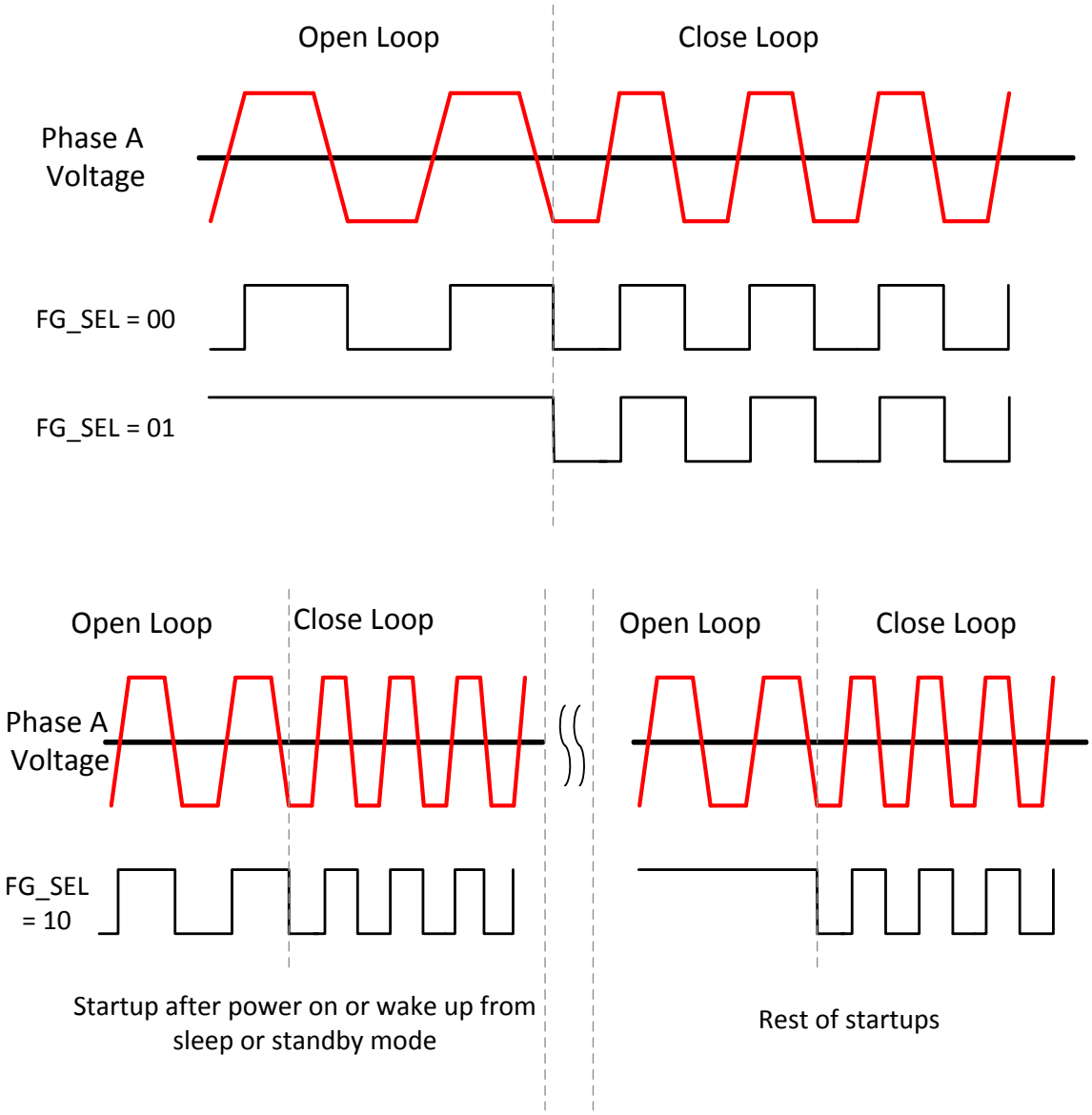


Figure 7-39. FG Behavior During Open Loop

7.3.19.3 FG During Motor Stop

The FG pin state when the motor stops rotating can be defined using FG_PIN_STOP_CONFIG. The motor stop is decided by FG_BEMF_THR.

If FG_PIN_STOP_CONFIG is set to,

- 00b: FG pin continues to toggle till motor stops. End state of FG not defined.
- 01b: FG pin in Hi-Z (high with external pull up) on motor stop.
- 10b: FG pin pulled low on motor stop.

7.3.19.4 FG Behaviour During Fault

The FG behaviour during faults (those reported on nFAULT pin) can be configured using FG_PIN_FAULT_CONFIG.

If FG_PIN_FAULT_CONFIG is set to,

- 00b: FG continues during fault as long as motor is spinning or coasting and stays at last FG level when motor stops

- 01b: FG pin in Hi-Z (high with external pull up) on reported faults.
- 10b: FG pin pulled low on fault.

7.3.20 Protections

The MCT8329A is protected from a host of fault events including motor lock, PVDD undervoltage, AVDD undervoltage, GVDD undervoltage, bootstrap undervoltage, overtemperature and overcurrent events. Table 7-2 summarizes the response, recovery modes, gate driver status, reporting mechanism for different faults.

Table 7-2. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
PVDD undervoltage (PVDD_UV)	$V_{PVDD} < V_{PVDD\_UV}$	—	nFAULT	Disabled[1]	Disabled	Automatic: $V_{PVDD} > V_{PVDD\_UV}$
AVDD POR (AVDD_POR)	$V_{AVDD} < V_{AVDD\_POR}$	—	nFAULT	Disabled[1]	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_POR}$
GVDD undervoltage (GVDD_UV)	$V_{GVDD} < V_{GVDD\_UV}$	—	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
BSTx undervoltage (BST_UV)	$V_{BSTx} - V_{SHx} < V_{BST\_UV}$	DIS_BST_FLT = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{SEL\_VDS\_LVL}$	DIS_VDS_FLT = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
V_{SENSE} overcurrent (SEN_OCP)	$V_{SP} > V_{SENSE\_LVL}$	DIS_SNS_FLT = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
3 Motor Lock (MTR_LCK)	Motor lock: Abnormal Speed; No Motor Lock; Loss of Sync	MTR_LCK_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0001b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation logic	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	High side brake logic	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake logic	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0101b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation logic	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	High side brake logic	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low side brake logic	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 1000b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		MTR_LCK_MODE = 1001b to 1111b	None	Active	Active	No action

Table 7-2. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
Cycle by Cycle Current Limit applicable for CBC_ILIMIT, OL_LIMIT, ALIGN_ILIMIT	(I x R_{SENSE}x CSA_GAIN) > ILIMIT	CBC_ILIMIT_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation logic	Active	Automatic: Next PWM cycle
		CBC_ILIMIT_MODE = 0001b	None	Recirculation logic	Active	Automatic: Next PWM cycle
		CBC_ILIMIT_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation logic	Active	Automatic: (I x R_{SENSE}x CSA_GAIN) < ILIMIT
		CBC_ILIMIT_MODE = 0011b	None	Recirculation logic	Active	Automatic: (I x R_{SENSE}x CSA_GAIN) < ILIMIT
		CBC_ILIMIT_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation logic	Active	Automatic: PWM cycle > CBC_RETRY_PWM_CYC
		CBC_ILIMIT_MODE = 0101b	None	Recirculation logic	Active	Automatic: PWM cycle > CBC_RETRY_PWM_CYC
		CBC_ILIMIT_MODE= 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		CBC_ILIMIT_MODE = 0111b, 1xxxb	None	Active	Active	No action
Lock-Detection Current Limit (LOCK_ILIMIT)	(I x R_{SENSE}x CSA_GAIN) > LOCK_ILIMIT	LOCK_ILIMIT_MODE = 0000b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0001b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation logic	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0010b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake logic	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake logic	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0100b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0101b	nFAULT and CONTROLLER_FAULT_STATUS register	Recirculation logic	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0110b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake logic	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake logic	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE= 1000b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		LOCK_ILIMIT_MODE = 1001b 1111b	None	Active	Active	No action
IPD Timeout Fault (IPD_T1_FAULT and IPD_T2_FAULT)	IPD TIME > 500ms (approx), during IPD current ramp up or ramp down	—	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
IPD Frequency Fault (IPD_FREQ_FAULT)	IPD pulse before the current decay in previous IPD	—	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT

Table 7-2. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
Thermal shutdown (TSD)	$T_J > T_{TSD}$	OTS_AUTO_RECOVERY = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
		OTS_AUTO_RECOVERY = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$ CLR_FLT

1. Disabled: Passive pull down for GLx and semi-active pull down for GHx
2. Pulled Low: GHx and GLx are actively pulled low by the gate driver

7.3.20.1 PVDD Supply Undervoltage Lockout (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD\_UV\_DG}$ time, the device detects a PVDD undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, the charge pump is disabled, the internal digital logic is disabled, and the nFAULT pin is driven low. Normal operation starts again (the gate driver becomes operable and the nFAULT pin is released) when the PVDD pin rises above V_{PVDD_UV}.

7.3.20.2 AVDD Power on Reset (AVDD_POR)

If at any time the supply voltage on the AVDD pin falls below the V_{AVDD_POR} threshold for longer than the $t_{AVDD\_POR\_DG}$ time, the device enters an inactive state, disabling the gate driver, the charge pump, and the internal digital logic, and nFAULT is driven low. Normal operation (digital logic operational) requires AVDD to exceed V_{AVDD_POR} level.

7.3.20.3 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold voltage for longer than the $t_{GVDD\_UV\_DG}$ time, the device detects a GVDD undervoltage event. After detecting the GVDD_UV undervoltage event, all of the gate driver outputs are driven low to disable the external MOSFETs, the charge pump is still running and nFAULT pin is driven low. Normal operation resumes after the GVDD_UV condition is cleared and a clear fault command is issued through the CLR_FLT bit.

7.3.20.4 BST Undervoltage Lockout (BST_UV)

If at any time the voltage across BSTx and SHx pins falls lower than the V_{BST_UV} threshold voltage for longer than the $t_{BST\_UV\_DG}$ time, the device detects a BST undervoltage event. After detecting the BST_UV event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. Normal operation resumes after the BST_UV condition is cleared and a clear fault command is issued through the CLR_FLT bit.

7.3.20.5 MOSFET VDS Overcurrent Protection (VDS_OCP)

The device has adjustable VDS voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the VDS voltage drop across the external MOSFET $R_{DS(on)}$. The high-side VDS monitors measure between the PVDD and SHx pins and the low-side VDS monitors measure between the SHx and LSS pins. If the voltage across external MOSFET exceeds the threshold set by SEL_VDS_LVL for longer than the t_{DS_DG} deglitch time, a V_{DS_OCP} event is recognized. After detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. V_{DS_OCP} can be disabled by configuring DIS_VDS_FLT to 1b. Normal operation resumes after the V_{DS_OCP} condition is cleared and a clear fault command is issued through the CLR_FLT bit.

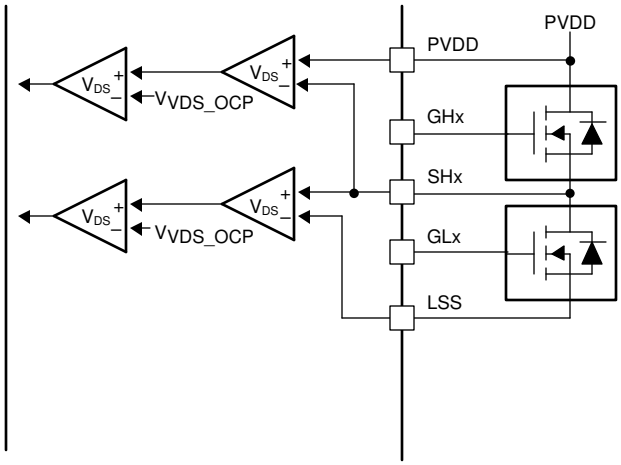


Figure 7-40. MCT8329A VDS Monitors

7.3.20.6 VSENSE Overcurrent Protection (SEN_OCP)

Overcurrent is also monitored by sensing the voltage drop across the external current sense resistor between LSS and GND pin. If at any time the voltage on the LSS input exceeds the VSEN_OCP threshold for longer than the t_{DS_DG} deglitch time, a SEN_OCP event is recognized. After detecting the SEN_OCP overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The V_{SENSE} threshold is fixed at 0.5 V. V_{SEN_OCP} can be disabled by configuring DIS_SNS_FLT to 1b. Normal operation resumes after the V_{SEN_OCP} condition is cleared and a clear fault command is issued through the CLR_FLT bit.

7.3.20.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), an OTSD event is recognized. After detecting the OTSD overtemperature event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. The over temperature protection can be configured for a latched mode or automatic recovery mode by configuring OTS_AUTO_RECOVERY. In latched mode, normal operation resumes after the T_{OTSD} condition is cleared and a clear fault command is issued through the CLR_FLT bit. In automatic recovery mode, normal operation resumes after the T_{OTSD} condition is cleared.

7.3.20.8 Cycle-by-Cycle (CBC) Current Limit (CBC_ILIMIT)

Cycle-by-cycle (CBC) current limit provides a means of controlling the amount of current delivered to the motor. This is useful when the system must limit the amount of current pulled from the power supply during motor operation. The CBC current limit limits the current applied to the motor from exceeding the configured threshold. CBC current limit functionality is achieved by connecting the output of current sense amplifier to a hardware comparator. If the voltage at output of current sense amplifier exceeds the CBC_ILIMIT threshold, a CBC_ILIMIT event is recognized and action is taken according to CBC_ILIMIT_MODE. Total delay in reaction to this event is dependent on the current sense amplifier gain and the comparator delay. CBC current limit in closed loop is set through CBC_ILIMIT while configuration of OL_ILIMIT_CONFIG sets the CBC current limit in open loop operation. Different modes can be configured through CBC_ILIMIT_MODE: CBC_ILIMIT automatic recovery next PWM cycle, CBC_ILIMIT automatic recovery threshold based, CBC_ILIMIT automatic recovery number of PWM cycles based, CBC_ILIMIT report only, CBC_ILIMIT disabled.

7.3.20.8.1 CBC_ILIMIT Automatic Recovery next PWM Cycle (CBC_ILIMIT_MODE = 000xb)

When a CBC_ILIMIT event happens in this mode, MCT8329A stops driving the FETs using recirculation mode to prevent the inductive energy from entering the DC input supply. The CBC_ILIMIT status bit is set to 1b in the fault status registers. Normal operation resumes at the start of next PWM cycle and CBC_ILIMIT status bit is reset to 0b. The status of CONTROLLER_FAULT bit and nFAULT pin will be determined by CBC_ILIMIT_MODE. When CBC_ILIMIT_MODE is 0000b, CONTROLLER_FAULT bit is set to 1b and nFAULT pin driven low until next PWM cycle. When CBC_ILIMIT_MODE is 0001b, CONTROLLER_FAULT bit is not set to 1b and nFAULT is not driven low.

7.3.20.8.2 CBC_ILIMIT Automatic Recovery Threshold Based (CBC_ILIMIT_MODE = 001xb)

When a CBC_ILIMIT event happens in this mode, MCT8329A stops driving the FETs using recirculation mode to prevent the inductive energy from entering the DC input supply. The CBC_ILIMIT status bit is set to 1b in the status registers. Normal operation resumes after the current falls below CBC_ILIMIT current threshold and CBC_ILIMIT status bit is set to 0b. The status of CONTROLLER_FAULT bit and nFAULT pin will be determined by CBC_ILIMIT_MODE. When CBC_ILIMIT_MODE is 0010b, CONTROLLER_FAULT bit is set to 1b and nFAULT pin driven low until current falls below CBC_ILIMIT current threshold. When CBC_ILIMIT_MODE is 0011b, CONTROLLER_FAULT bit is not set to 1b and nFAULT is not driven low.

7.3.20.8.3 CBC_ILIMIT Automatic Recovery after 'n' PWM Cycles (CBC_ILIMIT_MODE = 010xb)

When a CBC_ILIMIT event happens in this mode, MCT8329A stops driving the FETs using recirculation mode to prevent the inductive energy from entering the DC input supply. The CBC_ILIMIT status bit is set to 1b in the fault status registers. Normal operation resumes after (CBC_RETRY_PWM_CYC +1) PWM cycles and CBC_ILIMIT status bit is set to 0b. The status of CONTROLLER_FAULT bit and nFAULT pin will be determined by CBC_ILIMIT_MODE. When CBC_ILIMIT_MODE is 0100b, CONTROLLER_FAULT bit is set to1b and nFAULT pin driven low until (CBC_RETRY_PWM_CYC +1) PWM cycles lapse. When CBC_ILIMIT_MODE is 0101b, CONTROLLER_FAULT bit is not set to 1b and nFAULT is not driven low.

7.3.20.8.4 CBC_ILIMIT Report Only (CBC_ILIMIT_MODE = 0110b)

No protective action is taken when a CBC_ILIMIT event happens in this mode. The CBC current limit event is reported by setting the CONTROLLER_FAULT and CBC_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages the overcurrent condition by acting appropriately. The reporting clears when the CBC_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.20.8.5 CBC_ILIMIT Disabled (CBC_ILIMIT_MODE = 0111b or 1xxxb)

No action is taken when a CBC_ILIMIT event happens in this mode.

Note

In CBC_ILIMIT disabled mode and CBC_ILIMIT report only mode, when the motor is driven at 100% PWM duty (no switching) and if the current goes more than the CBC_ILIMIT current threshold, the gate driver pulls the high side gate driver output to low momentarily, at the set PWM_FREQ_OUT. To eliminate such unwanted switching at 100% duty cycle, the CBC_LIMIT threshold can be set to a high value more than the expected motor current during CBC_ILIMIT disabled mode and CBC_ILIMIT report only mode.

7.3.20.9 Lock Detection Current Limit (LOCK_ILIMIT)

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCT8329A continuously monitors the output of the current sense amplifier (CSA) through the ADC. If at any time, the voltage on the output of CSA exceeds LOCK_ILIMIT for a time longer than t_{LCK_ILIMIT}, a LOCK_ILIMIT event is recognized and action is taken according to LOCK_ILIMIT_MODE. The threshold is set through LOCK_ILIMIT, the t_{LCK_ILIMIT} is set through LOCK_ILIMIT_DEG. LOCK_ILIMIT_MODE can be set to four different modes: LOCK_ILIMIT latched shutdown, LOCK_ILIMIT automatic retry, LOCK_ILIMIT report only and LOCK_ILIMIT disabled.

7.3.20.9.1 LOCK_ILIMIT Latched Shutdown (LOCK_ILIMIT_MODE = 00xxb)

When a LOCK_ILIMIT event happens in this mode, the status of external MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of external MOSFETs driven from MCT8329A during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 0000b: All MOSFETs are turned OFF, the gate driver outputs pulled low.
- LOCK_ILIMIT_MODE = 0001b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.
- LOCK_ILIMIT_MODE = 0010b: All high-side MOSFETs (gate driver outputs) are turned ON.
- LOCK_ILIMIT_MODE = 0011b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.20.9.2 LOCK_ILIMIT Automatic Recovery (LOCK_ILIMIT_MODE = 01xxb)

When a LOCK_ILIMIT event happens in this mode, the status of external MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of external MOSFETs driven from MCT8329A during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 0100b: All MOSFETs are turned OFF, the gate driver outputs pulled low.
- LOCK_ILIMIT_MODE = 0101b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.
- LOCK_ILIMIT_MODE = 0110b: All high-side MOSFETs (gate driver outputs) are turned ON
- LOCK_ILIMIT_MODE = 0111b: All low-side MOSFETs (gate driver outputs) are turned ON

The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT and LOCK_ILIMIT bits are reset to 0b after the t_{LCK_RETRY} period expires.

7.3.20.9.3 LOCK_ILIMIT Report Only (LOCK_ILIMIT_MODE = 1000b)

No protective action is taken when a LOCK_ILIMIT event happens in this mode. The lock detection current limit event is reported by setting the CONTROLLER_FAULT and LOCK_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.20.9.4 LOCK_ILIMIT Disabled (LOCK_ILIMIT_MODE = 1xx1b)

No action is taken when a LOCK_ILIMIT event happens in this mode.

7.3.20.10 Motor Lock (MTR_LCK)

The MCT8329A continuously checks for different motor lock conditions (see Motor Lock Detection) during motor operation. When one of the enabled lock condition happens, a MTR_LCK event is recognized and action is taken according to the MTR_LCK_MODE.

In MCT8329A, all locks can be enabled or disabled individually and retry times can be configured through LCK_RETRY. MTR_LCK_MODE bit can operate in four different modes: MTR_LCK latched shutdown, MTR_LCK automatic retry, MTR_LCK report only and MTR_LCK disabled.

7.3.20.10.1 MTR_LCK Latched Shutdown (MTR_LCK_MODE = 00xxb)

When a MTR_LCK event happens in this mode, the status of external MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of external MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0000b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR_LCK_MODE = 0001b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.
- MTR_LCK_MODE = 0010b: All high-side MOSFETs (gate driver outputs) are turned ON.
- MTR_LCK_MODE = 0011b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.20.10.2 MTR_LCK Automatic Recovery (MTR_LCK_MODE= 01xxb)

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0100b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR_LCK_MODE = 0101b: MOSFET which was switching is turned OFF while the one which was conducting stays ON till inductive energy is completely recirculated.

- MTR_LCK_MODE = 0110b: All high-side MOSFETs (gate driver outputs) are turned ON.
- MTR_LCK_MODE = 0111b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are reset to 0b after the t_{LCK_RETRY} period expires.

7.3.20.10.3 MTR_LCK Report Only (MTR_LCK_MODE = 1000b)

No protective action is taken when a MTR_LCK event happens in this mode. The motor lock event is reported by setting the CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.20.10.4 MTR_LCK Disabled (MTR_LCK_MODE = 1xx1b)

No action is taken when a MTR_LCK event happens in this mode.

7.3.20.11 Motor Lock Detection

The MCT8329A provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCT8329A can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits.

7.3.20.11.1 Lock 1: Abnormal Speed (ABN_SPEED)

MCT8329A monitors the speed continuously and at any time the speed exceeds LOCK_ABN_SPEED, an ABN_SPEED lock event is recognized and action is taken according to the MTR_LCK_MODE.

The threshold is set through the LOCK_ABN_SPEED register. ABN_SPEED lock can be enabled/disabled by ABN_SPD_EN.

7.3.20.11.2 Lock 2: Loss of Sync (LOSS_OF_SYNC)

The motor is commutated by detecting the zero crossing on the phase which is in Hi-Z state. If the motor is locked, the back-EMF will disappear and MCT8329A will be not able to detect the zero crossing. If MCT8329A is not able to detect zero crossing for LOSS_SYNC_TIMES number of times, LOSS_OF_SYNC event is recognized and action is taken according to the MTR_LCK_MODE. LOSS_OF_SYNC lock can be enabled/disabled by LOSS_OF_SYNC_EN.

7.3.20.11.3 Lock3: No-Motor Fault (NO_MTR)

The MCT8329A continuously monitors the relevant phase current (low-side phase in the present phase pattern); if the relevant phase current stays below NO_MTR_THR for a time longer than NO_MTR_DEG_TIME, a NO_MTR event is recognized. The response to the NO_MTR event is configured through MTR_LCK_MODE . NO_MTR lock can be enabled/disabled by NO_MOTOR_EN.

7.3.20.12 IPD Faults

The MCT8329A uses 12-bit timers to estimate the time during the current ramp up and ramp down during IPD, when the motor start-up is configured as IPD (MTR_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD_CURR_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD_CURR_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD_CURR_THR) with all the four clock frequencies, then the IPD_T1_FAULT gets triggered. Similarly the algorithm checks for a successful current decay to zero during IPD current ramp down using all the mentioned IPD clock frequencies. If the IPD timer overflows (current does not ramp down to zero) in all the four attempts, then the IPD_T2_FAULT gets triggered.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCT8329A can generate a fault called IPD_FREQ_FAULT during such a scenario . The IPD_FREQ_FAULT maybe triggered if the IPD frequency is too high for the IPD current limit or if the motor inductance is too high for the IPD frequency and IPD current limit.

7.4 Device Functional Modes

7.4.1 Functional Modes

7.4.1.1 Sleep Mode

In sleep mode all gate drivers are disabled, the GVDD regulator is disabled ,the AVDD regulator is disabled, the sense amplifier, and the I^2C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV_MODE to 1b. The entry and exit from sleep state as described in Table 7-3.

Note

During power-up and power-down of the device, the nFAULT pin is held low as the internal regulators are disabled. After the regulators have been enabled, the nFAULT pin is automatically released.

7.4.1.2 Standby Mode

In standby mode the gate driver, AVDD LDO and I^2C bus are active. The device can be configured to enter standby mode by configuring DEV_MODE to 0b. The entry and exit from standby state is described in Table 7-3. The standby entry and exit criteria for different input modes (analog or PWM or frequency of I^2C) can be derived using Equation 12 through Equation 19.

$$V_{EN\_SB}(V) = ZERO\_DUTY\_THR \times V_{ANA\_FS}(V) \quad (12)$$

$$V_{EX\_SB}(V) = \left(ZERO\_DUTY\_THR + ZERO\_DUTY\_HYST\right) \times V_{ANA\_FS}(V) \quad (13)$$

$$DUTY_{EN\_SB}(V) = ZERO\_DUTY\_THR \quad (14)$$

$$DUTY_{EX\_SB}(V) = ZERO\_DUTY\_THR + ZERO\_DUTY\_HYST \quad (15)$$

$$F_{EN\_SB}(V) = ZERO\_DUTY\_THR \times INPUT\_MAX\_FREQUENCY(Hz) \quad (16)$$

$$F_{EX\_SB}(V) = \left(ZERO\_DUTY\_THR + ZERO\_DUTY\_HYST\right) \times INPUT\_MAX\_FREQUENCY(Hz) \quad (17)$$

$$SPEED\_CTRL_{EN\_SB}(V) = ZERO\_DUTY\_THR \times 32767 \quad (18)$$

$$SPEED\_CTRL_{EX\_SB}(V) = \left(ZERO\_DUTY\_THR + ZERO\_DUTY\_HYST\right) \times 32767 \quad (19)$$

Table 7-3. Conditions to Enter or Exit Sleep or Standby Modes

SPEED COMMAND MODE	ENTER STANDBY CONDITION, DEV_MODE = 0b	EXIT FROM STANDBY CONDITION	ENTER SLEEP CONDITION, DEV_MODE = 1b	EXIT FROM SLEEP CONDITION
Analog input at SPEED/ WAKE pin	SPEED/WAKE pin voltage < V_{EN_SB})	SPEED/WAKE pin voltage > V_{EX_SB}) for t_{DET_ANA}	SPEED/WAKE pin voltage < V_{EN_SL}; for $t_{DET\_SL\_ANA}$ (SPD_CTRL_MODE = 00b or 01b) or for $t_{DET\_SL\_PWM}$ (SPD_CTRL_MODE = 10b or 11b).	SPEED/WAKE pin high (V > V_{IH} for t_{DET_ANA}
Analog input at DACOUT/SOx/ SPEED_ANA pin	DACOUT/SOx/SPEED_ANA pin voltage < V_{EN_SB} or SPEED/WAKE pin low (V < V_{IL}) for $t_{EN\_SB\_PWM}$	DACOUT/SOx/SPEED_ANA pin voltage > V_{EX_SB} for t_{DET_ANA} and SPEED/WAKE pin high (V > V_{IH}) for t_{DET_PWM}	SPEED/WAKE pin low (V < V_{IL}) for $t_{DET\_SL\_PWM}$	SPEED/WAKE pin high (V > V_{IH}) for t_{DET_PWM}
PWM	SPEED/WAKE pin PWM Duty < $DUTY_{EN\_SB}$	SPEED/WAKE pin PWM Duty > $DUTY_{EX\_SB}$	SPEED/WAKE pin low (V < V_{IL}) for $t_{DET\_SL\_PWM}$	SPEED/WAKE pin high (V > V_{IH}) for t_{DET_PWM}

Table 7-3. Conditions to Enter or Exit Sleep or Standby Modes (continued)

SPEED COMMAND MODE	ENTER STANDBY CONDITION, DEV_MODE = 0b	EXIT FROM STANDBY CONDITION	ENTER SLEEP CONDITION, DEV_MODE = 1b	EXIT FROM SLEEP CONDITION
Frequency	SPEED/WAKE pin frequency < F_{EN_SB}	SPEED/WAKE pin frequency > F_{EX_SB}	SPEED/WAKE pin low (V < V_{IL}) for $t_{DET\_SL\_PWM}$	SPEED/WAKE pin high (V > V_{IH}) for t_{DET_PWM}
I^2C	SPEED_CTRL < $SPEED\_CTRL_{EN\_SB}$	SPEED_CTRL > $SPEED\_CTRL_{EX\_SB}$	SPEED/WAKE pin voltage < V_{IL} for $t_{DET\_SL\_PWM}$ and SPEED_CTRL is programmed as 0.	SPEED/WAKE pin voltage > V_{IH} for t_{DET_PWM}

7.4.1.3 Fault Reset (CLR_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR_FLT to 1b.

7.5 External Interface

7.5.1 DRVOFF - Gate Driver Shutdown Functionality

When DRVOFF is driven high, the gate driver goes into shutdown. DRVOFF bypasses the digital control logic inside the device, and is connected directly to the gate driver output (see Figure 7-41). This pin provides a mechanism for externally monitored faults to disable gate driver by directly bypassing the internal control logic. When MCT8329A detect logic high on the DRVOFF pin, the device disables the gate driver and puts it into pull down mode (see Figure 7-42). The gate driver shutdown sequence proceeds as shown in Figure 7-42. When the gate driver initiates the shutdown sequence, the active driver pull down is applied at I_{SINK} current for the $t_{SD\_SINK\_DIG}$ time, after which the gate driver moves to passive pull down mode.

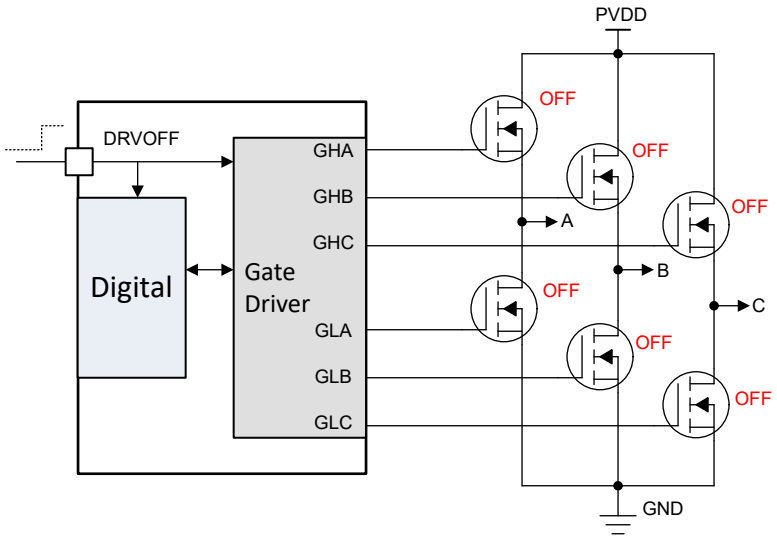


Figure 7-41. DRVOFF Gate Driver Output State

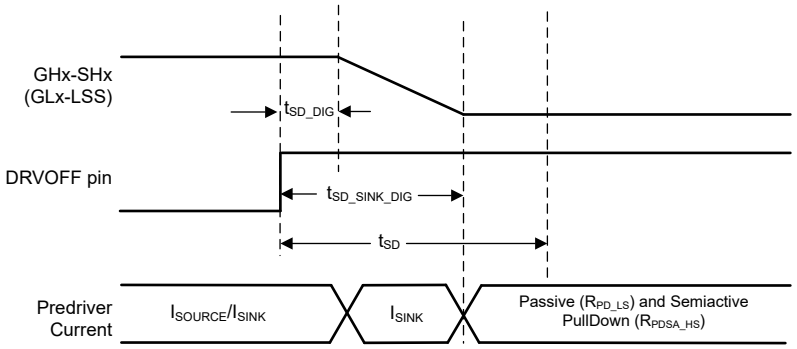


Figure 7-42. Gate Driver Shutdown Sequence

DRVOFF pin pulling high does not cause the device to go to sleep or standby mode and the digital core is still active. The DRVOFF status is reported on DRV_OFF bit and has a latency of up to 100 ms between the pin status change to DRV_OFF bit status update. The controller may report motor fault when DRVOFF goes logic high during motor operation. When DRVOFF pulled from high to low, MCT8329A execute motor start sequence (with a latency up to 100 ms after pulling DRVOFF pin low) as described in Section 7.3.9.

7.5.2 DAC outputs

MCT8329A has12-bit DACs which output analog voltage equivalent of digital variables on DACOUT pin with resolution of 12 bits and maximum voltage is 3-V. Signals available on DACOUT pins is useful in tracking algorithm variables in real-time and can be used for tuning speed controller or motor acceleration time. The address for variables for DACOUT is configured using DACOUT_VAR_ADDR.

Note

The DACOUT value for a selected variable may not be accurate during fault, brake, or HiZ states.

7.5.3 Current Sense Amplifier Output

MCT8329A can provide the built-in current sense amplifier's output on the DACOUT/SOx/SPEED_ANA pin by configuring DACOUT/SOx/SPEED_ANA.

7.5.4 Oscillator Source

MCT8329A has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCT832A9 is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In case MCT8329A does not meet accuracy requirements of timing measurement or speed loop, then MCT8329A has an option to support an external clock reference.

In order to improve EMI performance, MCT8329A provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SSM_CONFIG

.

7.5.4.1 External Clock Source

Speed loop accuracy of MCT8329A over wide operating temperature range can be improved by providing more accurate optional clock reference on EXT_CLK pin as shown in Figure 7-43. EXT_CLK will be used to calibrate internal clock oscillator and match the accuracy of the external clock. External clock source can be selected by configuring CLK_SEL to 11b and setting EXT_CLK_EN to 1b. The external clock source frequency can be configured through EXT_CLK_CONFIG.

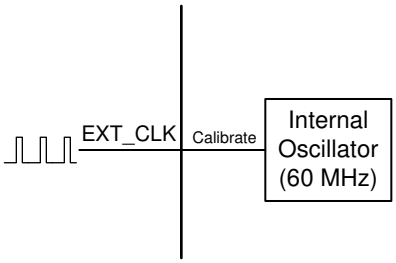


Figure 7-43. External Clock Reference

Note

External clock is optional and can be used when higher clock accuracy is needed. MCT8329A will always power up using the internal oscillator in all modes.

7.6 EEPROM access and I²C interface

7.6.1 EEPROM Access

MCT8329A has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I²C serial interface but erase cannot be performed using I²C serial interface. The shadow registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

Note

MCT8329A allows EEPROM write and read operations only when the motor is not spinning.

7.6.1.1 EEPROM Write

In MCT8329A, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD_CONFIG) with ISD configuration like resync enable, reverse drive enable, stationary detect threshold etc.,
2. Write register 0x000082 (MOTOR_STARTUP1) with motor start-up configuration like start-up method, first cycle frequency, IPD parameters, align parameters etc.,
3. Write register 0x000084 (MOTOR_STARTUP2) with motor start-up configuration like open loop acceleration, minimum duty cycle etc.,
4. Write register 0x000086 (CLOSED_LOOP1) with motor control configuration like closed loop acceleration, PWM frequency, PWM modulation etc.,
5. Write register 0x000088 (CLOSED_LOOP2) with motor control configuration like FG signal parameters, motor stop options etc.,
6. Write register 0x00008A (CLOSED_LOOP3) with motor control configuration like dynamic degauss parameters, BEMF thresholds, duty cycle thresholds etc.,
7. Write register 0x00008C (CLOSED_LOOP4) with motor control configuration like fast deceleration parameters including fast deceleration duty threshold, window, current limits etc.,
8. Write register 0x00008E (CONST_SPEED) with motor control configuration like speed loop parameters including closed loop mode, saturation limits, K_p, K_i etc.,
9. Write register 0x000090 (CONST_PWR) with motor control configuration like input power regulation parameters including maximum power, constant power mode, power level hysteresis, maximum speed etc.,
10. Write register 0x000092 (FAULT_CONFIG1) with fault control configuration like CBC, lock current limits and actions, retry times etc.,
11. Write register 0x000094 (FAULT_CONFIG2) with fault control configuration like OV, UV limits and actions, abnormal speed level, motor lock setting etc.,
12. Write registers 0x000096 and 0x000098 (150_DEG_TWO_PH_PROFILE, 150_DEG_THREE_PH_PROFILE) with PWM duty cycle configurations for 150^o modulation.
13. Write registers 0x00009A, 0x00009C, 0x00009E, 0x0000A0, 0x0000A2, 0x0000A4 (REF_PROFILES1 to REF_PROFILES6) with input profile configuration like profile type, duty cycle, clamp level etc.
14. Write registers 0x0000A6 and 0x0000A8 (PIN_CONFIG1 and PIN_CONFIG2) with pin configuration for DIR, BRAKE, DACOUT etc.,
15. Write register 0x0000AA (DEVICE_CONFIG) with device configuration like device mode, external clock enable, clock source, input PWM frequency range etc.,
16. Write registers 0x0000AC and 0x0000AE (GD_CONFIG1 and GD_CONFIG2) with gate driver configuration like CSA configurations, gate driver protections etc.
17. Write 0x8A500000 into register 0x0000E6 to write the shadow register (0x000080-0x0000AE) values into the EEPROM.
18. Wait for 300ms for the EEPROM write operation to complete

Steps 1-16 can be selectively executed based on registers/parameters that need to be modified. After all shadow registers have been updated with the required values, step 17 should be executed to copy the contents of the shadow registers into the EEPROM.

Note

EEPROM reserved bit field defaults settings must not be changed. To avoid changing the content of reserved bits, TI recommends using “read-modify-write” sequence to perform EEPROM write operation.

7.6.1.2 EEPROM Read

In MCT8329A, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000E6 to read the EEPROM data into the shadow registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow register values, 1 or 2 registers at a time, using the I^{2}C read command as explained in Section 7.6.2. Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

7.6.2 I^{2}C Serial Interface

MCT8329A interfaces with an external MCU over an I^{2}C serial interface. MCT8329A is an I^{2}C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCT8329A

Note

For reliable communication, a 100-µs delay should be used between every byte transferred over the I^{2}C bus.

7.6.2.1 I^{2}C Data Word

The I^{2}C data word format is shown in Table 7-4.

Table 7-4. I^{2}C Data Word Format

TARGET_ID	R/W	CONTROL WORD	DATA	CRC-8
A6 - A0	W0	CW23 - CW0	D15 / D31/ D63 - D0	C7 - C0

Target ID and R/W Bit: The first byte includes the 7-bit I^{2}C target ID (0x60), followed by the read/write command bit. Every packet in MCT8329A the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

24-bit Control Word: The Target Address is followed by a 24-bit control bit. The control word format is shown in Table 7-5.

Table 7-5. 24-bit Control Word Format

OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR
CW23	CW22	CW21- CW20	CW19 - CW16	CW15 - CW12	CW11 - CW0

Each field in the control word is explained in detail below.

OP_R/W – Read/Write: R/W bit gives information on whether this is a read operation or write operation. Bit value 0 indicates it is a write operation. Bit value 1 indicates it is a read operation. For write operation, MCT8329A will expect data bytes to be sent after the 24-bit control word. For read operation, MCT8329A will expect an I^{2}C read request with repeated start or normal start after the 24-bit control word.

CRC_EN – Cyclic Redundancy Check(CRC) Enable: MCT8329A supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

DLEN – Data Length: DLEN field determines the length of the data that will be sent by external MCU to MCT8329A. MCT8329A protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

Table 7-6. Data Length Configuration

DLEN Value	Data Length
00b	16-bit
01b	32-bit
10b	64-bit
11b	Reserved

MEM_SEC – Memory Section: Each memory location in MCT8329A is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

MEM_PAGE – Memory Page: Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

MEM_ADDR – Memory Address: Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCT8329A using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800)

Data Bytes: For a write operation to MCT8329A, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section.

CRC Byte: If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Procedure to calculate CRC is explained in CRC Byte Calculation below.

7.6.2.2 I^2C Write Operation

MCT8329A write operation over I^2C involves the following sequence.

1. I^2C start condition.
2. The sequence starts with I^2C target start byte, made up of 7-bit target ID (0x60) to identify the MCT8329A along with the R/W bit set to 0.
3. The start byte is followed by 24-bit control word. Bit 23 in the control word has to be 0 as it is a write operation.
4. The 24-bit control word is then followed by the data bytes. The length of the data byte depends on the DLEN field.
   a. While sending data bytes, the LSB byte is sent first. Refer below examples for more details.
   b. 16-bit/32-bit write – The data sent is written to the address mentioned in Control Word.
   c. 64-bit Write – 64-bit is treated as two 32-bit writes. The address mentioned in Control word is taken as Addr 0. Addr 1 is calculating internally by MCT8329A by incrementing Addr 0 by 2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first way) are written to Addr 0 and the next 4 bytes are written to Addr 1.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes).
6. I^2C stop condition.

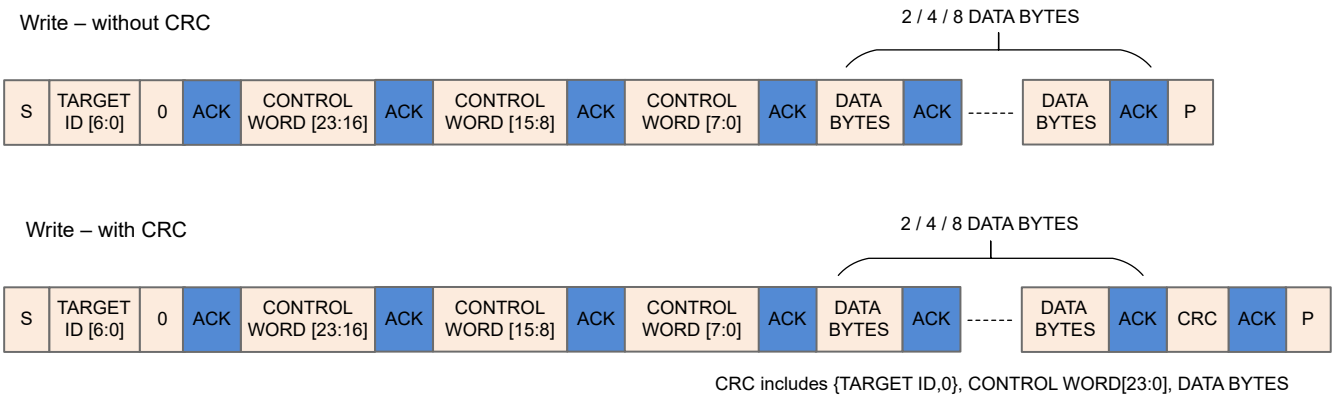


Figure 7-44. I²C Write Operation Sequence

7.6.2.3 I²C Read Operation

MCT8329A read operation over I²C involves the following sequence.

1. I²C start condition.
2. The sequence starts with I²C target Start Byte.
3. The Start Byte is followed by 24-bit Control Word. Bit 23 in the control word has to be 1 as it is a read operation.
4. The control word is followed by a repeated start or normal start.
5. MCT8329A sends the data bytes on SDA. The number of bytes sent by MCT8329A depends on the DLEN field value in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer the examples below for more details.
   b. 16-bit/32-bit Read – The data from the address mentioned in Control Word is sent back.
   c. 64-bit Read – 64-bit is treated as two 32-bit read. The address mentioned in Control Word is taken as Addr 0. Addr 1 is calculating internally by MCT8329A by incrementing Addr 0 by 2. A total of 8 data bytes are sent by MCT8329A. The first 4 bytes (sent in LSB first way) are read from Addr 0 and the next 4 bytes are read from Addr 1.
   d. MCT8329A takes some time to process the control word and read data from the given address. This involves some delay. It is quite possible that the repeated start with Target ID will be NACK'd. If the I²C read request has been NACK'd by MCT8329A, retry after few cycles. During this retry, it is not necessary to send the entire packet along with the control word. It is sufficient to send only the start condition with target ID and read bit.
6. If CRC is enabled, then MCT8329A sends an additional CRC byte at the end. If CRC is enabled, external MCU I²C controller has to read this additional byte before sending the stop bit. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I²C stop condition.

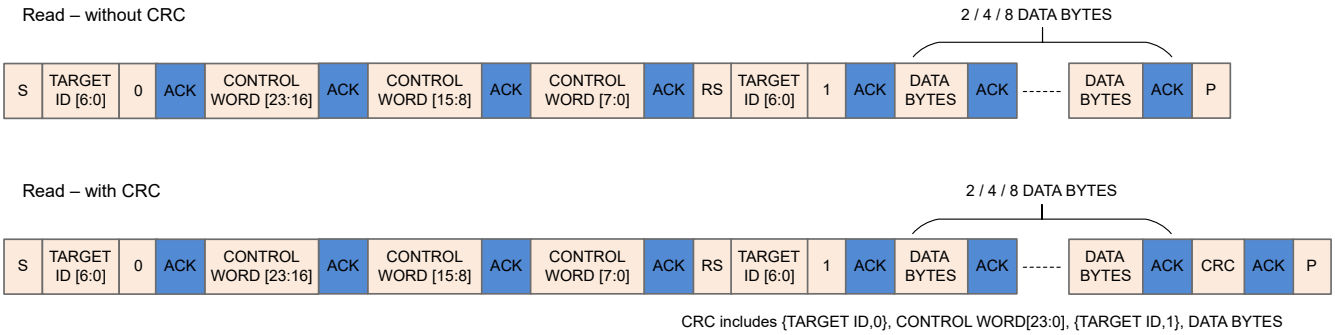


Figure 7-45. I²C Read Operation Sequence

7.6.2.4 Examples of I²C Communication Protocol Packets

All values used in this example section are in hex format. I²C target ID used in the examples is 0x00.

Example for 32-bit Write Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-7. Example for 32-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes				CRC
Target ID	I²C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x00	0x0	0x0	0x1	0x1	0x0	0x0	0x0	0x80	0xCD	0xAB	0x34	0x12	0x45
0x00		0x50				0x00		0x80	0xCD	0xAB	0x34	0x12	0x45

Example for 64-bit Write Operation: Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-8. Example for 64-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes	CRC
Target ID	I²C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0 - DB7	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	[D7-D0] x 8	C7-C0
0x00	0x0	0x0	0x1	0x2	0x0	0x0	0x0	0x80	0x67452301EFCDAB89	0x45
0x00		0x60				0x00		0x80	0x67452301EFCDAB89	0x45

Example for 32-bit Read Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

Table 7-9. Example for 32-bit Read Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Start Byte		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Target ID	I²C Write	R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	Target ID	I²C Read	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	A6-A0	W0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x00	0x0	0x1	0x1	0x1	0x0	0x0	0x0	0x80	0x00	0x1	0xCD	0xAB	0x34	0x12	0x56
0x00		0xD0				0x00		0x80	0x01		0xCD	0xAB	0x34	0x12	0x56

7.6.2.5 Internal Buffers

MCT8329A uses buffers internally to store the data received on I²C. Highest priority is given to collecting data on the I²C Bus. There are 2 buffers (ping-pong) for I²C Rx Data and 2 buffers (ping-pong) for I²C Tx Data.

A write request from external MCU is stored in Rx Buffer 1 and then the parsing block is triggered to work on this data in Rx Buffer 1. While MCT8329A is processing a write packet from Rx Buffer 1, if there is another new read/write request, the entire data from the I²C bus is stored in Rx Buffer 2 and it will be processed after the current request.

MCT8329A can accommodate a maximum of two consecutive read/write requests. If MCT8329A is busy due to high priority interrupts, the data sent will be stored in internal buffers (Rx Buffer 1 and Rx Buffer 2). At this point, if there is a third read/write request, the Target ID will be NACK'd as the buffers are already full.

During read operations, the read request is processed and the read data from the register is stored in the Tx Buffer along with the CRC byte, if enabled. Now if the external MCU initiates an I²C Read (Target ID + R bit), the data from this Tx Buffer is sent over I²C. Since there are two Tx Buffers, register data from 2 MCT8329A reads

can be buffered. Given this scenario, if there is a third read request, the control word will be stored in the Rx Buffer 1, but it will not be processed by MCT8329A as the Tx Buffers are full.

Once a data is read from Tx Buffer, the data is no longer stored in the Tx buffer. The buffer is cleared and it becomes available for the next data to be stored. If the read transaction was interrupted in between and if the MCU had not read all the bytes, external MCU can initiate another I^2C read (only I^2C read, without any control word information) to read all the data bytes from first.

7.6.2.6 CRC Byte Calculation

An 8-bit CCIT polynomial ($x^8 + x^2 + x + 1$) is used for CRC computation.

CRC Calculation in Write Operation: When the external MCU writes to MCT8329A, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCT8329A will compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

CRC Calculation in Read Operation: When the external MCU reads from MCT8329A, if the CRC is enabled, MCT8329A sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCT8329A. Input data for CRC calculation by external MCU to verify the data sent by MCT8329A are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

7.7 EEPROM (Non-Volatile) Register Map

7.7.1 Algorithm_Configuration Registers

Table 7-10 lists the memory-mapped registers for the Algorithm_Configuration registers. All register offset addresses not listed in Table 7-10 should be considered as reserved locations and the register contents should not be modified.

Table 7-10. ALGORITHM_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
80h	ISD_CONFIG	ISD configuration	ISD_CONFIG Register (Offset = 80h) [Reset = 00000000h]
82h	MOTOR_STARTUP1	Motor start-up configuration 1	MOTOR_STARTUP 1 Register (Offset = 82h) [Reset = 00000000h]
84h	MOTOR_STARTUP2	Motor start-up configuration 2	MOTOR_STARTUP 2 Register (Offset = 84h) [Reset = 00000000h]
86h	CLOSED_LOOP1	Closed loop configuration 1	CLOSED_LOOP1 Register (Offset = 86h) [Reset = 00000000h]
88h	CLOSED_LOOP2	Closed loop configuration 2	CLOSED_LOOP2 Register (Offset = 88h) [Reset = 00000000h]
8Ah	CLOSED_LOOP3	Closed loop configuration 3	CLOSED_LOOP3 Register (Offset = 8Ah) [Reset = 000000A0h]
8Ch	CLOSED_LOOP4	Closed loop configuration 4	CLOSED_LOOP4 Register (Offset = 8Ch) [Reset = 00000000h]
8Eh	CONST_SPEED	Constant speed configuration	CONST_SPEED Register (Offset = 8Eh) [Reset = 00000000h]
90h	CONST_PWR	Constant power configuration	CONST_PWR Register (Offset = 90h) [Reset = 00000000h]
96h	150_DEG_TWO_PH_PROFILE	150° Two-ph profile	150_DEG_TWO_PH _PROFILE Register (Offset = 96h) [Reset = 00000000h]
98h	150_DEG_THREE_PH_PROFILE	150° Three-ph profile	150_DEG_THREE_ PH_PROFILE Register (Offset = 98h) [Reset = 00000000h]
9Ah	REF_PROFILES1	Speed Profile Configuration1	REF_PROFILES1 Register (Offset = 9Ah) [Reset = X]
9Ch	REF_PROFILES2	Speed Profile Configuration2	REF_PROFILES2 Register (Offset = 9Ch) [Reset = X]

Table 7-10. ALGORITHM_CONFIGURATION Registers (continued)

Offset	Acronym	Register Name	Section
9Eh	REF_PROFILES3	Speed Profile Configuration3	REF_PROFILES3 Register (Offset = 9Eh) [Reset = X]
A0h	REF_PROFILES4	Speed Profile Configuration4	REF_PROFILES4 Register (Offset = A0h) [Reset = X]
A2h	REF_PROFILES5	Speed Profile Configuration5	REF_PROFILES5 Register (Offset = A2h) [Reset = X]
A4h	REF_PROFILES6	Speed Profile Configuration6	REF_PROFILES6 Register (Offset = A4h) [Reset = X]

Complex bit access types are encoded to fit into small table cells. Table 7-11 shows the codes that are used for access types in this section.

Table 7-11. Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.1.1 ISD_CONFIG Register (Offset = 80h) [Reset = 00000000h]

ISD_CONFIG is shown in Table 7-12.

Return to the Summary Table.

Register to configure initial speed detect settings

Table 7-12. ISD_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	ISD_EN	R/W	0h	ISD enable 0h = Disable 1h = Enable
29	BRAKE_EN	R/W	0h	Brake enable 0h = Disable 1h = Enable
28	HIZ_EN	R/W	0h	Hi-Z enable 0h = Disable 1h = Enable
27	RVS_DR_EN	R/W	0h	Reverse Resynchronization enable 0h = Disable 1h = Enable
26	RESYNC_EN	R/W	0h	Forward Resynchronization enable 0h = Disable 1h = Enable
25	STAT_BRK_EN	R/W	0h	Enable or disable brake during stationary 0h = Disable 1h = Enable
24-22	STAT_DETECT_THR	R/W	0h	Stationary BEMF detect threshold, phase voltage scaled down based on DYN_VOLT_SCALING_EN 0h = 5 mV 1h = 10 mV 2h = 15 mV 3h = 20 mV 4h = 25 mV 5h = 30 mV 6h = 50 mV 7h = 100 mV
21	BRK_MODE	R/W	0h	Brake mode 0h = All three low-side FETs turned ON 1h = All three high-side FETs turned ON
20-17	RESERVED	R/W	0h	Reserved
16-13	BRK_TIME	R/W	0h	Brake time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s

Table 7-12. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	HIZ_TIME	R/W	0h	Hi-Z time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
8-6	STARTUP_BRK_TIME	R/W	0h	Brake time when motor is stationary 0h = 1 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms
5-3	RESYNC_MIN_THRESHOLD	R/W	0h	Minimum phase BEMF below which the motor is coasted instead of resync 0h = MIN_DUTY * DC_BUS_VOLTAGE 1h = 300 mV 2h = 400 mV 3h = 500 mV 4h = 600 mV 5h = 800 mV 6h = 1000 mV 7h = 1250 mV
2-1	MTR_STARTUP	R/W	0h	Motor start-up method 0h = Align 1h = Double Align 2h = IPD 3h = Slow first cycle
0	RESERVED	R/W	0h	Reserved

7.7.1.2 MOTOR_STARTUP1 Register (Offset = 82h) [Reset = 00000000h]

MOTOR_STARTUP1 is shown in Table 7-13.

Return to the Summary Table.

Register to configure motor startup settings1

Table 7-13. MOTOR_STARTUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	ALIGN_RAMP_RATE	R/W	0h	Align voltage ramp rate 0h = 0.1 V/s 1h = 0.2 V/s 2h = 0.5 V/s 3h = 1 V/s 4h = 2.5 V/s 5h = 5 V/s 6h = 7.5 V/s 7h = 10 V/s 8h = 25 V/s 9h = 50 V/s Ah = 75 V/s Bh = 100 V/s Ch = 250 V/s Dh = 500 V/s Eh = 750 V/s Fh = 1000 V/s
26-23	ALIGN_TIME	R/W	0h	Align time 0h = 5 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 75 ms 5h = 100 ms 6h = 200 ms 7h = 400 ms 8h = 600 ms 9h = 800 ms Ah = 1 s Bh = 2 s Ch = 4 s Dh = 6 s Eh = 8 s Fh = 10 s

Table 7-13. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-18	ALIGN_CURR_THR	R/W	0h	Align current threshold. Align current threshold (A) = (ALIGN_CURR_THR - Offset) / (CSA_GAIN * RSENSE). Offset = 0.075V for VREF_SEL = UNI DIRECTIONAL CSA (Values rolls over after 1Bh). Offset = 0V for VREF_SEL = BI-DIRECTIONAL CSA (Values rolls over after 0Fh) 0h = 0.0 V 1h = 0.1 V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9V Ah = 1.0 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V 10h = 1.6 V 11h = 1.7 V 12h = 1.8 V 13h = 1.9 V 14h = 2.0 V 15h = 2.1 V 16h = 2.2 V 17h = 2.3 V 18h = 2.4 V 19h = 2.5 V 1Ah = 2.6 V 1Bh = N/A 1Ch = N/A 1Dh = N/A 1Eh = N/A 1Fh = N/A
17-16	ALIGN_DUTY	R/W	0h	Duty cycle limit during align 0h = 10 % 1h = 25 % 2h = 50 % 3h = 100 %
15-13	IPD_CLK_FREQ	R/W	0h	IPD clock frequency 0h = 50 Hz 1h = 100 Hz 2h = 250 Hz 3h = 500 Hz 4h = 1000 Hz 5h = 2000 Hz 6h = 5000 Hz 7h = 10000 Hz

Table 7-13. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	IPD_CURR_THR	R/W	0h	IPD current threshold. IPD current threshold (A) = (IPD_CURR_THR - Offset) / (CSA_GAIN * RSENSE). Offset = 0.075V for VREF_SEL = UNI DIRECTIONAL CSA (Values rolls over after 1Bh). Offset = 0V for VREF_SEL = BI-DIRECTIONAL CSA (Values rolls over after 0Fh) 0h = 0.0 V 1h = 0.1 V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9V Ah = 1.0 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V 10h = 1.6 V 11h = 1.7 V 12h = 1.8 V 13h = 1.9 V 14h = 2.0 V 15h = 2.1 V 16h = 2.2 V 17h = 2.3 V 18h = 2.4 V 19h = 2.5 V 1Ah = 2.6 V 1Bh = N/A 1Ch = N/A 1Dh = N/A 1Eh = N/A 1Fh = N/A
7-6	IPD_ADV_ANGLE	R/W	0h	IPD advance angle 0h = 0° 1h = 30° 2h = 60° 3h = 90°
5-4	IPD_REPEAT	R/W	0h	Number of times IPD is executed 0h = one 1h = average of 2 times 2h = average of 3 times 3h = average of 4 times
3-0	SLOW_FIRST_CYC_FREQ	R/W	0h	Frequency of first cycle 0h = 0.05 Hz 1h = 0.1 Hz 2h = 0.25 Hz 3h = 0.5 Hz 4h = 1 Hz 5h = 2 Hz 6h = 3 Hz 7h = 5 Hz 8h = 10 Hz 9h = 15 Hz Bh = 25 Hz Ch = 50 Hz Dh = 100 Hz Eh = 150 Hz Fh = 200 Hz

7.7.1.3 MOTOR_STARTUP2 Register (Offset = 84h) [Reset = 00000000h]

MOTOR_STARTUP2 is shown in Table 7-14.

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Register to configure motor startup settings2

Table 7-14. MOTOR_STARTUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	OL_DUTY	R/W	0h	Duty cycle limit during open loop 0h = 10% 1h = 15% 2h = 20% 3h = 25% 4h = 30% 5h = 40% 6h = 50% 7h = 100%
27-23	OL_ILIMIT	R/W	0h	Open Loop current threshold. OL current threshold (A) = (OL_CURR_THR - Offset) / (CSA_GAIN * RSENSE). Offset = 0.075V for VREF_SEL = UNI DIRECTIONAL CSA (Values rolls over after 1Bh). Offset = 0V for VREF_SEL = BI-DIRECTIONAL CSA (Values rolls over after 0Fh) 0h = 0.0 V 1h = 0.1 V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9V Ah = 1.0 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V 10h = 1.6 V 11h = 1.7 V 12h = 1.8 V 13h = 1.9 V 14h = 2.0 V 15h = 2.1 V 16h = 2.2 V 17h = 2.3 V 18h = 2.4 V 19h = 2.5 V 1Ah = 2.6 V 1Bh = N/A 1Ch = N/A 1Dh = N/A 1Eh = N/A 1Fh = N/A

Table 7-14. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-18	OL_ACC_A1	R/W	0h	Open loop acceleration A1 0h = 0.005 Hz/s 1h = 0.01 Hz/s 2h = 0.025 Hz/s 3h = 0.05 Hz/s 4h = 0.1 Hz/s 5h = 0.25 Hz/s 6h = 0.5 Hz/s 7h = 1 Hz/s 8h = 2.5 Hz/s 9h = 5 Hz/s Ah = 7.5 Hz/s Bh = 10 Hz/s Ch = 12.5 Hz/s Dh = 15 Hz/s Eh = 20 Hz/s Fh = 30 Hz/s 10h = 40 Hz/s 11h = 50 Hz/s 12h = 60 Hz/s 13h = 75 Hz/s 14h = 100 Hz/s 15h = 125 Hz/s 16h = 150 Hz/s 17h = 175 Hz/s 18h = 200 Hz/s 19h = 250 Hz/s 1Ah = 300 Hz/s 1Bh = 400 Hz/s 1Ch = 500 Hz/s 1Dh = 750 Hz/s 1Eh = 1000 Hz/s 1Fh = No Limit (32767) Hz/s

Table 7-14. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	OL_ACC_A2	R/W	0h	Open loop acceleration A2 0h = 0.005 Hz/s2 1h = 0.01 Hz/s2 2h = 0.025 Hz/s2 3h = 0.05 Hz/s2 4h = 0.1 Hz/s2 5h = 0.25 Hz/s2 6h = 0.5 Hz/s2 7h = 1 Hz/s2 8h = 2.5 Hz/s2 9h = 5 Hz/s2 Ah = 7.5 Hz/s2 Bh = 10 Hz/s2 Ch = 12.5 Hz/s2 Dh = 15 Hz/s2 Eh = 20 Hz/s2 Fh = 30 Hz/s2 10h = 40 Hz/s2 11h = 50 Hz/s2 12h = 60 Hz/s2 13h = 75 Hz/s2 14h = 100 Hz/s2 15h = 125 Hz/s2 16h = 150 Hz/s2 17h = 175 Hz/s2 18h = 200 Hz/s2 19h = 250 Hz/s2 1Ah = 300 Hz/s2 1Bh = 400 Hz/s2 1Ch = 500 Hz/s2 1Dh = 750 Hz/s2 1Eh = 1000 Hz/s2 1Fh = No Limit (32767) Hz/s2

Table 7-14. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	OPN_CL_HANDOFF_THR	R/W	0h	Open to closed loop handoff threshold 0h = 1 Hz 1h = 4 Hz 2h = 8 Hz 3h = 12 Hz 4h = 16 Hz 5h = 20 Hz 6h = 24 Hz 7h = 28 Hz 8h = 32 Hz 9h = 36 Hz Ah = 40 Hz Bh = 45 Hz Ch = 50 Hz Dh = 55 Hz Eh = 60 Hz Fh = 65 Hz 10h = 70 Hz 11h = 75 Hz 12h = 80 Hz 13h = 85 Hz 14h = 90 Hz 15h = 100 Hz 16h = 150 Hz 17h = 200 Hz 18h = 250 Hz 19h = 300 Hz 1Ah = 350 Hz 1Bh = 400 Hz 1Ch = 450 Hz 1Dh = 500 Hz 1Eh = 550 Hz 1Fh = 600 Hz
7	AUTO_HANDOFF	R/W	0h	Auto handoff enable 0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR) 1h = Enable Auto Handoff
6	FIRST_CYCLE_FREQ_SEL	R/W	0h	First cycle frequency during the Open Loop 0h = Defined by SLOW_FIRST_CYC_FREQ 1h = 0 Hz
5-2	MIN_DUTY	R/W	0h	Min operational duty cycle 0h = 0% 1h = 1.5 % 2h = 2.5 % 3h = 3 % 4h = 4 % 5h = 5 % 6h = 6 % 7h = 7 % 8h = 8 % 9h = 9 % Ah = 10 % Bh = 12 % Ch = 15 % Dh = 17.5 % Eh = 20 % Fh = 25 %
1-0	OL_HANDOFF_CYCLES	R/W	0h	Open loop handoff cycles 0h = 3 1h = 6 2h = 12 3h = 24

7.7.1.4 CLOSED_LOOP1 Register (Offset = 86h) [Reset = 00000000h]

CLOSED_LOOP1 is shown in Table 7-15.

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Register to configure close loop settings1

Table 7-15. CLOSED_LOOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	COMM_CONTROL	R/W	0h	Trapezodial commutation mode 0h = 120° Commutation 1h = Variable commutation between 120° and 150° 2h = N/A 3h = N/A
28-24	CL_ACC	R/W	0h	Closed loop acceleration rate 0h = 0.005 V/s 1h = 0.01 V/s 2h = 0.025 V/s 3h = 0.05 V/s 4h = 0.1 V/s 5h = 0.25 V/s 6h = 0.5 V/s 7h = 1 V/s 8h = 2.5 V/s 9h = 5 V/s Ah = 7.5 V/s Bh = 10 V/s Ch = 12.5 V/s Dh = 15 V/s Eh = 20 V/s Fh = 30 V/s 10h = 40 V/s 11h = 50 V/s 12h = 60 V/s 13h = 75 V/s 14h = 100 V/s 15h = 125 V/s 16h = 150 V/s 17h = 175 V/s 18h = 200 V/s 19h = 250 V/s 1Ah = 300 V/s 1Bh = 400 V/s 1Ch = 500 V/s 1Dh = 750 V/s 1Eh = 1000 V/s 1Fh = 32767 V/s
23	CL_DEC_CONFIG	R/W	0h	Closed loop decel configuration 0h = Close loop deceleration defined by CL_DEC 1h = Close loop deceleration defined by CL_ACC

Table 7-15. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-18	CL_DEC	R/W	0h	Closed loop deceleration rate 0h = 0.005 V/s 1h = 0.01 V/s 2h = 0.025 V/s 3h = 0.05 V/s 4h = 0.1 V/s 5h = 0.25 V/s 6h = 0.5 V/s 7h = 1 V/s 8h = 2.5 V/s 9h = 5 V/s Ah = 7.5 V/s Bh = 10 V/s Ch = 12.5 V/s Dh = 15 V/s Eh = 20 V/s Fh = 30 V/s 10h = 40 V/s 11h = 50 V/s 12h = 60 V/s 13h = 75 V/s 14h = 100 V/s 15h = 125 V/s 16h = 150 V/s 17h = 175 V/s 18h = 200 V/s 19h = 250 V/s 1Ah = 300 V/s 1Bh = 400 V/s 1Ch = 500 V/s 1Dh = 750 V/s 1Eh = 1000 V/s 1Fh = 32767 V/s

Table 7-15. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	PWM_FREQ_OUT	R/W	0h	Output PWM switching frequency 0h = 5 kHz 1h = 6 kHz 2h = 7 kHz 3h = 8 kHz 4h = 9 kHz 5h = 10 kHz 6h = 11 kHz 7h = 12 kHz 8h = 13 kHz 9h = 14 kHz Ah = 15 kHz Bh = 16 kHz Ch = 17 kHz Dh = 18 kHz Eh = 19 kHz Fh = 20 kHz 10h = 25 kHz 11h = 30 kHz 12h = 35 kHz 13h = 40 kHz 14h = 45 kHz 15h = 50 kHz 16h = 55 kHz 17h = 60 kHz 18h = 65 kHz 19h = 70 kHz 1Ah = 75 kHz 1Bh = 80 kHz 1Ch = 85 kHz 1Dh = 90 kHz 1Eh = 95 kHz 1Fh = 100 kHz
12-11	PWM_MODUL	R/W	0h	PWM modulation. 0h = High-Side Modulation 1h = Low-Side Modulation 2h = Mixed Modulation 3h = N/A
10	PWM_MODE	R/W	0h	PWM mode 0h = Single Ended Mode 1h = Complementary Mode
9	LD_ANGLE_POLARITY	R/W	0h	Polarity of applied lead angle 0h = Lag 1h = Lead
8-1	LD_ANGLE	R/W	0h	Lead Angle {Lead Angle (deg) = LD_ANGLE * 0.12}
0	RESERVED	R/W	0h	Reserved

7.7.1.5 CLOSED_LOOP2 Register (Offset = 88h) [Reset = 00000000h]

CLOSED_LOOP2 is shown in Table 7-16.

Return to the Summary Table.

Register to configure close loop settings2

Table 7-16. CLOSED_LOOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	FG_SEL	R/W	0h	FG mode select 0h = Output FG in open loop and closed loop 1h = Output FG in only closed loop 2h = Output FG in open loop for the first try. 3h = N/A
28-25	FG_DIV_FACTOR	R/W	0h	FG division factor 0h = Divide by 3 (2-pole motor mechanical speed*3) 1h = Divide by 1 (2-pole motor mechanical speed) 2h = Divide by 2 (4-pole motor mechanical speed) 3h = Divide by 3 (6-pole motor mechanical speed) 4h = Divide by 4 (8-pole motor mechanical speed) 5h = Divide by 5 (10-pole motor mechanical speed) 6h = Divide by 6 (12-pole motor mechanical speed) 7h = Divide by 7 (14-pole motor mechanical speed) 8h = Divide by 8 (16-pole motor mechanical speed) 9h = Divide by 9 (18-pole motor mechanical speed) Ah = Divide by 10 (20-pole motor mechanical speed) Bh = Divide by 11 (22-pole motor mechanical speed) Ch = Divide by 12 (24-pole motor mechanical speed) Dh = Divide by 13 (26-pole motor mechanical speed) Eh = Divide by 14 (28-pole motor mechanical speed) Fh = Divide by 15 (30-pole motor mechanical speed)
24	DEAD_TIME_COMP	R/W	0h	Dead Time Correction applied to calculate power in Power Limit and Closed Loop Power Control modes 0h = Disable 1h = Enable
23-21	FG_BEMF_THR	R/W	0h	FG output BEMF threshold, phase voltage scaled down based on DYN_VOLT_SCALING_EN 0h = +/- 1mV 1h = +/- 2mV 2h = +/- 5mV 3h = +/- 10mV 4h = +/- 20mV 5h = +/- 30mV 6h = N/A 7h = N/A
20-18	MTR_STOP	R/W	0h	Motor stop method 0h = Hi-z 1h = Recirculation 2h = Low-side braking 3h = High-side braking 4h = Active spin down 5h = N/A 6h = N/A 7h = N/A

Table 7-16. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-14	MTR_STOP_BRK_TIME	R/W	0h	Brake time during motor stop when configured as Brake Mode 0h = 1 ms 1h = 2 ms 2h = 5 ms 3h = 10 ms 4h = 15 ms 5h = 25 ms 6h = 50 ms 7h = 75 ms 8h = 100 ms 9h = 250 ms Ah = 500 ms Bh = 1000 ms Ch = 2500 ms Dh = 5000 ms Eh = 10000 ms Fh = 15000 ms
13-11	ACT_SPIN_BRK_THR	R/W	0h	Duty cycle threshold for motor stop using active spin down, low- and high-side braking 0h = Immediate 1h = 50 % 2h = 25 % 3h = 15 % 4h = 10 % 5h = 7.5 % 6h = 5 % 7h = 2.5 %
10-8	BRAKE_DUTY_THRESHOLD	R/W	0h	Duty cycle threshold for BRAKE pin based low-side braking 0h = Immediate 1h = 50 % 2h = 25 % 3h = 15 % 4h = 10 % 5h = 7.5 % 6h = 5 % 7h = 2.5 %
7	AVS_EN	R/W	0h	AVS enable 0h = Disable 1h = Enable

Table 7-16. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-2	CBC_ILIMIT	R/W	0h	Motor Run CBC current limit threshold. Motor Run current limit threshold (A) = (CBC_ILIMIT - Offset) / (CSA_GAIN * RSENSE). Offset = 0.075V for VREF_SEL = UNI DIRECTIONAL CSA (Values rolls over after 1Bh). Offset = 0V for VREF_SEL = BI-DIRECTIONAL CSA (Values rolls over after 0Fh). 0h = 0.0 V 1h = 0.1 V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9V Ah = 1.0 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V 11h = 1.7 V 12h = 1.8 V 13h = 1.9 V 14h = 2.0 V 15h = 2.1 V 16h = 2.2 V 17h = 2.3 V 18h = 2.4 V 19h = 2.5 V 1Ah = 2.6 V 1Bh = N/A 1Ch = N/A 1Dh = N/A 1Eh = N/A 1Fh = N/A
1	OL_ILIMIT_CONFIG	R/W	0h	Open loop current limit configuration 0h = Open loop current limit defined by OL_ILIMIT 1h = Open loop current limit defined by CBC_ILIMIT
0	INTEG_ZC_METHOD	R/W	0h	Commutation method select 0h = ZC based 1h = Integration based

7.7.1.6 CLOSED_LOOP3 Register (Offset = 8Ah) [Reset = 000000A0h]

CLOSED_LOOP3 is shown in Table 7-17.

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Register to configure close loop settings3

Table 7-17. CLOSED_LOOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	INTEG_CYCL_THR_LOW	R/W	0h	Number of BEMF samples per 30° below which commutation method switches from integration to ZC 0h = 3 1h = 4 2h = 6 3h = 8
28-27	INTEG_CYCL_THR_HIGH	R/W	0h	Number of BEMF samples per 30° above which commutation method switches from ZC to integration 0h = 4 1h = 6 2h = 8 3h = 10
26-25	INTEG_DUTY_THR_LOW	R/W	0h	Duty cycle below which commutation method switches from integration to ZC 0h = 12 % 1h = 15 % 2h = 18 % 3h = 20 %
24-23	INTEG_DUTY_THR_HIGH	R/W	0h	Duty cycle above which commutation method switches from ZC to integration 0h = 12 % 1h = 15 % 2h = 18 % 3h = 20 %

Table 7-17. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-17	BEMF_THRESHOLD2	R/W	0h	BEMF threshold for integration based commutation during falling floating phase voltage 0h = 0 1h = 25 2h = 50 3h = 75 4h = 100 5h = 125 6h = 150 7h = 175 8h = 200 9h = 225 Ah = 250 Bh = 275 Ch = 300 Dh = 325 Eh = 350 Fh = 375 10h = 400 11h = 425 12h = 450 13h = 475 14h = 500 15h = 525 16h = 550 17h = 575 18h = 600 19h = 625 1Ah = 650 1Bh = 675 1Ch = 700 1Dh = 725 1Eh = 750 1Fh = 775 20h = 800 21h = 850 22h = 900 23h = 950 24h = 1000 25h = 1050 26h = 1100 27h = 1150 28h = 1200 29h = 1250 2Ah = 1300 2Bh = 1350 2Ch = 1400 2Dh = 1450 2Eh = 1500 2Fh = 1550 30h = 1600 31h = 1700 32h = 1800 33h = 1900 34h = 2000 35h = 2100 36h = 2200 37h = 2300 38h = 2400 39h = 2600 3Ah = 2800 3Bh = 3000 3Ch = 3200 3Dh = 3400 3Eh = 3600 3Fh = 3800

Table 7-17. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-11	BEMF_THRESHOLD1	R/W	0h	BEMF threshold for integration based commutation during rising floating phase voltage 0h = 0 1h = 25 2h = 50 3h = 75 4h = 100 5h = 125 6h = 150 7h = 175 8h = 200 9h = 225 Ah = 250 Bh = 275 Ch = 300 Dh = 325 Eh = 350 Fh = 375 10h = 400 11h = 425 12h = 450 13h = 475 14h = 500 15h = 525 16h = 550 17h = 575 18h = 600 19h = 625 1Ah = 650 1Bh = 675 1Ch = 700 1Dh = 725 1Eh = 750 1Fh = 775 20h = 800 21h = 850 22h = 900 23h = 950 24h = 1000 25h = 1050 26h = 1100 27h = 1150 28h = 1200 29h = 1250 2Ah = 1300 2Bh = 1350 2Ch = 1400 2Dh = 1450 2Eh = 1500 2Fh = 1550 30h = 1600 31h = 1700 32h = 1800 33h = 1900 34h = 2000 35h = 2100 36h = 2200 37h = 2300 38h = 2400 39h = 2600 3Ah = 2800 3Bh = 3000 3Ch = 3200 3Dh = 3400 3Eh = 3600 3Fh = 3800

Table 7-17. CLOSED_LOOP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	DYN_DGS_FILT_COUNT	R/W	0h	Number of samples needed for dynamic degauss check 0h = 3 1h = 6 2h = 9 3h = 12 4h = 15 5h = 20 6h = 30 7h = 40
7-6	DYN_DGS_UPPER_LIM	R/W	2h	Dynamic degauss voltage upper bound 0h = (VM - 0.09) V 1h = (VM - 0.12) V 2h = (VM - 0.15) V 3h = (VM - 0.18) V
5-4	DYN_DGS_LOWER_LIM	R/W	2h	Dynamic degauss voltage lower bound 0h = 0.03 V 1h = 0.06 V 2h = 0.09 V 3h = 0.12 V
3-1	DEGAUSS_MAX_WIN	R/W	0h	Maximum degauss window 0h = 22.5° 1h = 10° 2h = 15° 3h = 18° 4h = 30° 5h = 37.5° 6h = 45° 7h = 60°
0	DYN_DEGAUSS_EN	R/W	0h	Dynamic degauss detection 0h = Disable 1h = Enable

7.7.1.7 CLOSED_LOOP4 Register (Offset = 8Ch) [Reset = 00000000h]

CLOSED_LOOP4 is shown in Table 7-18.

Return to the Summary Table.

Register to configure close loop settings4

Table 7-18. CLOSED_LOOP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	DYN_VOLT_SCALING_EN	R/W	0h	Dynamic Voltage Scaling Enable 0h = Disable 1h = Enable
29	HIGH_RES_SAMP	R/W	0h	Bandwidth of control loop. 0h = High bandwidth for control loop. 1h = Low bandwidth for control loop.
28	AVS_LIMIT_HYST	R/W	0h	AVS current hysteresis. (AVS positive current limit (A) = ((AVS_LIMIT_HYST + AVS_NEG_CURR_LIMIT) * 3 /4095) / (CSA_GAIN * RSENSE)) 0h = 20 1h = 10
27-25	AVS_NEG_CURR_LIMIT	R/W	0h	AVS negative current limit. (AVS negative current limit (A) = (AVS_NEG_CURRENT_LIMIT * 3 /4095) / (CSA_GAIN * RSENSE)) 0h = 0 1h = -60 2h = -40 3h = -30 4h = -20 5h = -10 6h = 15 7h = 30
24	RESERVED	R/W	0h	Reserved
23-22	RESERVED	R/W	0h	Reserved
21-20	FAST_DEC_DEG_TIME	R/W	0h	Fast Decel Deglitch Time 0h = 2uS 1h = 4uS 2h = 8uS 3h = 14uS
19	WCOMP_BLANK_EN	R/W	0h	Enable WCOMP blanking during fast deceleration 0h = Disable 1h = Enable
18-16	FAST_DEC_DUTY_WIN	R/W	0h	Fast deceleration duty window 0h = 0 % 1h = 2.5 % 2h = 5 % 3h = 7.5 % 4h = 10 % 5h = 15 % 6h = 20 % 7h = 25 %
15-13	FAST_DEC_DUTY_THR	R/W	0h	Fast deceleration duty threshold 0h = 100 % 1h = 95 % 2h = 90 % 3h = 85 % 4h = 80 % 5h = 75 % 6h = 70% 7h = 65 %

Table 7-18. CLOSED_LOOP4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	DYN_BRK_CURR_LOW_LIM	R/W	0h	Fast deceleration dynamic current limit lower threshold. Deceleration current lower threshold (A) = DYN_BRK_CURR_LOW_LIM / (CSA_GAIN * RSENSE). This setting is applicable for VREF_SEL = BI-DIRECTIONAL CSA only. 0h = N/A 1h = 0.1V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
8	DYNAMIC_BRK_CURR	R/W	0h	Enable dynamic decrease in current limit during fast deceleration 0h = Disable 1h = Enable
7	FAST_DECEL_EN	R/W	0h	Fast deceleration enable 0h = Disable 1h = Enable
6-3	FAST_DECEL_CURR_LIM	R/W	0h	Deceleration current threshold. Fast Deceleration current limit upper threshold (A) = FAST_DECEL_CURR_LIM / (CSA_GAIN * RSENSE). This setting is applicable for VREF_SEL = BI-DIRECTIONAL CSA only. 0h = N/A 1h = 0.1V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9 V Ah = 1 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V
2-0	FAST_BRK_DELTA	R/W	0h	Fast deceleration exit speed delta 0h = 0.5 % 1h = 1 % 2h = 1.5 % 3h = 2 % 4h = 2.5 % 5h = 3 % 6h = 4 % 7h = 5 %

7.7.1.8 CONST_SPEED Register (Offset = 8Eh) [Reset = 00000000h]

CONST_SPEED is shown in Table 7-19.

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Register to configure Constant speed mode settings

Table 7-19. CONST_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	RESERVED	R/W	0h	Reserved
29-20	SPD_POWER_KP	R/W	0h	Speed/ Power loop Kp (Kp = SPD_LOOP_KP / 10000)
19-8	SPD_POWER_KI	R/W	0h	Speed/ Power loop Ki (Ki = SPD_LOOP_KI / 1000000)
7-5	SPD_POWER_V_MAX	R/W	0h	Upper saturation limit for speed/ power loop 0h = 100 % 1h = 95 % 2h = 90 % 3h = 85 % 4h = 80 % 5h = 75 % 6h = 70% 7h = 65 %
4-2	SPD_POWER_V_MIN	R/W	0h	Lower saturation limit for speed/power loop 0h = 0 % 1h = 2.5 % 2h = 5 % 3h = 7.5 % 4h = 10 % 5h = 15 % 6h = 20 % 7h = 25 %
1-0	CLOSED_LOOP_MODE	R/W	0h	Closed loop mode 0h = Disabled 1h = Speed Loop 2h = Power Loop 3h = Reserved

7.7.1.9 CONST_PWR Register (Offset = 90h) [Reset = 00000000h]

CONST_PWR is shown in Table 7-20.

Return to the Summary Table.

Register to configure Constant power mode settings

Table 7-20. CONST_PWR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-15	MAX_SPEED	R/W	0h	Maximum Speed. (Maximum Speed (Hz) = MAX_SPEED / 16)
14-4	MAX_POWER	R/W	0h	Maximum power. Maximum power (W) = MAX_POWER*10 mOhm / RSENSE : {For MAX_POWER between 0 to 1023}. Maximum power (W) = (2*MAX_POWER - 1024)*10 mOhm / RSENSE : {For MAX_POWER between 1024 to 2047}.
3-2	CONST_POWER_LIMIT_HYST	R/W	0h	Hysteresis for input power regulation (% of MAX_POWER). Power Loop regulates power to reference only if the new reference is more than CONST_POWER_LIMIT_HYST 0h = 5 % 1h = 7.5 % 2h = 10 % 3h = 12.5 %
1-0	CONST_POWER_MODE	R/W	0h	Input power regulation mode 0h = Voltage Control mode 1h = Closed Loop Power Control 2h = Power Limit Control 3h = Reserved

7.7.1.10 150_DEG_TWO_PH_PROFILE Register (Offset = 96h) [Reset = 00000000h]

150_DEG_TWO_PH_PROFILE is shown in Table 7-21.

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Register to configure 150 degree modulation TWO phase duty

Table 7-21. 150_DEG_TWO_PH_PROFILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	TWOPH_STEP0	R/W	0h	150° modulation , Two ph - step duty - 0 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
27-25	TWOPH_STEP1	R/W	0h	150° modulation , Two ph - step duty - 1 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
24-22	TWOPH_STEP2	R/W	0h	150° modulation, Two ph - step duty - 2 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
21-19	TWOPH_STEP3	R/W	0h	150° modulation, Two ph - step duty - 3 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
18-16	TWOPH_STEP4	R/W	0h	150° modulation, Two ph - step duty - 4 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
15-13	TWOPH_STEP5	R/W	0h	150° modulation, Two ph - step duty - 5 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %

Table 7-21. 150_DEG_TWO_PH_PROFILE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	TWOPH_STEP6	R/W	0h	150° modulation, Two ph - step duty - 6 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
9-7	TWOPH_STEP7	R/W	0h	150° modulation, Two ph - step duty - 7 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
6-0	RESERVED	R/W	0h	reserved bits for algo parameter update

7.7.1.11 150_DEG_THREE_PH_PROFILE Register (Offset = 98h) [Reset = 00000000h]

150_DEG_THREE_PH_PROFILE is shown in Table 7-22.

Return to the Summary Table.

Register to configure 150 degree modulation Three phase duty

Table 7-22. 150_DEG_THREE_PH_PROFILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	THREEPH_STEP0	R/W	0h	150° modulation, Three ph - step duty - 0 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
27-25	THREEPH_STEP1	R/W	0h	150° modulation, Three ph - step duty - 1 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
24-22	THREEPH_STEP2	R/W	0h	150° modulation, Three ph - step duty - 2 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
21-19	THREEPH_STEP3	R/W	0h	150° modulation, Three ph - step duty - 3 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
18-16	THREEPH_STEP4	R/W	0h	150° modulation, Three ph - step duty - 4 0h = 0.0 % 1h = 0.5 % 2h = 0.75 % 3h = 0.8375 % 4h = 0.875 % 5h = 0.9375 % 6h = 0.975 % 7h = 0.99 %
15-13	THREEPH_STEP5	R/W	0h	150° modulation, Three ph - step duty - 5 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %

Table 7-22. 150_DEG_THREE_PH_PROFILE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	THREEPH_STEP6	R/W	0h	150° modulation, Three ph - step duty - 6 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
9-7	THREEPH_STEP7	R/W	0h	150° modulation, Three ph - step duty - 7 0h = 0% 1h = 50 % 2h = 75 % 3h = 83.75 % 4h = 87.5 % 5h = 93.75 % 6h = 97.5 % 7h = 99 %
6-5	LEAD_ANGLE_150DEG_ADV	R/W	0h	Angle advance for 150° modulation 0h = 0° 1h = 5° 2h = 10° 3h = 15°
4-0	RESERVED	R/W	0h	Reserved

7.7.1.12 REF_PROFILES1 Register (Offset = 9Ah) [Reset = X]

REF_PROFILES1 is shown in Table 7-23.

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Register to configure speed profile1

Table 7-23. REF_PROFILES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	REF_PROFILE_CONFIG	R/W	0h	Reference Profile Configuration 0h = Duty Control Mode 1h = Linear Mode 2h = Staircase Mode 3h = Forward Reverse Mode
28-21	DUTY_ON1	R/W	X	Duty_ON1 Configuration. Turn On Duty Cycle (%) = {(DUTY_ON1/255)*100}.
20-13	DUTY_OFF1	R/W	X	Duty_OFF1 Configuration. Turn Off Duty Cycle (%) = {(DUTY_OFF1/255)*100}.
12-5	DUTY_CLAMP1	R/W	X	Duty_CLAMP1 Configuration. Duty Cycle for clamping speed (%) = {(DUTY_CLAMP1/255)*100}.
4-0	DUTY_A	R/W	X	5 MSB bits for Duty Cycle A. Duty Cycle A (%) = {(DUTY_A/255)*100}.

7.7.1.13 REF_PROFILES2 Register (Offset = 9Ch) [Reset = X]

REF_PROFILES2 is shown in Table 7-24.

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Register to configure speed profile2

Table 7-24. REF_PROFILES2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	DUTY_A	R/W	X	3 LSB bits for Duty Cycle A. Duty Cycle A (%) = {(DUTY_A/255)*100}.
27-20	DUTY_B	R/W	X	Duty_B Configuration. Duty Cycle B (%) = {(DUTY_B/255)*100}.
19-12	DUTY_C	R/W	X	Duty_C Configuration. Duty Cycle C (%) = {(DUTY_C/255)*100}.
11-4	DUTY_D	R/W	X	Duty_D Configuration. Duty Cycle D (%) = {(DUTY_D/255)*100}.
3-0	DUTY_E	R/W	0h	4 MSB bits for Duty Cycle E. Duty Cycle E (%) = {(DUTY_E/255)*100}.

7.7.1.14 REF_PROFILES3 Register (Offset = 9Eh) [Reset = X]

REF_PROFILES3 is shown in Table 7-25.

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Register to configure speed profile3

Table 7-25. REF_PROFILES3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	DUTY_E	R/W	X	4 LSB bits for Duty Cycle E. Duty Cycle E (%) = {(DUTY_E/255)*100}.
26-19	DUTY_ON2	R/W	X	Duty_ON2 Configuration. Turn On Duty Cycle (%) = {(DUTY_ON2/255)*100}.
18-11	DUTY_OFF2	R/W	X	Duty_OFF2 Configuration. Turn Off Duty Cycle (%) = {(DUTY_OFF2/255)*100}.
10-3	DUTY_CLAMP2	R/W	X	Duty_CLAMP2 Configuration. Duty Cycle for clamping speed (%) = {(DUTY_CLAMP1/255)*100}.
2-1	STEP_HYST_BAND		0h	Hysteresis band used for Step changes 0h = 0% 1h = 2% 2h = 4% 3h = 6%
0	RESERVED	R/W	0h	Reserved

7.7.1.15 REF_PROFILES4 Register (Offset = A0h) [Reset = X]

REF_PROFILES4 is shown in Table 7-26.

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Register to configure speed profile4

Table 7-26. REF_PROFILES4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	REF_OFF1	R/W	X	Turn off Ref Configuration. Turn off Reference % = {(REF_OFF1/255)*100}.
22-15	REF_CLAMP1	R/W	X	Ref Clamp 1 Configuration. Clamp REF % = {(REF_CLAMP1/255)*100}.
14-7	REF_A	R/W	X	Ref A configuration. Ref A % = {(REF_A/255)*100}.
6-0	REF_B	R/W	X	7 MSB of REF_B configuration. REF B% = {(REF_B/255)*100}.

7.7.1.16 REF_PROFILES5 Register (Offset = A2h) [Reset = X]

REF_PROFILES5 is shown in Table 7-27.

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Register to configure speed profile5

Table 7-27. REF_PROFILES5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	REF_B	R/W	X	1 LSB of REF_B configuration. REF B% = {(REF_B/255)*100}.
29-22	REF_C	R/W	X	REF C configuration. REF C % = {(REF_A/255)*100}.
21-14	REF_D	R/W	X	REF D configuration. REF D % = {(REF_D/255)*100}.
13-6	REF_E	R/W	X	REF E Configuration. REF E% = {(REF_E/255)*100}.
5-0	RESERVED	R/W	0h	Reserved

7.7.1.17 REF_PROFILES6 Register (Offset = A4h) [Reset = X]

REF_PROFILES6 is shown in Table 7-28.

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Register to configure speed profile6

Table 7-28. REF_PROFILES6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	REF_OFF2	R/W	X	Turn off REF Configuration. Turn off REF % = {(REF_OFF2/255)*100}.
22-15	REF_CLAMP2	R/W	X	Clamp REF Configuration. Clamp REF % = {(REF_CLAMP2/255)*100}.
14-0	RESERVED	R/W	X	Reserved

7.7.2 Fault_Configuration Registers

Table 7-29 lists the memory-mapped registers for the Fault_Configuration registers. All register offset addresses not listed in Table 7-29 should be considered as reserved locations and the register contents should not be modified.

Table 7-29. FAULT_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
92h	FAULT_CONFIG1	Fault configuration 1	FAULT_CONFIG1 Register (Offset = 92h) [Reset = 00000000h]
94h	FAULT_CONFIG2	Fault configuration 2	FAULT_CONFIG2 Register (Offset = 94h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. Table 7-30 shows the codes that are used for access types in this section.

Table 7-30. Fault_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.2.1 FAULT_CONFIG1 Register (Offset = 92h) [Reset = 00000000h]

FAULT_CONFIG1 is shown in Table 7-31.

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Register to configure fault settings1

Table 7-31. FAULT_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	NO_MTR_DEG_TIME	R/W	0h	No motor detect deglitch time 0h = 1 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms
27-24	CBC_ILIMIT_MODE	R/W	0h	Cycle by cycle current limit. This mode is applied for CBC_ILIMIT, OL_ILIMT, ALIGN_ILIMIT 0h = Automatic recovery next PWM cycle; nFAULT active; driver is in recirculation mode 1h = Automatic recovery next PWM cycle; nFAULT inactive; driver is in recirculation mode 2h = Automatic recovery if current < ILIMIT; nFAULT active; driver is in recirculation mode (Only available with high-side modulation) 3h = Automatic recovery if current < ILIMIT; nFAULT inactive; driver is in recirculation mode (Only available with high-side modulation) 4h = Automatic recovery after CBC_RETRY_PWM_CYC; nFAULT active; driver is in recirculation mode 5h = Automatic recovery after CBC_RETRY_PWM_CYC; nFAULT inactive; driver is in recirculation mode 6h = Current > ILIMIT is report only but no action is taken 7h = Cycle by Cycle limit is disabled 8h = Cycle by Cycle limit is disabled 9h = Cycle by Cycle limit is disabled Ah = Cycle by Cycle limit is disabled Bh = Cycle by Cycle limit is disabled Ch = Cycle by Cycle limit is disabled Dh = Cycle by Cycle limit is disabled Eh = Cycle by Cycle limit is disabled Fh = Cycle by Cycle limit is disabled

Table 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-19	LOCK_ILIMIT	R/W	0h	Lock current threshold (Lock current threshold (A) = Lock_CURR_THR / CSA_GAIN*RSHUNT) 0h = 0.0 V 1h = 0.1 V 2h = 0.2 V 3h = 0.3 V 4h = 0.4 V 5h = 0.5 V 6h = 0.6 V 7h = 0.7 V 8h = 0.8 V 9h = 0.9V Ah = 1.0 V Bh = 1.1 V Ch = 1.2 V Dh = 1.3 V Eh = 1.4 V Fh = 1.5 V 11h = 1.7 V 12h = 1.8 V 13h = 1.9 V 14h = 2.0 V 15h = 2.1 V 16h = 2.2 V 17h = 2.3 V 18h = 2.4 V 19h = 2.5 V 1Ah = 2.6 V 1Bh = 2.7 V 1Ch = N/A 1Dh = N/A 1Eh = N/A 1Fh = N/A
18-15	LOCK_ILIMIT_MODE	R/W	0h	Lock detection current limit mode 0h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode 2h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 3h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 4h = Automatic recovery after tLCK_RETRY; Gate driver is tristated 5h = Automatic recovery after tLCK_RETRY; Gate driver is in recirculation mode 6h = Automatic recovery after tLCK_RETRY; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 7h = Automatic recovery after tLCK_RETRY; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 8h = Ilimit lock detection is in report only but no action is taken 9h = Ilimit lock detection is disabled Ah = Ilimit lock detection is disabled Bh = Ilimit lock detection is disabled Ch = Ilimit lock detection is disabled Dh = Ilimit lock detection is disabled Eh = Ilimit lock detection is disabled Fh = Ilimit lock detection is disabled

Table 7-31. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-11	LOCK_ILIMIT_DEG	R/W	0h	Lock detection current limit deglitch time 0h = 1 ms 1h = 2 ms 2h = 5 ms 3h = 10 ms 4h = 25 ms 5h = 50 ms 6h = 75 ms 7h = 100 ms 8h = 250 ms 9h = 500 ms Ah = 1 s Bh = 2.5 s Ch = 5 s Dh = 10 s Eh = 25 s Fh = 50 s
10-8	CBC_RETRY_PWM_CYC	R/W	0h	Number of PWM cycles for CBC current limit to retry 0h = 0 1h = 1 2h = 2 3h = 3 4h = 4 5h = 5 6h = 6 7h = 7
7	RESERVED	R/W	0h	Reserved
6-3	MTR_LCK_MODE	R/W	0h	Motor lock mode 0h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in recirculation mode 2h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 3h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 4h = Automatic recovery after tLCK_RETRY; Gate driver is tristated 5h = Automatic recovery after tLCK_RETRY; Gate driver is in recirculation mode 6h = Automatic recovery after tLCK_RETRY; Gate driver is in high-side brake mode (All high-side FETs are turned ON) 7h = Automatic recovery after tLCK_RETRY; Gate driver is in low-side brake mode (All low-side FETs are turned ON) 8h = Motor lock detection is in report only but no action is taken 9h = Motor lock detection is disabled Bh = Motor lock detection is disabled Ch = Motor lock detection is disabled Dh = Motor lock detection is disabled Eh = Motor lock detection is disabled Fh = Motor lock detection is disabled
2-0	LCK_RETRY	R/W	0h	Lock retry time 0h = 100 ms 1h = 500 ms 2h = 1000 ms 3h = 2000 ms 4h = 3000 ms 5h = 5000 ms 6h = 7500 ms 7h = 10000 ms

7.7.2.2 FAULT_CONFIG2 Register (Offset = 94h) [Reset = 00000000h]

FAULT_CONFIG2 is shown in Table 7-32.

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Register to configure fault settings2

Table 7-32. FAULT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	ABN_SPD_EN	R/W	0h	Abnormal SpeedEnable 0h = Disable 1h = Enable
29	LOSS_OF_SYNC_EN	R/W	0h	Loss of Sync Enable 0h = Disable 1h = Enable
28	NO_MOTOR_EN	R/W	0h	No Motor Enable 0h = Disable 1h = Enable
27-24	LOCK_ABN_SPEED	R/W	0h	Abnormal speed lock threshold 0h = 250 Hz 1h = 500 Hz 2h = 750 Hz 3h = 1000 Hz 4h = 1250 Hz 5h = 1500 Hz 6h = 1750 Hz 7h = 2000 Hz 8h = 2250 Hz 9h = 2500 Hz Ah = 2750 Hz Bh = 3000 Hz Ch = 3250 Hz Dh = 3500 Hz Eh = 3750 Hz Fh = 4000 Hz
23-21	LOSS_SYNC_TIMES	R/W	0h	Number of times sync lost for loss of sync lock fault 0h = Trigger after losing sync 2 times 1h = Trigger after losing sync 3 times 2h = Trigger after losing sync 4 times 3h = Trigger after losing sync 5 times 4h = Trigger after losing sync 6 times 5h = Trigger after losing sync 7 times 6h = Trigger after losing sync 8 times 7h = Trigger after losing sync 9 times
20-18	NO_MTR_THR	R/W	0h	Lock current threshold. Lock current threshold (A) = Lock_CURR_THR / (CSA_GAIN * RSENSE) 0h = 0.005 V 1h = 0.0075 V 2h = 0.010 V 3h = 0.0125 V 4h = 0.020 V 5h = 0.025 V 6h = 0.030 V 7h = 0.04 V
17	MAX_VM_MODE	R/W	0h	0h = Latch on Overvoltage 1h = Automatic clear if voltage in bounds

Table 7-32. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-14	MAX_VM_MOTOR	R/W	0h	Maximum voltage for running motor 0h = No Limit 1h = 10.0 V 2h = 15.0 V 3h = 22.0 V 4h = 32.0 V 5h = 40.0 V 6h = 50.0 V 7h = 60.0 V
13	MIN_VM_MODE	R/W	0h	0h = Latch on Undervoltage 1h = Automatic clear if voltage in bounds
12-10	MIN_VM_MOTOR	R/W	0h	Minimum voltage for running motor 0h = No Limit 1h = 5.0 V 2h = 6.0 V 3h = 7.0 V 4h = 8.0 V 5h = 10.0 V 6h = 12.0 V 7h = 15.0 V
9-7	AUTO_RETRY_TIMES	R/W	0h	Number of automatic retry attempts for LOCK Faults 0h = No Limit 1h = 2 2h = 3 3h = 5 4h = 7 5h = 10 6h = 15 7h = 20
6-4	LOCK_MIN_SPEED	R/W	0h	Speed below which lock fault is triggered 0h = 0.5 Hz 1h = 1 Hz 2h = 2 Hz 3h = 3 Hz 4h = 5 Hz 5h = 10 Hz 6h = 15 Hz 7h = 25 Hz
3-2	ABN_LOCK_SPD_RATIO	R/W	0h	Ratio of electrical speed between two consecutive cycles above which abnormal speed lock fault is triggered 0h = 2 1h = 4 2h = 6 3h = 8
1-0	ZERO_DUTY_THR	R/W	0h	Duty cycle below which target speed is zero 0h = 0% 1h = 1% 2h = 2.0% 3h = 2.5%

7.7.3 Hardware_Configuration Registers

Table 7-33 lists the memory-mapped registers for the Hardware_Configuration registers. All register offset addresses not listed in Table 7-33 should be considered as reserved locations and the register contents should not be modified.

Table 7-33. HARDWARE_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A6h	PIN_CONFIG1	Hardware pin configuration	PIN_CONFIG1 Register (Offset = A6h) [Reset = 00000000h]
A8h	PIN_CONFIG2	Hardware pin configuration	PIN_CONFIG2 Register (Offset = A8h) [Reset = 06000000h]
AAh	DEVICE_CONFIG	Peripheral configuration	DEVICE_CONFIG Register (Offset = AAh) [Reset = 00002000h]

Complex bit access types are encoded to fit into small table cells. Table 7-34 shows the codes that are used for access types in this section.

Table 7-34. Hardware_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.3.1 PIN_CONFIG1 Register (Offset = A6h) [Reset = 00000000h]

PIN_CONFIG1 is shown in Table 7-35.

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Register to configure hardware pins

Table 7-35. PIN_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-19	DACOUT_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored.
18-7	RESERVED	R/W	0h	RSVD
6-5	BRAKE_INPUT	R/W	0h	Brake input configuration 0h = Hardware pin based BRAKE 1h = BRAKE always ON 2h = BRAKE always OFF 3h = N/A
4-3	DIR_INPUT	R/W	0h	Direction input configuration 0h = Hardware Pin DIR 1h = Overwrite Hardware pin with clockwise rotation OUTA-OUTB-OUTC 2h = Overwrite Hardware pin with counter clockwise rotation OUTA-OUTC-OUTB 3h = N/A
2-1	SPD_CTRL_MODE	R/W	0h	Speed input configuration 0h = Analog mode speed Input 1h = PWM Mode Speed Input 2h = I2C Speed Input mode 3h = Frequency based speed Input mode
0	RESERVED	R/W	0h	Reserved

7.7.3.2 PIN_CONFIG2 Register (Offset = A8h) [Reset = 06000000h]

PIN_CONFIG2 is shown in Table 7-36.

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Register to configure hardware pins

Table 7-36. PIN_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	DAC_SOX_ANA_CONFIG	R/W	0h	DAC_SOX_ANA_SPEED configuration 0h = DACOUT 1h = CSA_OUT 2h = ANA_ON_PIN 3h = N/A
28-27	SLEEP_TIME	R/W	0h	Sleep Time 0h = Check low for 50 µs 1h = Check low for 200 µs 2h = Check low for 20 ms 3h = Check low for 200 ms
26-20	I2C_TARGET_ADDR	R/W	60h	I2C target address
19-14	RESERVED	R/W	0h	Reserved
13	FG_CONFIG	R/W	0h	Fault on FG Pin Configuration 0h = FG Pin ative till speed drops below BEMF threshold defined by FG_BEMF_THR 1h = FG Pin toggle as long as motor is actively driven
12-11	FG_PIN_FAULT_CONFIG	R/W	0h	FG pin status on actionable and reported faults 0h = FG Pin continues to toggle till motor stops 1h = FG Pin in Hi-Z state, pulled up externally 2h = FG Pin pulled Low 3h = N/A
10-9	FG_PIN_STOP_CONFIG	R/W	0h	FG pin status when motor is stopped 0h = FG Pin continues to toggle till motor stops 1h = FG Pin in Hi-Z state, pulled up externally 2h = FG Pin pulled Low 3h = N/A
8-5	TBLANK	R/W	0h	BEMF Comparator Blanking time after PWM edge for ZC detection 0h = 0 µs 1h = 1 µs 2h = 2 µs 3h = 3 µs 4h = 4 µs 5h = 5 µs 6h = 6 µs 7h = 7 µs 8h = 8 µs 9h = 9 µs Ah = 10 µs Bh = 11 µs Ch = 12 µs Dh = 13 µs Eh = 14 µs Fh = 15 µs
4-2	TPWDTH	R/W	0h	BEMF Comparator deglitch time 0h = 0 µs 1h = 1 µs 2h = 2 µs 3h = 3 µs 4h = 4 µs 5h = 5 µs 6h = 6 µs 7h = 7 µs

Table 7-36. PIN_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	ZERO_DUTY_HYST	R/W	0h	Duty cycle hysteresis to exit standby 0h = 0 % 1h = 2 % 2h = 4 % 3h = 6 %

7.7.3.3 DEVICE_CONFIG Register (Offset = AAh) [Reset = 00002000h]

DEVICE_CONFIG is shown in Table 7-37.

Return to the Summary Table.

Register to peripheral1

Table 7-37. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-16	INPUT_MAX_FREQUENCY	R/W	0h	Maximum frequency (in Hz) for frequency based speed input corresponding to 100% duty command. Hence, DUTY_CMD (%) = (Applied Frequency / INPUT_MAX_FREQUENCY) * 100.
15	STL_ENABLE	R/W	0h	STL enable 0h = Disable 1h = Enable
14	SSM_CONFIG	R/W	0h	SSM enable 0h = Enable 1h = Disable
13-12	RESERVED	R/W	2h	Reserved
11	DEV_MODE	R/W	0h	Device mode select 0h = Standby mode 1h = Sleep mode
10	SPD_PWM_RANGE_SELECT	R/W	0h	Speed Input PWM frequency range select 0h = 325 Hz to 95 kHz speed PWM input 1h = 10 Hz to 325 Hz speed PWM input
9-8	CLK_SEL	R/W	0h	Clock source 0h = Internal Oscillator 1h = N/A 2h = N/A 3h = External Clock input
7	EXT_CLK_EN	R/W	0h	External clock enable 0h = Disable 1h = Enable
6-4	EXT_CLK_CONFIG	R/W	0h	External clock frequency 0h = 8 kHz 1h = 16 kHz 2h = 32 kHz 3h = 64 kHz 4h = 128 kHz 5h = 256 kHz 6h = 512 kHz 7h = 1024 kHz
3-0	DIG_DEAD_TIME	R/W	0h	Digital Dead Time 0h = 0 1h = 50nS 2h = 100nS 3h = 150nS 4h = 200nS 5h = 250nS 6h = 300nS 7h = 350nS 8h = 400nS 9h = 450nS Ah = 500nS Bh = 600nS Ch = 700nS Dh = 800nS Eh = 900nS Fh = 1000nS

7.7.4 Gate_Driver_Configuration Registers

Table 7-38 lists the memory-mapped registers for the Gate_Driver_Configuration registers. All register offset addresses not listed in Table 7-38 should be considered as reserved locations and the register contents should not be modified.

Table 7-38. GATE_DRIVER_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
ACh	GD_CONFIG1	Gate driver configuration 1	GD_CONFIG1 Register (Offset = ACh) [Reset = 00000000h]
AEh	GD_CONFIG2	Gate driver configuration 2	GD_CONFIG2 Register (Offset = AEh) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. Table 7-39 shows the codes that are used for access types in this section.

Table 7-39. Gate_Driver_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.4.1 GD_CONFIG1 Register (Offset = ACh) [Reset = 00000000h]

GD_CONFIG1 is shown in Table 7-40.

Return to the Summary Table.

Register to configure gated driver settings1

Table 7-40. GD_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-20	RESERVED	R/W	0h	Reserved
19	RESERVED	R/W	0h	Reserved
18	VREF_SEL	R/W	0h	SELECT CSA CONFIG 0h = UNI DIRECTIONAL CSA 1h = BI-DIRECTIONAL CSA
17	RESERVED	R/W	0h	Reserved
16	DIS_BST_FLT	R/W	0h	Disable BST Fault 0h = Enable BST Fault 1h = Disable BST Fault
15	OTS_AUTO_RECOVERY	R/W	0h	OTS Auto recovery 0h = OTS Latched Fault 1h = OTS Auto Recovery
14-10	RESERVED	R/W	0h	Reserved
9	DIS_SNS_FLT	R/W	0h	Disable Sense Fault 0h = Enable SNS OCP Fault 1h = Disable SNS OCP Fault
8	DIS_VDS_FLT	R/W	0h	Disable VDS Fault 0h = Enable VDS OCP Fault 1h = Disable VDS OCP Fault
7	RESERVED	R/W	0h	Reserved
6-3	SEL_VDS_LVL	R/W	0h	Select the VDS_OCP Levels 0h = 0.06V 1h = 0.12V 2h = 0.18V 3h = 0.24V 4h = 0.3V 5h = 0.36V 6h = 0.42V 7h = 0.48V 8h = 0.6V 9h = 0.8V Ah = 1.0V Bh = 1.2V Ch = 1.4V Dh = 1.6V Eh = 1.8V Fh = 2.0V
2	RESERVED	R/W	0h	Reserved
1-0	CSA_GAIN	R/W	0h	Current Sense Amplifier (CSA) Gain 0h = 5V/V 1h = 10V/V 2h = 20V/V 3h = 40V/V

7.7.4.2 GD_CONFIG2 Register (Offset = AEh) [Reset = 00000000h]

GD_CONFIG2 is shown in Table 7-41.

Return to the Summary Table.

Register to configure gated driver settings2

Table 7-41. GD_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-0	RESERVED	R/W	0h	Reserved

7.8 RAM (Volatile) Register Map

7.8.1 Fault_Status Registers

Table 7-42 lists the memory-mapped registers for the Fault_Status registers. All register offset addresses not listed in Table 7-42 should be considered as reserved locations and the register contents should not be modified.

Table 7-42. FAULT_STATUS Registers

Offset	Acronym	Register Name	Section
E0h	GATE_DRIVER_FAULT_STATUS	Fault Status Register	GATE_DRIVER_FAULT_STATUS Register (Offset = E0h) [Reset = 00000000h]
E2h	CONTROLLER_FAULT_STATUS	Fault Status Register	CONTROLLER_FAULT_STATUS Register (Offset = E2h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. Table 7-43 shows the codes that are used for access types in this section.

Table 7-43. Fault_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.1.1 GATE_DRIVER_FAULT_STATUS Register (Offset = E0h) [Reset = 00000000h]

GATE_DRIVER_FAULT_STATUS is shown in Table 7-44.

Return to the Summary Table.

Status of various faults

Table 7-44. GATE_DRIVER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRIVER_FAULT	R	0h	Logic OR of driver fault registers 0h = No Gate Driver fault condition is detected 1h = Gate Driver fault condition is detected
30	PWR_ON	R	0h	Power On Detection 0h = Powerup condition is detected 1h = Powerup condition is cleared
29	RESERVED	R	0h	Reserved
28	OCP_VDS_FAULT	R	0h	Overcurrent VDS Fault status 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
27	OCP_SNS_FAULT	R	0h	Overcurrent Sense Fault status 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
26	BST_UV_FAULT	R	0h	Boot Strap UV protection status 0h = No BST undervoltage condition is detected on VM 1h = BST undervoltage condition is detected on VM
25	GVDD_UV_FLT	R	0h	GVDD UV fault status 0h = No GVDD undervoltage condition is detected on VM 1h = GVDD undervoltage condition is detected on VM
24	DRV_OFF	R	0h	Supply overvoltage protection status 0h = DRV is ON 1h = DRVOff state detected
23-0	RESERVED	R	0h	Reserved

7.8.1.2 CONTROLLER_FAULT_STATUS Register (Offset = E2h) [Reset = 00000000h]

CONTROLLER_FAULT_STATUS is shown in Table 7-45.

Return to the Summary Table.

Status of various faults

Table 7-45. CONTROLLER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONTROLLER_FAULT	R	0h	Logic OR of controller fault registers 0h = No controller fault condition is detected 1h = Controller fault condition is detected
30	RESERVED	R	0h	Reserved
29	IPD_FREQ_FAULT	R	0h	Indicates IPD frequency fault 0h = No IPD frequency fault detected 1h = IPD frequency fault detected
28	IPD_T1_FAULT	R	0h	Indicates IPD T1 fault 0h = No IPD T1 fault detected 1h = IPD T1 fault detected
27	RESERVED	R	0h	Reserved
26-24	RESERVED	R	0h	Reserved
23	ABN_SPEED	R	0h	Indicates abnormal speed motor lock condition 0h = No abnormal speed fault detected 1h = Abnormal Speed fault detected
22	LOSS_OF_SYNC	R	0h	Indicates sync lost motor lock condition 0h = No sync lost fault detected 1h = Sync lost fault detected
21	NO_MTR	R	0h	Indicates no motor fault 0h = No motor fault not detected 1h = No motor fault detected
20	MTR_LCK	R	0h	Indicates when one of the motor lock is triggered 0h = Motor lock fault not detected 1h = Motor lock fault detected
19	CBC_ILIMIT	R	0h	Indicates CBC current limit fault 0h = No CBC fault detected 1h = CBC fault detected
18	LOCK_ILIMIT	R	0h	Indicates lock detection current limit fault 0h = No lock current limit fault detected 1h = Lock current limit fault detected
17	MTR_UNDER_VOLTAGE	R	0h	Indicates motor undervoltage fault 0h = No motor undervoltag detected 1h = Motor undervoltage detected
16	MTR_OVER_VOLTAGE	R	0h	Indicates motor overvoltage fault 0h = No motor overvoltage detected 1h = Motor overvoltage detected
15	RESERVED	R	0h	Reserved
14-3	RESERVED	R	0h	Reserved
2	STL_EN	R	0h	Indicates STL is enabled in EEPROM 0h = STL Disable 1h = STL Enable
1	STL_STATUS	R	0h	Indicates STL success criteria Pass = 1b; Fail = 0b 0h = STL Fail 1h = STL Pass
0	APP_RESET	R	0h	App reset 0h = App Reset Fail 1h = App Reset Succesfull

7.8.2 System_Status Registers

Table 7-46 lists the memory-mapped registers for the System_Status registers. All register offset addresses not listed in Table 7-46 should be considered as reserved locations and the register contents should not be modified.

Table 7-46. SYSTEM_STATUS Registers

Offset	Acronym	Register Name	Section
E4h	SYS_STATUS1	System Status Register1	SYS_STATUS1 Register (Offset = E4h) [Reset = 00000000h]
EAh	SYS_STATUS2	System Status Register2	SYS_STATUS2 Register (Offset = EAh) [Reset = 00000000h]
ECh	SYS_STATUS3	System Status Register3	SYS_STATUS3 Register (Offset = ECh) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. Table 7-47 shows the codes that are used for access types in this section.

Table 7-47. System_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.2.1 SYS_STATUS1 Register (Offset = E4h) [Reset = 00000000h]

SYS_STATUS1 is shown in Table 7-48.

Return to the Summary Table.

Status of various system and motor parameters

Table 7-48. SYS_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VOLT_MAG	R	0h	Applied DC input voltage Input DC voltage (V) = (VOLT_MAG / 10)
15-1	SPEED_CMD	R	0h	Decoded speed command in PWM/Analog/Freq. mode (SPEED_CMD (%) = SPEED_CMD/32767 * 100%)
0	I2C_ENTRY_STATUS	R	0h	Indicates if I2C entry has happened 0h = I2C mode not entered through pin sequence 1h = I2C mode entered through pin sequence

7.8.2.2 SYS_STATUS2 Register (Offset = EAh) [Reset = 00000000h]

SYS_STATUS2 is shown in Table 7-49.

Return to the Summary Table.

Status of various system and motor parameters

Table 7-49. SYS_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	STATE	R	0h	Current status of state machine; 4-bit value indicating status of state machine 0h = SYSTEM_IDLE 1h = MOTOR_START 2h = MOTOR_RUN 3h = SYSTEM_INIT 4h = MOTOR_IPD 5h = MOTOR_ALIGN 6h = MOTOR_IDLE 7h = MOTOR_STOP 8h = FAULT 9h = MOTOR_DIRECTION Ah = HALL_ALIGN Ch = MOTOR_CALIBRATE Dh = MOTOR_DESCEL Eh = MOTOR_BRAKE Fh = N/A
27-18	RESERVED	R	0h	Reserved
17	STL_FAULT	R	0h	STL fault status 0h = Pass 1h = Fail
16	RESERVED	R	0h	Reserved
15-0	MOTOR_SPEED	R	0h	Speed output. Speed output (electrical Hz) = MOTOR_SPEED / 10

7.8.2.3 SYS_STATUS3 Register (Offset = ECh) [Reset = 00000000h]

SYS_STATUS3 is shown in Table 7-50.

Return to the Summary Table.

Status of various system and motor parameters

Table 7-50. SYS_STATUS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DC_BUS_CURR	R	0h	DC bus current. DC bus current (A) = DC_BUS_CURR / 256
15-0	DC_BATT_POW	R	0h	Battery (input) power. Input Power (W) = DC_BATT_POW / 64

7.8.3 Algo_Control Registers

Table 7-51 lists the memory-mapped registers for the Algo_Control registers. All register offset addresses not listed in Table 7-51 should be considered as reserved locations and the register contents should not be modified.

Table 7-51. ALGO_CONTROL Registers

Offset	Acronym	Register Name	Section
E6h	ALGO_CTRL1	Algorithm Control Parameters	ALGO_CTRL1 Register (Offset = E6h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. Table 7-52 shows the codes that are used for access types in this section.

Table 7-52. Algo_Control Access Type Codes

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.8.3.1 ALGO_CTRL1 Register (Offset = E6h) [Reset = 00000000h]

ALGO_CTRL1 is shown in Table 7-53.

Return to the Summary Table.

Algorithm Control Parameters

Table 7-53. ALGO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EEPROM_WRT	W	0h	Write the configuration to EEPROM 1h = Write to the EEPROM registers from shadow registers
30	EEPROM_READ	W	0h	Read the default configuration from EEPROM 1h = Read the EEPROM registers to shadow registers
29	CLR_FLT	W	0h	Clears all faults 1h = Clear all the driver and controller faults
28	CLR_FLT_RETRY_COUNT	W	0h	Clears fault retry count 1h = clear the lock fault retry counts
27-20	EEPROM_WRITE_ACCESS_KEY	W	0h	EEPROM write access key; 8-bit key to unlock the EEPROM write command
19-1	RESERVED	W	0h	Reserved
0	EXT_WD_STATUS_SET	W	0h	Watchdog status to be set by external MCU in I2C watchdog mode 0h = Reset automatically by the MCC 1h = To set the EXT_WD_STATUS_SET

7.8.4 Device_Control Registers

Table 7-54 lists the memory-mapped registers for the Device_Control registers. All register offset addresses not listed in Table 7-54 should be considered as reserved locations and the register contents should not be modified.

Table 7-54. DEVICE_CONTROL Registers

Offset	Acronym	Register Name	Section
E8h	DEVICE_CTRL	Device Control Parameters	DEVICE_CTRL Register (Offset = E8h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. Table 7-55 shows the codes that are used for access types in this section.

Table 7-55. Device_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.8.4.1 DEVICE_CTRL Register (Offset = E8h) [Reset = 00000000h]

DEVICE_CTRL is shown in Table 7-56.

Return to the Summary Table.

Device Control Parameters

Table 7-56. DEVICE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	W	0h	Reserved
30-16	SPEED_CTRL	W	0h	Digital speed command. (SPEED_CTRL (%) = SPEED_CTRL/32767 * 100%)
15	OVERRIDE	W	0h	Speed input select for I2C vs speed pin 0h = SPEED_CMD using Analog/Freq/PWM mode 1h = SPEED_CMD using SPD_CTRL[14:0]
14-0	RESERVED	R	0h	Reserved

7.8.5 Algorithm_Variables Registers

Table 7-57 lists the memory-mapped registers for the Algorithm_Variables registers. All register offset addresses not listed in Table 7-57 should be considered as reserved locations and the register contents should not be modified.

Table 7-57. ALGORITHM_VARIABLES Registers

Offset	Acronym	Register Name	Section
40Ch	INPUT_DUTY	Input Duty Cycle	INPUT_DUTY Register (Offset = 40Ch) [Reset = 00000000h]
512h	CURRENT_DUTY	Current Duty Cycle	CURRENT_DUTY Register (Offset = 512h) [Reset = 00000000h]
522h	SET_DUTY	Set Duty Cycle	SET_DUTY Register (Offset = 522h) [Reset = 00000000h]
5CEh	MOTOR_SPEED_PU	Motor Speed in PU	MOTOR_SPEED_PU Register (Offset = 5CEh) [Reset = 00000000h]
714h	DC_BUS_POWER_PU	DC Bus Power in PU	DC_BUS_POWER_PU Register (Offset = 714h) [Reset = 00000000h]

Complex bit access types are encoded to fit into small table cells. Table 7-58 shows the codes that are used for access types in this section.

Table 7-58. Algorithm_Variables Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.5.1 INPUT_DUTY Register (Offset = 40Ch) [Reset = 00000000h]

INPUT_DUTY is shown in Table 7-59.

Return to the Summary Table.

Input duty cycle set by the user

Table 7-59. INPUT_DUTY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INPUT_DUTY	R	0h	32-bit value indicating the duty cycle that the user commands. Input duty cycle (in %) = (Input Duty Cycle / 2^{30}) * 100

7.8.5.2 CURRENT_DUTY Register (Offset = 512h) [Reset = 00000000h]

CURRENT_DUTY is shown in Table 7-60.

Return to the Summary Table.

Current duty cycle

Table 7-60. CURRENT_DUTY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CURRENT_DUTY	R	0h	32-bit value indicating the duty cycle that is currently being applied. Current duty cycle (in %) = (Current Duty Cycle / 2^{30}) * 100

7.8.5.3 SET_DUTY Register (Offset = 522h) [Reset = 00000000h]

SET_DUTY is shown in Table 7-61.

Return to the Summary Table.

Target duty cycle at the present motor state

Table 7-61. SET_DUTY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SET_DUTY	R	0h	32-bit value indicating the duty cycle that the existing state (start up, OL, CL) of algorithm wants. Set duty cycle (in %) = (Set Duty Cycle / 2^{30}) * 100

7.8.5.4 MOTOR_SPEED_PU Register (Offset = 5CEh) [Reset = 00000000h]

MOTOR_SPEED_PU is shown in Table 7-62.

Return to the Summary Table.

Motor speed in PU

Table 7-62. MOTOR_SPEED_PU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MOTOR_SPEED_PU	R	0h	32-bit value indicating the speed of the motor (functional in closed loop). Motor speed (in Hz) = (Motor Speed in PU / 2^{30}) * Maximum speed

7.8.5.5 DC_BUS_POWER_PU Register (Offset = 714h) [Reset = 00000000h]

DC_BUS_POWER_PU is shown in Table 7-63.

Return to the Summary Table.

DC bus power in PU

Table 7-63. DC_BUS_POWER_PU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DC_BUS_POWER_PU	R	0h	32-bit value indicating the power drawn by the motor (functional in closed loop). DC Bus Power (in W) = (DC Bus Power in PU / 2^{30}) * Maximum power

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The MCT8329A is used in 3-phase sensorless trapezoidal motor control applications such as Cordless vacuum cleaners, HVAC blowers and ventilators, Appliance fans, pumps and Medical CPAP blowers.

8.2 Typical Applications

Figure 8-1 shows the typical schematic of MCT8329A. Table 7-1 shows the recommended values of the external components for the driver.

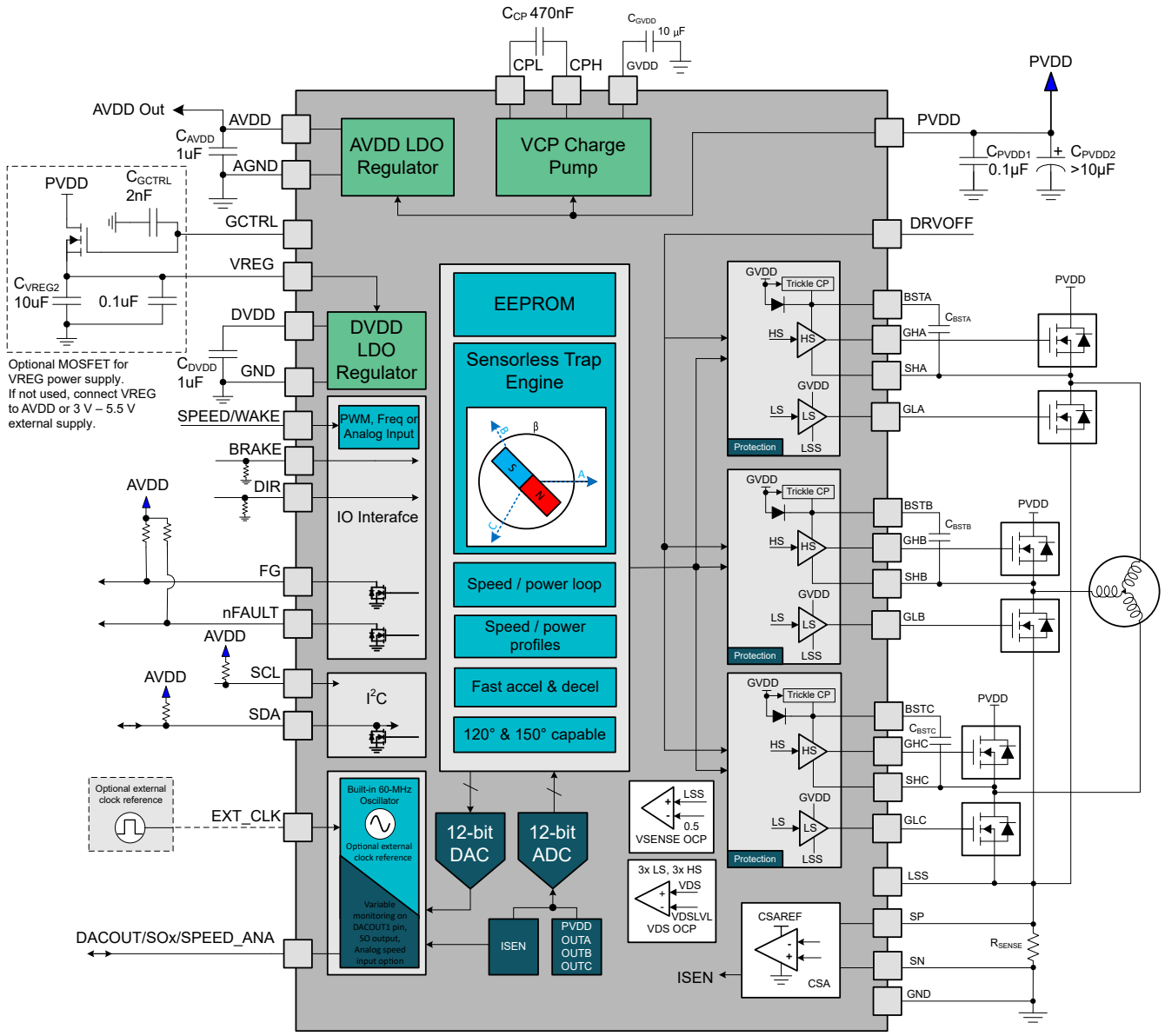


Figure 8-1. Typical Schematic of MCT8329A

Detailed Design Procedure

Table below lists the example input parameters for the system design.

Table 8-1. Design parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{PVDD}	24 V
Motor peak current	I_{PEAK}	20 A
PWM Frequency	f_{PWM}	20 kHz
MOSFET VDS Slew Rate	SR	120 V/us
MOSFET input gate capacitance	Q_G	54 nC
MOSFET input gate capacitance	Q_{GD}	14 nC
Dead time	t_{dead}	200 ns

Table 8-1. Design parameters (continued)

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Overcurrent protection	I_{OCP}	30 A

Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. Equation 20 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \quad (20)$$

ΔV_{BSTX}=12 V – 0.85 V – 4.45 V = 6.7 V

where

- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In the example, allowed voltage drop across bootstrap capacitor is 6.7 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and GVDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5 V to 1 V.

The total charge needed per switching cycle can be estimated with Equation 21:

$$Q_{TOT} = Q_G + \frac{IL_{BS\_TRAN}}{f_{SW}} \quad (21)$$

Q_{TOT}=54 nC + 115 µA/20 kHz = 54 nC + 5.8 nC = 59.8nC

where

- Q_G is the total MOSFET gate charge
- IL_{BS_TRAN} is the bootstrap pin leakage current
- f_{SW} is the is the PWM frequency

The minimum bootstrap capacitor can then be estimated as below assuming 1V of ΔV_{BSTx}:

$$C_{BST\_MIN} = {Q_{TOT}}/{\Delta V_{BSTX}} \quad (22)$$

C_{BST_MIN}= 59.8 nC / 1 V = 59.8 nF

The calculated value of minimum bootstrap capacitor is 59.8 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100 nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \geq 10 \times C_{BSTX} \quad (23)$$

C_{GVDD}= 10*100 nF= 1 µF

For this example application, choose a 1-µF C_{GVDD} capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long-term reliability of the system.

Note

For higher power system requiring 100% duty cycle support for longer duration it is recommended to use C_{BSTx} of ≥1µF and C_{GVDD} of ≥10 µF.

8.2.1 Selection of External MOSFET for VREG Power Supply

The MCT8329A device provides option to drive external MOSFET (using GCTRL pin) which can act as regulator to power internal digital circuitry through VREG pin, as explained in Section 7.3.4.3. Select the external MOSFET to make sure that the VREG pin voltage is between 2.2 V to 5.5 V across operating conditions. As an example calculation, use Equation 24 for the MOSFET selection to get a minimum VREG pin voltage of 2.4 V at a minimum GCTRL pin voltage of 4.9V ($V_{GCTRL(min)}$ - $V_{VREG(min)}$ = 2.5 V). Use Equation 25 to ensure that the maximum voltage at VREG pin is less than 5.5 V at maximum GCTRL pin voltage.

$$V_{GS(th)\_max} + V_{PVDD}\left(\frac{C_{GD}}{C_{GD} + C_{GCTRL}}\right) + \left(1.3 \times I_{GATE\_LEAK} \times 10^{6}\right) < 2.5\,V \quad (24)$$

$$V_{GCTRL(\max)} - V_{GS(th)\_min} < 5.5\,V \quad (25)$$

where,

$V_{GS(th)\_max}$ is the maximum gate to source threshold voltage of the external MOSFET across operating condition

$V_{GS(th)\_min}$ is the minimum gate to source threshold voltage of the external MOSFET across operating condition

V_{PVDD} is the voltage at the drain of the external MOSFET

C_{GD} is the gate to drain capacitance of the external MOSFET

C_{GCTRL} is the capacitance connected between GCTRL pin and GND

I_{GATE_LEAK} is the maximum gate leakage of the external MOSFET

$V_{GCTRL(max)}$ is the maximum voltage at GCTRL pin

The external MOSFET has to be selected so that the GCTRL pin voltage does not peak more than 0.5V from operating maximum value of GCTRL pin voltage and use Equation 26 for the MOSFET selection.

$$V_{PVDD}\left(\frac{C_{GD}}{C_{GD} + C_{GCTRL}}\right) + \left(1.3 \times I_{GATE\_LEAK} \times 10^{6}\right) < 0.5\,V \quad (26)$$

Table 8-2. Example External MOSFET

Part Number	V_{DS}(V)	Max $V_{GS(TH)}$ (V)	C_{ISS} (pF)	GCTRL-GND Cap (nF)	GCTRL Start up time (ms)
CSD18534Q5A	60	2.3	1770	2	20

Gate Drive Current

Selecting an appropriate gate drive current is essential when turning on or off power MOSFETs gates to switch motor current. The amount of gate drive current and input capacitance of the MOSFETs determines the drain-to-source voltage slew rate (V_{DS}). Gate drive current can be sourced from GVDD into the MOSFET gate (I_{SOURCE}) or sunk from the MOSFET gate into SHx or LSS (I_{SINK}).

Using too high of a gate drive current can turn on MOSFETs too quickly which may cause excessive ringing, dV/dt coupling, or cross-conduction from switching large amounts of current. If parasitic inductances and capacitances exist in the system, voltage spiking or ringing may occur which can damage the MOSFETs or MCT8329A device.

On the other hand, using too low of a gate drive current causes long V_{DS} slew rates. Turning on the MOSFETs too slowly may heat up the MOSFETs due to $R_{DS,on}$ switching losses.

The relationship between gate drive current I_{GATE}, MOSFET gate-to-drain charge Q_{GD}, and V_{DS} slew rate switching time $t_{rise,fall}$ are described by the following equations:

$$SR_{DS} = \frac{V_{DS}}{t_{rise,fall}} \quad (27)$$

$$I_{GATE} = \frac{Q_{gd}}{t_{rise,fall}} \quad (28)$$

It is recommend to evaluate at lower gate drive currents and increase gate drive current settings to avoid damage from unintended operation during initial evaluation.

Gate Resistor Selection

The slew rate of the SHx connection will be dependent on the rate at which the gate of the external MOSFETs is controlled. The pull-up/pull-down strength of MCT8329A is fixed internally, hence the slew rate of gate voltage can be controlled with an external series gate resistor. In some applications, the gate charge of the MOSFET, which is the load on gate driver device, is significantly larger than the gate driver peak output current capability. In such applications, external gate resistors can limit the peak output current of the gate driver. External gate resistors are also used to dampen ringing and noise.

The specific parameters of the MOSFET, system voltage, and board parasitics will all affect the final SHx slew rate, so generally selecting an optimal value or configuration of external gate resistor is an iterative process.

To lower the gate drive current, a series resistor R_{GATE} can be placed on the gate drive outputs to control the current for the source and sink current paths. A single gate resistor will have the same gate path for source and sink gate current, so larger R_{GATE} values will yield similar SHx slew rates. Note that gate drive current varies by PVDD voltage, junction temperature, and process variation of the device.

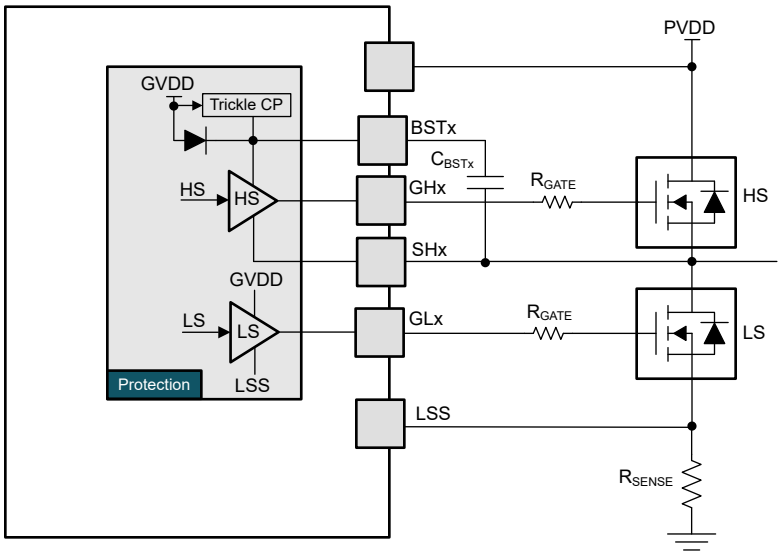


Figure 8-2. Gate driver outputs with series resistors

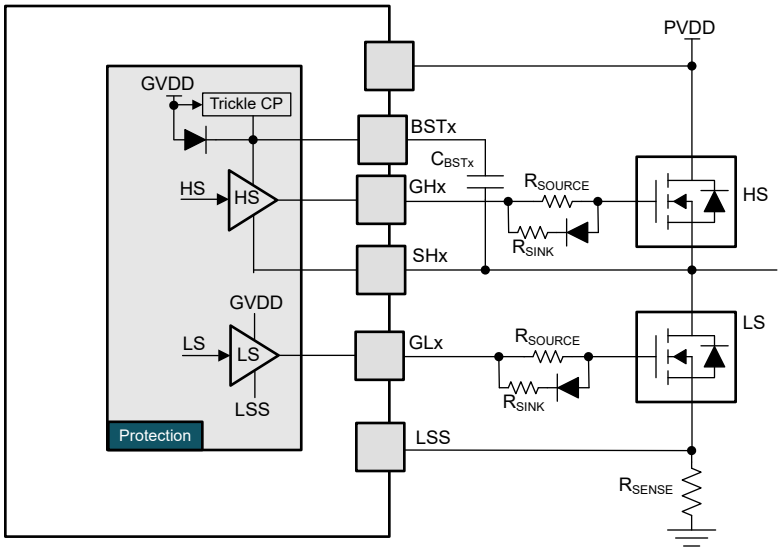


Figure 8-3. Gate driver outputs with separate source and sink current paths

Typically, it is recommended to have the sink current be twice the source current to implement a strong pull-down from gate to the source to ensure the MOSFET stays off while the opposite FET is switching. This can be implemented discretely by providing a separate path through a resistor for the source and sink currents by placing a diode and sink resistor (R_{SINK}) in parallel to the source resistor (R_{SOURCE}). Using the same value of source and sink resistors results in half the equivalent resistance for the sink path. This yields twice the gate drive sink current compared to the source current, and SHx will slew twice as fast when turning off the MOSFET.

System Considerations in High Power Designs

Higher power system designs can require design and application considerations that are not regarded in lower power system designs. It is important to combat the volatile nature of higher power systems by implementing troubleshooting guidelines, external components and circuits, driver product features, or layout techniques. For more information, please visit the System Design Considerations for High-Power Motor Driver Applications application note.

Capacitor Voltage Ratings

Use capacitors with voltage ratings that are 2x the supply voltage (PVDD, GVDD, AVDD, etc). Capacitors can experience up to half the rated capacitance due to poor DC voltage rating performance.

For example, since the bootstrap voltage is around 12 to 13-V with respect to SHx (BSTx-SHx) then the BSTx-SHx capacitor should be rated for 25-V or greater.

External Power Stage Components

External components in the power stage are not required by design but are helpful in suppressing transients, managing inductor coil energy, mitigating supply pumping, dampening phase ringing, or providing strong gate-to-source pulldown paths. These components are used for system tuning and debuggability so the BLDC motor system is robust while avoiding damage to the MCT8329A device or external MOSFETs.

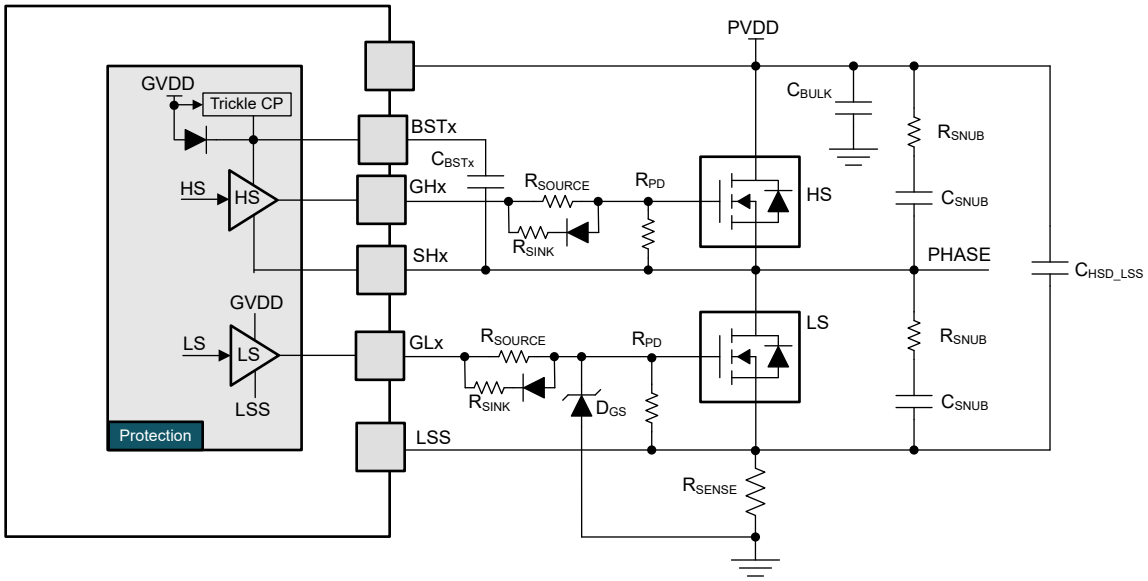


Figure 8-4. Optional external power stage components

Some examples of issues and external components that can resolve those issues are found in table below.

Table 8-3. Common issues and resolutions for power stage debugging

Issue	Resolution	Components
Gate drive current required is too large, resulting in very fast MOSFET V_{DS} slew rate	Series resistors required for gate drive current adjustability	0-100 Ω series resistors (RGATE/RSOURCE) at gate driver outputs (GHx/GLx), optional sink resistor (RSINK) and diode in parallel with gate resistor for adjustable sink current
Ringing at phase's switch node (SHx) resulting in high EMI emissions	RC snubbers placed in parallel to each HS/LS MOSFET to dampen oscillations	Resistor (RSNUB) and Capacitor (CSNUB) placed parallel to the MOSFET, calculate RC values based on ringing frequency using Proper RC Snubber Design for Motor Drivers
Negative transients at low-side source (LSS) below minimum specification	HS drain to LS source capacitor to suppress negative bouncing	0.01uF-1uF, PVDD-rated capacitor from PVDD-LSS (CHSD_LSS) placed near LS MOSFET's source
Negative transient at low-side gate (GLx) below minimum specification	Gate-to-ground Zener diode to clamp negative voltage	GVDD voltage rated Zener diode (DGS) with anode connected to GND and cathode connected to GLx
Extra protection required to ensure MOSFET is turned off if gate drive signals are Hi-Z	External gate-to-source pulldown resistors (after series gate resistors)	10 kΩ to 100 kΩ resistor (RPD) connected from gate to source for each MOSFET

8.2.2 Application curves

8.2.2.1 Motor startup

Figure 8-5 shows the phase current waveforms of various startup methods in MCT8329A such as align, double align, IPD and slow first cycle.

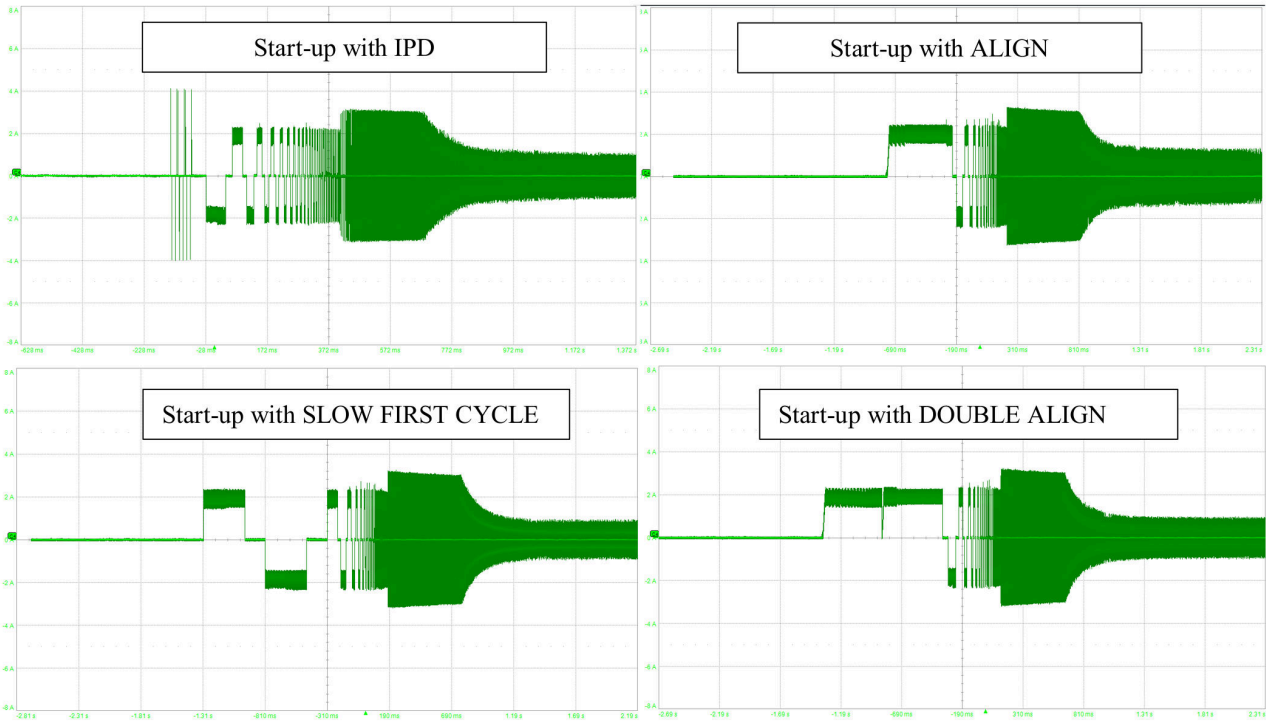


Figure 8-5. Motor phase current waveforms of all startup methods

8.2.2.2 120º and variable commutation

In 120° commutation scheme, each motor phase is driven for 120° and Hi-Z for 60° within each half electrical cycle, resulting in six different commutation states for a motor. Figure 8-6 shows the phase current and current waveform FFT in 120° commutation mode. In variable commutation scheme, MCT8329A device switches dynamically between 120° and 150° trapezoidal commutation depending on motor speed. The device operates

in 150° mode at lower speeds and moves to 120° mode at higher speeds. Figure 8-7 shows the phase current and current waveform FFT in 150° commutation.

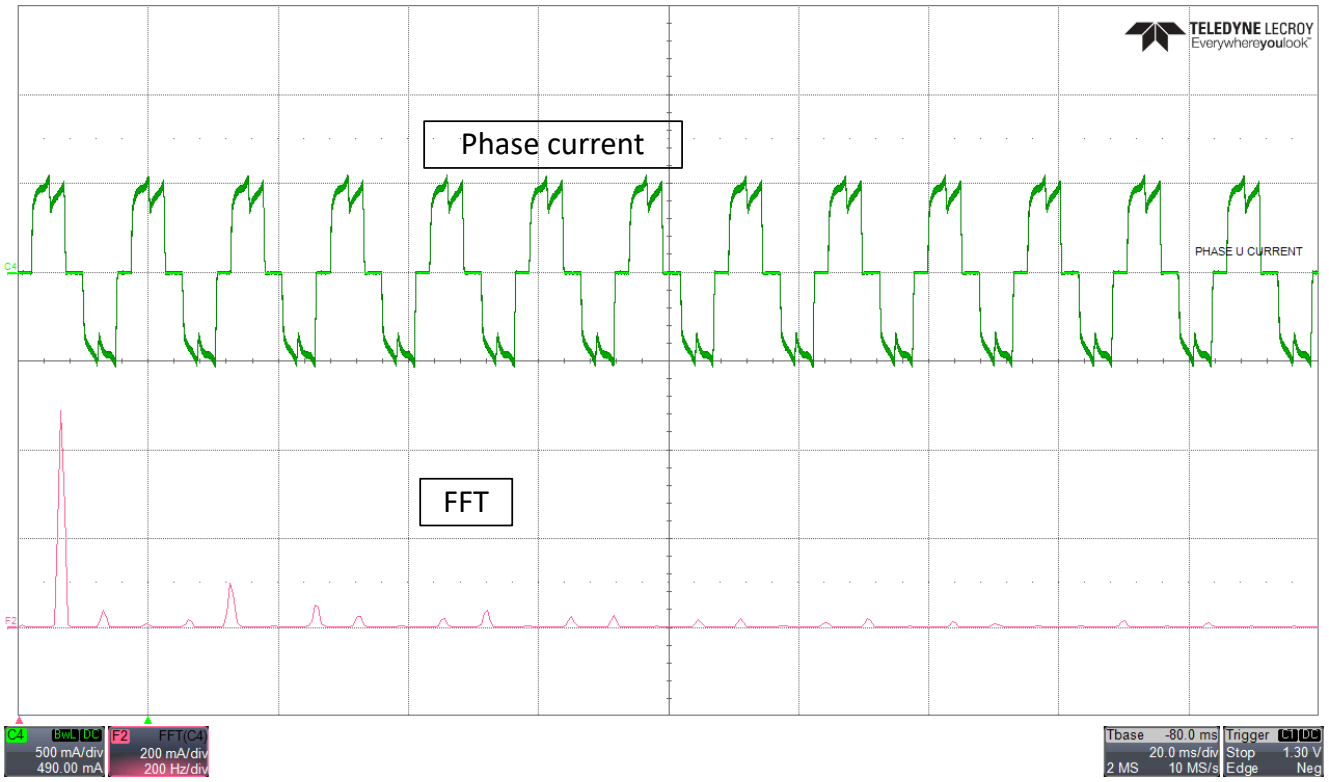


Figure 8-6. Phase current and FFT - 120 °commutation

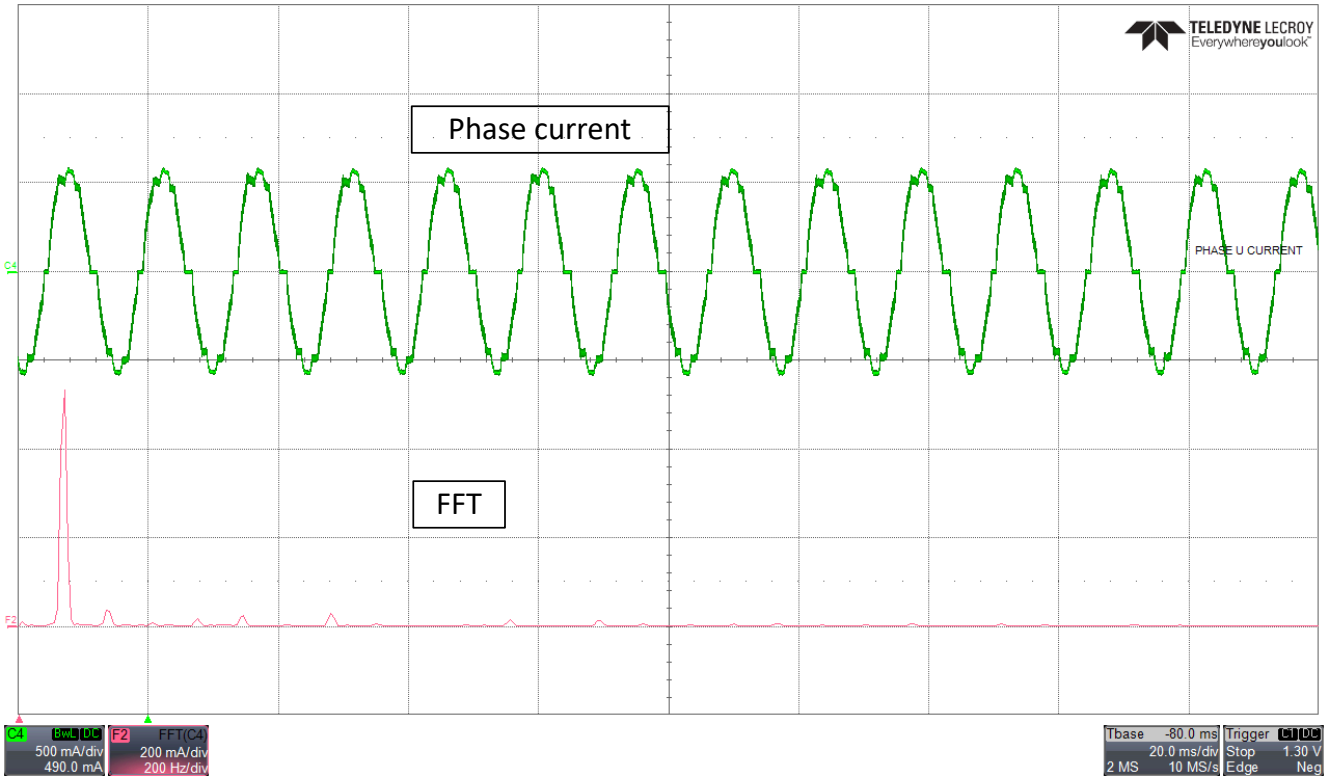


Figure 8-7. Phase current and FFT - 150°commutation

8.2.2.3 Faster startup time

Startup time is the time taken for the motor to reach the target speed from zero speed. Faster startup time can be achieved in MCT8329A by tuning motor startup, open loop and closed loop settings. Figure 8-8 shows FG, phase current and motor electrical speed waveform. Motor takes 50 ms to reach target speed from zero speed.

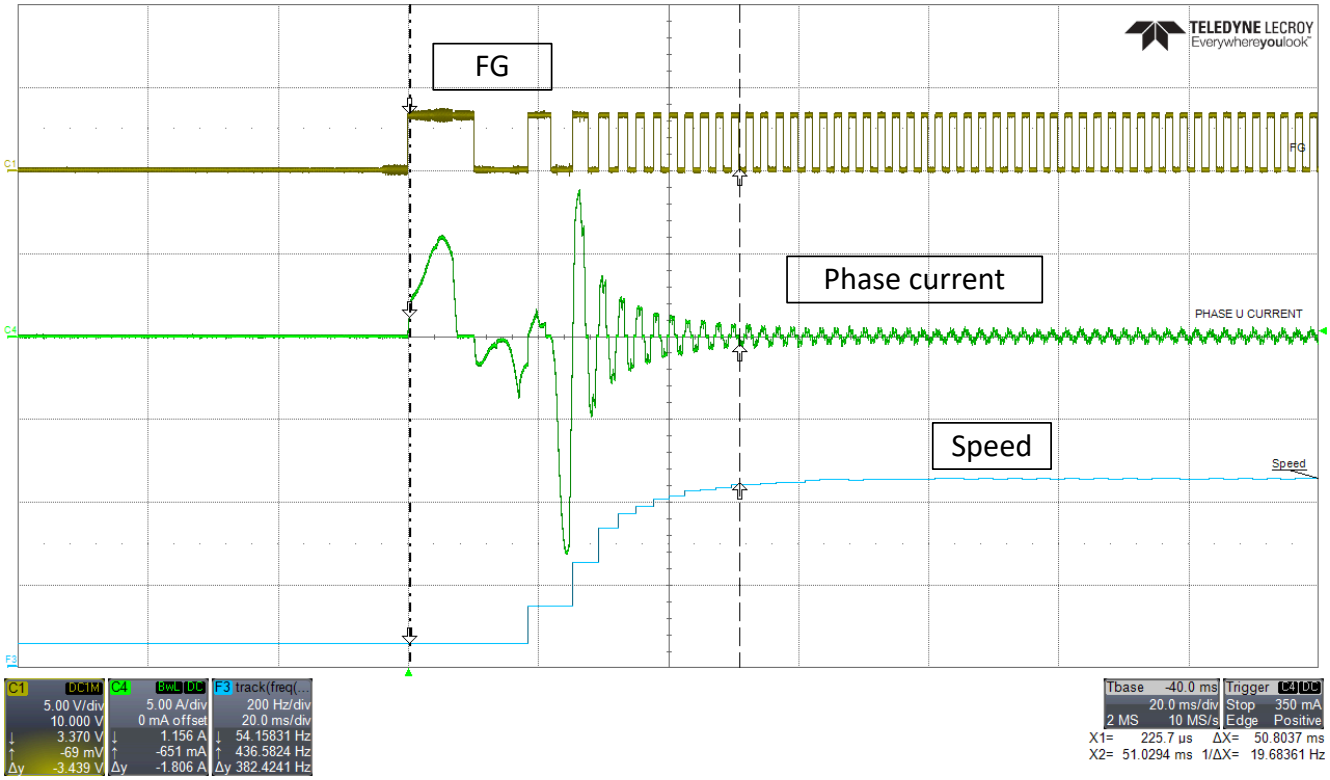


Figure 8-8. Phase current, FG and motor speed - Faster startup time

8.2.2.4 Setting the BEMF threshold

The BEMF_THRESHOLD1 and BEMF_THRESHOLD2 values used for commutation instant detection in MCT8329A can be computed from the motor phase voltage waveforms during coasting. For example, consider the three-phase voltage waveforms of a BLDC motor while coasting as in Figure 8-9. The motor phase voltage during coasting is the motor back-EMF.

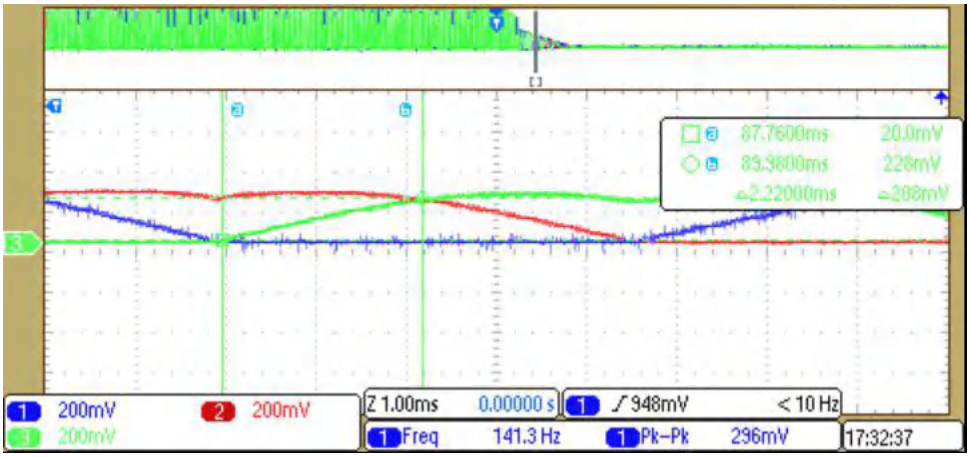


Figure 8-9. Motor phase voltage during coasting

In Figure 8-9, one floating phase voltage interval is denoted by the vertical markers on channel 3. The Vpeak (peak-peak back-EMF) on channel 3 is 208-mV and Tc (commutation interval) is 2.22-ms as denoted by the horizontal and vertical markers on channel 3. The digital equivalent counts for Vpeak and Tc are calculated as follows.

In MCT8329A, a 3-V analog input corresponds to 4095 counts(12-bit) and phase voltage is scaled down by 10x factor before ADC input; therfore, Vpeak of 208-mV corresponds to an ADC input of 20.8mV, which in turn equals 29 ADC counts. Assuming the PWM switching frequency is 25-kHz, one back-EMF sample is available every 40-µs. So, in a time interval of 2.22-ms, a total of 55 back-EMF samples are integrated. Therefore, the BEMF_THRESHOLD1 or BEMF_THRESHOLD2 value calculated is (½) * (29/2) * (55/2) = 199. Hence, in this example, BEMF_THRESHOLD1 and BEMF_THRESHOLD2 are set to 8h (corresponding to 200 which is the closest value to 199) for commutation instant detection using back-EMF integration method during fast start-up. The exact speed at which the Vpeak and Tc values are measured to calculate the BEMF_THRESHOLD1 and BEMF_THRESHOLD2 values is not critical (as long as there is sufficient resolution in digital counts) since the product (Vpeak * Tc) is, largely, a constant for a given BLDC motor.

8.2.2.5 Maximum speed

Figure 8-10 shows phase current, phase voltage and FG of a motor that spins at maximum electrical speed of 3 kHz.

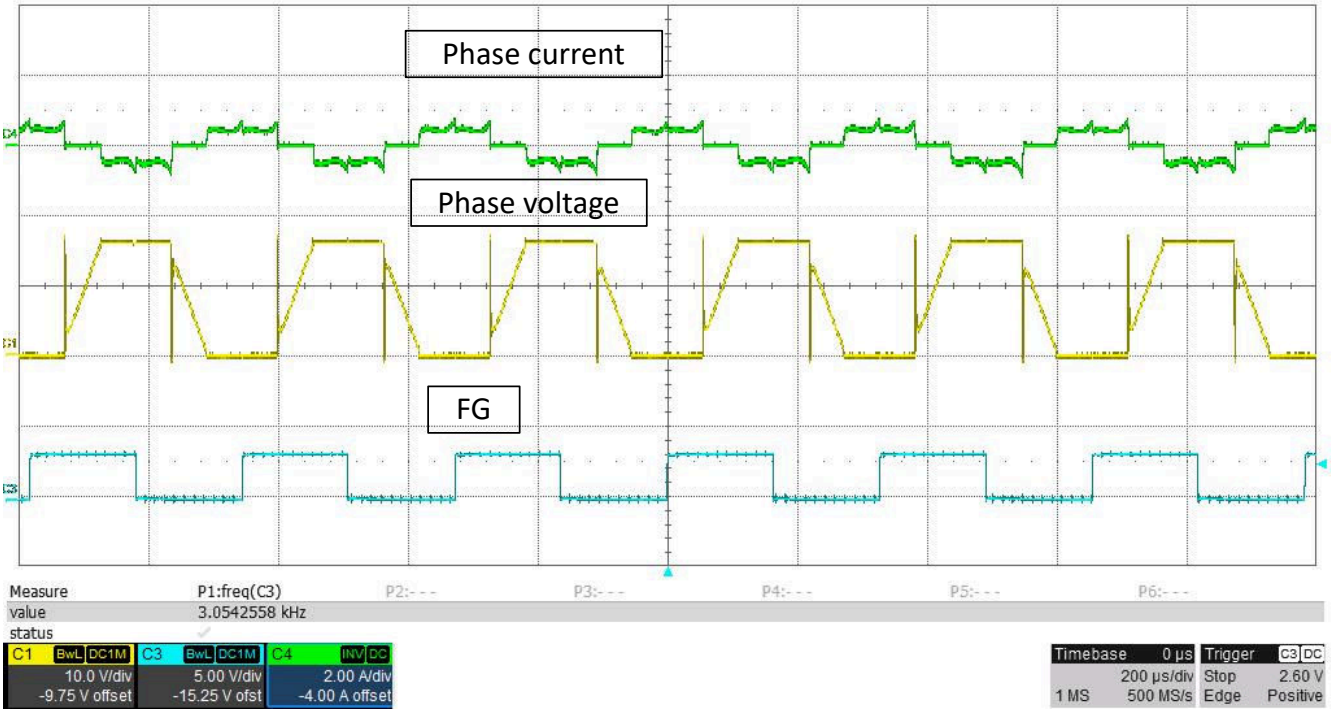


Figure 8-10. Phase current, Phase voltage and FG at Maximum speed

8.2.2.6 Faster deceleration

MCT8329A has features to decelerate the motor quickly. Figure 8-11 shows phase current and motor electrical speed waveform when the motor decelerates from 100% duty cycle to 10% duty cycle. Time taken for the motor to decelerate from 100% duty cycle to 10% duty cycle when fast deceleration is disabled is around 10 seconds. Figure 8-12 shows phase current and motor electrical speed waveform when the motor decelerates from 100% duty cycle to 10% duty cycle. Time taken for the motor to decelerate from 100% duty cycle to 10% duty cycle when fast deceleration is enabled is around 1.5 seconds.

Note

Please note that when fast deceleration is enabled and anti-voltage surge (AVS) is disabled, there might be voltage spikes seen in supply voltage. Enable AVS to protect the power supply from voltage overshoots during motor deceleration.

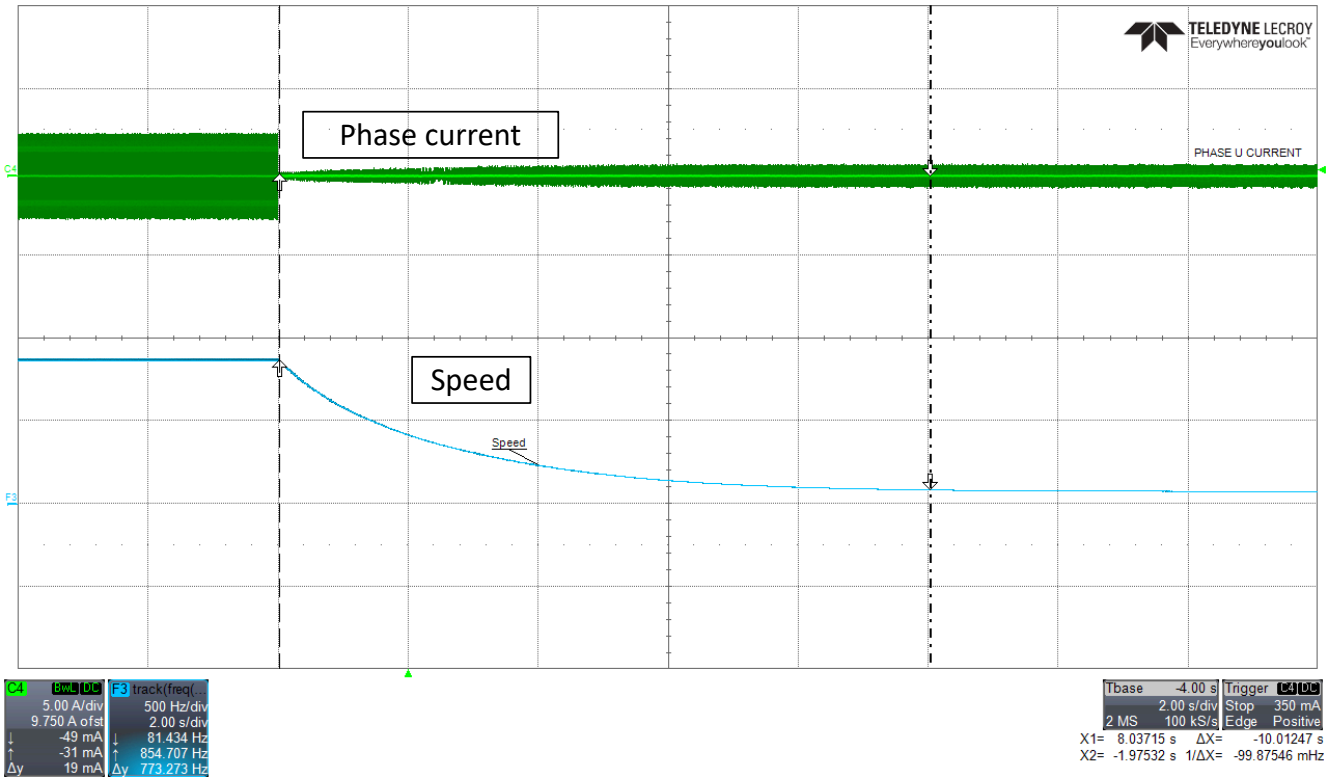


Figure 8-11. Phase current and motor speed - Faster deceleration disabled

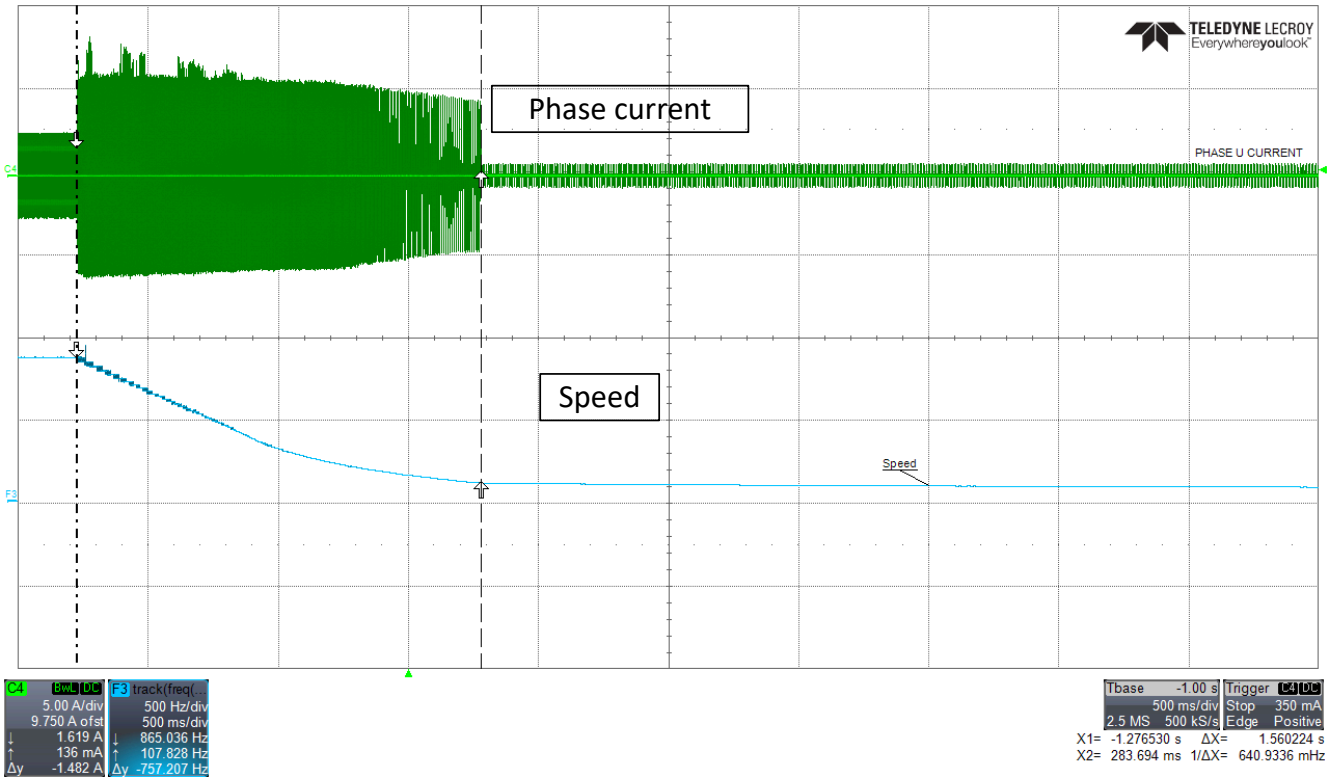


Figure 8-12. Phase current and motor speed -Faster deceleration enabled

9 Power Supply Recommendations

The MCT8329A is designed to operate from an input voltage supply (PVDD) range from 4.5 V to 60 V. A 10-µF and 0.1-µF ceramic capacitor rated for PVDD must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the PVDD pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in PVDD voltage. When adequate bulk capacitance is used, the PVDD voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor. The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

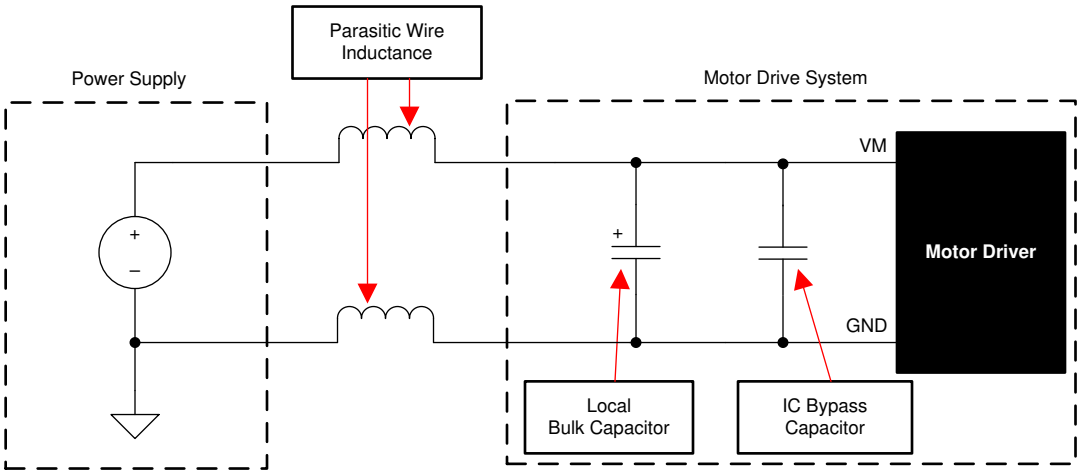


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

Bypass the PVDD pin to the GND (PGND) pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the PVDD pin using a bulk capacitor rated for PVDD. This component can be electrolytic. This capacitance must be at least 10 µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 470 nF, rated for PVDD, and be of type X5R or X7R.

The bootstrap capacitors (BSTx-SHx) should be placed closely to device pins to minimize loop inductance for the gate drive paths.

Bypass the AVDD pin to the AGND pin with a 1-µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

Bypass the DVDD pin to the GND pin with a 1-µF low-ESR ceramic capacitor rated for ≥ 4 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the GND pin.

Bypass the VREG pin with an adequate low-ESR ceramic capacitor rated of type X5R or X7R.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

When designing higher power systems, physics in the PCB layout can cause parasitic inductance, capacitance, and impedance that deter the performance of the system. Understanding the parasitic that are present in a higher power motor drive system can help designers mitigate their effects through good PCB layout. For more information, please visit the System Design Considerations for High-Power Motor Driver Applications and Best Practices for Board Layout of Motor Drivers application notes.

Gate drive traces (BSTx, GHx, SHx, GLx, LSS) should be at least 15-20mil wide and as short as possible to the MOSFET gates to minimize parasitic inductance and impedance. This helps supply large gate drive currents, turn MOSFETs on efficiently, and improves VGS and VDS monitoring. Ensure that the shunt resistor selected to monitor the low-side current from LSS to GND, is wide to minimize inductance introduced at the low-side source LSS.

Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance. The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the heat that is generated in the device. To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

10.2 Layout Example

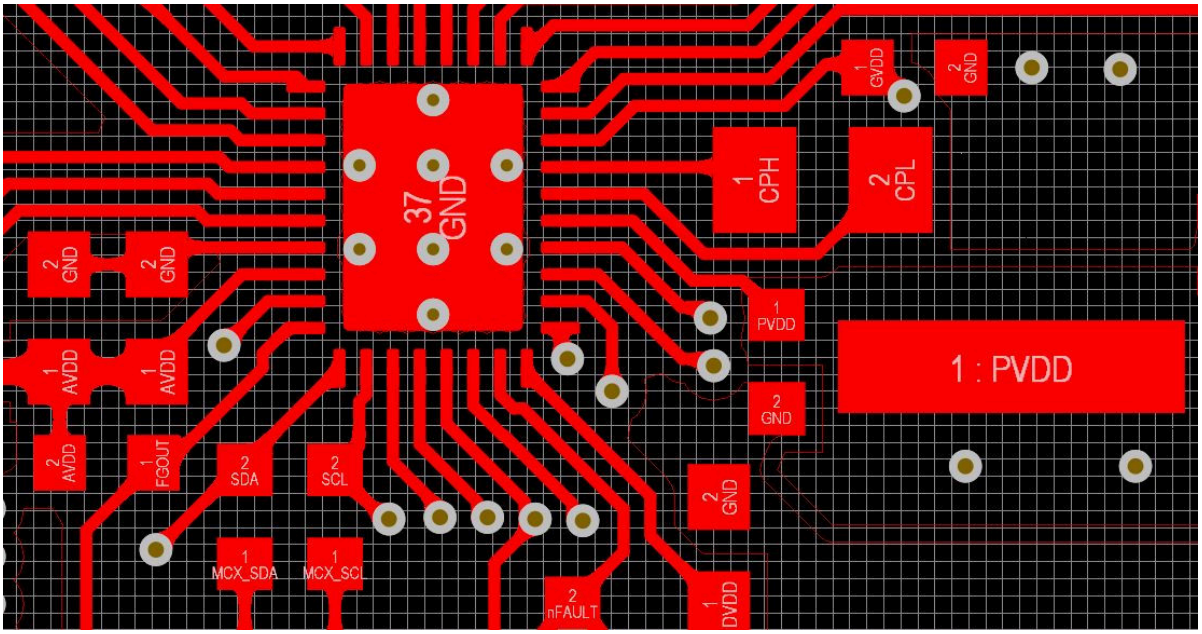


Figure 10-1. Layout example of MCT8329A device

10.3 Thermal Considerations

The MCT8329A has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heat-sinking, or too high an ambient temperature.

10.3.1 Power Dissipation

The MCT8329A integrates a variety of circuits that contribute to total power losses. These power losses include standby power losses, GVDD power losses, AVDD power losses, DVDD power losses. At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration. The maximum amount of power that the device can dissipate depends on ambient temperature and heat-sinking.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- Refer to the application note Power Delivery in Cordless Power Tools Using DRV8329
- Refer to the application note System Design Considerations for High-Power Motor Driver Applications
- Refer to the E2E FAQ How to Conduct a BLDC Schematic Review and Debug
- Refer to the application note Best Practices for Board Layout of Motor Drivers
- Refer to the application note QFN and SON PCB Attachment
- Refer to the application note Cut-Off Switch in High-Current Motor-Drive Applications

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

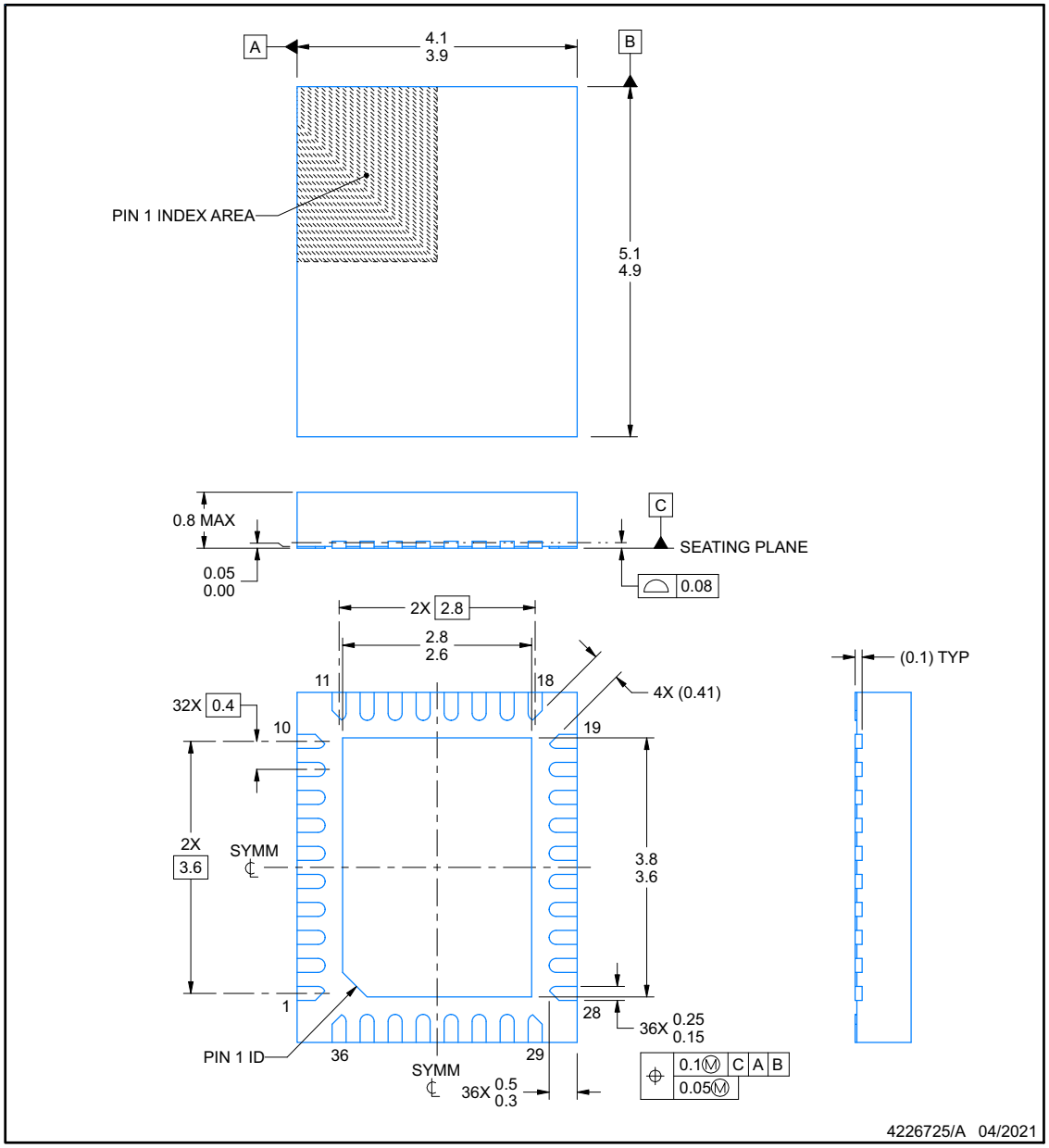
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGE OUTLINE

REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

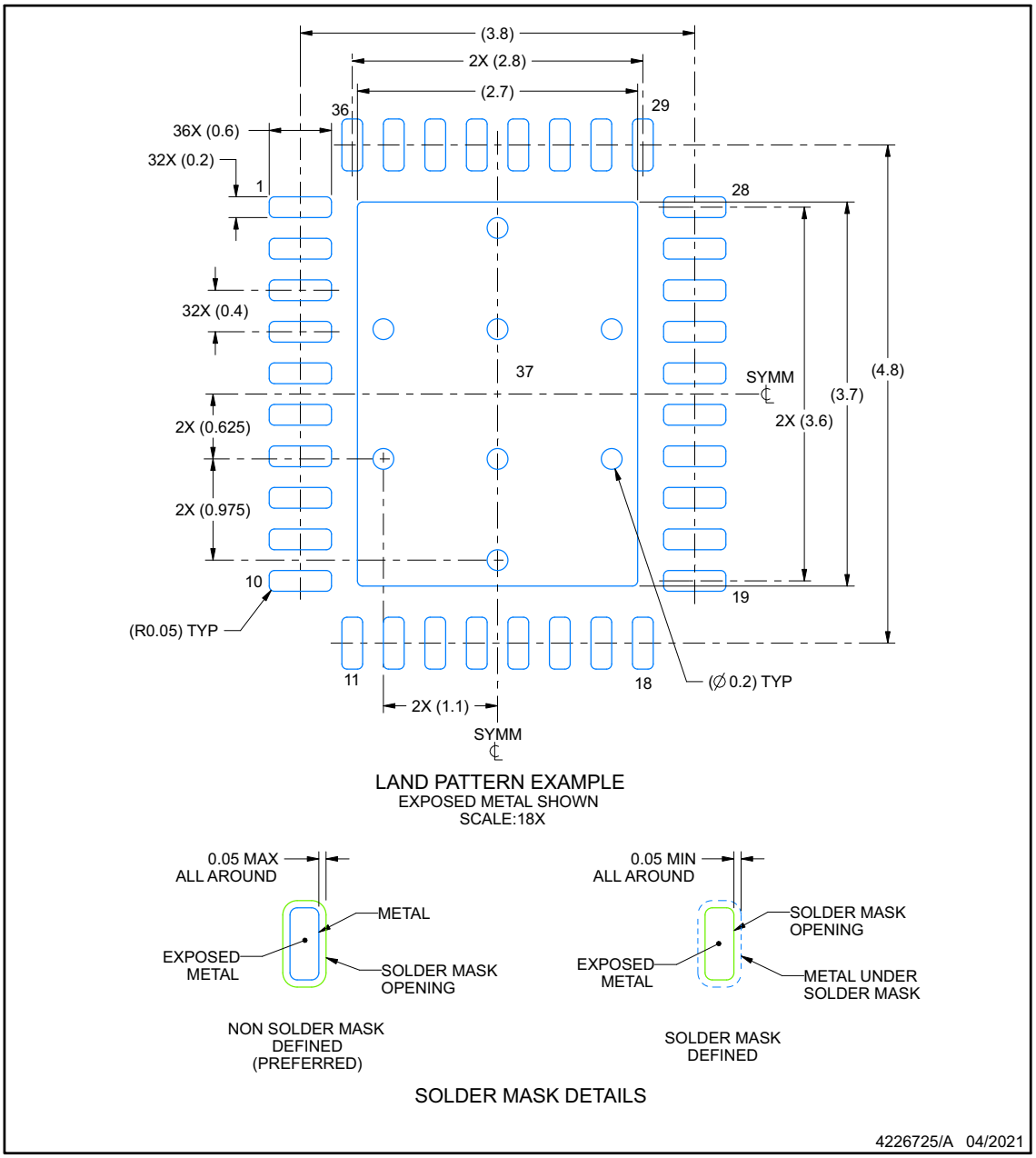
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

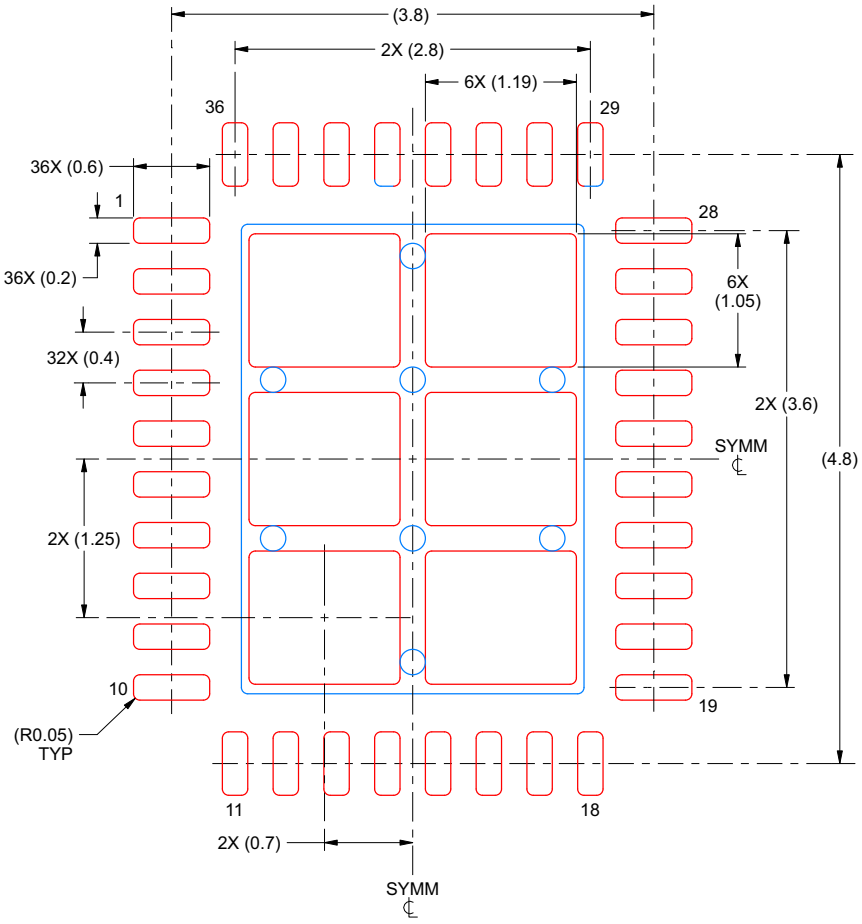
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4226725/A 04/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MCT8329A1IREER	Active	Production	WQFN (REE) | 36	5000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	MCT83 29A1I
MCT8329A1IREER.A	Active	Production	WQFN (REE) | 36	5000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	MCT83 29A1I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

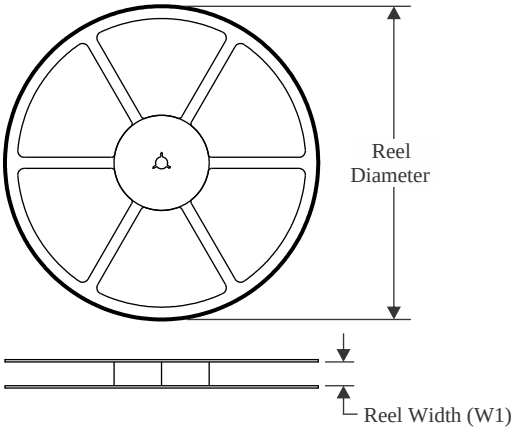
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

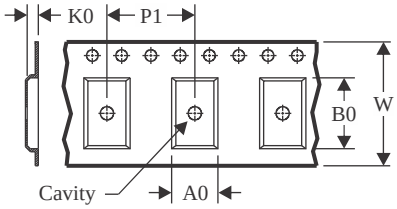
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

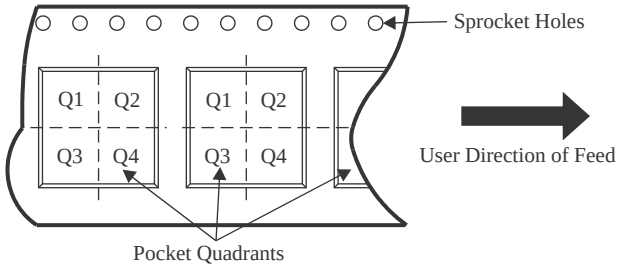


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

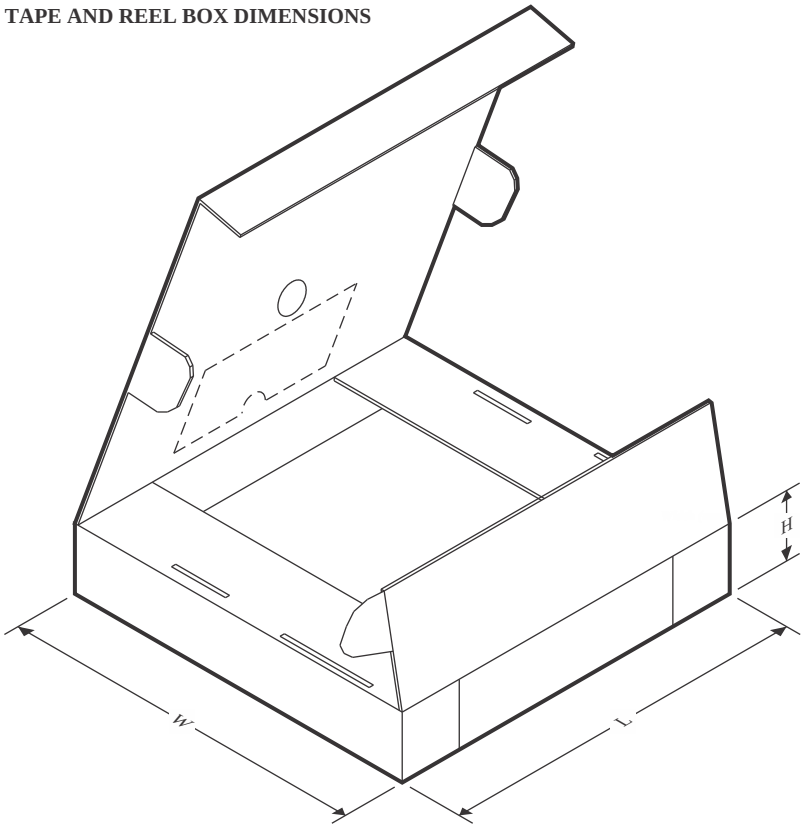
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCT8329A1IREER	WQFN	REE	36	5000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

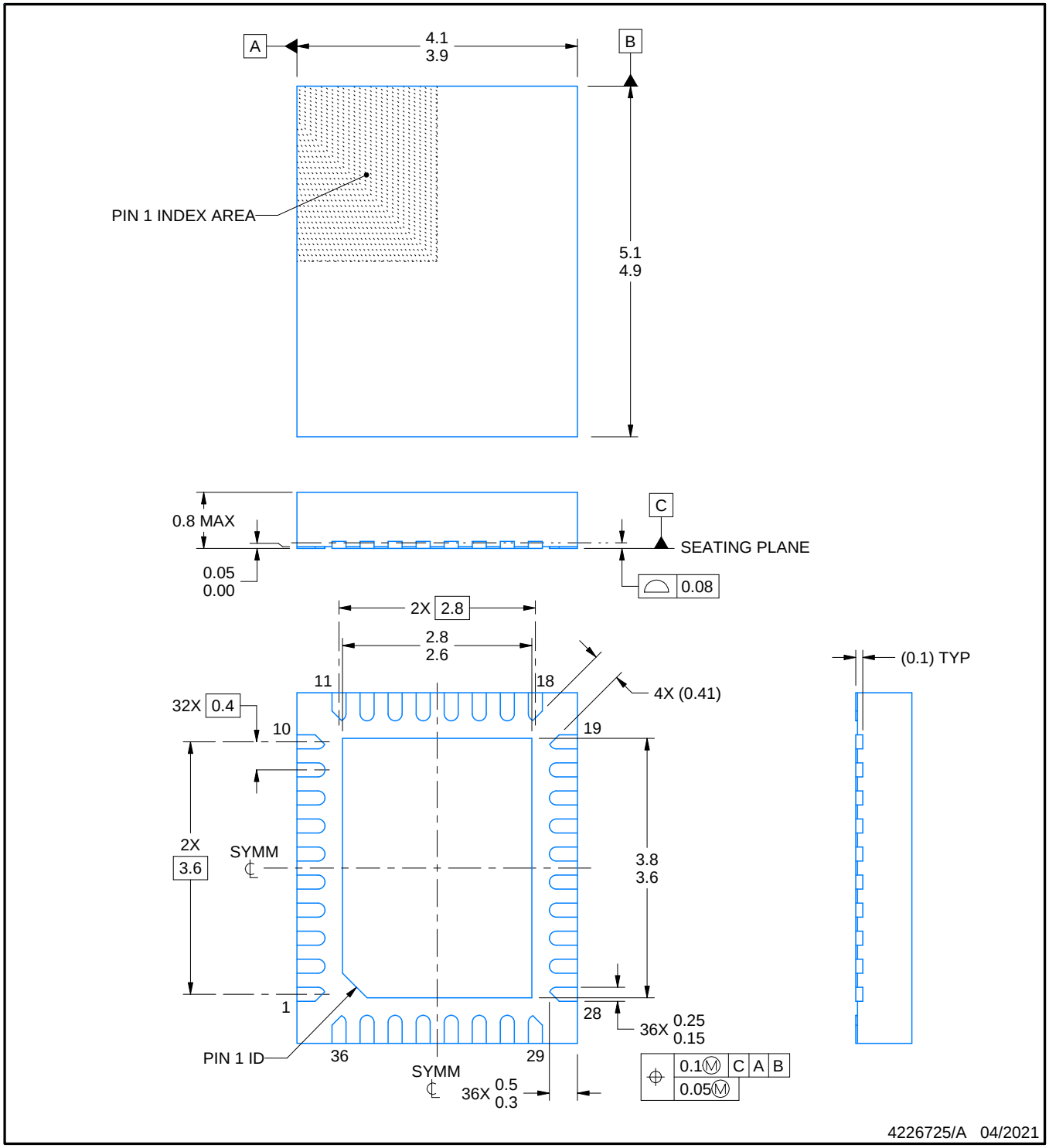
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCT8329A1IREER	WQFN	REE	36	5000	367.0	367.0	35.0

REE0036A

PACKAGE OUTLINE

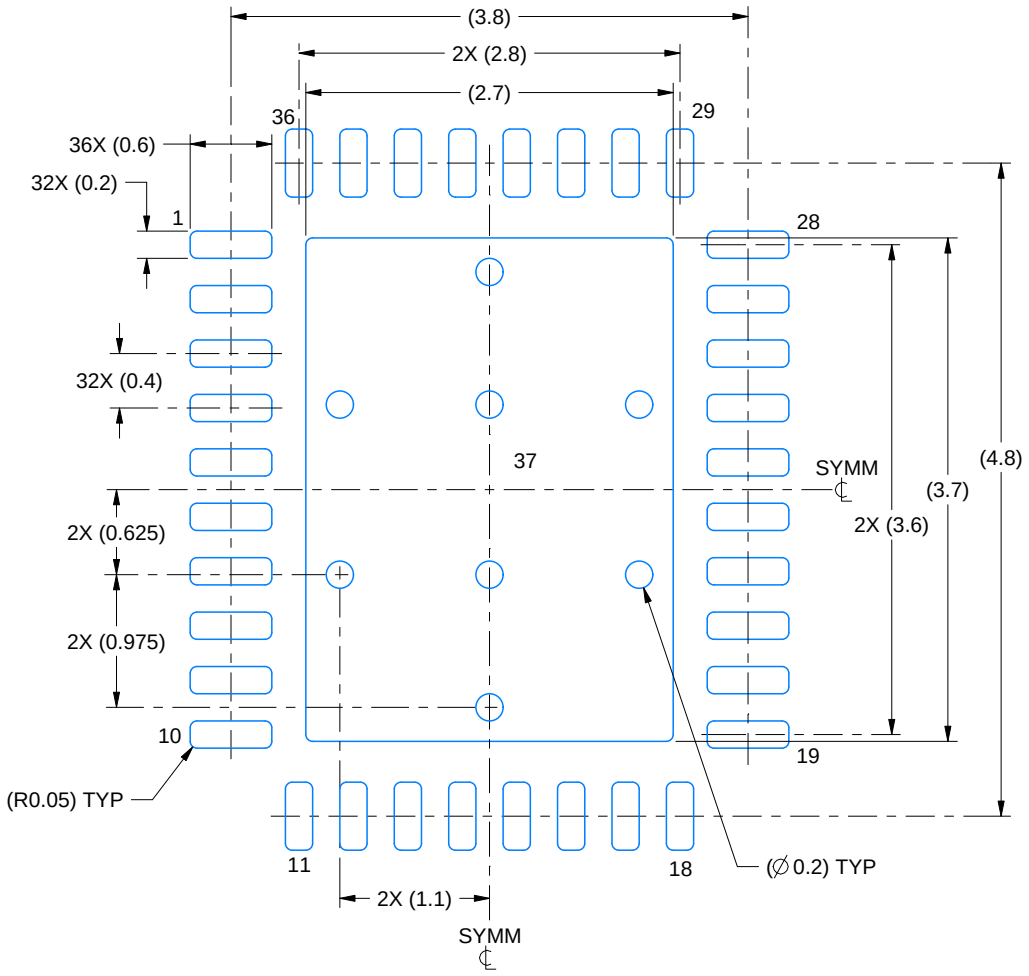
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

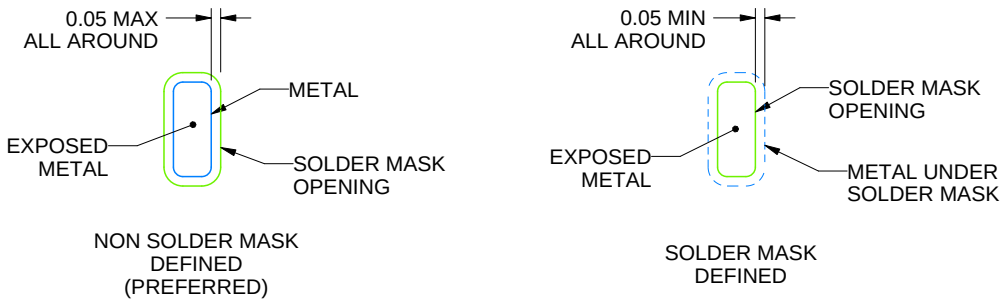


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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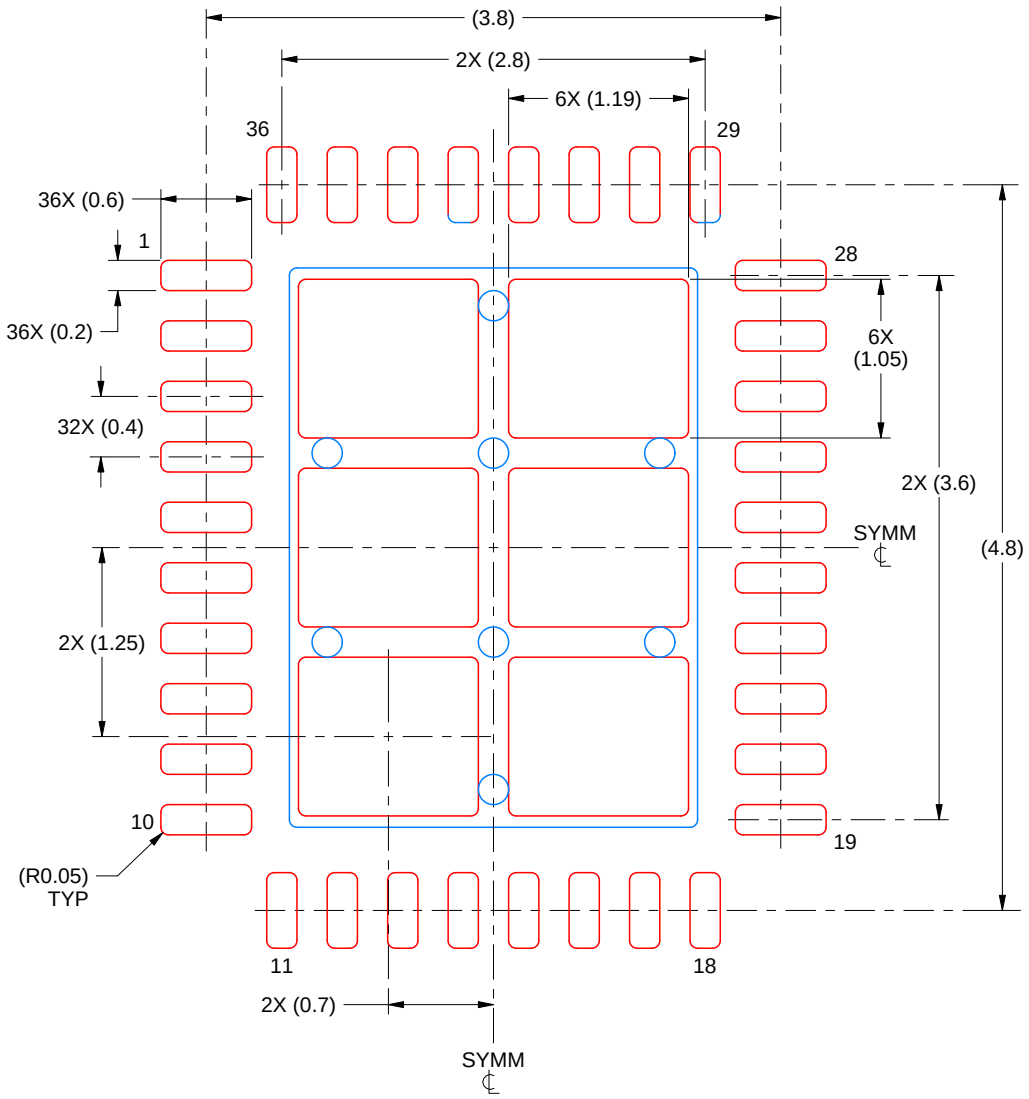
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025