

MUX36xxx 36-V, Low-Capacitance, Low-Leakage-Current, Precision Analog Multiplexers

1 Features

- Low on-capacitance
 - MUX36S16: 13.5 pF
 - MUX36D08: 8.7 pF
- Low input leakage: 1 pA
- Low charge injection: 0.31 pC
- Rail-to-rail operation
- Wide supply range: ± 5 V to ± 18 V, 10 V to 36 V
- Low on-resistance: 125 Ω
- Transition time: 97 ns
- Break-before-make switching action
- EN Pin connectable to V_{DD}
- Logic levels: 2 V to V_{DD}
- Low supply current: 45 μ A
- ESD protection HBM: 2000 V
- Industry-standard TSSOP/ SOIC package and smaller WQFN package options

2 Applications

- [Factory automation and industrial process control](#)
- [Programmable logic controllers \(PLC\)](#)
- [Analog input modules](#)
- ATE Test equipment
- [Digital multimeters](#)
- [Battery monitoring systems](#)

3 Description

The MUX36S16 and MUX36D08 (MUX36xxx) are modern complementary metal-oxide semiconductor (CMOS) precision analog multiplexers (muxes). The MUX36S16 offers 16:1 single-ended channels, whereas the MUX36D08 offers differential 8:1 or dual 8:1 single-ended channels. The MUX36S16 and MUX36D08 work equally well with either dual supplies (± 5 V to ± 18 V) or a single supply (10 V to 36 V). These devices also perform well with symmetric supplies (such as $V_{DD} = 12$ V, $V_{SS} = -12$ V), and unsymmetric supplies (such as $V_{DD} = 12$ V, $V_{SS} = -5$ V). All digital inputs have transistor-transistor logic (TTL) compatible thresholds, providing both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

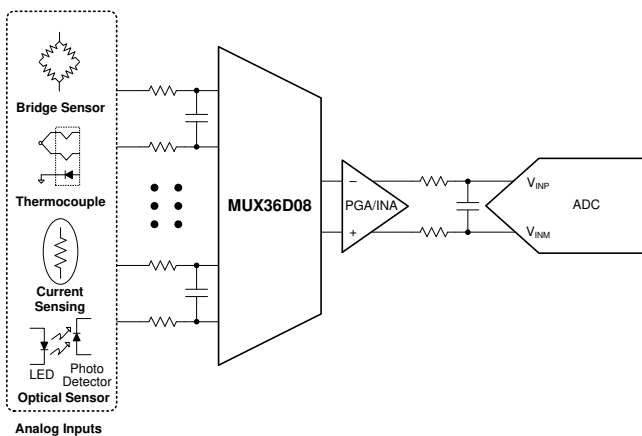
The MUX36S16 and MUX36D08 have very low on- and off-leakage currents, allowing these multiplexers to switch signals from high input impedance sources with minimal error. A low supply current of 45 μ A enables use in power-sensitive applications.

Device Information⁽¹⁾

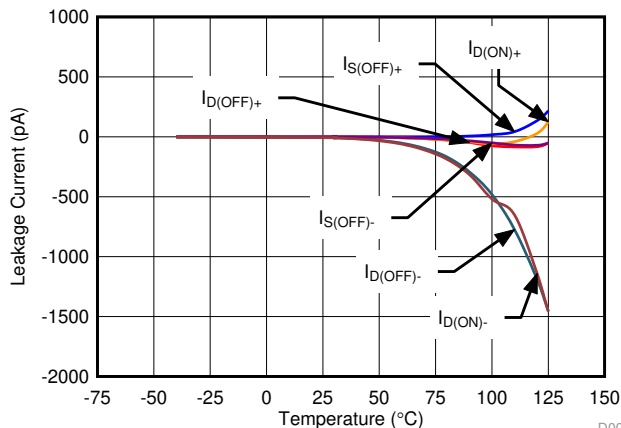
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------------|-----------------|-------------------|
| MUX36S16 MUX36D08 | TSSOP (28) | 9.70 mm x 6.40 mm |
| | SOIC (28) | 17.9 mm x 7.50 mm |
| | WQFN (RTV) (32) | 5.00 mm x 5.00 mm |
| | WQFN (RSN) (32) | 4.00 mm x 4.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic



Leakage Current vs Temperature



D006



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4 Revision History

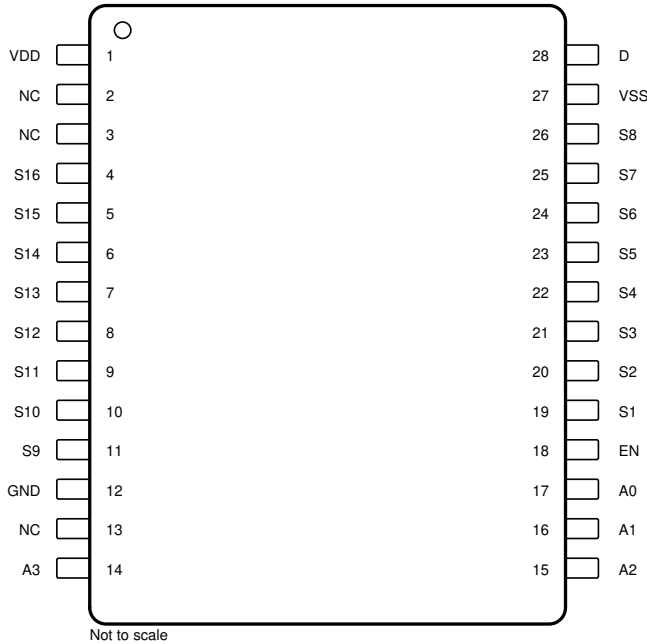
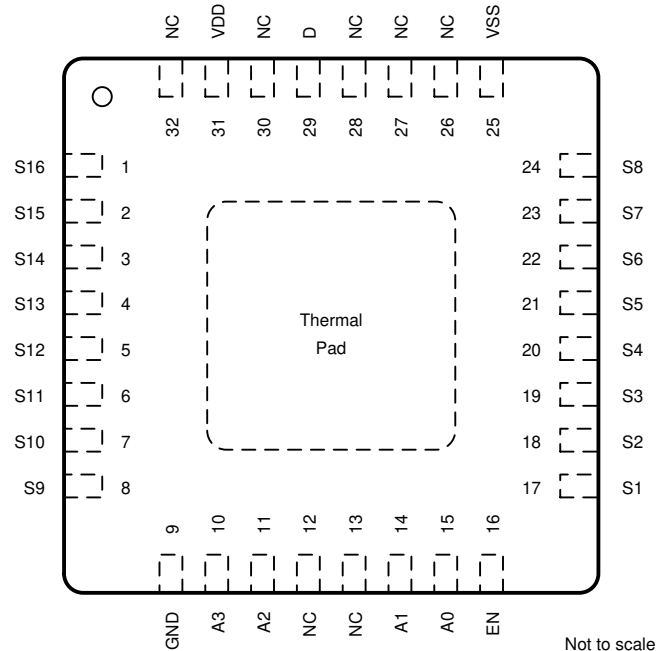
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (April 2018) to Revision C | Page |
|--|------|
| • Added BW, THD+N, and C_{IN} rows to the <i>Electrical Characteristics: Dual Supply</i> | 9 |
| • Changed V_{DD} and V_{SS} supply current MAX values for $\pm 15V$ supplies in <i>Electrical Characteristics: Dual Supply</i> | 9 |
| • Changed V_{DD} and V_{SS} supply current MAX values for 12V supplies in <i>Electrical Characteristics: Single Supply</i> | 11 |

| Changes from Revision A (November 2017) to Revision B | Page |
|--|------|
| • Added WQFN Package option in Features | 1 |
| • Added Added WQFN package option in <i>Device Information</i> | 1 |
| • Added pinout information for WQFN packages | 3 |
| • Added data for WQFN packages to <i>Thermal Information</i> | 8 |

| Changes from Original (November 2016) to Revision A | Page |
|--|------|
| • Changed Transition Time From: 85 ns To: 97ns (Typ) in the <i>Features</i> list..... | 1 |
| • Added SOIC packages to <i>Feature</i> and <i>Device Information</i> | 1 |
| • Added the DW (SOIC) package to the <i>Pin Configuration and Functions</i> section | 3 |
| • Added SOIC package to the <i>Thermal Information</i> table | 8 |
| • Changed Transition time Typ value From 85: ns To: 97ns for $\pm 15 V$ supplies in the <i>Electrical Characteristics: Dual Supply</i> table..... | 9 |
| • Added additional specifications for the SOIC packages (Q_J , Off-isolation, and channel-to-channel crosstalk) for $\pm 15 V$ supplies in <i>Electrical Characteristics: Dual Supply</i> | 9 |
| • Changed Transition time Typ value From: 91 To: 102 ns for 12 V supply in the <i>Electrical Characteristics: Single Supply</i> table | 11 |
| • Added additional specifications for the SOIC packages (Q_J , Off-isolation, and channel-to-channel crosstalk) for 12 V supply in <i>Electrical Characteristics: Single Supply</i> | 11 |

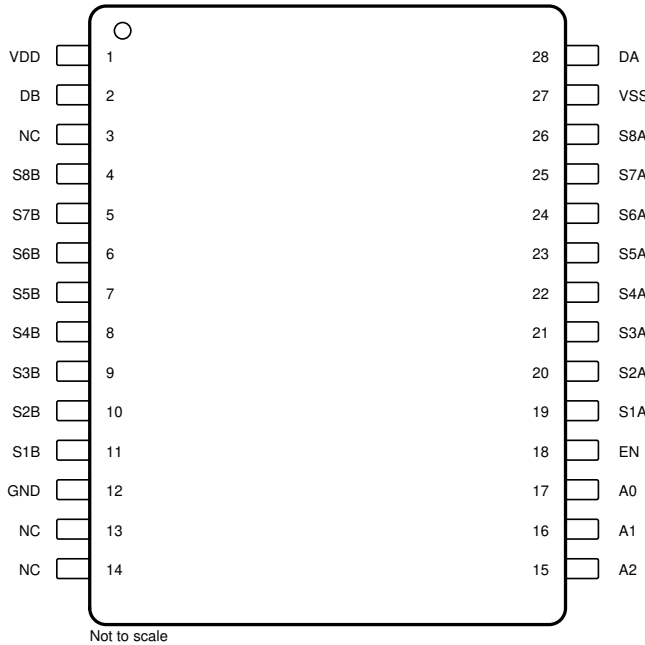
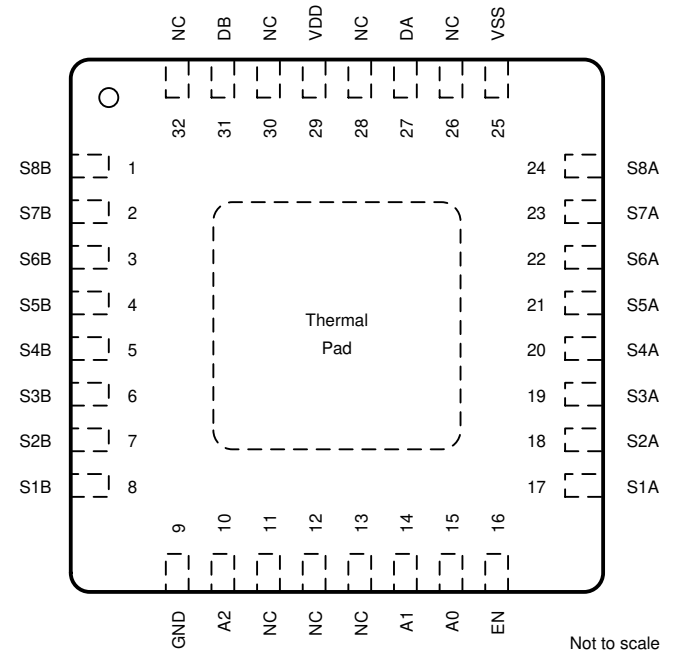
5 Pin Configuration and Functions

**MUX36S16: DW and PW Package
28-Pin SOIC and TSSOP
Top View**

**MUX36S16: RTV and RSN Package
32-Pin WQFN
Top View**

Pin Functions, MUX36S16

| PIN | | FUNCTION | DESCRIPTION |
|------|----------------|-------------------------------------|--|
| NAME | TSSOP/ SOIC | | |
| A0 | 17 | 15 | Digital input Address line 0 |
| A1 | 16 | 14 | Digital input Address line 1 |
| A2 | 15 | 11 | Digital input Address line 2 |
| A3 | 14 | 10 | Digital input Address line 3 |
| D | 28 | 29 | Analog input or output Drain pin. Can be an input or output. |
| EN | 18 | 16 | Digital input Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[3:0] logic inputs determine which switch is turned on. |
| GND | 12 | 9 | Power supply Ground (0 V) reference |
| NC | 2, 3, 13 | 12, 13, 26, 27, 28, 30, 32 | No connect Do not connect |
| S1 | 19 | 17 | Analog input or output Source pin 1. Can be an input or output. |
| S2 | 20 | 18 | Analog input or output Source pin 2. Can be an input or output. |
| S3 | 21 | 19 | Analog input or output Source pin 3. Can be an input or output. |
| S4 | 22 | 20 | Analog input or output Source pin 4. Can be an input or output. |
| S5 | 23 | 21 | Analog input or output Source pin 5. Can be an input or output. |
| S6 | 24 | 22 | Analog input or output Source pin 6. Can be an input or output. |
| S7 | 25 | 23 | Analog input or output Source pin 7. Can be an input or output. |
| S8 | 26 | 24 | Analog input or output Source pin 8. Can be an input or output. |
| S9 | 11 | 8 | Analog input or output Source pin 9. Can be an input or output. |
| S10 | 10 | 7 | Analog input or output Source pin 10. Can be an input or output. |

Pin Functions, MUX36S16 (continued)

| PIN | | | FUNCTION | DESCRIPTION |
|------|----------------|------|------------------------|--|
| NAME | TSSOP/ SOIC | WQFN | | |
| S11 | 9 | 6 | Analog input or output | Source pin 11. Can be an input or output. |
| S12 | 8 | 5 | Analog input or output | Source pin 12. Can be an input or output. |
| S13 | 7 | 4 | Analog input or output | Source pin 13. Can be an input or output. |
| S14 | 6 | 3 | Analog input or output | Source pin 14. Can be an input or output. |
| S15 | 5 | 2 | Analog input or output | Source pin 15. Can be an input or output. |
| S16 | 4 | 1 | Analog input or output | Source pin 16. Can be an input or output. |
| VDD | 1 | 31 | Power supply | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V_{DD} and GND. |
| VSS | 27 | 25 | Power supply | Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V_{SS} and GND. |

**MUX36D08: DW and PW Package
28-Pin SOIC and TSSOP
Top View**

**MUX36D08: RTV and RSN Package
32-Pin WQFN
Top View**

Pin Functions: MUX36D08

| NAME | PIN | | FUNCTION | DESCRIPTION |
|------|----------------|----------------------------|------------------------|---|
| | TSSOP/ SOIC | WQFN | | |
| A0 | 17 | 15 | Digital input | Address line 0 |
| A1 | 16 | 14 | Digital input | Address line 1 |
| A2 | 15 | 10 | Digital input | Address line 2 |
| DA | 28 | 27 | Analog input or output | Drain pin A. Can be an input or output. |
| DB | 2 | 31 | Analog input or output | Drain pin B. Can be an input or output. |
| EN | 18 | 16 | Digital input | Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] logic inputs determine which pair of switches is turned on. |
| GND | 12 | 9 | Power supply | Ground (0 V) reference |
| NC | 3, 13, 14 | 11, 12, 13, 26, 28, 30, 32 | No connect | Do not connect |
| S1A | 19 | 17 | Analog input or output | Source pin 1A. Can be an input or output. |
| S2A | 20 | 18 | Analog input or output | Source pin 2A. Can be an input or output. |
| S3A | 21 | 19 | Analog input or output | Source pin 3A. Can be an input or output. |
| S4A | 22 | 20 | Analog input or output | Source pin 4A. Can be an input or output. |
| S5A | 23 | 21 | Analog input or output | Source pin 5A. Can be an input or output. |
| S6A | 24 | 22 | Analog input or output | Source pin 6A. Can be an input or output. |
| S7A | 25 | 23 | Analog input or output | Source pin 7A. Can be an input or output. |
| S8A | 26 | 24 | Analog input or output | Source pin 8A. Can be an input or output. |
| S1B | 11 | 8 | Analog input or output | Source pin 1B. Can be an input or output. |
| S2B | 10 | 7 | Analog input or output | Source pin 2B. Can be an input or output. |
| S3B | 9 | 6 | Analog input or output | Source pin 3B. Can be an input or output. |

Pin Functions: MUX36D08 (continued)

| PIN | | | FUNCTION | DESCRIPTION |
|------|----------------|------|------------------------|--|
| NAME | TSSOP/ SOIC | WQFN | | |
| S4B | 8 | 5 | Analog input or output | Source pin 4B. Can be an input or output. |
| S5B | 7 | 4 | Analog input or output | Source pin 5B. Can be an input or output. |
| S6B | 6 | 3 | Analog input or output | Source pin 6B. Can be an input or output. |
| S7B | 5 | 2 | Analog input or output | Source pin 7B. Can be an input or output. |
| S8B | 4 | 1 | Analog input or output | Source pin 8B. Can be an input or output. |
| VDD | 1 | 29 | Power supply | Positive power supply. This pin is the most positive power supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V_{DD} and GND. |
| VSS | 27 | 25 | Power supply | Negative power supply. This pin is the most negative power supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V_{SS} and GND. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------------|--|-------------------|----------------|------|---|
| Voltage | Supply | V_{DD} | -0.3 | 40 | V |
| | | V_{SS} | -40 | 0.3 | |
| | | $V_{DD} - V_{SS}$ | | 40 | |
| | Digital pins ⁽²⁾ : EN, A0, A1, A2, A3 | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | | |
| | Analog pins ⁽²⁾ : Sx, SxA, SxB, D, DA, DB | $V_{SS} - 2$ | $V_{DD} + 2$ | | |
| Current ⁽³⁾ | | -30 | 30 | mA | |
| Temperature | Operating, T_A | -55 | 150 | °C | |
| | Junction, T_J | | 150 | | |
| | Storage, T_{stg} | -65 | 150 | | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage limits are valid if current is limited to ± 30 mA.

(3) Only one pin at a time.

6.2 ESD Ratings

| | | VALUE | UNIT | |
|-------------|-------------------------|--|------|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|-------------------------|--|---------------|-----|----------|------|
| V_{DD} ⁽¹⁾ | Positive power-supply voltage | Dual supply | 5 | 18 | V |
| | | Single supply | 10 | 36 | |
| V_{SS} ⁽²⁾ | Negative power-supply voltage (dual supply) | -5 | | -18 | V |
| $V_{DD} - V_{SS}$ | Supply voltage | 10 | | 36 | V |
| V_S | Source pins voltage ⁽³⁾ | V_{SS} | | V_{DD} | V |
| V_D | Drain pins voltage | V_{SS} | | V_{DD} | V |
| V_{EN} | Enable pin voltage | V_{SS} | | V_{DD} | V |
| V_A | Address pins voltage | V_{SS} | | V_{DD} | V |
| I_{CH} | Channel current ($T_A = 25^\circ\text{C}$) | -25 | | 25 | mA |
| T_A | Operating temperature | -40 | | 125 | °C |

(1) When $V_{SS} = 0$ V, V_{DD} can range from 10 V to 36 V.

(2) V_{DD} and V_{SS} can be any value as long as $10 \text{ V} \leq (V_{DD} - V_{SS}) \leq 36 \text{ V}$.

(3) V_S is the voltage on all the S pins.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | MUX36S16/ MUX36D08 | | | | UNIT |
|-------------------------------|--|--------------------|--------------|---------------|---------------|------|
| | | PW (TSSOP) | DW (SOIC) | RTV (WQFN) | RSN (WQFN) | |
| | | 28 PINS | 28 PINS | 32 PINS | 32 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 79.8 | 53.6 | 33.0 | 33.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 24.0 | 30.1 | 20.8 | 26.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 37.6 | 28.5 | 13.9 | 13.4 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 1.2 | 9.0 | 0.3 | 0.3 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 37.1 | 28.4 | 13.8 | 13.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | 4.1 | 4.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics: Dual Supply

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|---|--|----------------------------------|-----------------|-------|-----------------|------|
| ANALOG SWITCH | | | | | | | |
| Analog signal range | | T _A = -40°C to +125°C | | V _{SS} | | V _{DD} | V |
| R _{ON} | On-resistance | V _S = 0 V, I _S = -1 mA | | | 125 | 170 | Ω |
| | | V _S = ±10 V, I _S = -1 mA | T _A = -40°C to +85°C | | 145 | 200 | |
| | | | T _A = -40°C to +125°C | | | 230 | |
| ΔR _{ON} | On-resistance mismatch between channels | V _S = ±10 V, I _S = -1 mA | | | 6 | 9 | Ω |
| | | T _A = -40°C to +85°C | | | | 14 | |
| R _{FLAT} | On-resistance flatness | V _S = 10 V, 0 V, -10 V | | | 20 | 45 | Ω |
| | | T _A = -40°C to +85°C | | | | 53 | |
| | | T _A = -40°C to +125°C | | | | 58 | |
| On-resistance drift | | V _S = 0 V | | | 0.62 | | Ω/°C |
| I _{S(OFF)} | Input leakage current | Switch state is off, V _S = ±10 V, V _D = ±10 V ⁽¹⁾ | | -0.04 | 0.001 | 0.04 | nA |
| | | T _A = -40°C to +85°C | | -0.15 | | 0.15 | |
| | | T _A = -40°C to +125°C | | -1.2 | | 1.2 | |
| I _{D(OFF)} | Output off-leakage current | Switch state is off, V _S = ±10 V, V _D = ±10 V ⁽¹⁾ | | -0.15 | 0.01 | 0.15 | nA |
| | | T _A = -40°C to +85°C | | -1 | | 1 | |
| | | T _A = -40°C to +125°C | | -4.5 | | 4.5 | |
| I _{D(ON)} | Output on-leakage current | Switch state is on, V _D = ±10 V, V _S = floating | | -0.2 | 0.01 | 0.2 | nA |
| | | T _A = -40°C to +85°C | | -1 | | 1 | |
| | | T _A = -40°C to +125°C | | -5.3 | | 5.3 | |
| I _{DL(ON)} | Differential on-leakage current | Switch state is on, V _{DA} = V _{DB} = ±10 V, V _S = floating | | -15 | 3 | 15 | pA |
| | | T _A = -40°C to +85°C | | -100 | | 100 | |
| | | T _A = -40°C to +125°C | | -500 | | 500 | |
| LOGIC INPUT | | | | | | | |
| V _{IH} | Logic voltage high | | | 2 | | | V |
| V _{IL} | Logic voltage low | | | | | 0.8 | V |
| I _D | Input current | | | | | 0.1 | μA |

(1) When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics: Dual Supply (continued)

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|--|---------------|-----------|------|---------------|
| SWITCH DYNAMICS⁽²⁾ | | | | | | | |
| t_{ON} | Enable turn-on time | $V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | 82 | 136 | ns |
| | | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 145 | |
| | | | | | | 151 | |
| t_{OFF} | Enable turn-off time | $V_S = \pm 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | 63 | 78 | ns |
| | | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 89 | |
| | | | | | | 97 | |
| t_t | Transition time | $V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | 97 | 143 | ns |
| | | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 151 | |
| | | | | | | 157 | |
| t_{BBM} | Break-before-make time delay | $V_S = 10\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | 30 | 54 | | ns |
| Q_J | Charge injection | $C_L = 1\text{ nF}$, $R_S = 0\ \Omega$ | $V_S = 0\text{ V}$ | TSSOP package | 0.31 | | pC |
| | | | | SOIC package | 0.67 | | |
| | | | $V_S = -15\text{ V to } +15\text{ V}$ | TSSOP package | ± 0.9 | | |
| | | | | SOIC package | ± 1.1 | | |
| Off-isolation | $R_L = 50\ \Omega$, $V_S = 1\text{ V}_{RMS}$, $f = 1\text{ MHz}$ | Nonadjacent channel to D, DA, DB | TSSOP package | -98 | | dB | |
| | | | SOIC package | -94 | | | |
| | | Adjacent channel to D, DA, DB | TSSOP package | -94 | | | |
| | | | SOIC package | -88 | | | |
| Channel-to-channel crosstalk | $R_L = 50\ \Omega$, $V_S = 1\text{ V}_{RMS}$, $f = 1\text{ MHz}$ | Nonadjacent channels | TSSOP package | -100 | | dB | |
| | | | SOIC package | -96 | | | |
| | | Adjacent channels | TSSOP package | -88 | | | |
| | | | SOIC package | -83 | | | |
| BW | -3dB Bandwidth | $V_S = 1\text{ V}_{RMS}$, $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ | MUX36S16 | | 260 | | dB |
| | | | MUX36D08 | | 430 | | |
| THD + N | Total harmonic distortion plus noise | $V_S = 0\text{ V or } V_{DD}$, $R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz to } 20\text{ kHz}$ | | | 0.09% | | |
| C_{IN} | Digital input capacitance | $V_{IN} = 0\text{ V or } V_{DD}$ | | | 1.1 | | pF |
| $C_{S(OFF)}$ | Input off-capacitance | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ | | | 2.1 | 3 | pF |
| $C_{D(OFF)}$ | Output off-capacitance | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ | MUX36S16 | | 11.1 | 12.2 | pF |
| | | | MUX36D08 | | 6.4 | 7.5 | |
| $C_{S(ON)}$, $C_{D(ON)}$ | Output on-capacitance | $f = 1\text{ MHz}$, $V_S = 0\text{ V}$ | MUX36S16 | | 13.5 | 15 | pF |
| | | | MUX36D08 | | 8.7 | 10.2 | |
| POWER SUPPLY | | | | | | | |
| V_{DD} supply current | All $V_A = 0\text{ V or } 3.3\text{ V}$, $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$, | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | 45 | 59 | μA |
| | | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 62 | |
| | | | | | | 69 | |
| V_{SS} supply current | All $V_A = 0\text{ V or } 3.3\text{ V}$, $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$, | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | 26 | 33 | μA |
| | | | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | | | 36 | |
| | | | | | | 43 | |

(2) Specified by design; not subject to production testing.

6.6 Electrical Characteristics: Single Supply

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|---------------------------------|--|---|----------|-------|----------|-------------------------|
| ANALOG SWITCH | | | | | | | |
| Analog signal range | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | V_{SS} | | V_{DD} | V |
| R_{ON} | On-resistance | $V_S = 10\text{ V}$, $I_S = -1\text{ mA}$ | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | 235 | 340 | Ω |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 390 | |
| | | | | | | 430 | |
| ΔR_{ON} | On-resistance match | $V_S = 10\text{ V}$, $I_S = -1\text{ mA}$ | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | 7 | 20 | Ω |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 35 | |
| | | | | | | 40 | |
| On-resistance drift | | $V_S = 10\text{ V}$ | | | 1.07 | | $\Omega/^\circ\text{C}$ |
| $I_{S(OFF)}$ | Input leakage current | Switch state is off, $V_S = 1\text{ V}$ and $V_D = 10\text{ V}$, or $V_S = 10\text{ V}$ and $V_D = 1\text{ V}$ ⁽¹⁾ | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | -0.04 | 0.001 | 0.04 | nA |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | -0.15 | | 0.15 | |
| | | | | -1.2 | | 1.2 | |
| $I_{D(OFF)}$ | Output off leakage current | Switch state is off, $V_S = 1\text{ V}$ and $V_D = 10\text{ V}$, or $V_S = 10\text{ V}$ and $V_D = 1\text{ V}$ ⁽¹⁾ | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | -0.15 | 0.01 | 0.15 | nA |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | -0.75 | | 0.75 | |
| | | | | -2.4 | | 2.4 | |
| $I_{D(ON)}$ | Output on leakage current | Switch state is on, $V_D = 1\text{ V}$ and 10 V , $V_S =$ floating | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | -0.15 | 0.01 | 0.15 | nA |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | -0.75 | | 0.75 | |
| | | | | -2.5 | | 2.5 | |
| $I_{DL(ON)}$ | Differential on-leakage current | Switch state is on, $V_{DA} = V_{DB} = 1\text{ V}$ and 10 V , $V_S =$ floating | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | -15 | 3 | 15 | pA |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | -100 | | 100 | |
| | | | | -500 | | 500 | |
| LOGIC INPUT | | | | | | | |
| V_{IH} | Logic voltage high | | | 2.0 | | | V |
| V_{IL} | Logic voltage low | | | | | 0.8 | V |
| I_D | Input current | | | | | 0.1 | μA |

 (1) When V_S is 1 V, V_D is 10 V, and vice versa.

Electrical Characteristics: Single Supply (continued)

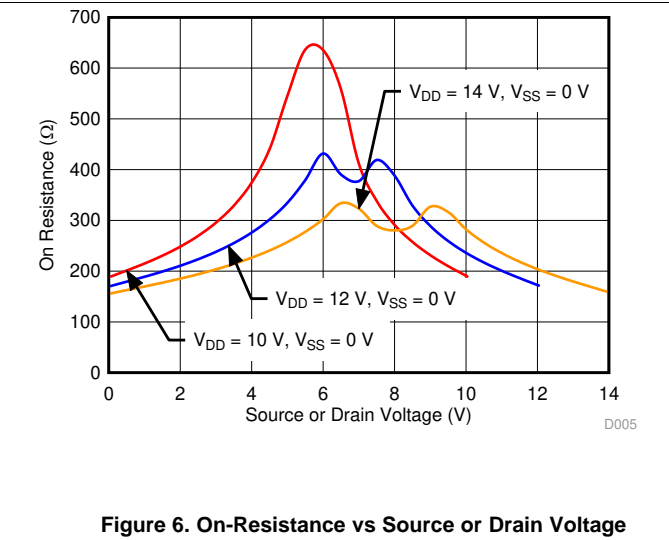
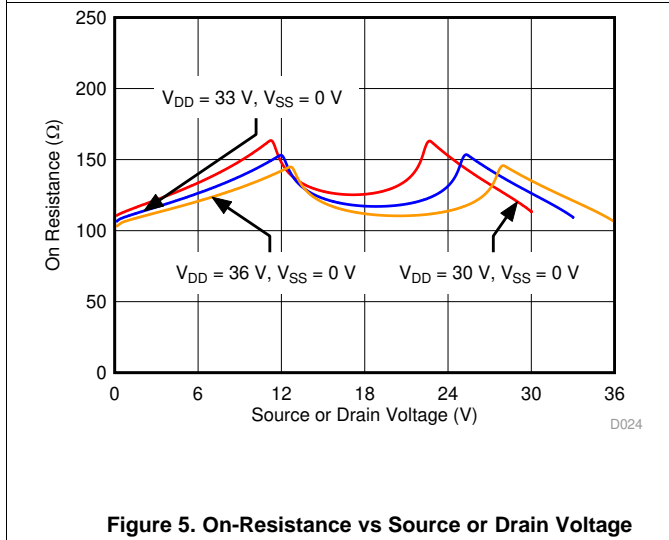
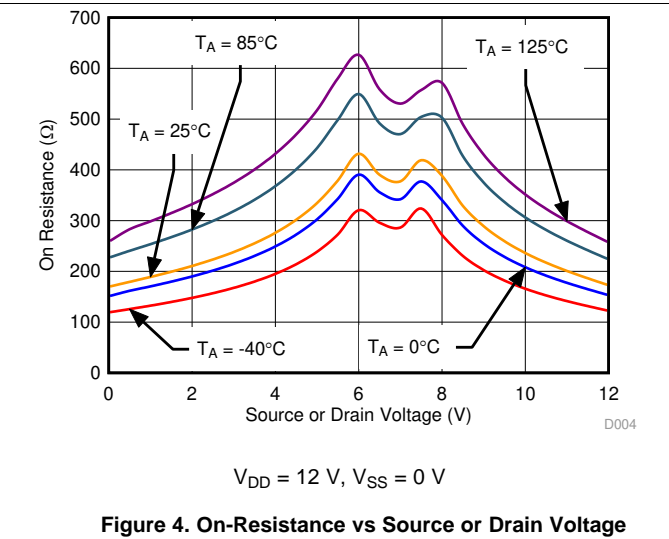
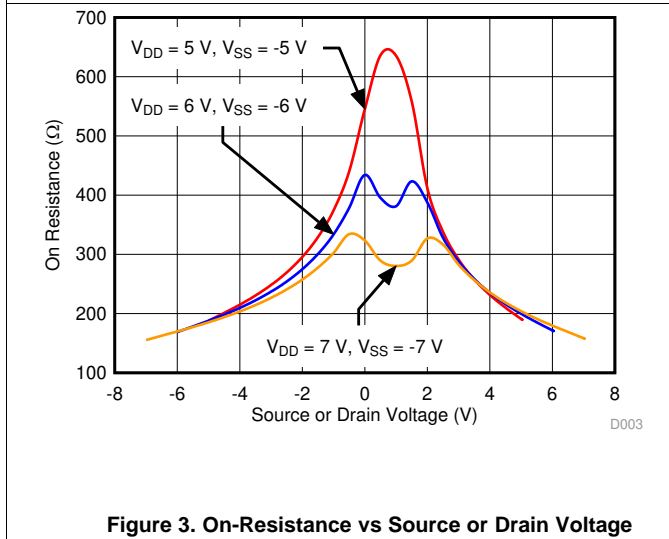
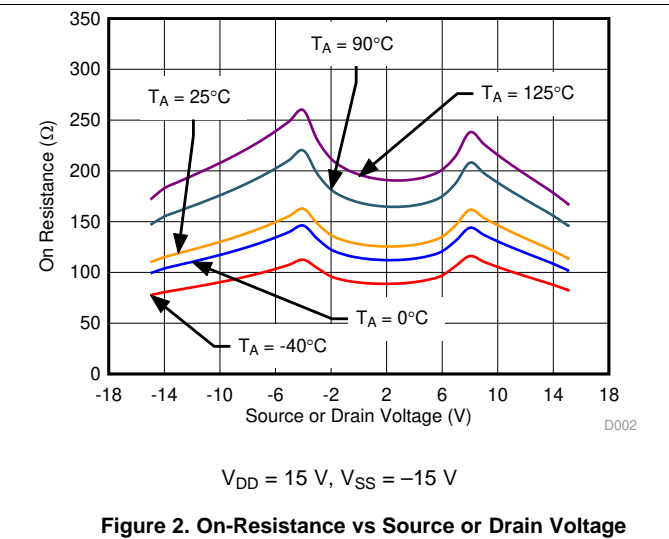
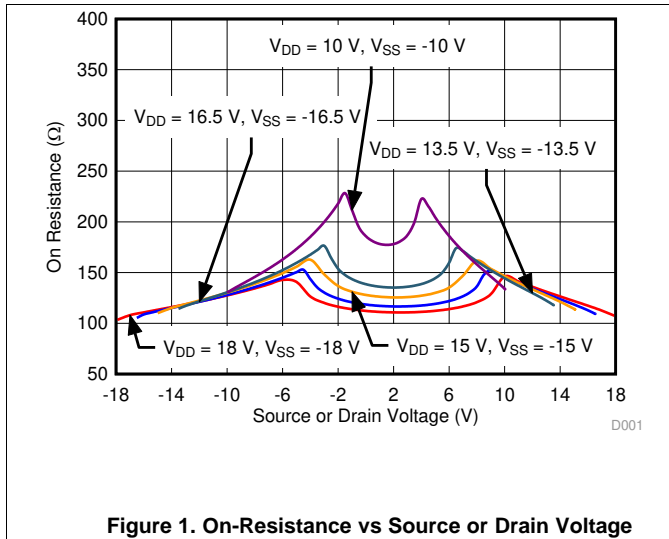
 at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|--|--|---|---------------|------------|------|---------------|
| SWITCH DYNAMIC CHARACTERISTICS⁽²⁾ | | | | | | | |
| t_{ON} | Enable turn-on time | $V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ | | | 90 | 145 | ns |
| | | | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | | 145 | |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 149 | |
| t_{OFF} | Enable turn-off time | $V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ | | | 66 | 84 | ns |
| | | | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | | 94 | |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 102 | |
| t_t | Transition time | $V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, | | | 107 | 147 | ns |
| | | | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | | 153 | |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 155 | |
| t_{BBM} | Break-before-make time delay | $V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 30 | 54 | ns |
| Q_J | Charge injection | $C_L = 1\text{ nF}$, $R_S = 0\ \Omega$ | $V_S = 6\text{ V}$ | TSSOP package | 0.12 | | pC |
| | | | | SOIC package | 0.38 | | |
| | | | $V_S = 0\text{ V}$ to 12 V | TSSOP | ± 0.17 | | |
| | | | | SOIC package | ± 0.48 | | |
| Off-isolation | Nonadjacent channel to D, DA, DB | $R_L = 50\ \Omega$, $V_S = 1\text{ V}_{RMS}$, $f = 1\text{ MHz}$ | Nonadjacent channel to D, DA, DB | TSSOP package | -97 | | dB |
| | | | | SOIC package | -94 | | |
| | | | Adjacent channel to D, DA, DB | TSSOP package | -94 | | |
| | | | | SOIC package | -88 | | |
| Channel-to-channel crosstalk | Nonadjacent channels | $R_L = 50\ \Omega$, $V_S = 1\text{ V}_{RMS}$, $f = 1\text{ MHz}$ | Nonadjacent channels | TSSOP package | -100 | | dB |
| | | | | SOIC package | -99 | | |
| | | | Adjacent channels | TSSOP | -88 | | |
| | | | | SOIC package | -83 | | |
| $C_{S(OFF)}$ | Input off-capacitance | $f = 1\text{ MHz}$, $V_S = 6\text{ V}$ | | | 2.4 | 3.4 | pF |
| $C_{D(OFF)}$ | Output off-capacitance | $f = 1\text{ MHz}$, $V_S = 6\text{ V}$ | MUX36S16 | | 14 | 15.4 | pF |
| | | | MUX36D08 | | 7.8 | 9.1 | |
| $C_{S(ON)}$, $C_{D(ON)}$ | Output on-capacitance | $f = 1\text{ MHz}$, $V_S = 6\text{ V}$ | MUX36S16 | | 16.2 | 18 | pF |
| | | | MUX36D08 | | 9.9 | 11.6 | |
| POWER SUPPLY | | | | | | | |
| V_{DD} supply current | All $V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$ | | | | 41 | 59 | μA |
| | | | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | | 56 | |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 62 | |
| V_{SS} supply current | All $V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$ | | | | 22 | 29 | μA |
| | | | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | | | 31 | |
| | | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 37 | |

(2) Specified by design, not subject to production test.

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

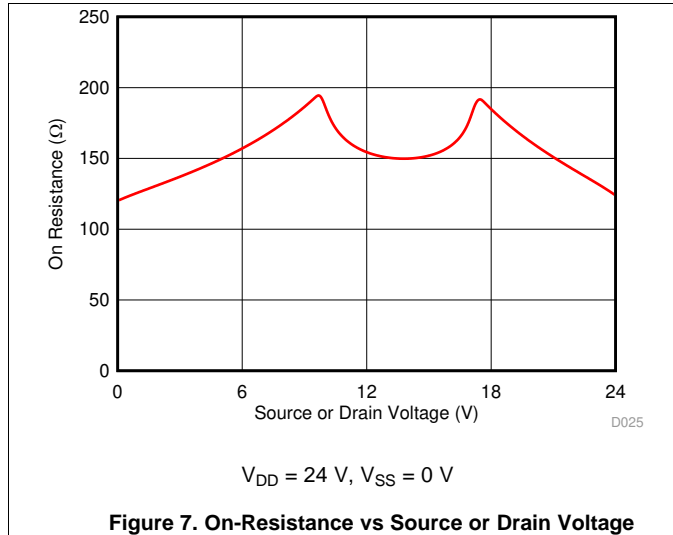


Figure 7. On-Resistance vs Source or Drain Voltage

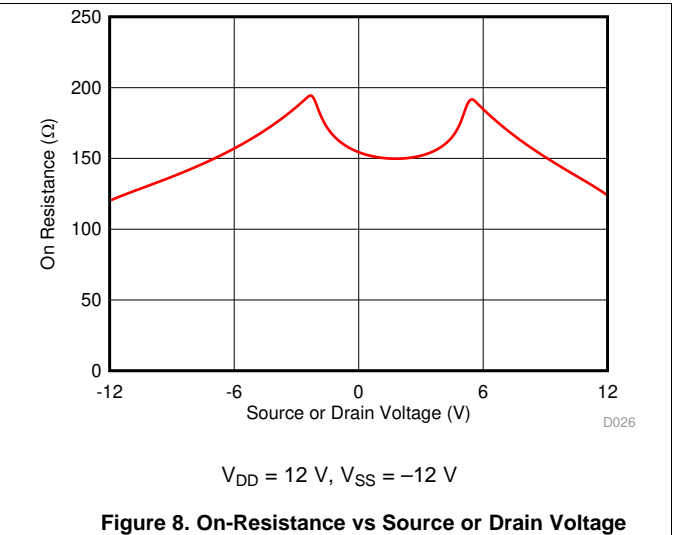


Figure 8. On-Resistance vs Source or Drain Voltage

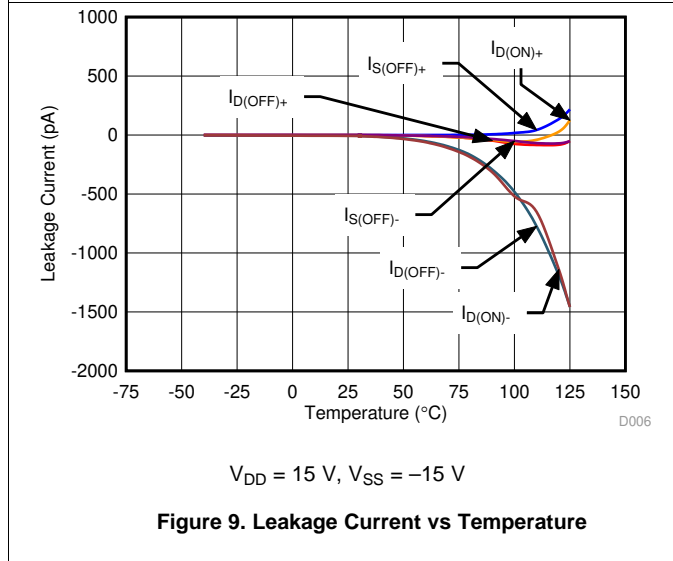


Figure 9. Leakage Current vs Temperature

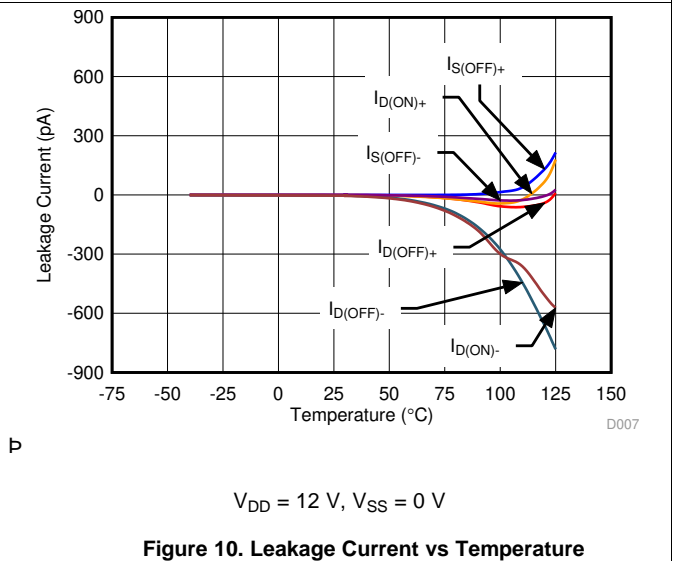


Figure 10. Leakage Current vs Temperature

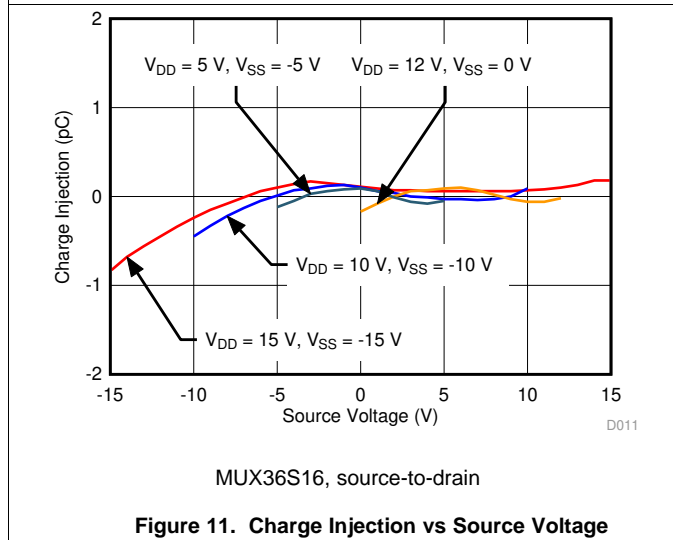


Figure 11. Charge Injection vs Source Voltage

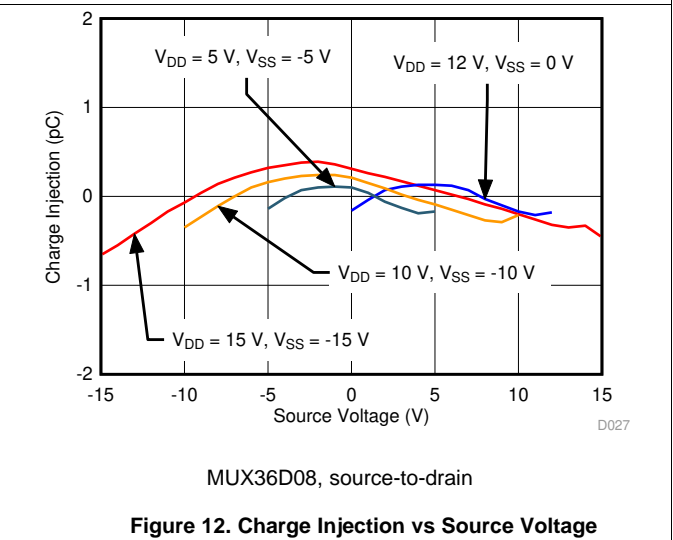


Figure 12. Charge Injection vs Source Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

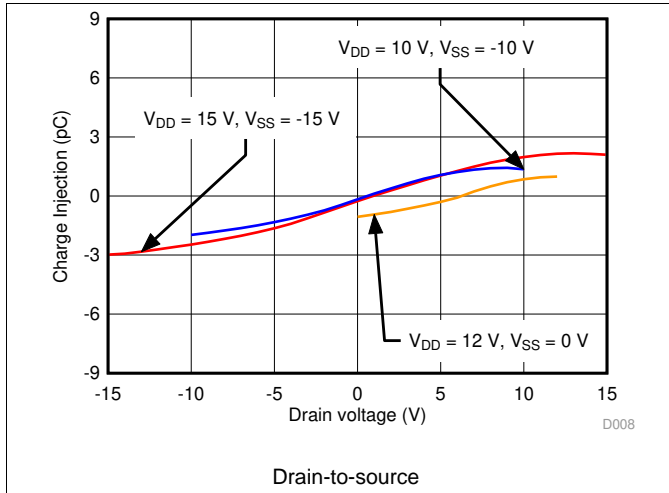


Figure 13. Charge Injection vs Drain Voltage

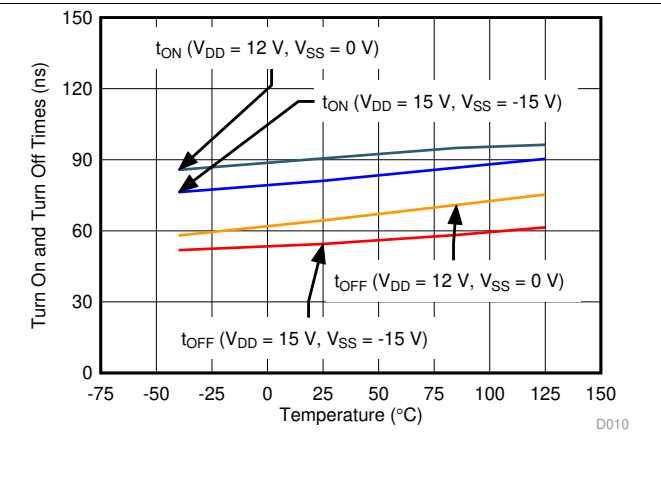


Figure 14. Turn-On and Turn-Off Times vs Temperature

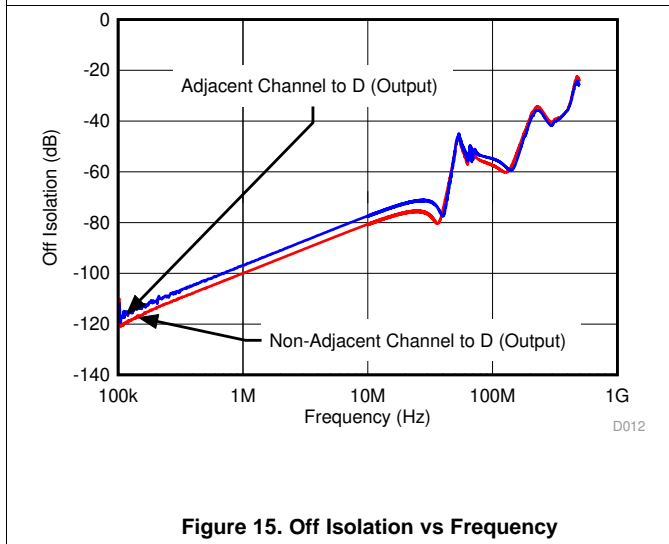


Figure 15. Off Isolation vs Frequency

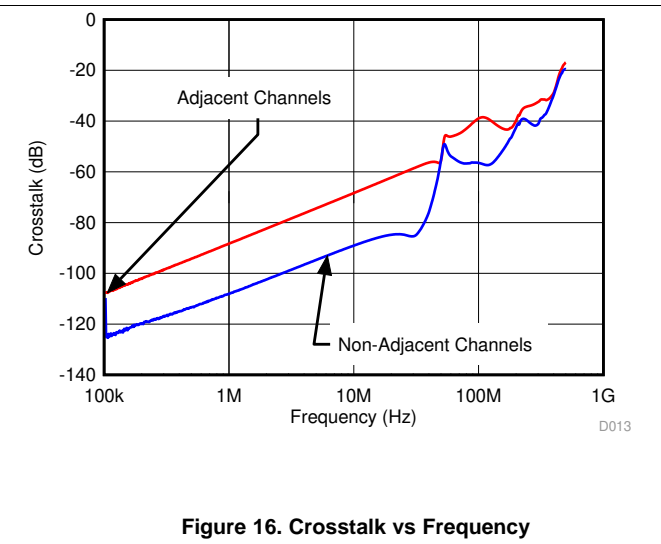


Figure 16. Crosstalk vs Frequency

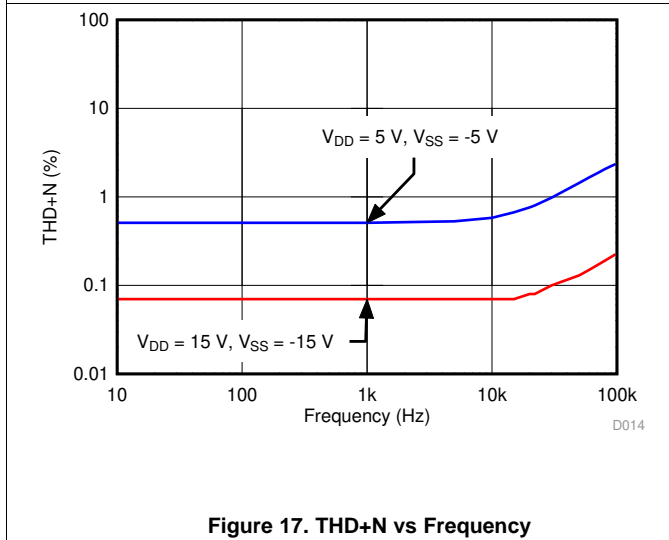


Figure 17. THD+N vs Frequency

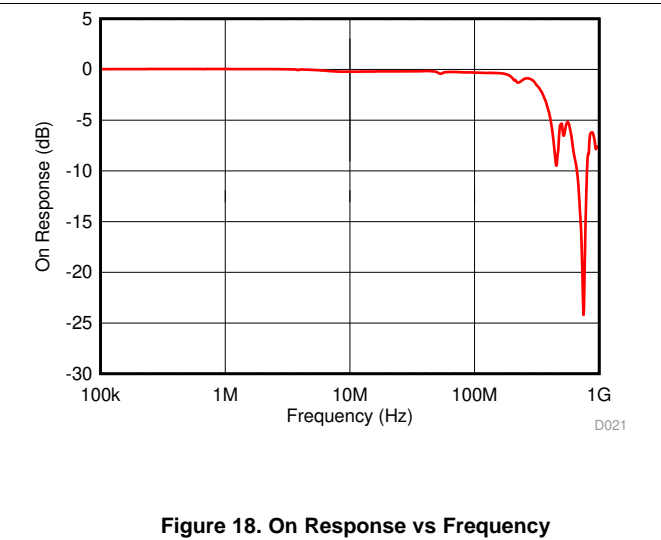
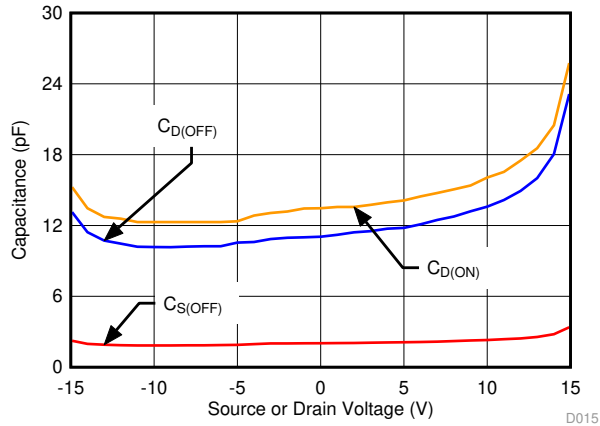


Figure 18. On Response vs Frequency

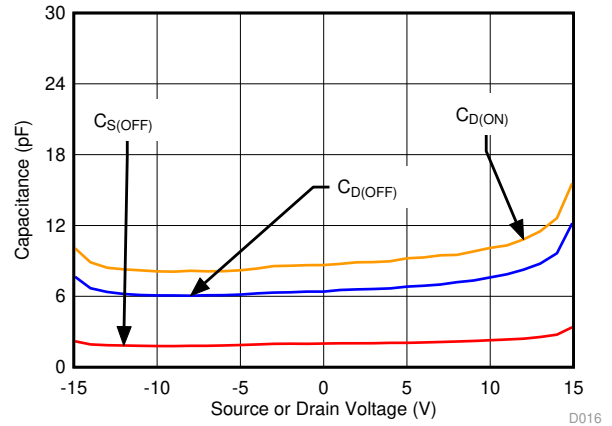
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)



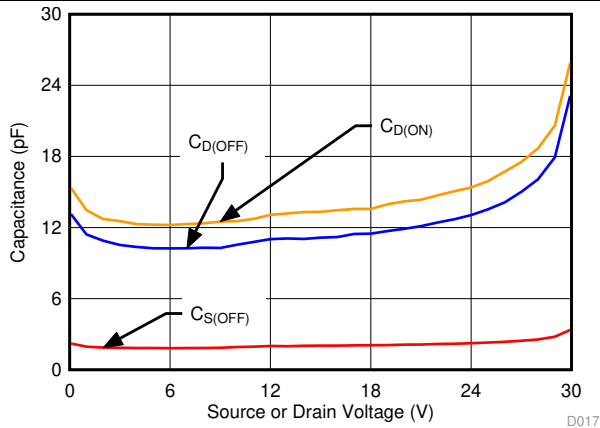
MUX36S16, $V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

Figure 19. Capacitance vs Source Voltage



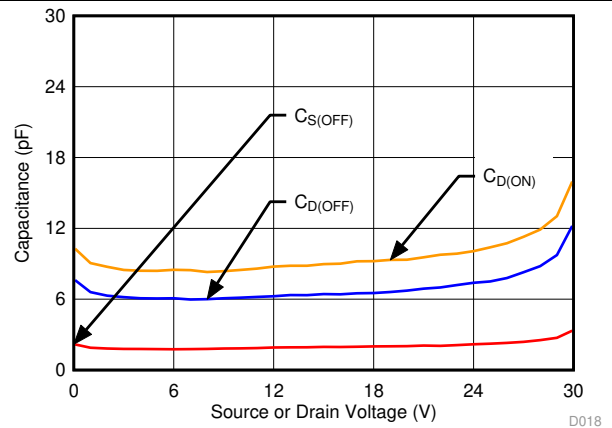
MUX36D08, $V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$

Figure 20. Capacitance vs Source Voltage



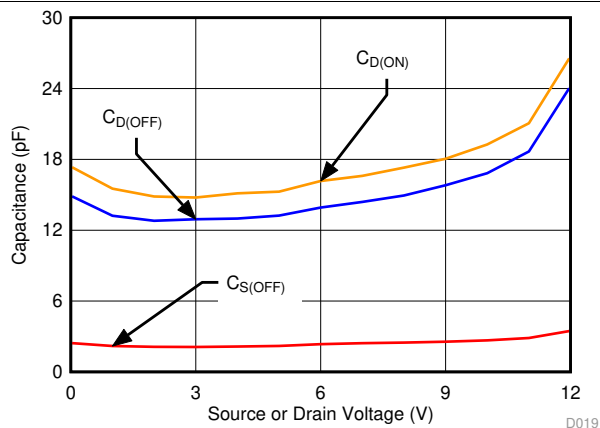
MUX36S16, $V_{DD} = 30\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 21. Capacitance vs Source Voltage



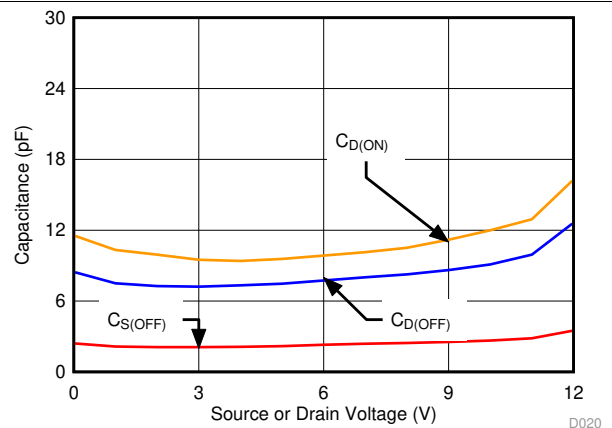
MUX36D08, $V_{DD} = 30\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 22. Capacitance vs Source Voltage



MUX36S16, $V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 23. Capacitance vs Source Voltage



MUX36D08, $V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$

Figure 24. Capacitance vs Source Voltage

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

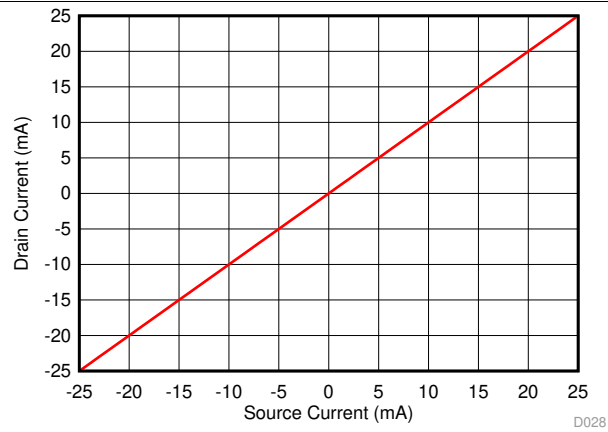


Figure 25. Source Current vs Drain Current

7 Parameter Measurement Information

7.1 Truth Tables

Table 1. MUX36S16

| EN | A3 | A2 | A1 | A0 | ON-CHANNEL |
|----|------------------|------------------|------------------|------------------|----------------------|
| 0 | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽¹⁾ | All channels are off |
| 1 | 0 | 0 | 0 | 0 | Channel 1 |
| 1 | 0 | 0 | 0 | 1 | Channel 2 |
| 1 | 0 | 0 | 1 | 0 | Channel 3 |
| 1 | 0 | 0 | 1 | 1 | Channel 4 |
| 1 | 0 | 1 | 0 | 0 | Channel 5 |
| 1 | 0 | 1 | 0 | 1 | Channel 6 |
| 1 | 0 | 1 | 1 | 0 | Channel 7 |
| 1 | 0 | 1 | 1 | 1 | Channel 8 |
| 1 | 1 | 0 | 0 | 0 | Channel 9 |
| 1 | 1 | 0 | 0 | 1 | Channel 10 |
| 1 | 1 | 0 | 1 | 0 | Channel 11 |
| 1 | 1 | 0 | 1 | 1 | Channel 12 |
| 1 | 1 | 1 | 0 | 0 | Channel 13 |
| 1 | 1 | 1 | 0 | 1 | Channel 14 |
| 1 | 1 | 1 | 1 | 0 | Channel 15 |
| 1 | 1 | 1 | 1 | 1 | Channel 16 |

(1) X denotes *don't care*.

Table 2. MUX36D08

| EN | A2 | A1 | A0 | ON-CHANNEL |
|----|------------------|------------------|------------------|----------------------|
| 0 | X ⁽¹⁾ | X ⁽¹⁾ | X ⁽¹⁾ | All channels are off |
| 1 | 0 | 0 | 0 | Channels 1A and 1B |
| 1 | 0 | 0 | 1 | Channels 2A and 2B |
| 1 | 0 | 1 | 0 | Channels 3A and 3B |
| 1 | 0 | 1 | 1 | Channels 4A and 4B |
| 1 | 1 | 0 | 0 | Channels 5A and 5B |
| 1 | 1 | 0 | 1 | Channels 6A and 6B |
| 1 | 1 | 1 | 0 | Channels 7A and 7B |
| 1 | 1 | 1 | 1 | Channels 8A and 8B |

(1) X denotes *don't care*.

7.1.1 On-Resistance

The on-resistance of the MUX36xxx is the ohmic resistance across the source (Sx, SxA, or SxB) and drain (D, DA, or DB) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 26. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in Equation 1:

$$R_{ON} = V / I_{CH} \quad (1)$$

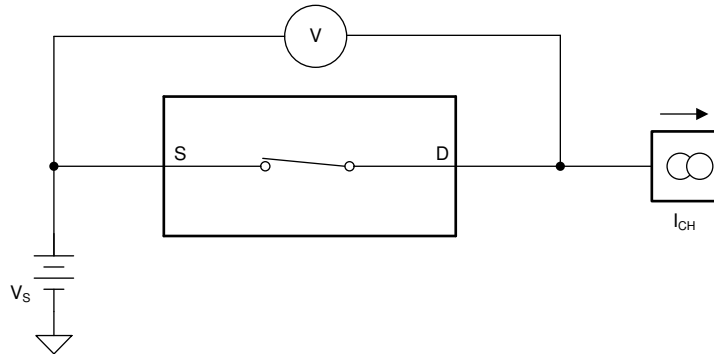


Figure 26. On-Resistance Measurement Setup

7.1.2 Off Leakage

There are two types of leakage currents associated with a switch during the OFF state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 27

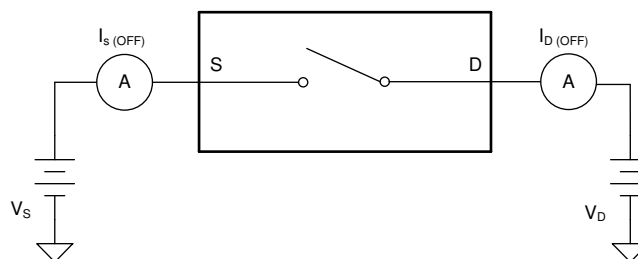


Figure 27. Off-Leakage Measurement Setup

7.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the ON state. The source pin is left floating during the measurement. Figure 28 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

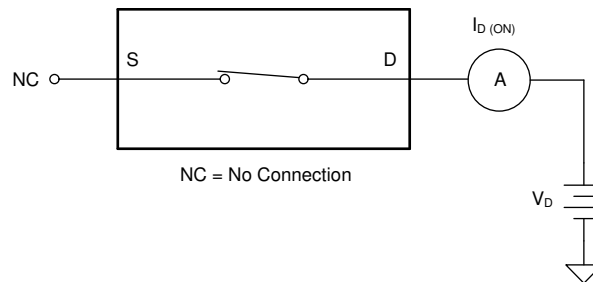


Figure 28. On-Leakage Measurement Setup

7.1.4 Differential On-Leakage Current

In case of a differential signal, the on-leakage current is defined as the differential leakage current that flows into, or out of, the drain pins when the switches are in the ON state. The source pins are left floating during the measurement. Figure 29 shows the circuit used for measuring the on-leakage current on each signal path, denoted by $I_{DA(ON)}$ and $I_{DB(ON)}$. The absolute difference between these two currents is defined as the differential on-leakage current, denoted by $I_{DL(ON)}$.

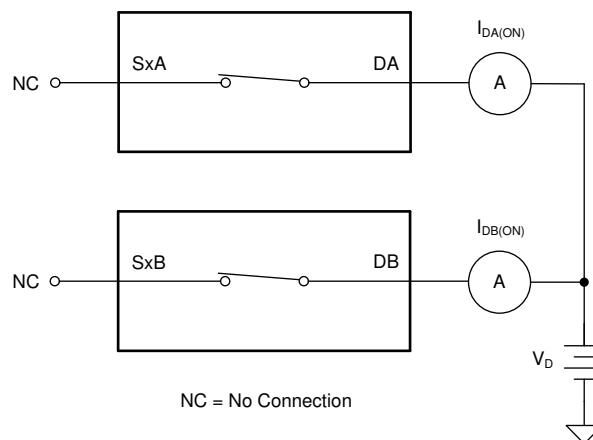


Figure 29. Differential On-Leakage Measurement Setup

7.1.5 Transition Time

Transition time is defined as the time taken by the output of the MUX36xxx to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. Figure 30 shows the setup used to measure transition time, denoted by the symbol t_t .

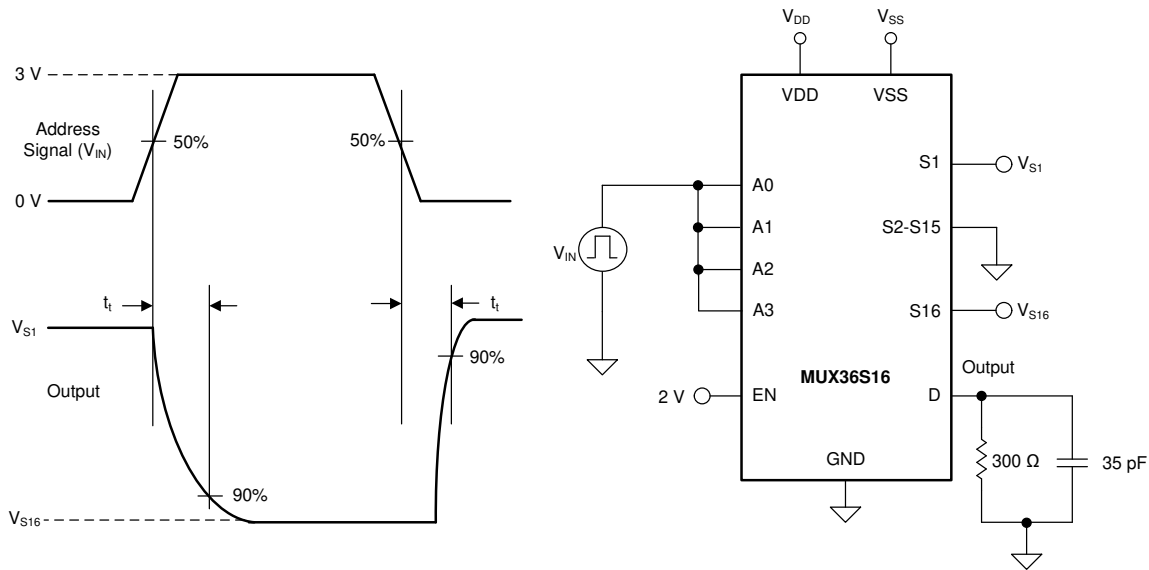


Figure 30. Transition-Time Measurement Setup

7.1.6 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the MUX36xxx is switching. The MUX36xxx output first breaks from the ON-state switch before making the connection with the next ON-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 31 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM} .

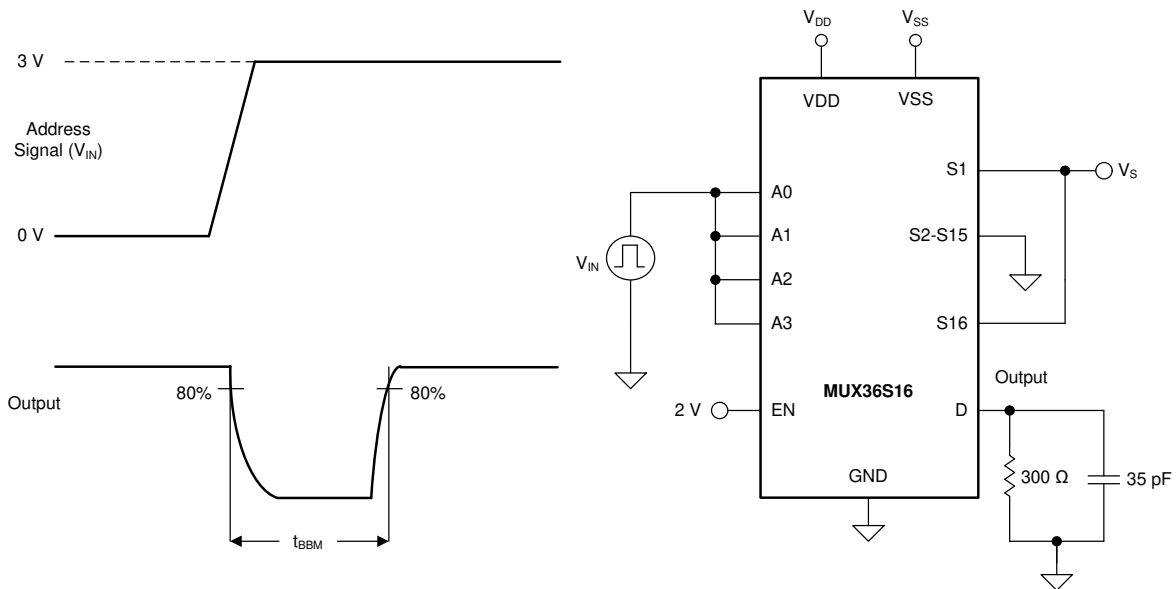


Figure 31. Break-Before-Make Delay Measurement Setup

7.1.7 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the MUX36xxx to rise to 90% final value after the enable signal has risen to 50% final value. Figure 32 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON} .

Turn off time is defined as the time taken by the output of the MUX36xxx to fall to 10% initial value after the enable signal has fallen to 50% initial value. Figure 32 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF} .

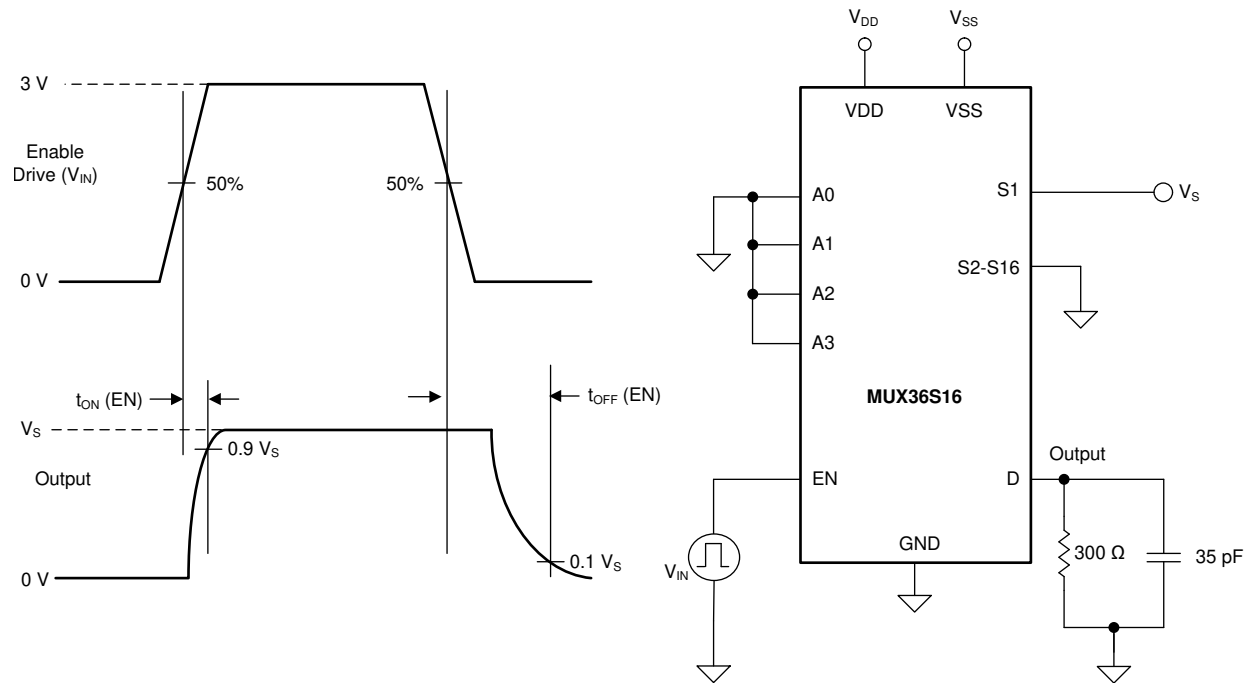


Figure 32. Turn-On and Turn-Off Time Measurement Setup

7.1.8 Charge Injection

The MUX36xxx have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the source or drain of the device during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ} . Figure 33 shows the setup used to measure charge injection.

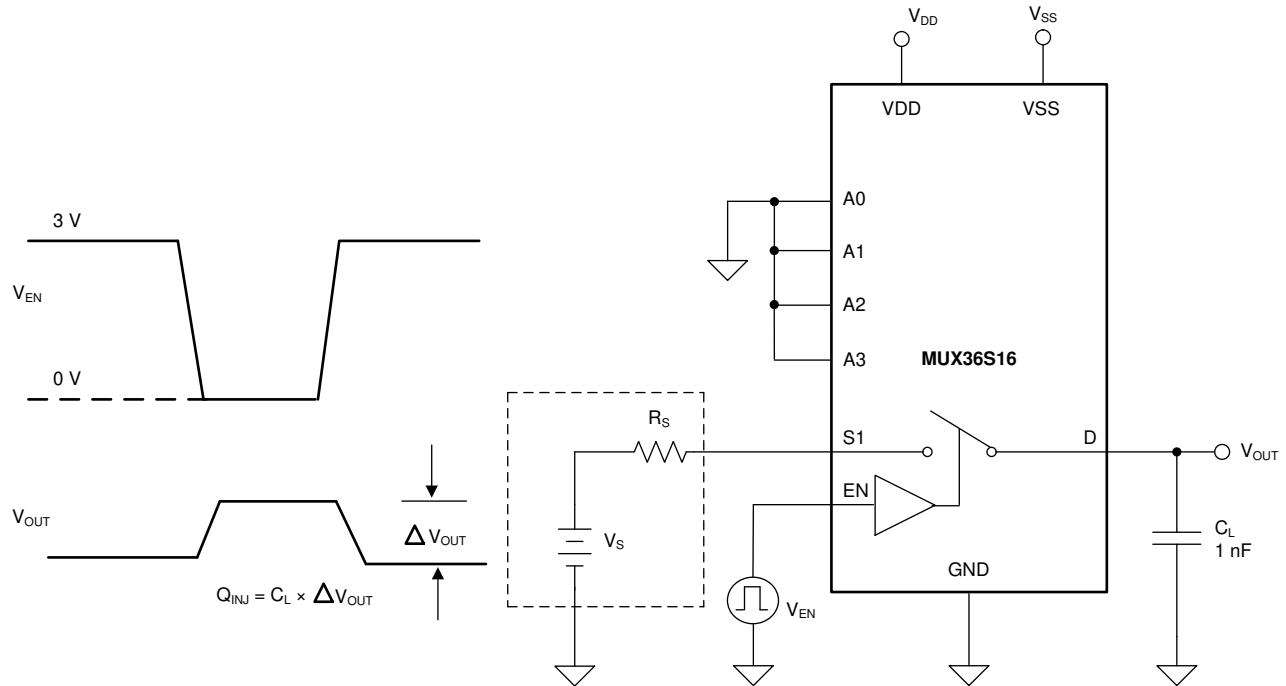


Figure 33. Charge-Injection Measurement Setup

7.1.9 Off Isolation

Off isolation is defined as the voltage at the drain pin (D, DA, or DB) of the MUX36xxx when a 1- V_{RMS} signal is applied to the source pin (Sx, SxA, or SxB) of an off-channel. Figure 34 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.

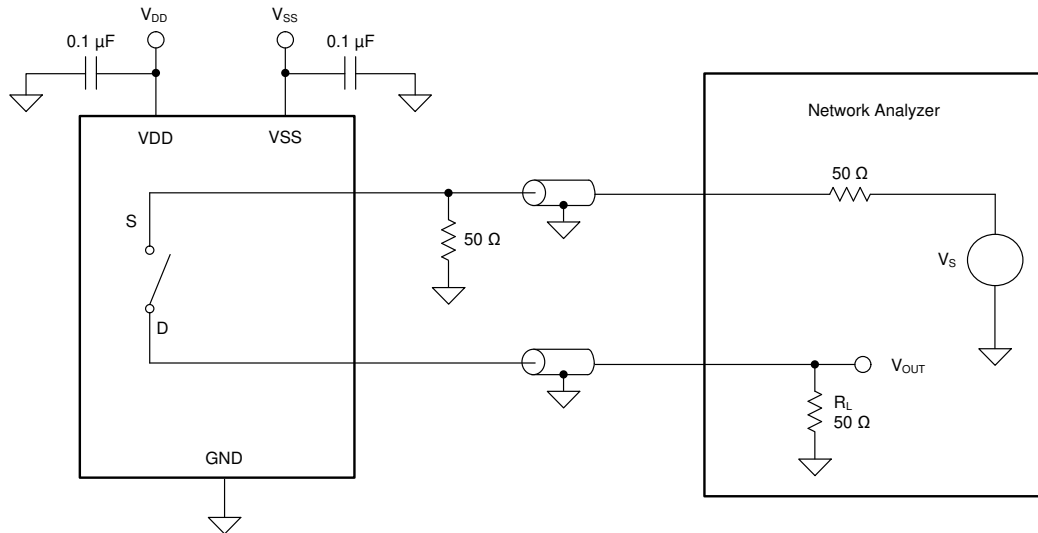


Figure 34. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_{\text{S}}} \right) \quad (2)$$

7.1.10 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx, SxA, or SxB) of an off-channel, when a 1- V_{RMS} signal is applied at the source pin of an on-channel. Figure 35 shows the setup used to measure channel-to-channel crosstalk. Use Equation 3 to compute, channel-to-channel crosstalk.

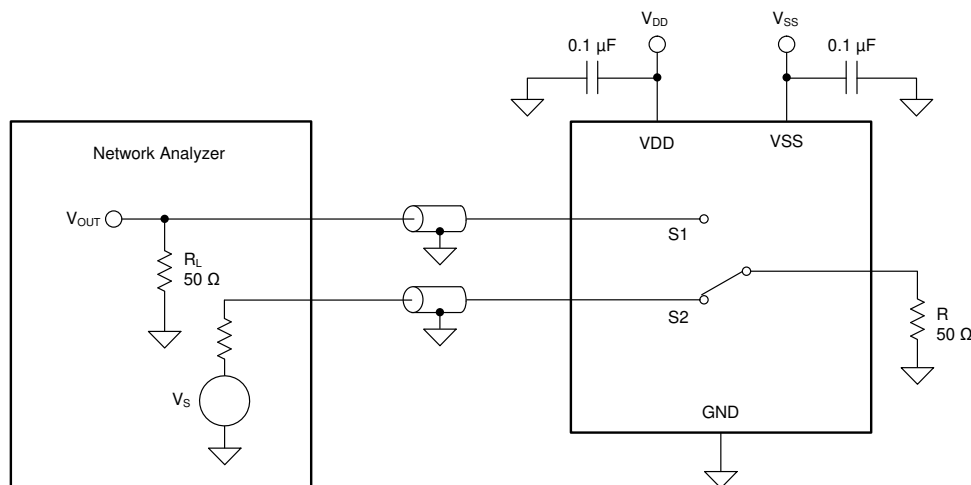


Figure 35. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_{\text{S}}} \right) \quad (3)$$

7.1.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin of an on-channel, and the output measured at the drain pin of the MUX36xxx. Figure 36 shows the setup used to measure on-channel bandwidth of the mux. Use Equation 4 to compute the attenuation.

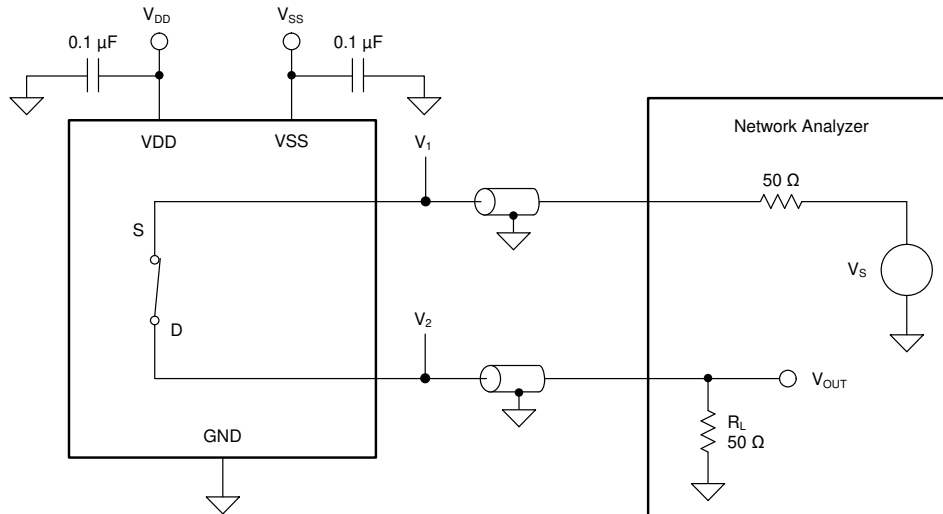


Figure 36. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log} \left(\frac{V_2}{V_1} \right)$$

(4)

7.1.12 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the MUX36xxx varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 37 shows the setup used to measure THD+N of the MUX36xxx.

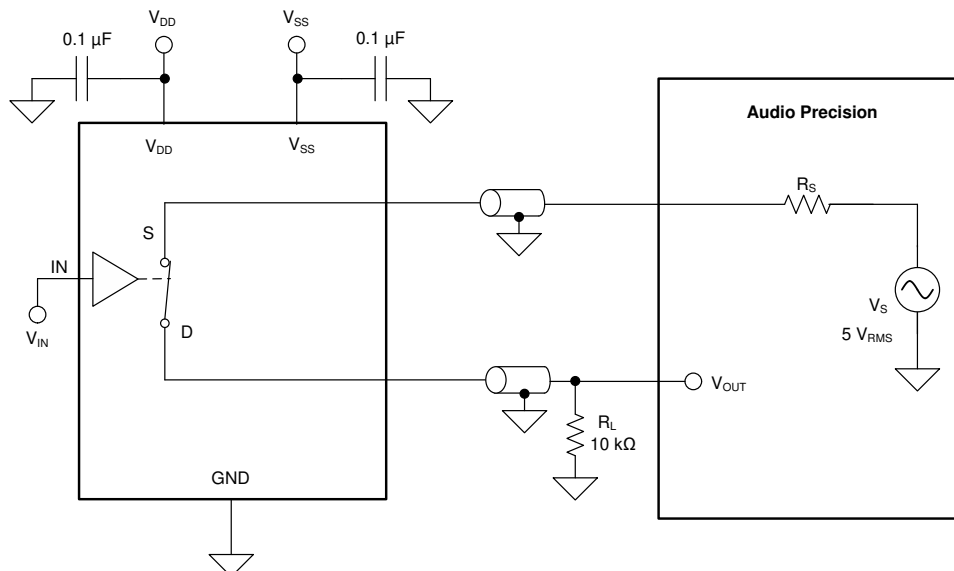


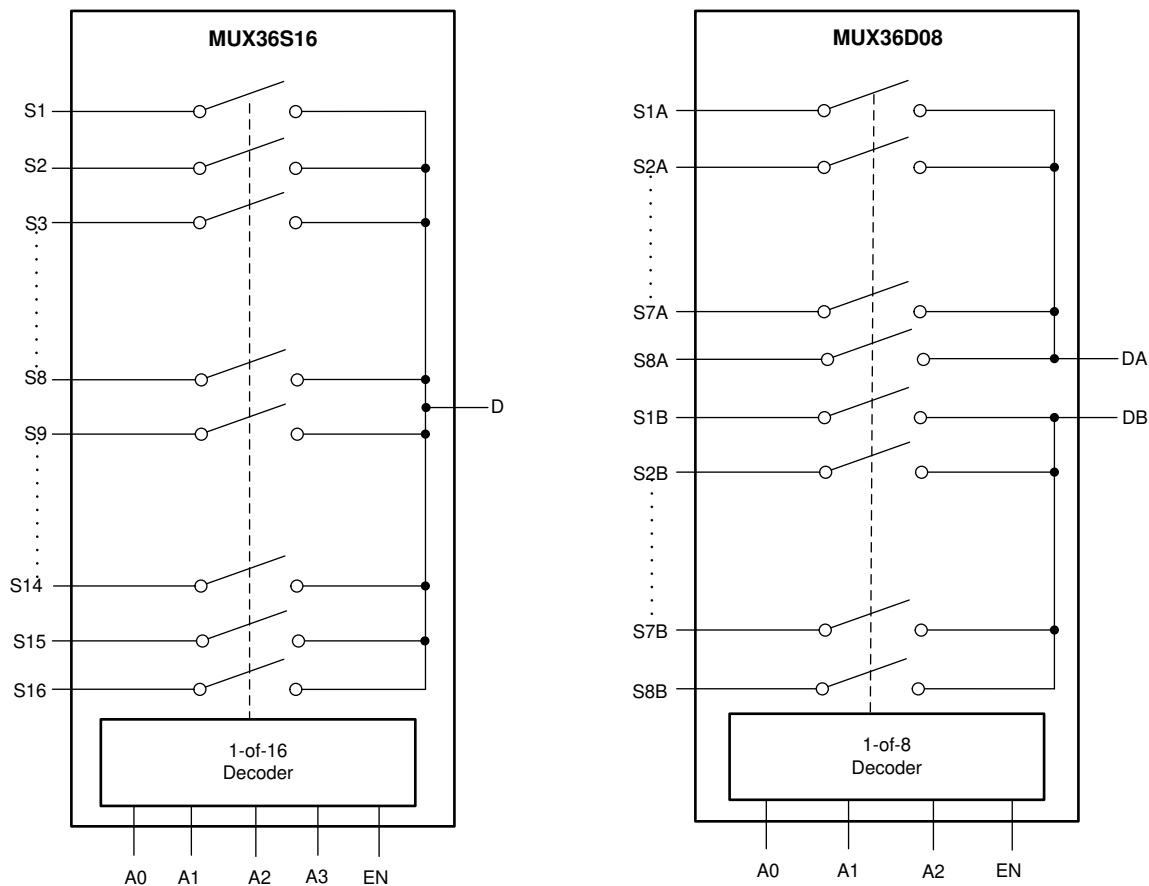
Figure 37. THD+N Measurement Setup

8 Detailed Description

8.1 Overview

The MUX36xxx are a family of analog multiplexers. The *Functional Block Diagram* section provides a top-level block diagram of both the MUX36S16 and MUX36D08. The MUX36S16 is a 16-channel, single-ended, analog mux. The MUX36D08 is an 8-channel, differential or dual 8:1, single-ended, analog mux. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Ultralow Leakage Current

The MUX36xxx provide extremely low on- and off-leakage currents. The MUX36xxx are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. Figure 38 shows typical leakage currents of the MUX36xxx versus temperature.

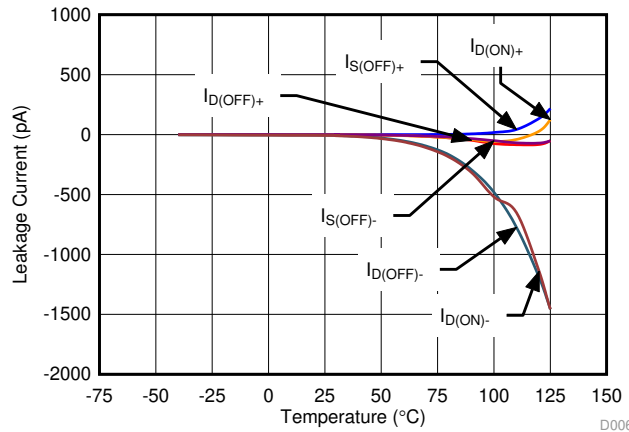


Figure 38. Leakage Current vs Temperature

8.3.2 Ultralow Charge Injection

The MUX36xxx have a simple transmission gate topology, as shown in Figure 39. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

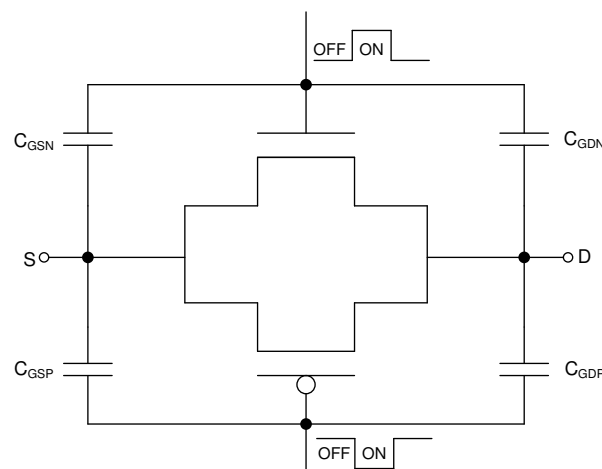


Figure 39. Transmission Gate Topology

Feature Description (continued)

The MUX36xxx have special charge-injection cancellation circuitry that reduces the source-to-drain charge injection to as low as 0.31 pC at $V_S = 0$ V, and ± 0.9 pC in the full signal range, as shown in Figure 40.

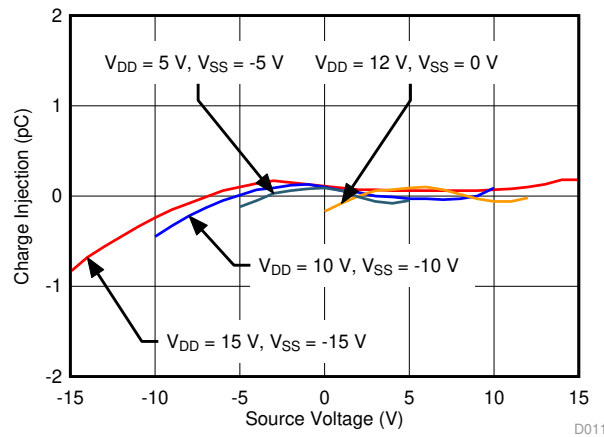


Figure 40. Source-to-Drain Charge Injection

The drain-to-source charge injection becomes important when the device is used as a demultiplexer (demux), where D becomes the input and Sx becomes the output. Figure 41 shows the drain-to-source charge injection across the full signal range.

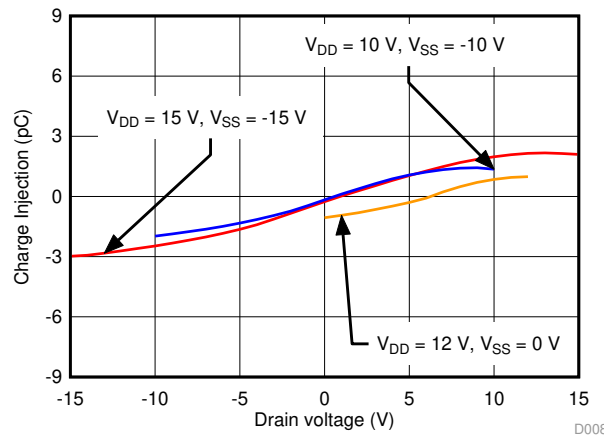


Figure 41. Drain-to-Source Charge Injection

Feature Description (continued)

8.3.3 Bidirectional Operation

The MUX36xxx are operable as both a mux and demux. The source (Sx, SxA, SxB) and drain (D, DA, DB) pins of the MUX36xxx are used either as input or output. Each MUX36xxx channel has very similar characteristics in both directions.

8.3.4 Rail-to-Rail Operation

The valid analog signal for the MUX36xxx ranges from V_{SS} to V_{DD} . The input signal to the MUX36xxx swings from V_{SS} to V_{DD} without any significant degradation in performance. The on-resistance of the MUX36xxx varies with input signal, as shown in Figure 42

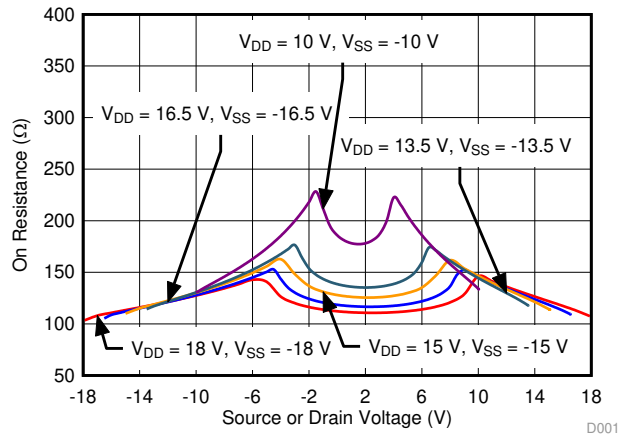


Figure 42. On-resistance vs Source or Drain Voltage

8.4 Device Functional Modes

When the EN pin of the MUX36xxx is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state irrespective of the state of the address lines. The EN pin can be connected to V_{DD} (as high as 36 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MUX36xxx family offers outstanding input/output leakage currents and ultra-low charge injection. These devices operate up to 36 V, and offer true rail-to-rail input and output. The on-capacitance of the MUX36xxx is very low. These features makes the MUX36xxx a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

9.2 Typical Application

Figure 43 shows a 16-bit, differential, 8-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential mux. This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the MUX36D08, OPA192 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

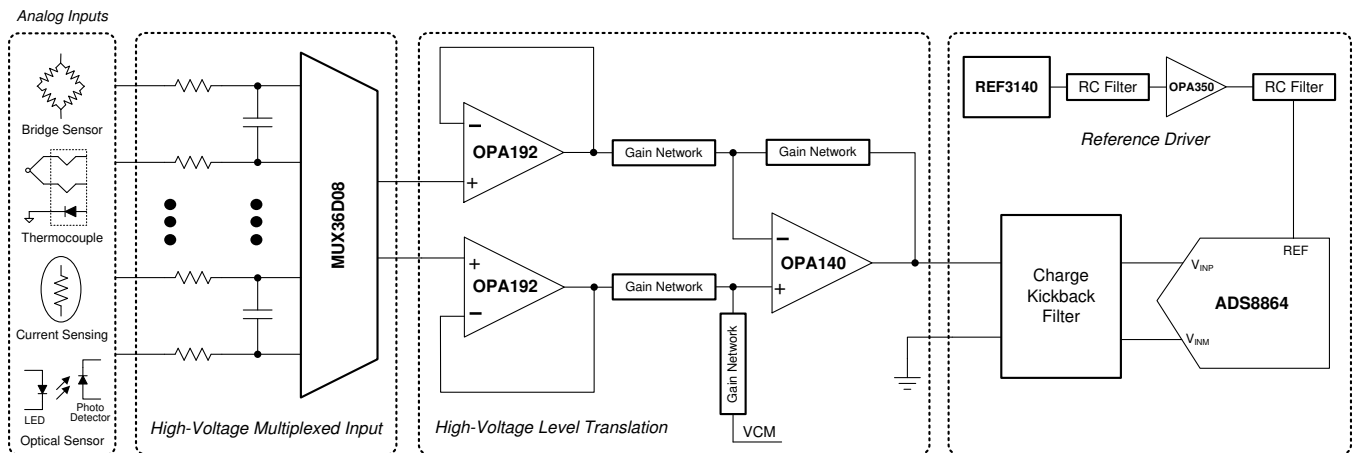


Figure 43. 16-Bit Precision Multiplexed Data-Acquisition System for High-Voltage Inputs With Lowest Distortion

9.2.1 Design Requirements

The primary objective is to design a ± 20 V, differential, 8-channel, multiplexed, data-acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure, sine-wave input. The design requirements for this block design are:

- System supply voltage: ± 15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 20 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

Typical Application (continued)

9.2.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in [Figure 43](#). The circuit is a multichannel, data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, attenuating SAR ADC driver, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. Detailed design considerations and component selection procedure can be found in the TI Precision Design [TIPD151](#), *16-Bit, 400-kSPS, 4-Channel Multiplexed Data-Acquisition System for High-Voltage Inputs with Lowest Distortion*.

9.2.3 Application Curve

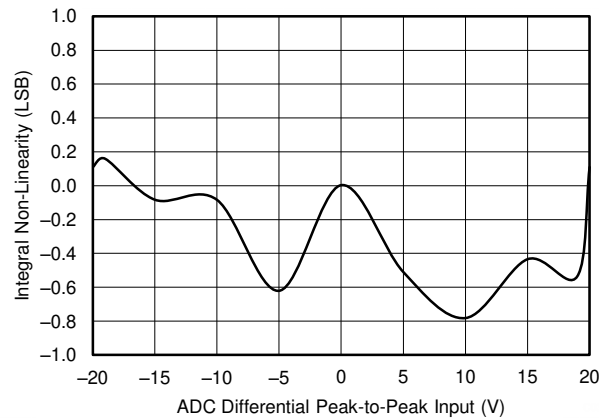


Figure 44. ADC 16-Bit Linearity Error for the Multiplexed Data-Acquisition Block

10 Power Supply Recommendations

The MUX36xxx operates across a wide supply range of ± 5 V to ± 18 V (10 V to 36 V in single-supply mode). The devices also perform well with unsymmetric supplies such as $V_{DD} = 12$ V and $V_{SS} = -5$ V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 μ F to 10 μ F at both the VDD and VSS pins to ground.

The on-resistance of the MUX36xxx varies with supply voltage, as illustrated in [Figure 45](#)

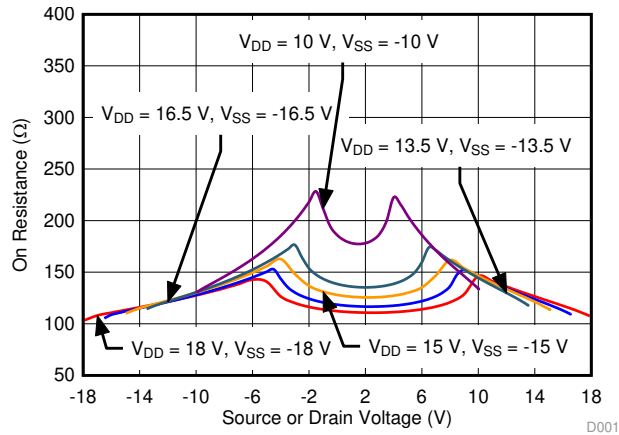


Figure 45. On-Resistance Variation With Supply and Input Voltage

11 Layout

11.1 Layout Guidelines

Figure 46 illustrates an example of a PCB layout with the MUX36S16IPW, and Figure 47 illustrates an example of a PCB layout with MUX36D08IPW.

Some key considerations are:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1- μ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible. In case of the differential signal, make sure the A inputs and B inputs are as symmetric as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

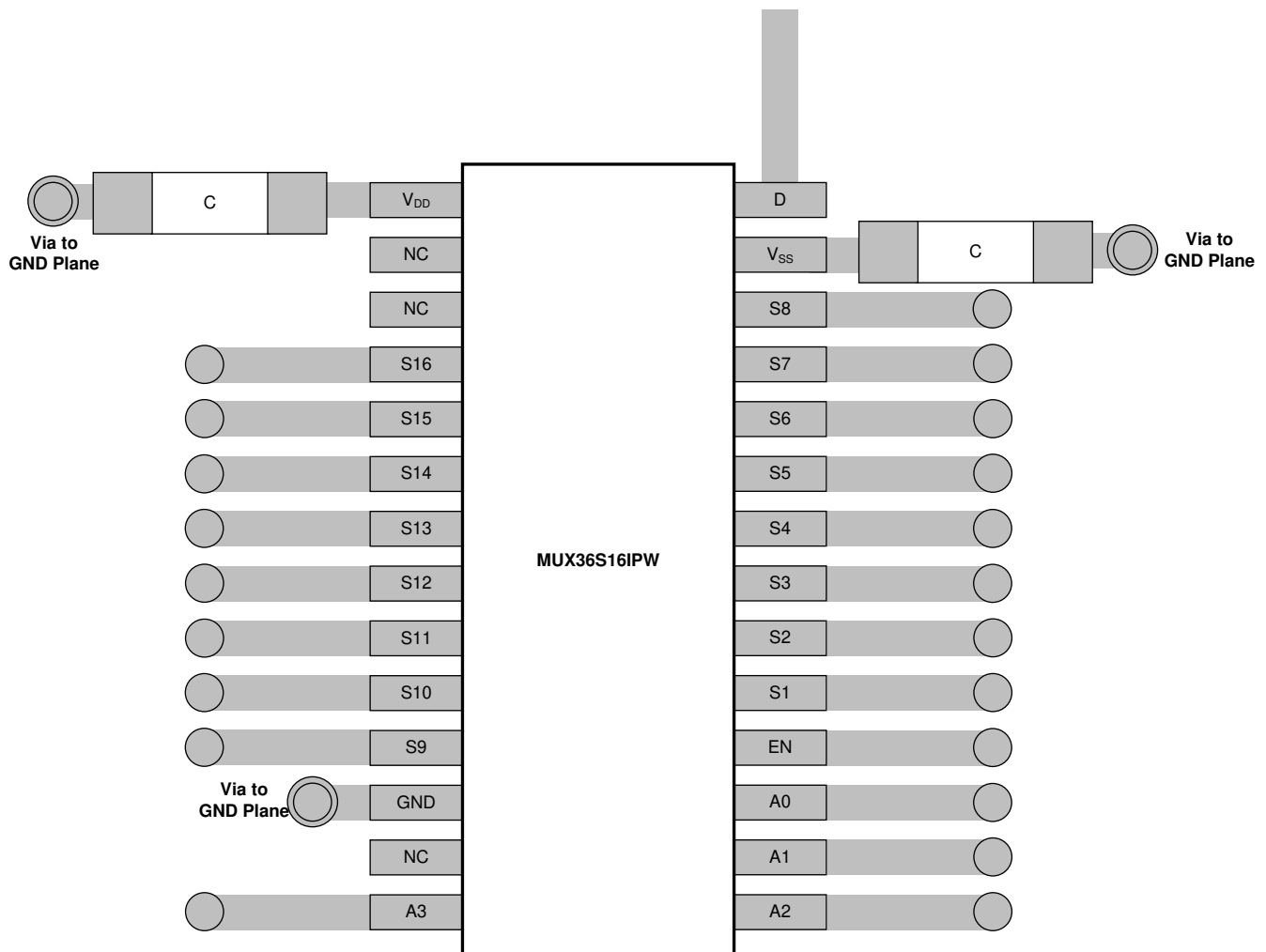


Figure 46. MUX36S16IPW Layout Example

Layout Example (continued)

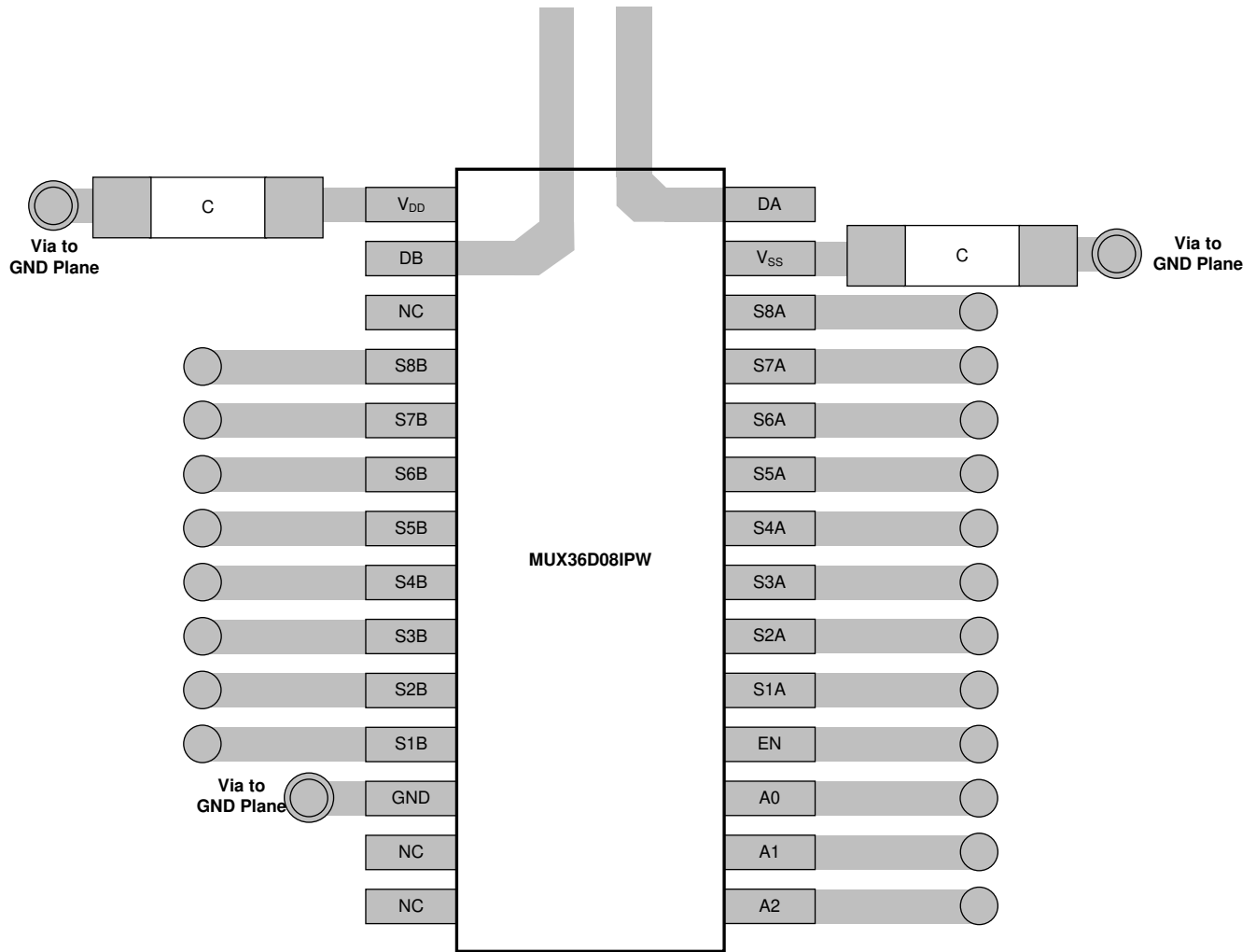


Figure 47. MUX36D08IPW Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [ADS8864 16-Bit, 400-kSPS, Serial Interface, microPower, Miniature, Single-Ended Input, SAR Analog-to-Digital Converter](#) (SBAS572)
- [OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim](#) (SBOS620)
- [OPAx140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz JFET Op Amp](#) (SBOS498)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MUX36S16 | Click here | Click here | Click here | Click here | Click here |
| MUX36D08 | Click here | Click here | Click here | Click here | Click here |

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| MUX36D08IDWR | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D08D |
| MUX36D08IDWR.B | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D08D |
| MUX36D08IDWRG4 | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D08D |
| MUX36D08IDWRG4.B | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D08D |
| MUX36D08IPW | Active | Production | TSSOP (PW) 28 | 50 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D080A |
| MUX36D08IPW.B | Active | Production | TSSOP (PW) 28 | 50 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D080A |
| MUX36D08IPWR | Active | Production | TSSOP (PW) 28 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D080A |
| MUX36D08IPWR.B | Active | Production | TSSOP (PW) 28 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D080A |
| MUX36D08IPWRG4 | Active | Production | TSSOP (PW) 28 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D080A |
| MUX36D08IPWRG4.B | Active | Production | TSSOP (PW) 28 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36D080A |
| MUX36D08IRSNR | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | MUX 36D08 |
| MUX36D08IRSNR.B | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | MUX 36D08 |
| MUX36D08IRSNRG4 | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36D08 |
| MUX36D08IRSNRG4.B | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36D08 |
| MUX36D08IRTVR | Active | Production | WQFN (RTV) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36D08 |
| MUX36D08IRTVR.B | Active | Production | WQFN (RTV) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36D08 |
| MUX36S16IDWR | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36S16DA |
| MUX36S16IDWR.B | Active | Production | SOIC (DW) 28 | 1000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36S16DA |
| MUX36S16IPW | Active | Production | TSSOP (PW) 28 | 50 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36S160A |
| MUX36S16IPW.B | Active | Production | TSSOP (PW) 28 | 50 TUBE | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36S160A |
| MUX36S16IPWR | Active | Production | TSSOP (PW) 28 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36S160A |
| MUX36S16IPWR.B | Active | Production | TSSOP (PW) 28 | 2000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | MUX36S160A |
| MUX36S16IRSNR | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36S16 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| MUX36S16IRSNR.B | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36S16 |
| MUX36S16IRSNRG4 | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36S16 |
| MUX36S16IRSNRG4.B | Active | Production | QFN (RSN) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36S16 |
| MUX36S16IRTVR | Active | Production | WQFN (RTV) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36S16 |
| MUX36S16IRTVR.B | Active | Production | WQFN (RTV) 32 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX 36S16 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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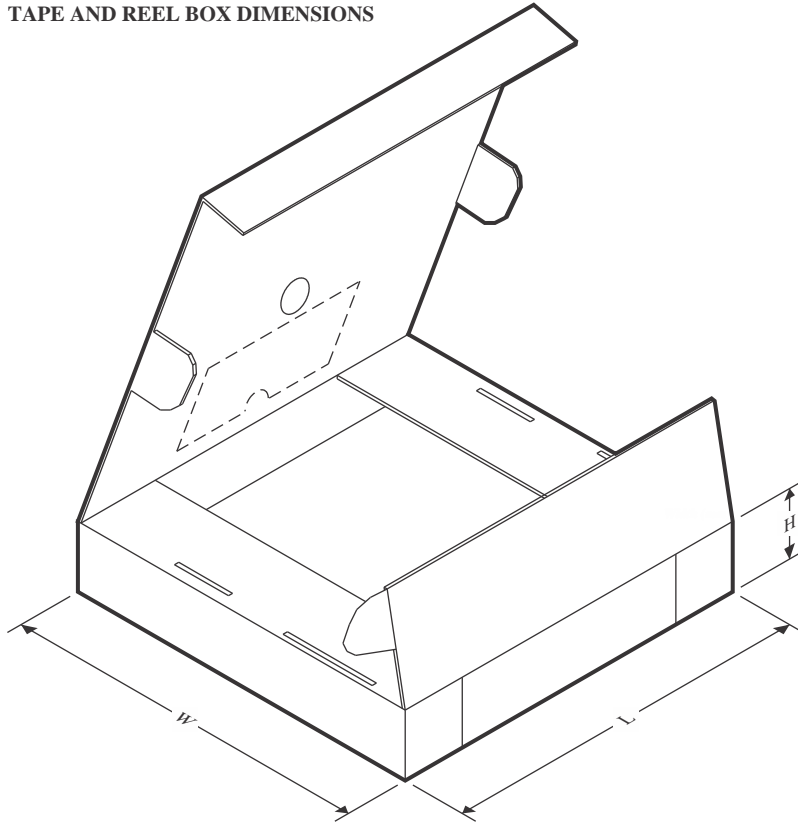
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MUX36D08IDWR | SOIC | DW | 28 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| MUX36D08IDWRG4 | SOIC | DW | 28 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| MUX36D08IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MUX36D08IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MUX36D08IPWRG4 | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MUX36D08IPWRG4 | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MUX36D08IRSNR | QFN | RSN | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MUX36D08IRSNRG4 | QFN | RSN | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MUX36D08IRTVR | WQFN | RTV | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MUX36S16IDWR | SOIC | DW | 28 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| MUX36S16IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MUX36S16IPWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| MUX36S16IRSNR | QFN | RSN | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MUX36S16IRSNRG4 | QFN | RSN | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MUX36S16IRTVR | WQFN | RTV | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MUX36D08IDWR | SOIC | DW | 28 | 1000 | 350.0 | 350.0 | 66.0 |
| MUX36D08IDWRG4 | SOIC | DW | 28 | 1000 | 350.0 | 350.0 | 66.0 |
| MUX36D08IPWR | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MUX36D08IPWR | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MUX36D08IPWRG4 | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MUX36D08IPWRG4 | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MUX36D08IRSNR | QFN | RSN | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MUX36D08IRSNRG4 | QFN | RSN | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MUX36D08IRTVR | WQFN | RTV | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MUX36S16IDWR | SOIC | DW | 28 | 1000 | 350.0 | 350.0 | 66.0 |
| MUX36S16IPWR | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MUX36S16IPWR | TSSOP | PW | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| MUX36S16IRSNR | QFN | RSN | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MUX36S16IRSNRG4 | QFN | RSN | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MUX36S16IRTVR | WQFN | RTV | 32 | 3000 | 367.0 | 367.0 | 35.0 |

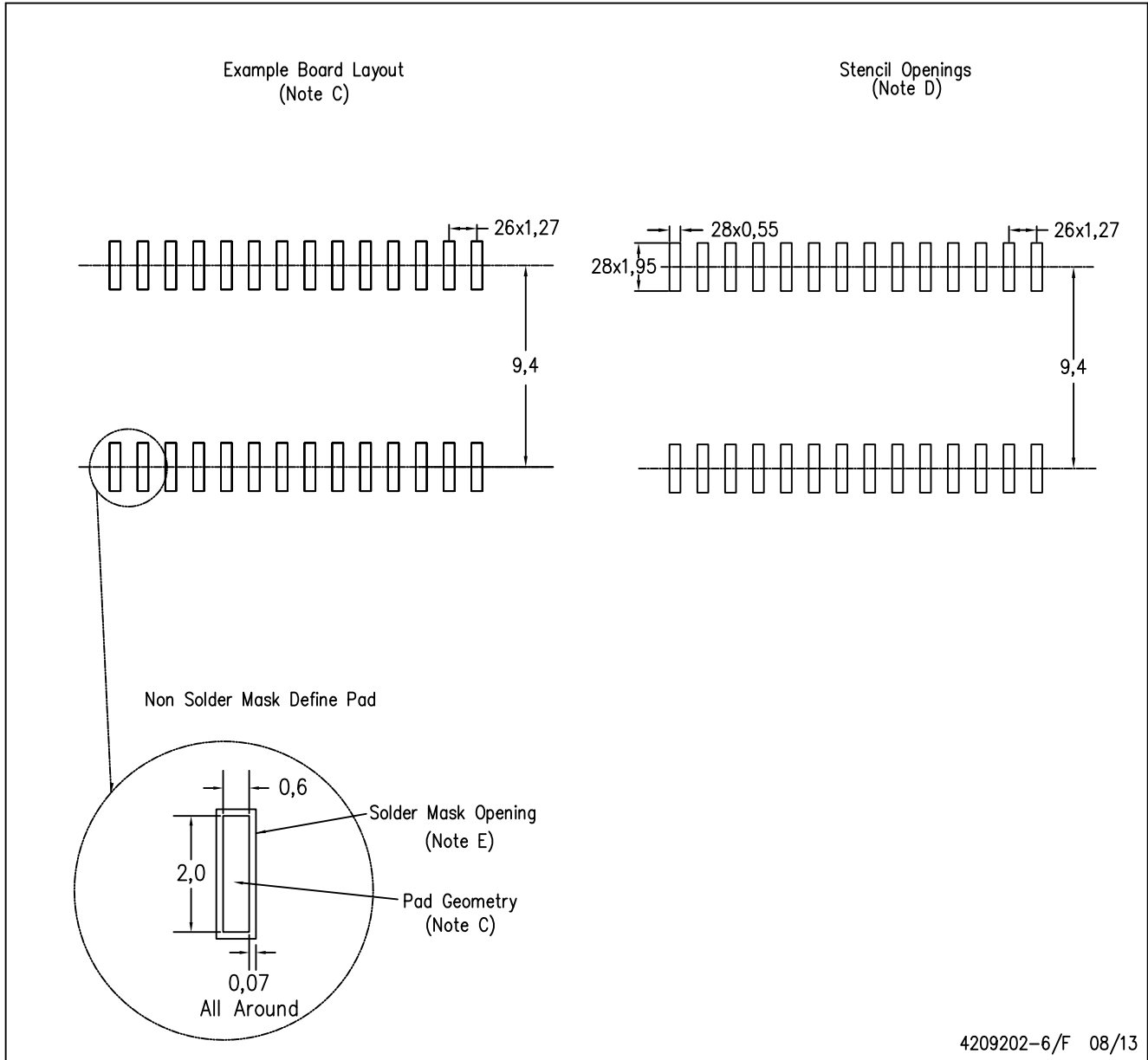
TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| MUX36D08IPW | PW | TSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |
| MUX36D08IPW.B | PW | TSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |
| MUX36S16IPW | PW | TSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |
| MUX36S16IPW.B | PW | TSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



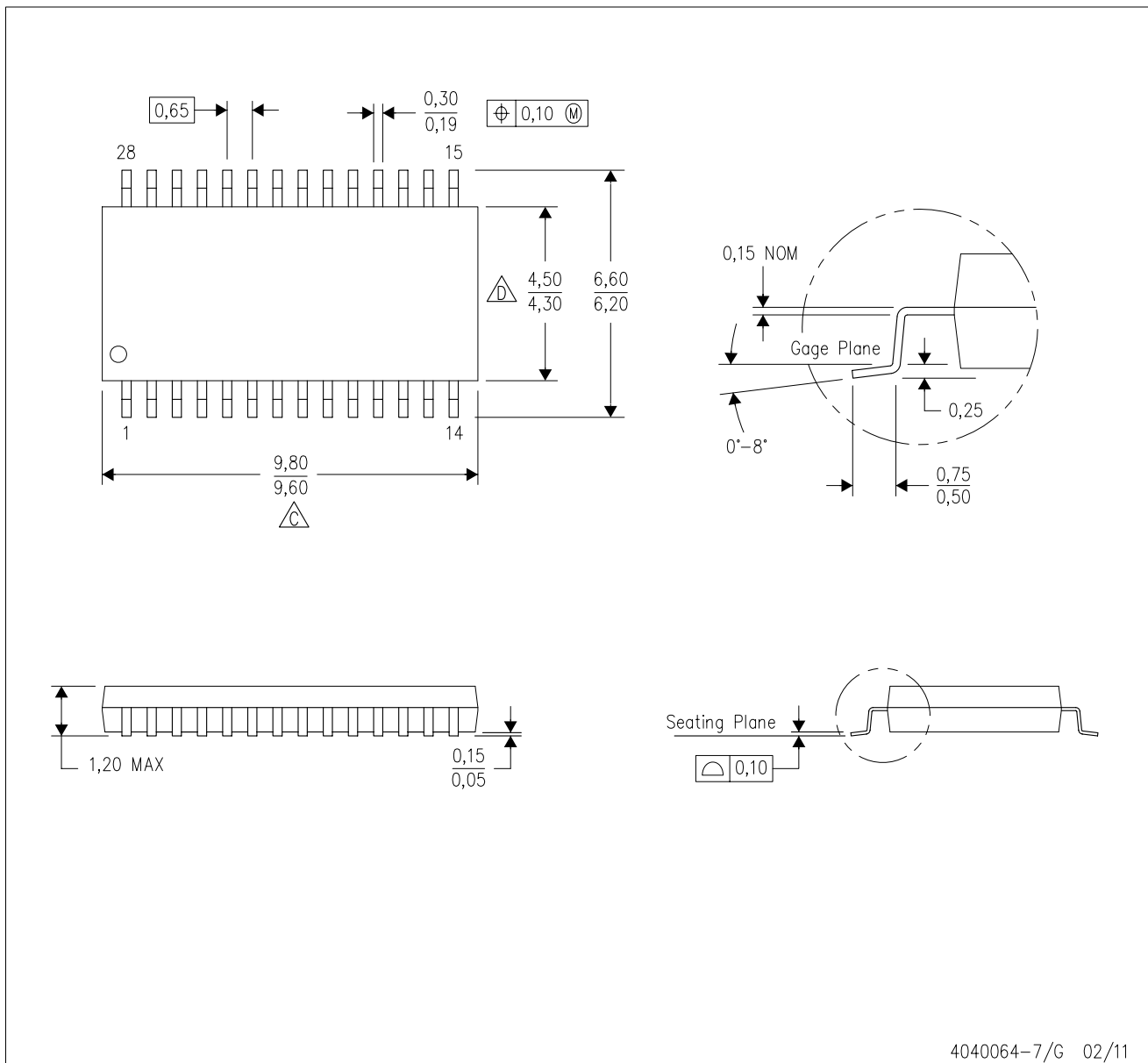
4209202-6/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

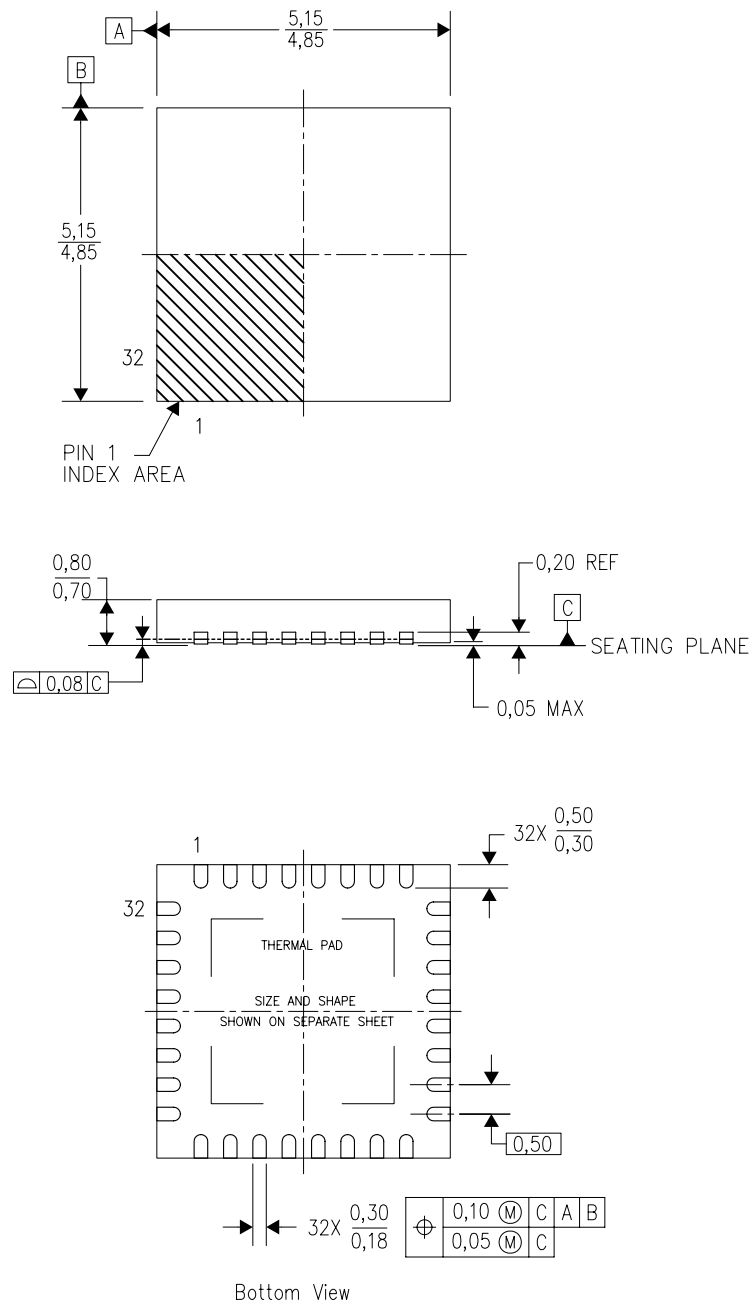


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

RTV (S-PWQFN-N32)

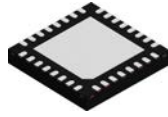
PLASTIC QUAD FLATPACK NO-LEAD



4206245/C 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

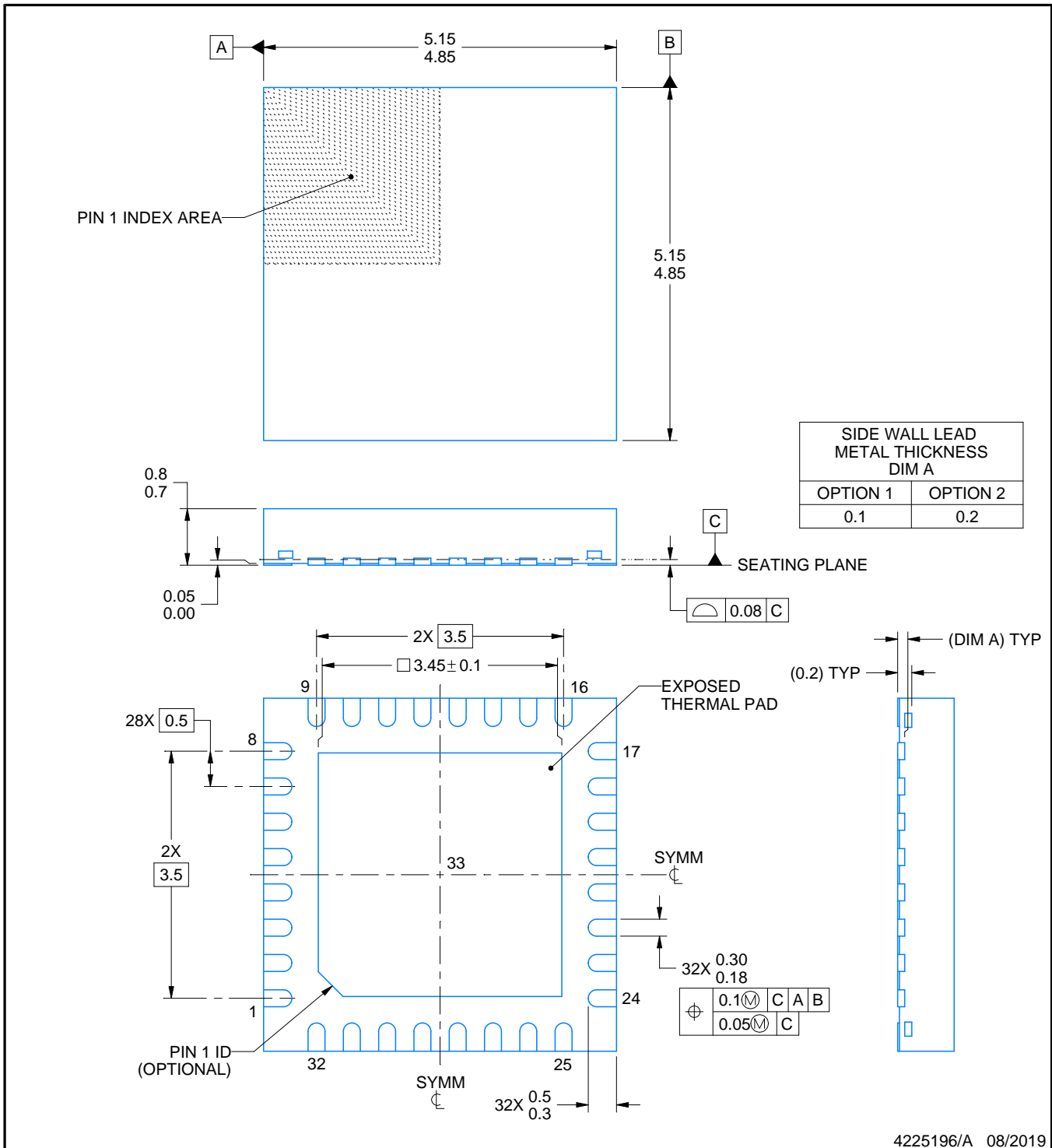
RTV0032E



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4225196/A 08/2019

NOTES:

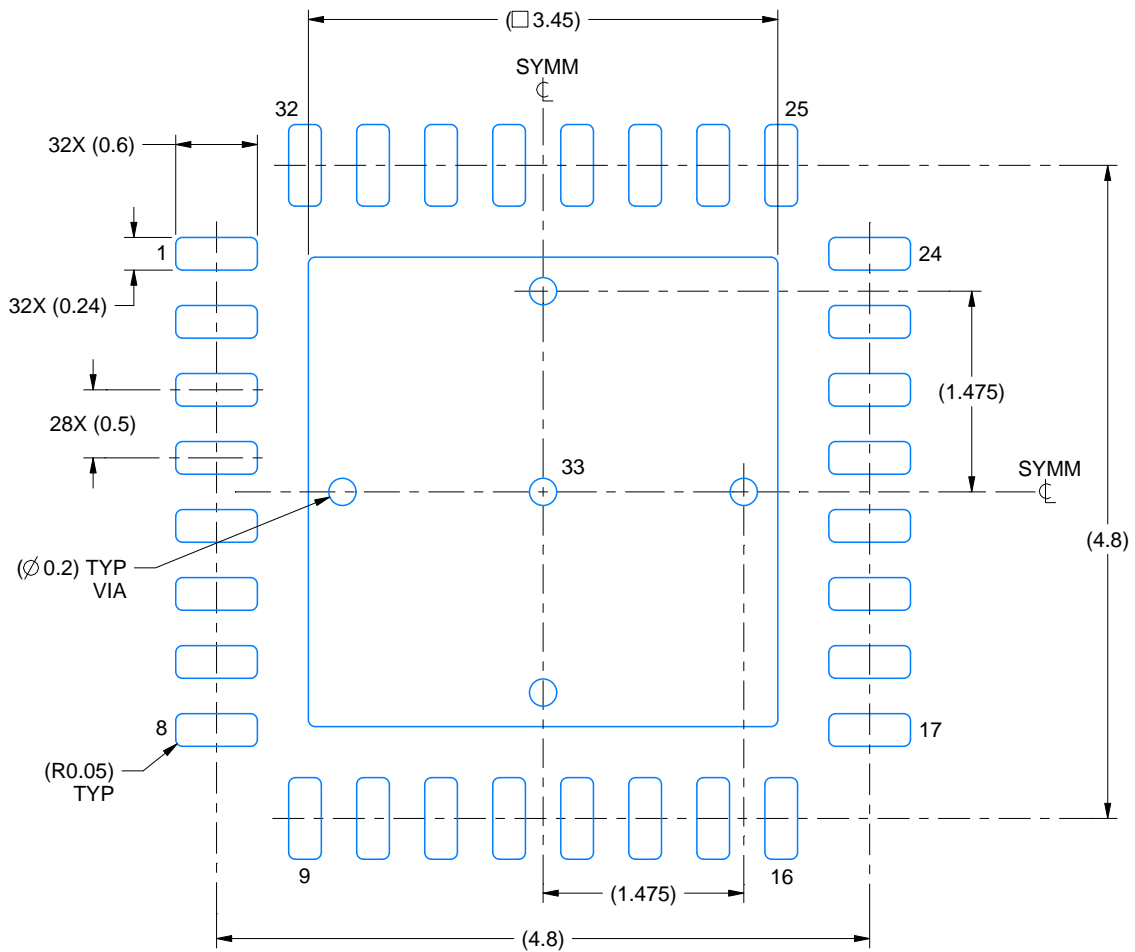
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

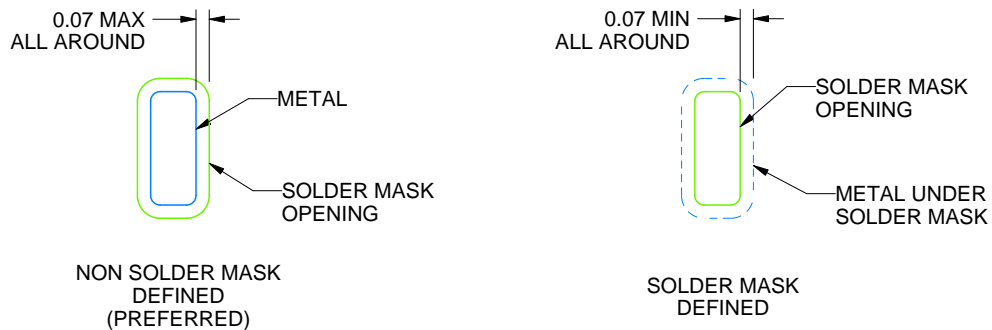
RTV0032E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4225196/A 08/2019

NOTES: (continued)

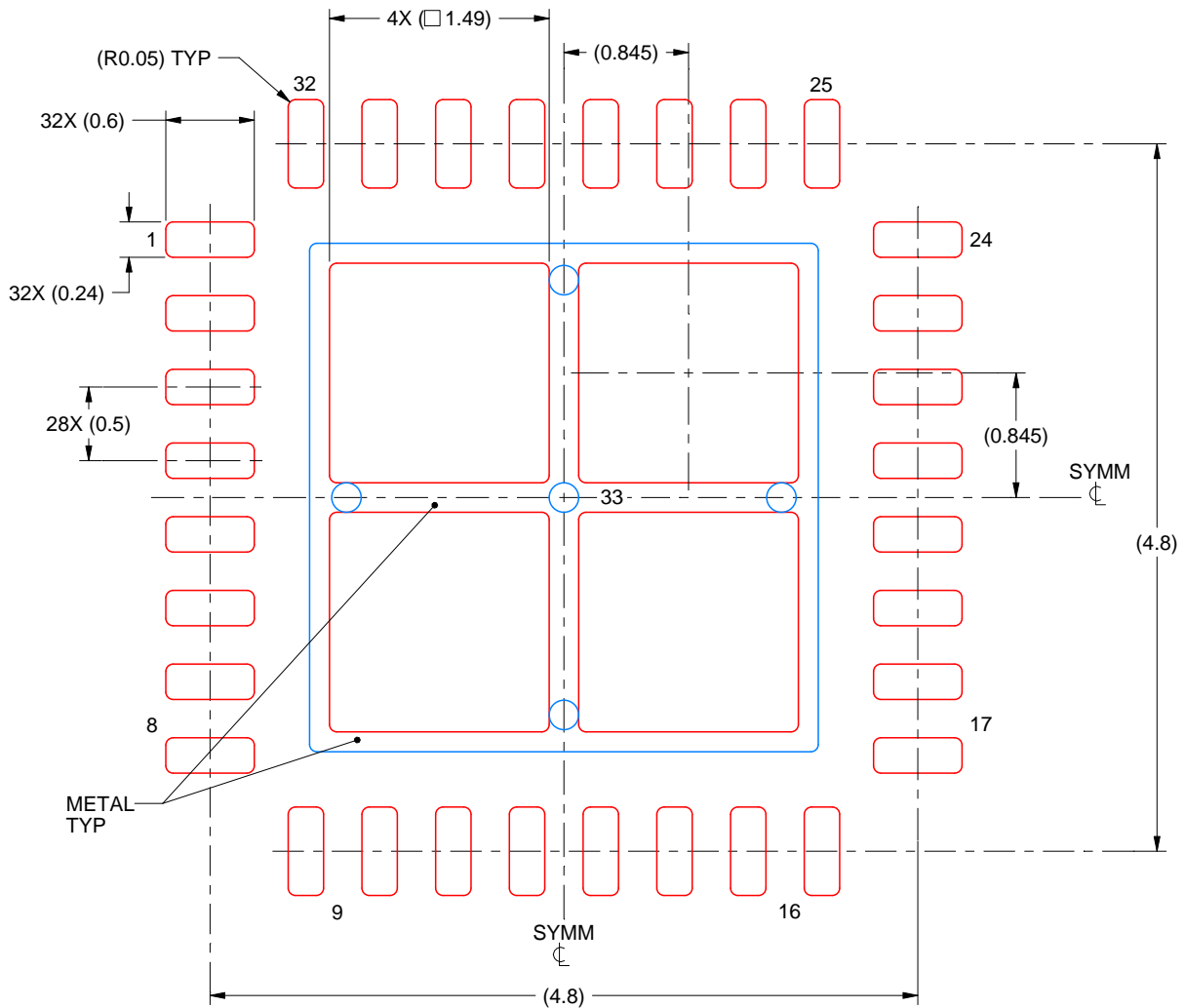
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTV0032E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225196/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

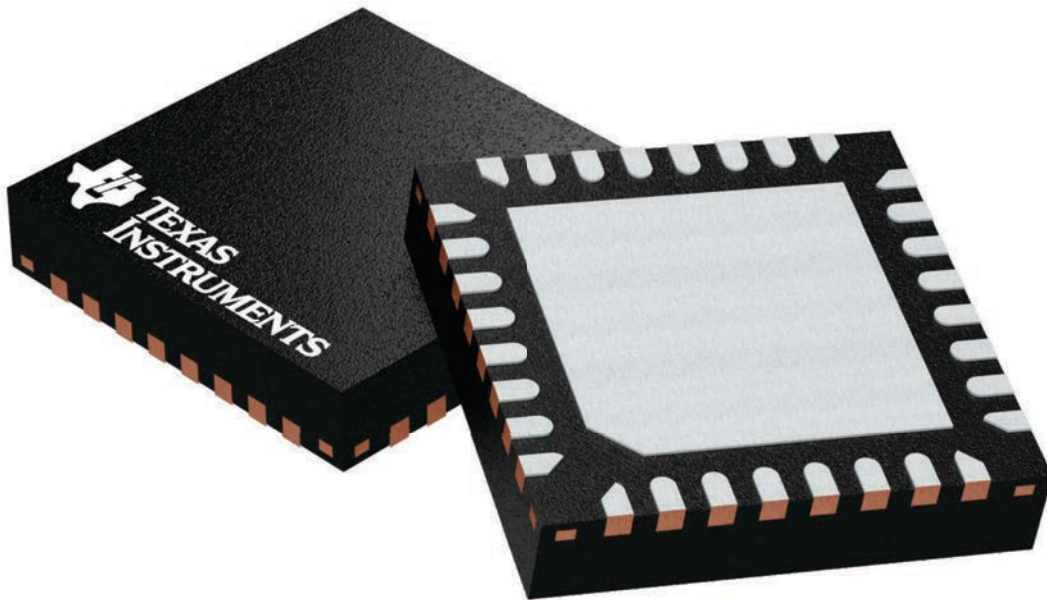
RSN 32

WQFN - 0.8 mm max height

4 x 4, 0.4 mm pitch

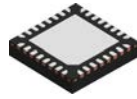
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225265/A

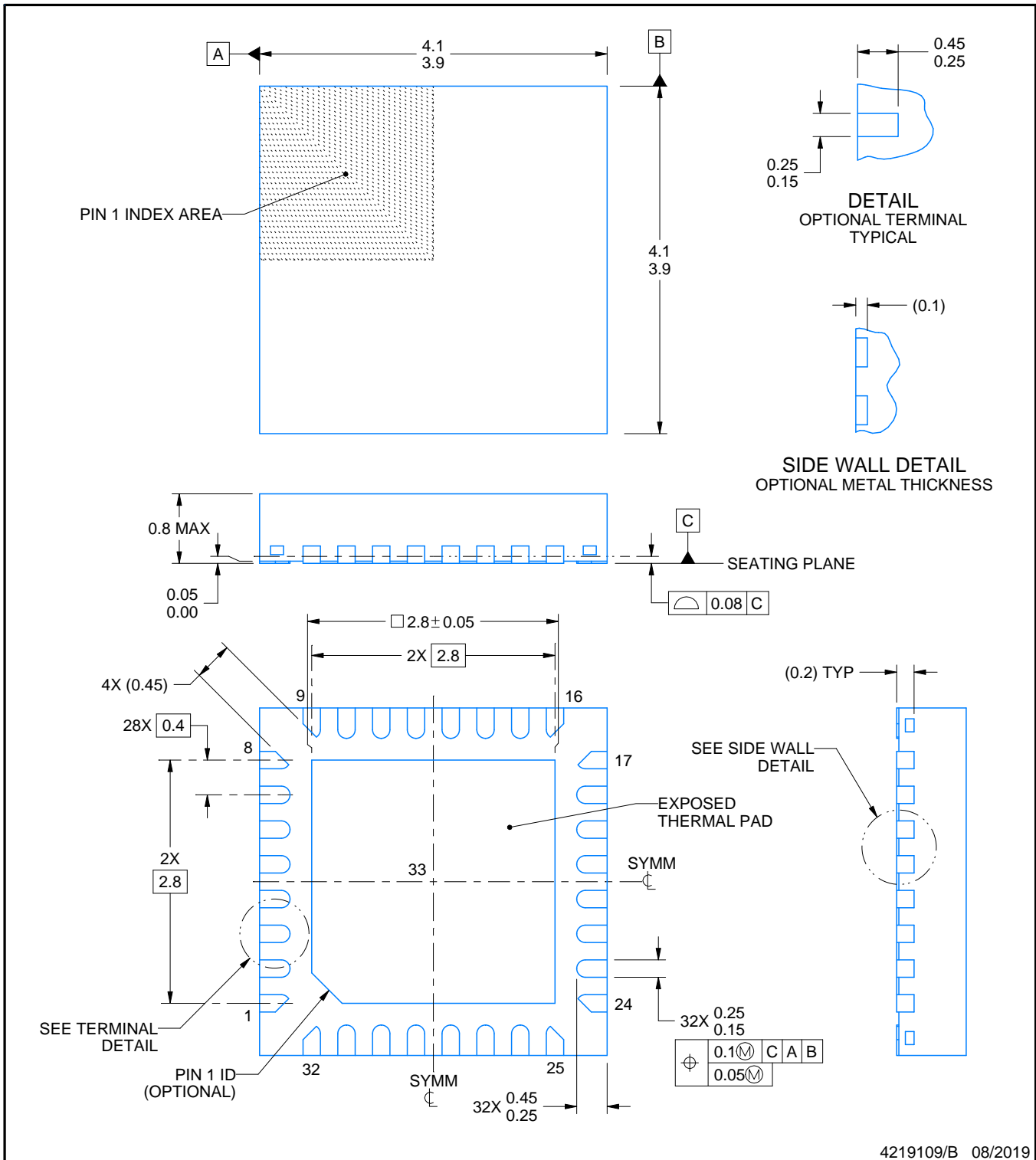
RSN0032B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

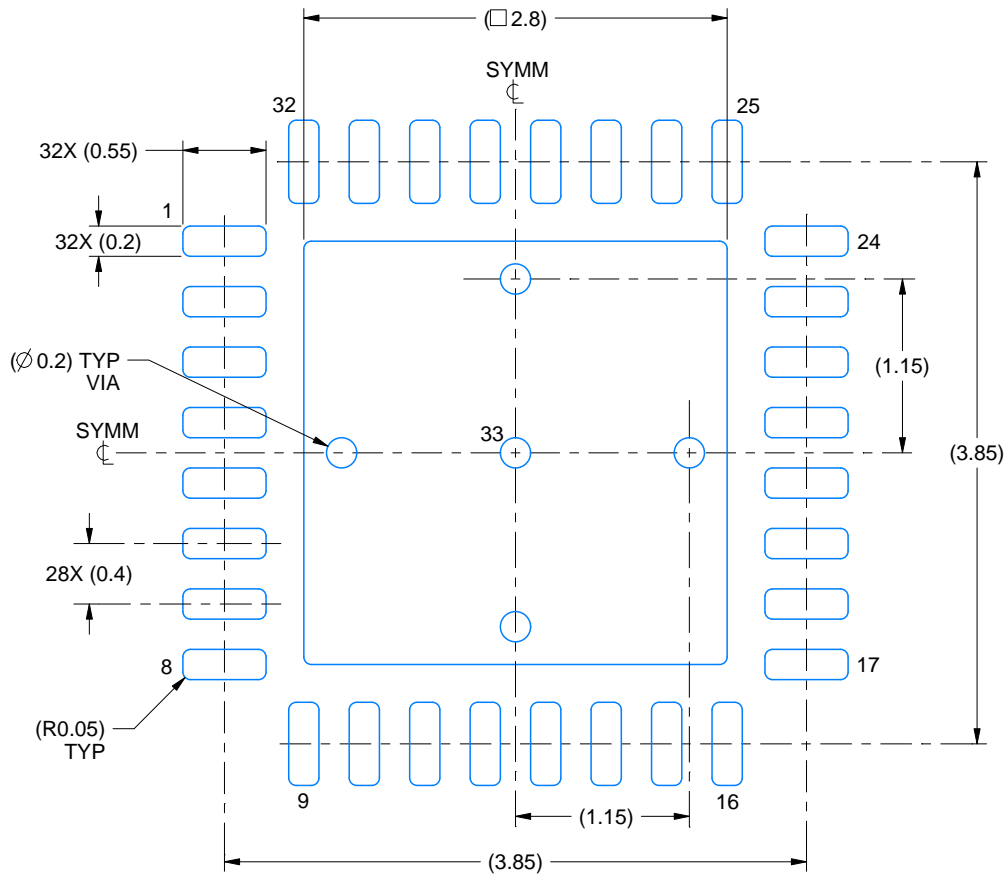
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

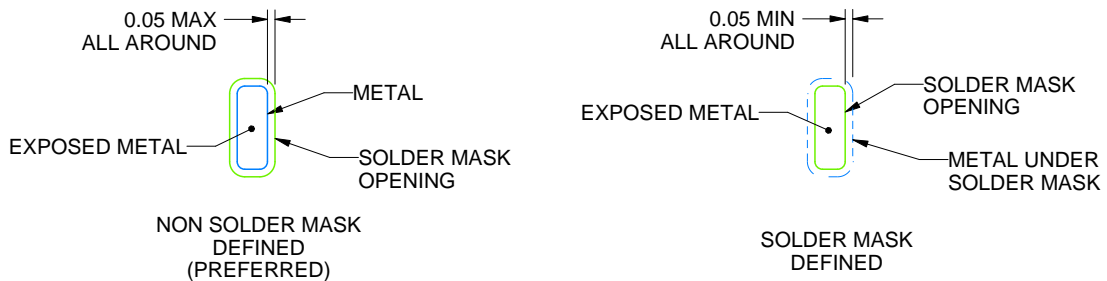
RSN0032B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219109/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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