

OPAx377-Q1 Low-Noise, Low Quiescent Current, Precision Automotive Grade Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level 3A
 - Device CDM ESD Classification Level C6
- Low Noise: 7.5 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- 0.1-Hz to 10-Hz Noise: 0.8 μV_{PP}
- Quiescent Current: 760 μA (typical)
- Low Offset Voltage: 250 μV (typical)
- Gain Bandwidth Product: 5.5 MHz
- Rail-to-Rail Input and Output
- Single-Supply Operation
- Supply Voltage: 2.2 V to 5.5 V
- Space-Saving Packages:
 - SOT-23, VSSOP, TSSOP

2 Applications

- Active Cruise Control
- Park Assist
- Tire Pressure Monitoring
- Infotainment
- Active Filtering
- Sensor Signal Conditioning

3 Description

The OPAx377-Q1 family of operational amplifiers are wide-bandwidth CMOS amplifiers that provide very low noise, low input bias current, and low offset voltage while operating on a low quiescent current of 0.76 mA (typical).

The OPAx377-Q1 op amps are optimized for low-voltage, single-supply applications. The exceptional combination of ac and dc performance make them ideal for a wide range of applications, including small signal conditioning, audio, and active filters. In addition, these parts have a wide supply range with excellent PSRR, making them attractive for applications that run directly from batteries without regulation.

The OPA377-Q1 is available in the SOT23-5 package. The dual, OPA2377-Q1, is offered in the MSOP-8 package and the quad OPA4377-Q1 is offered in the TSSOP-14 package. All versions are specified for operation from –40°C to +125°C.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| OPA377-Q1 | SOT-23 (5) | 2.90 mm x 1.60 mm |
| OPA2377-Q1 | VSSOP (8) | 3.00 mm x 3.00 mm |
| OPA4377-Q1 | TSSOP (14) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Low-Side Current Sense Amplifier

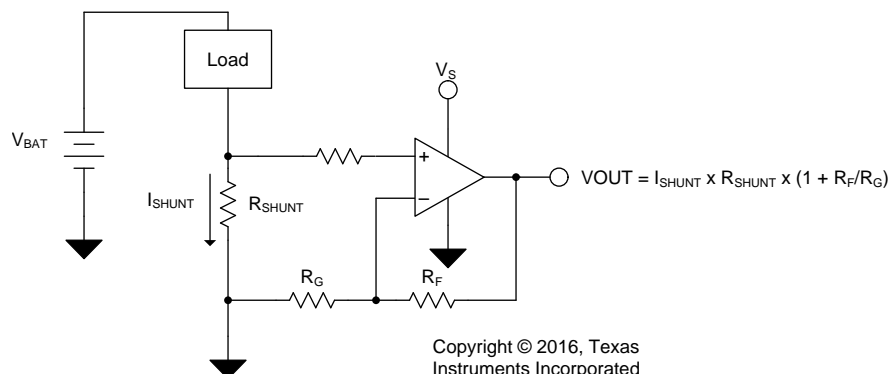


Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 7.3 Feature Description..... | 14 |
| 2 Applications | 1 | 7.4 Device Functional Modes..... | 15 |
| 3 Description | 1 | 8 Application and Implementation | 16 |
| 4 Revision History | 2 | 8.1 Application Information..... | 16 |
| 5 Pin Configuration and Functions | 3 | 8.2 Typical Application | 16 |
| 6 Specifications | 6 | 9 Power Supply Recommendations | 18 |
| 6.1 Absolute Maximum Ratings | 6 | 10 Layout | 18 |
| 6.2 ESD Ratings | 6 | 10.1 Layout Guidelines | 18 |
| 6.3 Recommended Operating Conditions..... | 6 | 10.2 Layout Example | 18 |
| 6.4 Thermal Information: OPA377-Q1 | 6 | 11 Device and Documentation Support | 20 |
| 6.5 Thermal Information: OPA2377-Q1 | 6 | 11.1 Device Support | 20 |
| 6.6 Thermal Information: OPA4377-Q1 | 7 | 11.2 Documentation Support | 21 |
| 6.7 Electrical Characteristics: $V_S = 2.2\text{ V to }5.5\text{ V}$ | 7 | 11.3 Community Resources..... | 21 |
| 6.8 Typical Characteristics | 9 | 11.4 Trademarks | 21 |
| 7 Detailed Description | 13 | 11.5 Electrostatic Discharge Caution..... | 21 |
| 7.1 Overview | 13 | 11.6 Glossary | 21 |
| 7.2 Functional Block Diagram | 13 | 12 Mechanical, Packaging, and Orderable Information | 21 |

4 Revision History

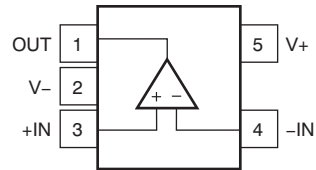
Changes from Original (May 2016) to Revision A

Page

| | |
|---|----------|
| • Changed device status from <i>Product Preview</i> to <i>Production Data</i> | 1 |
|---|----------|

5 Pin Configuration and Functions

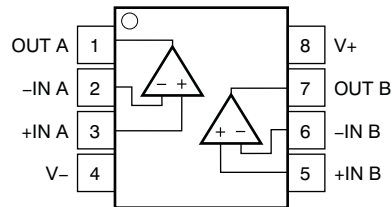
OPA377-Q1: DBV Package
5-Pin SOT23
Top View



Pin Functions: OPA377-Q1

| PIN | | I/O | DESCRIPTION |
|------|------------|-----|---|
| NAME | NO. DBV | | |
| +IN | 3 | I | Noninverting input |
| -IN | 4 | I | Inverting input |
| NC | — | — | No internal connection (can be left floating) |
| OUT | 1 | O | Output |
| V- | 2 | — | Negative (lowest) power supply |
| V+ | 5 | — | Positive (highest) power supply |

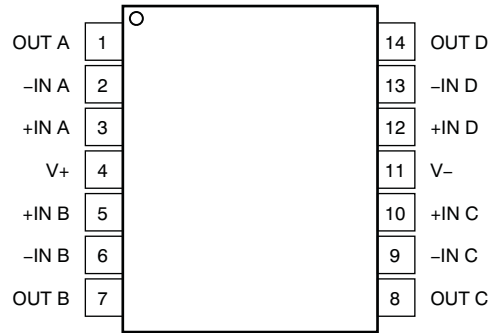
**OPA2377-Q1: DGK Package
8-Pin VSSOP and SOIC
Top View**



Pin Functions: OPA2377-Q1

| PIN | | I/O | DESCRIPTION |
|-------|------------|-----|---------------------------------|
| NAME | NO. DGK | | |
| -IN A | 2 | I | Inverting input, channel A |
| -IN B | 6 | I | Inverting input, channel B |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V- | 4 | — | Negative (lowest) power supply |
| V+ | 8 | — | Positive (highest) power supply |

**OPA4377-Q1: PW Package
14-Pin TSSOP
Top View**



Pin Functions: OPA4377-Q1

| PIN | | I/O | DESCRIPTION |
|-------|-----------|-----|---------------------------------|
| NAME | NO. PW | | |
| -IN A | 2 | I | Inverting input, channel A |
| -IN B | 6 | I | Inverting input, channel B |
| -IN C | 9 | I | Inverting input, channel C |
| -IN D | 13 | I | Inverting input, channel D |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| +IN C | 10 | I | Noninverting input, channel C |
| +IN D | 12 | I | Noninverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V- | 11 | — | Negative (lowest) power supply |
| V+ | 4 | — | Positive (highest) power supply |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|--|------------|------------|------|
| $V_S = (V+) - (V-)$ | Supply voltage | | 7 | V |
| | Signal input terminal voltage ⁽²⁾ | (V-) – 0.5 | (V+) + 0.5 | V |
| | Signal input terminal current ⁽²⁾ | –10 | 10 | mA |
| | Output short-circuit current ⁽³⁾ | Continuous | | |
| T_A | Operating temperature | –40 | 150 | °C |
| T_J | Junction temperature | | 150 | °C |
| T_{stg} | Storage temperature | –65 | 150 | °C |

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|---|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-------|-----------------------|-----|-----|------|
| | Supply voltage | 2.2 | 5.5 | V |
| T_A | Operating temperature | –40 | 150 | °C |

6.4 Thermal Information: OPA377-Q1

| THERMAL METRIC ⁽¹⁾ | | OPA377-Q1 | UNIT |
|-------------------------------|--|-------------|------|
| | | DBV (SOT23) | |
| | | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 273.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 126.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 85.9 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 10.9 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 84.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Thermal Information: OPA2377-Q1

| THERMAL METRIC ⁽¹⁾ | | OPA2377-Q1 | UNIT |
|-------------------------------|---|-------------|------|
| | | DGK (VSSOP) | |
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 171.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 63.9 | °C/W |

- For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

Thermal Information: OPA2377-Q1 (continued)

| THERMAL METRIC ⁽¹⁾ | | OPA2377-Q1 | UNIT |
|-------------------------------|--|-------------|------|
| | | DGK (VSSOP) | |
| | | 8 PINS | |
| R _{θJB} | Junction-to-board thermal resistance | 92.8 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 9.2 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 91.2 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

6.6 Thermal Information: OPA4377-Q1

| THERMAL METRIC ⁽¹⁾ | | OPA4377-Q1 | UNIT |
|-------------------------------|--|------------|------|
| | | PW (TSSOP) | |
| | | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 107.8 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 29.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 52.6 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 1.5 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 51.6 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.7 Electrical Characteristics: V_S = 2.2 V to 5.5 V

At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|------------|---|------------|------------------|
| OFFSET VOLTAGE | | | | | | |
| V _{OS} | Input offset voltage | V _S = 5 V | | 0.25 | 1 | mV |
| | Input offset voltage versus temperature | At T _A = -40°C to +125°C, V _S = 2.2 V to 5.5 V, V _{CM} < (V+) - 1.3 V | | 5 | | μV/V |
| dV _{OS} /dT | Input offset voltage versus drift | At T _A = -40°C to +125°C | | 0.32 | 2 | μV/°C |
| PSRR | Input offset voltage versus power supply | At T _A = 25°C, V _S = 2.2 V to 5.5 V, V _{CM} < (V+) - 1.3 V | | 5 | 28 | μV/V |
| | Channel separation, dc (dual, quad) | | | 0.5 | | μV/V |
| INPUT BIAS CURRENT | | | | | | |
| I _{IB} | Input bias current | | | ±0.2 | ±10 | pA |
| | Input bias current versus temperature | | | See Typical Characteristics | | pA |
| I _{OS} | Input offset current | | | ±0.2 | ±10 | pA |
| NOISE | | | | | | |
| | Input voltage noise | f = 0.1 Hz to 10 Hz | | 0.8 | | μV _{PP} |
| e _n | Input voltage noise density | f = 1 kHz | | 7.5 | | nV/√Hz |
| i _n | Input current noise density | f = 1 kHz | | 2 | | fA/√Hz |
| INPUT VOLTAGE RANGE | | | | | | |
| V _{CM} | Common-mode voltage range | | (V-) - 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | (V-) < V _{CM} < (V+) - 1.3 V | 70 | 90 | | dB |
| INPUT CAPACITANCE | | | | | | |
| | Differential | | | 6.5 | | pF |
| | Common-mode | | | 13 | | pF |
| OPEN-LOOP GAIN | | | | | | |
| A _{OL} | Open-loop voltage gain | 50 mV < V _O < (V+) - 50 mV, R _L = 10 kΩ | 112 | 134 | | dB |
| | | 100 mV < V _O < (V+) - 100 mV, R _L = 2 kΩ | | 126 | | dB |
| FREQUENCY RESPONSE, V_S = 5.5 V | | | | | | |

Electrical Characteristics: $V_S = 2.2\text{ V to }5.5\text{ V}$ (continued)

 At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_{S/2}$, $V_{CM} = V_{S/2}$, and $V_{OUT} = V_{S/2}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|-----------------------------------|--|-----|---|------|------------------|
| GBW | Gain-bandwidth product | | | 5.5 | | MHz |
| SR | Slew rate | $G = +1$ | | 2 | | V/ μs |
| t_s | Settling time | At 0.1%, 2-V step, $G = +1$ | | 1.6 | | μs |
| | | At 0.01%, 2-V step, $G = +1$ | | 2 | | μs |
| | Overload recovery time | $V_{IN} \times \text{Gain} > V_S$ | | 0.33 | | μs |
| THD+N | Total harmonic distortion + noise | $V_O = 1\text{ V}_{RMS}$, $G = +1$, $f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$ | | 0.00027% | | |
| OUTPUT | | | | | | |
| | Voltage output swing from rail | At $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ | | 10 | 20 | mV |
| | | At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ | | | 40 | mV |
| I_{SC} | Short-circuit current | | | +30/-50 | | mA |
| C_{LOAD} | Capacitive load drive | | | See Typical Characteristics | | |
| R_O | Open-loop output impedance | | | 150 | | Ω |
| POWER SUPPLY | | | | | | |
| V_S | Specified voltage | | 2.2 | | 5.5 | V |
| I_Q | Quiescent current (per amplifier) | At $T_A = 25^\circ\text{C}$, $I_O = 0$, $V_S = 5.5\text{ V}$ | | 0.76 | 1.05 | mA |
| | | At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 1.2 | mA |
| TEMPERATURE | | | | | | |
| | Specified temperature | | -40 | | +125 | $^\circ\text{C}$ |

6.8 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

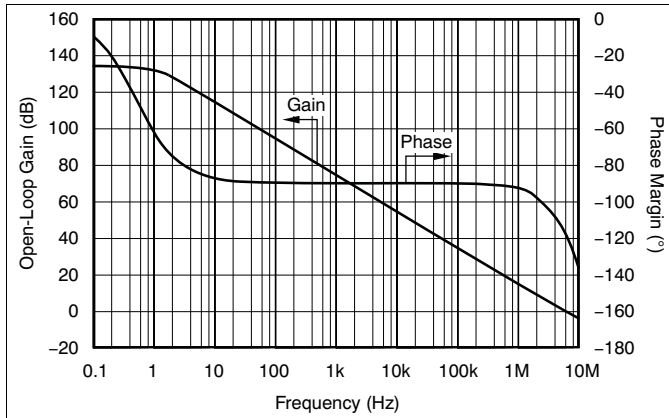


Figure 1. Open-Loop Gain and Phase vs Frequency

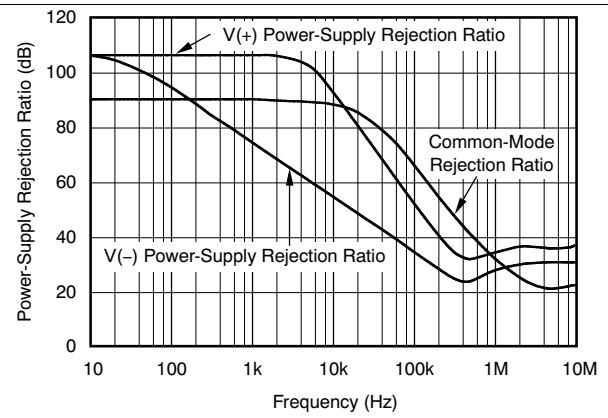


Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

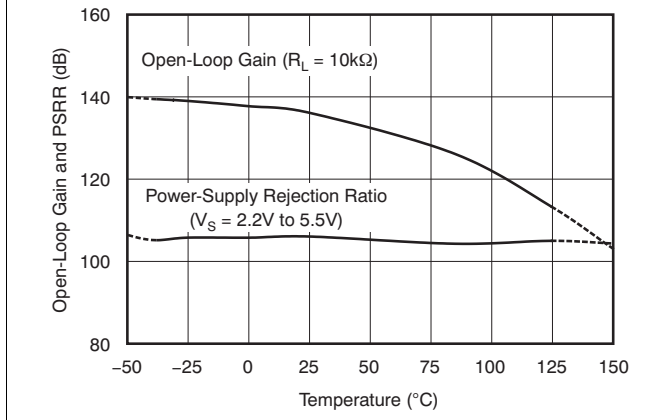


Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

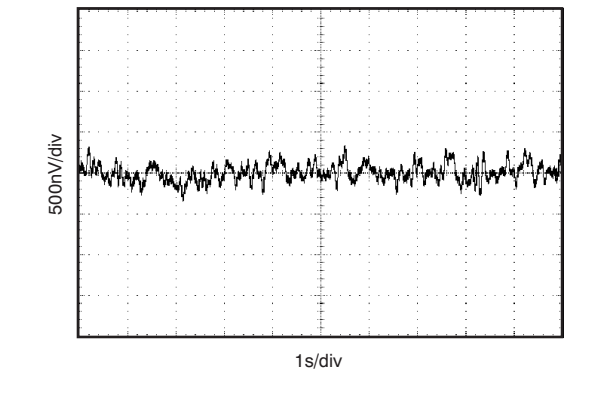


Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise

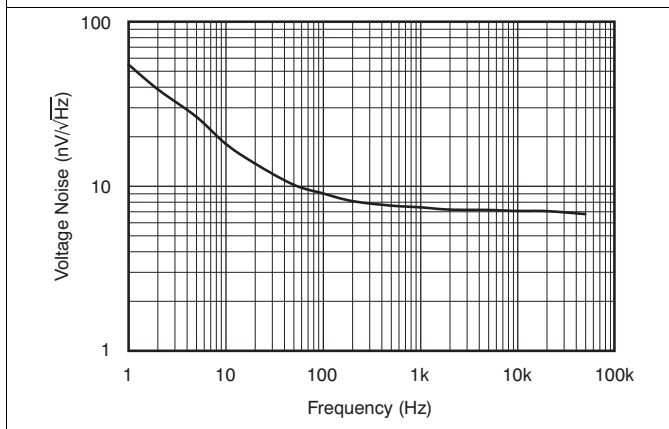


Figure 5. Input Voltage Noise Spectral Density

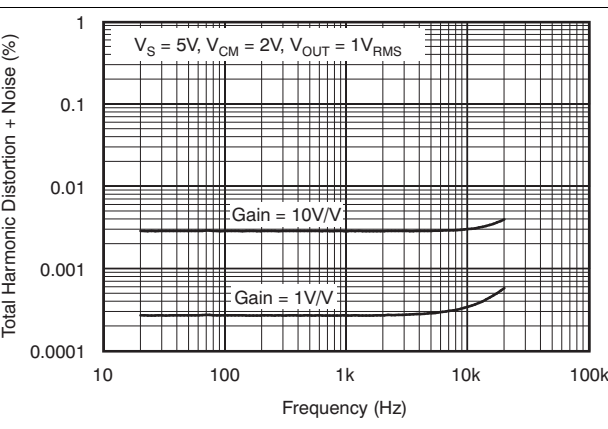


Figure 6. Total Harmonic Distortion and Noise vs Frequency

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

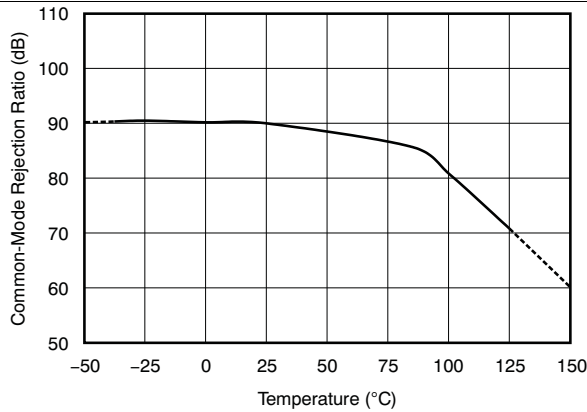


Figure 7. Common-Mode Rejection Ratio vs Temperature

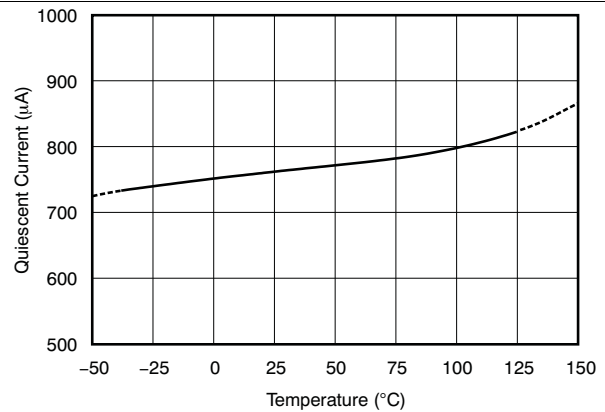


Figure 8. Quiescent Current vs Temperature

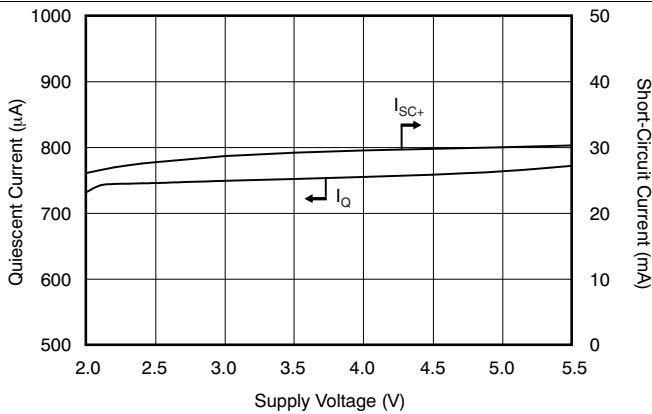


Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage

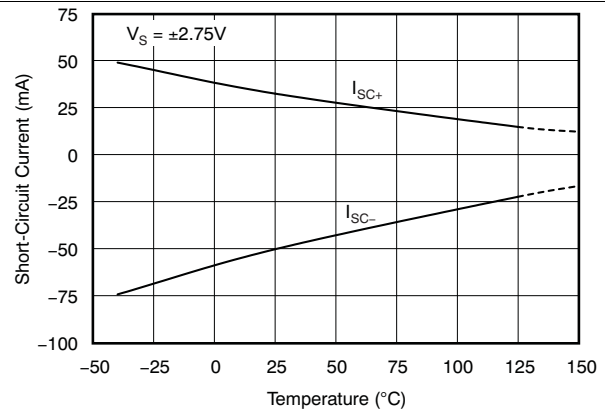


Figure 10. Short-Circuit Current vs Temperature

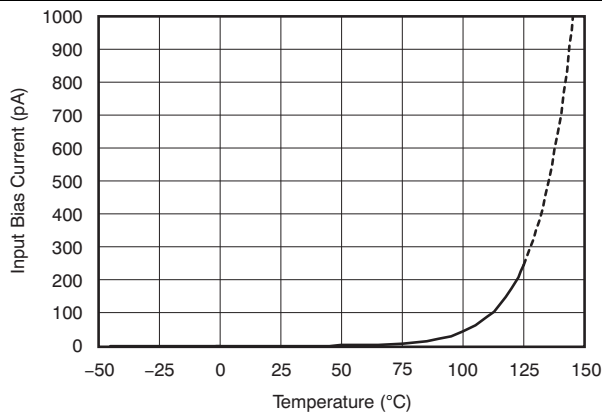


Figure 11. Input Bias Current vs Temperature

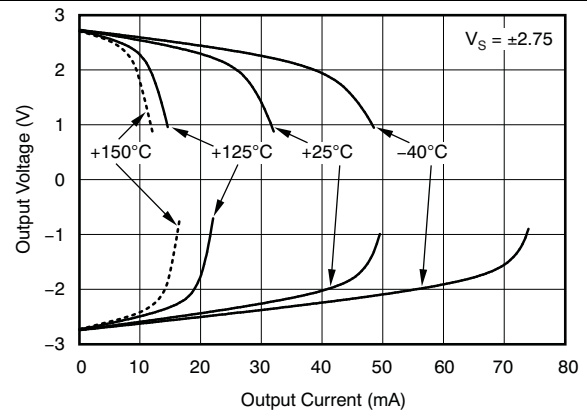


Figure 12. Output Voltage vs Output Current

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

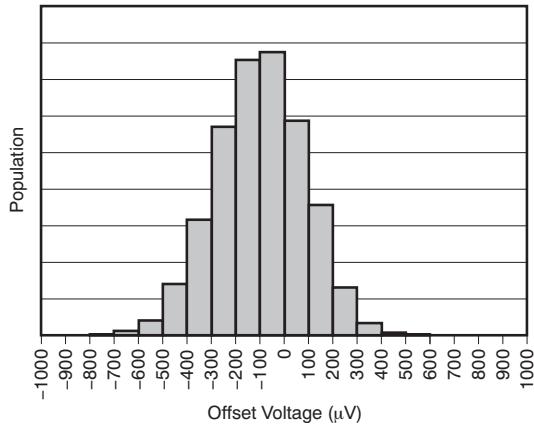


Figure 13. Offset Voltage Production Distribution

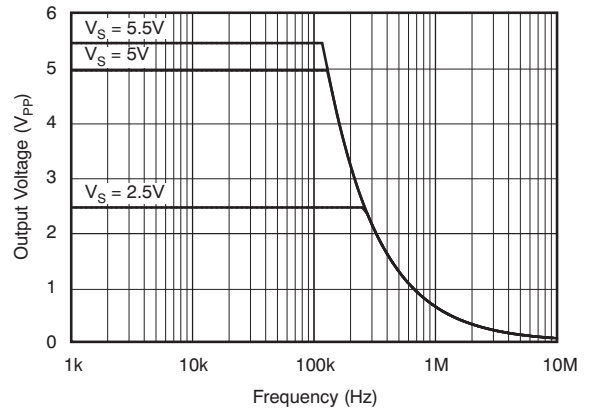


Figure 14. Maximum Output Voltage vs Frequency

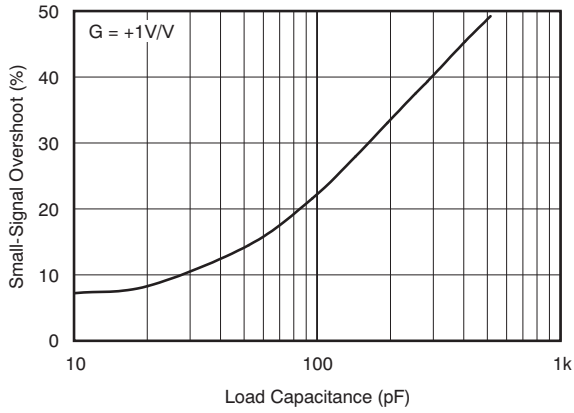


Figure 15. Small-Signal Overshoot vs Load Capacitance

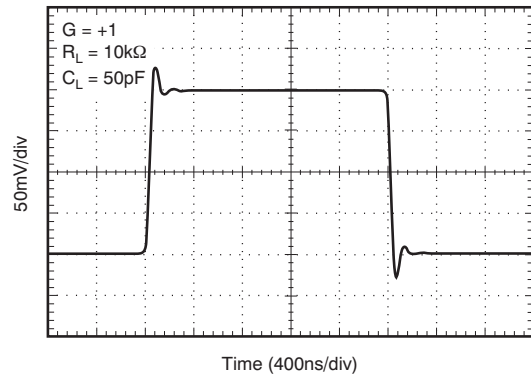


Figure 16. Small-Signal Pulse Response

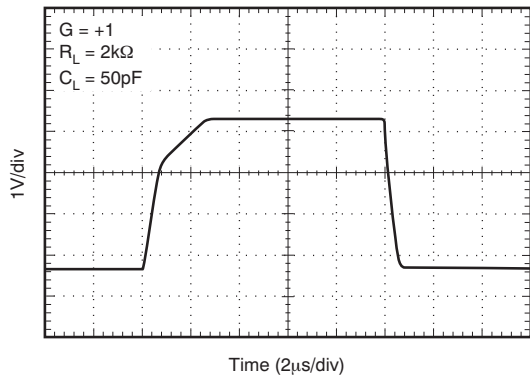


Figure 17. Large-Signal Pulse Response

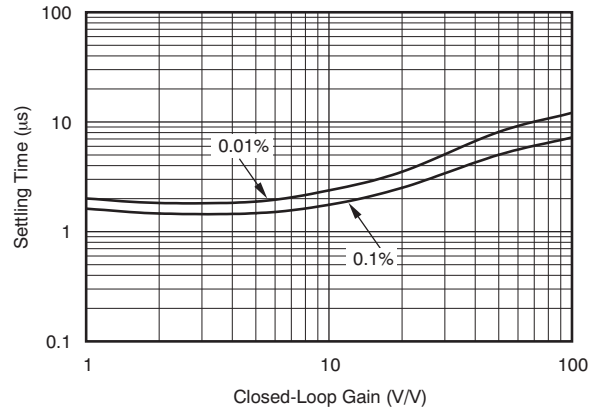


Figure 18. Settling Time vs Closed-Loop Gain

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

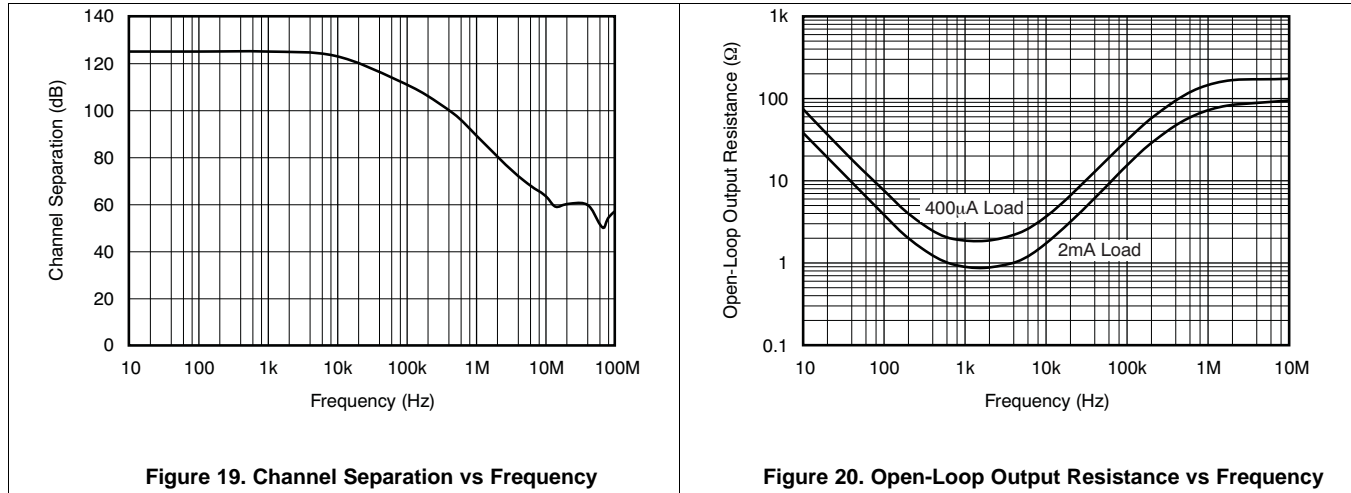


Figure 19. Channel Separation vs Frequency

Figure 20. Open-Loop Output Resistance vs Frequency

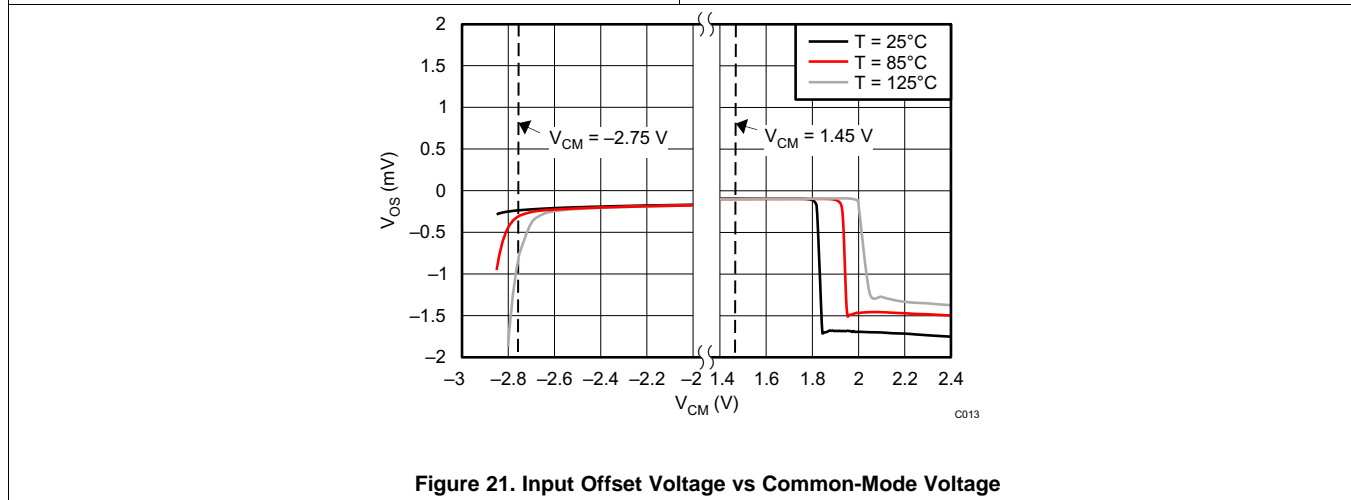


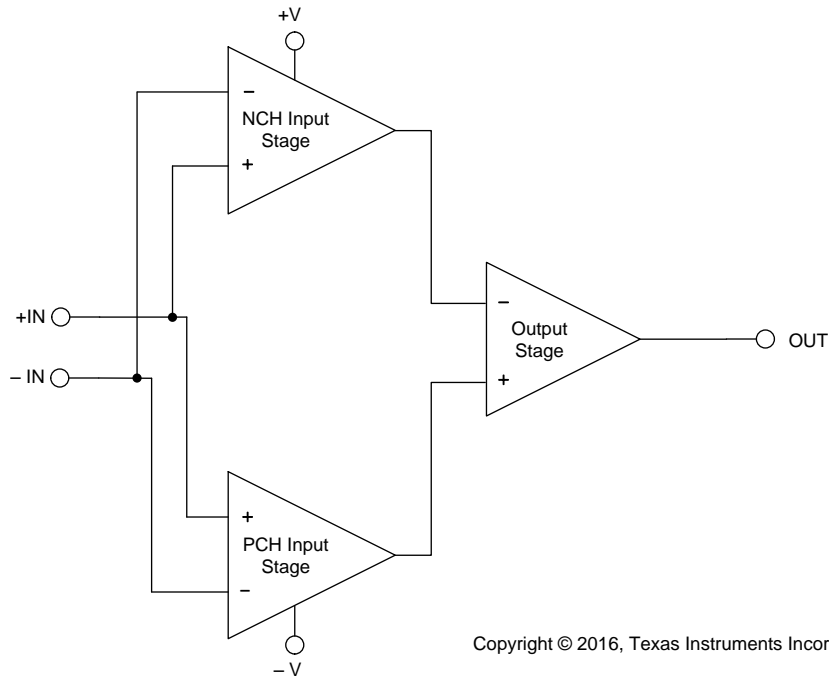
Figure 21. Input Offset Voltage vs Common-Mode Voltage

7 Detailed Description

7.1 Overview

The OPAx377-Q1 family belongs to a new generation of low-noise operational amplifiers, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery-powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx377-Q1 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (± 1.1 V to ± 2.75 V). Many of the specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx377-Q1 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is low, from approximately $(V-)$ to $(V+) - 1$ V, as shown in Figure 22. The offset voltage increases as common-mode voltage exceeds $(V+) - 1$ V. Common-mode rejection is specified from $(V-) - 1.3$ V.

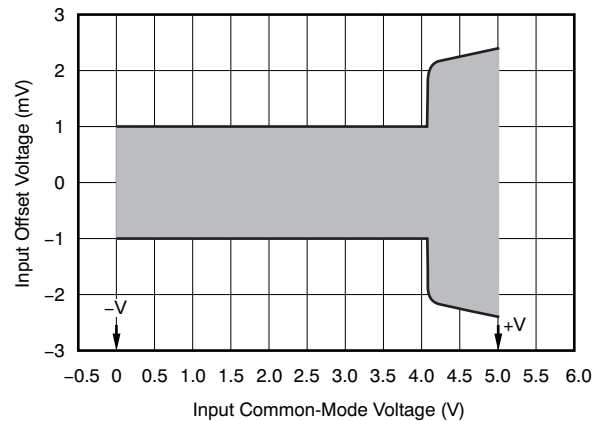
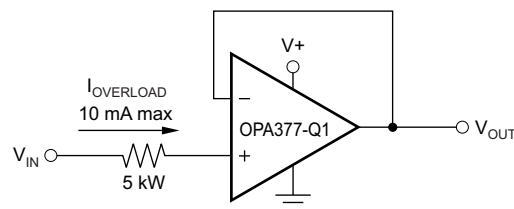


Figure 22. Offset and Common-Mode Voltage

7.3.3 Input and ESD Protection

The OPAx377-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table.

Figure 23 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.



Copyright © 2016, Texas Instruments Incorporated

Figure 23. Input Current Protection

Feature Description (continued)

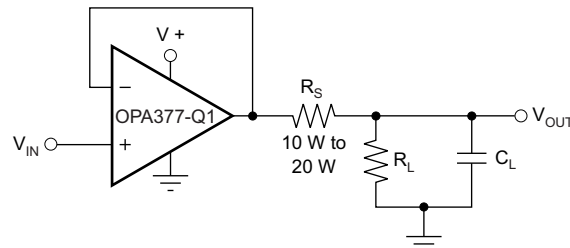
7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from the nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx377-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 75 MHz (–3 dB), with a roll-off of 20 dB per decade.

7.3.5 Capacitive Load and Stability

The OPAx377-Q1 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx377-Q1 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

The OPAx377-Q1 in a unity-gain configuration can directly drive up to 250-pF pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic plot, [Figure 15](#). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S , in series with the output, as shown in [Figure 24](#). This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S/R_L , and is generally negligible at low output current levels.



Copyright © 2016, Texas Instruments Incorporated

Figure 24. Improving Capacitive Load Drive

7.4 Device Functional Modes

The OPAx377-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (± 1.1 V). The maximum power supply voltage for the OPAx376-Q1 is 5.5 V (± 2.75 V).

8 Application and Implementation

NOTE

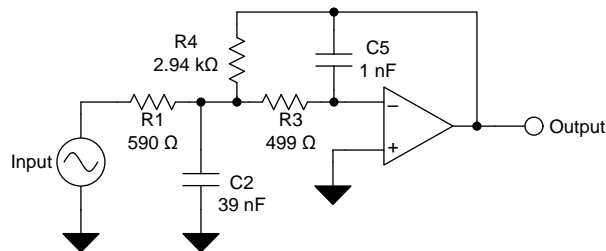
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx377-Q1 family of operational amplifiers is built on a precision analog CMOS technology featuring low noise and low offset voltage. The OPAx377-Q1 family delivers excellent offset voltage (250 μ V, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL} . These 5.5-MHz CMOS op amps operate on 760 μ A (typical) quiescent current.

8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA377-Q1 is ideally suited to construct high-speed, high-precision active filters. [Figure 25](#) shows a second-order, low-pass filter commonly encountered in signal processing applications.



Copyright © 2016, Texas Instruments Incorporated

Figure 25. Typical Application Schematic

8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in [Figure 25](#). Use [Equation 1](#) to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by [Equation 2](#):

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi} \sqrt{(1/R_3 R_4 C_2 C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. [WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Typical Application (continued)

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

8.2.3 Application Curve

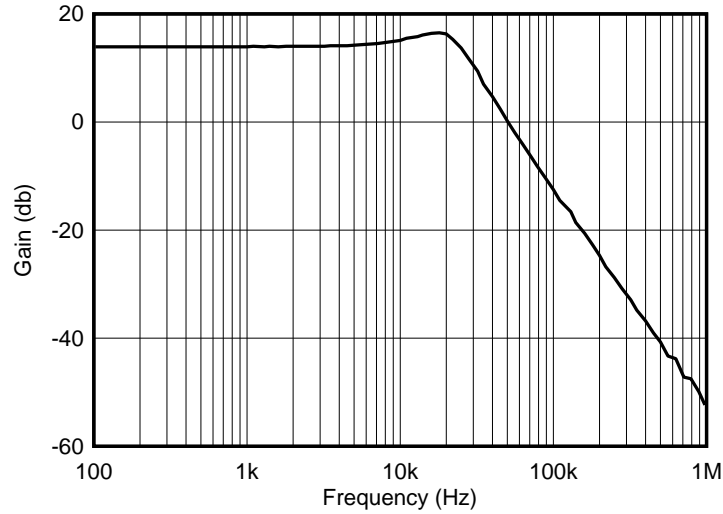


Figure 26. Low-Pass Filter Transfer Function

9 Power Supply Recommendations

The OPAx377-Q1 family of devices is specified for operation from 2.2 V to 5.5 V (± 1.1 V to ± 2.75 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to the application report, *Circuit Board Layout Techniques*, [SLOA089](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 28](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

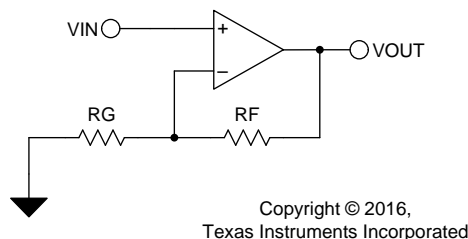
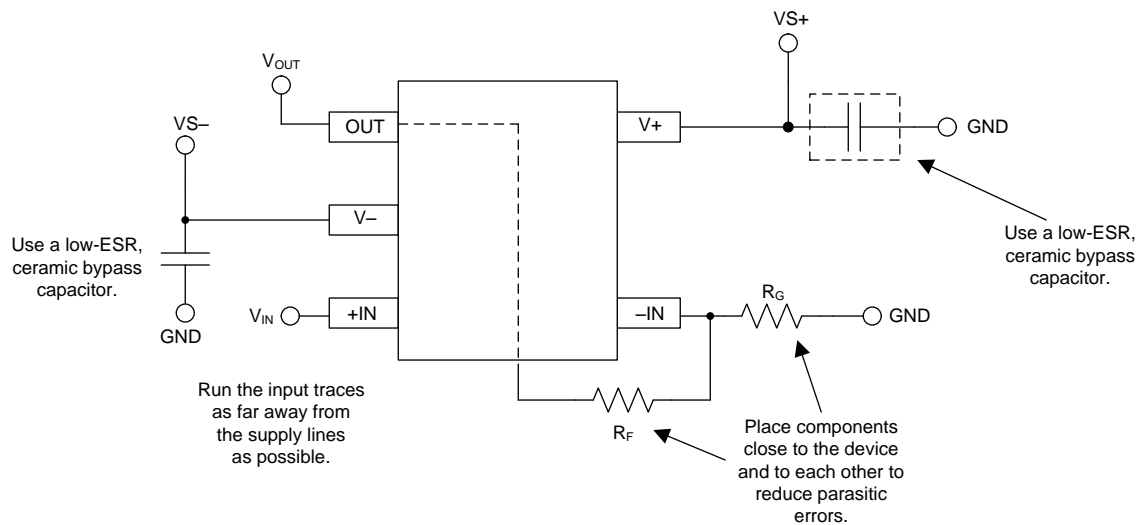


Figure 27. Typical Schematic for PCB Layout Example

Layout Example (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 28. Typical PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

11.1.1.2 DIP Adapter EVM

The [DIP Adapter EVM](#) tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Op Amp EVM

The [Universal Op Amp EVM](#) is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at <http://www.ti.com/ww/en/analog/precision-designs/>.

11.1.1.5 WEBENCH® Filter Designer

[WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques*, [SLOA089](#)
- *Operational Amplifier Gain stability, Part 3: AC Gain-Error Analysis*, [SLYT383](#)
- *Operational Amplifier Gain Stability, Part 2: DC Gain-Error Analysis*, [SLYT374](#)
- *Op Amp Performance Analysis*, [SBOS054](#)
- *Shelf-Life Evaluation of Lead-Free Component Finishes*, [SZZA046](#)
- *Single-Supply Operation of Operational Amplifiers*, [SBOA059](#)
- *Tuning in Amplifiers*, [SBOA067](#)
- *Using Infinite-Gain, MFB Filter Topology in Fully Differential Active Filters*, [SLYT343](#)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

TINA, DesignSoft are trademarks of DesignSoft, Inc.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| OPA2377QDGKRQ1 | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2377 |
| OPA2377QDGKRQ1.A | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2377 |
| OPA2377QDGKRQ1.B | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 2377 |
| OPA377QDBVRQ1 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 377Q |
| OPA377QDBVRQ1.B | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 377Q |
| OPA4377AQPWRQ1 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4377Q1 |
| OPA4377AQPWRQ1.B | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4377Q1 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2377-Q1, OPA377-Q1, OPA4377-Q1 :

- Catalog : [OPA2377](#), [OPA377](#), [OPA4377](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OPA2377QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2377QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA377QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA4377AQPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

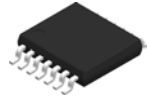
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| OPA2377QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2377QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| OPA377QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| OPA4377AQPWRQ1 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

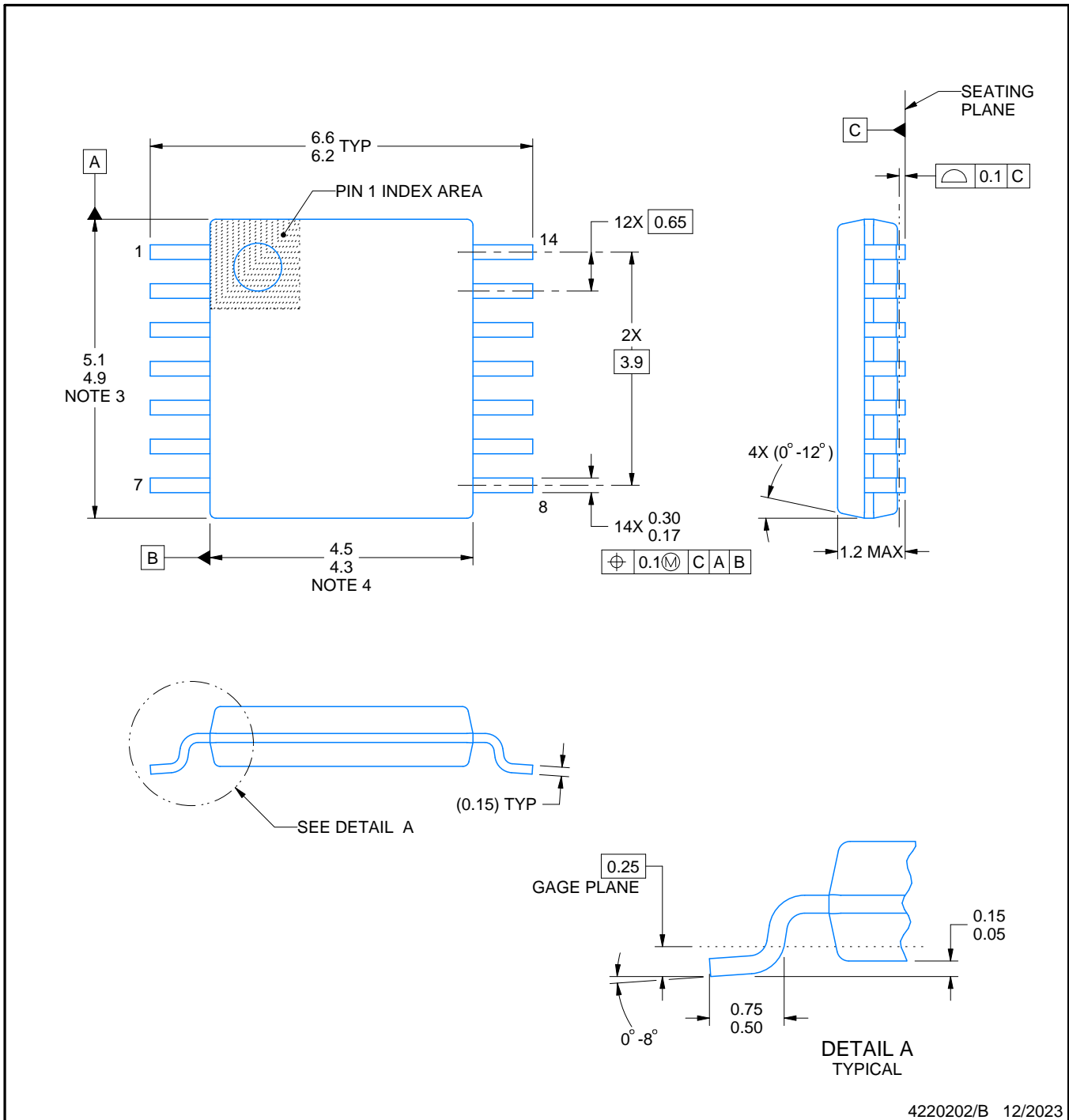
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

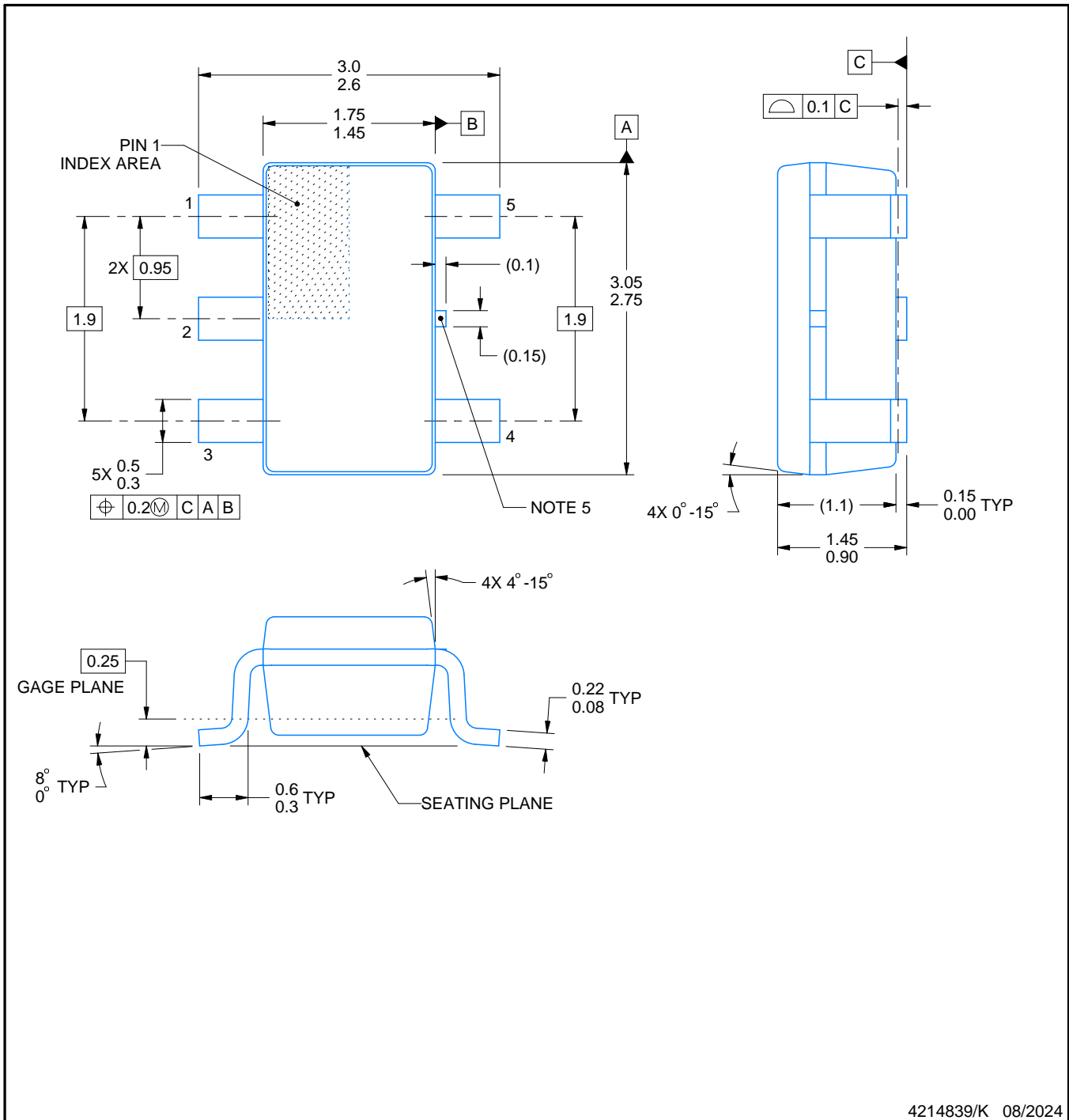
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0005A



PACKAGE OUTLINE
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

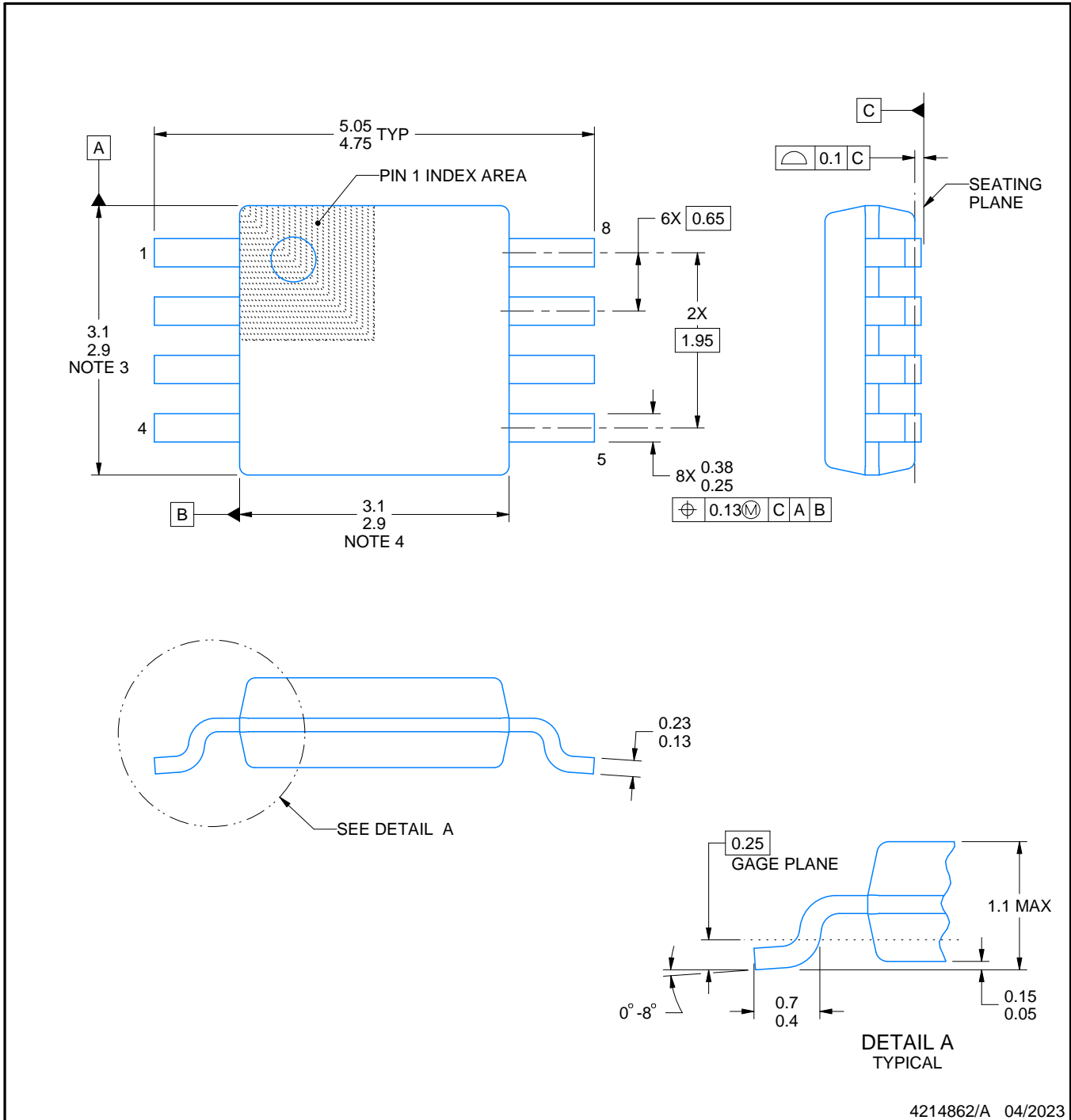
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025