

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
**BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

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**'46A, '47A, 'LS47  
feature**

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

**'48, 'LS48  
feature**

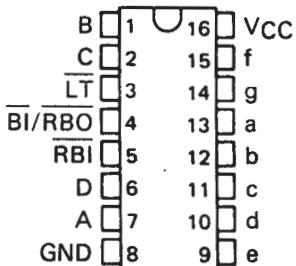
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

**'LS49  
feature**

- Open-Collector Outputs
- Blanking Input

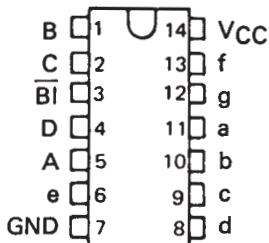
SN5446A, SN5447A, SN54LS47, SN5448,  
 SN54LS48 . . . J PACKAGE  
 SN7446A, SN7447A,  
 SN7448 . . . N PACKAGE  
 SN74LS47, SN74LS48 . . . D OR N PACKAGE

(TOP VIEW)

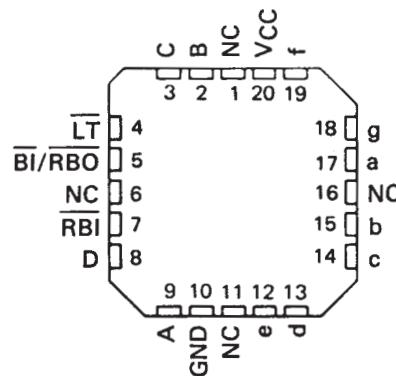


SN54LS49 . . . J OR W PACKAGE  
 SN74LS49 . . . D OR N PACKAGE

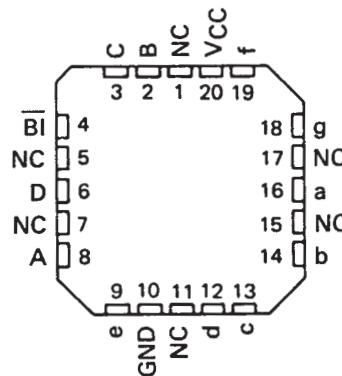
(TOP VIEW)



SN54LS47, SN54LS48 . . . FK PACKAGE  
 (TOP VIEW)



SN54LS49 . . . FK PACKAGE  
 (TOP VIEW)



NC – No internal connection

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
**BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

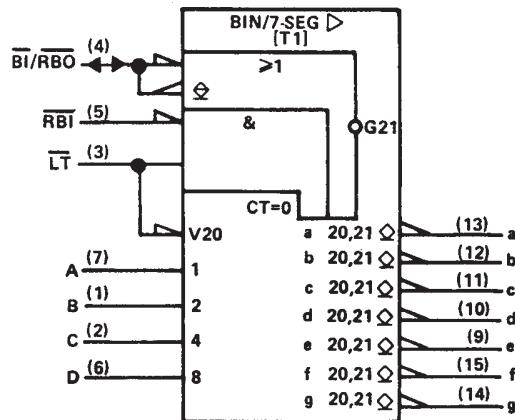
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- All Circuit Types Feature Lamp Intensity Modulation Capability

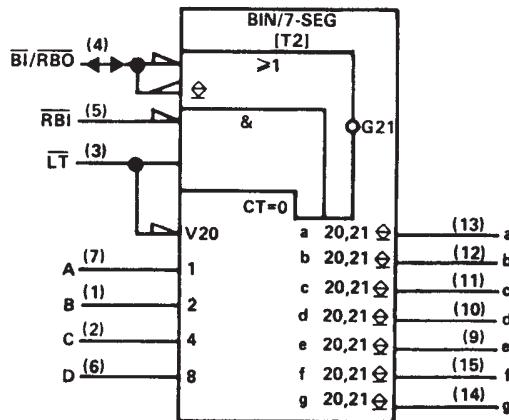
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, W
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols†

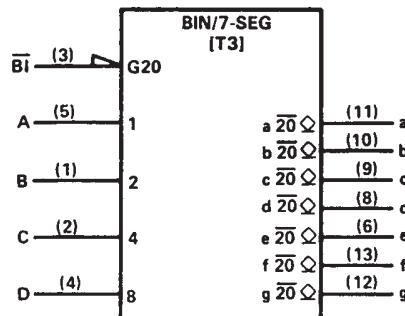
'46A, '47A, 'LS47



'48, 'LS48



'LS49



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

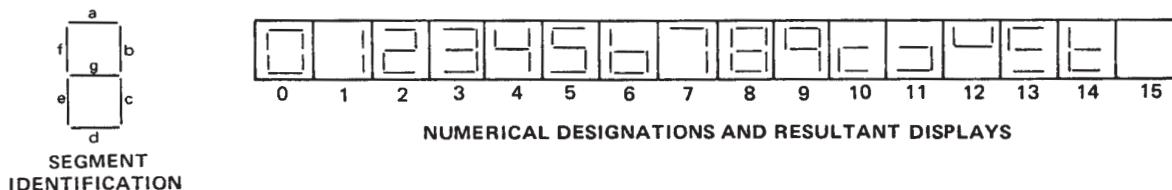
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description

The '46A, '47A, and 'LS47 feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. The '48, 'LS48, and 'LS49 feature active-high outputs for driving lamp buffers or common-cathode LEDs. All of the circuits except 'LS49 have full ripple-blanking input/output controls and a lamp test input. The 'LS49 circuit incorporates a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control ( $\overline{BI}$  and  $\overline{RBO}$ ). Lamp test ( $LT$ ) of these types may be performed at any time when the  $BI/RBO$  node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input ( $BI$ ), which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 and '247 and the SN54LS247/SN74LS247 and 'LS248 compose the  $\square$  and the  $\square$  with tails and were designed to offer the designer a choice between two indicator fonts.



H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input ( $\overline{BI}$ ) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input ( $\overline{RBI}$ ) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input ( $\overline{BI}$ ), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input ( $\overline{RBI}$ ) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output ( $\overline{RBO}$ ) goes to a low level (response condition).
4. When the blanking input/ripple blanking output ( $\overline{BI/RBO}$ ) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

<sup>†</sup> $\overline{BI/RBO}$  is wire AND logic serving as blanking input ( $\overline{BI}$ ) and/or ripple-blanking output ( $\overline{RBO}$ ).

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
 SN7446A, '747A, '48, SN74LS47, 'LS48, 'LS49  
**BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

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'48, 'LS48  
 FUNCTION TABLE (T2)

DECIMAL OR FUNCTION	INPUTS					BI/RBO <sup>†</sup>	OUTPUTS							NOTE
	LT	RBI	D	C	B	A	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	L	
1	H	X	L	L	L	H	H	L	H	H	L	L	L	
2	H	X	L	L	H	L	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	
11	H	X	H	L	H	H	H	L	L	H	H	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	
BI	X	X	X	X	X		L	L	L	L	L	L	L	2
RBI	H	L	L	L	L		L	L	L	L	L	L	L	3
LT	L	X	X	X	X		H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.  
 2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.  
 3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RB<sup>O</sup>) goes to a low level (response condition).  
 4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

<sup>†</sup>BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RB<sup>O</sup>).

'LS49  
 FUNCTION TABLE (T3)

DECIMAL OR FUNCTION	INPUTS					BI	OUTPUTS							NOTE
	D	C	B	A			a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	H	L	
1	L	L	L	H	H	L	H	H	L	L	L	L		
2	L	L	H	L	H	H	H	L	H	H	L	H		
3	L	L	H	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	H	
12	H	H	L	L	H	L	H	L	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	L	
BI	X	X	X	X		L	L	L	L	L	L	L	L	2

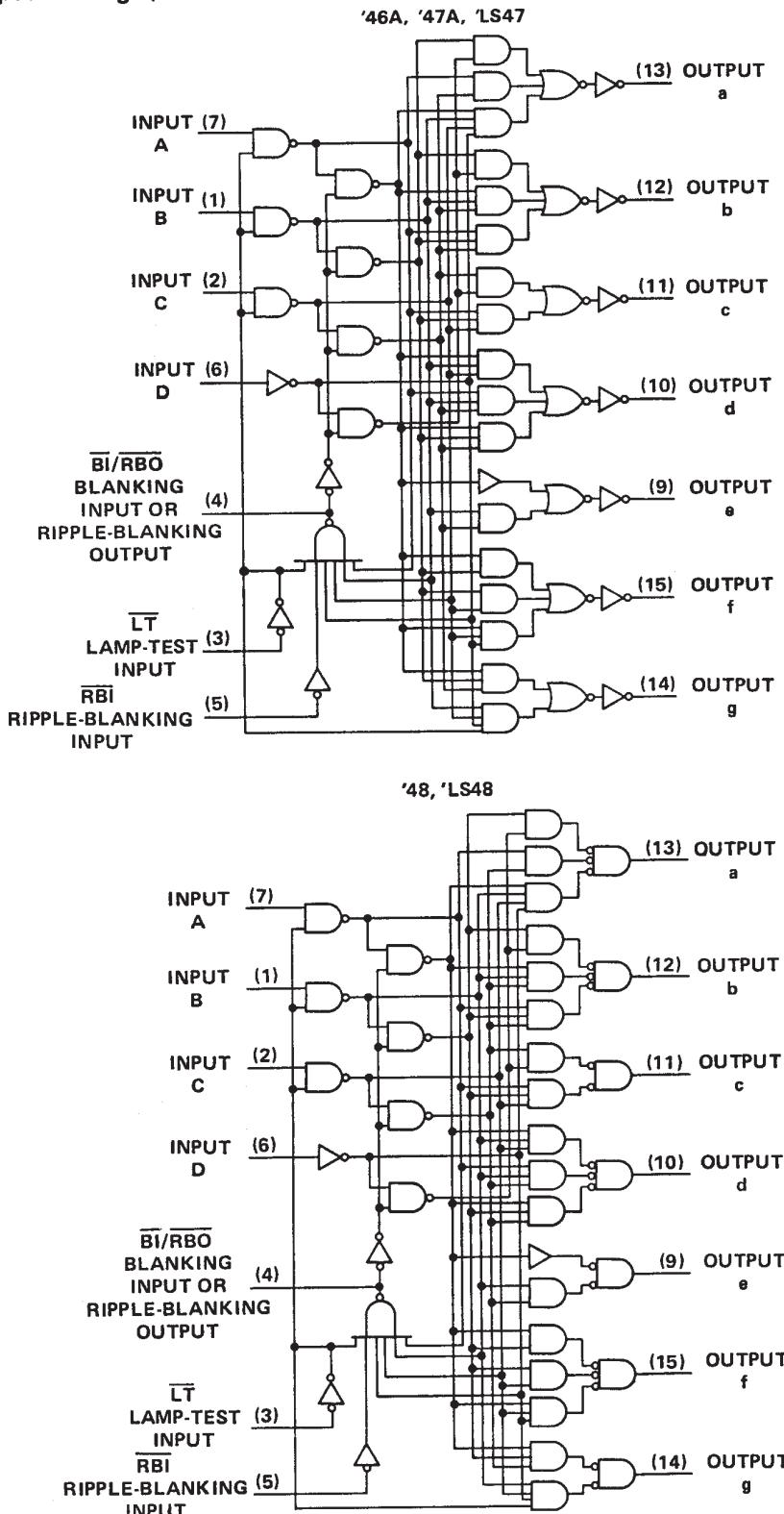
H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.  
 2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.



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logic diagrams (positive logic)

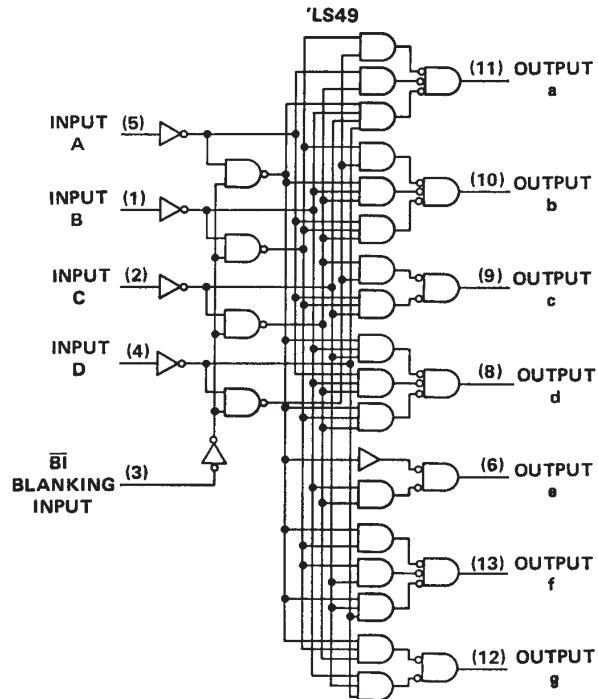


Pin numbers shown are for D, J, N, and W packages.

SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
**BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

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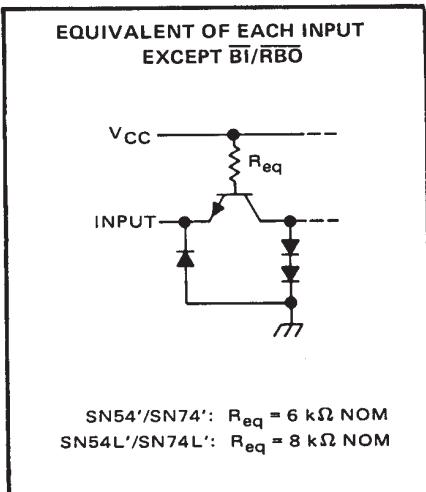
logic diagrams (continued)



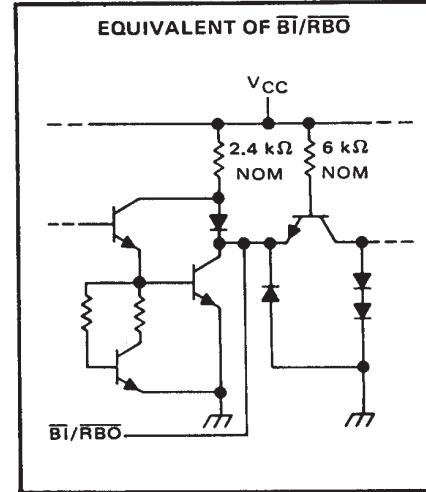
Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

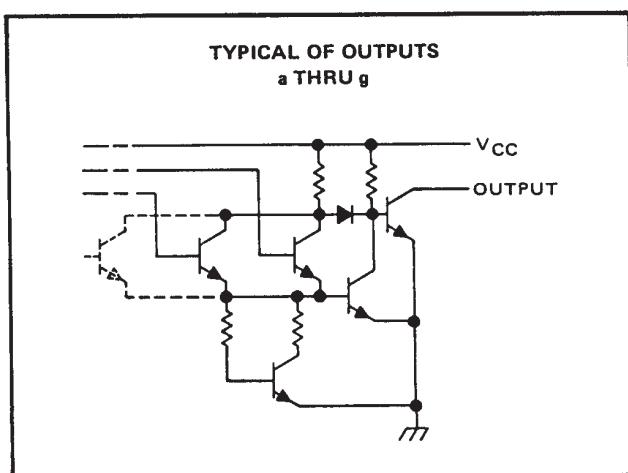
'46A, '47A, '48



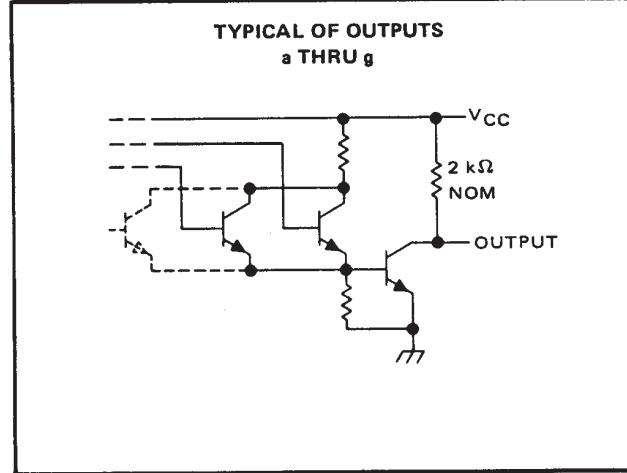
'46A, '47A, '48



'46A, '47A



'48



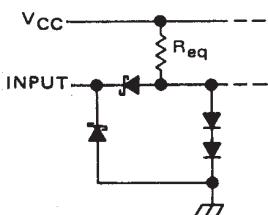
SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
**BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

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**schematics of inputs and outputs**

'LS47, 'LS48, 'LS49

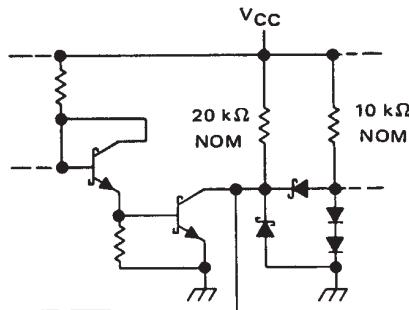
**EQUIVALENT OF EACH INPUT  
EXCEPT  $\overline{BI}/\overline{RBO}$**



$L\bar{T}$  and  $\overline{RBI}$  ('LS47, 'LS48):  $Req = 20\text{ k}\Omega$  NOM  
 $\overline{BI}$  ('LS49):  $Req = 20\text{ k}\Omega$  NOM  
 A, B, C, and D:  $Req = 25\text{ k}\Omega$  NOM

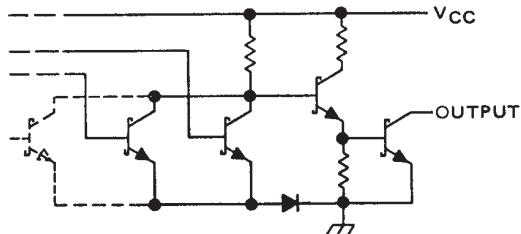
'LS47, 'LS48, 'LS49

**EQUIVALENT OF  $\overline{BI}/\overline{RBO}$**



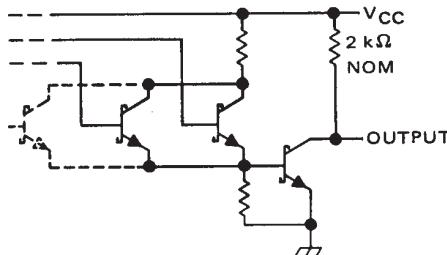
'LS47

**TYPICAL OF OUTPUTS  
a THRU g**



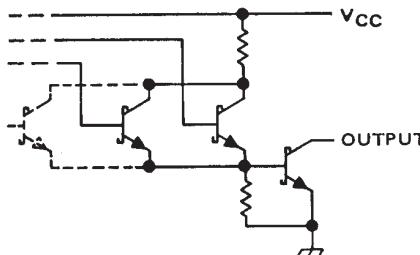
'LS48

**TYPICAL OF OUTPUTS  
a THRU g**



'LS49

**TYPICAL OF OUTPUTS  
a THRU g**



SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN5446A, SN5447A	-55°C to 125°C
SN7446A, SN7447A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5446A			SN5447A			SN7446A			SN7447A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g		30		15		30		15		15		V
On-state output current, $I_{O(on)}$	a thru g		40		40		40		40		40		mA
High-level output current, $I_{OH}$	$\bar{B}1/\bar{R}BO$		-200		-200		-200		-200		-200		μA
Low-level output current, $I_{OL}$	$\bar{B}1/\bar{R}BO$		8		8		8		8		8		mA
Operating free-air temperature, $T_A$	-55	125	-55	125	0	70	0	70	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT	
$V_{IH}$ High-level input voltage			2		V	
$V_{IL}$ Low-level input voltage			0.8		V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$		-1.5		V	
$V_{OH}$ High-level output voltage	$\bar{B}1/\bar{R}BO$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -200 \mu\text{A}$	2.4	3.7	V	
$V_{OL}$ Low-level output voltage	$\bar{B}1/\bar{R}BO$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 8 \text{ mA}$	0.27	0.4	V	
$I_{O(off)}$ Off-state output current	a thru g	$V_{CC} = \text{MAX}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $V_{O(off)} = \text{MAX}$		250	μA	
$V_{O(on)}$ On-state output voltage	a thru g	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{O(on)} = 40 \text{ mA}$	0.3	0.4	V	
$I_I$ Input current at maximum input voltage	Any input except $\bar{B}1/\bar{R}BO$	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		1	mA	
$I_{IH}$ High-level input current	Any input except $\bar{B}1/\bar{R}BO$	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$		40	μA	
$I_{IL}$ Low-level input current	Any input except $\bar{B}1/\bar{R}BO$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$		-1.6	mA	
	$\bar{B}1/\bar{R}BO$			-4		
$I_{OS}$ Short-circuit output current	$\bar{B}1/\bar{R}BO$	$V_{CC} = \text{MAX}$		-4	mA	
$I_{CC}$ Supply current		$V_{CC} = \text{MAX}$ , See Note 2	SN54'	64	85	mA
			SN74'	64	103	

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

NOTE 2:  $I_{CC}$  is measured with all outputs open and all inputs at 4.5 V.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{off}$ Turn-off time from A input	$C_L = 15 \text{ pF}$ , $R_L = 120 \Omega$ , See Note 3		100		ns
$t_{on}$ Turn-on time from A input			100		ns
$t_{off}$ Turn-off time from $\bar{B}1$ input			100		ns
$t_{on}$ Turn-on time from $\bar{B}1$ input			100		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### **recommended operating conditions**

	SN5448			SN7448			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	a thru g		-400		-400		$\mu A$
	BI/RBO		-200		-200		
Low-level output current, $I_{OL}$	a thru g		6.4		6.4		mA
	BI/RBO		8		8		
Operating free-air temperature, $T_A$	-55	125	0	0	70	0	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>		MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IH}$	High-level input voltage				2		V
$V_{IL}$	Low-level input voltage					0.8	V
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$			-1.5	V
$V_{OH}$	High-level output voltage	a thru g	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ ,	2.4	4.2		V
		$\overline{BI}/\overline{BO}$	$V_{IL} = 0.8 \text{ V}$ , $I_{OH} = \text{MAX}$	2.4	3.7		
$I_O$	Output current	a thru g	$V_{CC} = \text{MIN}$ , $V_O = 0.85 \text{ V}$ , Input conditions as for $V_{OH}$	-1.3	-2		mA
$V_{OL}$	Low-level output voltage		$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = \text{MAX}$		0.27	0.4	V
$I_I$	Input current at maximum input voltage	Any input except $\overline{BI}/\overline{BO}$	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	High-level input current	Any input except $\overline{BI}/\overline{BO}$	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40	$\mu\text{A}$
$I_{IL}$	Low-level input current	Any input except $\overline{BI}/\overline{BO}$	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-1.6	mA
		$\overline{BI}/\overline{BO}$				-4	
$I_{OS}$	Short-circuit output current	$\overline{BI}/\overline{BO}$	$V_{CC} = \text{MAX}$			-4	mA
$I_{CC}$	Supply current		$V_{CC} = \text{MAX}$ , See Note 2	SN5448	53	76	mA
				SN7448	53	90	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>†</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

NOTE 2:  $I_{CC}$  is measured with all outputs open and all inputs at 4.5 V.

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$ Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega$ See Note 3			100	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from A input				100	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from $\overline{RBI}$ input				100	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from $\overline{RBI}$ input				100	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Peak output current ( $t_W \leq 1$ ms, duty cycle $\leq 10\%$ )	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS47	-55°C to 125°C
SN74LS47	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS47			SN74LS47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_O(\text{off})$	a thru g				15		15	V
On-state output current, $I_O(\text{on})$	a thru g				12		24	mA
High-level output current, $I_{OH}$	Bi/RBO				-50		-50	μA
Low-level output current, $I_{OL}$	Bi/RBO				1.6		3.2	mA
Operating free-air temperature, $T_A$		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS47			SN74LS47			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage					0.7		0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -18$ mA				-1.5		-1.5	V
$V_{OH}$ High-level output voltage	Bi/RBO	$V_{CC} = \text{MIN}$ , $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max, $I_{OH} = -50$ μA	2.4	4.2		2.4	4.2	V
$V_{OL}$ Low-level output voltage	Bi/RBO	$V_{CC} = \text{MIN}$ , $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max	0.25	0.4	0.25	0.4		V
		$I_{OL} = 1.6$ mA			0.35	0.5		
		$I_{OL} = 3.2$ mA						
$I_{O(\text{off})}$ Off-state output current	a thru g	$V_{CC} = \text{MAX}$ , $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max, $V_O(\text{off}) = 15$ V			250		250	μA
$V_O(\text{on})$ On-state output voltage	a thru g	$V_{CC} = \text{MIN}$ , $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max	0.25	0.4	0.25	0.4		V
		$I_{O(\text{on})} = 12$ mA			0.35	0.5		
		$I_{O(\text{on})} = 24$ mA						
$I_I$ Input current at maximum input voltage		$V_{CC} = \text{MAX}$ , $V_I = 7$ V			0.1		0.1	mA
$I_{IH}$ High-level input current		$V_{CC} = \text{MAX}$ , $V_I = 2.7$ V			20		20	μA
$I_{IL}$ Low-level input current	Any input except Bi/RBO	$V_{CC} = \text{MAX}$ , $V_I = 0.4$ V			-0.4		-0.4	mA
	Bi/RBO				-1.2		-1.2	
$I_{OS}$ Short-circuit output current	Bi/RBO	$V_{CC} = \text{MAX}$	-0.3	-2	-0.3	-2		mA
$I_{CC}$ Supply current		$V_{CC} = \text{MAX}$ , See Note 2	7	13	7	13		mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

NOTE 2:  $I_{CC}$  is measured with all outputs open and all inputs at 4.5 V.

switching characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{off}$ Turn-off time from A input				100	
$t_{on}$ Turn-on time from A input				100	ns
$t_{off}$ Turn-off time from Bi/RBO input, outputs (a-f) only	$C_L = 15$ pF, $R_L = 665$ Ω, See Note 3			100	
$t_{on}$ Turn-on time from Bi/RBO input, outputs (a-f) only				100	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49  
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49  
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

	SN54LS48			SN74LS48			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	a thru g		-100		-100		$\mu A$
	$\overline{BI}/RBO$		-50		-50		
Low-level output current, $I_{OL}$	a thru g		2		6		$mA$
	$\overline{BI}/RBO$		1.6		3.2		
Operating free-air temperature, $T_A$	-55	125	0	70			$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>		SN54LS48			SN74LS48			UNIT
				MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IH</sub>	High-level input voltage				2		2			V
V <sub>IL</sub>	Low-level input voltage					0.7			0.8	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	High-level output voltage	a thru g and B <sub>I</sub> /R <sub>BO</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = MAX	2.4	4.2		2.4	4.2		V
I <sub>O</sub>	Output current	a thru g	V <sub>CC</sub> = MIN, V <sub>O</sub> = 0.85 V, Input conditions as for V <sub>OH</sub>	-1.3	-2		-1.3	-2		mA
V <sub>OL</sub>	Low-level output voltage	a thru g	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 2 mA	0.25	0.4	0.25	0.4		V
				I <sub>OL</sub> = 6 mA				0.35	0.5	
		B <sub>I</sub> /R <sub>BO</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 1.6 mA	0.25	0.4	0.25	0.4		V
				I <sub>OL</sub> = 3.2 mA				0.35	0.5	
I <sub>I</sub>	Input current at maximum input voltage	Any input except B <sub>I</sub> /R <sub>BO</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	High-level input current	Any input except B <sub>I</sub> /R <sub>BO</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	Low-level input current	Any input except B <sub>I</sub> /R <sub>BO</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
		B <sub>I</sub> /R <sub>BO</sub>				-1.2			-1.2	
I <sub>OS</sub>	Short-circuit output current	B <sub>I</sub> /R <sub>BO</sub>	V <sub>CC</sub> = MAX	-0.3	-2	-0.3	-2	-0.3	-2	mA
I <sub>CC</sub>	Supply current		V <sub>CC</sub> = MAX, See Note 2	25	38		25	38		mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

†All typical values are at  $V_{CC} = 5$  V,  $T = 25^\circ\text{C}$ .

NOTE 2:  $I_{CC}$  is measured with all outputs open and all inputs at 4.5 V.

switching characteristics.  $V_{DD} = 5$  V,  $T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $I_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}$ , $R_L = 4 \text{ k}\Omega$ , See Note 3			100	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from A input				100	
$t_{PHL}$	Propagation delay time, high-to-low-level output (a-f only) from $\overline{RBI}$ input	$C_L = 15 \text{ pF}$ , $R_L = 6 \text{ k}\Omega$ , See Note 3			100	ns
$t_{PLH}$	Propagation delay time, low-to-high-level output (a-f only) from $\overline{RBI}$ input				100	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to network ground terminal.

### **recommended operating conditions**

	SN54LS49			SN74LS49			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, $V_{OH}$			5.5			5.5	V
Low-level output current, $I_{OL}$			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS49			SN74LS49			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IH</sub>	High-level input voltage				2		2	V
V <sub>IL</sub>	Low-level input voltage					0.7		0.8 V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA			-1.5		-1.5 V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V,		250		250	μA
		V <sub>IL</sub> = V <sub>IL</sub> max,	V <sub>OH</sub> = 5.5 V					
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN,	I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4	V
		V <sub>IH</sub> = 2 V,				0.35	0.5	
		V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 8 mA					
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 7 V		0.1		0.1	mA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V		20		20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V		-0.4		-0.4	mA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX,	See Note 2	8	15	8	15	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>†</sup>All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

NOTE 2:  $I_{CC}$  is measured with all outputs open and all inputs at 4.5 V.

switching characteristics,  $V_{CC} = 5$  V,  $TA = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$	Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}$ , $R_L = 4 \text{ k}\Omega$ , See Note 3		100		ns
$t_{PLH}$	Propagation delay time, low-to-high-level output from A input			100		
$t_{PHL}$	Propagation delay time, high-to-low-level output (a-f only) from $\overline{RBI}$ input	$C_L = 15 \text{ pF}$ , $R_L = 6 \text{ k}\Omega$ , See Note 3		100		ns
$t_{PLH}$	Propagation delay time, low-to-high-level output (a-f only) from $\overline{RBI}$ input			100		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9856401QEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9856401QE A SNJ5447AJ
5962-9856401QFA	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9856401QF A SNJ5447AW
7604501EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7604501EA SNJ54LS47J
SN5447AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5447AJ
SN5447AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5447AJ
SN54LS47J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS47J
SN54LS47J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS47J
SN54LS49J	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS49J
SN54LS49J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS49J
SN7447AN	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN7447AN
SN7447AN.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN7447AN
SN7447ANE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN7447AN
SN74LS47D	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS47
SN74LS47D.A	Active	Production	SOIC (D)   16	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS47
SN74LS47DR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	LS47
SN74LS47DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS47
SN74LS47N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS47N
SN74LS47N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS47N
SN74LS47NE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS47N
SN74LS47NSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS47
SN74LS47NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS47
SNJ5447AJ	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9856401QE A SNJ5447AJ

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ5447AJ.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9856401QE A SNJ5447AJ
<a href="#">SNJ5447AW</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9856401QF A SNJ5447AW
SNJ5447AW.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9856401QF A SNJ5447AW
<a href="#">SNJ54LS47FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 47FK
SNJ54LS47FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 47FK
<a href="#">SNJ54LS47J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7604501EA SNJ54LS47J
SNJ54LS47J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7604501EA SNJ54LS47J
<a href="#">SNJ54LS49J</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS49J
SNJ54LS49J.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS49J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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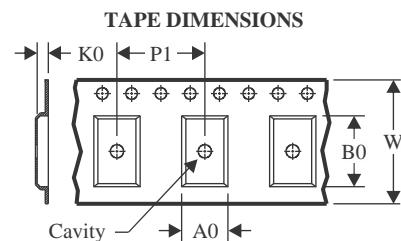
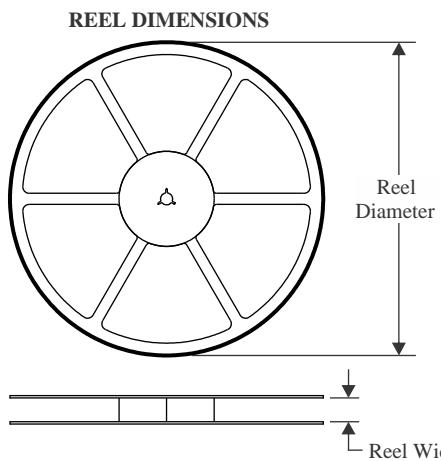
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN5447A, SN54LS47, SN7447A, SN74LS47 :**

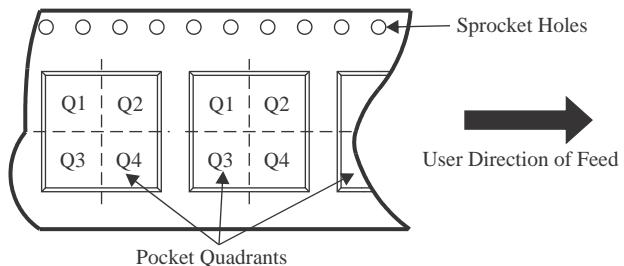
- Catalog : [SN7447A](#), [SN74LS47](#)
- Military : [SN5447A](#), [SN54LS47](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

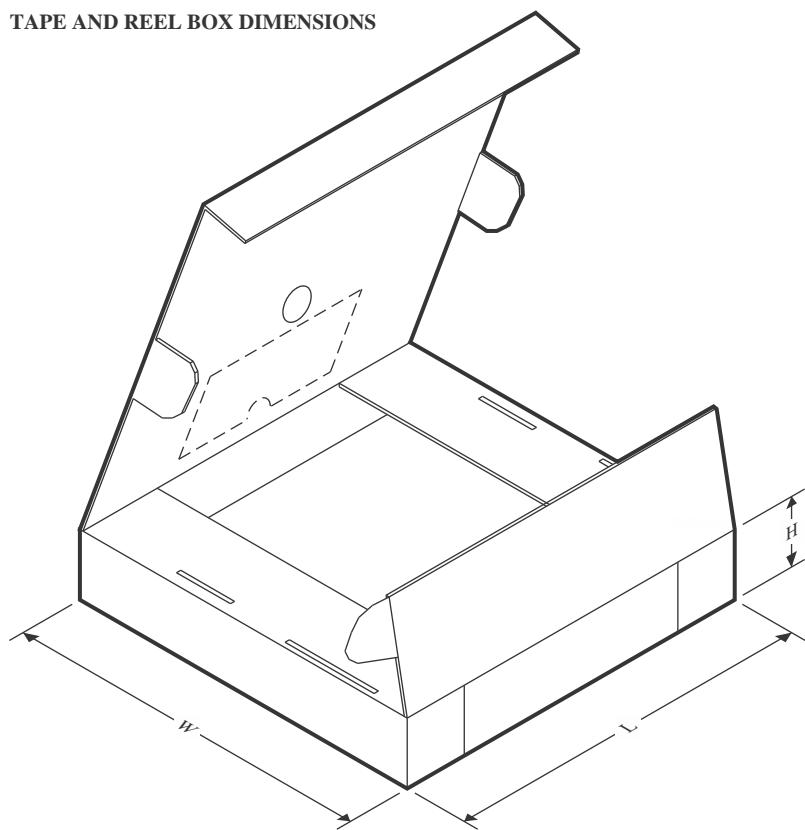
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


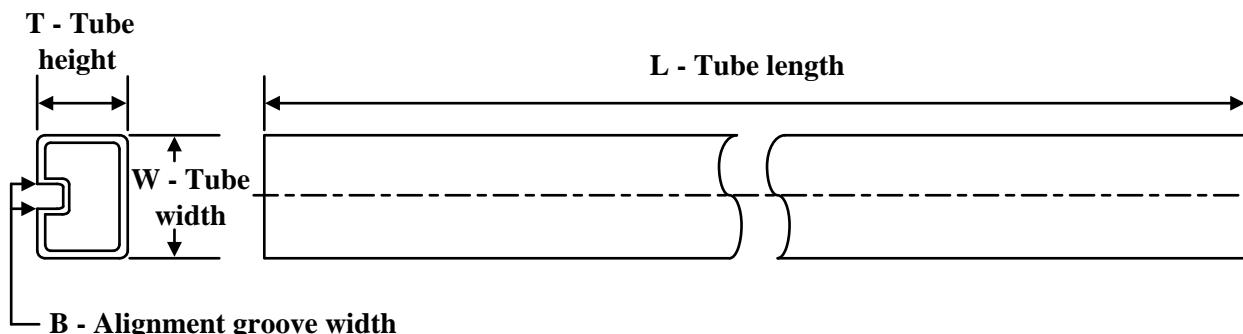
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS47DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS47NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS47DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LS47NSR	SOP	NS	16	2000	353.0	353.0	32.0

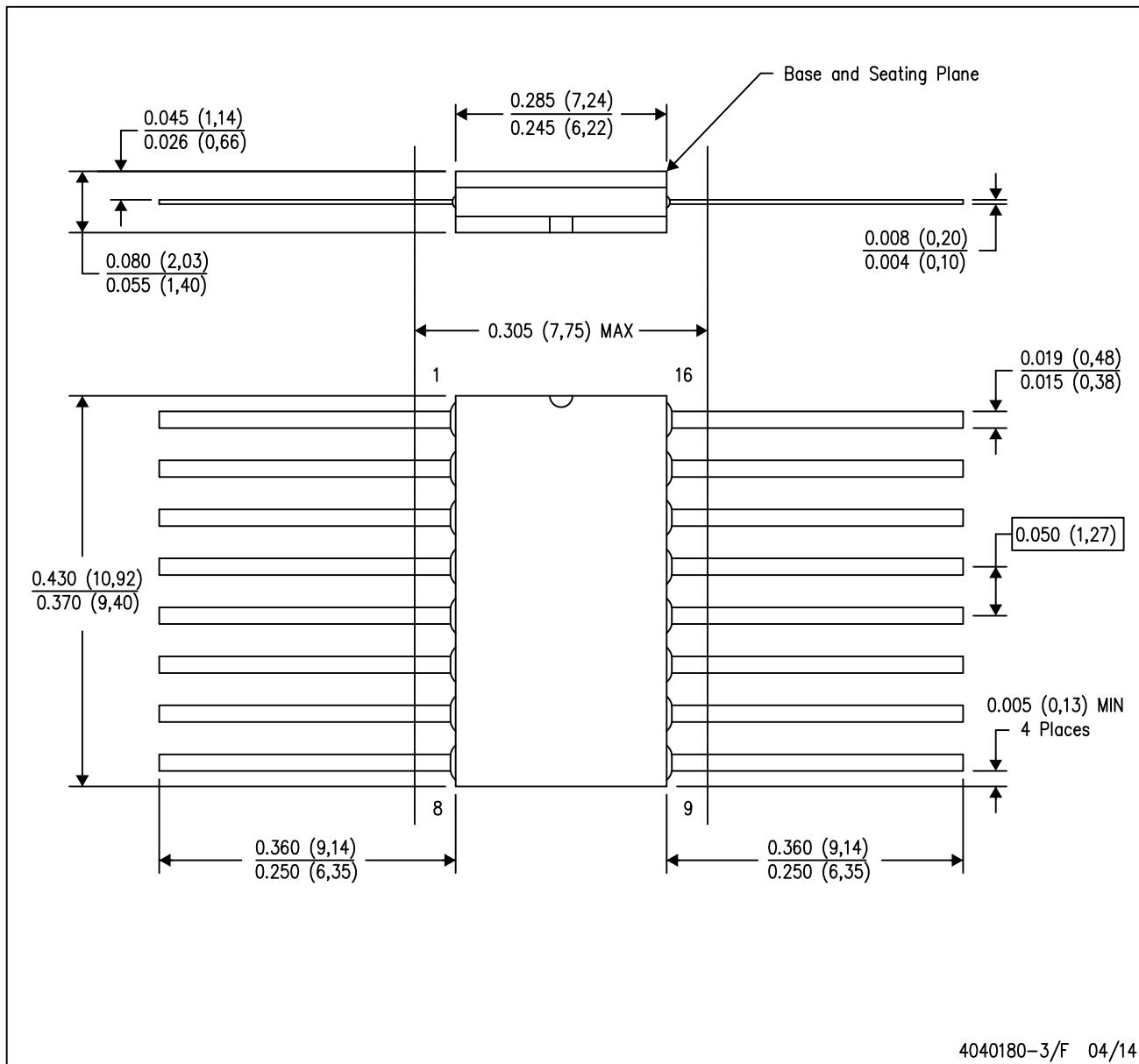
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9856401QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN7447AN	N	PDIP	16	25	506	13.97	11230	4.32
SN7447AN	N	PDIP	16	25	506	13.97	11230	4.32
SN7447AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN7447AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN7447ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN7447ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47D	D	SOIC	16	40	507	8	3940	4.32
SN74LS47D.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS47N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ5447AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ5447AW.A	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS47FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS47FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL-STD 1835 GDFP2-F16

# GENERIC PACKAGE VIEW

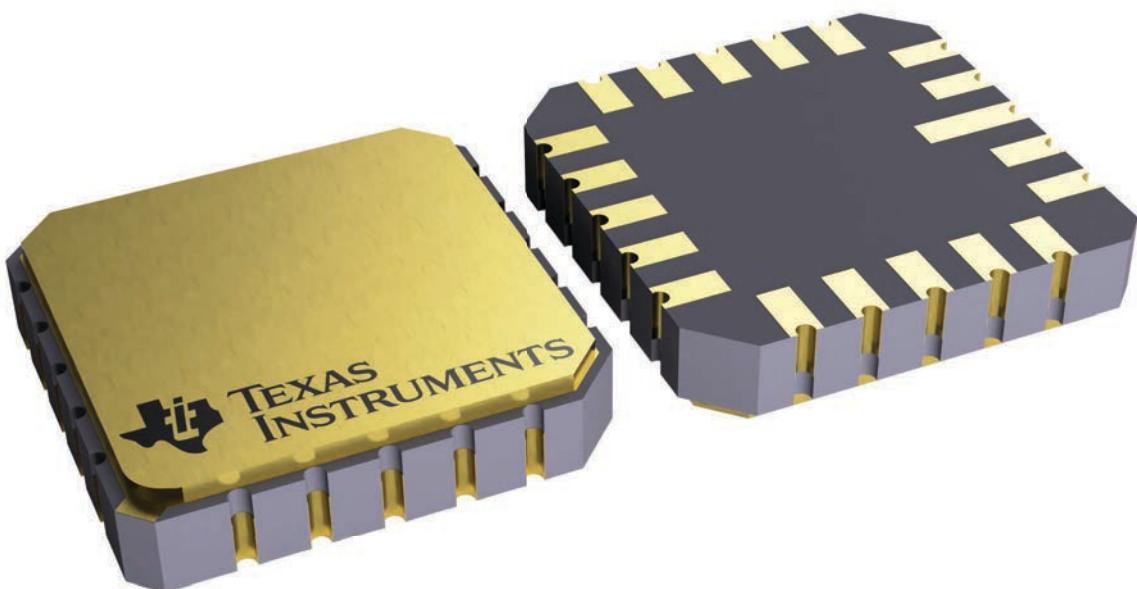
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

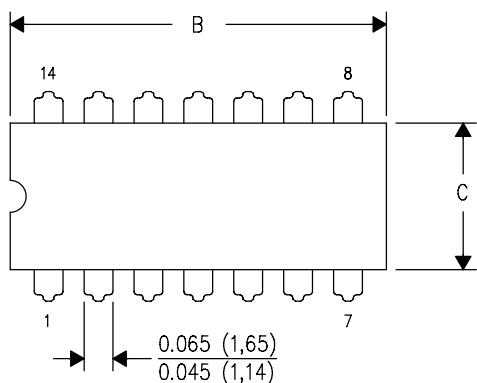


4229370VA\

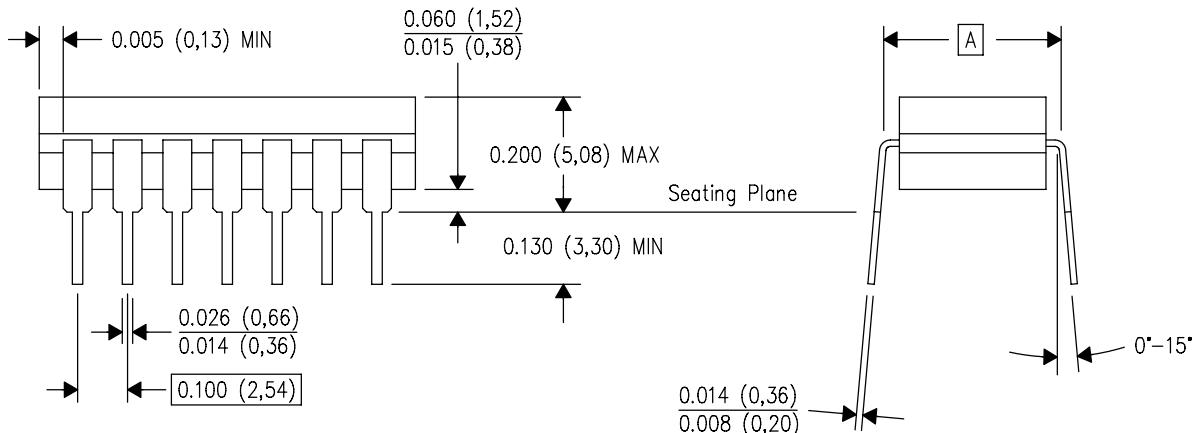
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

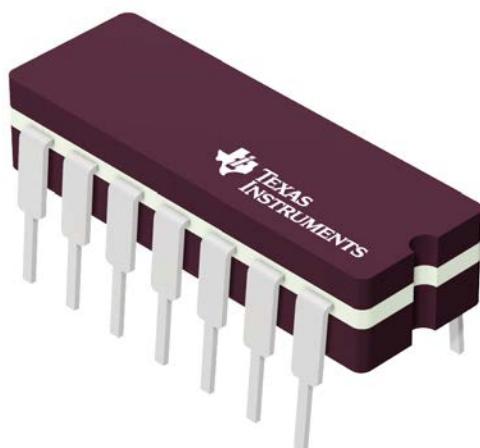
- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# GENERIC PACKAGE VIEW

**J 14**

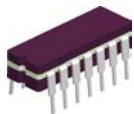
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

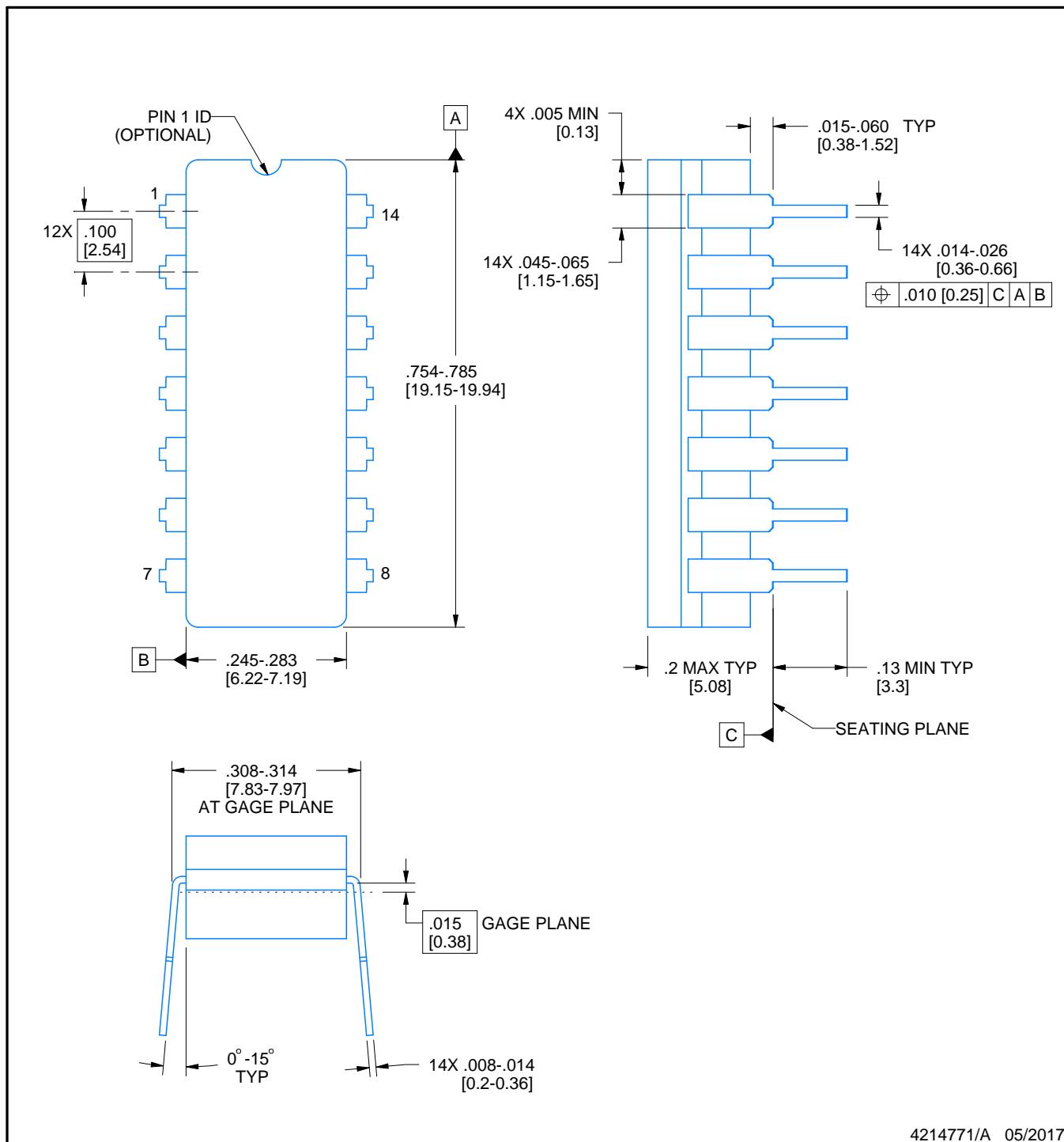


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

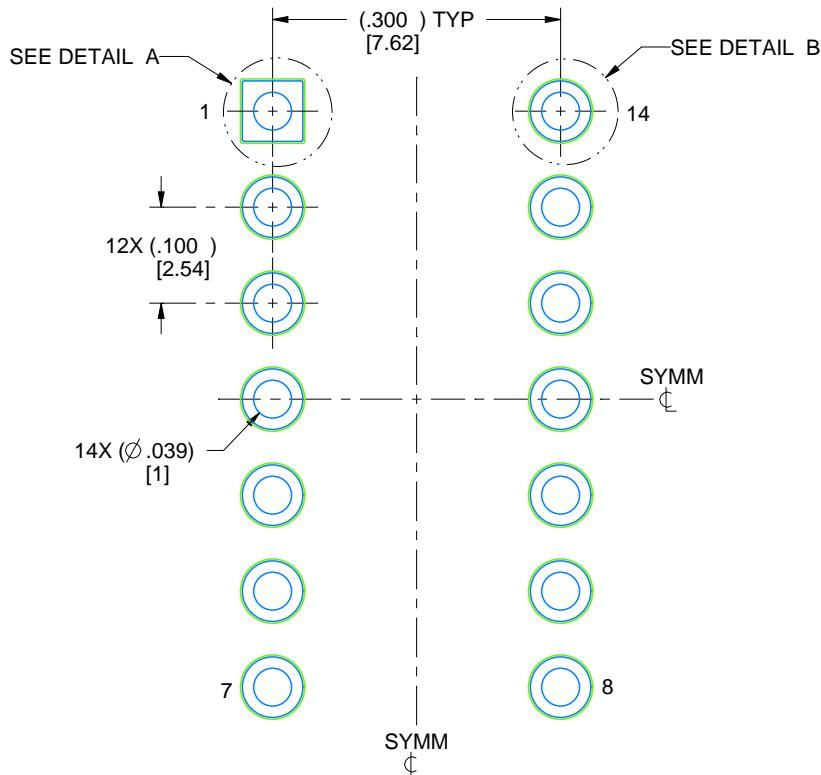
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

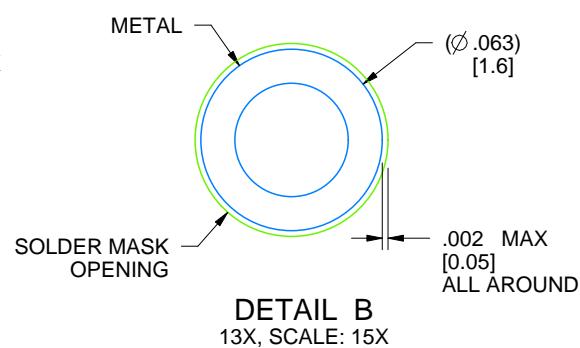
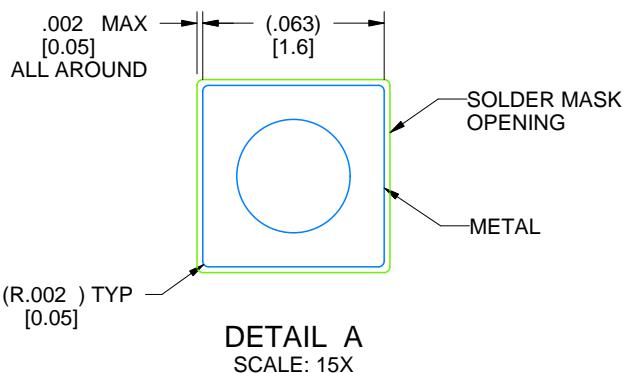
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

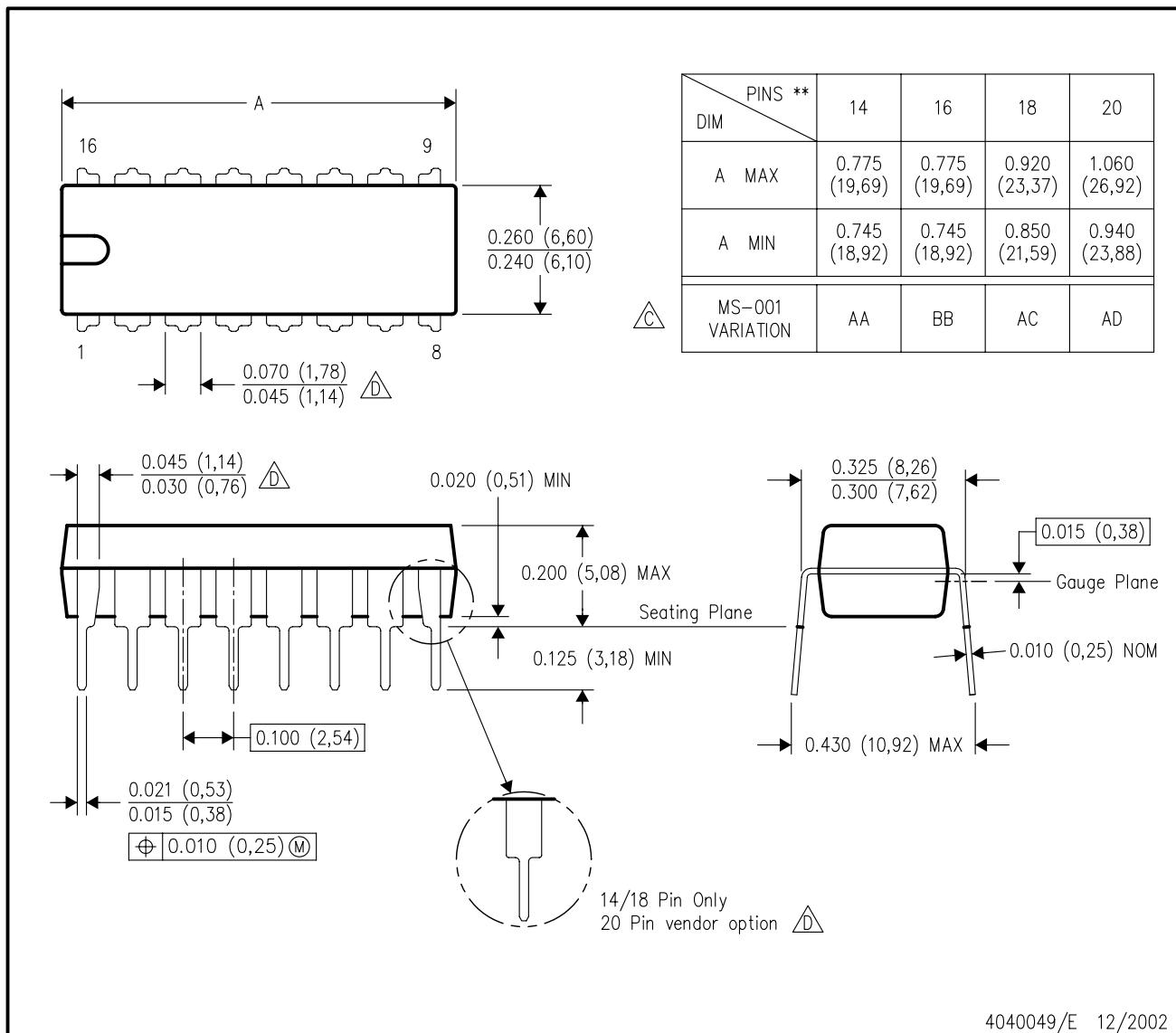


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

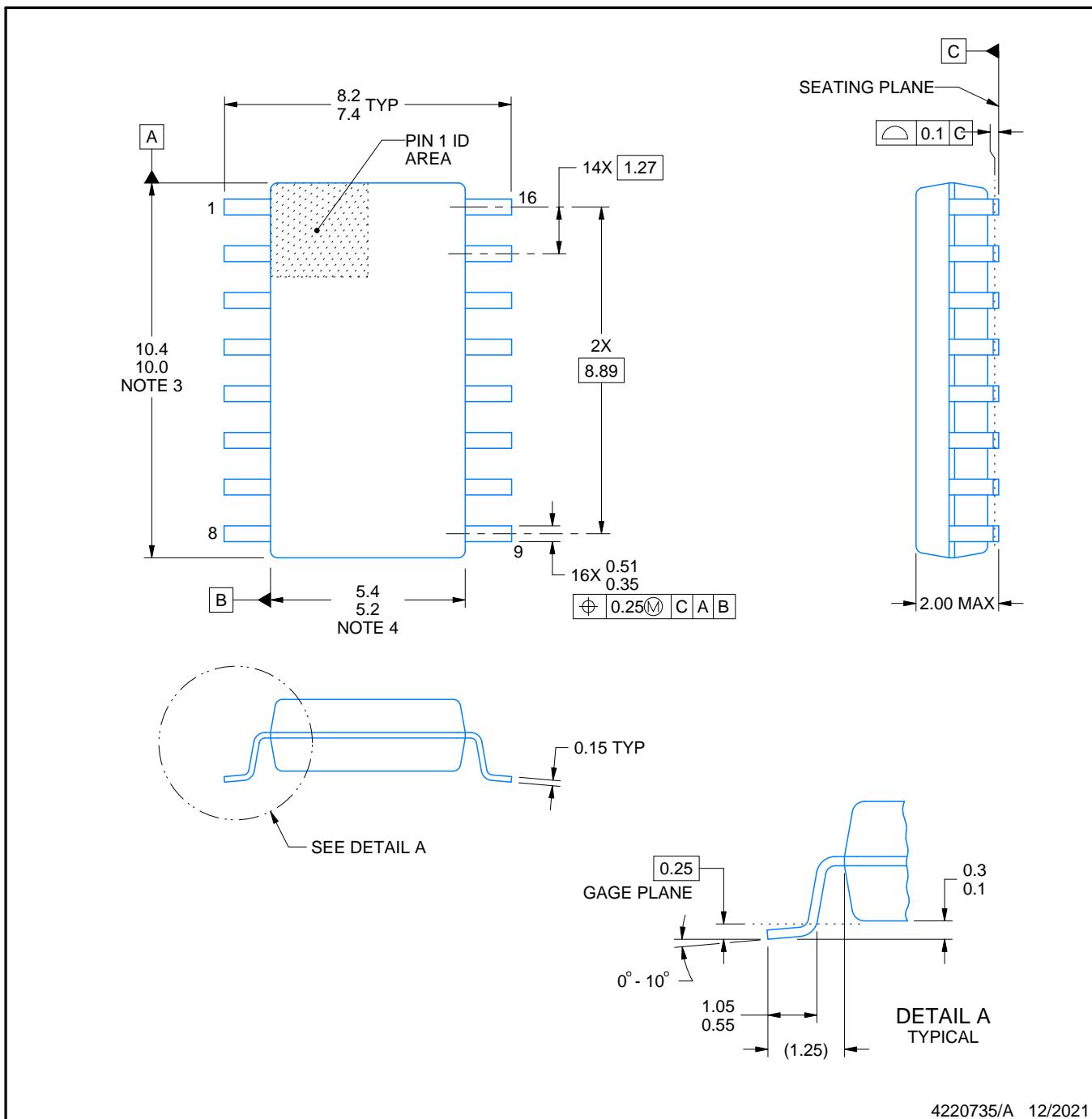
△ The 20 pin end lead shoulder width is a vendor option, either half or full width.



# PACKAGE OUTLINE

## SOP - 2.00 mm max height

SOP



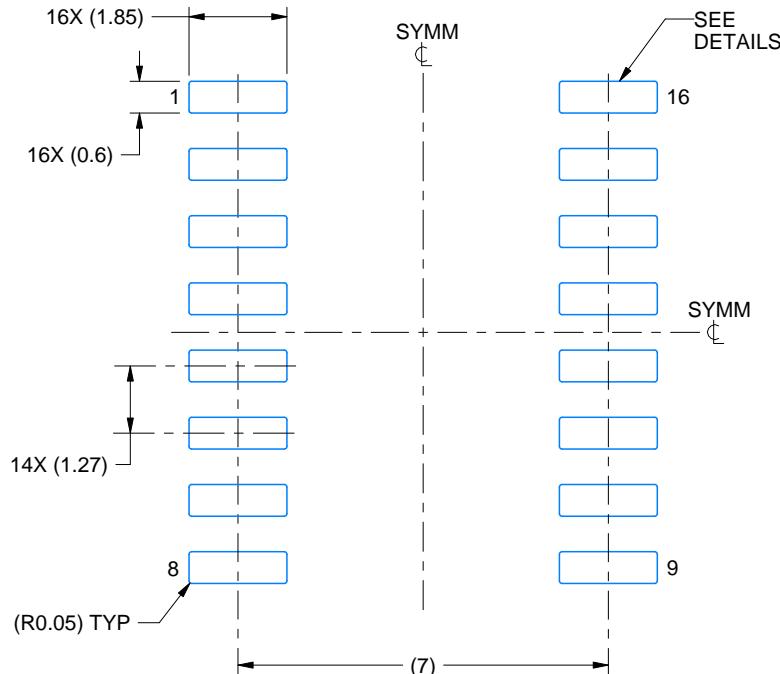
4220735/A 12/2021

# EXAMPLE BOARD LAYOUT

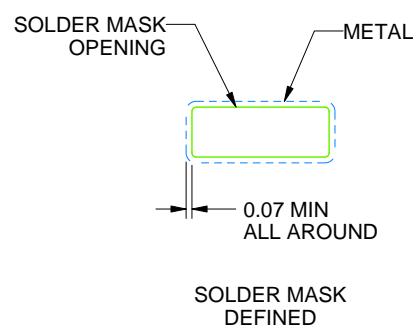
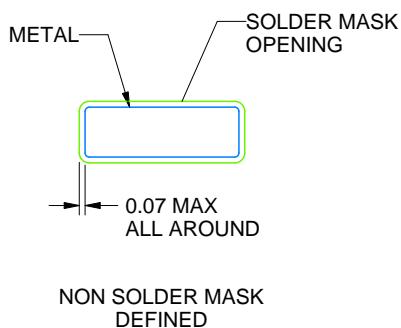
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

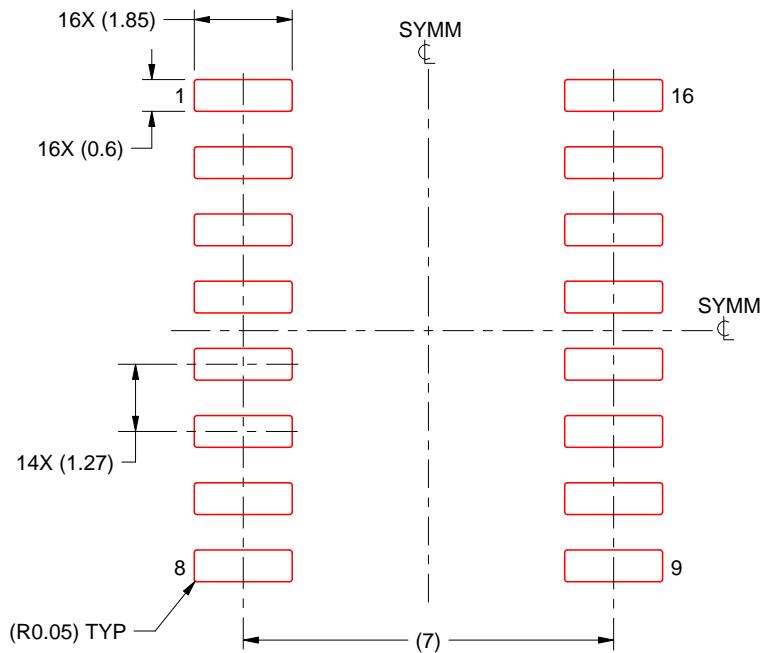
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

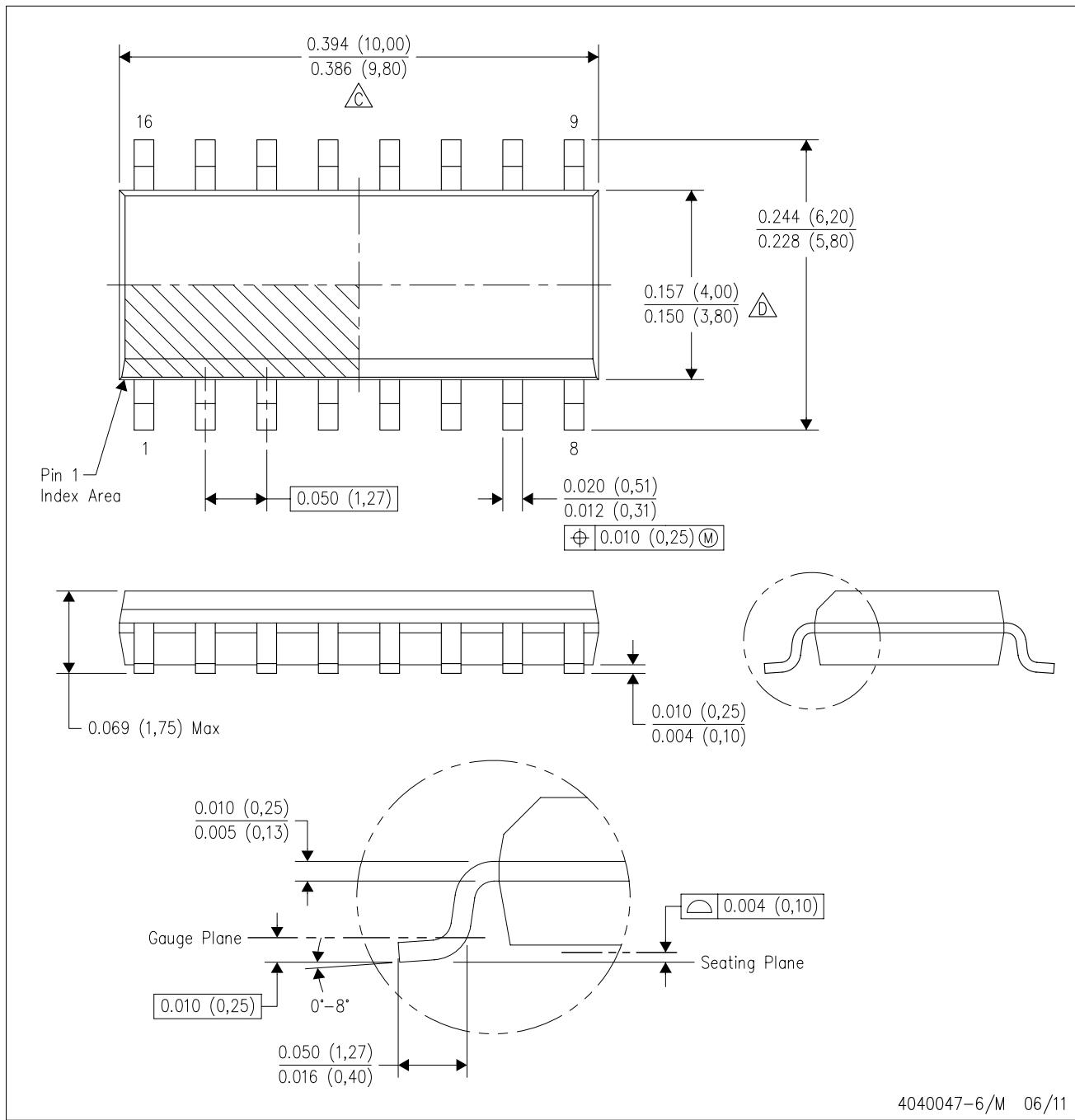
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

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