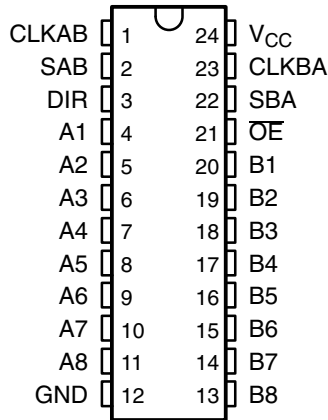


SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

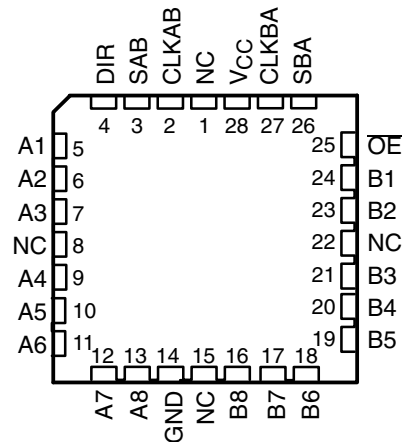
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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54BCT646 . . . JT OR W PACKAGE
SN74BCT646 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'BCT646 devices.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – NT	Tube	SN74BCT646NT	BCT646
	SOIC – DW	Tube	SN74BCT646DW	
		Tape and reel	SN74BCT646DWR	
–55°C to 125°C	CDIP – JT	Tube	SNJ54BCT646JT	SNJ54BCT646JT
	CFP – W	Tube	SNJ54BCT646W	SNJ54BCT646W
	LCCC – FK	Tube	SNJ54BCT646FK	SNJ54BCT646FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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description/ordering information(continued)

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

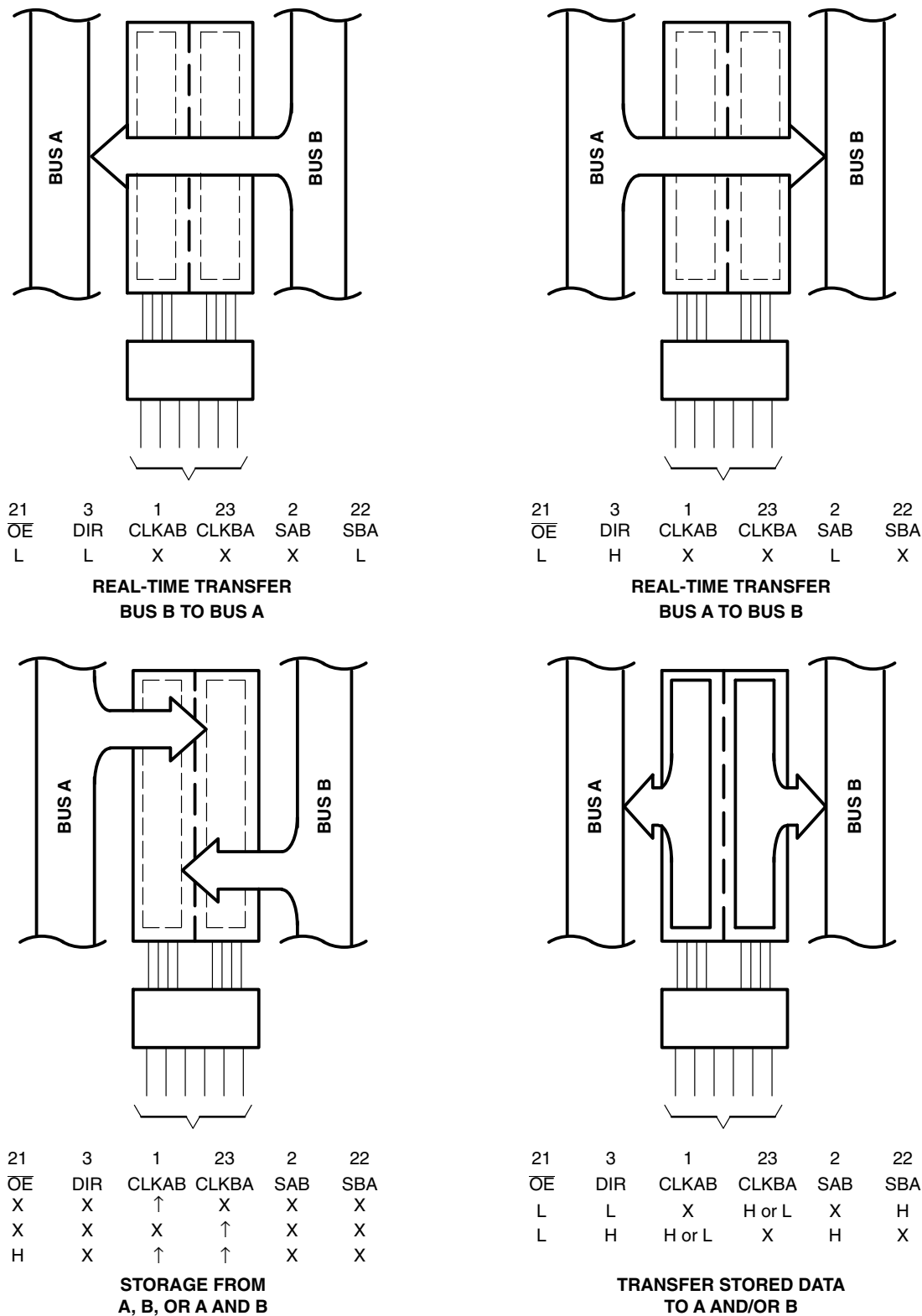
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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Pin numbers shown are for the DW, JT, NT, and W packages.

Figure 1. Bus-Management Functions



SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

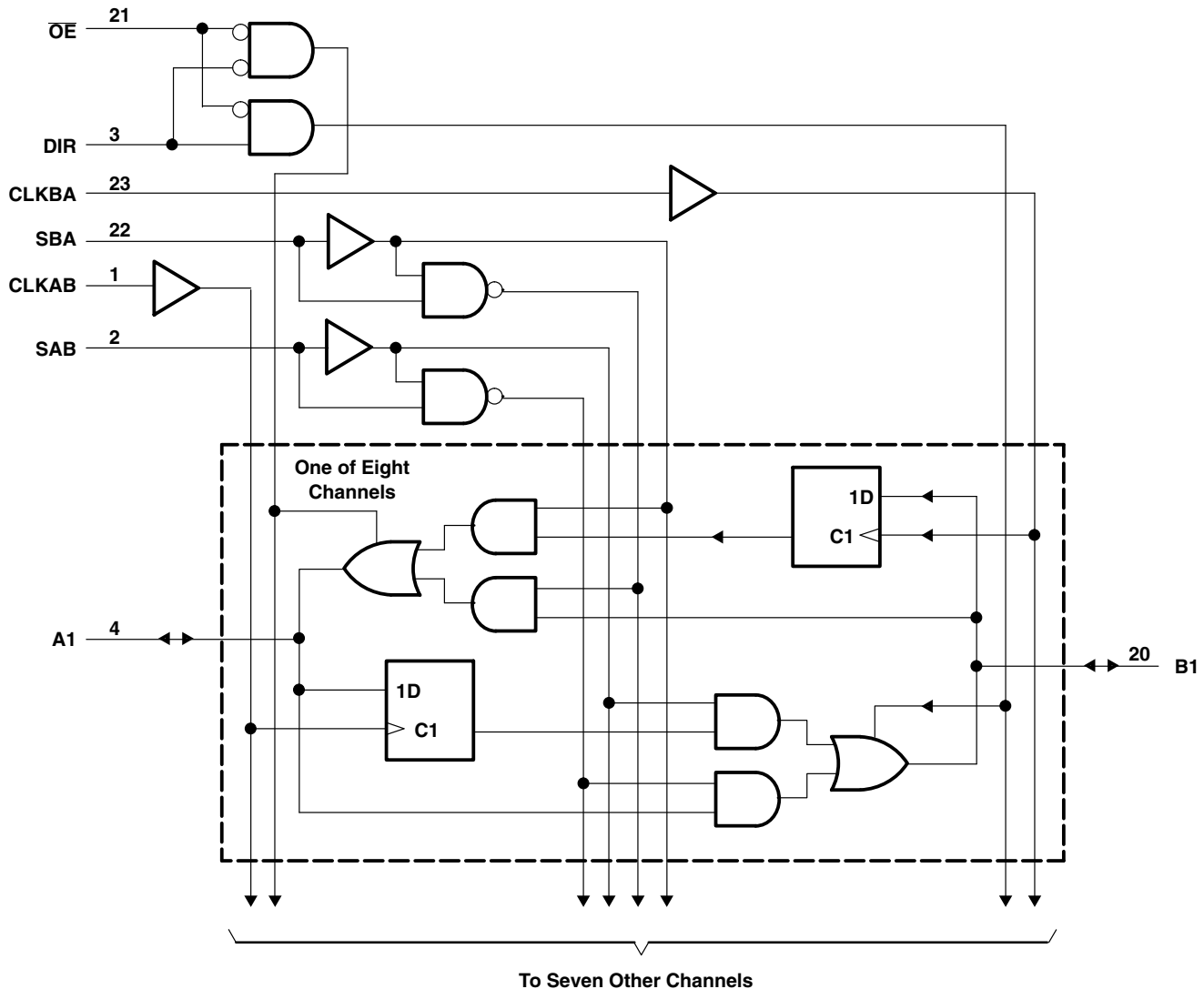
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FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at the \overline{OE} and DIR inputs. Data input functions always are enabled, i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range: Control inputs (see Note 1)	–0.5 V to 7 V
I/O ports (see Note 1)	–0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O	–0.5 V to V_{CC}
Current into any output in the low state: SN54BCT646	96 mA
SN74BCT646	128 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	46°C/W
(see Note 3): NT package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-3.

recommended operating conditions (see Note 4)

		SN54BCT646			SN74BCT646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT646			SN74BCT646			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$		-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		2.4	3.3		V
		$I_{OH} = -12\text{ mA}$	2	3.2					
		$I_{OH} = -15\text{ mA}$				2	3.1		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$	0.38	0.55					V
		$I_{OL} = 64\text{ mA}$				0.42	0.55		
I_I	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$	1			1			mA
	Control inputs		1			1			
I_{IH}^\ddagger	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$	70			70			μA
	Control inputs		20			20			
I_{IL}^\ddagger	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 0.5\text{ V}$	-0.7			-0.7			mA
	Control inputs		-0.7			-0.7			
I_{OS}^\S		$V_{CC} = 5.5\text{ V}$, $V_O = 0$	-100		-225	-100		-225	mA
I_{CCL}	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = \text{GND}$	42	67		42	67		mA
I_{CCH}	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 4.5\text{ V}$	5.6	9		5.6	9		mA
I_{CCZ}	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = \text{GND}$	10	16		10	16		mA
C_i	Control inputs	$V_{CC} = 5\text{ V}$, $V_I = 2.5\text{ V}$ or 0.5 V	6			6			pF
C_{io}	A or B port	$V_{CC} = 5\text{ V}$, $V_O = 2.5\text{ V}$ or 0.5 V	12			14			pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54BCT646		SN74BCT646		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	83		83		83		MHz
t_w	Pulse duration, CLK high or low	6		6		6		ns
t_{su}	Setup time, A or B before CLKAB \uparrow or CLKBA \uparrow	6		7		6		ns
t_h	Hold time, A or B after CLKAB \uparrow or CLKBA \uparrow	0.5		0.5		0.5		ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54BCT646		SN74BCT646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			83			83		83		MHz
t_{PLH}	CLKBA or CLKAB	A or B	3.6	7	9.4	3.6	12.4	3.6	11.2	ns
t_{PHL}			3.9	7	9.2	3.9	11.5	3.9	10.6	
t_{PLH}	A or B	B or A	3.1	6	8.1	3.1	11.1	3.1	9.5	ns
t_{PHL}			3.7	6.8	8.9	3.7	12.1	3.7	10.5	
t_{PLH}	SAB or SBA [†] (with A or B high)	A or B	4.5	8.8	11.2	4.5	15.2	4.5	13.8	ns
t_{PHL}			3.3	6	8.1	3.3	9.8	3.3	9.1	
t_{PLH}	SAB or SBA [†] (with A or B low)	A or B	3.9	7.7	10.2	3.9	13.3	3.9	12	ns
t_{PHL}			4.7	8.3	10.8	4.7	13.7	4.7	12.9	
t_{PZH}	\overline{OE}	A or B	4	7.9	10.7	4	14	4	13.2	ns
t_{PZL}			4.6	8.8	11.8	4.6	15.4	4.6	14.4	
t_{PHZ}	\overline{OE}	A or B	4	7.2	9.4	4	12	4	10.9	ns
t_{PLZ}			3.4	7	9.3	3.4	11.6	3.4	10.5	
t_{PZH}	DIR	A or B	2.8	7.8	10.7	2.8	14	2.8	13.1	ns
t_{PZL}			3.8	8.9	11.9	3.8	15.6	3.8	14.6	
t_{PHZ}	DIR	A or B	3.8	8.4	10.7	3.8	13.2	3.8	12.6	ns
t_{PLZ}			3.2	7.3	9.9	3.2	12.6	3.2	11.8	

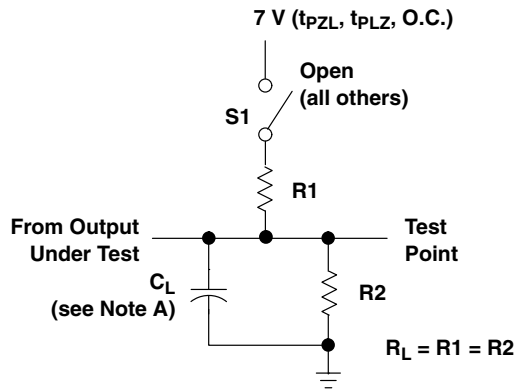
[†] These parameters are measured with the internal output state of the storage register opposite that of the bus input.



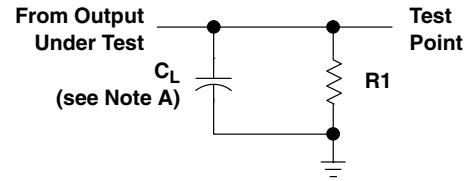
SN54BCT646, SN74BCT646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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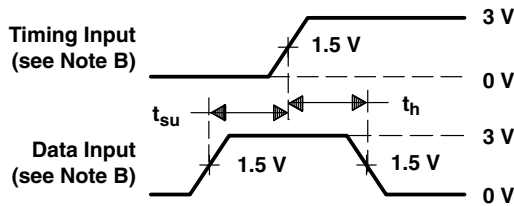
PARAMETER MEASUREMENT INFORMATION



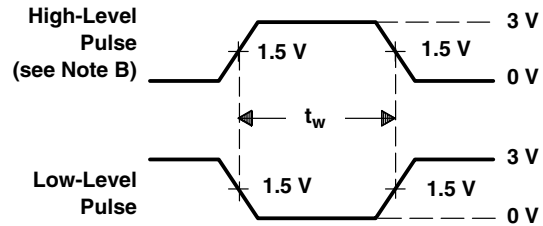
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



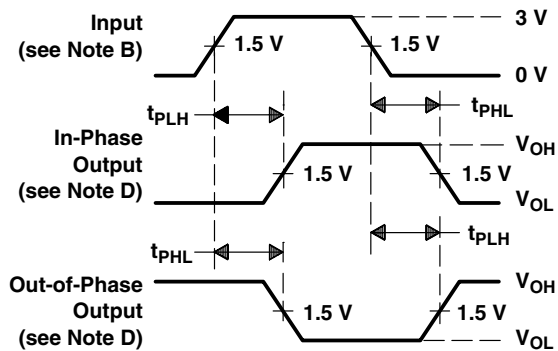
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



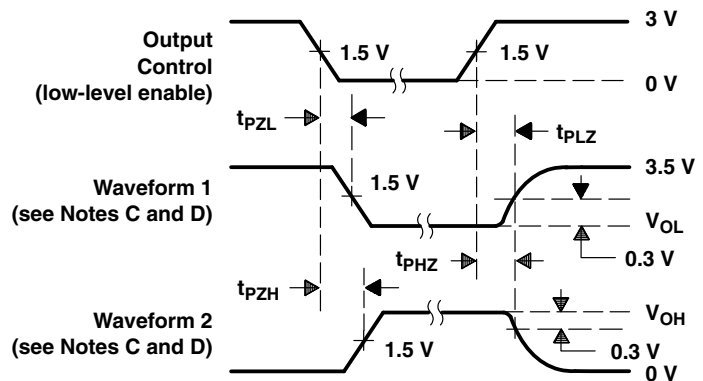
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
- C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- F. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9155501M3A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9155501M3A SNJ54BCT 646FK
5962-9155501MLA	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9155501ML A SNJ54BCT646JT
SNJ54BCT646FK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9155501M3A SNJ54BCT 646FK
SNJ54BCT646FK.A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9155501M3A SNJ54BCT 646FK
SNJ54BCT646JT	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9155501ML A SNJ54BCT646JT
SNJ54BCT646JT.A	Active	Production	CDIP (JT) 24	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9155501ML A SNJ54BCT646JT

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(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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