SN65HVD1040-Q1 EMC-Optimized Can Transceiver

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level:
    - Level 3A for All Pins Except 1, 5, 6, and 7
    - Level 3B for Pins 1, 5, 6, and 7
  - Device CDM ESD Classification Level C6
  - Device MM ESD Classification Level M3
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Improved Drop-In Replacement for TJA1040
- Meets or Exceeds the Requirements of ISO 11898-5
- GIFT/ICT Compliant
- ESD Protection up to ±8 kV (Human-Body Model) on Bus Pins
- Low-Current Standby Mode With Bus Wakeup, <12 µA Maximum
- High Electromagnetic Immunity (EMI)
- Low Electromagnetic Emissions (EME)
- Bus-Fault Protection of –27 V to 40 V
- Dominant Time-Out Function
- Thermal Shutdown Protection
- Power-Up or Down Glitch-Free Bus Inputs and Outputs
  - High Input Impedance With Low V_{CC}
  - Monotonic Outputs During Power Cycling

2 Applications

- GMW3122 Dual-Wire CAN Physical Layer
- SAE J2284 High-Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface
- Industrial Automation
  - DeviceNet™ Data Buses (Vendor ID #806)

3 Description

The SN65HVD1040-Q1 device meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications.

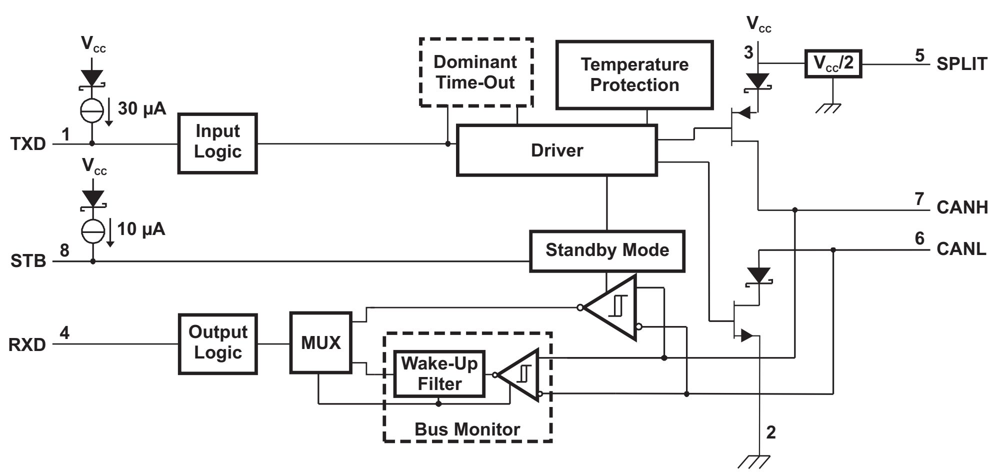
As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD1040-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2011) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Removed *Ordering Information* table, see POA at the end of the data sheet	3

5 Description (continued)

Designed for operation in especially harsh environments, the SN65HVD1040-Q1 features cross-wire, overvoltage, and loss of ground protection from –27 V to 40 V, overtemperature protection, a –12-V to 12-V common-mode range, and withstands voltage transients from –200 V to 200 V, according to ISO 7637.

STB (pin 8) provides two different modes of operation: high-speed mode or low-current standby mode. The high-speed mode of operation is selected by connecting STB (pin 8) to ground.

If a high logic level is applied to the STB pin of the SN65HVD1040-Q1, the device enters a low-current standby mode, while the receiver remains active in a low-power bus-monitor standby mode.

In the low-current standby mode, a dominant bit greater than 5 µs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

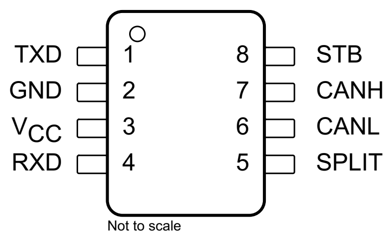
A dominant time-out circuit in the SN65HVD1040-Q1 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

SPLIT (pin 5) is available as a $V_{CC}/2$ common-mode bus voltage bias for a split-termination network (see *SPLIT*).

The SN65HVD1040 is characterized for operation from –40°C to 125°C.

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	TXD	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	GND	Device ground
3	V_{CC}	Supply	Transceiver 5-V supply
4	RXD	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	SPLIT	O	Reference output voltage ($V_{CC}/2$)
6	CANL	I/O	Low level CAN bus line
7	CANH	I/O	High level CAN bus line
8	STB	I	Mode select: Strong pulldown to GND for high-speed mode, strong pullup to V_{CC} for low power mode.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	6	V
	Voltage at bus terminals (CANH, CANL, SPLIT)		–27	40	V
I_O	Receiver output current		20	20	mA
V_I	Voltage input, ac transient pulse(3) (CANH, CANL)		–200	200	V
V_I	Voltage input (TXD, STB)		–0.3	6	V
T_J	Junction temperature		–40	170	°C
T_A	Operating free-air temperature		–40	125	°C
P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF	112		mW
		V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		170	
	Thermal shutdown temperature			185	°C
T_{stg}	Storage temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637-1, test pulses 1, 2, 3a, 3b, 5, 6, and 7. ISO 7637-1 transient tests are ac only; if dc may be coupled in with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal (–27 V to 40 V). If common-mode chokes are used in the system and the bus lines may be shorted to dc, ensure that the choke type and value in combination with the node termination and shorting voltage either does not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	All pins except 1, 5, 6, and 7	±4000	V
			Pins 1, 5, 6, and 7	±8000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)		±1000	
		Machine model (MM)		±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Tested in accordance JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance JEDEC Standard 22, Test Method C101.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, STB	2	5.25	V
V_{IL}	Low-level input voltage	TXD, STB	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver		2	
T_J	Junction temperature	See *Thermal Information*.		150	°C

7.4 Thermal Information

THERMAL METRIC(1)			SN65HVD1040-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance(2)	211	°C/W
		High-K thermal resistance(2)	131	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		53	°C/W
ψ_{JT}	Junction-to-top characterization parameter		15.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter		53.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.

7.5 Electrical Characteristics: Supply Current

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	5-V supply current	Standby mode	STB at V_{CC}, $V_I = V_{CC}$		6	12	μA
		Dominant	V_I = 0 V, 60-Ω load, STB at 0 V		50	70	mA
		Recessive	$V_I = V_{CC}$, No load, STB at 0 V		6	10	

7.6 Electrical Characteristics: Driver

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, STB at 0 V, R_L = 60 Ω, See Figure 11 and Figure 12	2.9	3.4	4.5	V
		CANL		0.8		1.75	
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 11 and Figure 12	2	2.5	3	V
V_O	Bus output voltage (standby mode)		STB at Vcc, R_L = 60 Ω, See Figure 11 and Figure 12	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, STB at 0 V, See Figure 11, Figure 12, and Figure 13	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, STB at 0 V, See Figure 11, Figure 12, and Figure 13	1.4		3	
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, STB at 0 V, R_L = 60 Ω, See Figure 11 and Figure 12	–0.012		0.012	V
			V_I = 3 V, STB at 0 V, No load	–0.5		0.05	
V_{SYM}	Output symmetry (dominant or recessive) ($V_{O(CANH)} + V_{O(CANL)}$)		STB at 0 V, R_L = 60 Ω, See Figure 23	0.9 × V_{CC}	V_{CC}	1.1 × V_{CC}	V
$V_{OC(ss)}$	Steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 18	2	2.5	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage		STB at 0 V, R_L = 60 Ω, See Figure 18		30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	μA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	μA
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	μA

(1) All typical values are at 25°C with a 5-V supply.

Electrical Characteristics: Driver (continued)

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{OS(ss)}$	Short-circuit steady-state output current	V_{CANH} = –12 V, CANL open, See Figure 21	–120	–85		mA
		V_{CANH} = 12 V, CANL open, See Figure 21		0.4	1	
		V_{CANL} = –12 V, CANH open, See Figure 21	–1	–0.6		
		V_{CANL} = 12 V, CANH open, See Figure 21		75	120	
C_O	Output capacitance	See receiver input capacitance				

7.7 Electrical Characteristics: Receiver

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1		800	900	mV
V_{IT-}	Negative-going input threshold voltage, high-speed mode	STB at 0 V, See Table 1	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)		100	125		mV
V_{IT}	Input threshold voltage, standby mode	STB at V_{CC}	500		1150	mV
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 16	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 16		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH = CANL = 5 V, V_{CC} at 0 V, TXD at 0 V			3	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, $V_I = 0.4 \sin(4E6\pi t) + 2.5$ V		12		pF
C_{ID}	Differential input capacitance	TXD at 3 V, $V_I = 0.4 \sin(4E6\pi t)$		2		pF
R_{ID}	Differential input resistance	TXD at 3 V, STB at 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, STB at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching [1 – ($R_{IN\ (CANH)}$ / $R_{IN\ (CANL)}$)] × 100%	$V_{(CANH)} = V_{(CANL)}$	–3%	0%	3%	

(1) All typical values are at 25°C with a 5-V supply.

7.8 Switching Characteristics: Device

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	STB at 0 V, See Figure 19	90	230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive		90	230	ns

7.9 Switching Characteristics: Driver

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, See Figure 14	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low level output	STB at 0 V, See Figure 14	25	45	120	ns
t_r	Differential output signal rise time	STB at 0 V, See Figure 14		25		ns
t_f	Differential output signal fall time	STB at 0 V, See Figure 14		45		ns
t_{en}	Enable time from standby mode to dominant	See Figure 17			10	µs
$t_{(dom)}$	Dominant time-out	$\downarrow V_I$, See Figure 20	300	450	700	µs

7.10 Switching Characteristics: Receiver

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V, See Figure 16	60	90	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output	STB at 0 V, See Figure 16	45	70	130	ns
t_r	Output signal rise time	STB at 0 V, See Figure 16		8		ns
t_f	Output signal fall time	STB at 0 V, See Figure 16		8		ns
t_{BUS}	Dominant time required on bus for wakeup from standby	STB at V_{CC}, See Figure 22	1.5		5	µs

7.11 STB Pin Characteristics

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{IH}	High-level input current	STB at V_{CC}	–10	0	µA
I_{IL}	Low-level input current	STB at 0 V	–10	0	µA

7.12 SPLIT Pin Characteristics

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3 × V_{CC}	0.5 × V_{CC}	0.7 × V_{CC}	V
$I_{O(stb)}$	Leakage current, standby mode	STB at 2 V, –12 V ≤ V_O ≤ 12 V	–5		5	µA

7.13 Typical Characteristics

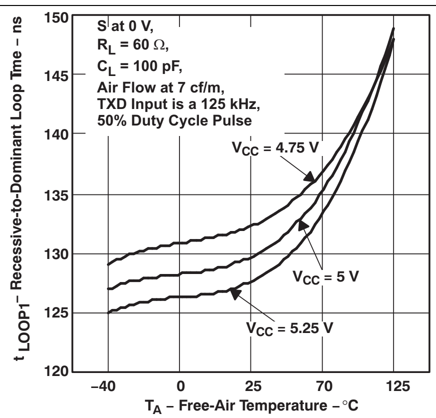


Figure 1. Recessive-to-Dominant Loop Time vs Free-Air Temperature (Across V_{CC})

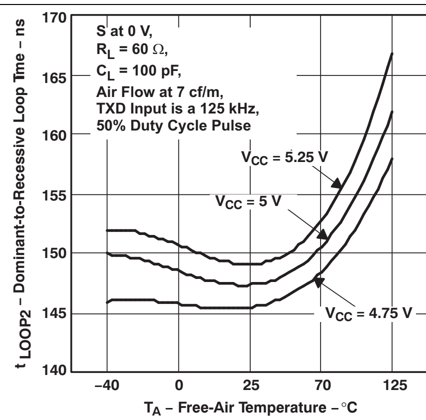


Figure 2. Dominant-to-Recessive Loop Time vs Free-Air Temperature (Across V_{CC})

Typical Characteristics (continued)

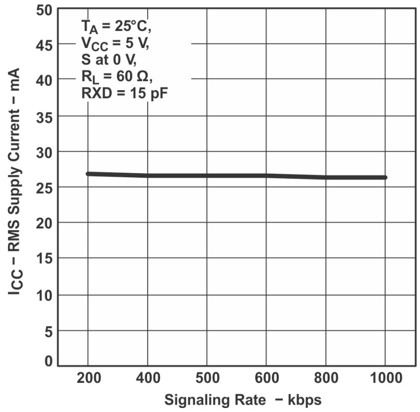


Figure 3. Supply Current (RMS) vs Signaling Rate

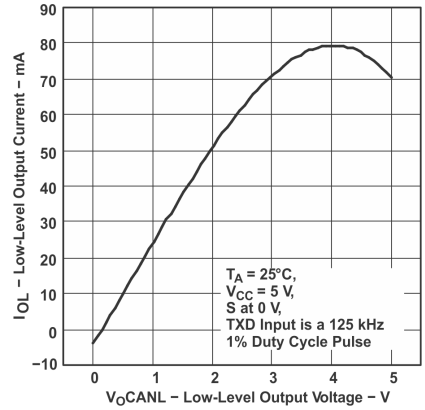


Figure 4. Driver Low-Level Output Voltage vs Low-Level Output Current

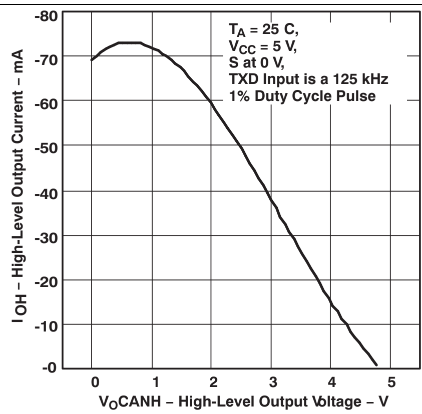


Figure 5. Driver High-Level Output Voltage vs High-Level Output Current

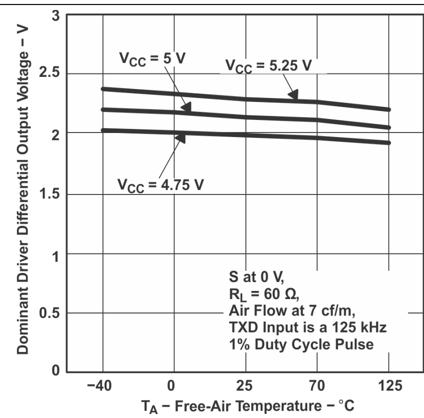


Figure 6. Driver Differential Output Voltage vs Free-Air Temperature (Across V_{CC})

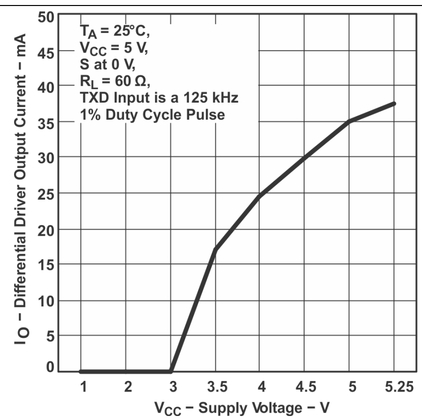


Figure 7. Driver Output Current vs Supply Voltage

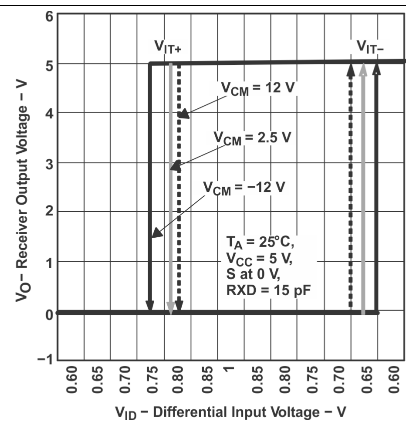


Figure 8. Receiver Output Voltage vs Differential Input Voltage

Typical Characteristics (continued)

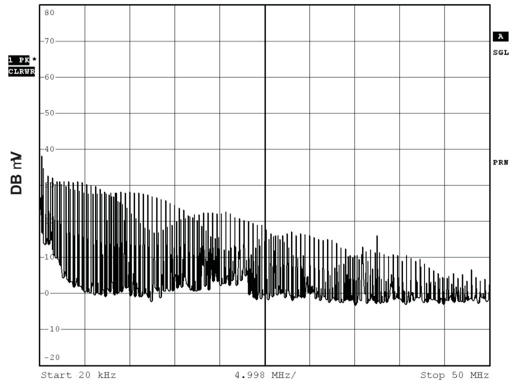


Figure 9. Frequency Spectrum of Common-Mode Emissions

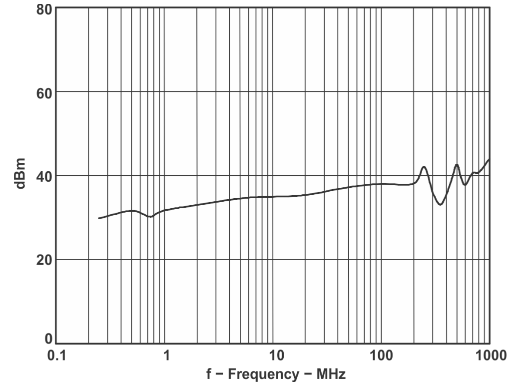


Figure 10. Direct Power Injection (DPI) Response vs Frequency

8 Parameter Measurement Information

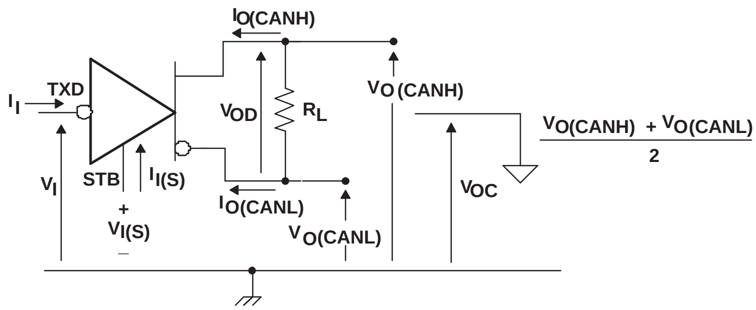


Figure 11. Driver Voltage, Current, and Test Definition

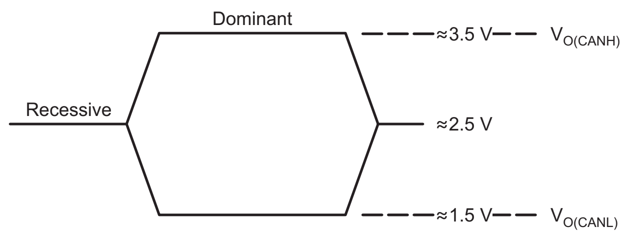


Figure 12. Bus Logic-State Voltage Definitions

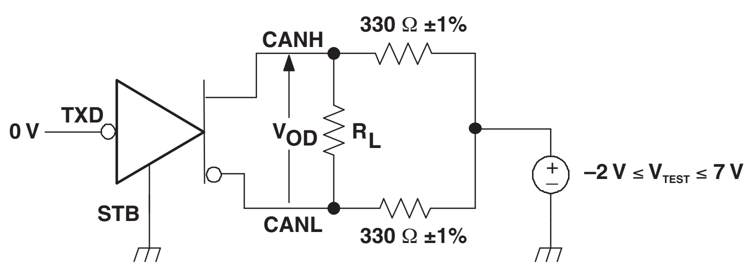


Figure 13. Driver V_{OD} Test Circuit

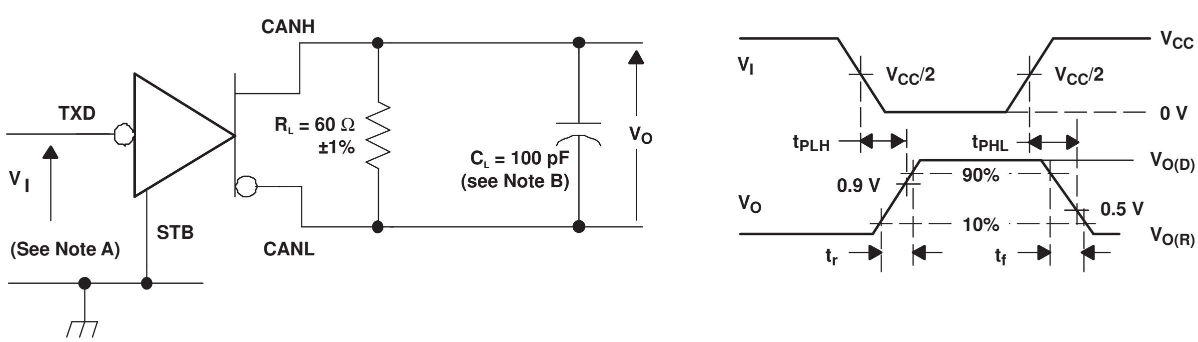


Figure 14. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

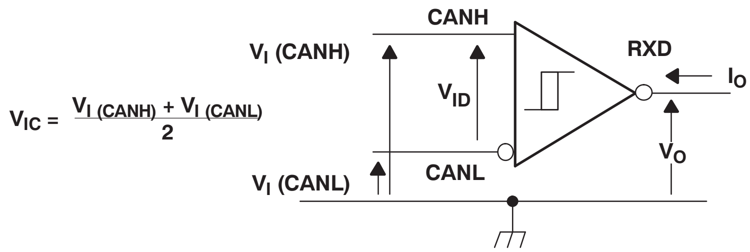
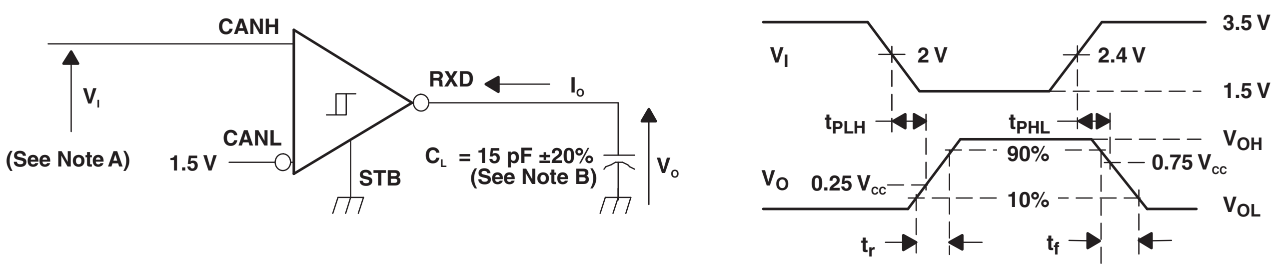


Figure 15. Receiver Voltage and Current Definitions



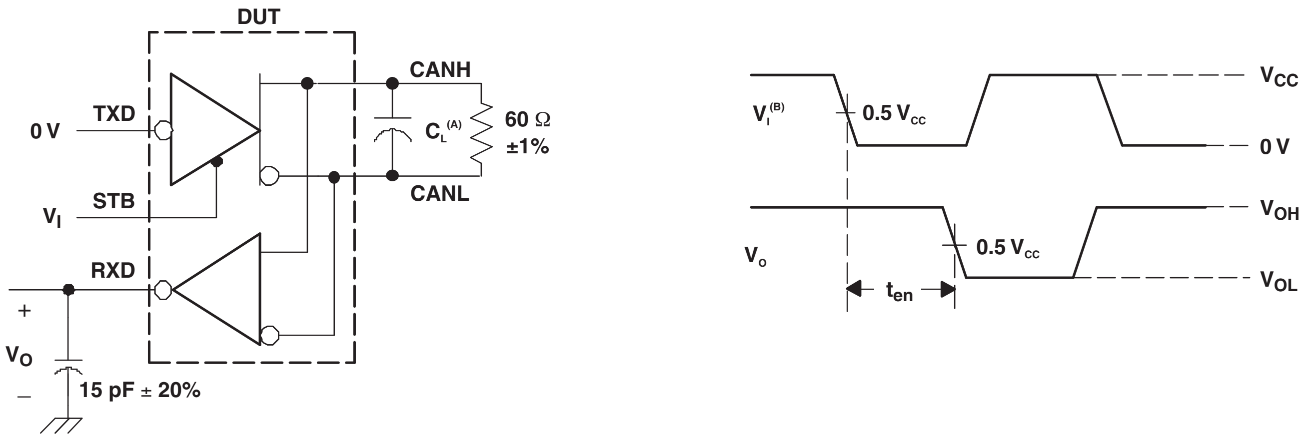
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 16. Receiver Test Circuit and Voltage Waveforms

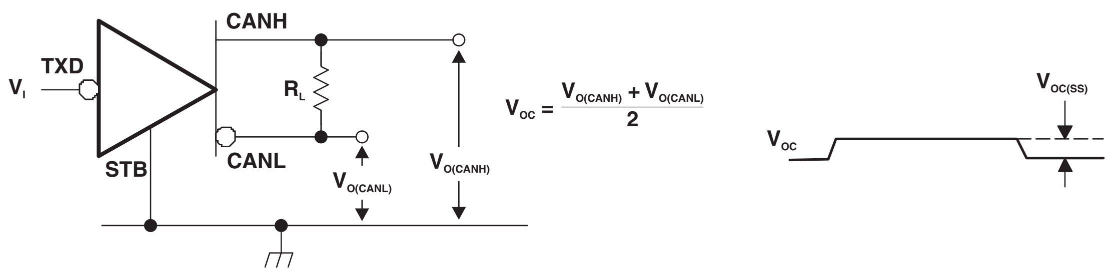
Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\|V_{ID}\|$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



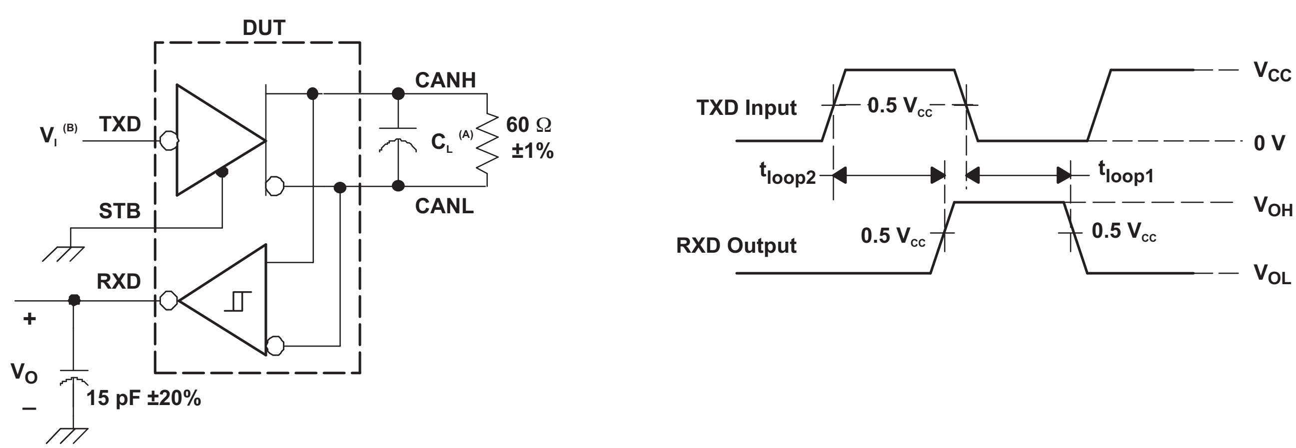
A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 17. t_{en} Test Circuit and Waveforms



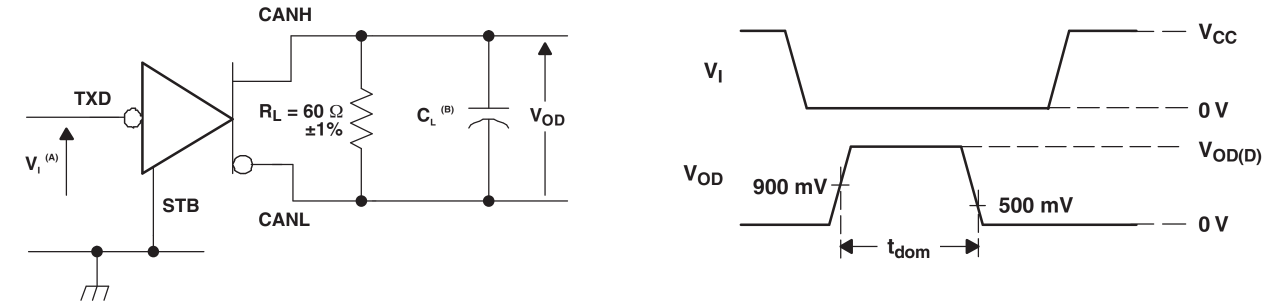
A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 18. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.
B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 19. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 20. Dominant Time-Out Test Circuit and Waveforms

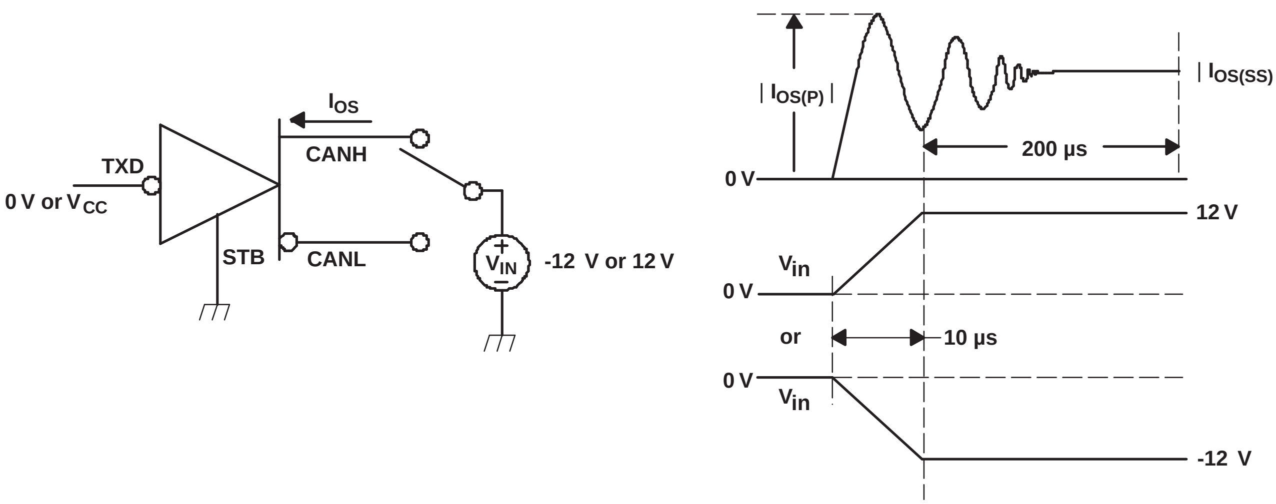
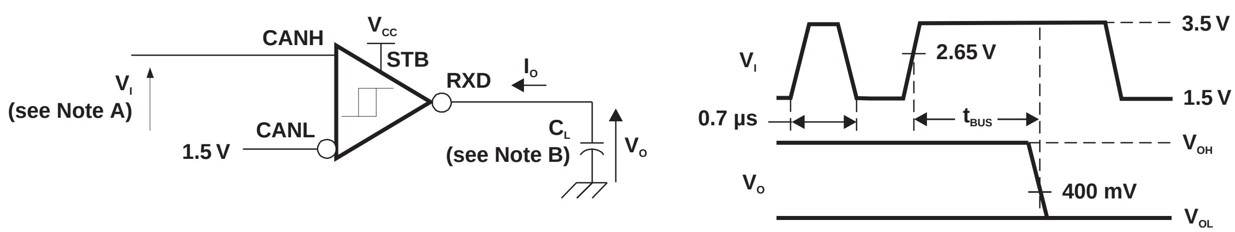


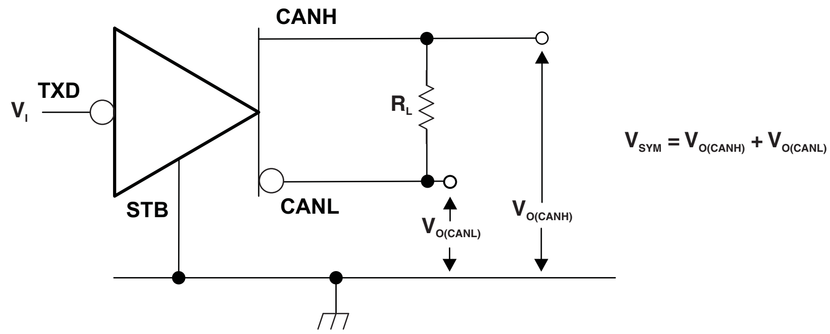
Figure 21. Driver Short-Circuit Current Test and Waveforms



A. For V_I bit width ≤ 0.7 µs, $V_O = V_{OH}$. For V_I bit width ≥ 5 µs, $V_O = V_{OL}$. V_I input pulses are supplied from a generator with the following characteristics: t_r/t_f < 6 ns.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 22. t_{BUS} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: $t_r/t_f \leq 6$ ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

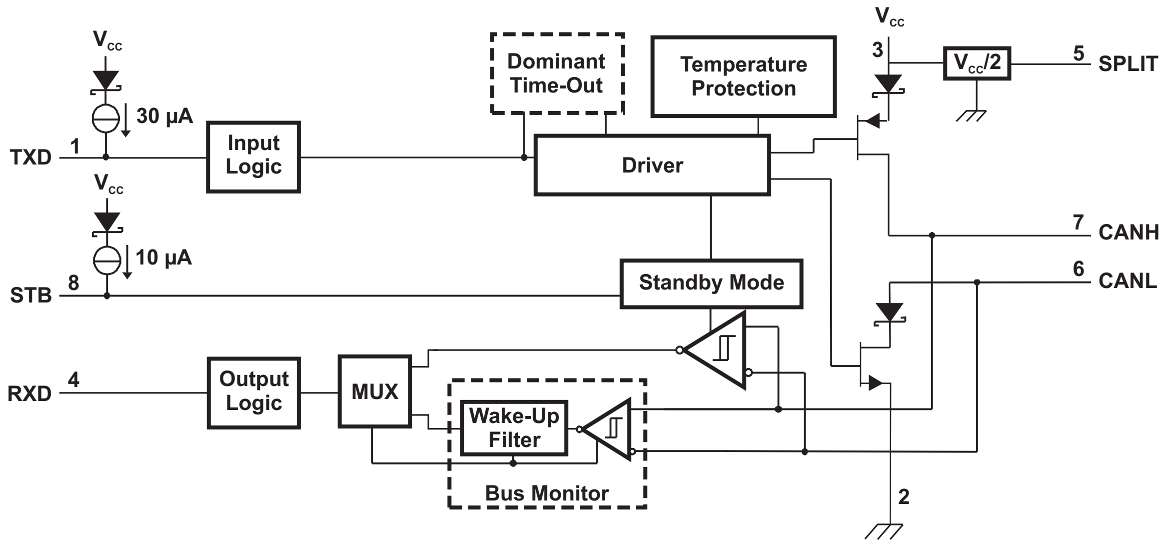
Figure 23. Driver Output Symmetry Test Circuit

9 Detailed Description

9.1 Overview

The SN65HVD1040-Q1 CAN bus transceiver meets or exceeds the ISO 11898 standard as a high-speed controller area network (CAN) bus physical layer device. The device is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Mode Control

9.3.1.1 High-Speed Mode

Select the high-speed mode of the device operation by setting the STB pin low. The CAN bus driver and receiver are fully operational and the CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

9.3.1.2 Low-Power Mode

If a high logic level is applied to the STB pin, the device enters a low-power bus-monitor standby mode. While the SN65HVD1040-Q1 is in the low-power bus-monitor standby mode, a dominant bit greater than 5 µs on the bus is passed by the bus-monitor circuit to the receiver output. The local protocol controller may then reactivate the device when it needs to transmit to the bus.

9.3.2 Dominant State Time-Out

During normal mode, the mode where the CAN driver is active, the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. The DTO circuit is triggered on a falling edge on the driver input, TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen on TXD before the time-out period expires. This frees the CAN bus for communication between other nodes on the network. The CAN driver is re-enabled when a rising edge is seen on the driver input, TXD, thus clearing the TXD DTO condition. The receiver and RXD pin still reflect the CAN bus, and the bus pins are biased to recessive level during a TXD DTO.

Feature Description (continued)

NOTE

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate on the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate using: Minimum Data Rate = 11 / t_{TXD_DTO}.

9.3.3 Thermal Shutdown

The SN65HVD1040-Q1 device has a thermal shutdown that turns off the driver outputs when the junction temperature nears 190°C. This shutdown prevents catastrophic failure from bus shorts, but does not protect the circuit from possible damage. The user should strive to maintain recommended operating conditions, and not exceed absolute maximum ratings at all times. If the SN65HVD1040-Q1 device is subjected to many or long durations faults that can put the device into thermal shutdown, it must be replaced.

9.3.4 SPLIT

A reference voltage (V_{CC}/2) is available through the SPLIT output pin. The SPLIT voltage must be tied to the common-mode point in a split termination network, hence the pin name, to help stabilize the output common-mode voltage. See Figure 28 for more application specific information on properly terminating the CAN bus.

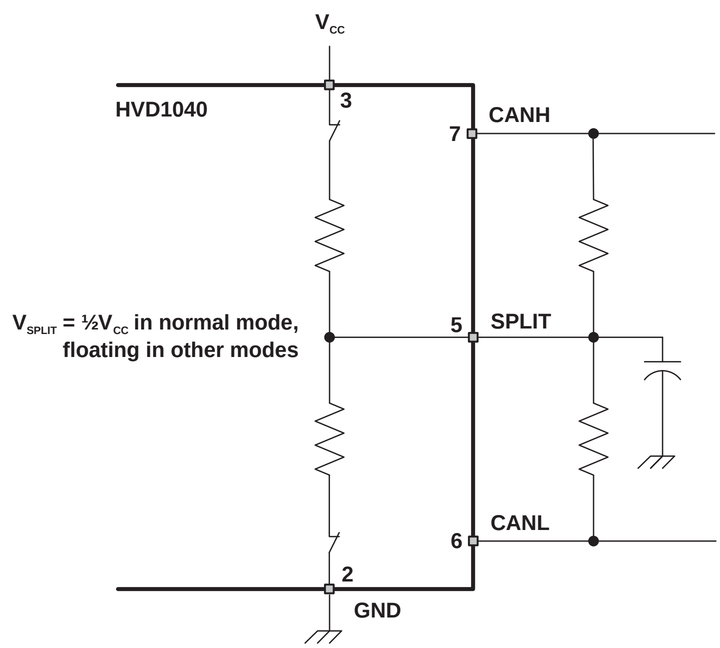


Figure 24. SPLIT Pin Stabilization Circuitry and Application

9.3.5 Operating Temperature Range

The SN65HVD1040-Q1 is characterized for operation from –40°C to 125°C.

9.4 Device Functional Modes

Table 2 and Table 3 lists the functional modes of the SN65HVD1040-Q1.

Table 2. Driver Function Table(1)

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	Dominant
H	L	Z	Z	Recessive
Open	L	Z	Z	Recessive
X	H or Open	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Y = weak pulldown do GND, Z = high impedance

Table 3. Receiver Function Table(1)

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	STB	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	L	Dominant
$V_{ID} \geq 1.15$ V	H or Open	L	Dominant
0.5 V < V_{ID} < 0.9 V	X	?	?
$V_{ID} \leq 0.5$ V	X	H	Recessive
Open	X	H	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

Table 4. Parametric Cross Reference With the TJA1040

TJA1040 (1)	PARAMETER	HVD10xx
TJA1040 DRIVER SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	Driver I_{IH}
I_{IL}	Low-level input current	Driver I_{IL}
TJA1040 BUS SECTION		
$V_{th(dif)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{hys(dif)}$	Differential input hysteresis	Receiver V_{hys}
$V_{O(dom)}$	Dominant output voltage	Driver $V_{O(D)}$
$V_{O(reces)}$	Recessive output voltage	Driver $V_{O(R)}$
$V_{I(dif)(th)}$	Differential input voltage	Receiver V_{IT} and recommended V_{ID}
$V_{O(dif0(bus)}$	Differential bus voltage	Driver $V_{OD(D)}$ and $V_{OD(R)}$
I_{LI}	Power-off bus input current	Receiver $I_{I(off)}$
$I_{O(SC)}$	Short-circuit output current	Driver $I_{OS(SS)}$
$R_{I(cm)}$	CANH, CANL input resistance	Receiver R_{IN}
$R_{I(def)}$	Differential input resistance	Receiver R_{ID}
$R_{I(cm)\ (m)}$	Input resistance matching	Receiver $R_{I\ (m)}$
$C_{I(cm)}$	Input capacitance to ground	Receiver C_I
$C_{I(dif)}$	Differential input capacitance	Receiver C_{ID}
TJA1040 RECEIVER SECTION		
I_{OH}	High-level output current	Recommended I_{OH}
I_{OL}	Low-level output current	Recommended I_{OL}
TJA1040 SPLIT PIN SECTION		
V_O	Reference output voltage	V_O
TJA1040 TIMING SECTION		
$t_{d(TXD\text{-}BUSon)}$	Delay TXD to bus active	Driver t_{PLH}
$t_{d(TXD\text{-}BUSoff)}$	Delay TXD to bus inactive	Driver t_{PHL}
$t_{d(BUSon\text{-}RXD)}$	Delay bus active to RXD	Receiver t_{PHL}
$t_{d(BUSoff\text{-}RXD)}$	Delay bus inactive to RXD	Receiver t_{PLH}
$t_{PD(TXD–RXD)}$	Prop delay TXD to RXD	Device t_{LOOP1} and t_{LOOP2}
$t_{d(stb\text{-}norm)}$	Enable time from standby to dominant	Driver t_{en}
TJA1040 STB PIN SECTION		
V_{IH}	High-level input voltage	Recommended V_{IH}
V_{IL}	Low-level input voltage	Recommended V_{IL}
I_{IH}	High-level input current	I_{IH}
I_{IL}	Low-level input current	I_{IL}

(1) From TJA1040 Product Specification, NXP, February 19, 2003.

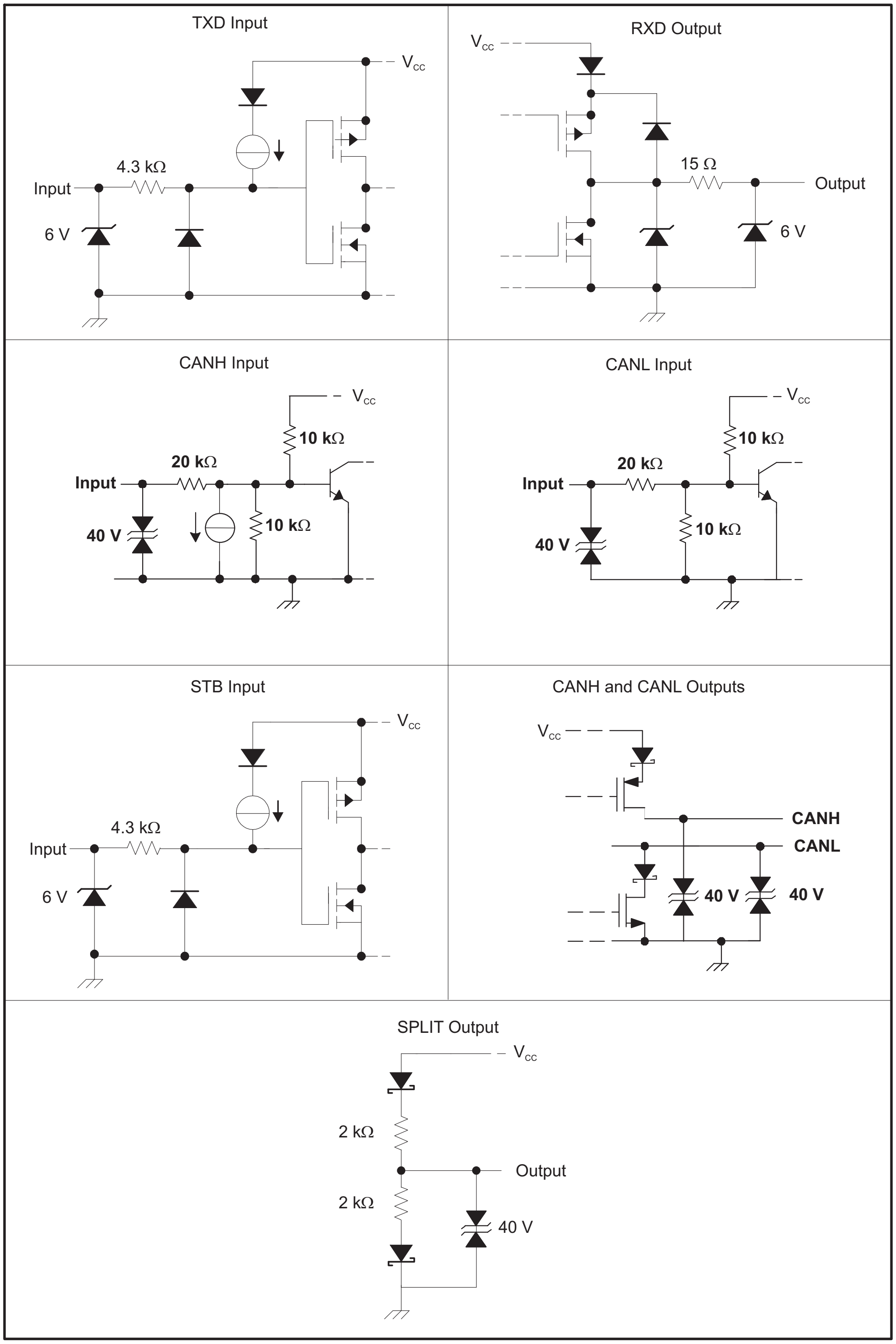


Figure 25. Equivalent Input and Output Schematic Diagrams

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 CAN Nodes Using Common-Mode Chokes

The SN65HVD1040-Q1 has been EMC optimized to allow use in CAN systems without a common-mode choke. However, sometimes the CAN network and termination architecture may require their use. If a common-mode choke is used in a CAN node where bus line shorts to DC voltages may be possible, take care in the choice of common-mode choke (winding type, core type, and value) along with the termination and protection scheme of the node and bus. During CAN bus shorts to DC voltages the inductance of the common-mode choke may cause inductive flyback transients. Some combinations of common-mode chokes, bus termination, and shorting voltages can take the bus voltages outside the absolute maximum ratings of the device, possibly leading to damage.

10.2 Typical Application

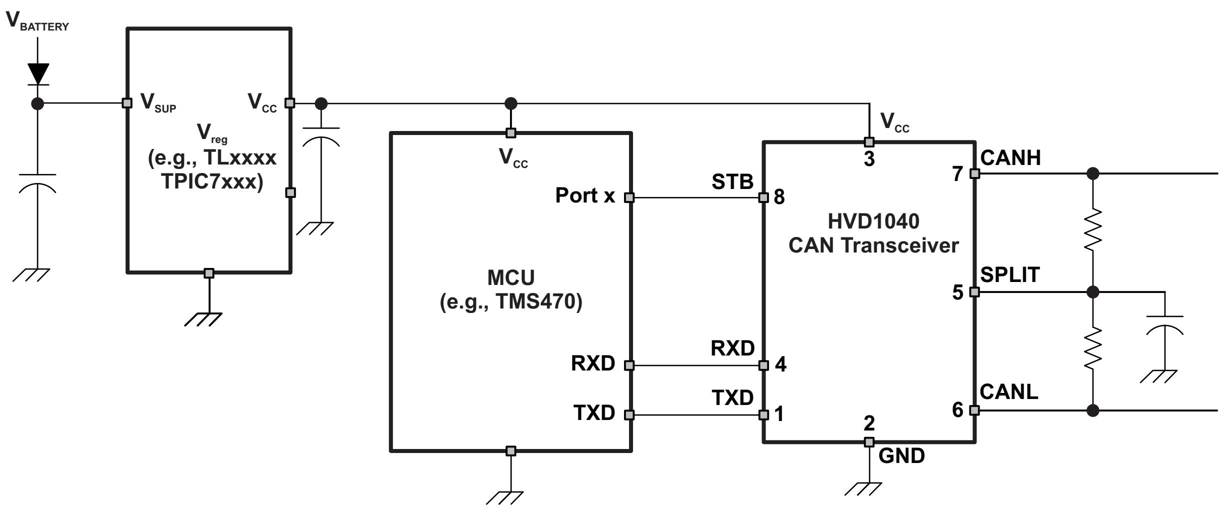


Figure 26. Typical Application Using Split Termination for Stabilization

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length, and Number of Nodes

The ISO 11898 Standard specifies up to 1 Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are SAE J1939, CANopen, DeviceNet, and NMEA2000.

Typical Application (continued)

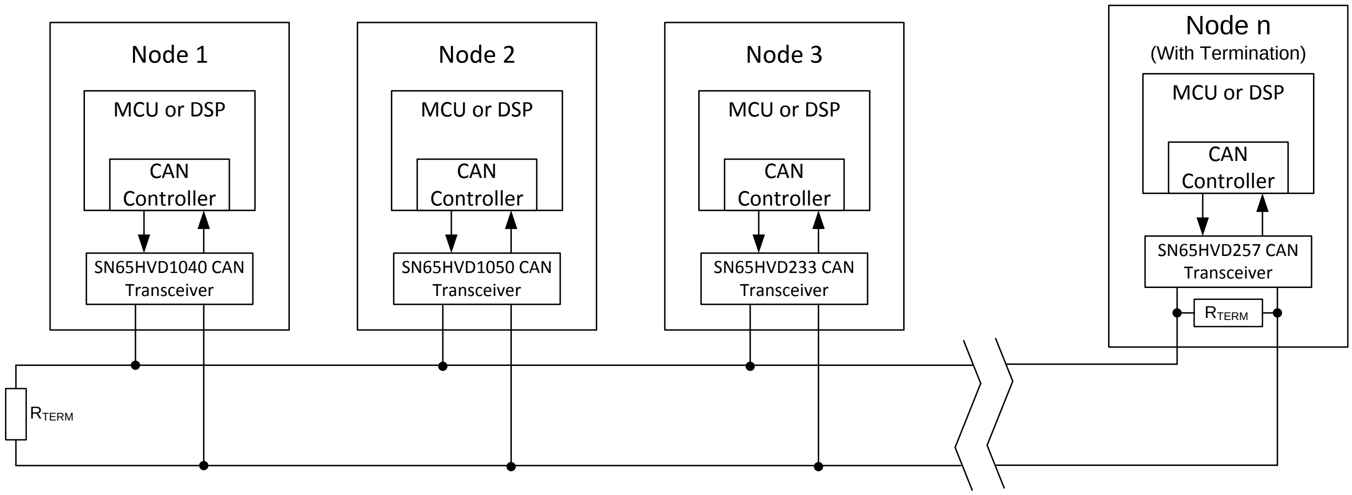


Figure 27. Typical CAN Bus

A high number of nodes requires a transceiver with high input impedance and wide common mode range such as the SN65HVD1040 CAN transceiver. ISO 11898-2 specifies the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVD1040 device is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common-mode range of –2 V to 7 V through a 330-Ω coupling network. This network represents the bus loading of 90 SN65HVD1040 transceivers based on their minimum differential input resistance of 30 kΩ. Therefore, the SN65HVD1040 supports up to 90 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets, and signal integrity, thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

10.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used (see Figure 28). Split termination uses two 60-Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

Take care determining the power ratings of the termination resistors. A typical worst-case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the current limit of the CAN transceiver.

Typical Application (continued)

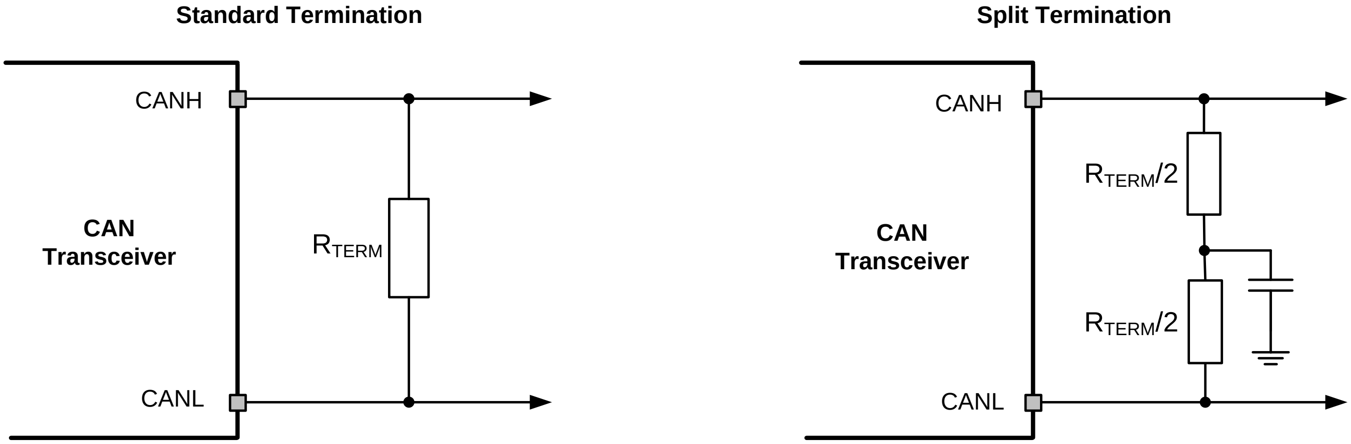


Figure 28. CAN Termination

10.2.1.3 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (TXD pin) to the differential outputs (CANH and CANL pins), plus the delay from the receiver inputs (CANH and CANL) to its output (RXD pin). A typical loop delay for the SN65HVD1050 transceiver is displayed in Figure 32.

10.2.2 Detailed Design Procedure

10.2.2.1 CAN Basics

The basics of arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this *sample* is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the approximately 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system also must be accounted for with adjustments in signaling rate and stub and bus length. Table 5 lists the maximum signaling rates achieved with the SN65HVD1040 with several bus lengths of category 5, shielded twisted pair (CAT 5 STP) cable.

Table 5. Maximum Signaling Rates for Various Cable Lengths

BUS LENGTH (m)	SIGNALING RATE (kbps)
30	1000
100	500
250	250
500	125
1000	62.5

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and must be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the standard should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the standard's –2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity. The SN65HVD1040 enhances the standard's insurance of data integrity with an extended –12 V to 12 V range of common-mode operation.

An eye pattern is a useful tool for measuring overall signal quality. As displayed in Figure 29, the differential signal changes logic states in two places on the display, producing an *eye*. Instead of viewing only one logic crossing on the scope, an entire *bit* of data is brought into view. The resulting eye pattern includes all of the effects of systemic and random distortion, and displays the time during which a signal may be considered valid.

The height of the eye above or below the receiver threshold voltage level at the sampling point is the noise margin of the system. Jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal. Note that jitter present at the receiver threshold voltage level is considered by some to be a more effective representation of the jitter at the input of a receiver.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate sampling, and lowering the height enters the 900-mV or 500-mV threshold of a receiver.

Different sources induce noise onto a signal. The more obvious noise sources are the components of a transmission circuit themselves; the signal transmitter, traces and cables, connectors, and the receiver. Beyond that, there is a termination dependency, cross-talk from clock traces and other proximity effects, V_{CC} and ground bounce, and electromagnetic interference from near-by electrical equipment.

The balanced receiver inputs of the SN65HVD1040 mitigate most all sources of signal corruption, and when used with a quality shielded twisted-pair cable, help insure data integrity.

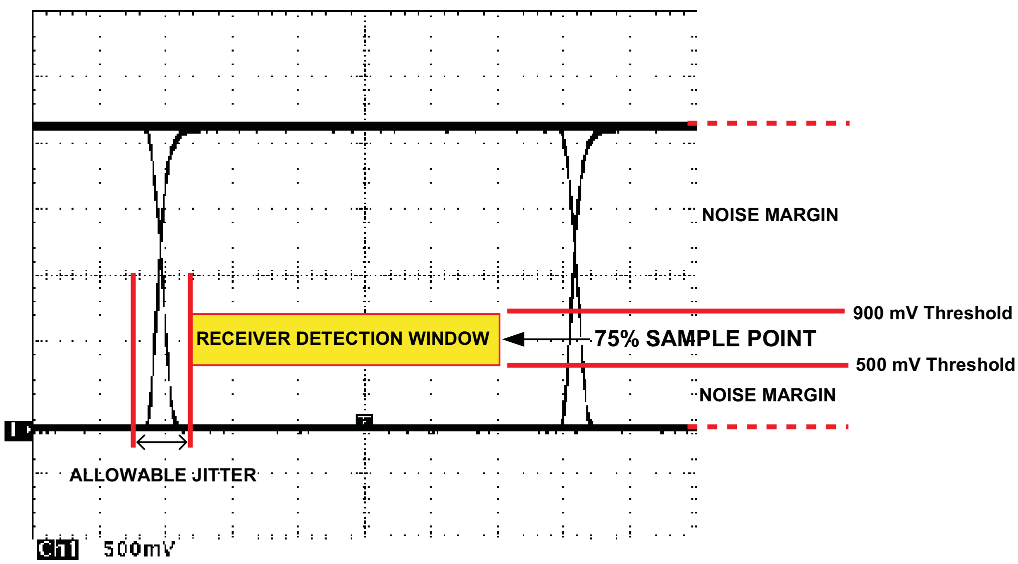


Figure 29. Typical CAN Differential Signal Eye-Pattern

10.2.2.1.1 Differential Signal

CAN is a differential bus where complementary signals are sent over two wires and the voltage difference between the two wires defines the logical state of the bus. The differential CAN receiver monitors this voltage difference and outputs the bus state with a single-ended logic level output signal.

The CAN driver creates the differential voltage between CANH and CANL in the dominant state. The dominant differential output of the SN65HVD1040 is greater than 1.5 V and less than 3 V across a 60-Ω load as defined by the ISO 11898 standard. Figure 30 shows CANH, CANL, and the differential dominant state level for the SN65HVD1040.

A CAN receiver is required to output a recessive state when less than 500 mV of differential voltage exists on the bus, and a dominant state when more than 900 mV of differential voltage exists on the bus. The CAN receiver must do this with common-mode input voltages from –2 V to 7 V.

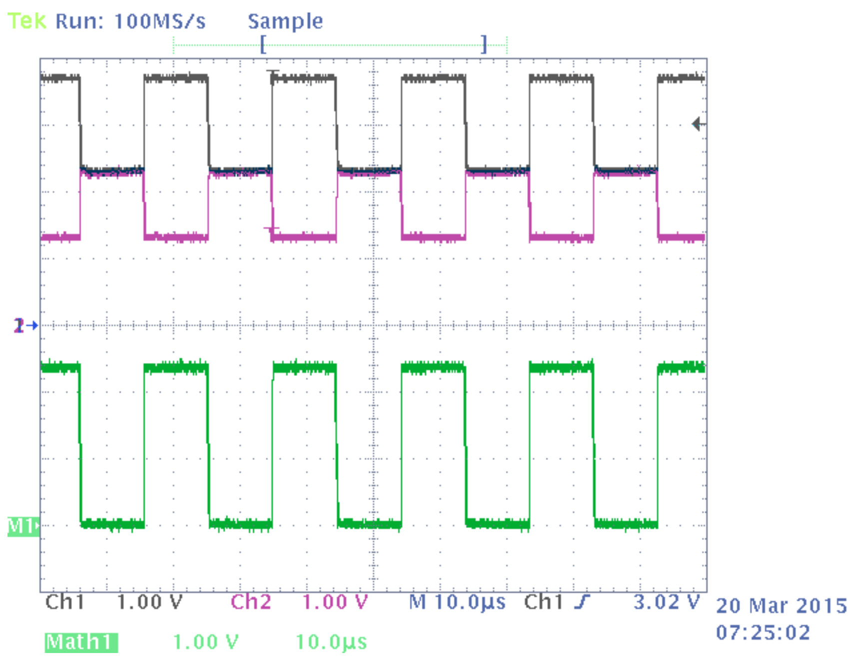


Figure 30. Differential Output Waveform

10.2.2.1.2 Common-Mode Signal

A common-mode or recessive signal is an average voltage of the two signal wires that the differential receiver rejects. The common-mode signal comes from the CAN driver, ground noise, and coupled bus noise. Because the bias voltage of the recessive state of the device is dependent on V_{CC} , any noise present or variation of V_{CC} has an effect on this bias voltage seen by the bus. The SN65HVD1040 CAN transceiver has the recessive bias voltage set to 0.5 × V_{CC} to comply with the ISO 11898-2 CAN standard.

10.2.2.1.3 ESD Protection

A typical application that employees a CAN bus network may require some form of ESD, burst, and surge protection to shield the CAN transceiver against unwanted transients that can potential damage the transceiver. To help shield the SN65HVD1040 transceiver against these high energy transients, transient voltage suppressors can be implemented on the CAN differential bus terminals. These devices will help absorb the impact of a ESD, burst, or surge strike.

10.2.2.1.4 Transient Voltage Suppresser (TVS) Diodes

Transient voltage suppressors are the preferred protection components for a CAN bus due to their low capacitance, which allows them to be designed into every node of a multi-node network without requiring a reduction in data rate. With response times of a few picoseconds and power ratings of up to several kilowatts, TVS diodes present the most effective protection against ESD, burst, and surge transients.

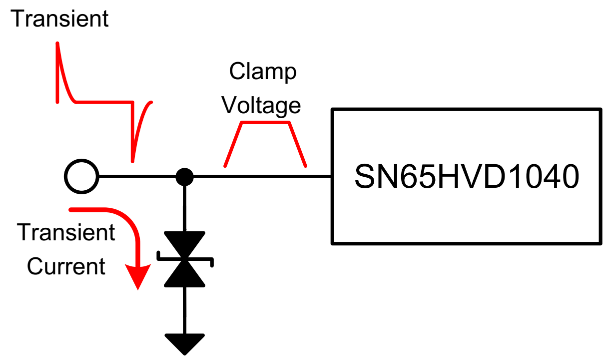


Figure 31. Transient

10.2.3 Application Curve

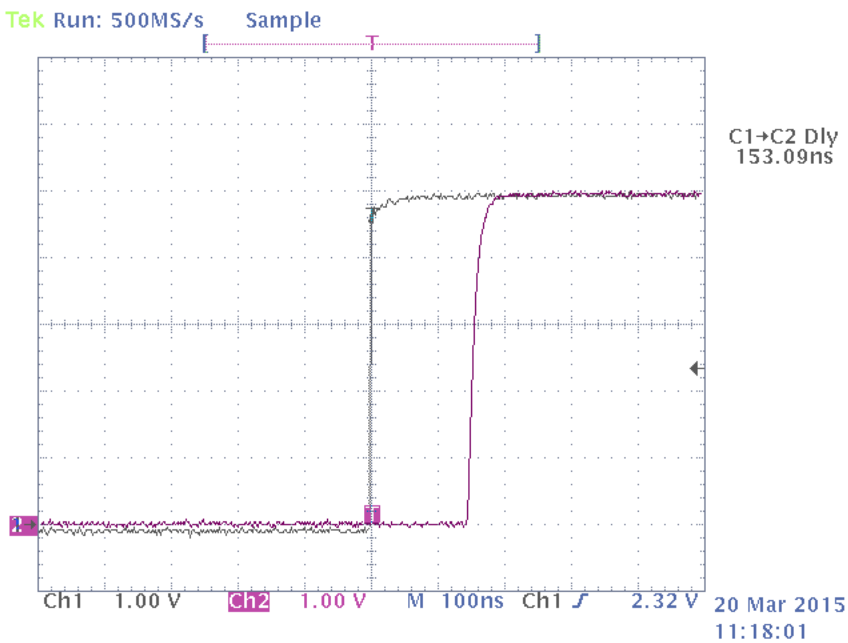


Figure 32. t_{loop} Delay Waveform

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close as possible to the V_{CC} supply pins as possible. The TPS76350 is a linear voltage regulator suitable for the 5-V supply rail.

12 Layout

12.1 Layout Guidelines

For the printed-circuit board design to be successful, start with the design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. On-chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

NOTE

High-frequency current follows the path of least inductance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 33.

The bus transient protection and filtering components must be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 33 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground through capacitor C6. Split termination provides common-mode filtering for the bus. When termination is placed on the board instead of directly on the bus, take care ensuring the terminating node is not removed from the bus as this causes signal integrity issues of the bus is not properly terminated on both ends.

Bypass and bulk capacitors must be placed as close as possible to the supply pins of transceiver, examples C2, C3 (V_{CC}). Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3, and R4.

To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor must be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the TXD pin of the device an external pullup resistor between 1 kΩ and 10 kΩ must be used to drive the recessive input state of the device.

Pin 5: SPLIT must be connected to the center point of a split termination scheme to help stabilize the common-mode voltage to $V_{CC}/2$. If SPLIT is unused it must be left floating.

Pin 8: This pin is shown assuming the mode pin, STB, is used. If the device is only used in normal mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

12.2 Layout Example

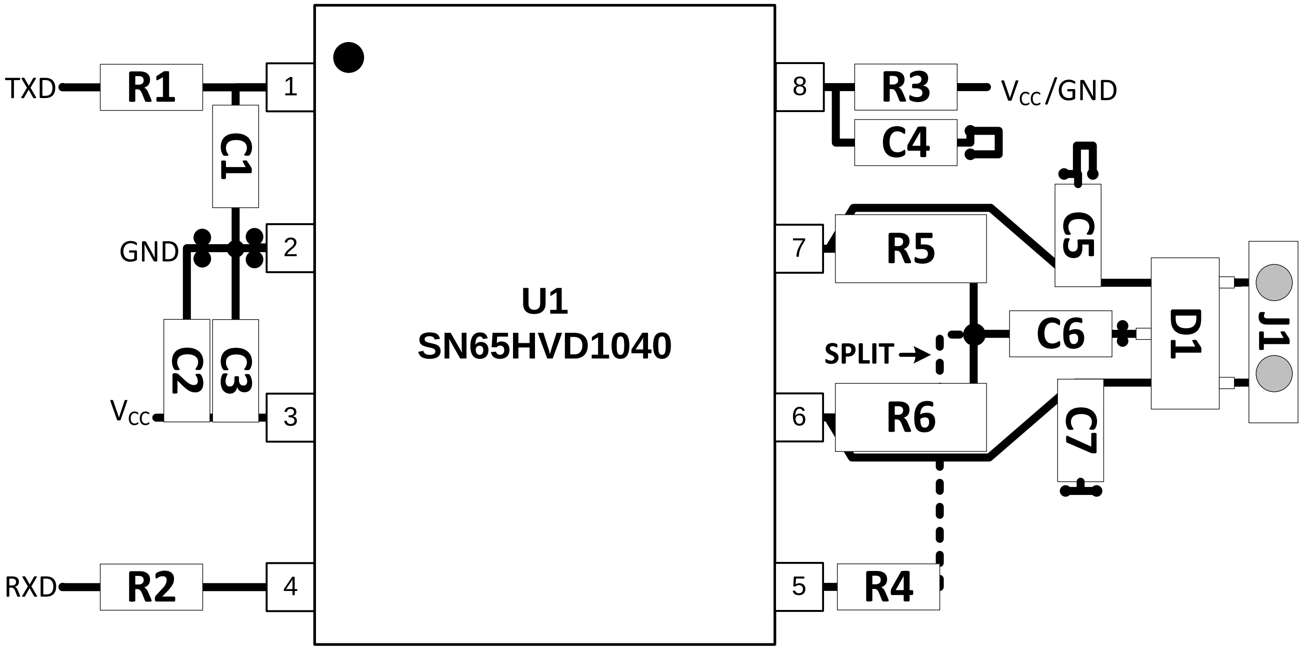


Figure 33. Layout Recommendation

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

DeviceNet, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1040QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H1040Q
SN65HVD1040QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	H1040Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN65HVD1040-Q1 :

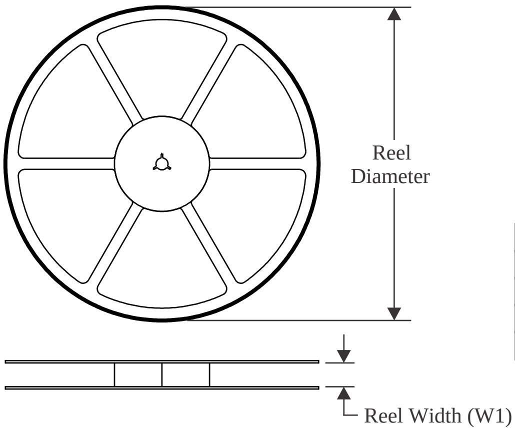
- Catalog : SN65HVD1040

NOTE: Qualified Version Definitions:

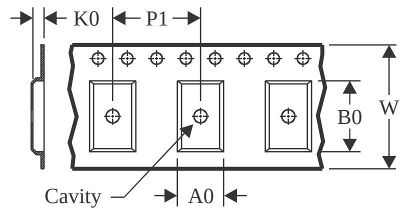
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

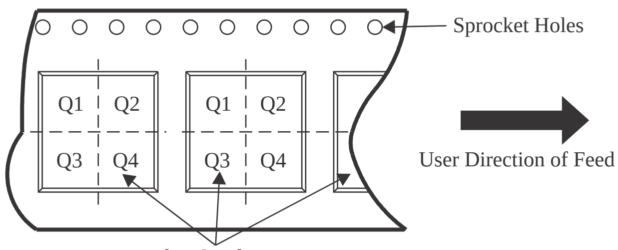


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

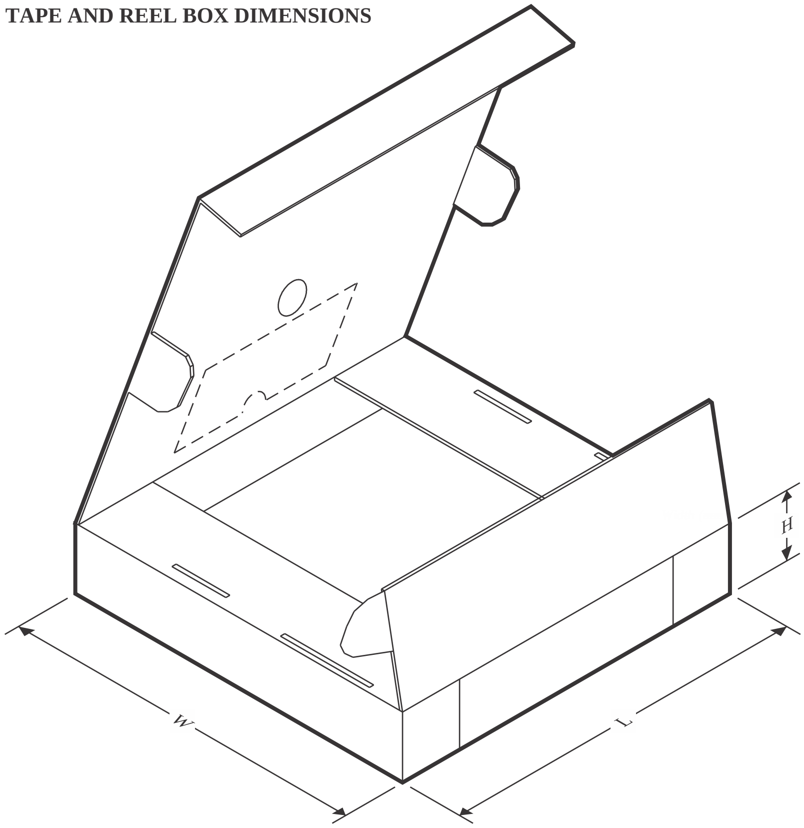
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

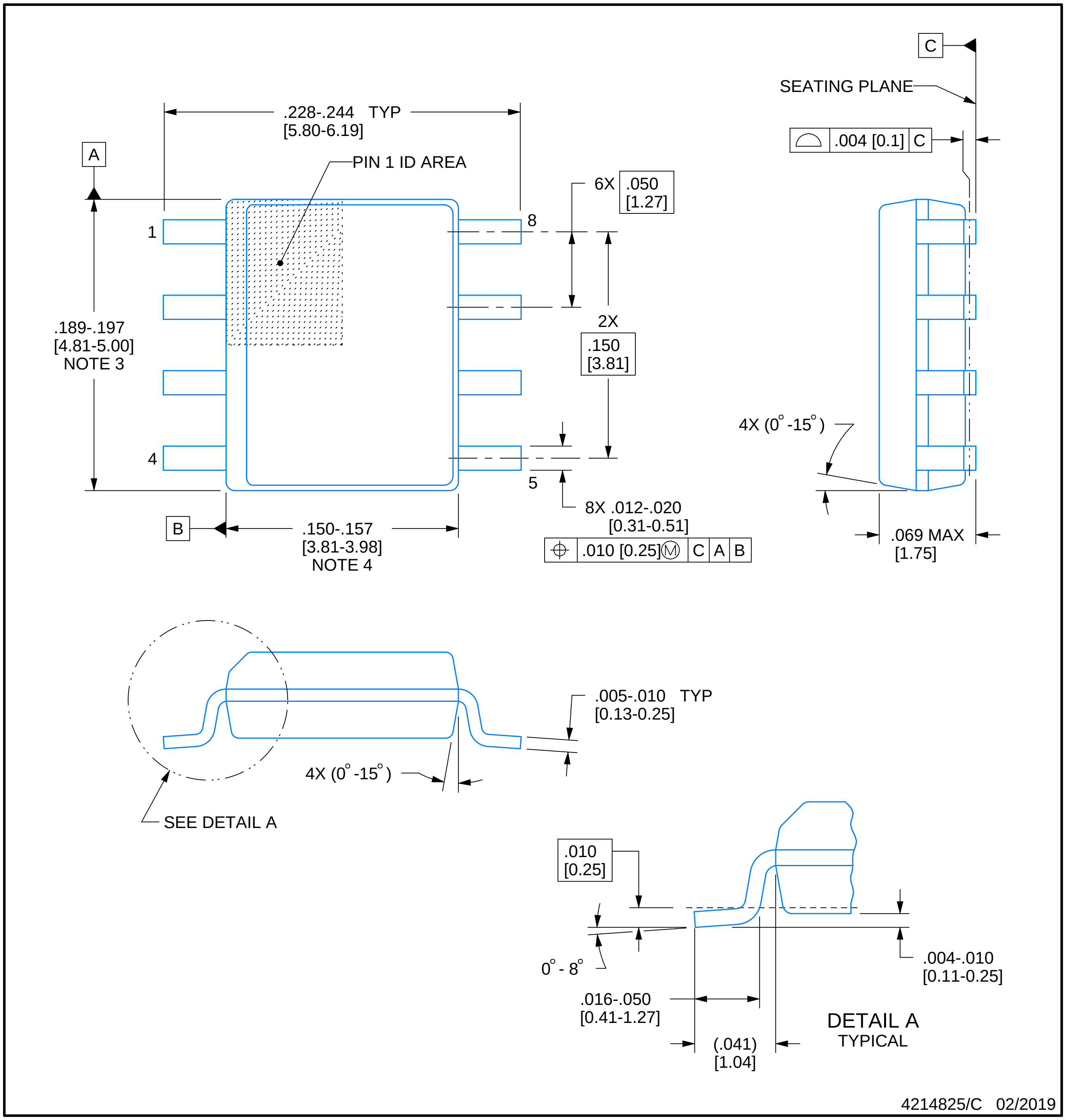
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1040QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



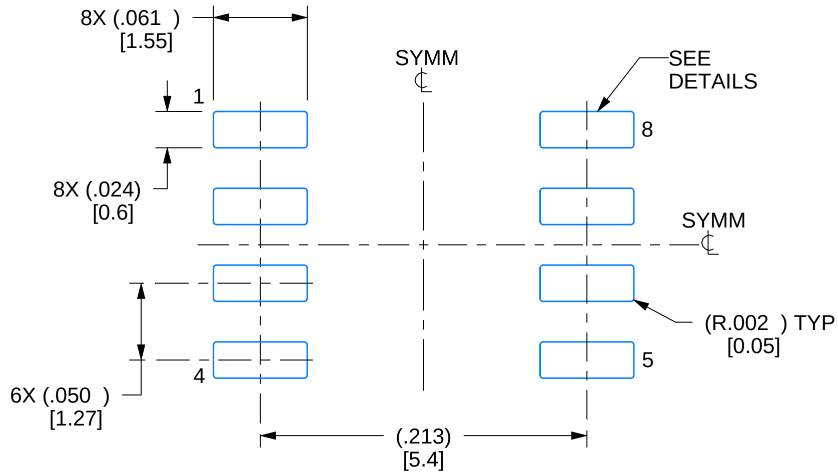
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1040QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

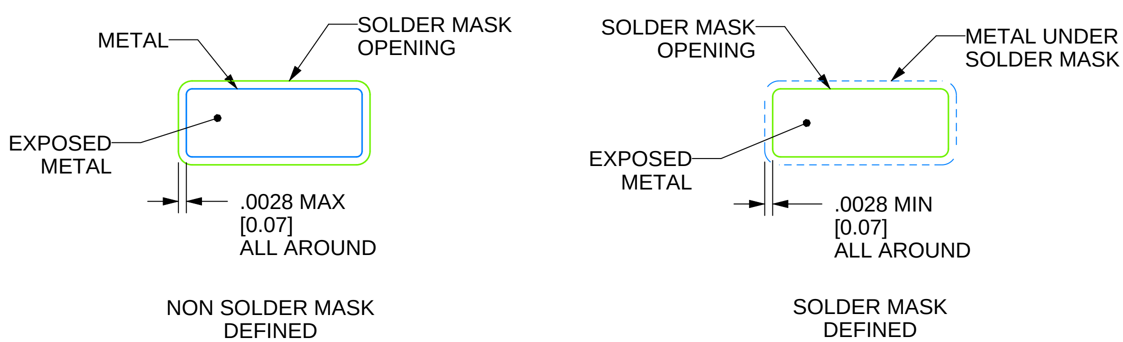


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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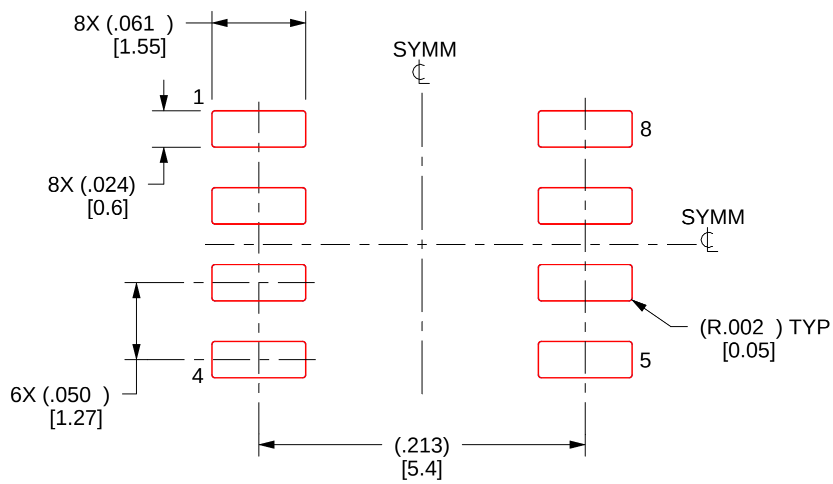
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.