

# SN54ABT162823A, SN74ABT162823A 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS666B – JULY 1996 – REVISED JUNE 2004

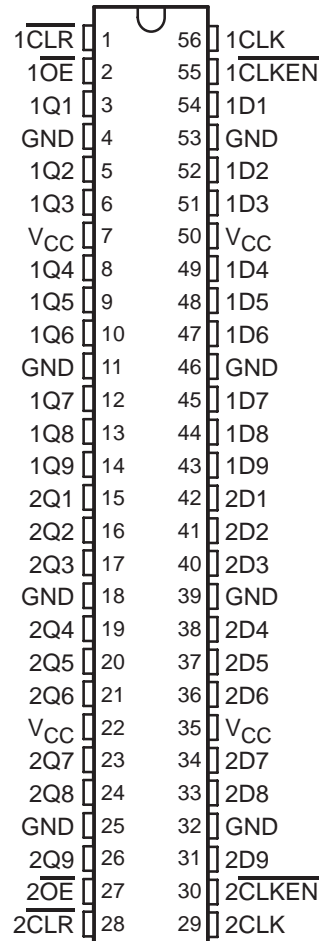
- **Members of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 25-Ω Series Resistors So No External Resistors Are Required**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $<1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**
- **High-Impedance State During Power Up and Power Down**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**

## description/ordering information

These 18-bit bus-interface flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT162823A devices can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

SN54ABT162823A . . . WD PACKAGE  
SN74ABT162823A . . . DGG OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ABT162823ADL	ABT162823A
		Tape and reel	SN74ABT162823ADLR	
	TSSOP – DGG	Tape and reel	SN74ABT162823ADGGR	ABT162823A
-55°C to 125°C	CFP – WD	Tube	SNJ54ABT162823AWD	SNJ54ABT162823AWD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN54ABT162823A, SN74ABT162823A

## 18-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### description/ordering information (continued)

A buffered output-enable ( $\overline{OE}$ ) input places the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.  $\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25- $\Omega$  series resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using  $I_{OFF}$  and power-up 3-state. The  $I_{OFF}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  shall be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

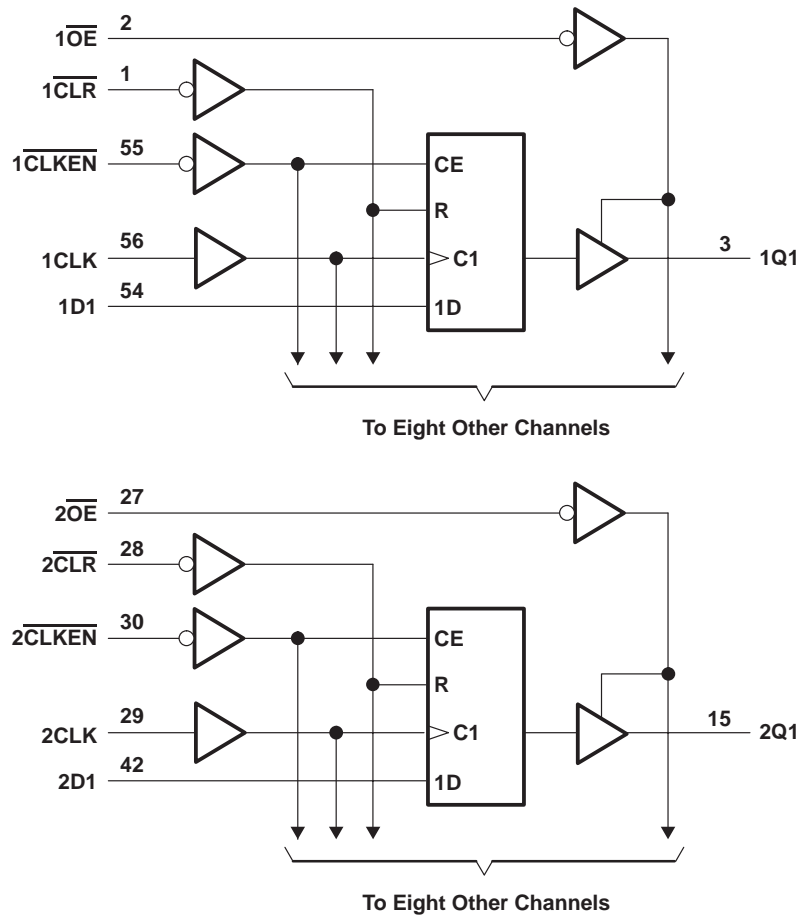
FUNCTION TABLE  
(each 9-bit flip-flop)

INPUTS					OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	L	L	X	$Q_0$
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

# SN54ABT162823A, SN74ABT162823A 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## 18-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

			SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage		2		2		V
$V_{IL}$	Low-level input voltage			0.8		0.8	V
$V_I$	Input voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current			-3		-12	mA
$I_{OL}$	Low-level output current			8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Input transition rise or fall rate		200		200		$\mu$ s/V
$T_A$	Operating free-air temperature		-55	125	-40	85	$^{\circ}$ C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$T_A = 25^{\circ}\text{C}$			SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$				-1.2		-1.2		-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -1\text{ mA}$		2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -1\text{ mA}$		3			3		3		
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4			2.4		2.4		
		$I_{OH} = -12\text{ mA}$	2*					2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 8\text{ mA}$		0.4			0.8		0.65	V
		$I_{OL} = 12\text{ mA}$			0.8*				0.8	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$ or GND				$\pm 1$		$\pm 1$		$\pm 1$	$\mu$ A
$I_{OZPU}$	$V_{CC} = 0$ to $2.1\text{ V}$ , $V_O = 0.5\text{ V}$ to $2.7\text{ V}$ , $\overline{OE} = X$				$\pm 50$		$\pm 50$		$\pm 50$	$\mu$ A
$I_{OZPD}$	$V_{CC} = 2.1\text{ V}$ to $0$ , $V_O = 0.5\text{ V}$ to $2.7\text{ V}$ , $\overline{OE} = X$				$\pm 50$		$\pm 50$		$\pm 50$	$\mu$ A
$I_{OZH}^{\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$				10		10		10	$\mu$ A
$I_{OZL}^{\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$				-10		-10		-10	$\mu$ A
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5\text{ V}$				$\pm 100$				$\pm 100$	$\mu$ A
$I_{CEX}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$	Outputs high			50		50		50	$\mu$ A
$I_{O}^{\S}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$		-25	-55	-100	-25	-100	-25	-100	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high			0.5		0.5		0.5	mA
		Outputs low			80		80		80	
		Outputs disabled			0.5		0.5		0.5	
$\Delta I_{CC}^{\P}$	$V_{CC} = 5.5\text{ V}$ , One input at $3.4\text{ V}$ , Other inputs at $V_{CC}$ or GND				1.5		1.5		1.5	mA
$C_i$	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$			3.5						pF
$C_O$	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$			9						pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than  $V_{CC}$  or GND.

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# SN54ABT162823A, SN74ABT162823A 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5\text{ V}$ , $T_A = 25^{\circ}\text{C}$		SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		150		150		150		MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
$t_{\text{su}}$	Setup time before CLK $\uparrow$	$\overline{\text{CLR}}$ inactive	1.6		2		1.6		ns
		Data	2		2		2		
		$\overline{\text{CLKEN}}$ low	2.8		2.8		2.8		
$t_h$	Hold time after CLK $\uparrow$	Data	1.2		1.2		1.2		ns
		$\overline{\text{CLKEN}}$ low	0.6		0.6		0.6		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT162823A		SN74ABT162823A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150			150		150		MHz
$t_{\text{PLH}}$	CLK	Q	2.3	4.6	6.2	2.3	8.4	2.3	7.5	ns
$t_{\text{PHL}}$			2.8	4.6	6.1	2.8	7.1	2.8	6.7	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	2.8	5	6.3	2.8	7.2	2.8	7	ns
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1.7	3.8	5	1.7	5.8	1.7	5.9	ns
$t_{\text{PZL}}$			3	5	6.1	3	7.2	3	7	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	2.6	4.8	6.1	2.6	7.3	2.6	6.6	ns
$t_{\text{PLZ}}$			1.9	4.6	6.7	1.9	10.2	1.9	9	

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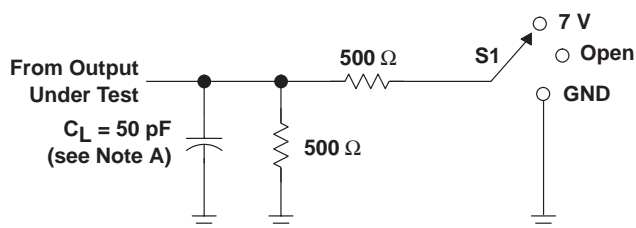
# SN54ABT162823A, SN74ABT162823A

## 18-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### PARAMETER MEASUREMENT INFORMATION

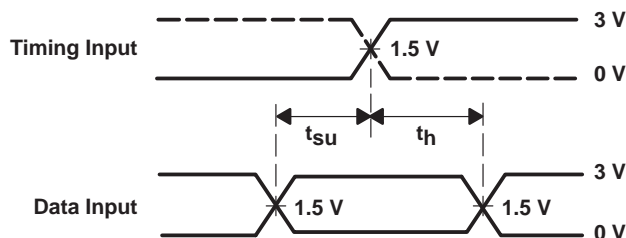


LOAD CIRCUIT

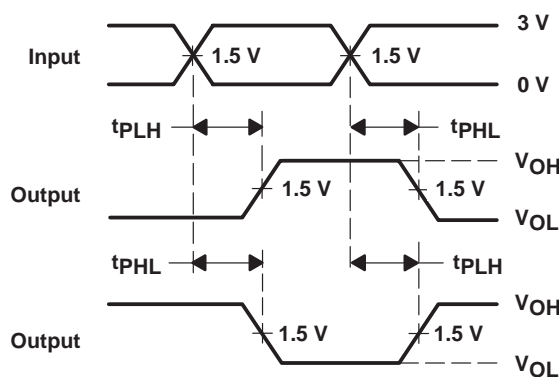
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



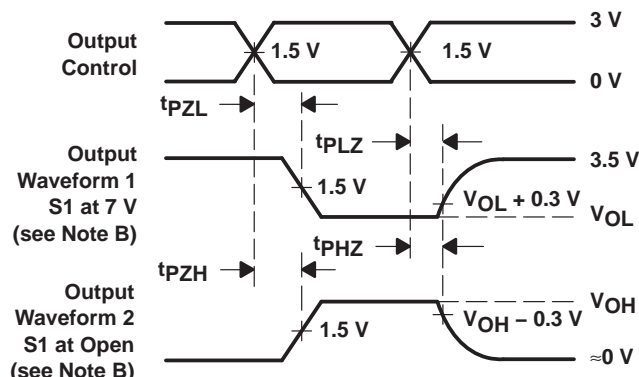
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74ABT162823ADL</a>	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162823A
SN74ABT162823ADL.B	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162823A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TUBE



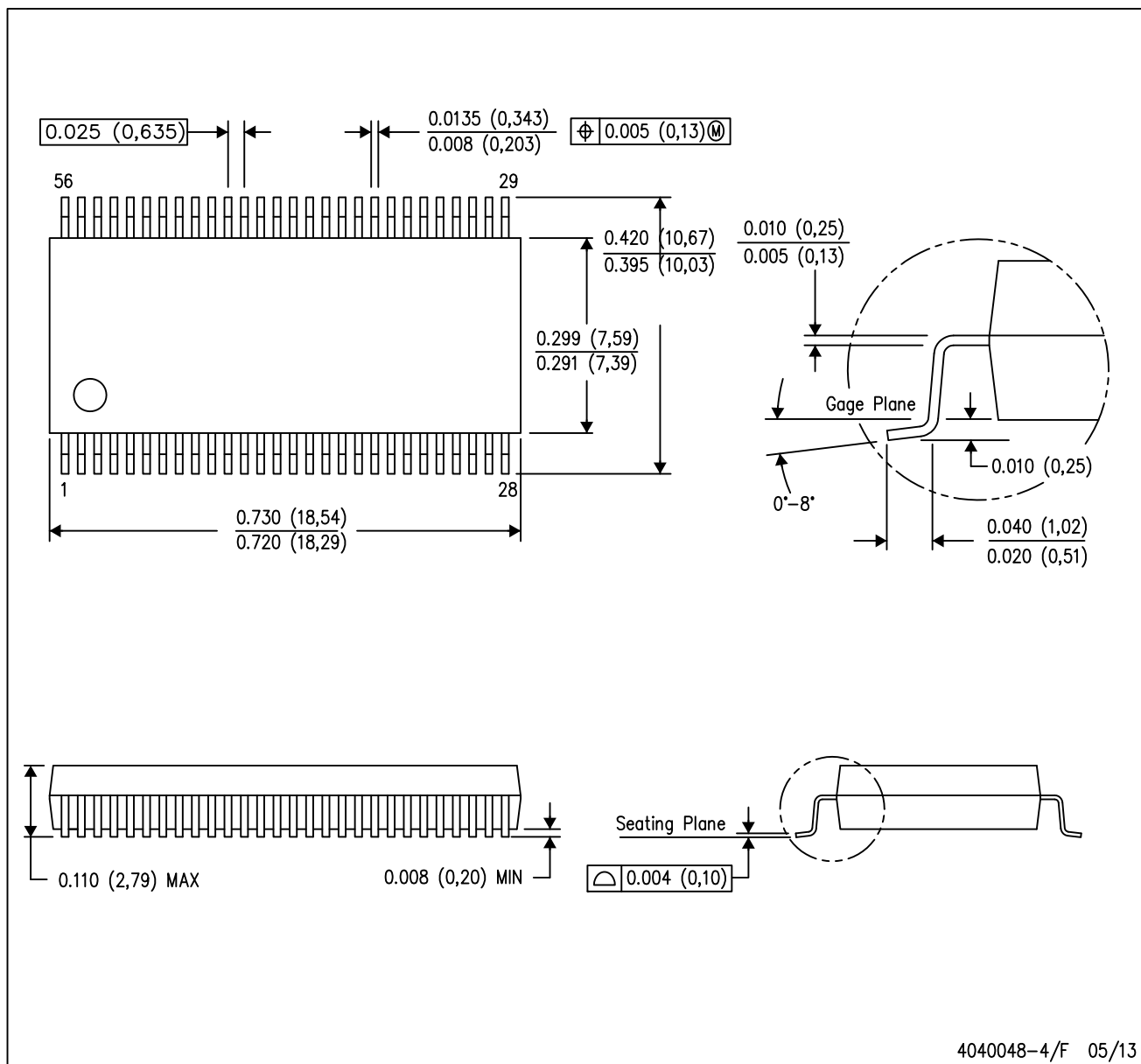
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT162823ADL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT162823ADL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87



DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed  $0.006$  (0,15).
  - Falls within JEDEC MO-118

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