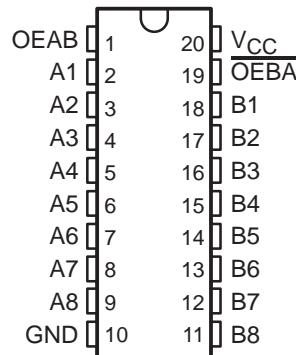
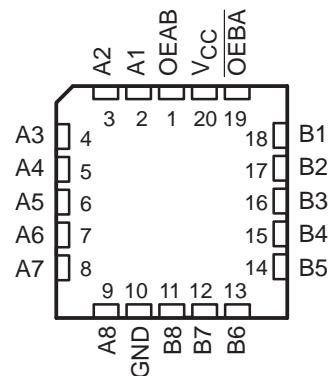


- State-of-the-Art **EPIC-IITM** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (-32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (N) and Ceramic (JT) DIPs

SN54ABT623A . . . JT OR W PACKAGE
SN74ABT623 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT623A . . . FK PACKAGE
(TOP VIEW)



description

The SN54ABT623A and SN74ABT623 bus transceivers are designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing. The SN54ABT623A and SN74ABT623 provide true data at their outputs.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable (OEAB and \overline{OEBA}) inputs.

The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and \overline{OEBA} . Each output reinforces its input in this configuration. When both OEAB and \overline{OEBA} are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 total) remain at their last states.

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT623A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT623 is characterized for operation from -40°C to 85°C .



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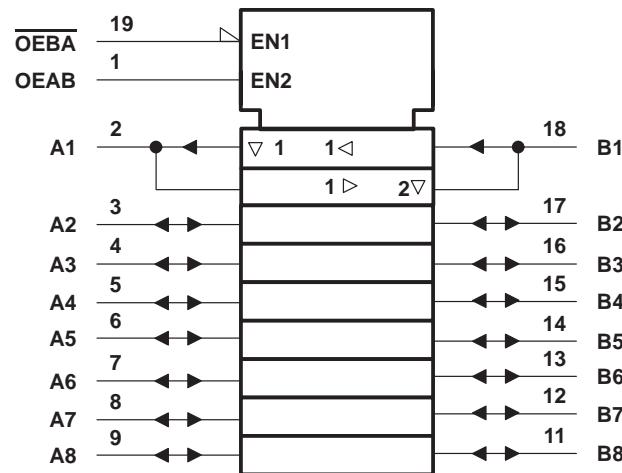
SN54ABT623A, SN74ABT623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS114D – FEBRUARY 1991 – REVISED MAY 1997

FUNCTION TABLE

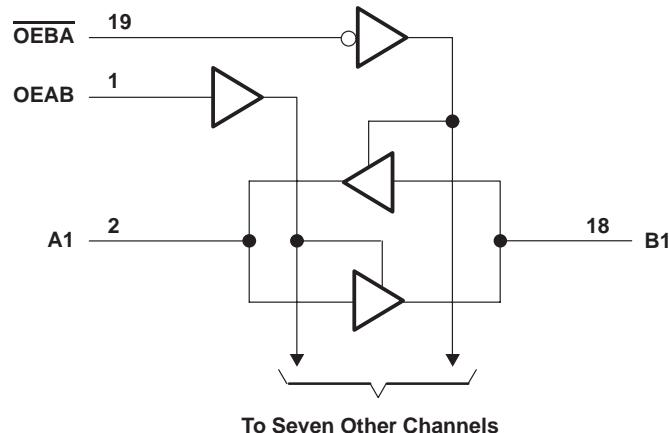
INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V	
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V	
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V	
Current into any output in the low state, I_O : SN54ABT623A	96 mA	
SN74ABT623	128 mA	
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA	
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA	
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W	
DW package	97°C/W	
N package	67°C/W	
PW package	128°C/W	
Storage temperature range, T_{stg}	–65°C to 150°C	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT623A		SN74ABT623		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

**SN54ABT623A, SN74ABT623
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

SCBS114D – FEBRUARY 1991 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA = 25°C			SN54ABT623A		SN74ABT623		UNIT
		MIN	TYPT†	MAX	MIN	MAX	MIN	MAX	
VIK	VCC = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
VOH	VCC = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	VCC = 5 V, I _{OH} = -3 mA	3			3		3		
	VCC = 4.5 V	I _{OH} = -24 mA	2		2				
		I _{OH} = -32 mA	2*				2		
VOL	VCC = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V
		I _{OL} = 64 mA		0.55*				0.55	
V _{hys}			100						mV
I _I	Control inputs A or B ports	VCC = 5.5 V, V _I = VCC or GND		±1	±1	±1			µA
				±100	±100	±100			
I _{OZH} ‡	VCC = 5.5 V, V _O = 2.7 V			50**		10		50	µA
I _{OZL} ‡	VCC = 5.5 V, V _O = 0.5 V			-50**		-10		-50	µA
I _{off}	VCC = 0, V _I or V _O ≤ 4.5 V			±100				±100	µA
I _{CEX}	VCC = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	µA
I _O §	VCC = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-180	-50	mA
I _{CC}	A or B ports	VCC = 5.5 V, I _O = 0, V _I = VCC or GND	Outputs high	5	250	250	250	250	µA
			Outputs low	22	30	30	30	30	mA
			Outputs disabled	1	250	250	250	250	µA
ΔI _{CC} ¶	Data inputs	VCC = 5.5 V, One input at 3.4 V, Other inputs at VCC or GND	Outputs enabled		1.5	1.5	1.5		mA
			Outputs disabled		0.05	0.05	0.05		
	Control inputs	VCC = 5.5 V, One input at 3.4 V, Other inputs at VCC or GND			1.5	1.5	1.5		
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4					pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		7					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** These limits apply only to the SN74ABT623.

† All typical values are at VCC = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54ABT623A, SN74ABT623
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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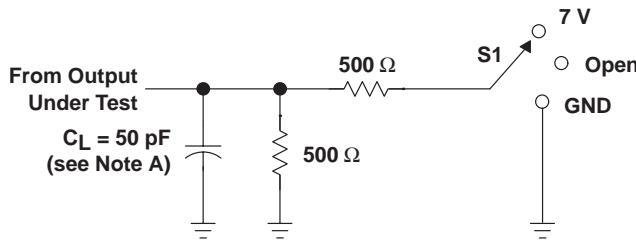
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$			SN54ABT623A	SN74ABT623	UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	2.6	4.1	1	4	1 4.6
t_{PHL}			1	2.6	4.2	0.8	4.1	1 4.6
t_{PZH}	OEBA	A	1.7	3.4	6.5	1.2	5.4	1.7 7.5
t_{PZL}			1.7	3.8	6.5	1.5	6.8	1.7 7.5
t_{PHZ}	OEBA	A	1.7	4.2	6.5	1.7	7.1	1.7 7.5
t_{PLZ}			1.7	4.7	6.5	1.5	7.1	1.7 7.5
t_{PZH}	OEAB	B	1.7	4.8	6.5	1.2	6.8	1.7 7.5
t_{PZL}			1.7	4	6.5	1.7	6.5	1.7 7.5
t_{PHZ}	OEAB	B	1.7	3.9	6.5	1.5	6.8	1.7 7.5
t_{PLZ}			1.7	3.2	6.5	1.3	5.8	1.7 7.5

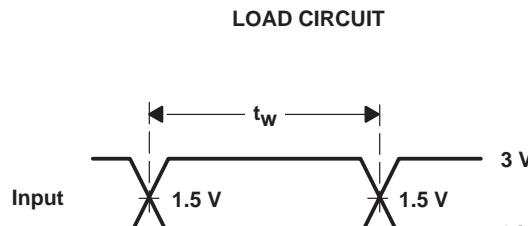
**SN54ABT623A, SN74ABT623
OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

SCBS114D – FEBRUARY 1991 – REVISED MAY 1997

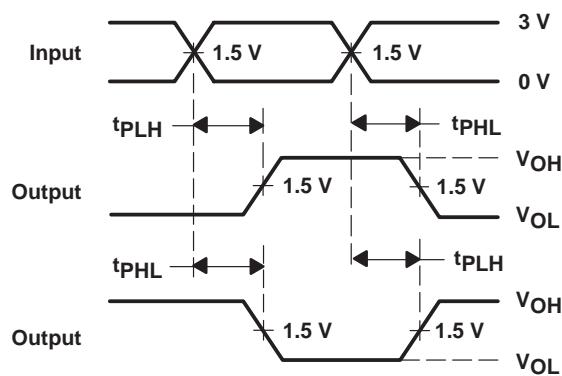
PARAMETER MEASUREMENT INFORMATION



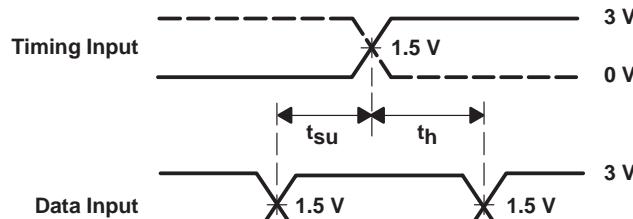
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



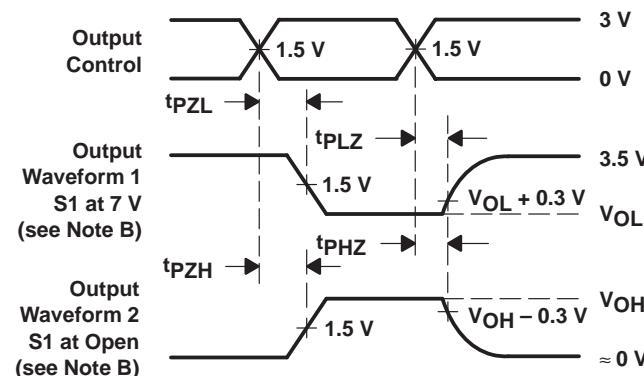
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9461801Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9461801Q2A SNJ54 ABT623AFK
5962-9461801QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9461801QR A SNJ54ABT623AJ
SN74ABT623DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB623
SN74ABT623DBR.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB623
SN74ABT623DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT623
SN74ABT623DW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT623
SN74ABT623DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT623
SN74ABT623DWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT623
SN74ABT623N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT623N
SN74ABT623N.B	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ABT623N
SN74ABT623PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB623
SN74ABT623PWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB623
SNJ54ABT623AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9461801Q2A SNJ54 ABT623AFK
SNJ54ABT623AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9461801QR A SNJ54ABT623AJ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

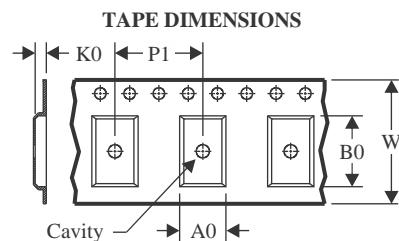
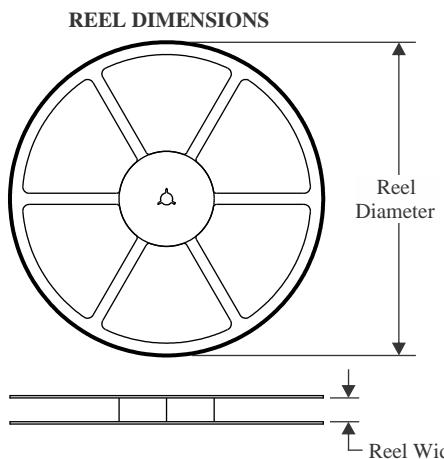
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

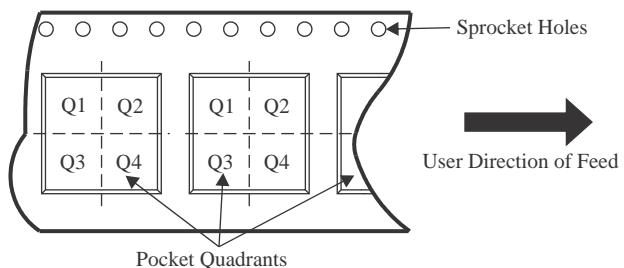
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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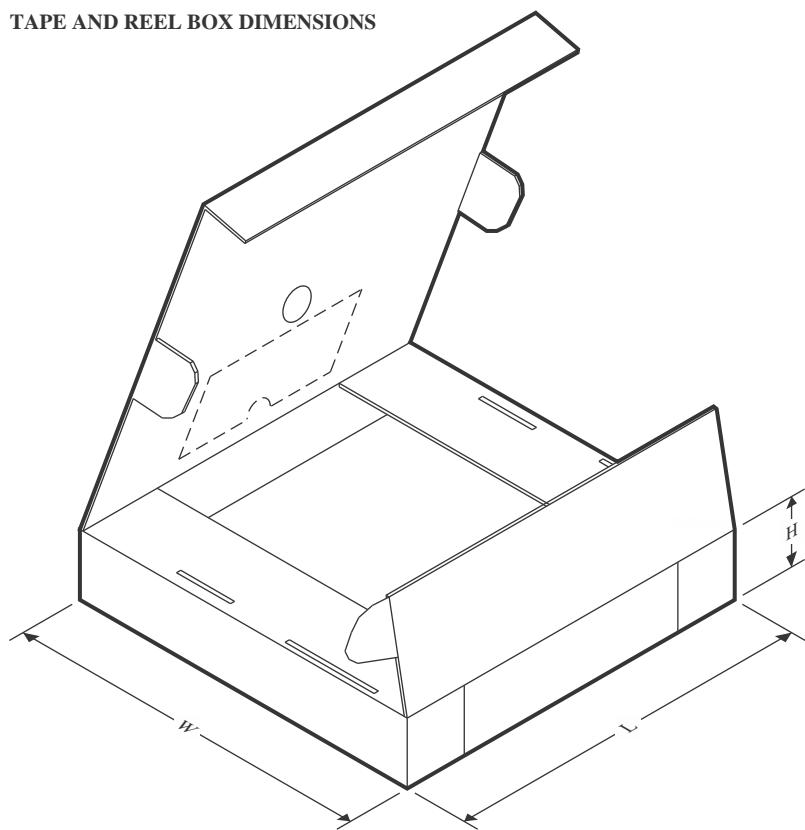
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


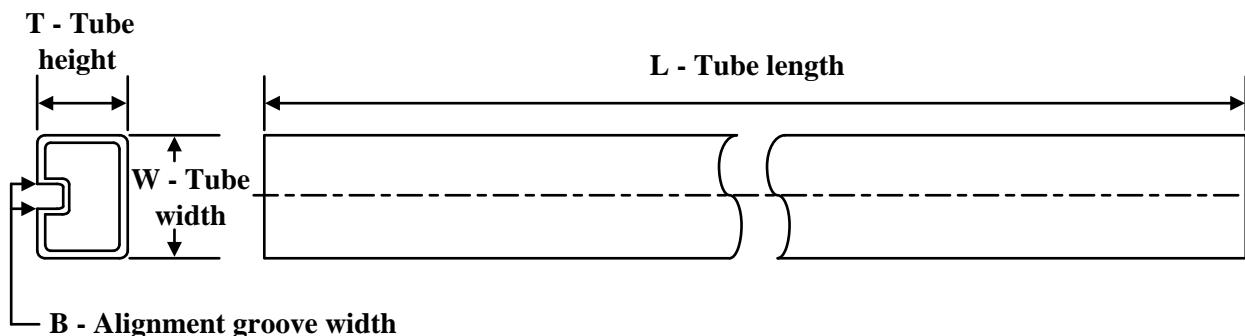
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT623DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT623DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT623PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT623DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ABT623DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ABT623PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-9461801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ABT623DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT623DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT623N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT623N.B	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ABT623AFK	FK	LCCC	20	55	506.98	12.06	2030	NA

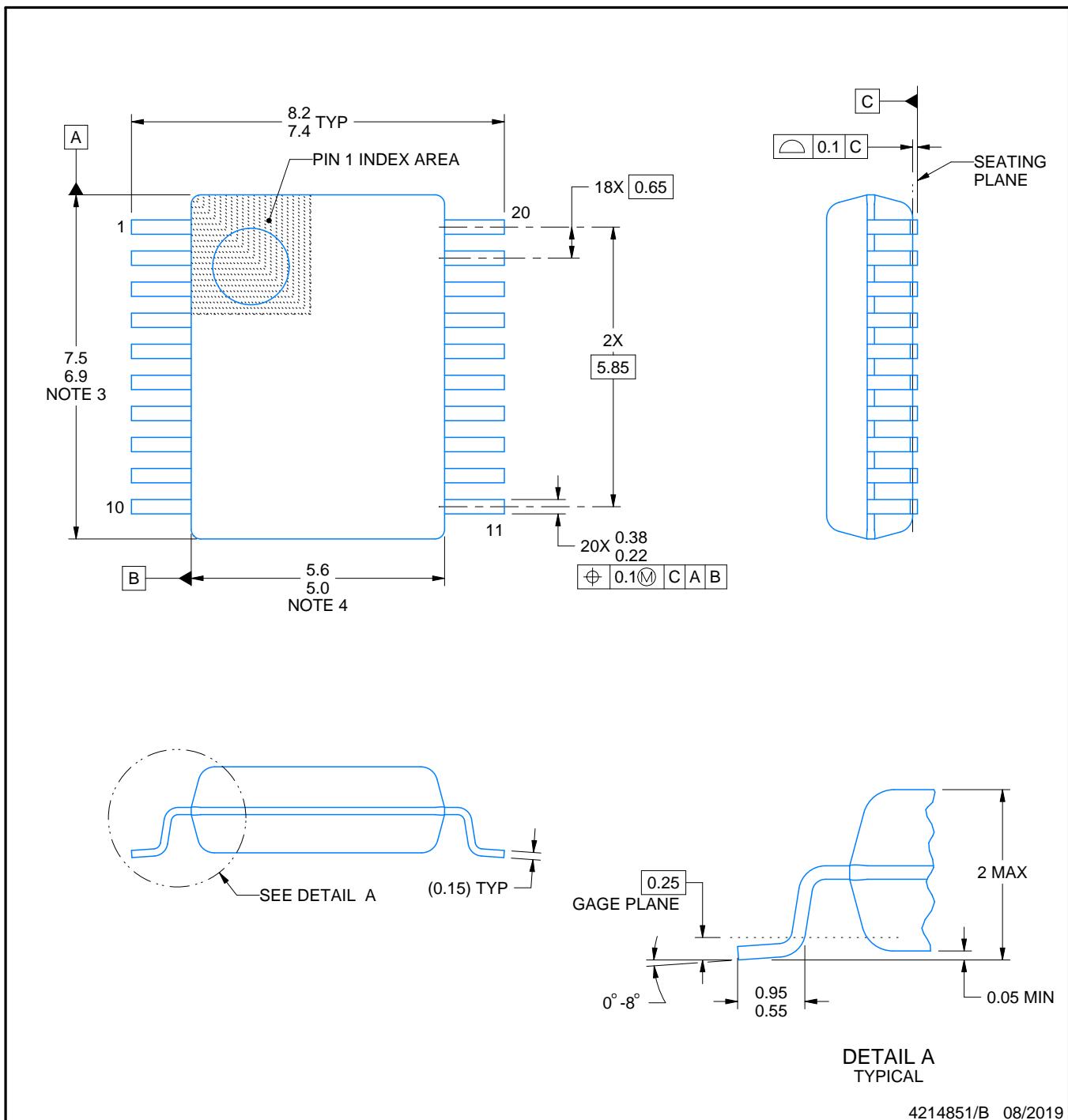
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

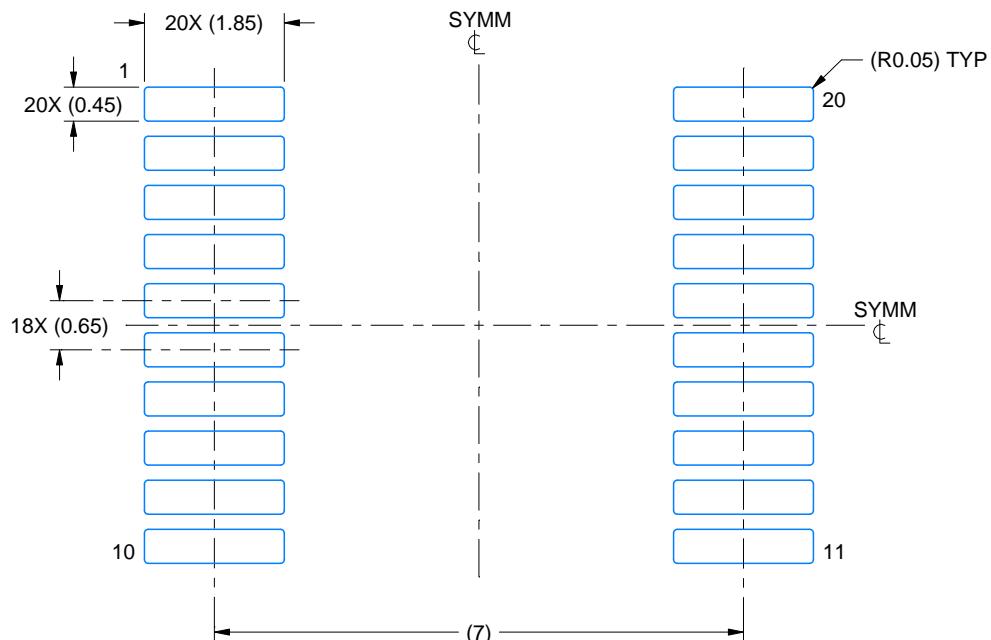
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

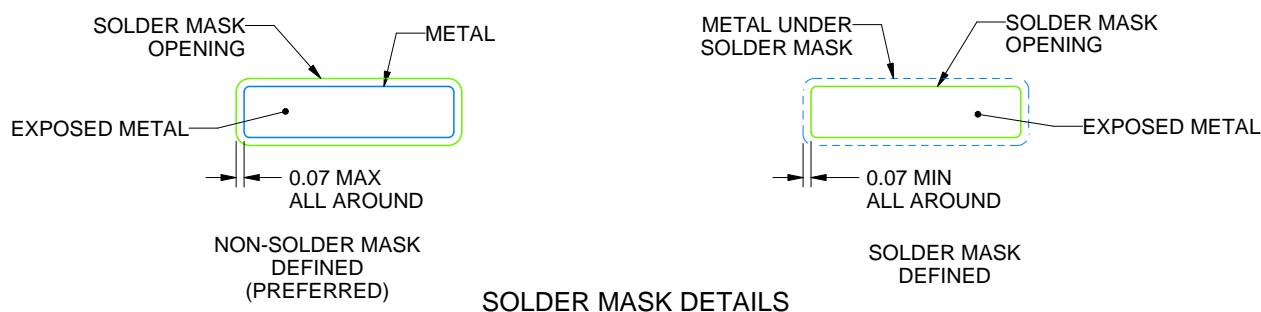
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

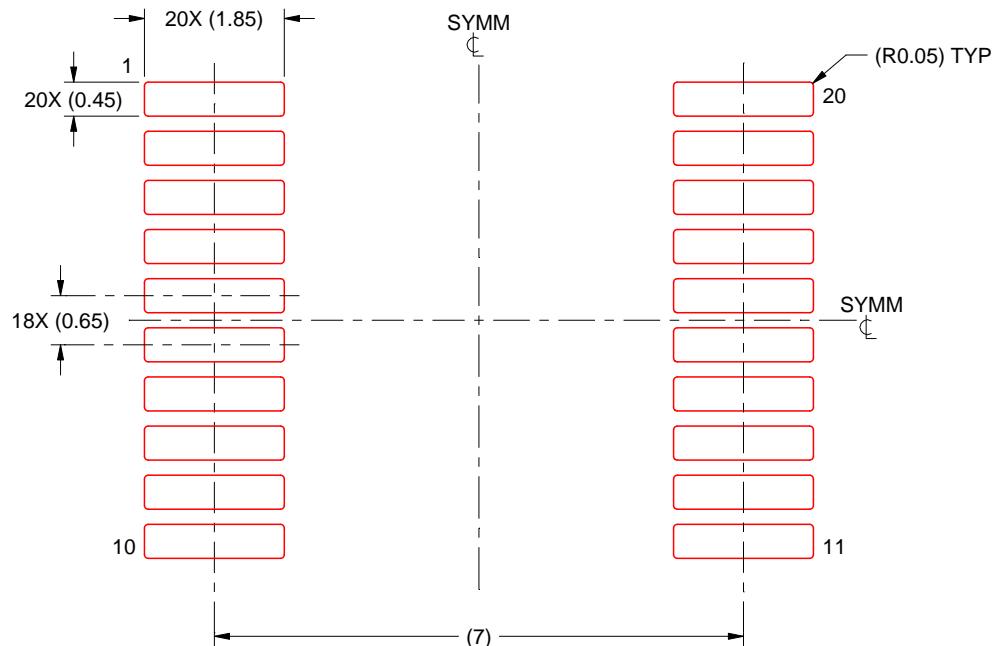
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X**

4214851/B 08/2019

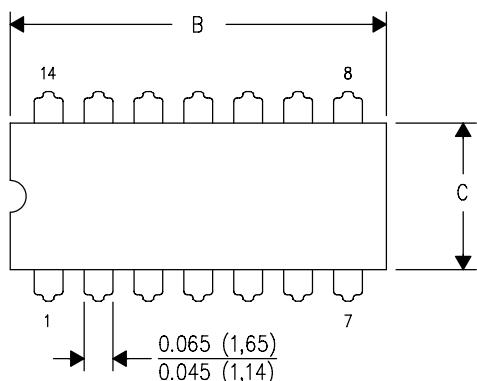
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
 9. Board assembly site may have different recommendations for stencil design.

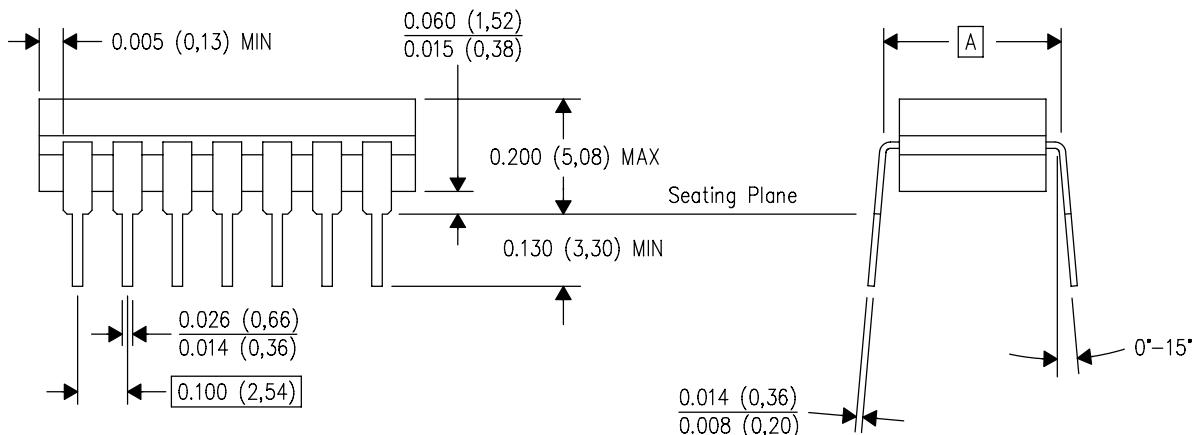
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

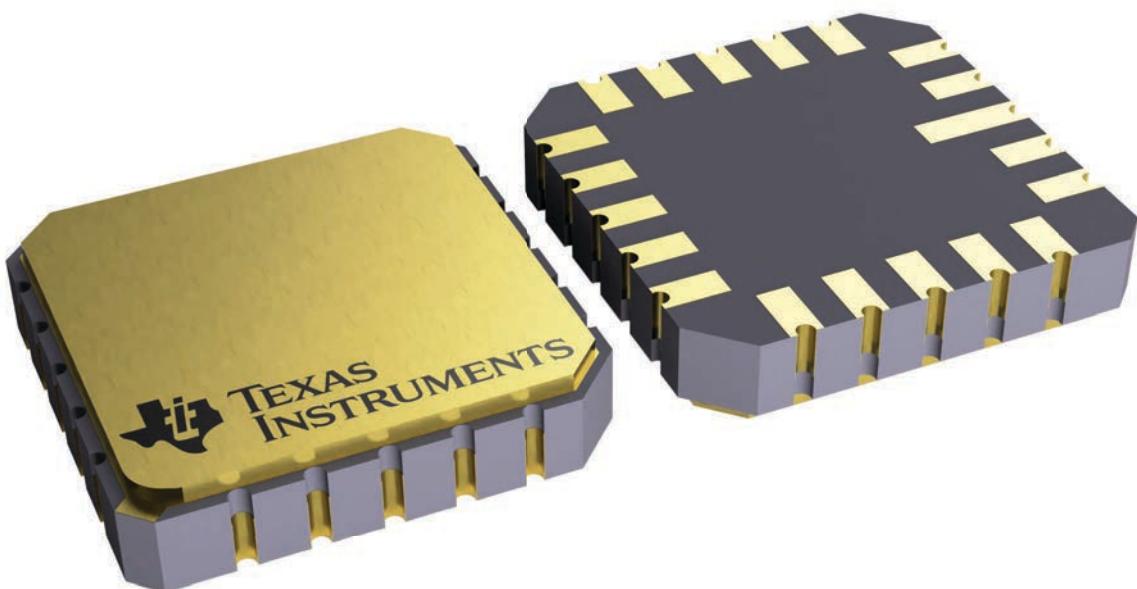
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

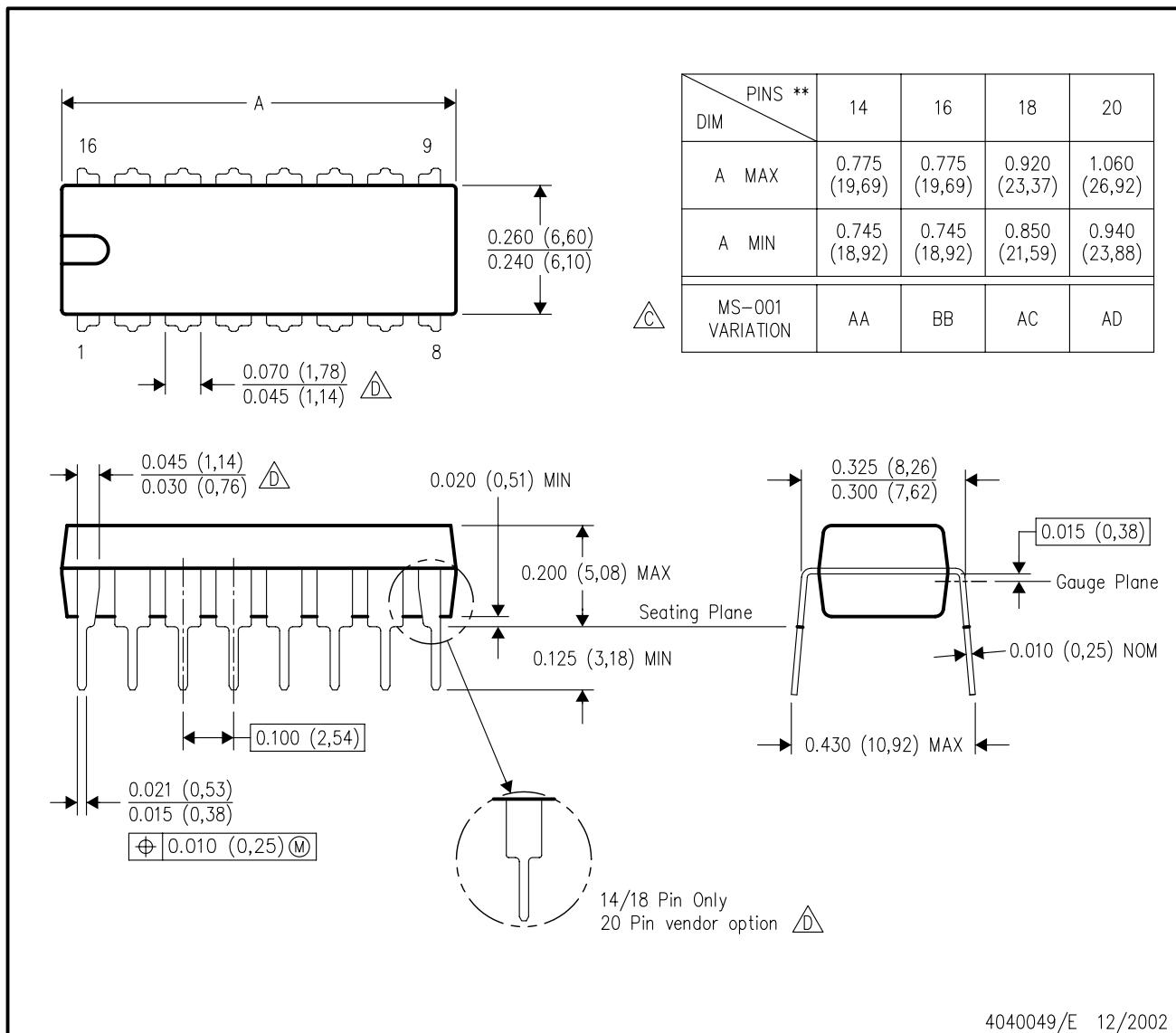


4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

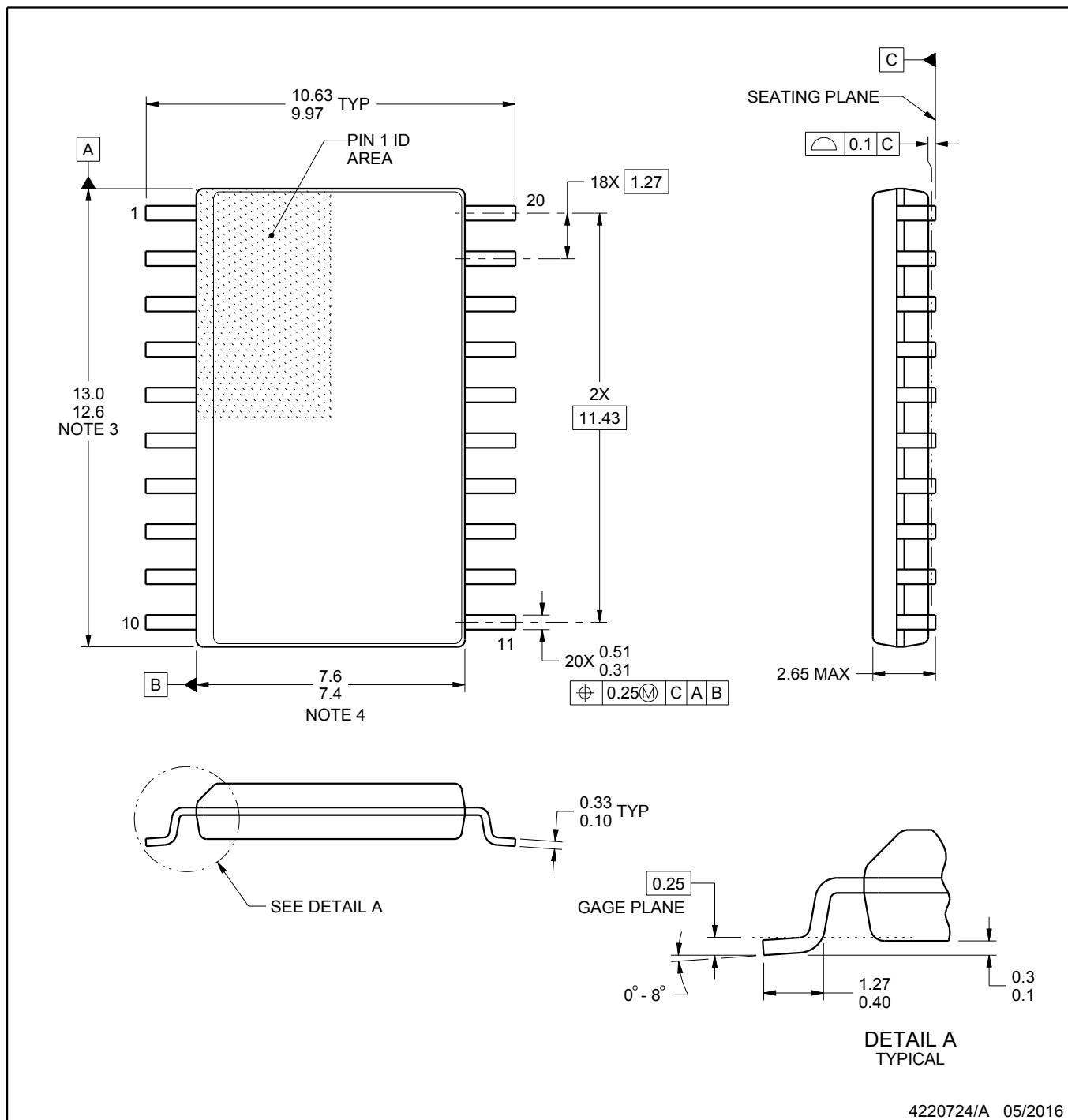


PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

SOIC



NOTES:

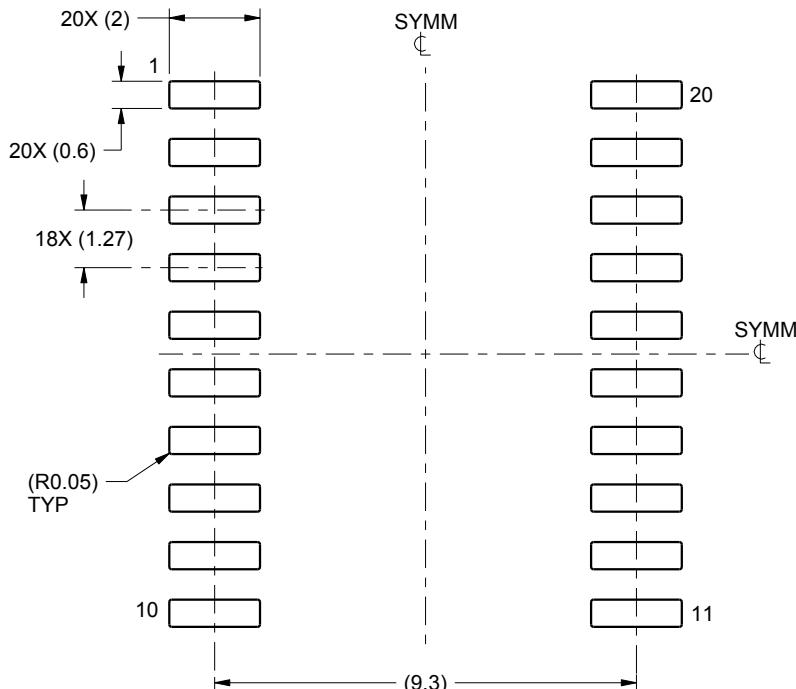
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
 5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

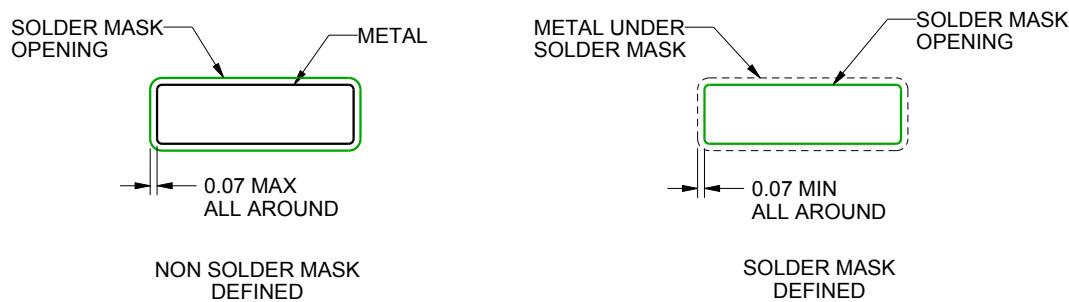
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

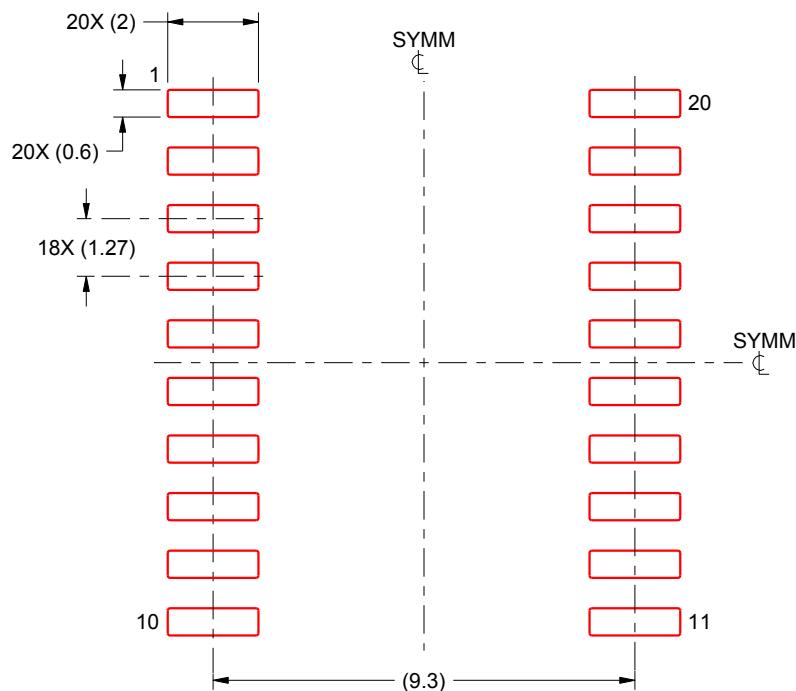
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

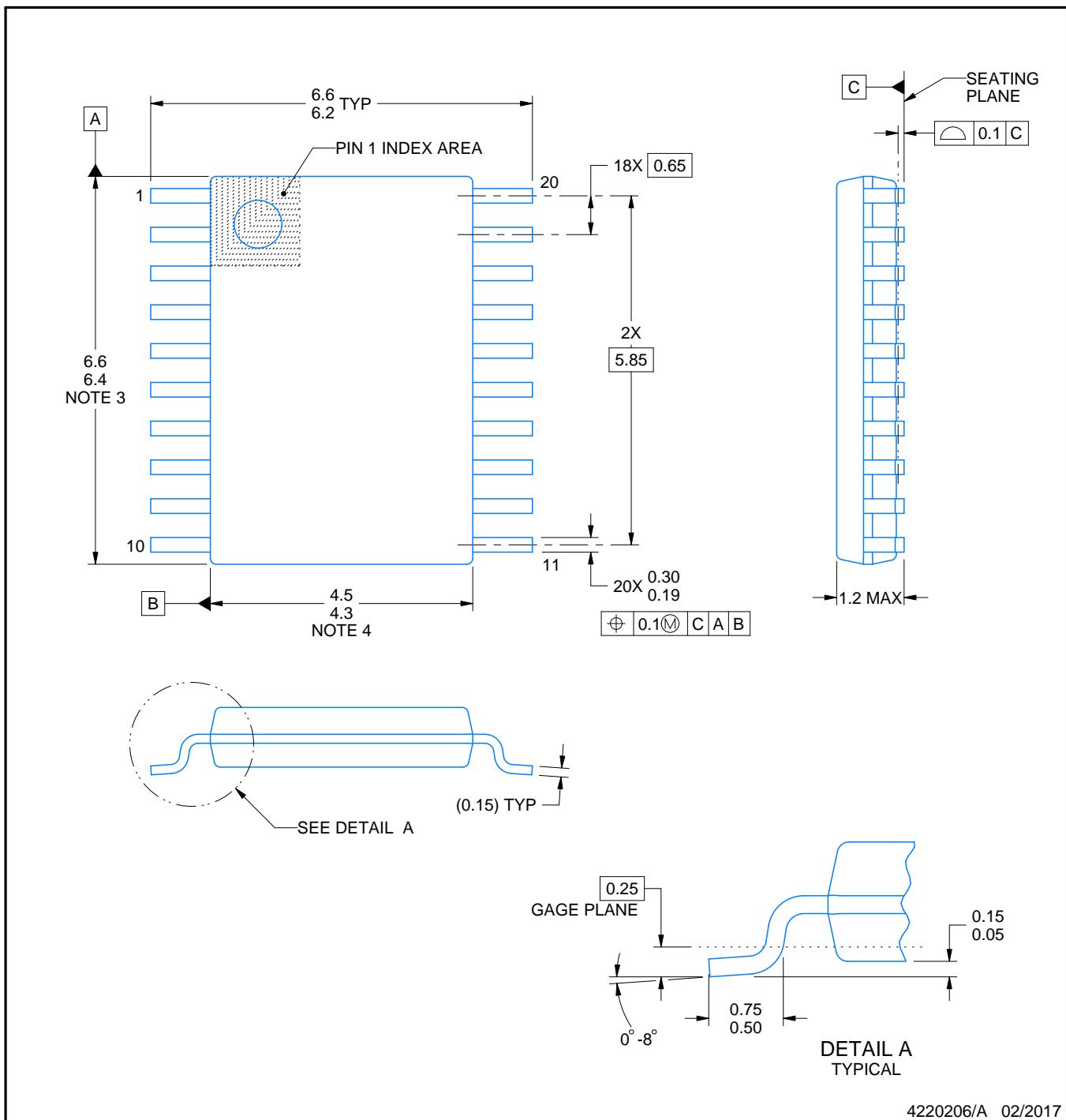
PACKAGE OUTLINE

PW0020A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

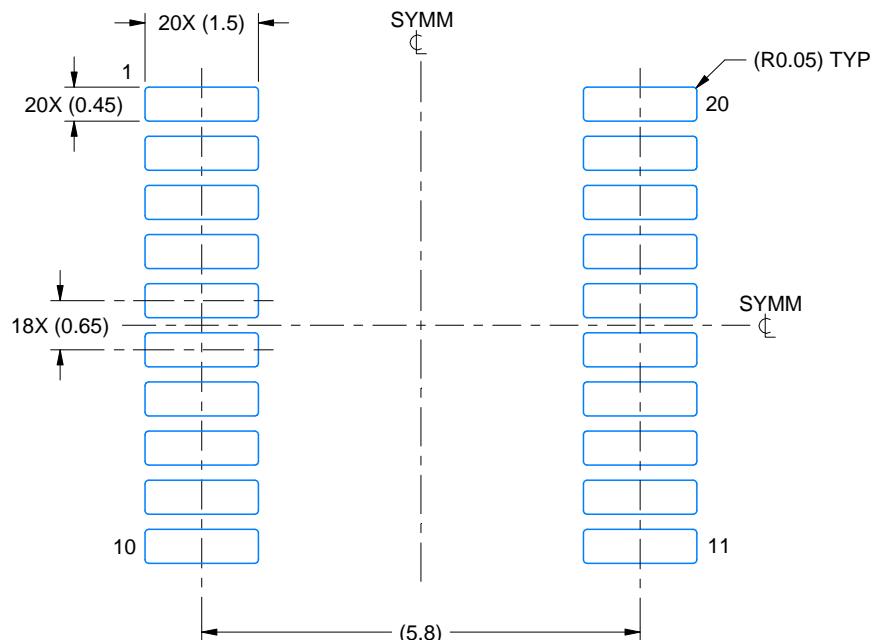
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
 5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

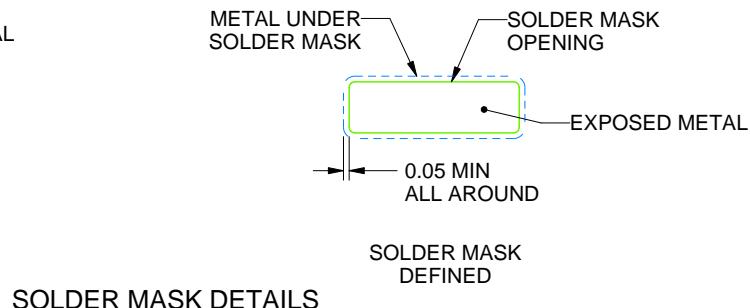
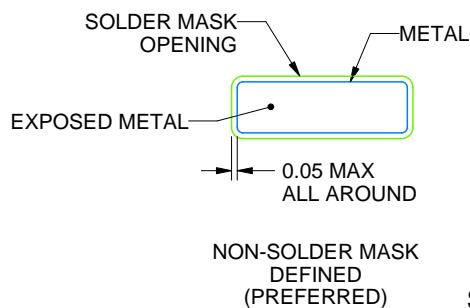
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

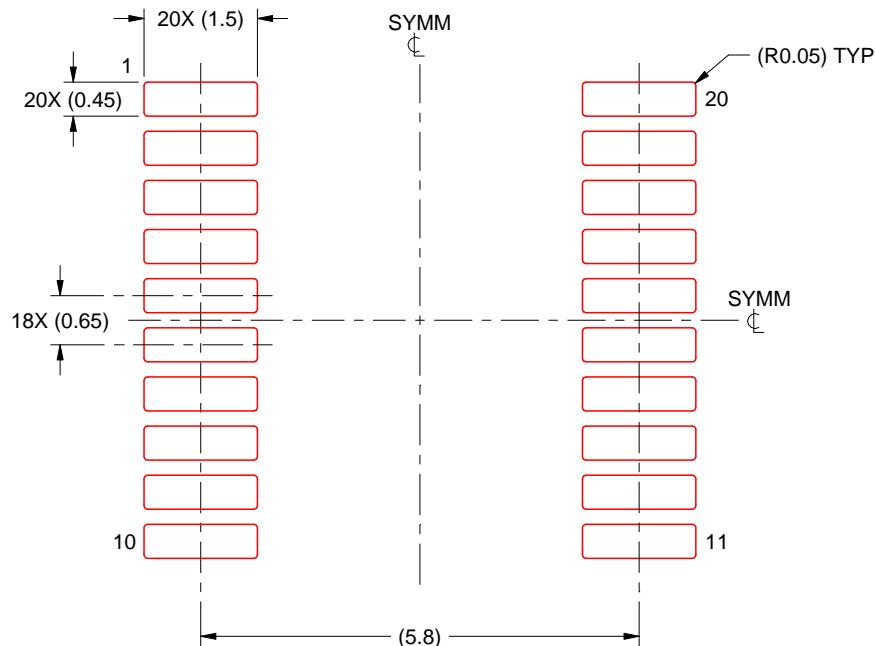
6. Publication IPC-7351 may have alternate designs.
 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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