

# SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation:**
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- **Operate With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for n-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - Stacked or Push-Down Registers
  - Buffer Storage
  - Accumulator Registers
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

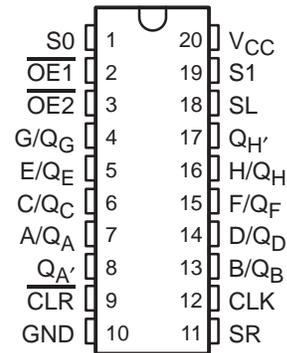
## description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select ( $S_0$ ,  $S_1$ ) inputs and two output-enable ( $\overline{OE1}$ ,  $\overline{OE2}$ ) inputs can be used to choose the modes of operation listed in the function table.

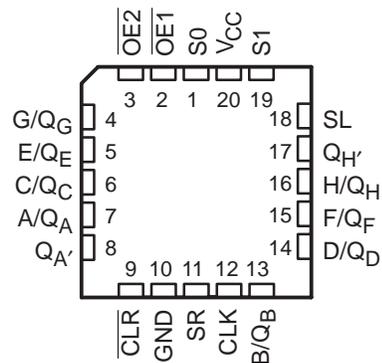
Synchronous parallel loading is accomplished by taking both  $S_0$  and  $S_1$  high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when the clear ( $\overline{CLR}$ ) input is low. Taking either  $\overline{OE1}$  or  $\overline{OE2}$  high disables the outputs, but has no effect on clearing, shifting, or storing data.

The SN54ALS299 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS299 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS299 . . . J PACKAGE  
SN74ALS299 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS299 . . . FK PACKAGE  
(TOP VIEW)



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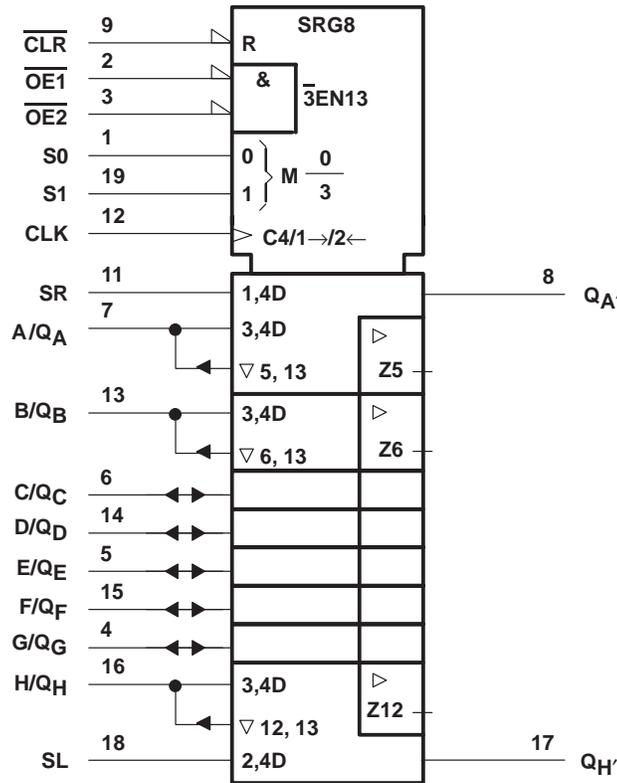
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	CLR	S1	S0	$\overline{OE1}\dagger$	$\overline{OE2}\dagger$	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

## logic symbol‡

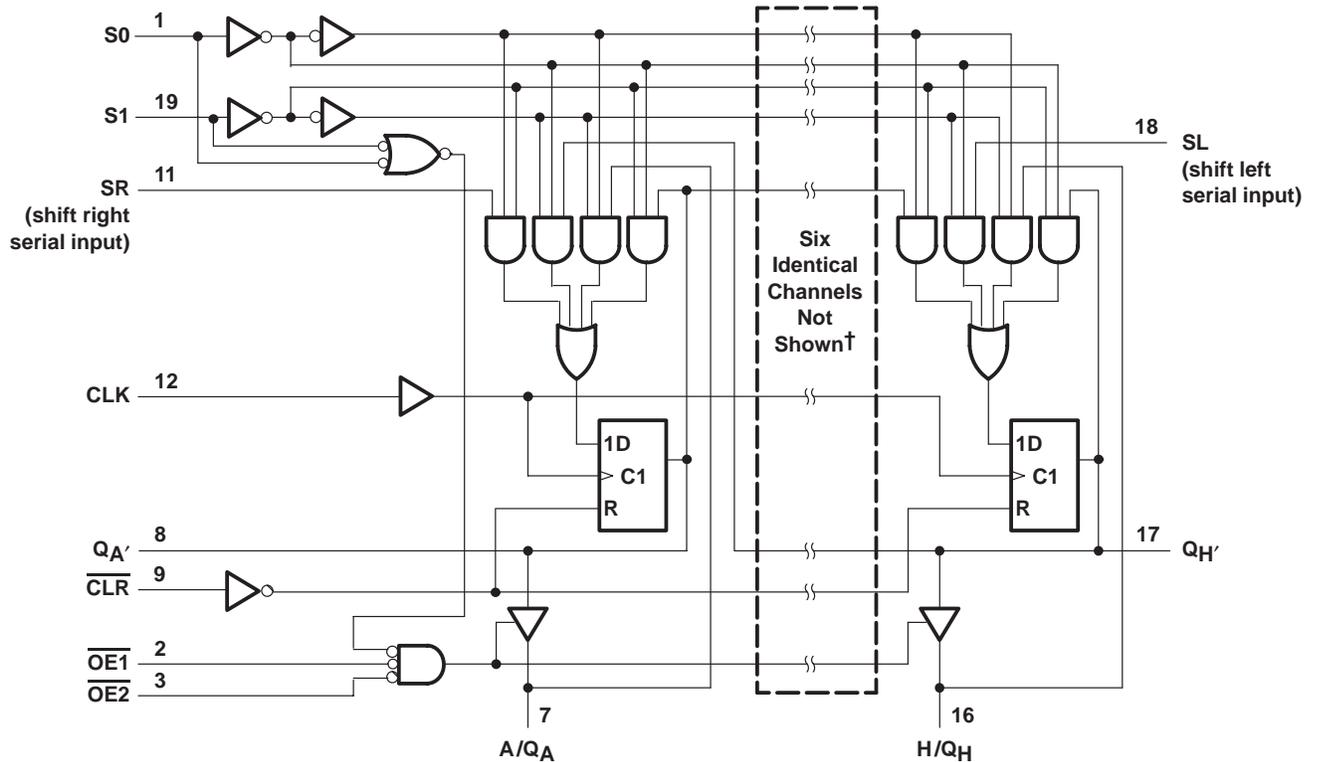


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## logic diagram (positive logic)



† I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS299	-55°C to 125°C
SN74ALS299	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN54ALS299, SN74ALS299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions

		SN54ALS299			SN74ALS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current	$Q_A'$ or $Q_H'$		-0.4			-0.4	mA
		$Q_A - Q_H$			-1			
$I_{OL}$	Low-level output current	$Q_A'$ or $Q_H'$		4		8		mA
		$Q_A - Q_H$		12		24		
$T_A$	Operating free-air temperature	-55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299			SN74ALS299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.5			-1.5			V
$V_{OH}$	All outputs	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
	$Q_A - Q_H$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$		2.4	3.3			2.4 3.2	
			$I_{OH} = -2.6\text{ mA}$							
$V_{OL}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$		0.25	0.4	0.25	0.4	V	
			$I_{OL} = 8\text{ mA}$				0.35	0.5		
	$Q_A - Q_H$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$		0.25	0.4	0.25	0.4		
			$I_{OL} = 24\text{ mA}$				0.35	0.5		
$I_I$	A – H	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$		0.1			0.1	mA	
	Any others		$V_I = 7\text{ V}$		0.1			0.1		
$I_{IH}^\ddagger$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		20			20	µA	
$I_{IL}^\ddagger$	S0, S1, SR, SL	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$		-0.2			-0.2	mA	
	Any others				-0.1			-0.1		
$I_{OS}^\S$	$Q_A'$ or $Q_H'$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$		-15	-70	-15	-70	mA	
	$Q_A - Q_H$				-20	-112	-30	-112		
$I_{CC}$	$V_{CC} = 5.5\text{ V}$		Outputs high		15	28	15	28	mA	
			Outputs low		22	38	22	38		
			Outputs disabled		23	40	23	40		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports ( $Q_A - Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

		SN54ALS299		SN74ALS299		UNIT	
		MIN	MAX	MIN	MAX		
$f_{\text{clock}}$	Clock frequency (at 50% duty cycle)	0	17	0	30	MHz	
$t_w$	Pulse duration	CLK high or low		16.5		ns	
		CLR low		10			
$t_{\text{su}}$	Setup time before CLK $\uparrow$	S0 or S1		20		ns	
		Serial or parallel data	High		16		
			Low		6		
	Inactive-state setup time before CLK $\uparrow$ $\dagger$	CLR		15			
$t_h$	Hold time after CLK $\uparrow$	S0 or S1		0		ns	
		Serial or parallel data		0			

$\dagger$  Inactive-state setup time is also referred to as recovery time.

## switching characteristics (see Figure 1)

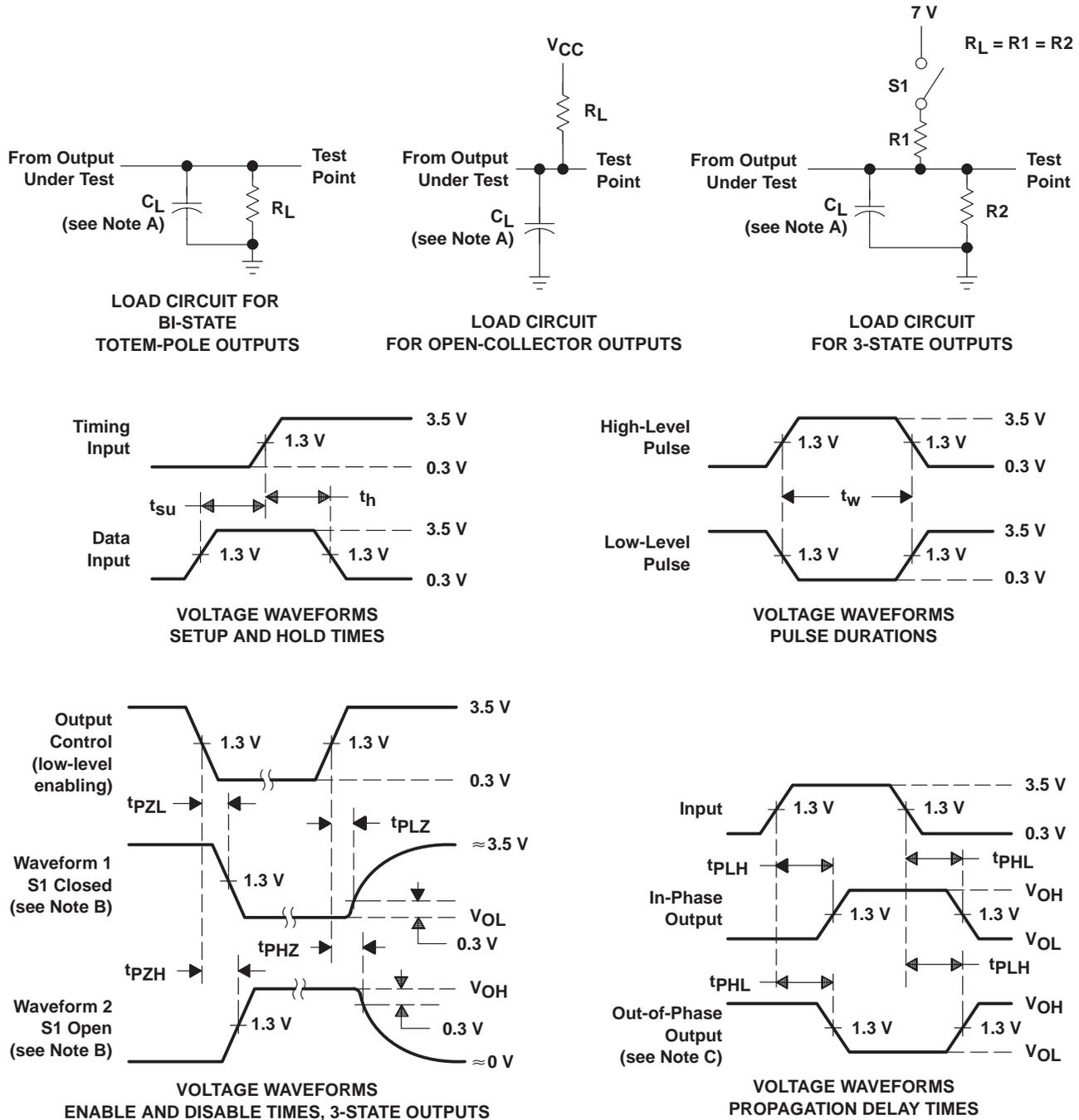
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}\ddagger$				UNIT
			SN54ALS299		SN74ALS299		
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			17		30	MHz	
$t_{\text{PLH}}$	CLK	$Q_A - Q_H$	2	19	4	13	ns
$t_{\text{PHL}}$			4	25	7	19	
$t_{\text{PLH}}$	CLK	$Q_{A'} \text{ or } Q_{H'}$	2	21	5	15	ns
$t_{\text{PHL}}$			4	25	8	18	
$t_{\text{PHL}}$	CLR	$Q_A - Q_H$	6	29	6	22	ns
		$Q_{A'} \text{ or } Q_{H'}$	6	29	6	22	
$t_{\text{PZH}}$	$\overline{OE1}, \overline{OE2}$	$Q_A - Q_H$	5	22	6	16	ns
$t_{\text{PZL}}$			6	27	8	22	
$t_{\text{PZH}}$	S0, S1	$Q_A - Q_H$	5	27	7	17	ns
$t_{\text{PZL}}$			6	26	8	22	
$t_{\text{PHZ}}$	$\overline{OE1}, \overline{OE2}$	$Q_A - Q_H$	1	15	1	8	ns
$t_{\text{PLZ}}$			4	38	5	15	
$t_{\text{PHZ}}$	S0, S1	$Q_A - Q_H$	1	16	1	12	ns
$t_{\text{PLZ}}$			4	34	8	25	

$\ddagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">83021012A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
<a href="#">8302101RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
<a href="#">8302101SA</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W
<a href="#">SN74ALS299DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS299
SN74ALS299DW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS299
<a href="#">SN74ALS299N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS299N
SN74ALS299N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS299N
<a href="#">SNJ54ALS299FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
SNJ54ALS299FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
<a href="#">SNJ54ALS299J</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
SNJ54ALS299J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
<a href="#">SNJ54ALS299W</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W
SNJ54ALS299W.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

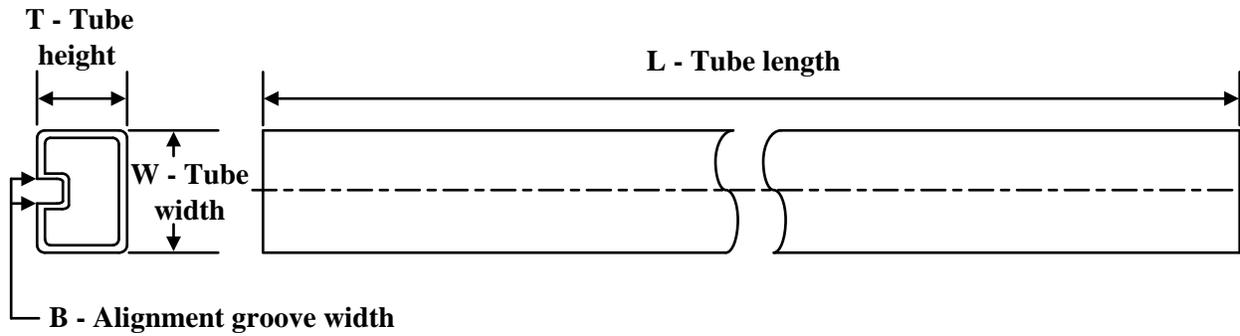
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS299, SN74ALS299 :**

- Catalog : [SN74ALS299](#)
- Military : [SN54ALS299](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

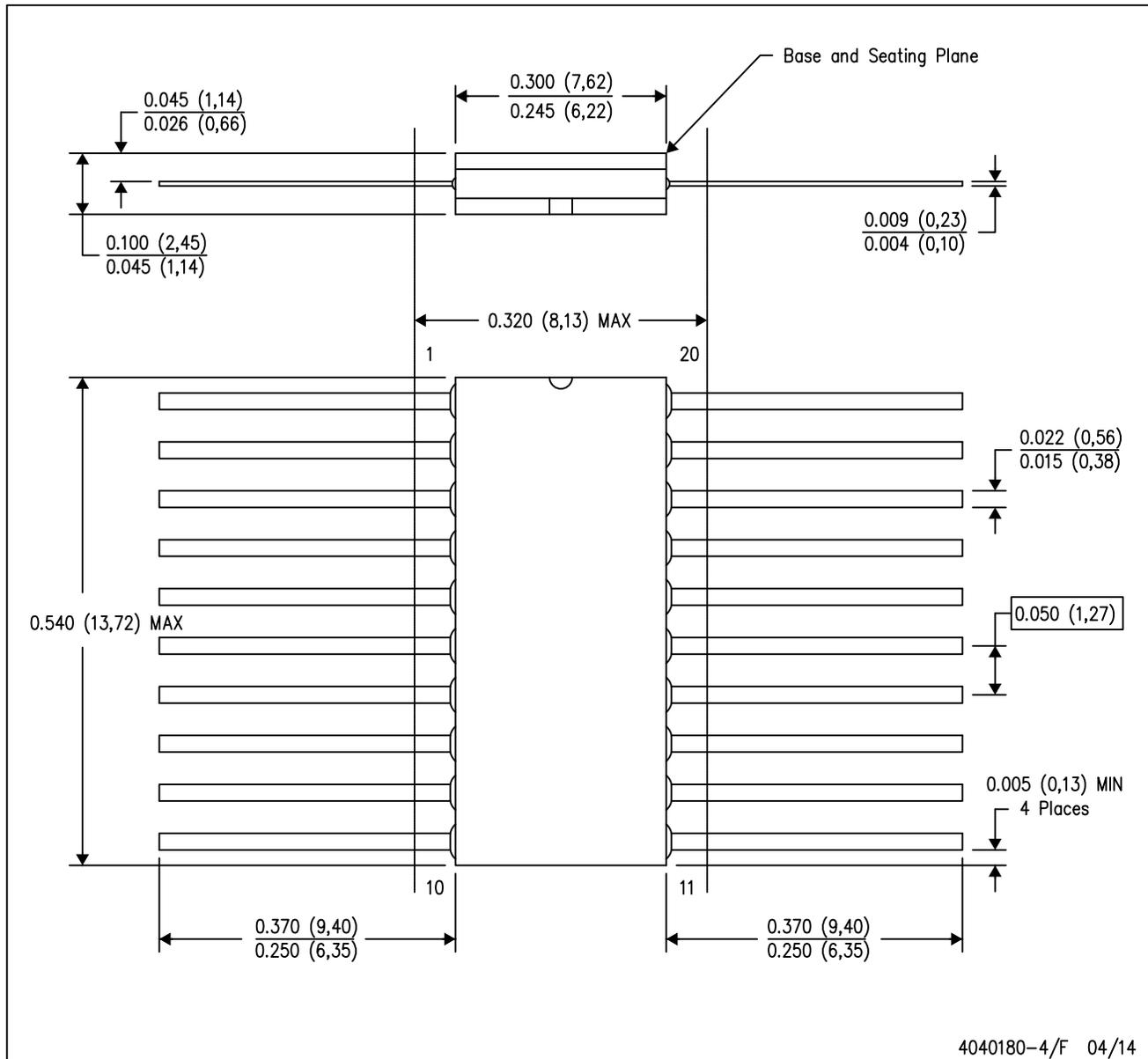
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
83021012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8302101SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ALS299DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS299DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS299N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS299N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS299FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS299FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS299W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS299W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

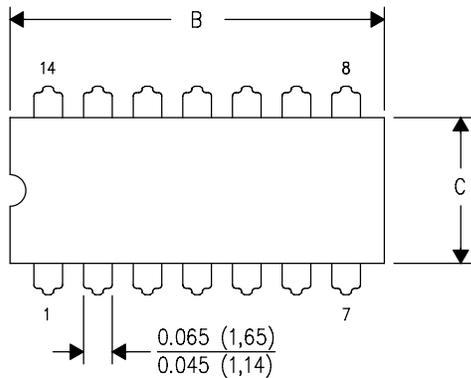


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

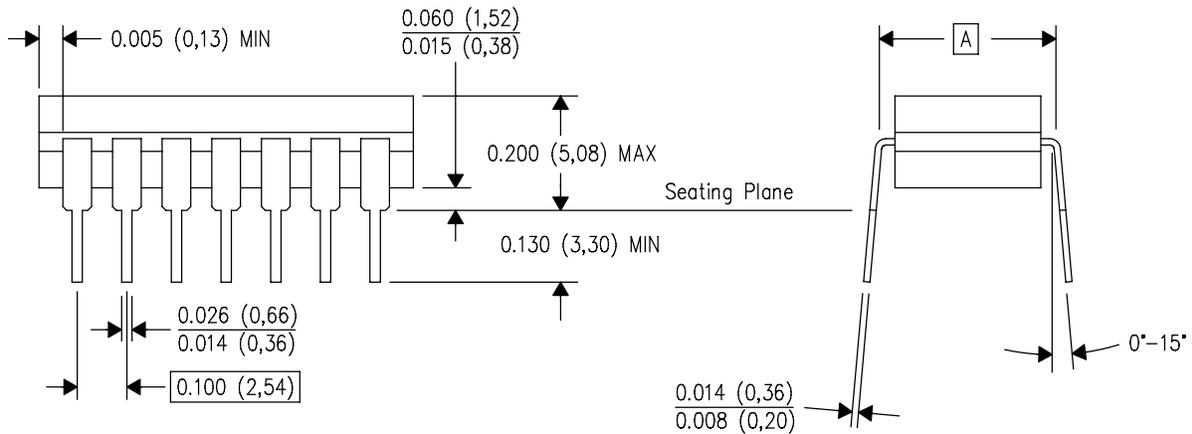
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

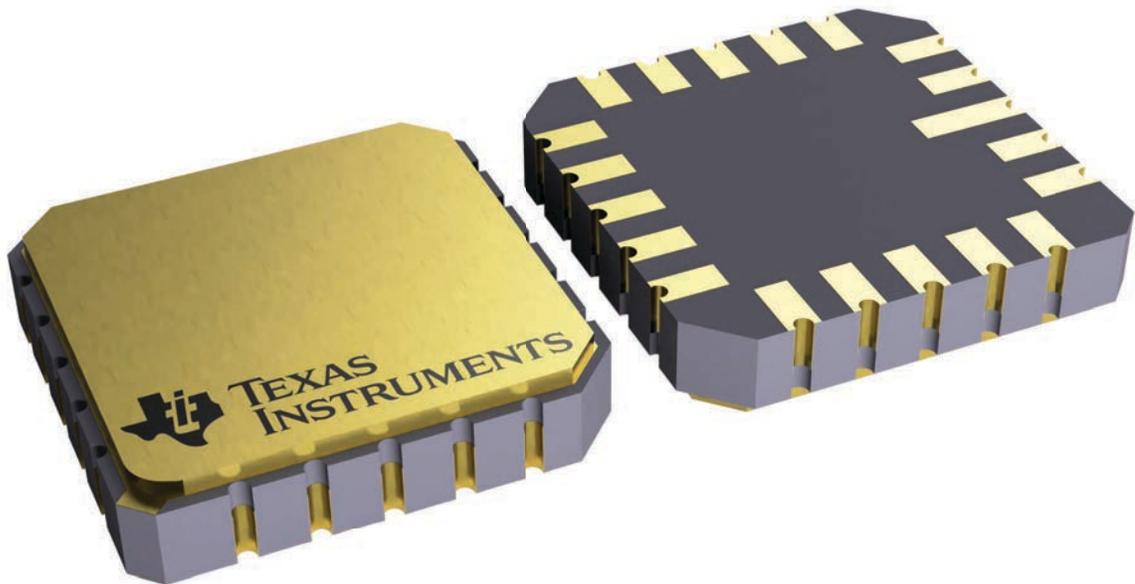
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

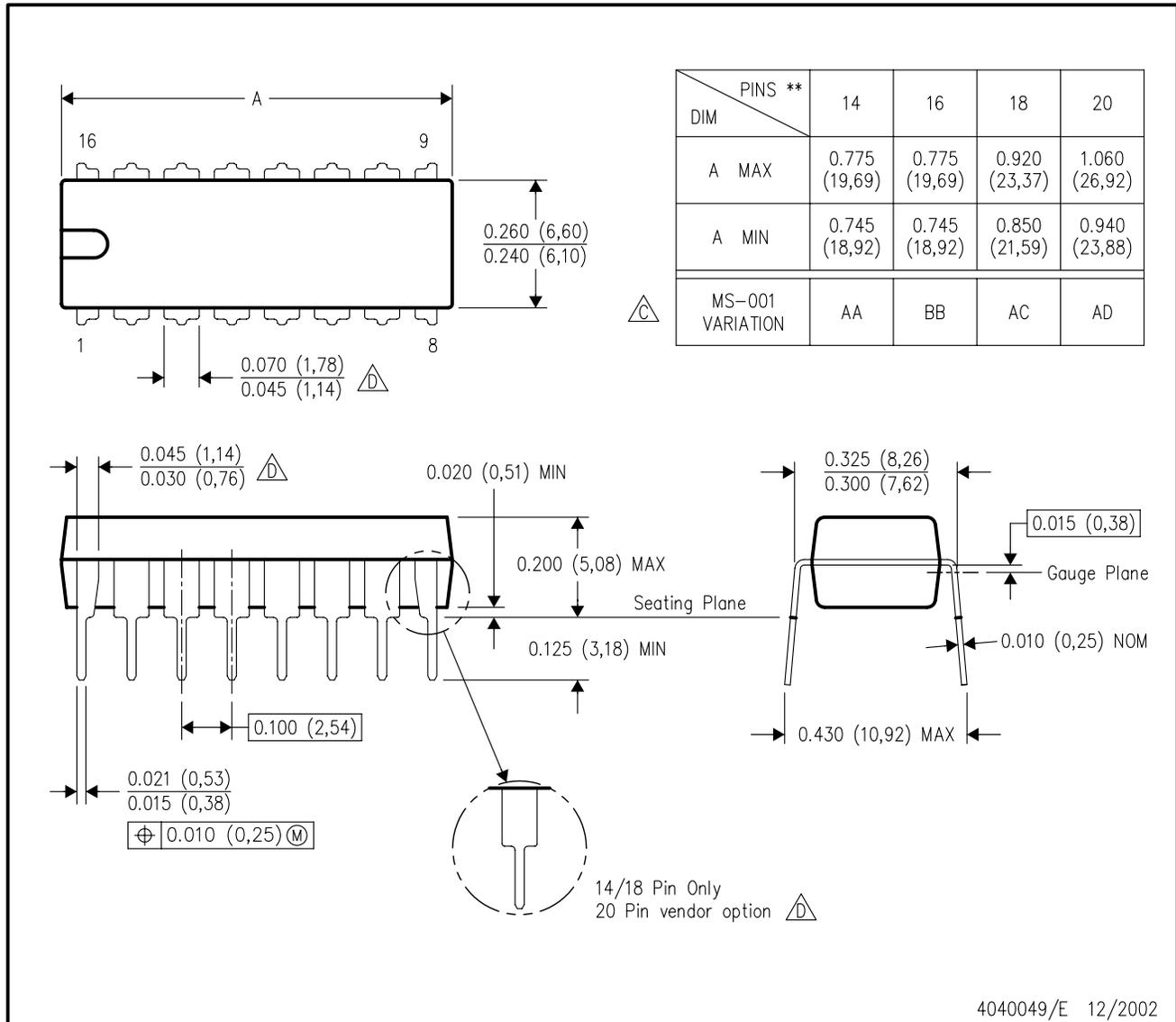


4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

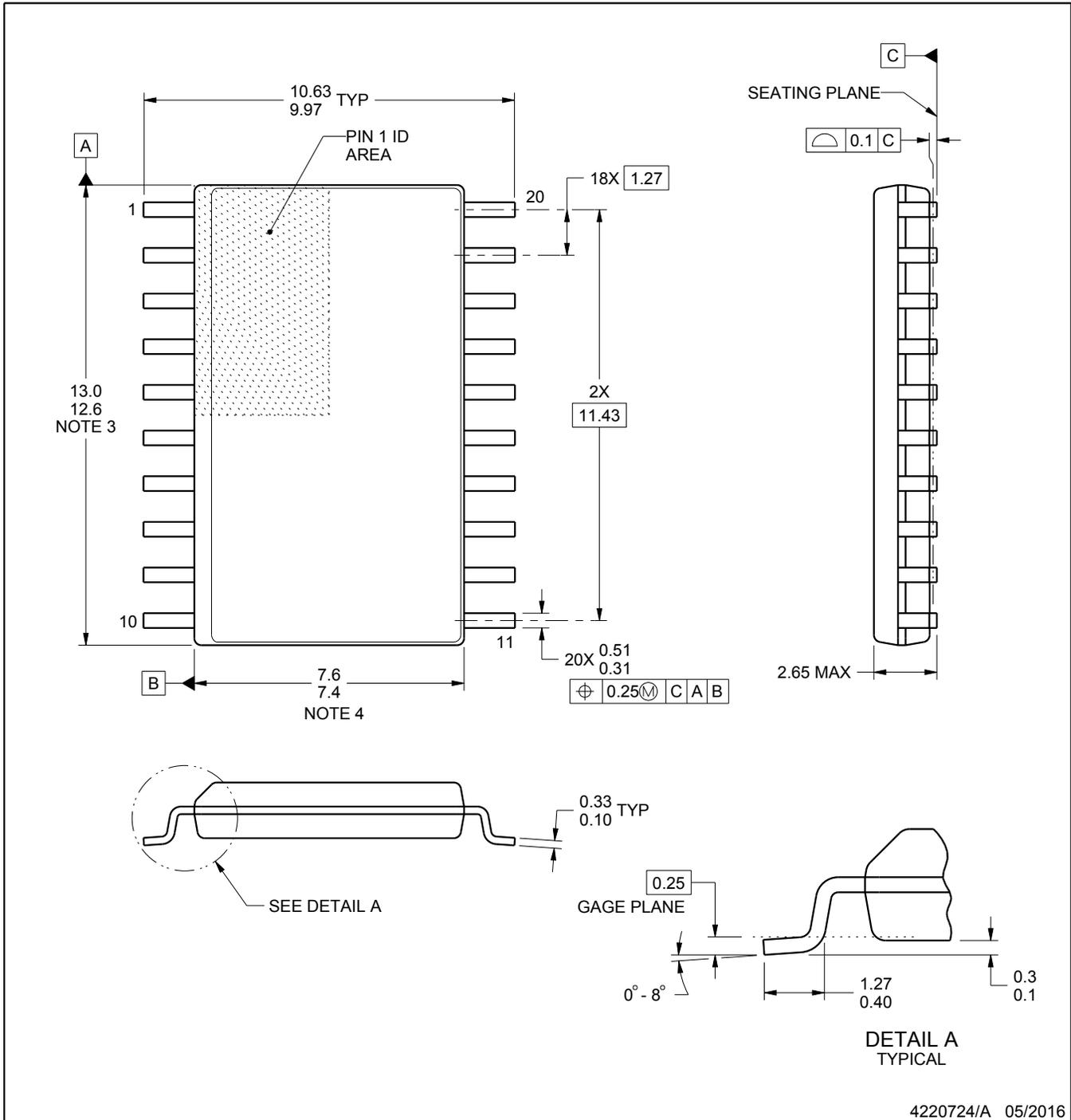
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



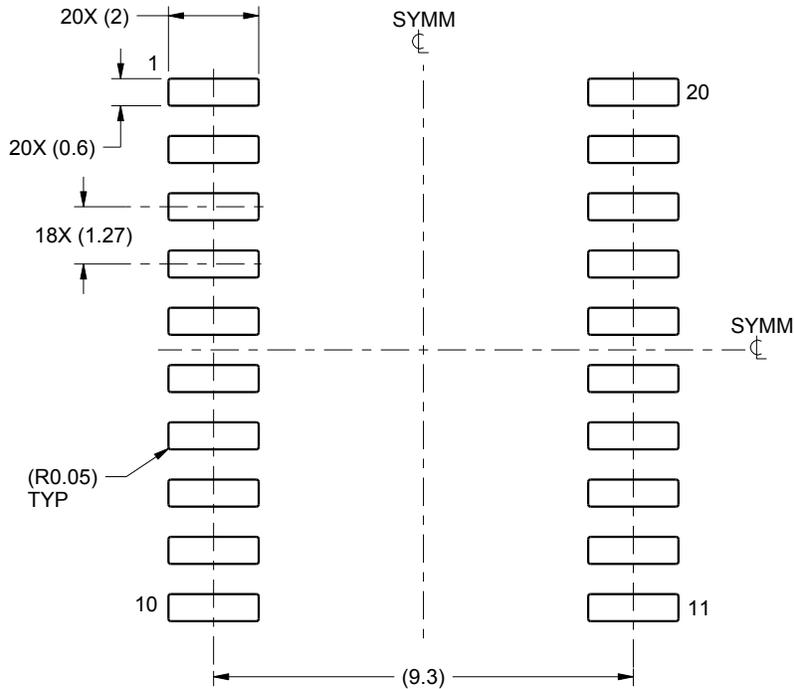
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# EXAMPLE BOARD LAYOUT

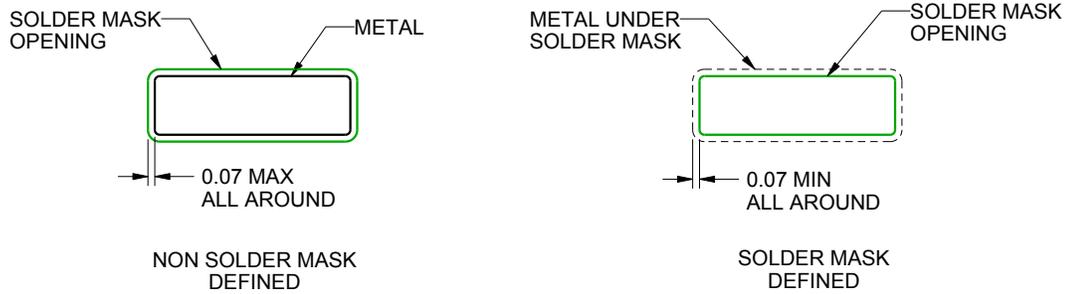
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

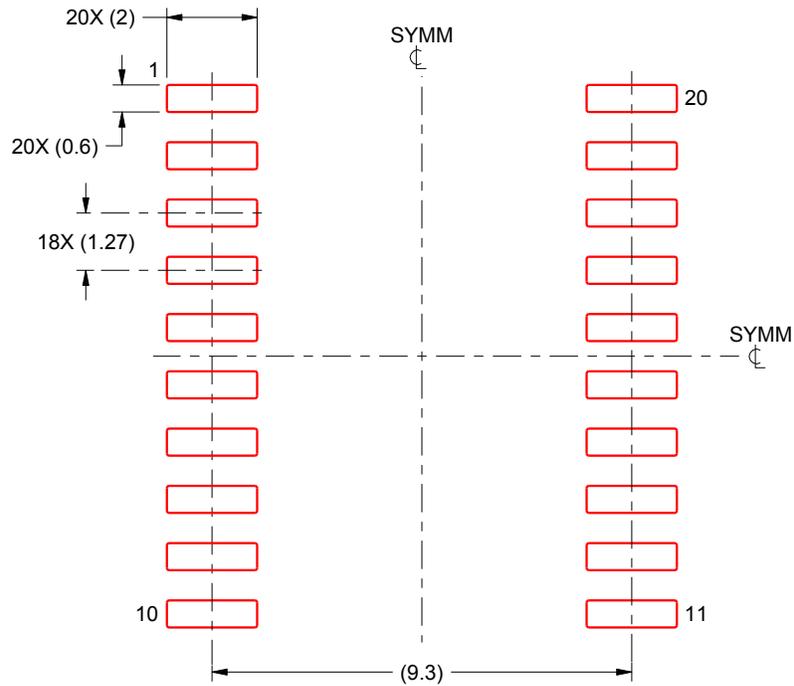
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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