

# SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C – APRIL 1982 – REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

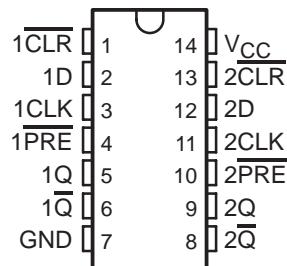
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY ( $C_L = 50 \text{ pF}$ ) (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS74A	50	6
'AS74A	134	26

## description

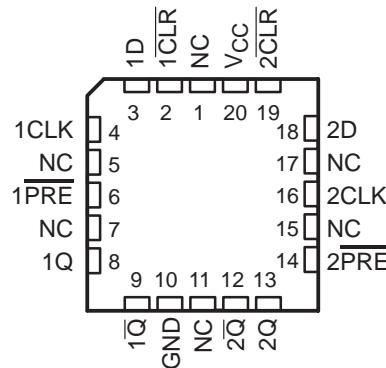
These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74A are characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ALS74A and SN74AS74A are characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

SN54ALS74A, SN54AS74A . . . J PACKAGE  
SN74ALS74A, SN74AS74A . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS74A, SN54AS74A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup>The output levels in this configuration are not specified to meet the minimum levels for  $V_{OH}$  if the lows at PRE and CLR are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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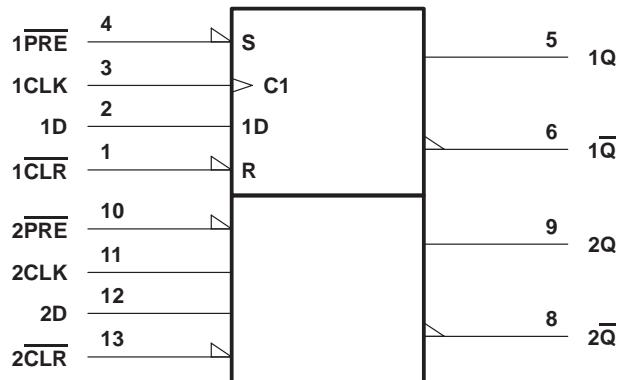
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# **SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET**

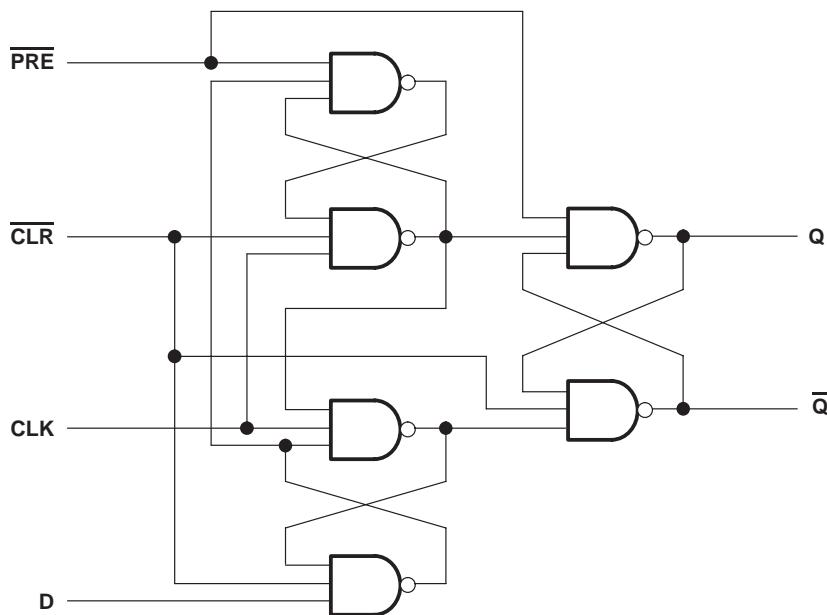
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

### logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A**  
**DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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**recommended operating conditions**

		SN54ALS74A			SN74ALS74A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current			4			8	mA
f <sub>clock</sub>	Clock frequency	0	25	0	0	25	34	MHz
t <sub>w</sub>	Pulse duration	PRE or CLR low		15	15			ns
		CLK high		17.5	14.5			
		CLK low		17.5	14.5			
t <sub>su</sub>	Setup time before CLK↑	Data		16	15			ns
		PRE or CLR inactive		10	10			
t <sub>h</sub>	Hold time after CLK↑	Data		2	0			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0	25	70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54ALS74A			SN74ALS74A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA	V <sub>CC</sub> -2			V <sub>CC</sub> -2			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4		V
		I <sub>OL</sub> = 8 mA			0.35	0.5		
I <sub>I</sub>	CLK or D PRE or CLR	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 7 V		0.1		0.1		mA
				0.2		0.2		
I <sub>IH</sub>	CLK or D PRE or CLR	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 2.7 V		20		20		μA
				40		40		
I <sub>IL</sub>	CLK or D PRE or CLR	V <sub>CC</sub> = 4.5 V, V <sub>I</sub> = 0.4 V		-0.2		-0.2		mA
				-0.4		-0.4		
I <sub>O</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-20	-112	-30	-112	-30	-112	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, See Note 1		2.4	4	2.4	4	2.4	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.  
 NOTE 1: I<sub>CC</sub> is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT	
			SN54ALS74A		SN74ALS74A			
			MIN	MAX	MIN	MAX		
f <sub>max</sub>			25	34			MHz	
t <sub>PLH</sub>	PRE or CLR	Q or $\overline{Q}$	3	18	3	13	ns	
t <sub>PHL</sub>			5	17	5	15		
t <sub>PLH</sub>	CLK	Q or $\overline{Q}$	5	23	5	16	ns	
t <sub>PHL</sub>			5	20	5	18		

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## **recommended operating conditions**

			SN54AS74A			SN74AS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			0.8	V
I <sub>OH</sub>	High-level output current				-2			-2	mA
I <sub>OL</sub>	Low-level output current				20			20	mA
f <sub>clock</sub> *	Clock frequency		0		90	0		105	MHz
t <sub>w</sub> *	Pulse duration	PRE or CLR low		4		4			ns
		CLK high		4		4			
		CLK low		5.5		5.5			
t <sub>su</sub> *	Setup time before CLK↑	Data		4.5		4.5			ns
		PRE or CLR inactive		2		2			
t <sub>h</sub> *	Hold time after CLK↑	Data		0		0			ns
T <sub>A</sub>	Operating free-air temperature		-55		125	0		70	°C

\* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested.

**SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A**  
**DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54AS74A			SN74AS74A			UNIT
		MIN	TYPT <sup>†</sup>	MAX	MIN	TYPT <sup>†</sup>	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA	V <sub>CC</sub> -2			V <sub>CC</sub> -2			V
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA		0.25	0.5		0.25	0.5	V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	CLK or D PRE or CLR	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20			20	μA
				40			40	
I <sub>IL</sub>	CLK or D PRE or CLR	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-0.5			-0.5	mA
				-1.8			-1.8	
I <sub>O</sub> <sup>‡</sup>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-30	-112	-30	-112		mA	
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, See Note 1	10.5	16	10.5	16		mA	

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.  
 NOTE 1: I<sub>CC</sub> is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX <sup>§</sup>				UNIT	
			SN54AS74A		SN74AS74A			
			MIN	MAX	MIN	MAX		
f <sub>max</sub> <sup>*</sup>			90		105		MHz	
t <sub>PLH</sub>	PRE or CLR	Q or $\bar{Q}$	2	9	2	7.5	ns	
			2.5	11.5	2.5	10.5		
t <sub>PHL</sub>	CLK	Q or $\bar{Q}$	2.5	10	3	8	ns	
			3.5	10.5	3	9		

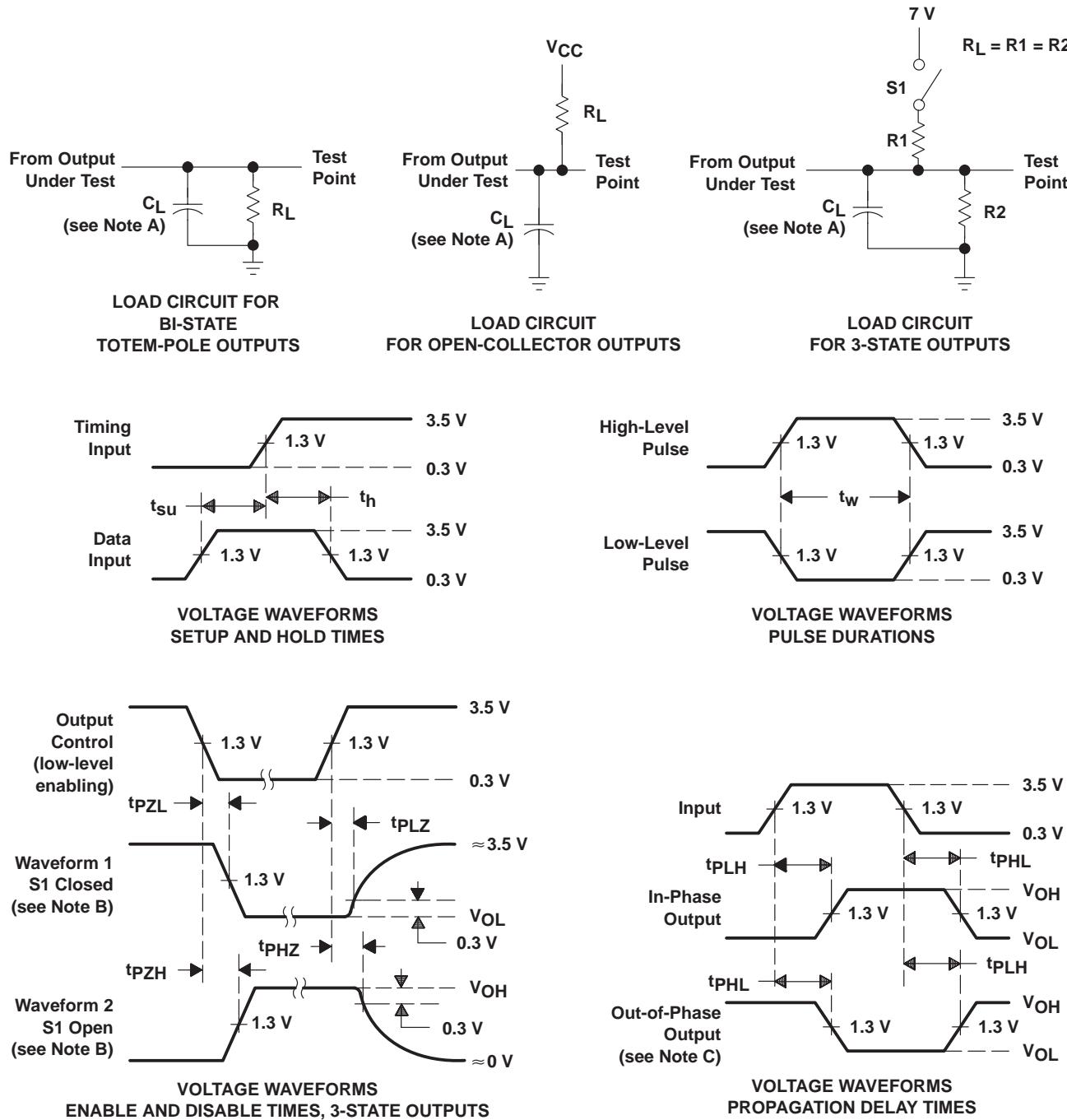
<sup>\*</sup> On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested.

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A  
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS  
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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9862701QCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9862701QC A SNJ54AS74AJ
84011012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84011012A SNJ54ALS 74AFK
8401101CA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401101CA SNJ54ALS74AJ
8401101DA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401101DA SNJ54ALS74AW
JM38510/37101B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37101B2A
JM38510/37101B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37101B2A
JM38510/37101BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37101BCA
JM38510/37101BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37101BCA
M38510/37101B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37101B2A
M38510/37101BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37101BCA
SN54ALS74AJ	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS74AJ
SN54ALS74AJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS74AJ
SN54AS74AJ	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS74AJ
SN54AS74AJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS74AJ
SN74ALS74AD	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	ALS74A
SN74ALS74ADR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A
SN74ALS74ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A
SN74ALS74AN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS74AN
SN74ALS74AN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS74AN
SN74ALS74ANSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS74ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS74A
<a href="#">SN74AS74AD</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	AS74A
<a href="#">SN74AS74ADR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS74A
SN74AS74ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS74A
<a href="#">SN74AS74AN</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS74AN
SN74AS74AN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS74AN
<a href="#">SN74AS74ANSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS74A
SN74AS74ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS74A
<a href="#">SNJ54ALS74AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84011012A SNJ54ALS 74AFK
SNJ54ALS74AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84011012A SNJ54ALS 74AFK
<a href="#">SNJ54ALS74AJ</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401101CA SNJ54ALS74AJ
SNJ54ALS74AJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401101CA SNJ54ALS74AJ
<a href="#">SNJ54ALS74AW</a>	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401101DA SNJ54ALS74AW
SNJ54ALS74AW.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8401101DA SNJ54ALS74AW
<a href="#">SNJ54AS74AJ</a>	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9862701QC A SNJ54AS74AJ
SNJ54AS74AJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9862701QC A SNJ54AS74AJ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

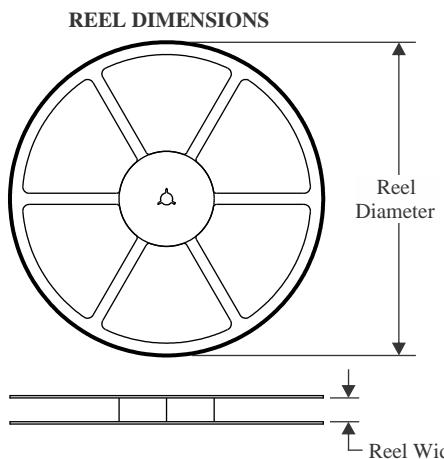
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A :**

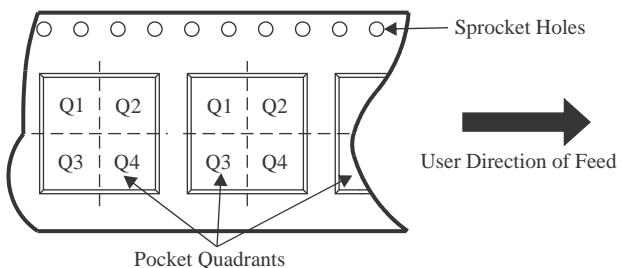
- Catalog : [SN74ALS74A](#), [SN74AS74A](#)
- Military : [SN54ALS74A](#), [SN54AS74A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


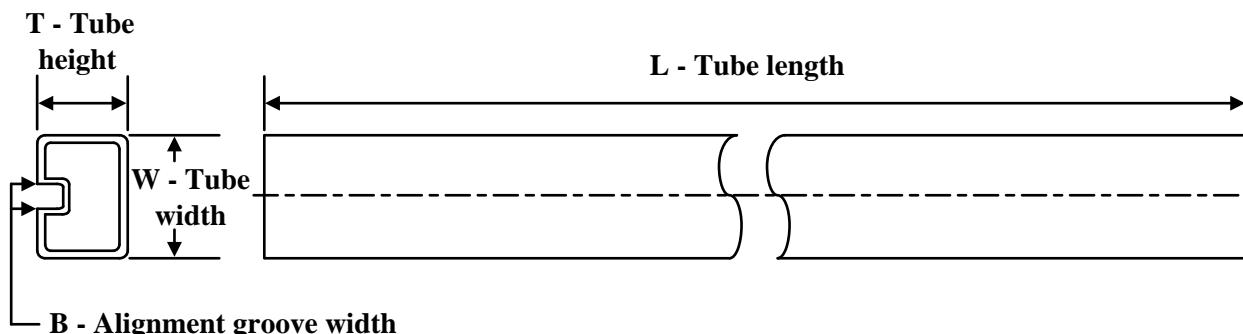
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALS74ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AS74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AS74ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS74ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74ALS74ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74AS74ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AS74ANSR	SOP	NS	14	2000	353.0	353.0	32.0

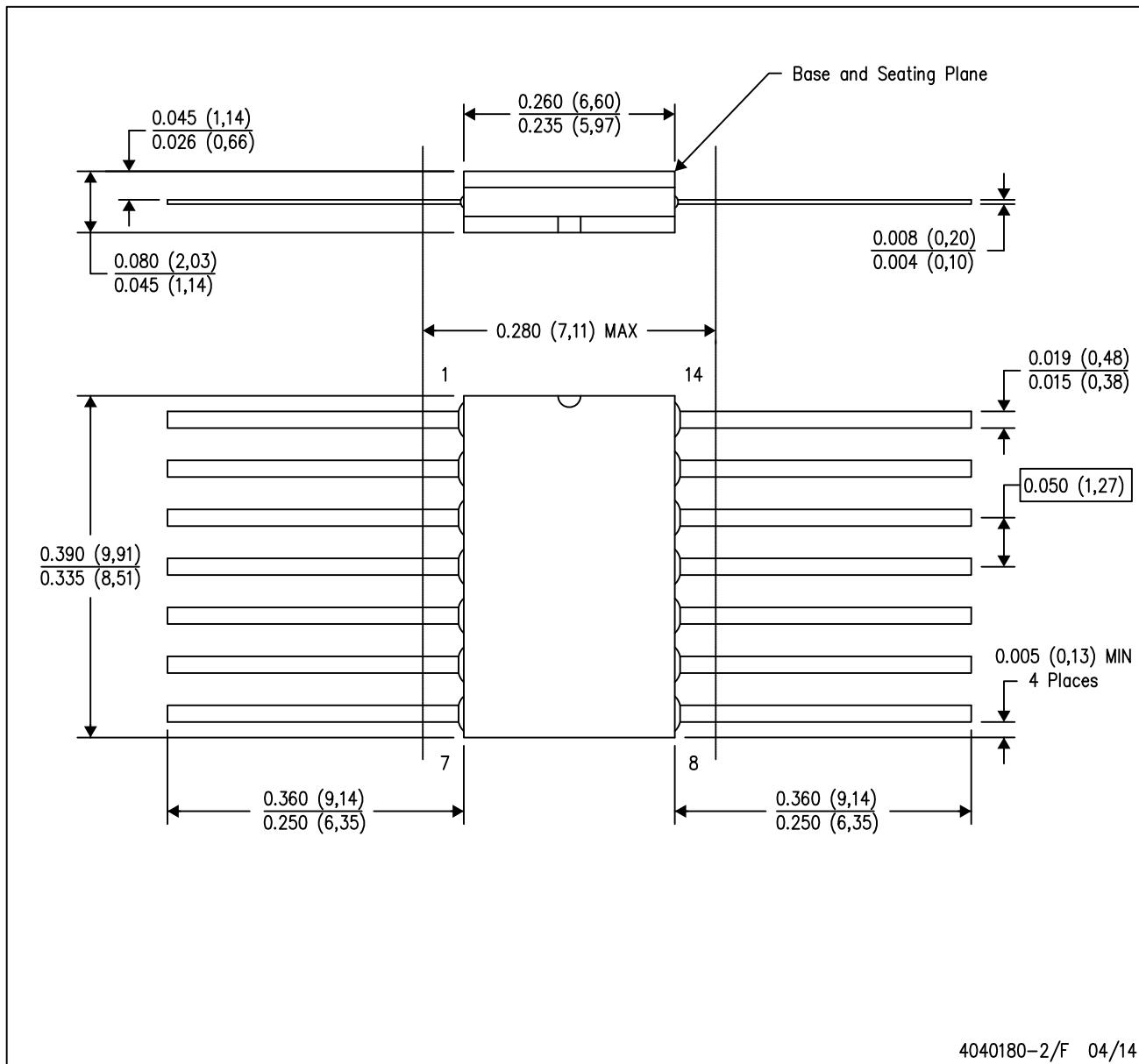
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84011012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8401101DA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/37101B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/37101B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/37101B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS74AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS74AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS74AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS74AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS74AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ALS74AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS74AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS74AW	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54ALS74AW.A	W	CFP	14	25	506.98	26.16	6220	NA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

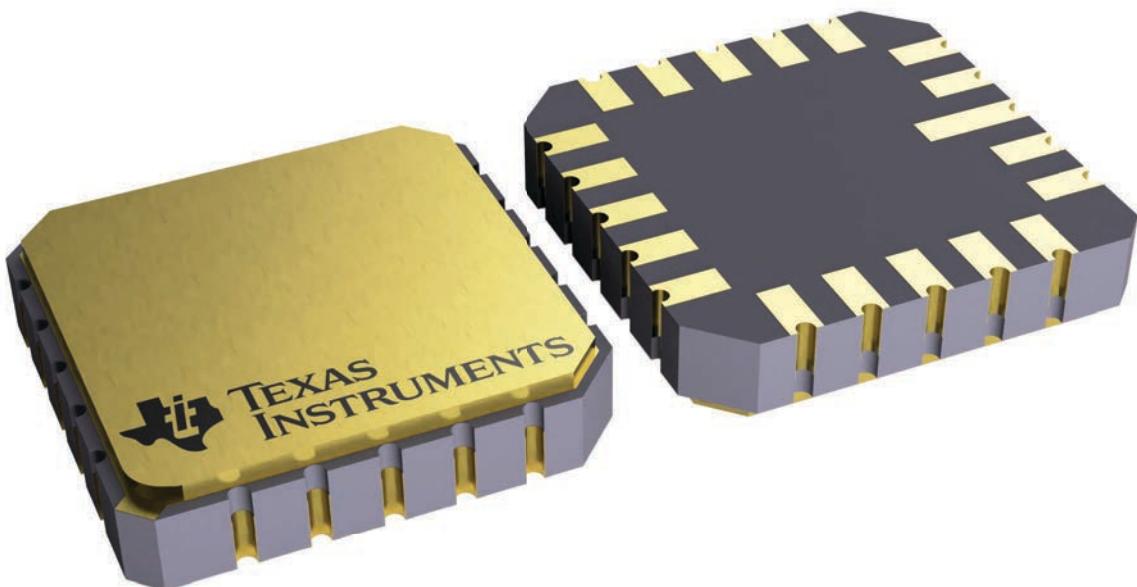
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



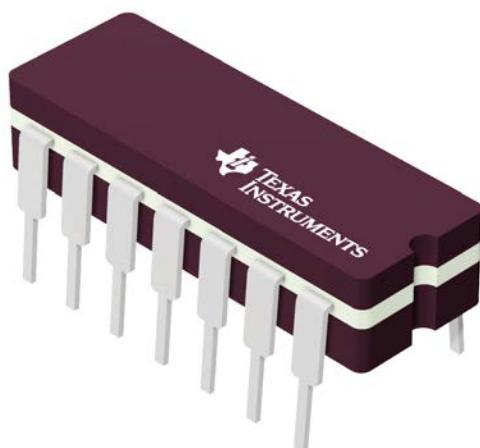
4229370VA\

# GENERIC PACKAGE VIEW

**J 14**

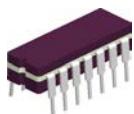
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

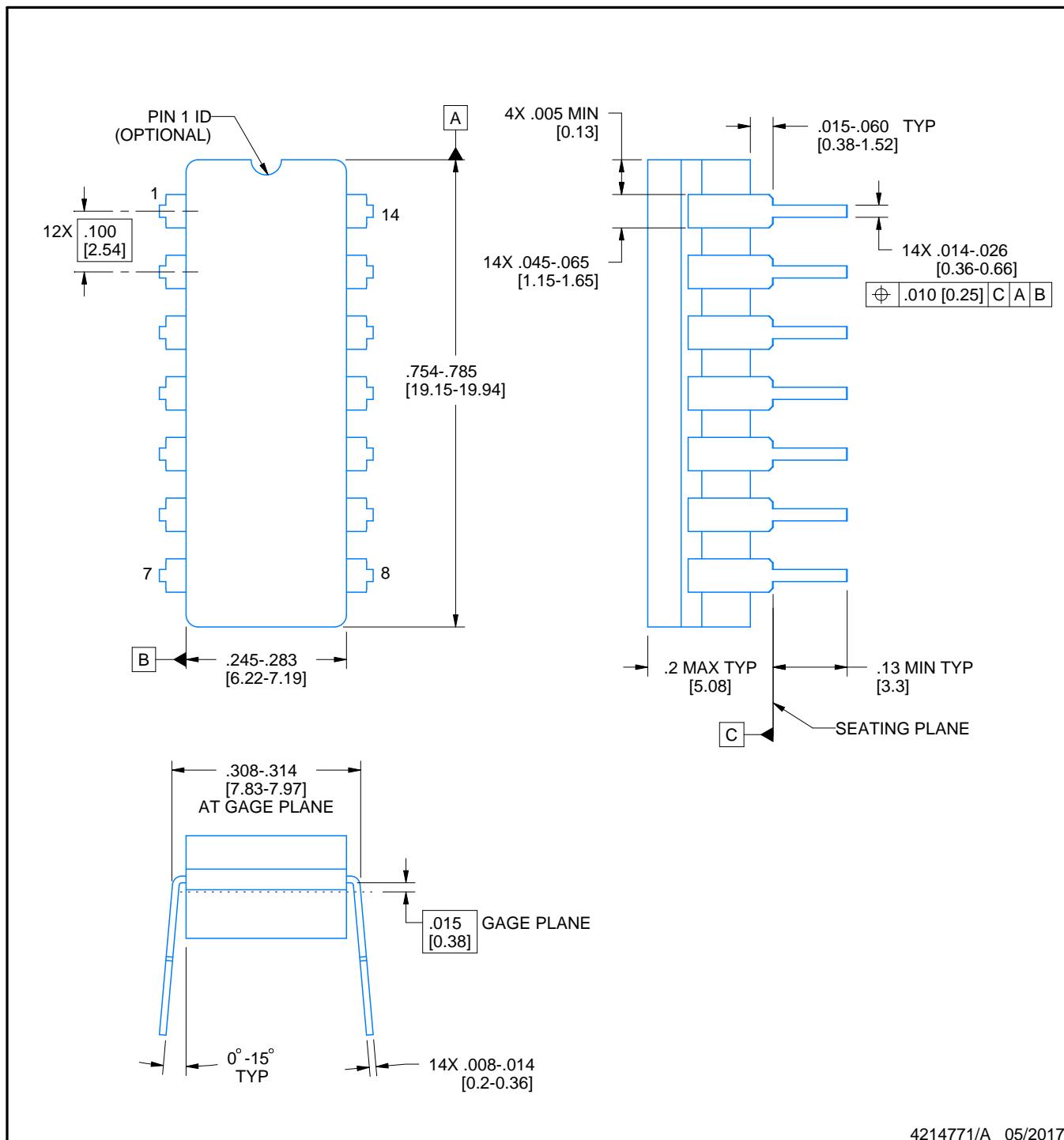


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

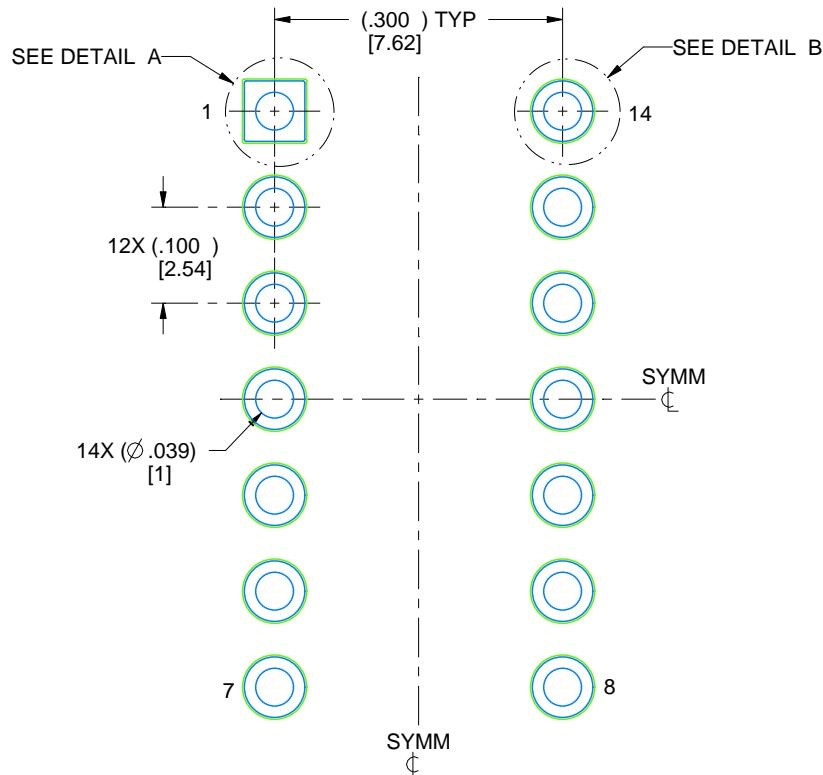
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

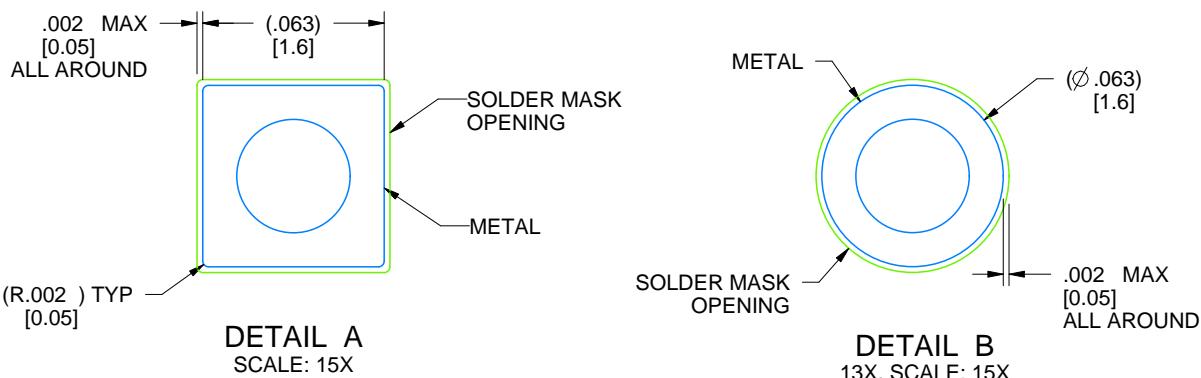
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

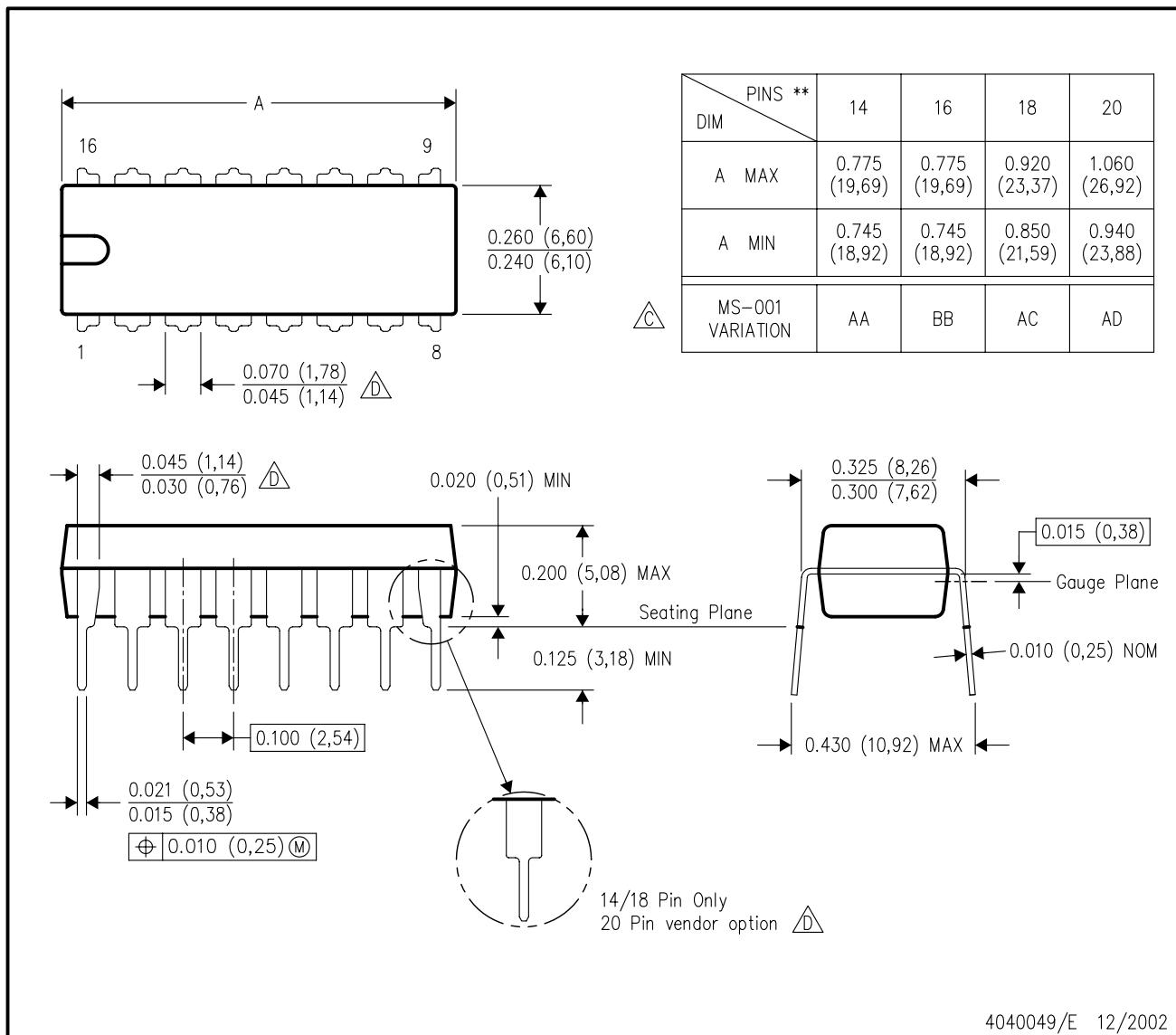


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE

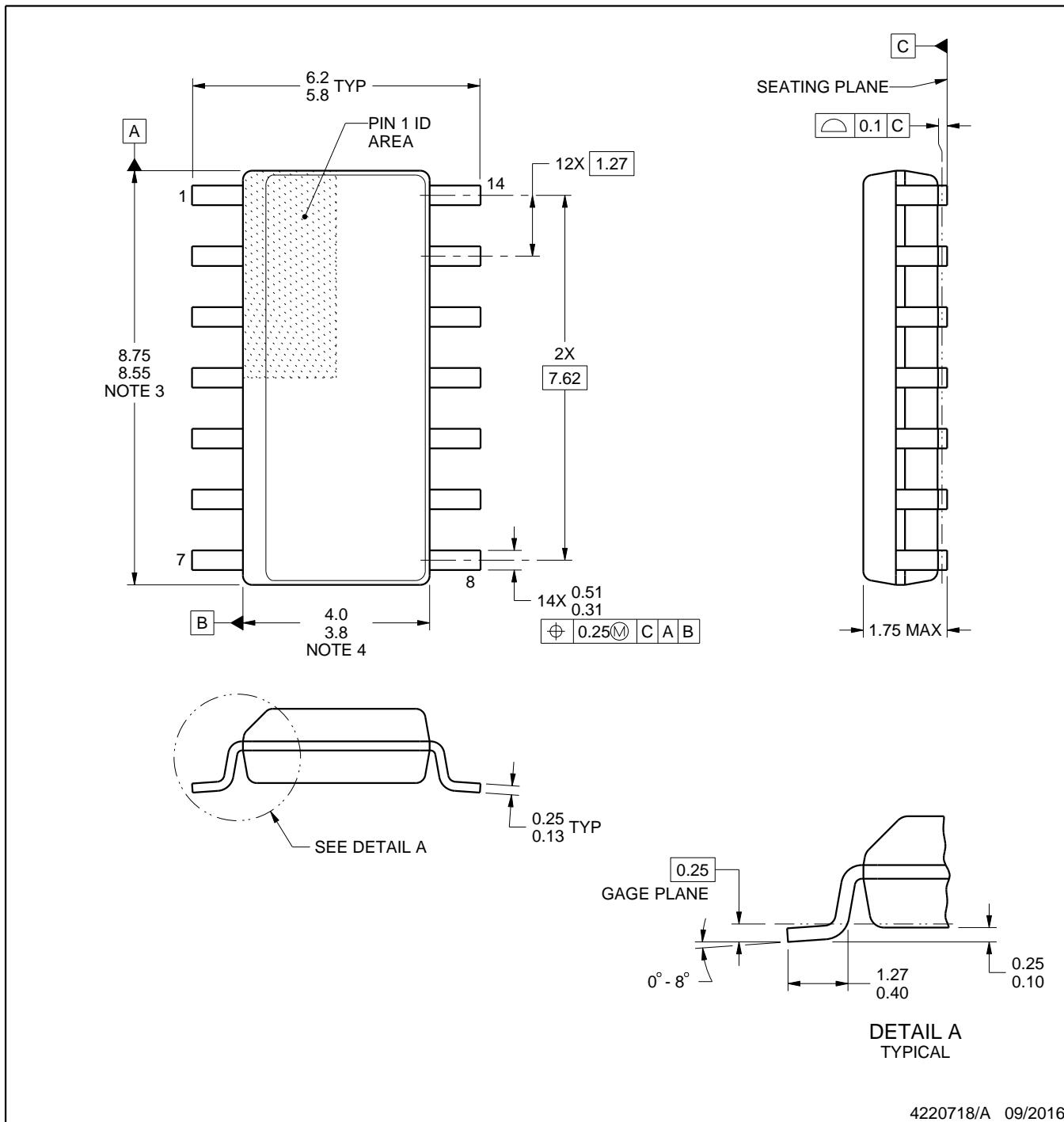


# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

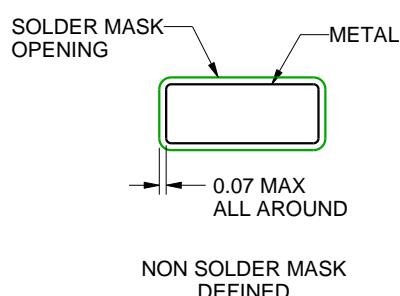
D0014A

SOIC - 1.75 mm max height

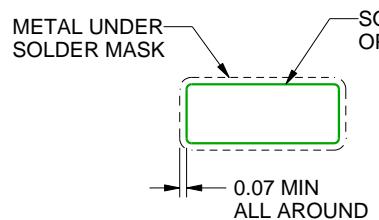
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

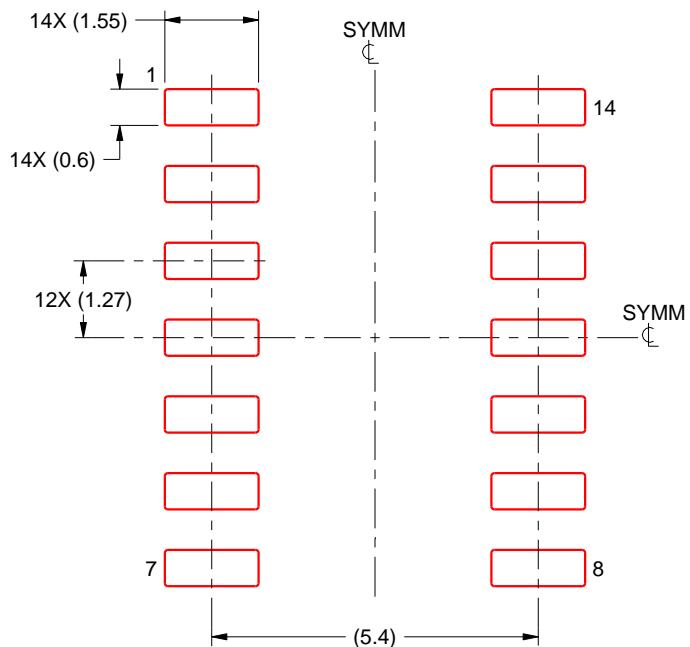
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**D0014A**

## **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



**SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X**

4220718/A 09/2016

#### NOTES: (continued)

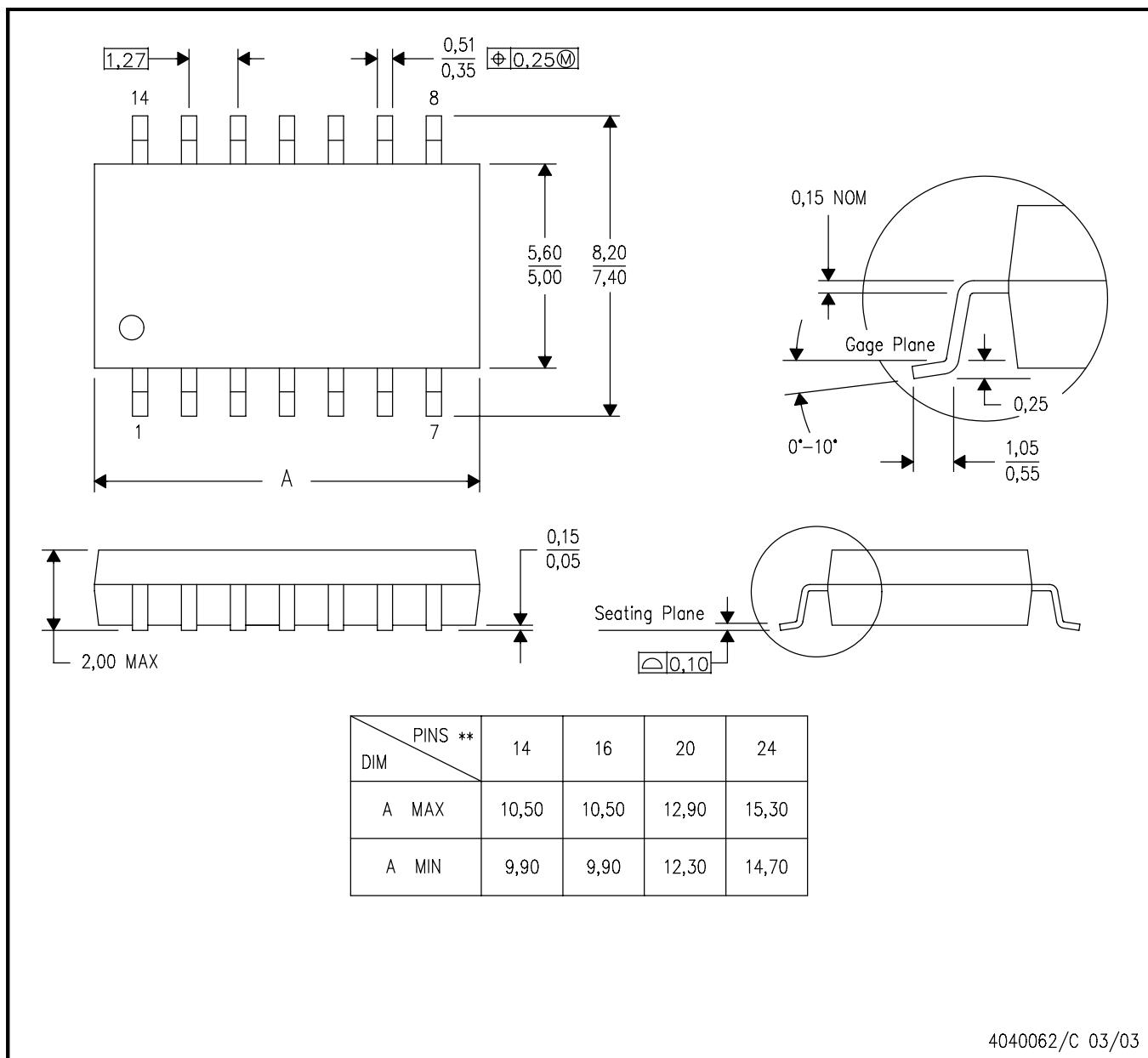
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

4040062/C 03/03

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