

SN54HC623, SN74HC623 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCLS149C – DECEMBER 1982 – REVISED DECEMBER 2002

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 8$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Lock Bus-Latch Capability
- True Logic

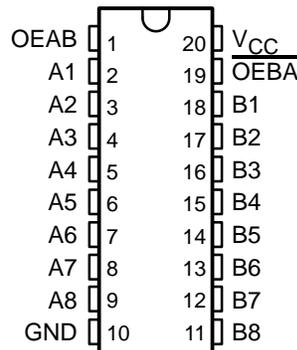
description/ordering information

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

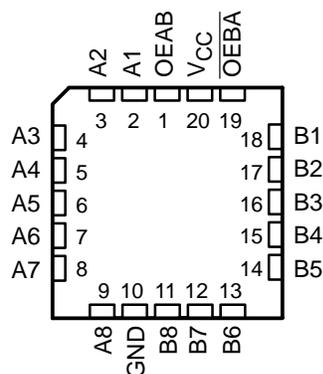
The 'HC623 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and \overline{OEBA}) inputs.

OEAB and \overline{OEBA} disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability to store data by simultaneously enabling OEAB and \overline{OEBA} . Each output reinforces its input in this transceiver configuration. When both OEAB and \overline{OEBA} are enabled and all other data sources to the two sets of bus lines are in the high-impedance state, both sets of bus lines (16 total) remain at their last states. The 8-bit codes appearing on the two sets of buses are identical.

SN54HC623 . . . J OR W PACKAGE
SN74HC623 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54HC623 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HC623N	SN74HC623N
	SOIC – DW	Tube	SN74HC623DW	HC623
		Tape and reel	SN74HC623DWR	
	SOP – NS	Tape and reel	SN74HC623NSR	HC623
-55°C to 125°C	CDIP – J	Tube	SNJ54HC623J	SNJ54HC623J
	CFP – W	Tube	SNJ54HC623W	SNJ54HC623W
	LCCC – FK	Tube	SNJ54HC623FK	SNJ54HC623FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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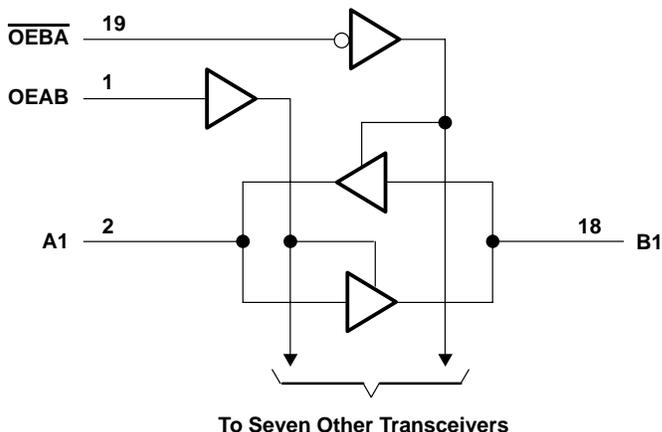
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FUNCTION TABLE

INPUTS		OPERATION
\overline{OEBA}	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		SN54HC623			SN74HC623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5		V	
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 6 V			1.8			
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V			1000		ns	
		V _{CC} = 4.5 V			500			
		V _{CC} = 6 V			400			
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC623		SN74HC623		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9	1.9	V		
			4.5 V	4.4	4.499	4.4	4.4			
			6 V	5.9	5.999	5.9	5.9			
		I _{OH} = -6 mA	4.5 V	3.98	4.3	3.7	3.84			
			6 V	5.48	5.8	5.2	5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.002	0.1	0.1	0.1	V		
			4.5 V	0.001	0.1	0.1	0.1			
			6 V	0.001	0.1	0.1	0.1			
		I _{OL} = 6 mA	4.5 V	0.17	0.26	0.4	0.33			
			6 V	0.15	0.26	0.4	0.33			
I _I	OEAB or OEBA	V _I = V _{CC} or 0	6 V	±0.1	±100	±1000	±1000	nA		
I _{OZ}	A or B	V _O = V _{CC} or 0	6 V	±0.01	±0.5	±10	±5	μA		
I _{CC}		V _I = V _{CC} or 0, I _O = 0	6 V		8	160	80	μA		
C _i	OEAB or OEBA		2 V to 6 V	3	10	10	10	pF		

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC623		SN74HC623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	2 V		29	105		160		130	ns
			4.5 V		10	21		32		26	
			6 V		8	18		27		22	
t _{en}	\overline{OEBA}	A	2 V		112	210		315		265	ns
			4.5 V		27	42		63		53	
			6 V		20	36		54		45	
t _{dis}	\overline{OEBA}	A	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t _{en}	OEAB	B	2 V		112	210		315		265	ns
			4.5 V		27	42		63		53	
			6 V		20	36		54		45	
t _{dis}	OEAB	B	2 V		40	150		225		190	ns
			4.5 V		18	30		45		38	
			6 V		16	26		38		32	
t _t		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

switching characteristics over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC623		SN74HC623		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	2 V		44	135		200		170	ns
			4.5 V		14	27		40		34	
			6 V		11	23		34		29	
t _{en}	\overline{OEBA}	A	2 V		130	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		23	46		69		56	
	OEAB	B	2 V		130	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		23	46		69		56	
t _t		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

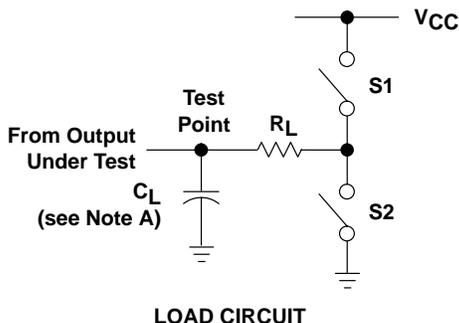
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per transceiver	No load	40	pF

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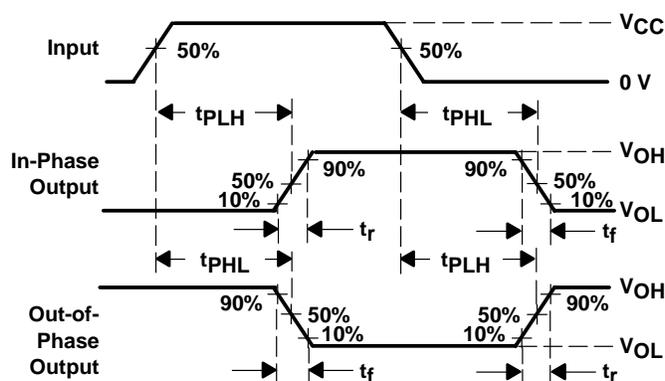
PARAMETER MEASUREMENT INFORMATION



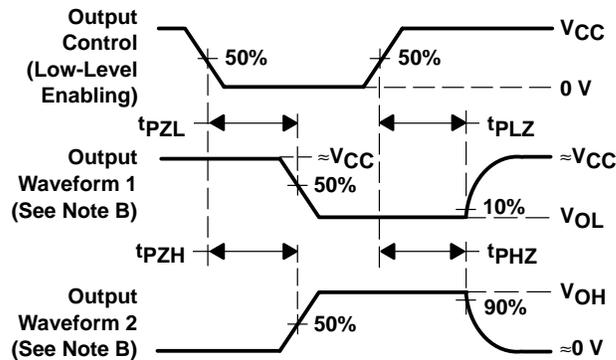
PARAMETER	R_L	C_L	S1	S2
t_{en}	1 k Ω	50 pF or 150 pF	Open	Closed
			Closed	Open
t_{dis}	1 k Ω	50 pF	Open	Closed
			Closed	Open
t_{pd} or t_t	—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC623DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623
SN74HC623DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623
SN74HC623N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC623N
SN74HC623N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC623N
SN74HC623NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623
SN74HC623NSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC623

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

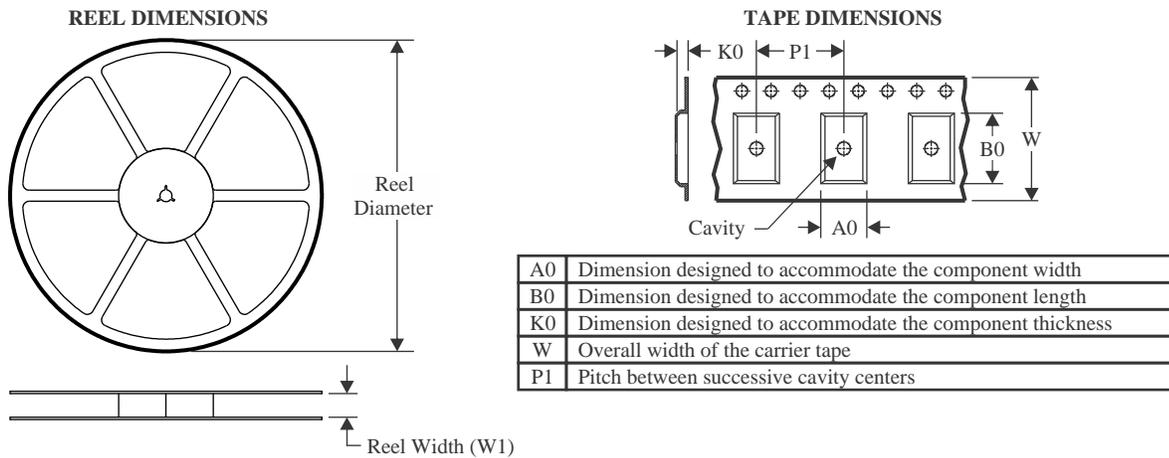
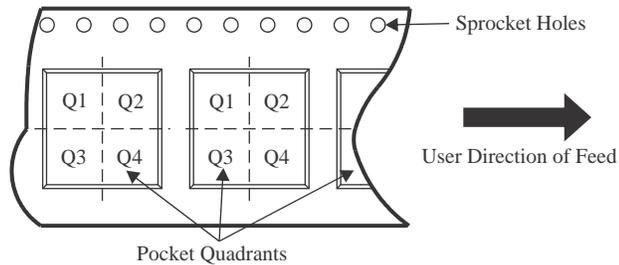
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

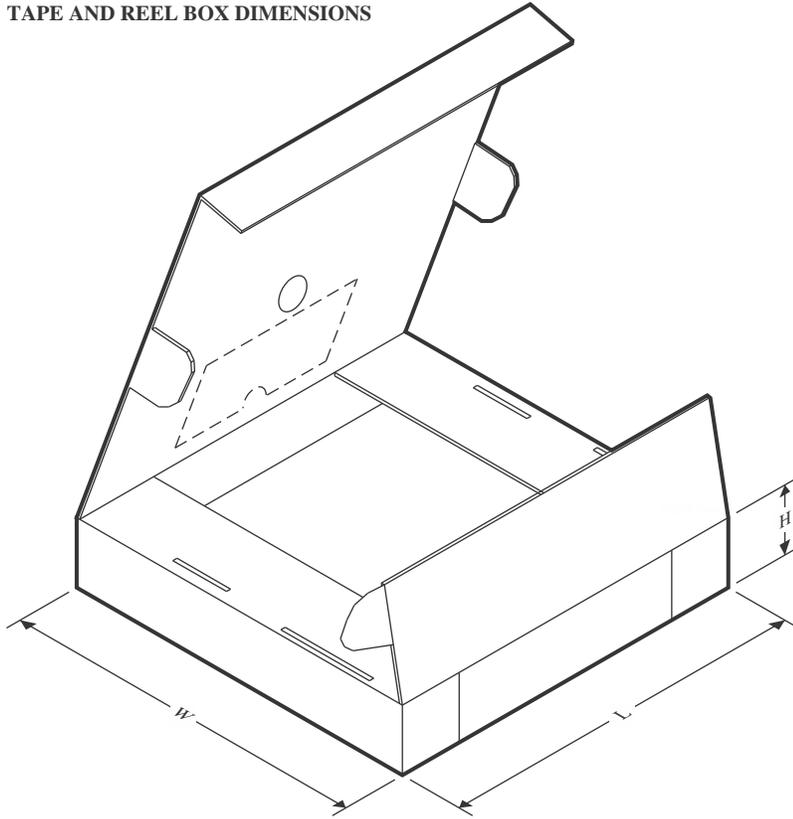
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


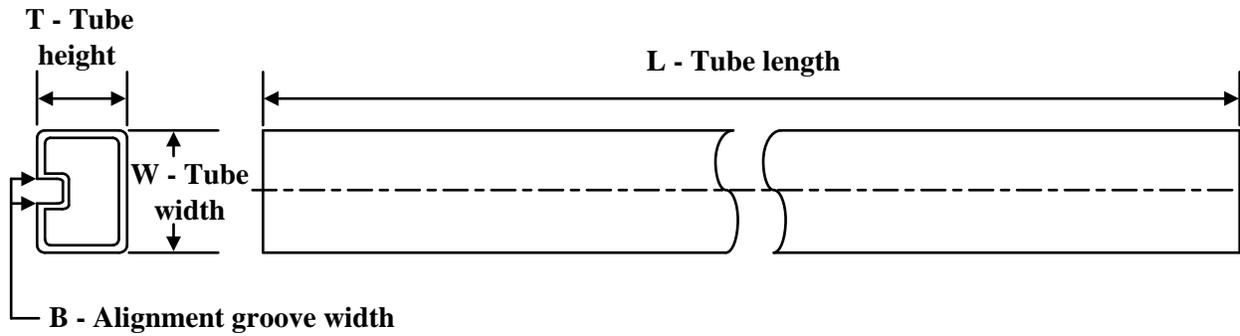
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC623NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC623NSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE


*All dimensions are nominal

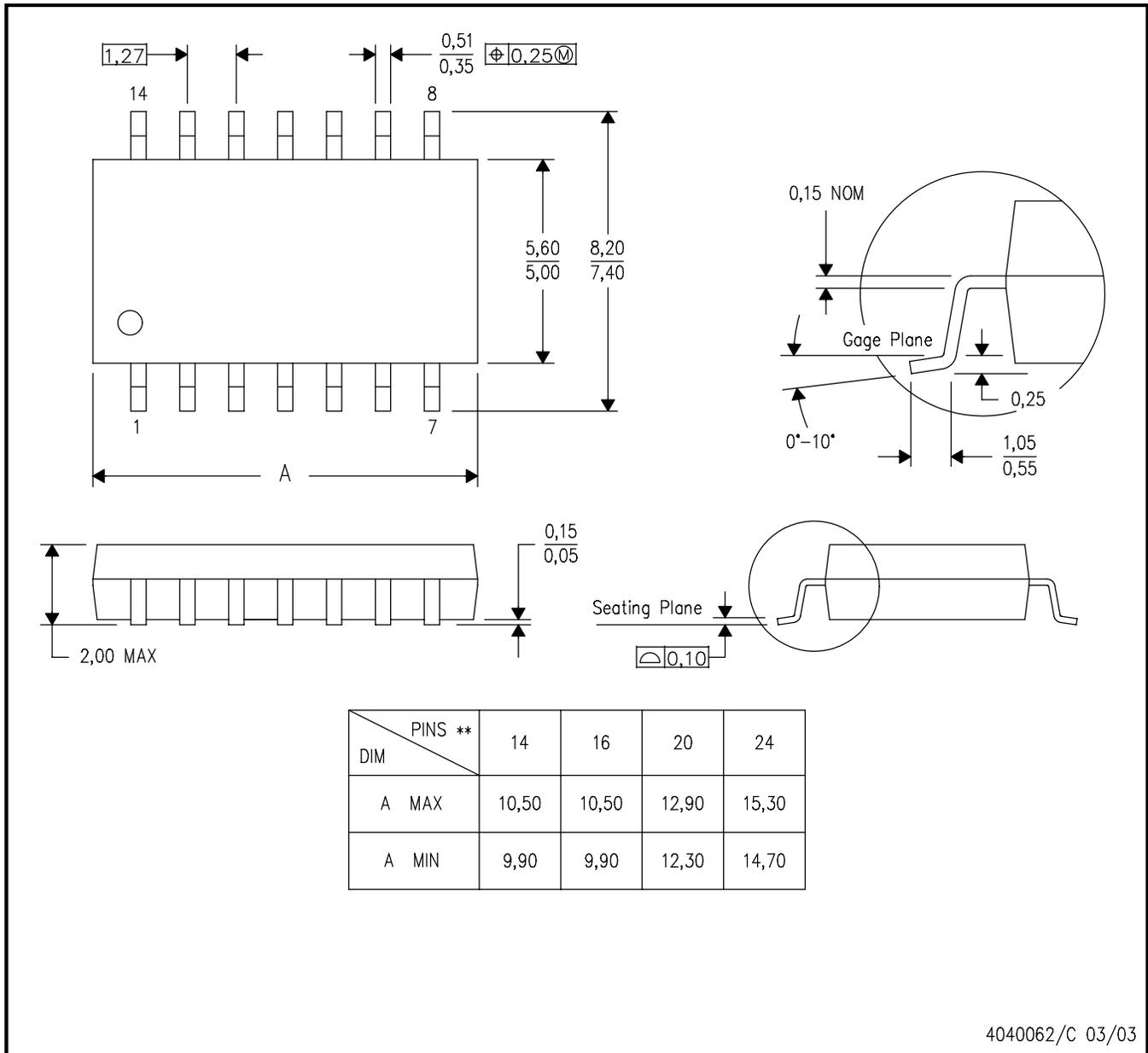
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HC623DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC623DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC623N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC623N.A	N	PDIP	20	20	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

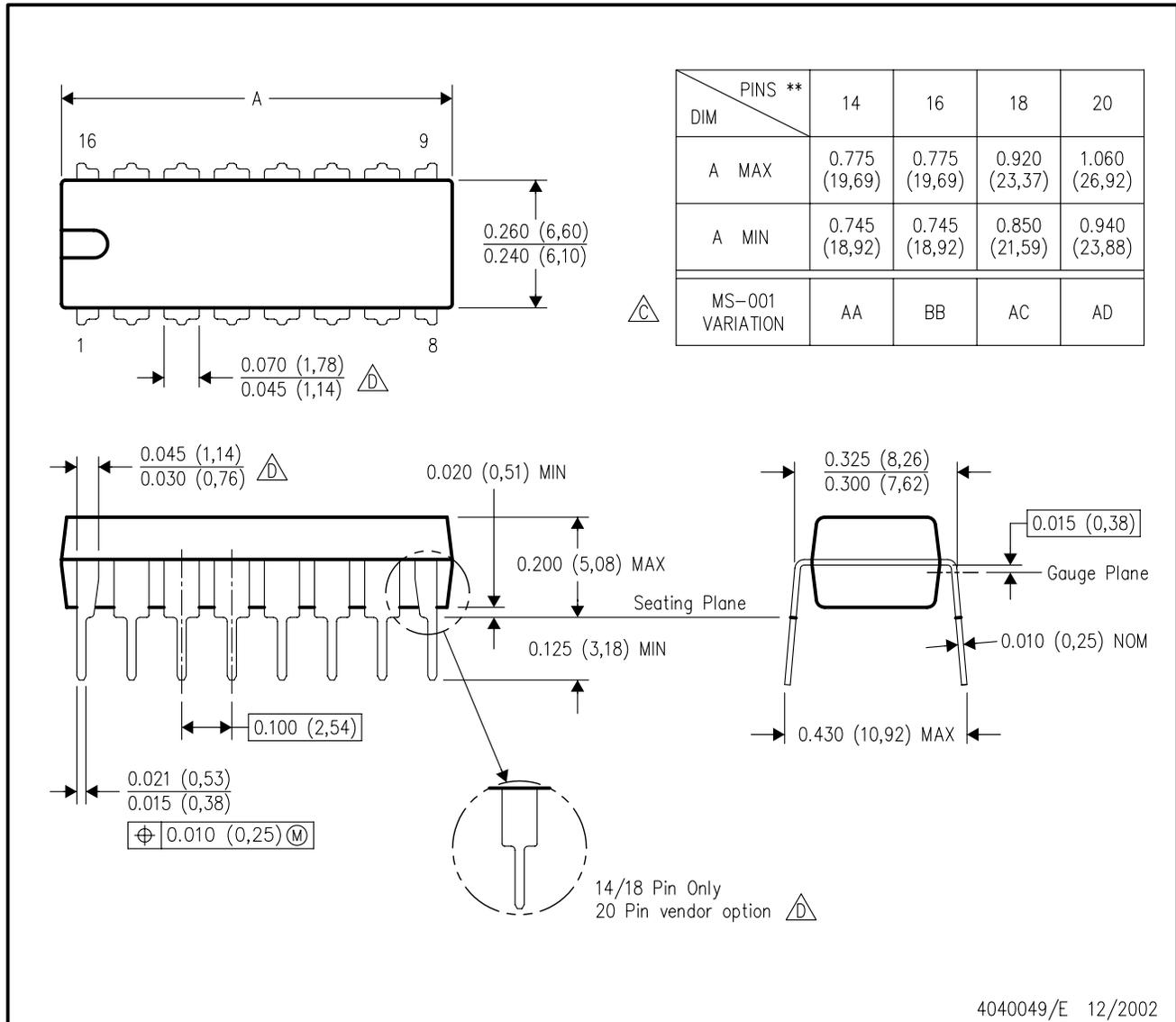


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

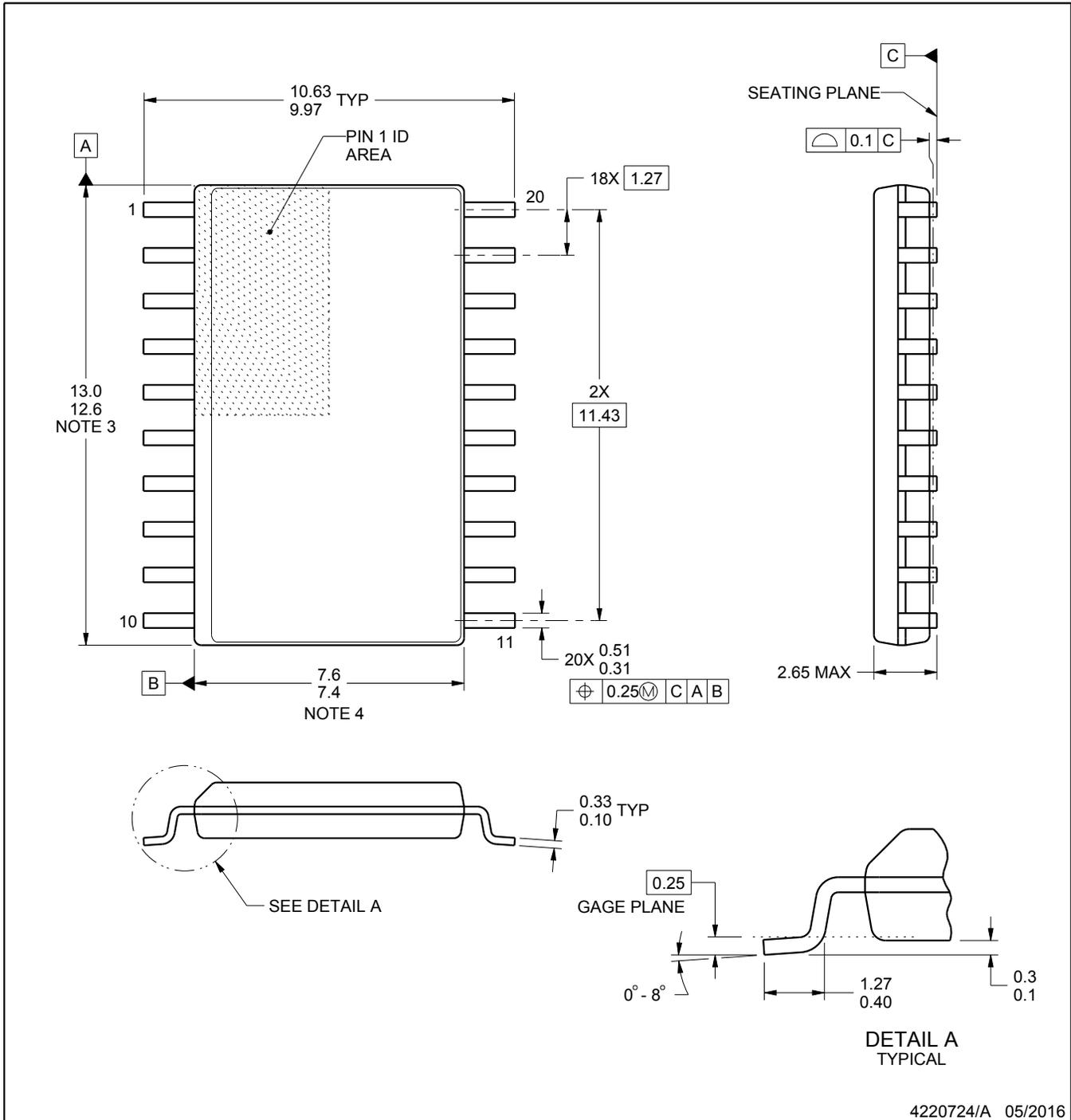
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

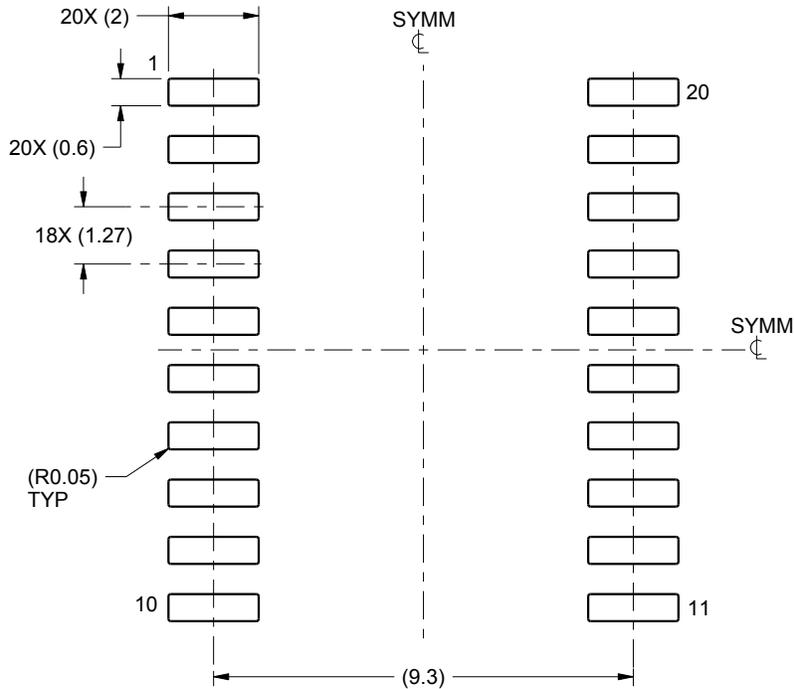
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

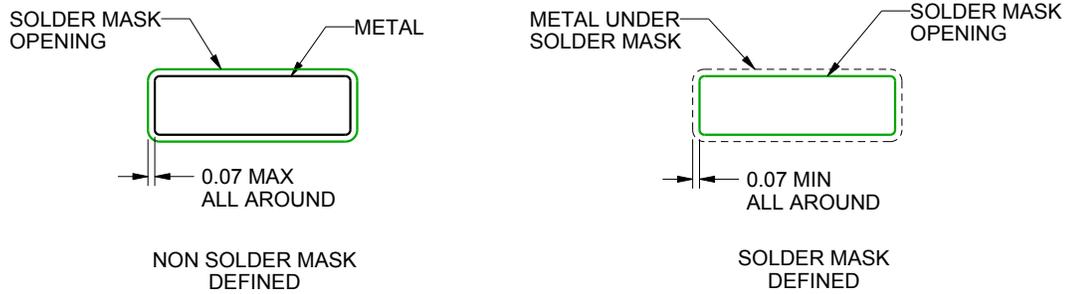
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

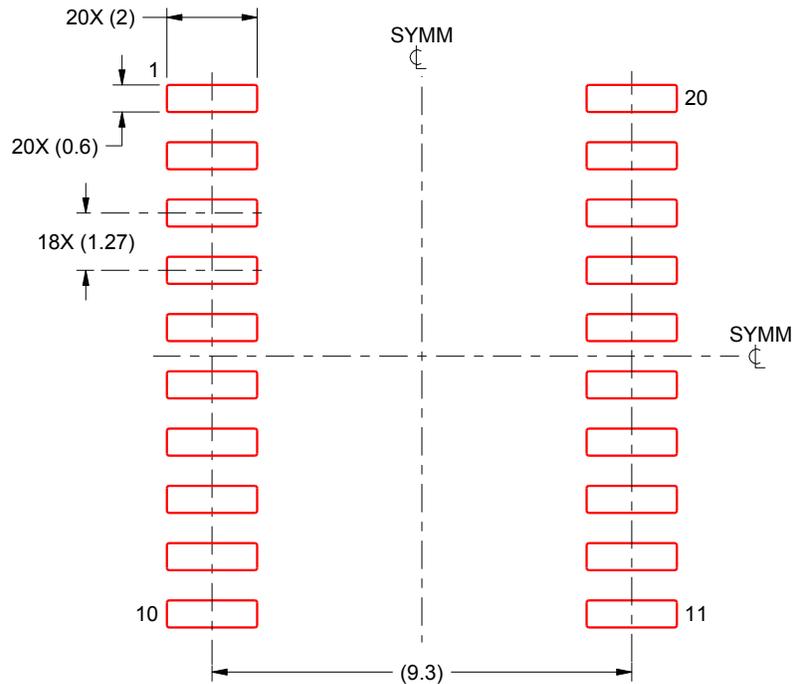
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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